GE VERNOVA

# MiCOM P40 Agile

## P443

**Technical Manual**
**Distance Protection IED**

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# CHAPTER 1

# INTRODUCTION

## 1.1 CHAPTER OVERVIEW

This chapter provides some general information about the technical manual and an introduction to the device(s) described in this technical manual.

This chapter contains the following sections:

Chapter Overview 2
Disclaimer 3
Product Scope 5
Features and Functions 8
Logic Diagrams 11
Functional Overview 13

## 1.2 DISCLAIMER

It is the responsibility of the user to verify and validate the suitability of all GE Grid Automation products. This equipment must be used within its design limits. The proper application including the configuration and setting of this product to suit the power system assets is the responsibility of the user, who is also required to ensure that all local or regional safety guidelines are adhered to. Incorrect application of this product could risk damage to property/the environment, personal injuries or fatalities and shall be the sole responsibility of the person/entity applying and qualifying the product for use.

The content of this document has been developed to provide guidance to properly install, configure and maintain this product for its intended applications. This guidance is not intended to cover every possible contingency that may arise during commissioning, operation, service, or maintenance activities. Should you encounter any circumstances not clearly addressed in this document, please contact your local GE service site.

The information contained in this document is subject to change without notice.

**IT IS THE SOLE RESPONSIBILITY OF THE USER TO SECURE THEIR NETWORK AND ASSOCIATED DEVICES AGAINST CYBER SECURITY INTRUSIONS OR ATTACKS. GE GRID AUTOMATION AND ITS AFFILIATES ARE NOT LIABLE FOR ANY DAMAGES AND/OR LOSSES ARISING FROM OR RELATED TO SUCH SECURITY INTRUSION OR ATTACKS.**

### 1.2.1 TARGET AUDIENCE

This manual is aimed towards all professionals charged with installing, commissioning, maintaining, troubleshooting, or operating any of the products within the specified product range. This includes installation and commissioning personnel as well as engineers who will be responsible for operating the product.

The level at which this manual is written assumes that installation and commissioning engineers have knowledge of handling electronic equipment. Also, system and protection engineers have a thorough knowledge of protection systems and associated equipment.

### 1.2.2 TYPOGRAPHICAL CONVENTIONS

The following typographical conventions are used throughout this manual.

- The names for special keys appear in capital letters.
  For example: ENTER
- When describing software applications, menu items, buttons, labels etc as they appear on the screen are written in bold type.
  For example: Select **Save** from the file menu.
- Filenames and paths use the courier font
  For example: `Example\File.text`
- Special terminology is written with leading capitals
  For example: Sensitive Earth Fault
- If reference is made to the IED's internal settings and signals database, the menu group heading (column) text is written in upper case italics
  For example: The *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the setting cells and DDB signals are written in bold italics
  For example: The ***Language*** cell in the *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the value of a cell's content is written in the Courier font
  For example: The ***Language*** cell in the *SYSTEM DATA* column contains the value `English`

### 1.2.3 NOMENCLATURE

Due to the technical nature of this manual, many special terms, abbreviations and acronyms are used throughout the manual. Some of these terms are well-known industry-specific terms while others may be special product-specific terms used by GE Vernova. The first instance of any acronym or term used in a particular chapter is explained. In addition, a separate glossary is available on the GE Vernova website, or from the GE Vernova contact centre.

We would like to highlight the following changes of nomenclature however:

- The word 'relay' is no longer used to describe the device itself. Instead, the device is referred to as the 'IED' (Intelligent Electronic Device), the 'device', or the 'product'. The word 'relay' is used purely to describe the electromechanical components within the device, i.e. the output relays.
- British English is used throughout this manual.
- The British term 'Earth' is used in favour of the American term 'Ground'.

### 1.2.4 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

## 1.3 PRODUCT SCOPE

The P443 has been designed for distance protection of overhead line and underground cable applications. Version M85 has been designed for both solidly grounded systems and Petersen Coil grounded systems. It is used for single circuit breaker applications. As well as distance protection, this device can also be used for 4-shot phase-segregated Autoreclose protection, and a range of standard current, voltage, power and frequency backup protection applications.

The P443 is available in five variants; models A, B, C, D and Y. The difference between the variants is the amount of I/O and the type of output contacts used. These differences are summarised in the table below:

| Feature | Model A | Model B | Model C | Model D | Model Y |
|---|---|---|---|---|---|
| Number of CT Inputs | 5 | 5 | 5 | 5 | 5 |
| Number of VT inputs | 4 | 4 | 4 | 4 | 4 |
| Opto-coupled digital inputs | 16 | 24 | 16 | 24 | 32 |
| Standard relay output contacts | 24 | 32 | 16 | 16 | 32 |
| High speed high break output contacts | | | 4 | 8 | |

### 1.3.1 PRODUCT VERSIONS

This product belongs to the P40L family. Although this technical manual is specific to this product, it is useful to know where the product fits into the family and to describe the evolution path of the entire product family. The following diagram attempts to do this:

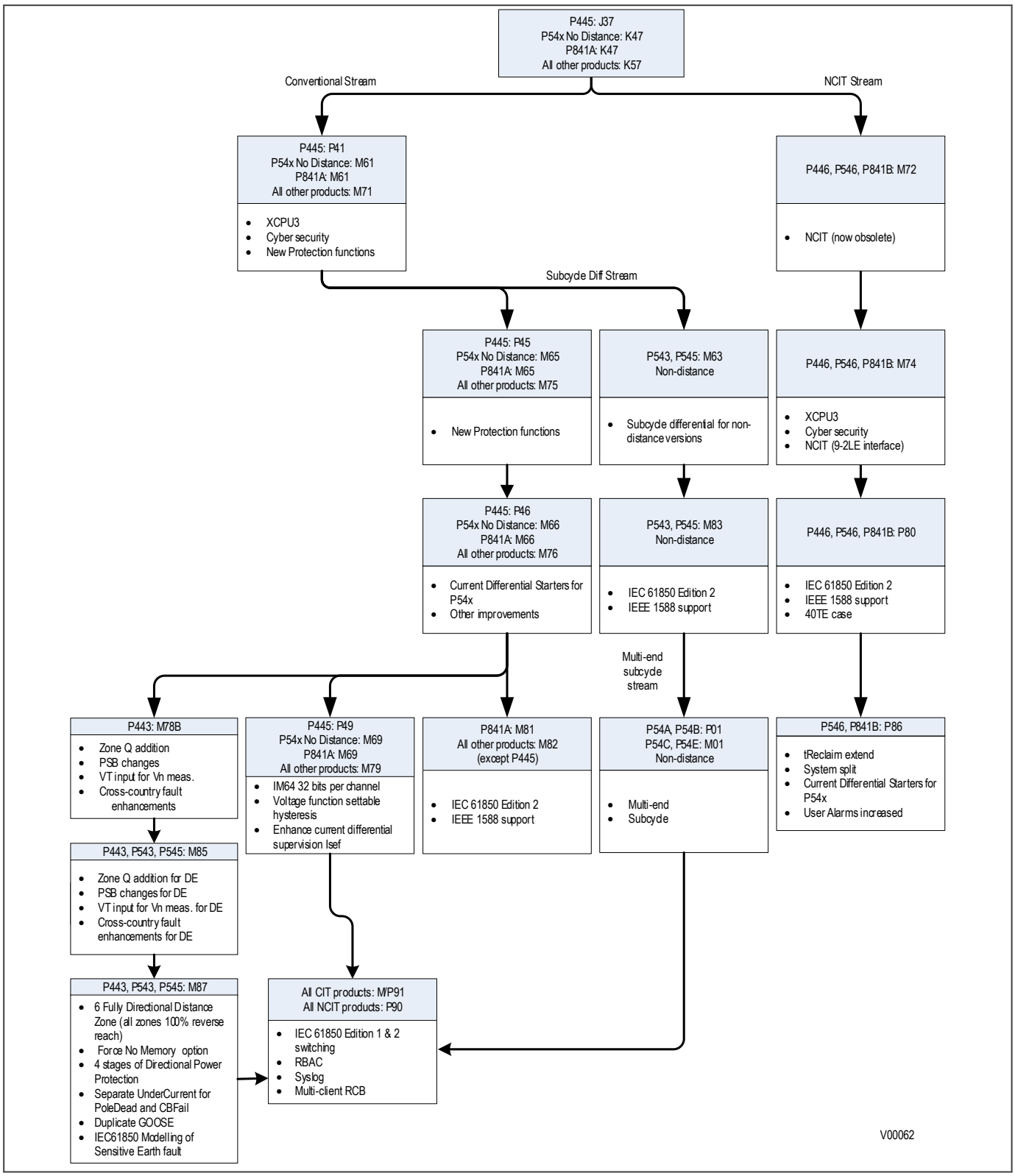



**Figure 1: P40L family - version evolution**

## 1.3.2 ORDERING OPTIONS

All current models and variants for this product are defined in an interactive spreadsheet called the Cortec. This is available on the company website.

Alternatively, you can obtain it via the Contact Centre at:

GA.support@gevernova.com

A copy of the Cortec is also supplied as a static table in the Appendices of this document. However, it should only be used for guidance as it provides a snapshot of the interactive data taken at the time of publication.

# 1.4 FEATURES AND FUNCTIONS

## 1.4.1 DISTANCE PROTECTION FUNCTIONS

| Feature | IEC 61850 | ANSI |
|---|---|---|
| Distance zones, full-scheme protection (6) | DisPDIS | 21/21N |
| Phase characteristic (Mho and quadrilateral) | | |
| Ground characteristic (Mho and quadrilateral) | | |
| Zone 1 and Zone 4 (Forward or Reverse) | | |
| Zones 2, 3, P and Q (Forward or Reverse or Offset) | | |
| CVT transient overreach elimination | | |
| Load blinder | | |
| Easy setting mode | | |
| Communication-aided schemes, PUTT, POTT, Blocking, Weak Infeed | DisPSCH | 85 |
| Accelerated tripping - loss of load and Z1 extension | | |
| Switch on to fault and trip on reclose - elements for fast fault clearance on breaker closure | SofPSOF/ TorPSOF | 50SOTF/27SOTF |
| Power swing blocking | PsbRPSB | 68 |
| Directional earth fault (DEF) unit protection | | 67N |
| Out of step | OstRPSB | 78 |
| Delta directional comparison - fast channel schemes operating on fault generated superimposed quantities | | 78DCB/78DCUB |
| Mutual compensation (for fault locator and distance zones) | | |
| Cross-country fault detection | | |
| InterMiCOM$^{64}$ teleprotection for direct device-to-device communication (optional) | | |

## 1.4.2 PROTECTION FUNCTIONS

| Feature | IEC 61850 | ANSI |
|---|---|---|
| Tripping Mode (1 & 3 pole) | PTRC | |
| ABC and ACB phase rotation | | |
| Phase overcurrent, with optional directionality (4 stages) | OcpPTOC/RDIR | 50/51/67 |
| Earth/Ground overcurrent stages, with optional directionality (4 stages) | EfdPTOC/RDIR | 50N/51N/ 67N |
| Sensitive earth fault (SEF) (4 stages) | SenPTOC/RDIR | 50N/51N/67N |
| High impedance restricted earth fault (REF) | SenRefPDIF | 64 |
| Transient Earth Fault Detection (TEFD) | PTEF | |
| Negative sequence overcurrent stages, with optional directionality (4 stages) | NgcPTOC/RDIR | 67/46 |
| Broken conductor, used to detect open circuit faults | | 46 |
| Thermal overload protection | ThmPTTR | 49 |
| Phase directional power (4 stages) | PdpPDOP/PDUP | 32 |

| Feature | IEC 61850 | ANSI |
|---|---|---|
| Undervoltage protection (2 stages) | VtpPhsPTUV | 27 |
| Overvoltage protection (2 stages) | VtpPhsPTOV | 59 |
| Remote overvoltage protection (2 stages) | VtpCmpPTOV | 59R |
| Residual voltage protection (2 stages) | VtpResPTOV | 59N |
| Underfrequency protection (4 stages) | FrqPTUF | 81 |
| Overfrequency protection (2 stages) | FrqPTOF | 81 |
| Rate of change of frequency protection (4 stages) | DfpPFRC | 81 |
| High speed breaker fail suitable for re-tripping and back-tripping (2 stages) | RBRF | 50BF |
| Current Transformer supervision | | 46 |
| Voltage transformer supervision | | 47/27 |
| Auto-reclose (4 shots) | RREC | 79 |
| Check synchronisation (2 stages) | RSYN | 25 |

### 1.4.3 CONTROL FUNCTIONS

| Feature | IEC 61850 | ANSI |
|---|---|---|
| Watchdog contacts | | |
| Read-only mode | | |
| Function keys | FnkGGIO | |
| Programmable LEDs | LedGGIO | |
| Programmable hotkeys | | |
| Programmable allocation of digital inputs and outputs | | |
| Fully customizable menu texts | | |
| Circuit breaker control, status & condition monitoring | XCBR | 52 |
| CT supervision | | |
| VT supervision | | |
| Trip circuit and coil supervision | | |
| Control inputs | PloGGIO1 | |
| Power-up diagnostics and continuous self-monitoring | | |
| Dual rated 1A and 5A CT inputs | | |
| Alternative setting groups (4) | | |
| Graphical programmable scheme logic (PSL) | | |
| Fault locator | RFLO | |

### 1.4.4 MEASUREMENT FUNCTIONS

| Measurement Function | IEC 61850 | ANSI |
|---|---|---|
| Measurement of all instantaneous & integrated values<br>(Exact range of measurements depend on the device model) | | MET |
| Disturbance recorder for waveform capture – specified in samples per cycle | RDRE | DFR |
| Fault Records | | |

| Measurement Function | IEC 61850 | ANSI |
|---|---|---|
| Maintenance Records | | |
| Event Records/Event logging | | Event records |
| Time Stamping of Opto-inputs | Yes | Yes |

## 1.4.5 COMMUNICATION FUNCTIONS

| Feature | ANSI |
|---|---|
| NERC compliant cyber-security | |
| Front RS232 serial communication port for configuration | 16S |
| Rear serial RS485 communication port for SCADA control | 16S |
| 2 Additional rear serial communication ports for SCADA control and teleprotection (fibre and copper) (optional) | 16S |
| Ethernet communication (optional) | 16E |
| Redundant Ethernet communication (optional) | 16E |
| Courier Protocol | 16S |
| IEC 61850 edition 1 or edition 2 (optional) | 16E |
| IEC 60870-5-103 (optional) | 16S |
| DNP3.0 over serial link (optional) | 16S |
| SNMP | 16E |
| IRIG-B time synchronisation (optional) | CLK |
| IEEE 1588 PTP (Edition 2 devices only) | |

## 1.5 LOGIC DIAGRAMS

This technical manual contains many logic diagrams, which should help to explain the functionality of the device. Although this manual has been designed to be as specific as possible to the chosen product, it may contain diagrams, which have elements applicable to other products. If this is the case, a qualifying note will accompany the relevant part.

The logic diagrams follow a convention for the elements used, using defined colours and shapes. A key to this convention is provided below. We recommend viewing the logic diagrams in colour rather than in black and white. The electronic version of the technical manual is in colour, but the printed version may not be. If you need coloured diagrams, they can be provided on request by calling the contact centre and quoting the diagram number.

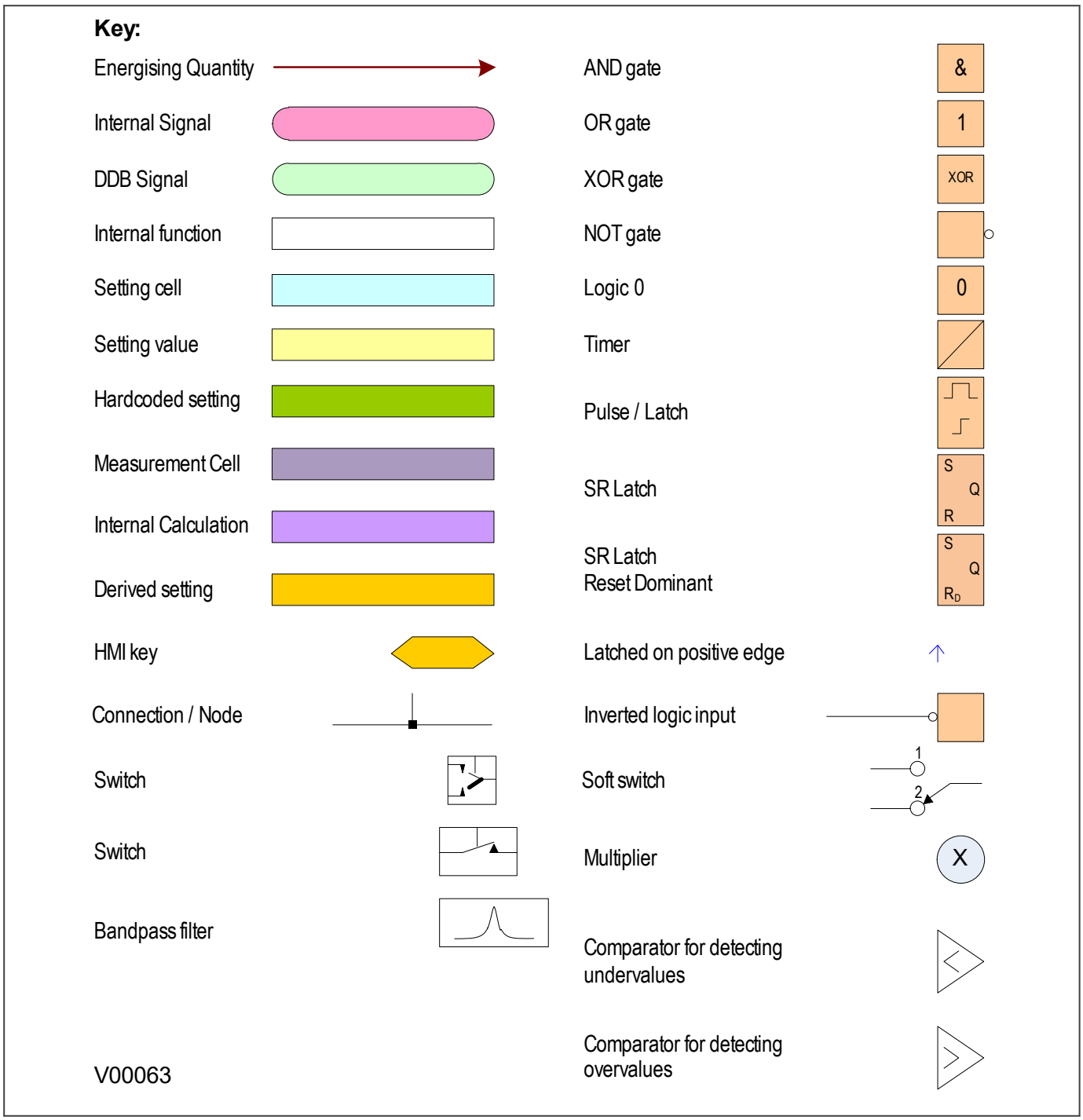



**Figure 2: Key to logic diagrams**

## 1.6 FUNCTIONAL OVERVIEW

This diagram is applicable to the P443.

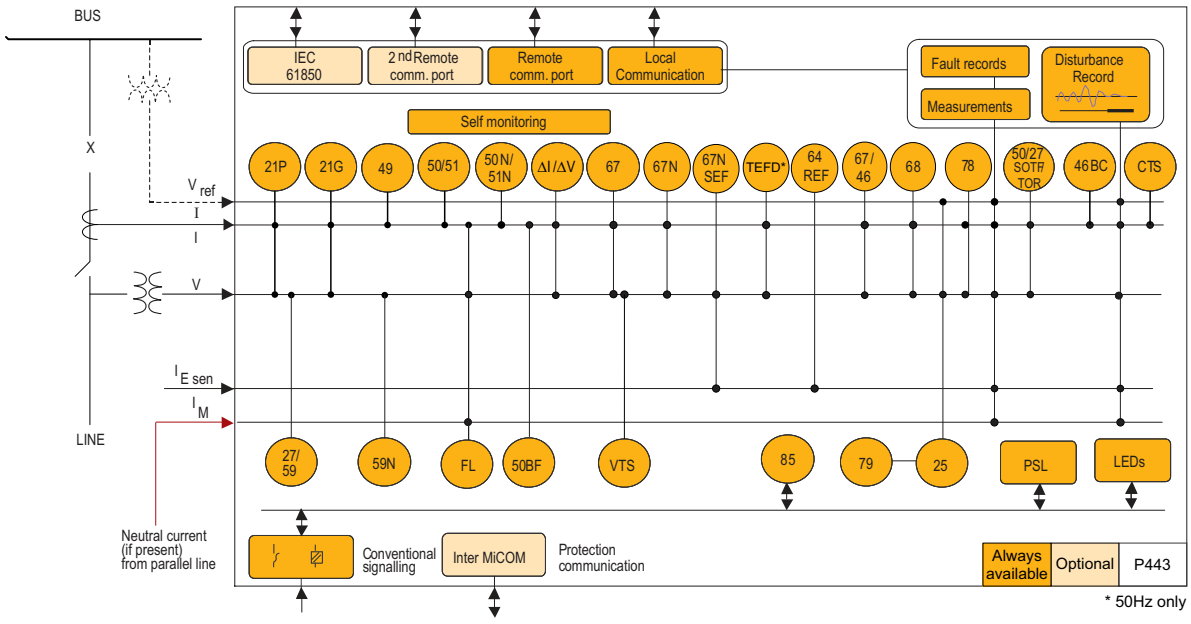



**Figure 3: Functional Overview**

# CHAPTER 2

# SAFETY INFORMATION

## 2.1 CHAPTER OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

This chapter contains the following sections:

Chapter Overview 15

Health and Safety 16

Symbols 17

Installation, Commissioning and Servicing 18

Decommissioning and Disposal 24

Regulatory Compliance 25

## 2.2 HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

## 2.3 SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.

**Caution:**
**Refer to equipment documentation. Failure to do so could result in damage to the equipment**

**Warning:**
**Risk of electric shock**

**Warning:**
**Risk of damage to eyesight**

Earth terminal. *Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.*

Protective conductor (earth) terminal

Instructions on disposal requirements

*Note:*
*The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.*

## 2.4 INSTALLATION, COMMISSIONING AND SERVICING

### 2.4.1 LIFTING HAZARDS

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

### 2.4.2 ELECTRICAL HAZARDS

**Caution:**
**All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.**

**Caution:**
**Consult the equipment documentation before installing, commissioning, or servicing the equipment.**

**Caution:**
**Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.**

**Warning:**
**Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.**

**Warning:**
**Isolate the equipment before working on the terminal strips.**

**Warning:**
**Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.**

**Caution:**
**Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.**

**Warning:**
**NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.**

**Warning:**
**Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.**

**Caution:**
**Operate the equipment within the specified electrical and environmental limits.**

**Caution:**
**Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.**

*Note:*
*Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.*

## 2.4.3 UL/CSA/CUL REQUIREMENTS

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.

**Caution:**
**Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).**

**Caution:**
**To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.**

## 2.4.4 FUSING REQUIREMENTS

**Caution:**
**Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).**

**Caution:**
**Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).**
**For P50 models, use a 1A maximum T-type fuse.**
**For P60 models, use a 4A maximum T-type fuse.**

**Caution:**
**Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.**

**Caution:**
**CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages**

## 2.4.5 EQUIPMENT CONNECTIONS

**Warning:**
**Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.**

**Caution:**
**Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.**
**Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.**

**Caution:**
**Always use insulated crimp terminations for voltage and current connections.**

**Caution:**
**Always use the correct crimp terminal and tool according to the wire size.**

**Caution:**
**Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.**

## 2.4.6 PROTECTION CLASS 1 EQUIPMENT REQUIREMENTS

**Caution:**
**Earth the equipment with the supplied PCT (Protective Conductor Terminal).**

**Caution:**
**Do not remove the PCT.**

**Caution:**
**The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.**

**Caution:**
**Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.**

**Caution:**
**The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations. For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.**

**Caution:**
**The PCT connection must have low-inductance and be as short as possible.**

**Caution:**
**All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.**

## 2.4.7 PRE-ENERGISATION CHECKLIST

**Caution:**
**Check voltage rating/polarity (rating label/equipment documentation).**

**Caution:**
**Check CT circuit rating (rating label) and integrity of connections.**

**Caution:**
**Check protective fuse or miniature circuit breaker (MCB) rating.**

**Caution:**
**Check integrity of the PCT connection.**

**Caution:**
**Check voltage and current rating of external wiring, ensuring it is appropriate for the application.**

## 2.4.8 PERIPHERAL CIRCUITRY

**Warning:**
**Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.**

*Note:*
*For most GE Vernova equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.*

**Caution:**
**Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.**

**Warning:**
**Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.**

**Warning:**
**Data communication cables with accessible screens and/or screen conductors, (including optical fibre cables with metallic elements), may create an electric shock hazard in a sub-station environment if both ends of the cable screen are not connected to the same equipotential bonded earthing system.**

**To reduce the risk of electric shock due to transferred potential hazards:**

**i. The installation shall include all necessary protection measures to ensure that no fault currents can flow in the connected cable screen conductor.**

**ii. The connected cable shall have its screen conductor connected to the protective conductor terminal (PCT) of the connected equipment at both ends. This connection may be inherent in the connectors provided on the equipment but, if there is any doubt, this must be confirmed by a continuity test.**

**iii. The protective conductor terminal (PCT) of each piece of connected equipment shall be connected directly to the same equipotential bonded earthing system.**

**iv. If, for any reason, both ends of the cable screen are not connected to the same equipotential bonded earth system, precautions must be taken to ensure that such screen connections are made safe before work is done to, or in proximity to, any such cables.**

**v. No equipment shall be connected to any download or maintenance circuits or connectors of this product except temporarily and for maintenance purposes only.**

**vi. Equipment temporarily connected to this product for maintenance purposes shall be protectively earthed (if the temporary equipment is required to be protectively earthed), directly to the same equipotential bonded earthing system as the product.**

**Warning:**
**Small Form-factor Pluggable (SFP) modules which provide copper Ethernet connections typically do not provide any additional safety isolation. Copper Ethernet SFP modules must only be used in connector positions intended for this type of connection.**

## 2.4.9 UPGRADING/SERVICING

**Warning:**
**Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.**

**Caution:**
**Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.**

## 2.5 DECOMMISSIONING AND DISPOSAL

**Caution:**
**Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.**

**Caution:**
**Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.**

## 2.6 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

### 2.6.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

### 2.6.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

### 2.6.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

### 2.6.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL us

# CHAPTER 3

# HARDWARE DESIGN

## 3.1 CHAPTER OVERVIEW

This chapter provides information about the product's hardware design.

This chapter contains the following sections:

Chapter Overview 27
Hardware Architecture 28
Mechanical Implementation 30
Front Panel 32
Rear Panel 36
Boards and Modules 38

## 3.2 HARDWARE ARCHITECTURE

The main components comprising devices based on the Px4x platform are as follows:

- The housing, consisting of a front panel and connections at the rear
- The Main processor module consisting of the main CPU (Central Processing Unit), memory and an interface to the front panel HMI (Human Machine Interface)
- A selection of plug-in boards and modules with presentation at the rear for the power supply, communication functions, digital I/O, analogue inputs, and time synchronisation connectivity

All boards and modules are connected by a parallel data and address bus, which allows the processor module to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sampled data from the input module to the CPU. These parallel and serial databuses are shown as a single interconnection module in the following figure, which shows typical modules and the flow of data between them.

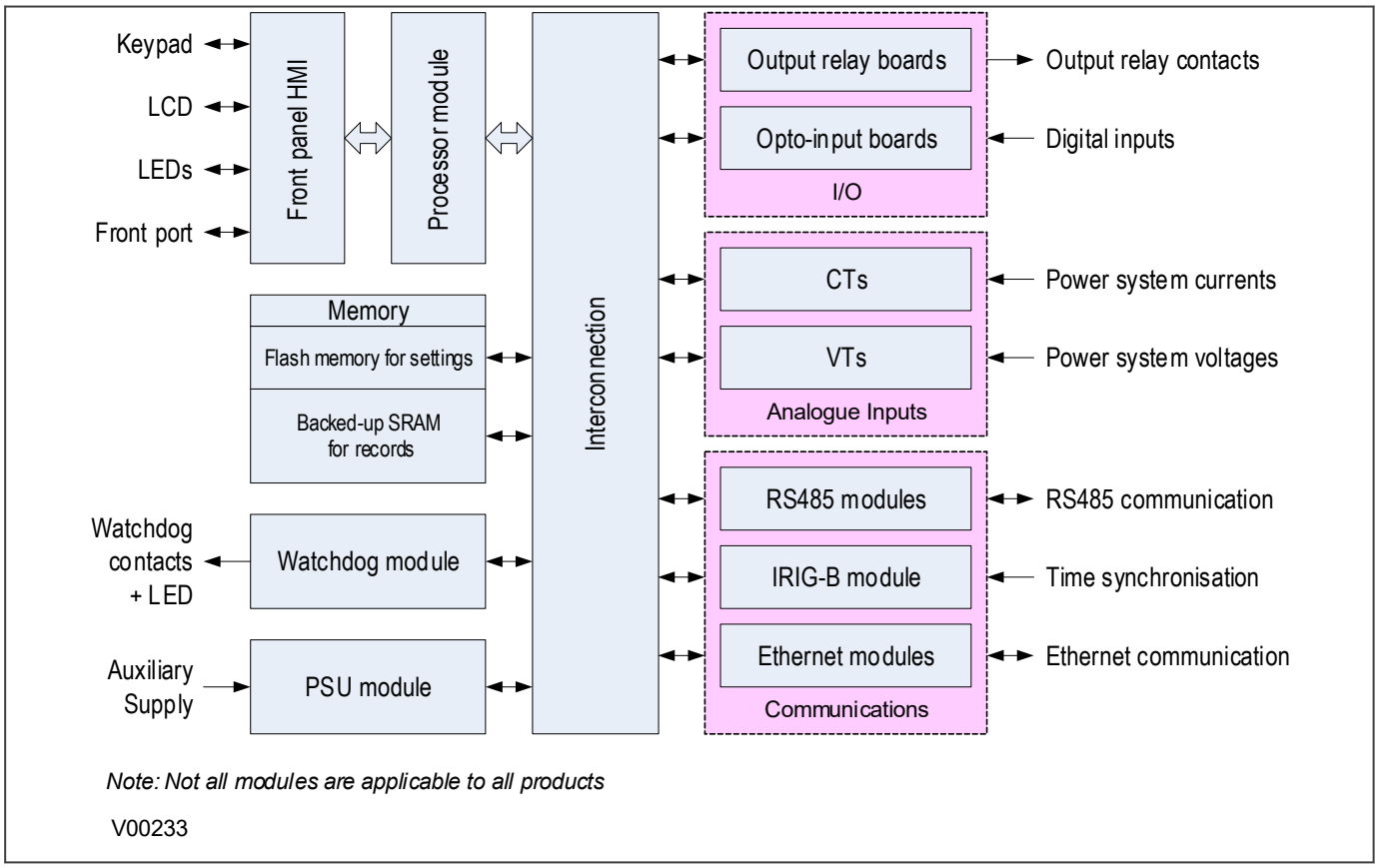



**Figure 4: Hardware architecture**

### 3.2.1 COPROCESSOR HARDWARE ARCHITECTURE

Some products are equipped with a coprocessor board for extra computing power. There are several variants of coprocessor board, depending on the required communication requirements. Some models do not need any external communication inputs, some models need inputs for current differential functionality and some models need an input for GPS time synchronisation.

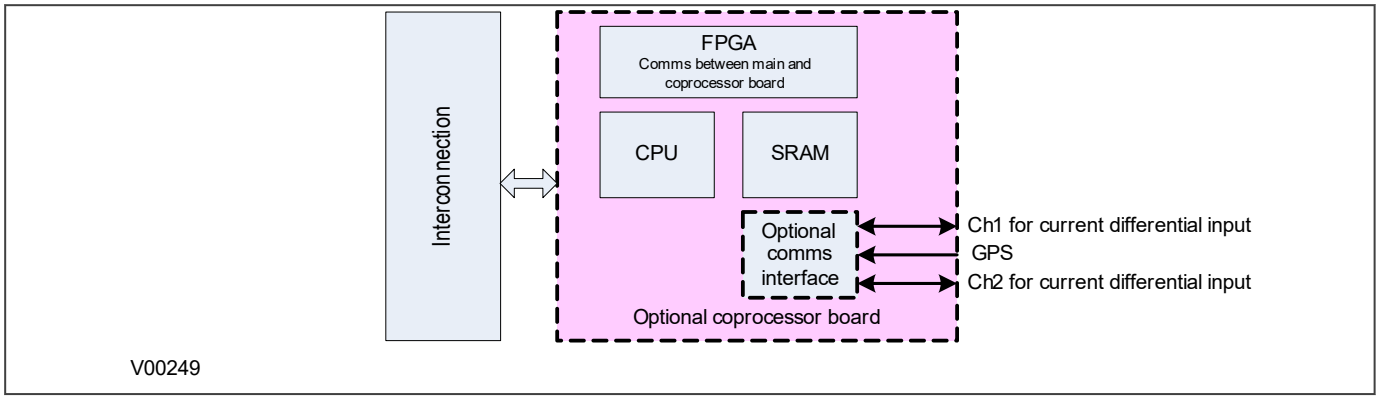



**Figure 5: Coprocessor hardware architecture**

## 3.3 MECHANICAL IMPLEMENTATION

All products based on the Px4x platform have common hardware architecture. The hardware is modular and consists of the following main parts:

- Case and terminal blocks
- Boards and modules
- Front panel

The case comprises the housing metalwork and terminal blocks at the rear. The boards fasten into the terminal blocks and are connected together by a ribbon cable. This ribbon cable connects to the processor in the front panel.

The following diagram shows an exploded view of a typical product. The diagram shown does not necessarily represent exactly the product model described in this manual.

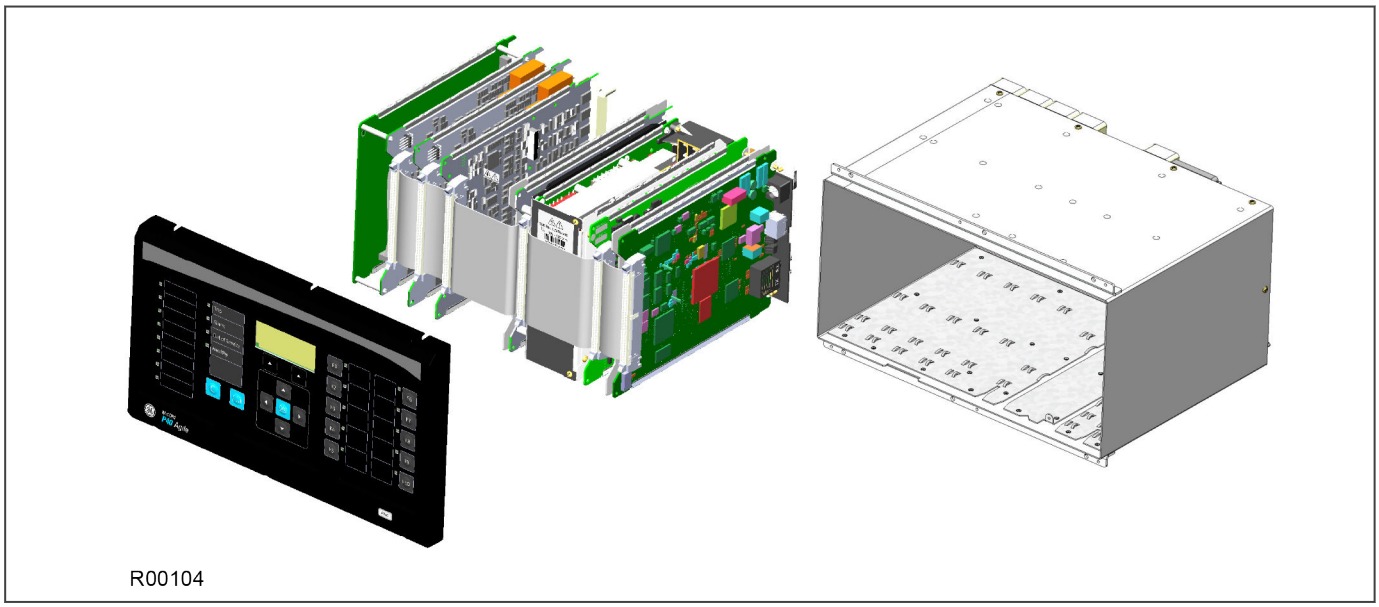



**Figure 6: Exploded view of IED**

### 3.3.1 HOUSING VARIANTS

The Px4x range of products are implemented in a range of case sizes. Case dimensions for industrial products usually follow modular measurement units based on rack sizes. These are: U for height and TE for width, where:

- 1U = 1.75 inches = 44.45 mm
- 1TE = 0.2 inches = 5.08 mm

The products are available in panel-mount or standalone versions. All products are nominally 4U high. This equates to 177.8 mm or 7 inches.

The cases are pre-finished steel with a conductive covering of aluminium and zinc. This provides good grounding at all joints, providing a low resistance path to earth that is essential for performance in the presence of external noise.

The case width depends on the product type and its hardware options. There are three different case widths for the described range of products: 40TE, 60TE and 80TE. The case dimensions and compatibility criteria are as follows:

| Case width (TE) | Case width (mm) | Case width (inches) |
|---|---|---|
| 40TE | 203.2 | 8 |
| 60TE | 304.8 | 12 |
| 80TE | 406.4 | 16 |

*Note:*
*Not all case sizes are available for all models.*

### 3.3.2 LIST OF BOARDS

The product's hardware consists of several modules drawn from a standard range. The exact specification and number of hardware modules depends on the model number and variant. Depending on the exact model, the product in question will use a selection of the following boards.

| Board | Use |
|---|---|
| Main Processor board - 40TE or smaller | Main Processor board - without support for function keys |
| Main Processor board - 60TE or larger | Main Processor board - with support for function keys |
| Power supply board - 24/54V DC | Power supply input. Accepts DC voltage between 24V and 54V |
| Power supply board - 48/125V DC | Power supply input. Accepts DC voltage between 48V and 125V |
| Power supply board - 110/250V DC | Power supply input. Accepts DC voltage between 110V and 125V |
| Transformer board | Contains the voltage and current transformers |
| Input board | Contains the A/D conversion circuitry |
| Input board with opto-inputs | Contains the A/D conversion circuitry + 8 digital opto-inputs |
| Output relay output board | Standard output relay board |
| High-break output relay board | Output relay board with high breaking capacity relays |
| IRIG-B board - modulated input | Interface board for modulated IRIG-B timing signal |
| IRIG-B board - demodulated input | Interface board for demodulated IRIG-B timing signal |
| Fibre board | Interface board for fibre-based RS485 connection |
| Fibre board + IRIG-B | Interface board for fibre-based RS485 connection + demodulated IRIG-B |
| 2nd rear communications board | Interface board for RS232 / RS485 connections |
| 2nd rear communications board with IRIG-B input | Interface board for RS232 / RS485 + IRIG-B connections |
| Redundant Ethernet RSTP + PRP + HSR + Failover universal IRIG-B | 2 ST duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with onboard universal IRIG-B (Hardware option R) |
| Redundant Ethernet RSTP + PRP + HSR + Failover universal IRIG-B | 2 RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B (Hardware option S) |
| Single Ethernet RSTP + PRP + HSR + Failover universal IRIG-B | Single Ethernet port running RSTP + PRP + HSR + Failover (one copper, RJ45 one ST multi-mode fibre optic), with on-board universal IRIG-B (Hardware option T) |
| Single Ethernet, universal IRIG-B, IEEE1588 | Single LC duplex Ethernet port (one LC multi-mode fibre optic) with universal IRIG-B (Hardware option U) |
| Redundant Ethernet RSTP + PRP + HSR + Failover universal IRIG-B | 2 RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B (Hardware option W) |
| Redundant Ethernet RSTP + PRP + HSR + Failover, universal IRIG-B | 2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B (Hardware option Y) |
| Combined opto-input/output relay board | Combined digital input/output board with opto-inputs + output relays |
| Power line carrier board | Power line carrier board for phase comparison |
| Coprocessor board | Coprocessor board for processing special algorithms |
| Coprocessor board with on-board GPS | Coprocessor board with GPS input for time synchronisation |

# 3.4 FRONT PANEL

## 3.4.1 FRONT PANEL

Depending on the exact model and chosen options, the product will be housed in either a 40TE, 60TE or 80TE case. By way of example, the following diagram shows the front panel of a typical 60TE unit. The front panels of the products based on 40TE and 80TE cases have a lot of commonality and differ only in that the 40TE front panel does not include 10 function keys with their associated user-programmable LEDs.

R00298

**Figure 7: Front panel (60TE)**

The front panel consists of:

- Top and bottom compartments with hinged cover
- LCD display
- Keypad
- USB Type B port inside the bottom compartment
- Fixed function LEDs
- Function keys and LEDs (60TE and 80TE models)
- Programmable LEDs

### 3.4.1.1 FRONT PANEL COMPARTMENTS

The top compartment contains labels for the:

- Order code, Serial number and Test ID

*Note:*
*The Test ID on the label in the top compartment of the front panel is the serial number of the relay and consists of 6 numeric and 1 alphanumeric characters, for example 123456Z. The serial number is also shown in the System Data menu of the HMI. This serial number can be used to obtain the recovery password from the Contact Centre.*
*The serial number on the label in the top compartment of the front panel is the SAP manufacturing serial number and consists of 8 numeric characters, for example 37123456.*

- Current and voltage ratings

The bottom compartment contains:

- USB type B port

### 3.4.1.2 HMI PANEL

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the LCD. The LCD is a high resolution monochrome display with 16 characters by 3 lines and controllable back light.

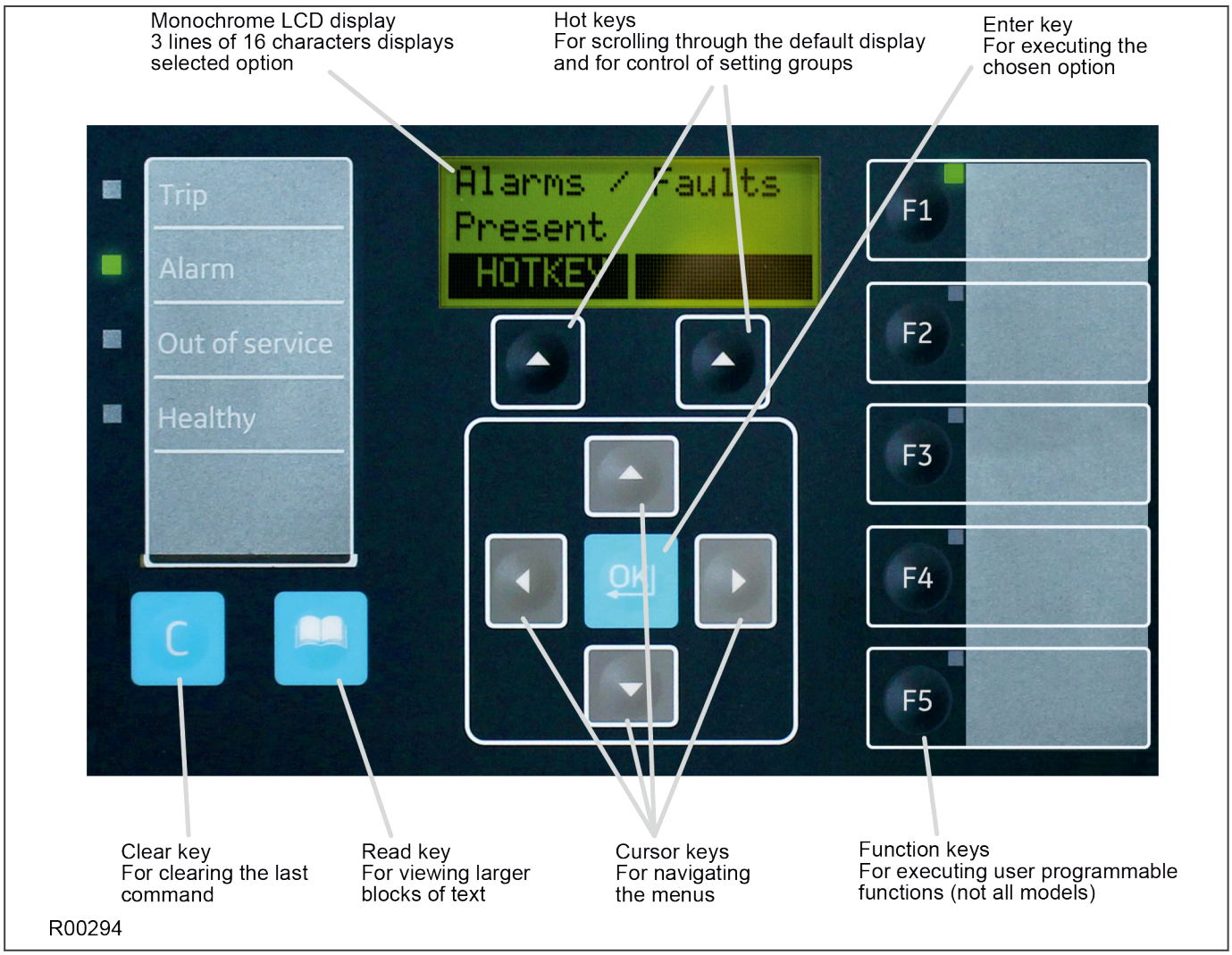
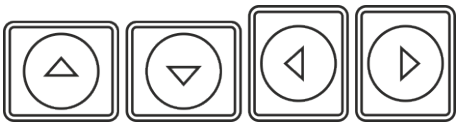



**Figure 8: HMI panel**

*Note:*
*As the LCD display has a resolution of 16 characters by 3 lines, some of the information is in a condensed mnemonic form.*

### 3.4.1.3 KEYPAD

The keypad consists of the following keys:

| | |
|---|---|
| 4 arrow keys to navigate the menus (organised around the Enter key) |  |
| An enter key for executing the chosen option | |
| A clear key for clearing the last command | |
| A read key for viewing larger blocks of text (arrow keys now used for scrolling) | |
| 2 hot keys for scrolling through the default display and for control of setting groups. These are situated directly below the LCD display. | |

#### 3.4.1.3.1 LIQUID CRYSTAL DISPLAY

The LCD is a high resolution monochrome display with 16 characters by 3 lines and controllable back light.

### 3.4.1.4 USB PORT

The USB port is situated inside the bottom compartment, and is used to communicate with a locally connected PC. It has two main purposes:

- To transfer settings information to/from the PC from/to the device.
- For downloading firmware updates and menu text editing.

The port is intended for temporary connection during testing, installation and commissioning. It is not intended to be used for permanent SCADA communications. This port supports the Courier communication protocol only. Courier is a proprietary communication protocol to allow communication with a range of protection equipment, and between the device and the Windows-based support software package.

You can connect the unit to a PC with a USB cable up to 5 m in length.

The inactivity timer for the front port is set to 15 minutes. This controls how long the unit maintains its level of password access on the front port. If no messages are received on the front port for 15 minutes, any password access level that has been enabled is cancelled.

*Note:*
*The front USB port does not support automatic extraction of event and disturbance records, although this data can be accessed manually.*

**Caution:**
**When not in use, always close the cover of the USB port to prevent contamination.**

#### 3.4.1.5 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

#### 3.4.1.6 FUNCTION KEYS

The programmable function keys are available for custom use for some models.

Factory default settings associate specific functions to these keys, but by using programmable scheme logic, you can change the default functions of these keys to fit specific needs. Adjacent to these function keys are programmable LEDs, which are usually set to be associated with their respective function keys.

#### 3.4.1.7 PROGRAMABLE LEDS

The device has a number of programmable LEDs, which can be associated with PSL-generated signals. The programmable LEDs for most models are tri-colour and can be set to RED, YELLOW or GREEN. However the programmable LEDs for some models are single-colour (red) only. The single-colour LEDs can be recognised by virtue of the fact they are large and slightly oval, whereas the tri-colour LEDs are small and round.

## 3.5 REAR PANEL

The MiCOM Px40 series uses a modular construction. Most of the internal structure consists of boards and modules that fit into slots. Some of the boards plug into terminal blocks, which are bolted onto the rear of the unit. However, some boards such as the communications boards have their own connectors. The rear panel consists of these terminal blocks plus the rears of the communications boards.

The back panel cut-outs and slot allocations vary. This depends on the product, the type of boards and the terminal blocks needed to populate the case. The following diagram shows a typical rear view of a case populated with various boards.

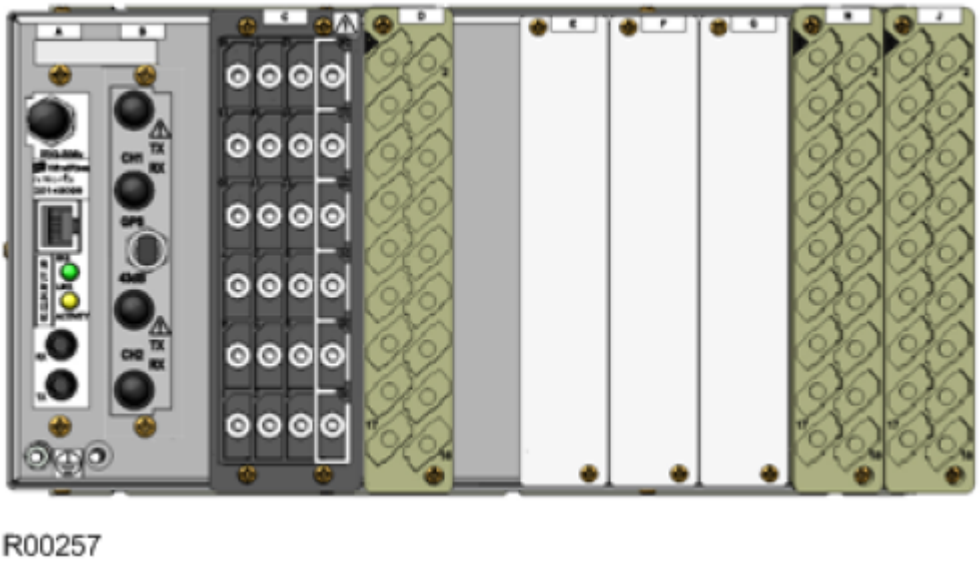



**Figure 9: Rear view of populated case**

*Note:*
*This diagram is just an example and may not show the exact product described in this manual. It also does not show the full range of available boards, just a typical arrangement.*

Not all slots are the same size. The slot width depends on the type of board or terminal block. For example, HD (heavy duty) terminal blocks, as required for the analogue inputs, require a wider slot size than MD (medium duty) terminal blocks. The board positions are not generally interchangeable. Each slot is designed to house a particular type of board. Again this is model-dependent.

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, opto-inputs, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

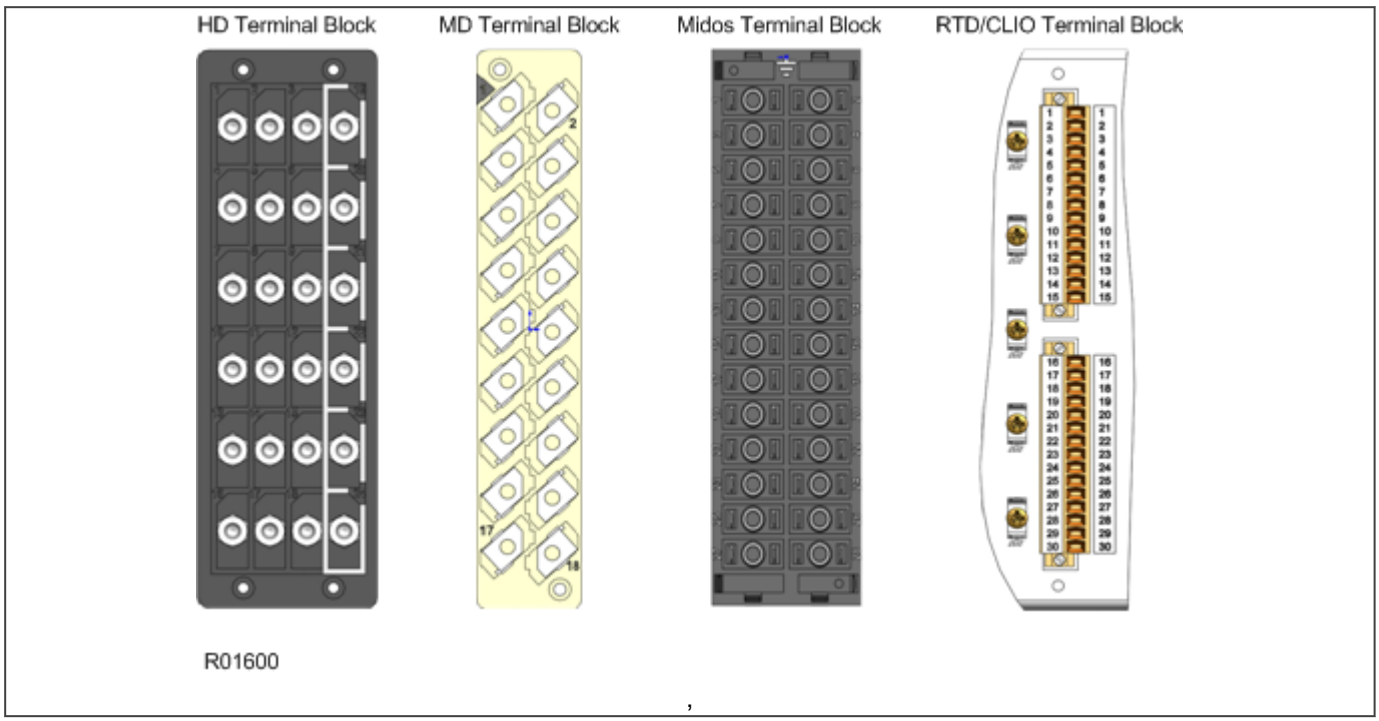



**Figure 10: Terminal block types**

*Note:*
*Not all products use all types of terminal blocks. The product described in this manual may use one or more of the above types.*

### 3.5.1 TERMINAL BLOCK INGRESS PROTECTION

IP2x shields and side cover panels are designed to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers may be attached during installation or retrofitted to upgrade existing installations - see figure below. For more information, contact your local sales office or our worldwide Contact Centre.

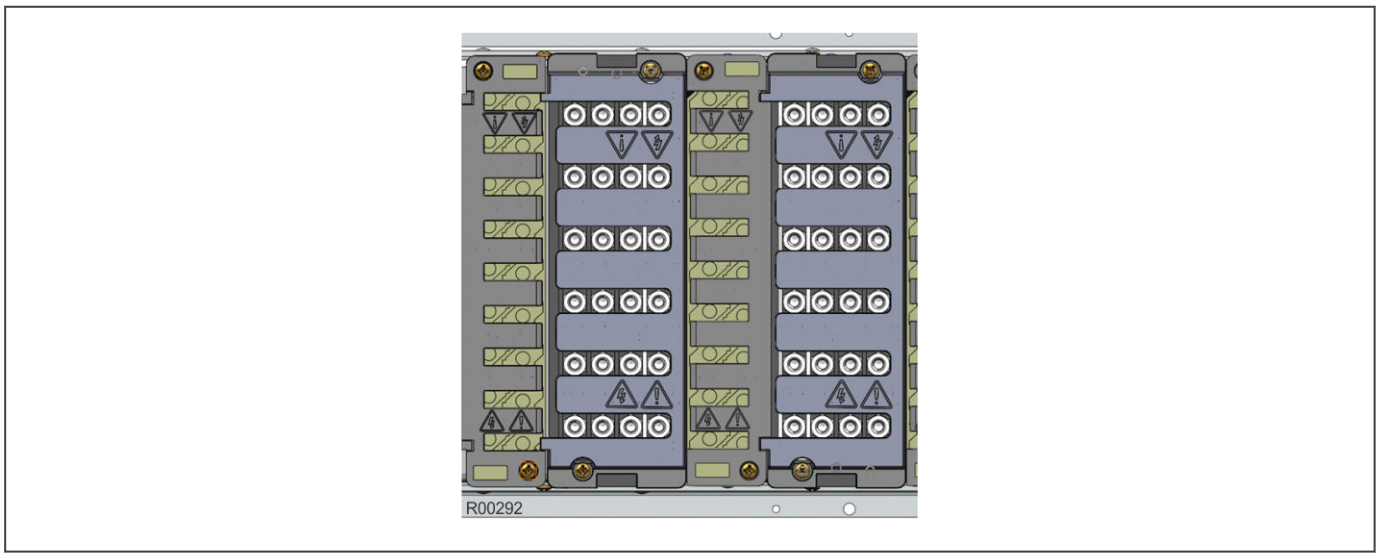



**Figure 11: Example - fitted IP2x shields (cabling omitted for clarity)**

## 3.6 BOARDS AND MODULES

Each product comprises a selection of PCBs (Printed Circuit Boards) and subassemblies, depending on the chosen configuration.

### 3.6.1 PCBS

A PCB typically consists of the components, a front connector for connecting into the main system parallel bus via a ribbon cable, and an interface to the rear. This rear interface may be:

- Directly presented to the outside world (as is the case for communication boards such as Ethernet Boards)
- Presented to a connector, which in turn connects into a terminal block bolted onto the rear of the case (as is the case for most of the other board types)

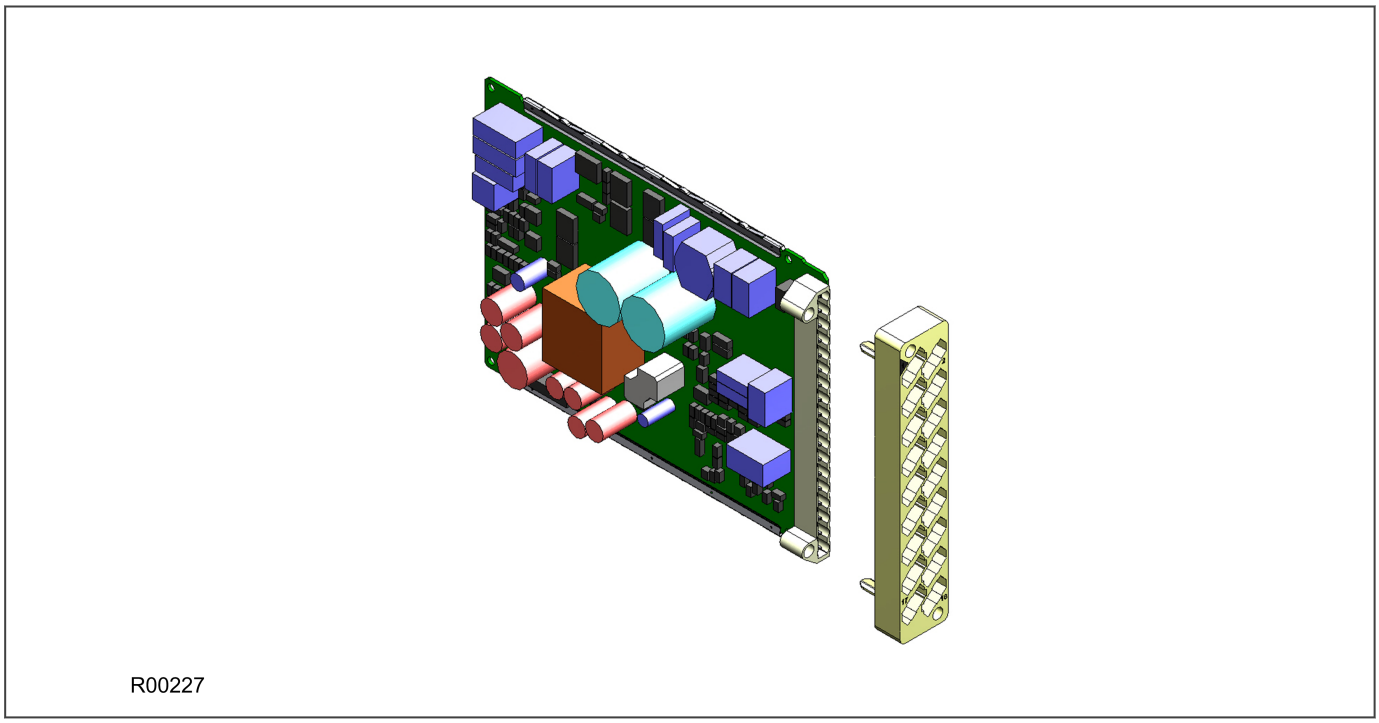



**Figure 12: Rear connection to terminal block**

### 3.6.2 SUBASSEMBLIES

A sub-assembly consists of two or more boards bolted together with spacers and connected with electrical connectors. It may also have other special requirements such as being encased in a metal housing for shielding against electromagnetic radiation.

Boards are designated by a part number beginning with ZN, whereas pre-assembled sub-assemblies are designated with a part number beginning with GN. Sub-assemblies, which are put together at the production stage, do not have a separate part number.

The products in the Px40 series typically contain two sub-assemblies:

- The power supply assembly comprising:
  - A power supply board
  - An output relay board
- The input module comprising:
  - One or more transformer boards, which contains the voltage and current transformers (partially or fully populated)
  - One or more input boards
  - Metal protective covers for EM (electromagnetic) shielding

The input module is pre-assembled and is therefore assigned a GN number, whereas the power supply module is assembled at production stage and does not therefore have an individual part number.

### 3.6.3 MAIN PROCESSOR BOARD

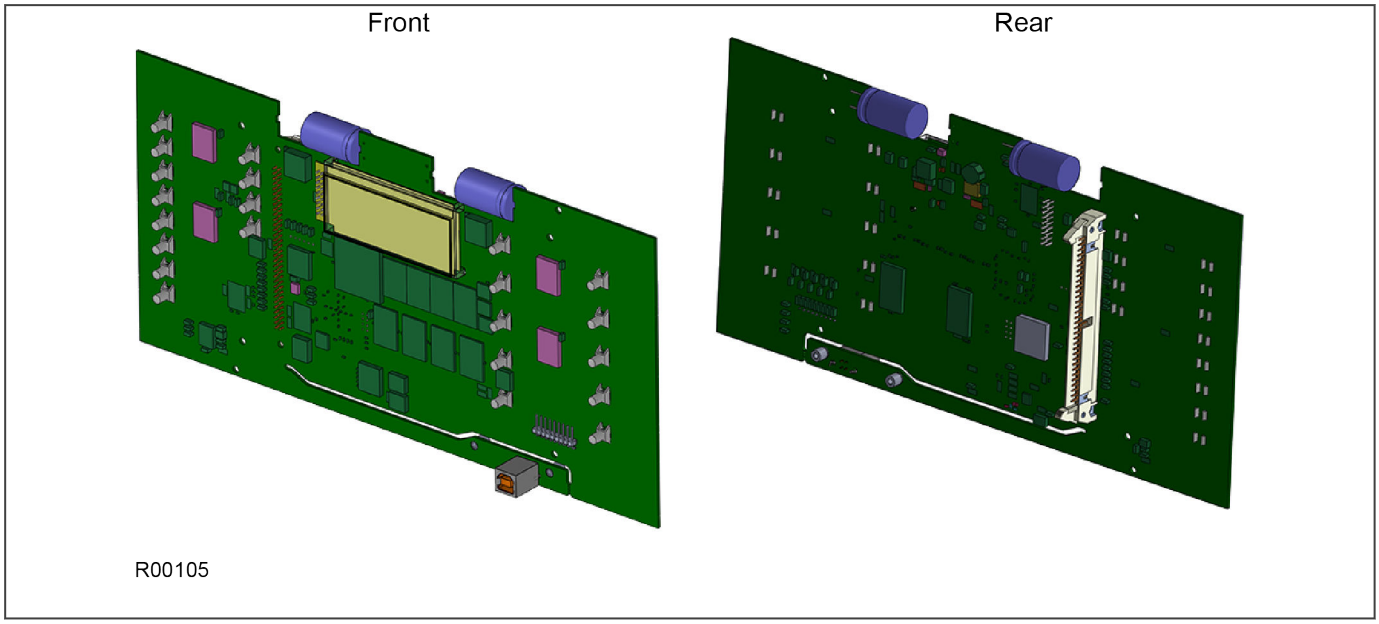



**Figure 13: Main processor board**

The main processor board performs all calculations and controls the operation of all other modules in the IED, including the data communication and user interfaces. This is the only board that does not fit into one of the slots. It resides in the front panel and connects to the rest of the system using an internal ribbon cable.

The LCD and LEDs are mounted on the processor board along with the front panel communication ports.

The memory on the main processor board is split into two categories: volatile and non-volatile. The volatile memory is fast access SRAM, used by the processor to run the software and store data during calculations. The non-volatile memory is sub-divided into two groups:

- Flash memory to store software code, text and configuration data including the present setting values.
- Supercapacitor-backed SRAM to store disturbance, event, fault and maintenance record data.

There are two board types available depending on the size of the case:

- For models in 40TE cases
- For models in 60TE cases and larger

### 3.6.4 POWER SUPPLY BOARD

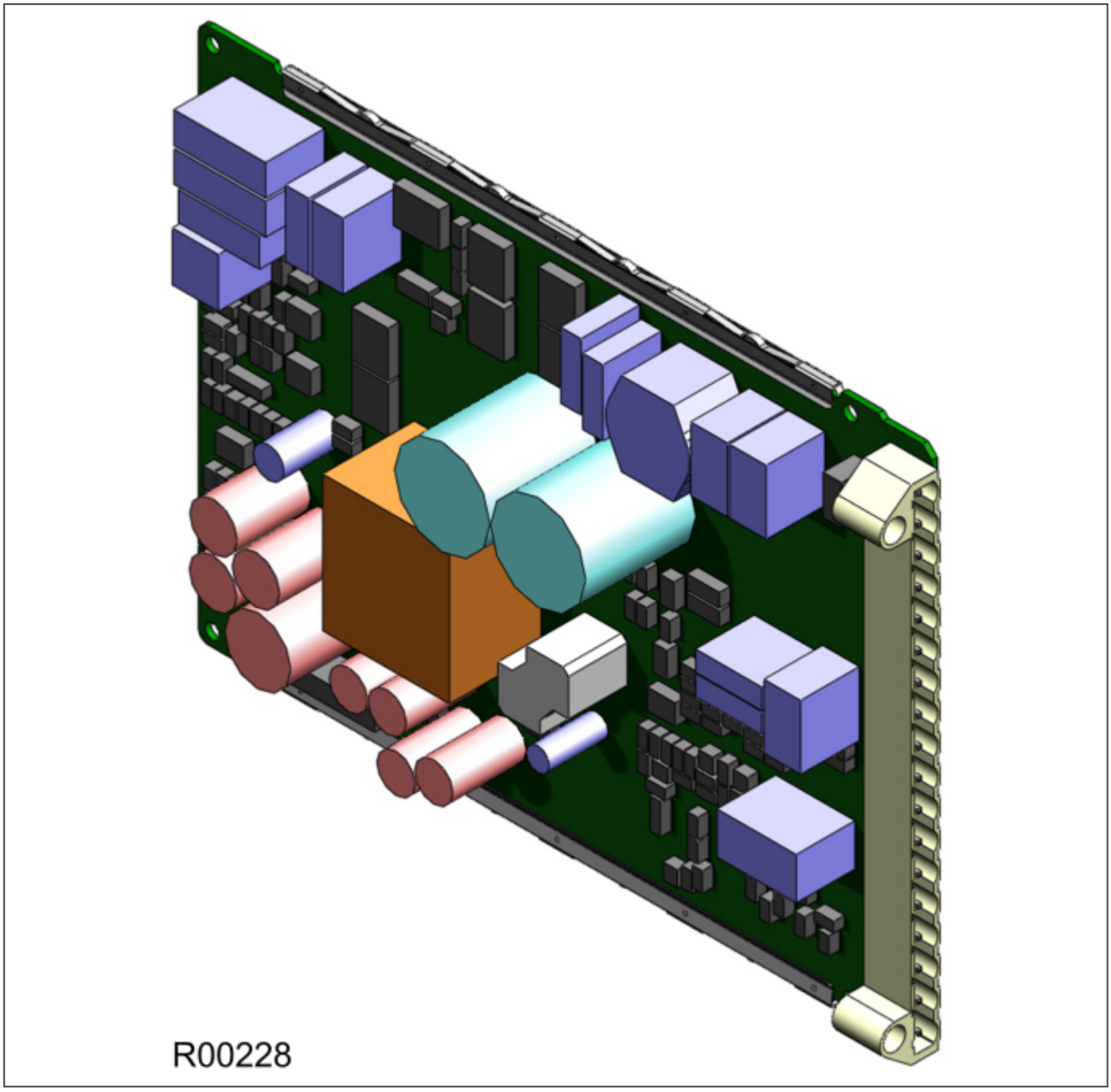



**Figure 14: Power supply board**

The power supply board provides power to the unit. One of three different configurations of the power supply board can be fitted to the unit. This is specified at the time of order and depends on the magnitude of the supply voltage that will be connected to it.

There are three board types, which support the following voltage ranges:

- 24/54 V DC
- 48/125 V DC or 40-100V AC
- 110/250 V DC or 100-240V AC

The power supply board connector plugs into a medium duty terminal block. This terminal block is always positioned on the right hand side of the unit looking from the rear.

The power supply board is usually assembled together with a relay output board to form a complete subassembly, as shown in the following diagram.

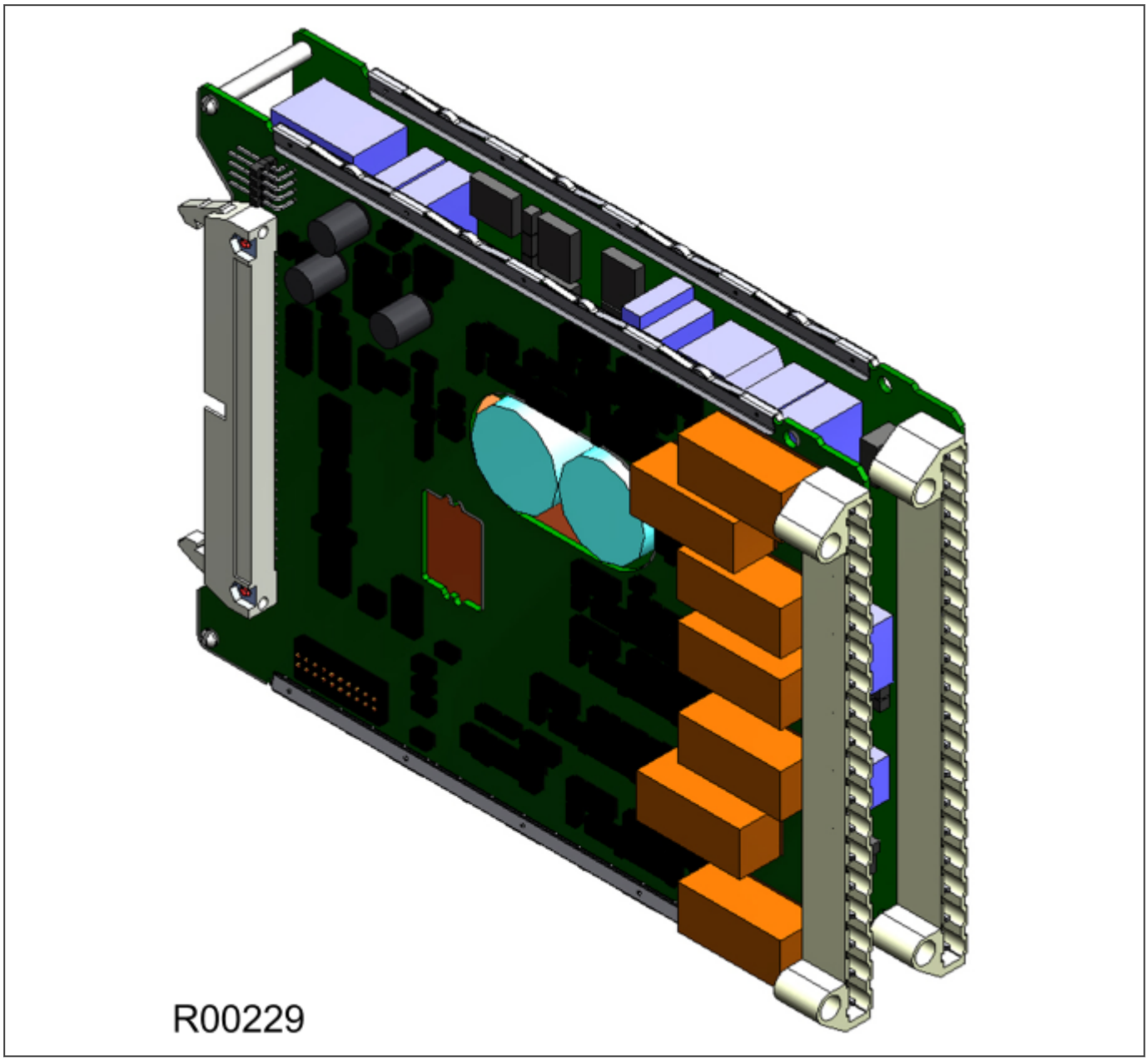



**Figure 15: Power supply assembly**

The power supply outputs are used to provide isolated power supply rails to the various modules within the unit. Three voltage levels are used by the unit's modules:

- 5.1 V for all of the digital circuits
- +/- 16 V for the analogue electronics such as on the input board
- 22 V for driving the output relay coils.

All power supply voltages, including the 0 V earth line, are distributed around the unit by the 64-way ribbon cable.

The power supply board incorporates inrush current limiting. This limits the peak inrush current to approximately 10 A.

Power is applied to pins 1 and 2 of the terminal block, where pin 1 is negative and pin 2 is positive. The pin numbers are clearly marked on the terminal block as shown in the following diagram.

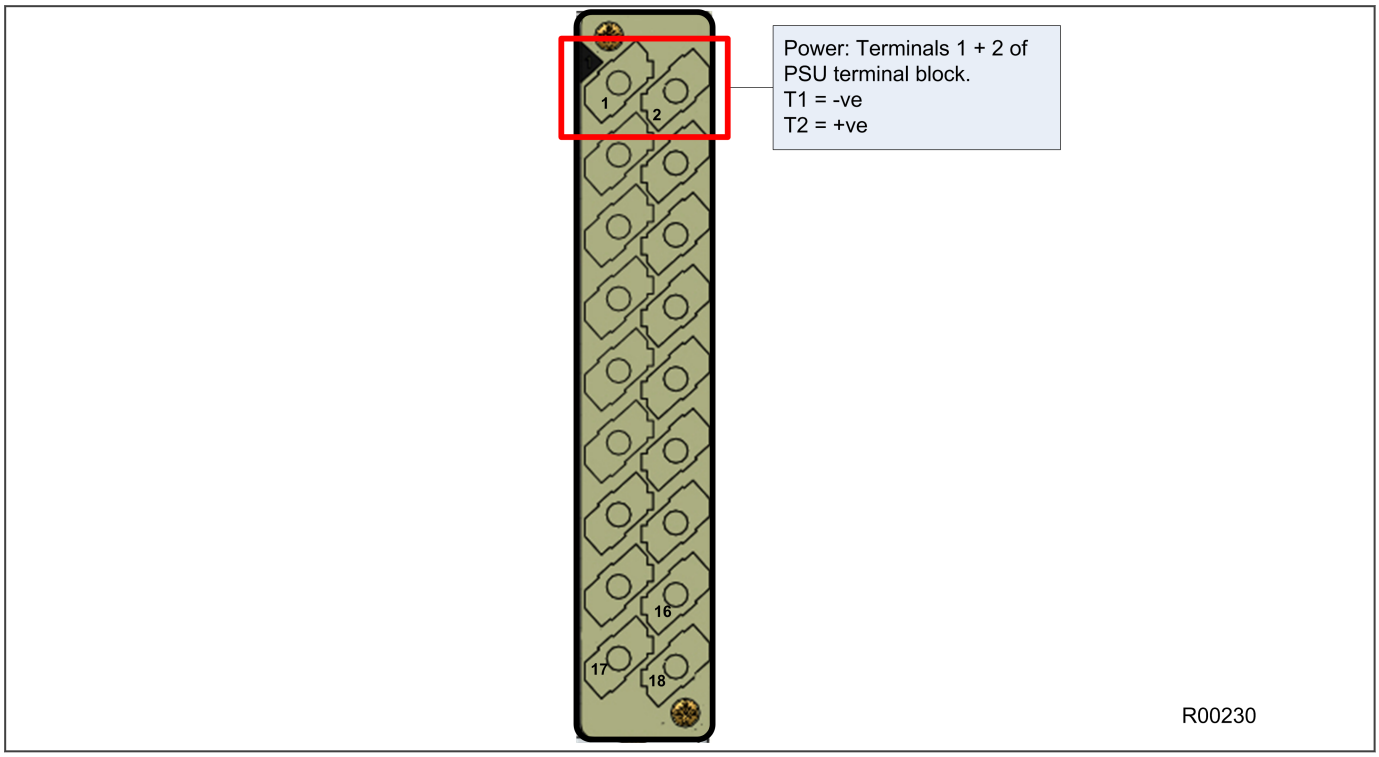



**Figure 16: Power supply terminals**

### 3.6.4.1 WATCHDOG

The Watchdog contacts are also hosted on the power supply board. The Watchdog facility provides two output relay contacts, one normally open and one normally closed. These are used to indicate the health of the device and are driven by the main processor board, which continually monitors the hardware and software when the device is in service.

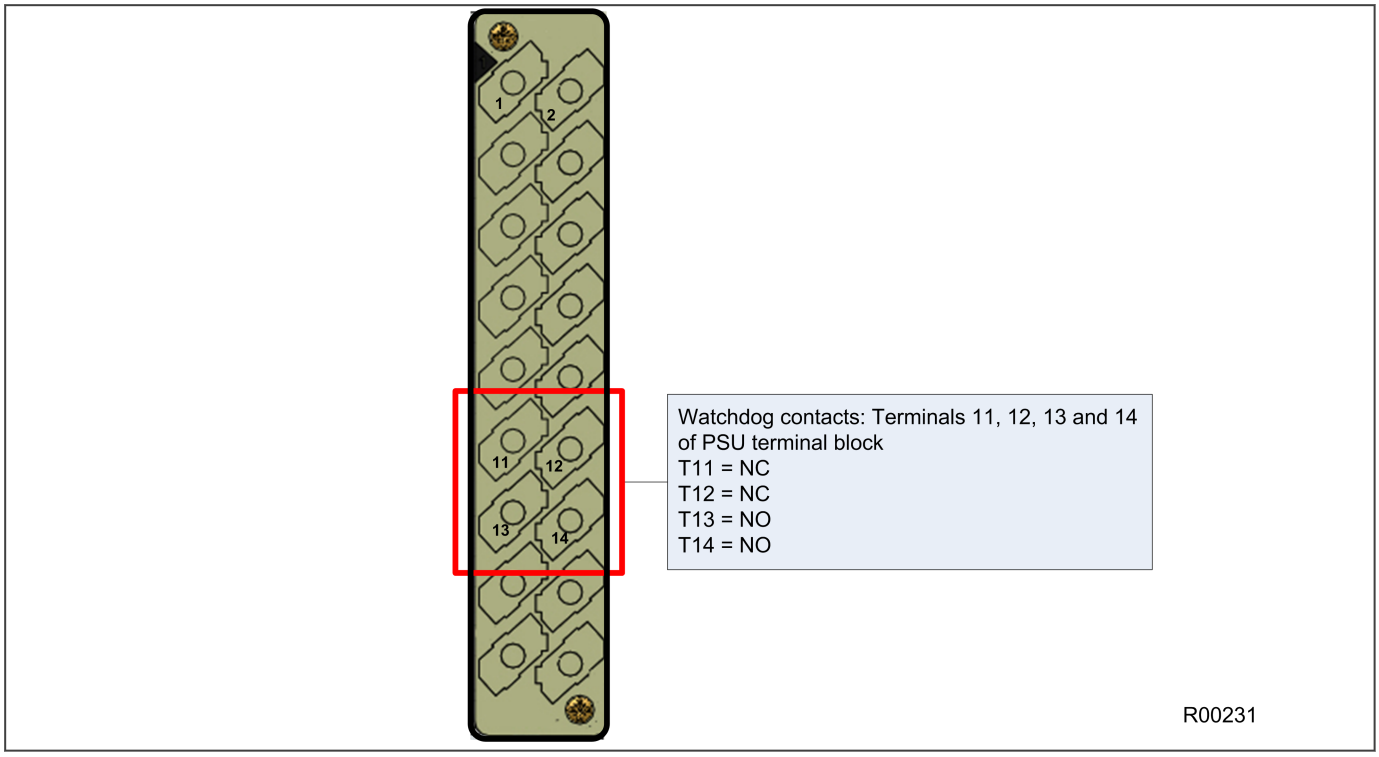



**Figure 17: Watchdog contact terminals**

### 3.6.4.2 REAR SERIAL PORT

The rear serial port (RP1) is housed on the power supply board. This is a three-terminal EIA(RS)485 serial communications port and is intended for use with a permanently wired connection to a remote control centre for SCADA communication. The interface supports half-duplex communication and provides optical isolation for the serial data being transmitted and received.

The physical connectivity is achieved using three screw terminals; two for the signal connection, and the third for the earth shield of the cable. These are located on pins 16, 17 and 18 of the power supply terminal block, which is on the far right looking from the rear. The interface can be selected between RS485 and K-bus. When the K-Bus option is selected, the two signal connections are not polarity conscious.

The polarity independent K-bus can only be used for the Courier data protocol. The polarity conscious MODBUS, IEC 60870-5-103 and DNP3.0 protocols need RS485.

The following diagram shows the rear serial port. The pin assignments are as follows:

- Pin 16: Earth shield
- Pin 17: Negative signal
- Pin 18: Positive signal

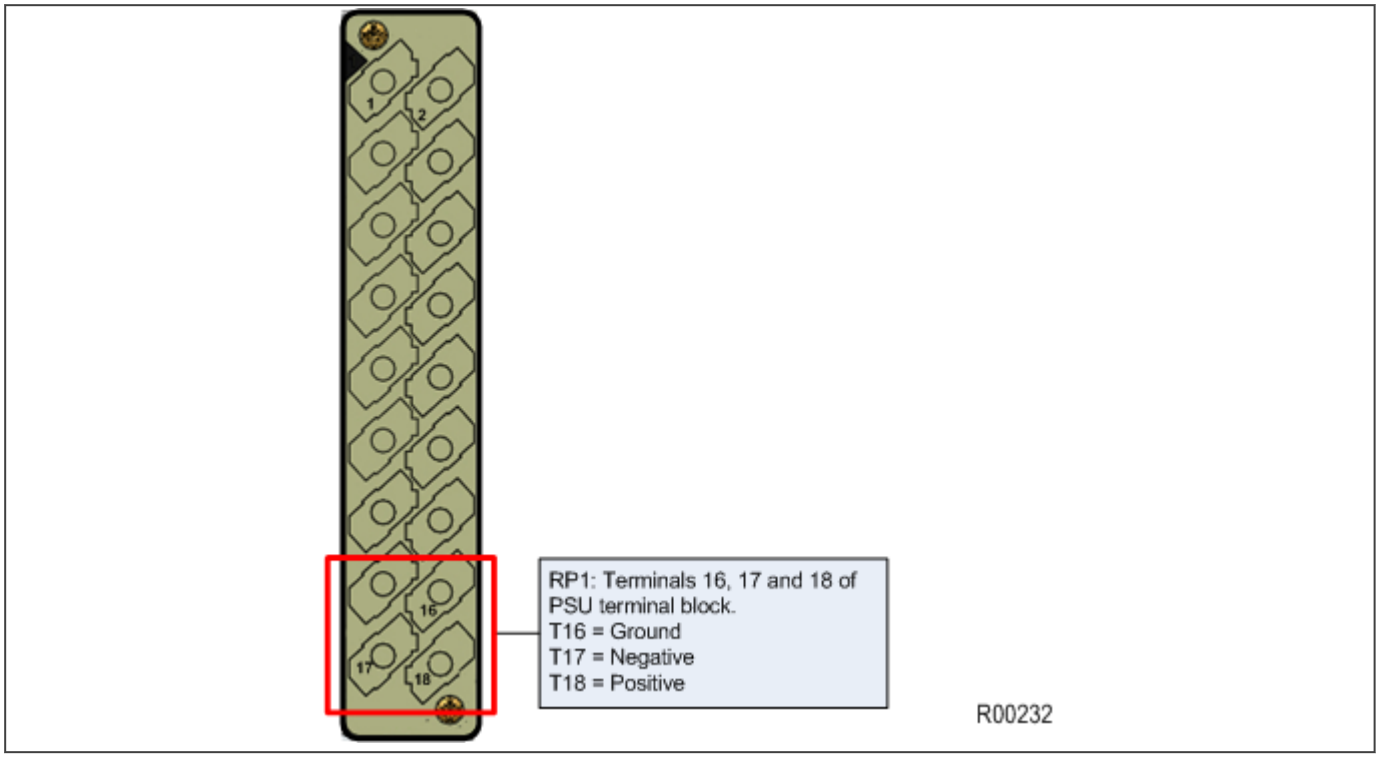



**Figure 18: Rear serial port terminals**

An additional serial port with D-type presentation is available as an optional board, if required.

## 3.6.5 INPUT MODULE - 1 TRANSFORMER BOARD

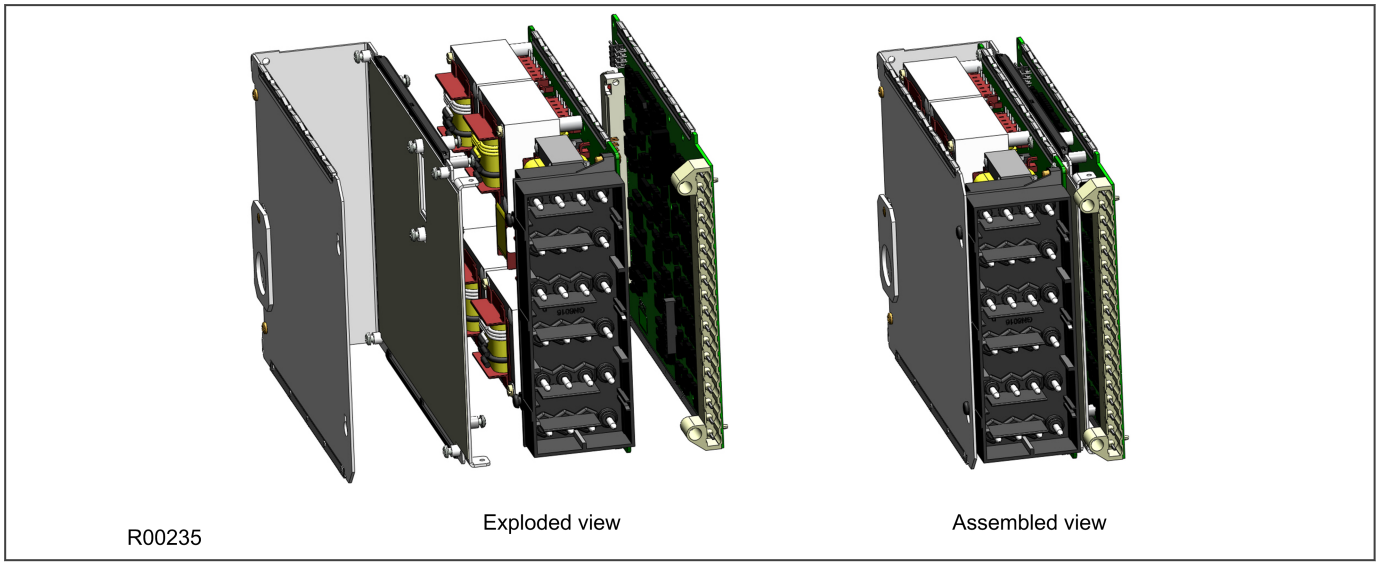



**Figure 19: Input module - 1 transformer board**

The input module consists of the main input board coupled together with an instrument transformer board. The instrument transformer board contains the voltage and current transformers, which isolate and scale the analogue input signals delivered by the system transformers. The input board contains the A/D conversion and digital processing circuitry, as well as eight digital isolated inputs (opto-inputs).

The boards are connected together physically and electrically. The module is encased in a metal housing for shielding against electromagnetic interference.

### 3.6.5.1 INPUT MODULE CIRCUIT DESCRIPTION

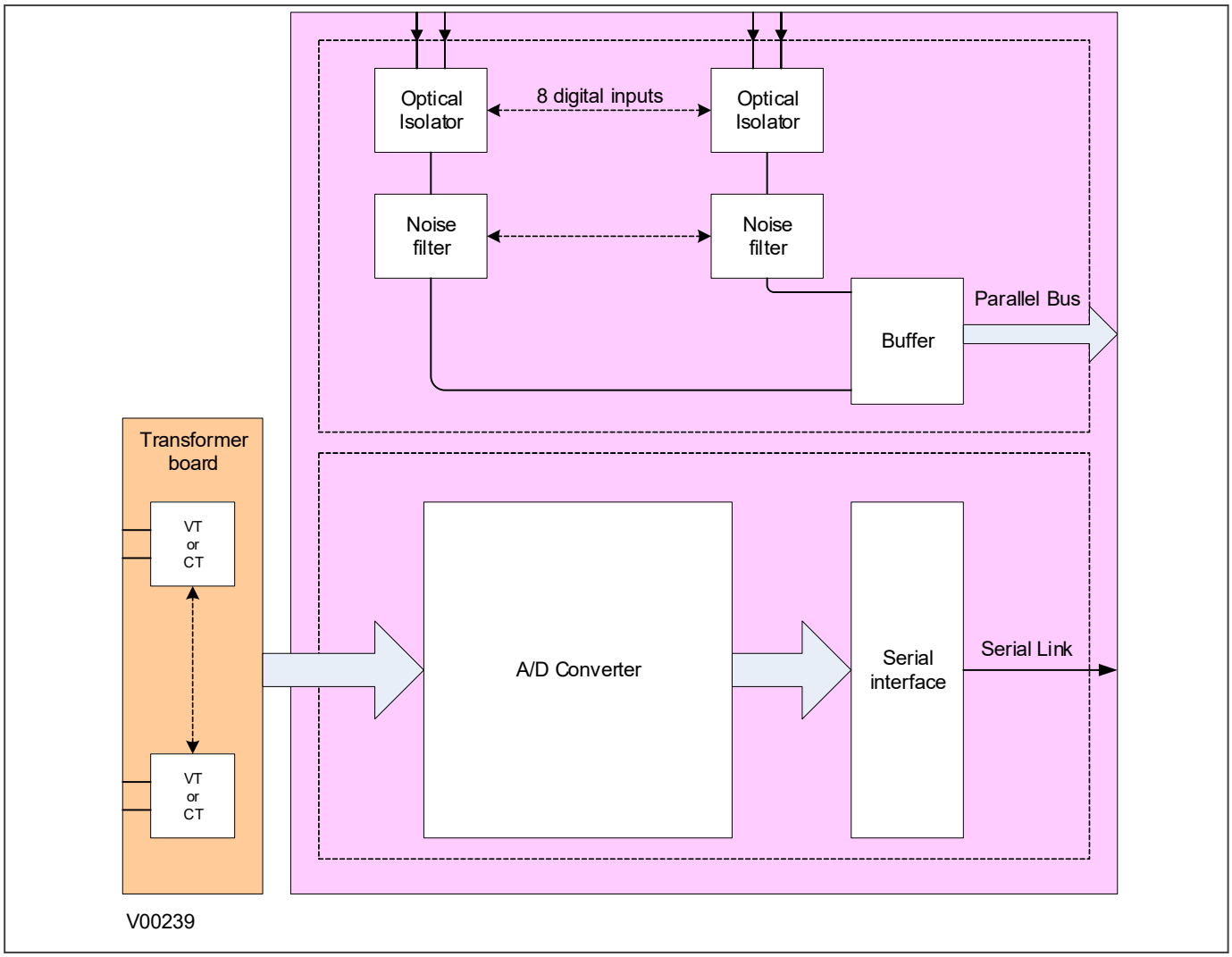



**Figure 20: Input module schematic**

#### A/D Conversion

The differential analogue inputs from the CT and VT transformers are presented to the main input board as shown. Each differential input is first converted to a single input quantity referenced to the input board's earth potential. The analogue inputs are sampled and converted to digital, then filtered to remove unwanted properties. The samples are then passed through a serial interface module which outputs data on the serial sample data bus.

The calibration coefficients are stored in non-volatile memory. These are used by the processor board to correct for any amplitude or phase errors introduced by the transformers and analogue circuitry.

#### Opto-isolated inputs

The other function of the input board is to read in the state of the digital inputs. As with the analogue inputs, the digital inputs must be electrically isolated from the power system. This is achieved by means of the 8 on-board optical isolators for connection of up to 8 digital signals. The digital signals are passed through an optional noise filter before being buffered and presented to the unit's processing boards in the form of a parallel data bus.

This selectable filtering allows the use of a pre-set filter of ½ cycle which renders the input immune to induced power-system noise on the wiring. Although this method is secure it can be slow, particularly for inter-tripping. This

can be improved by switching off the ½ cycle filter, in which case one of the following methods to reduce ac noise should be considered.

- Use double pole switching on the input
- Use screened twisted cable on the input circuit

The opto-isolated logic inputs can be configured for the nominal battery voltage of the circuit for which they are a part, allowing different voltages for different circuits such as signalling and tripping.

*Note:*
*The opto-input circuitry can be provided without the A/D circuitry as a separate board, which can provide supplementary opto-inputs.*

### 3.6.5.2 TRANSFORMER BOARD

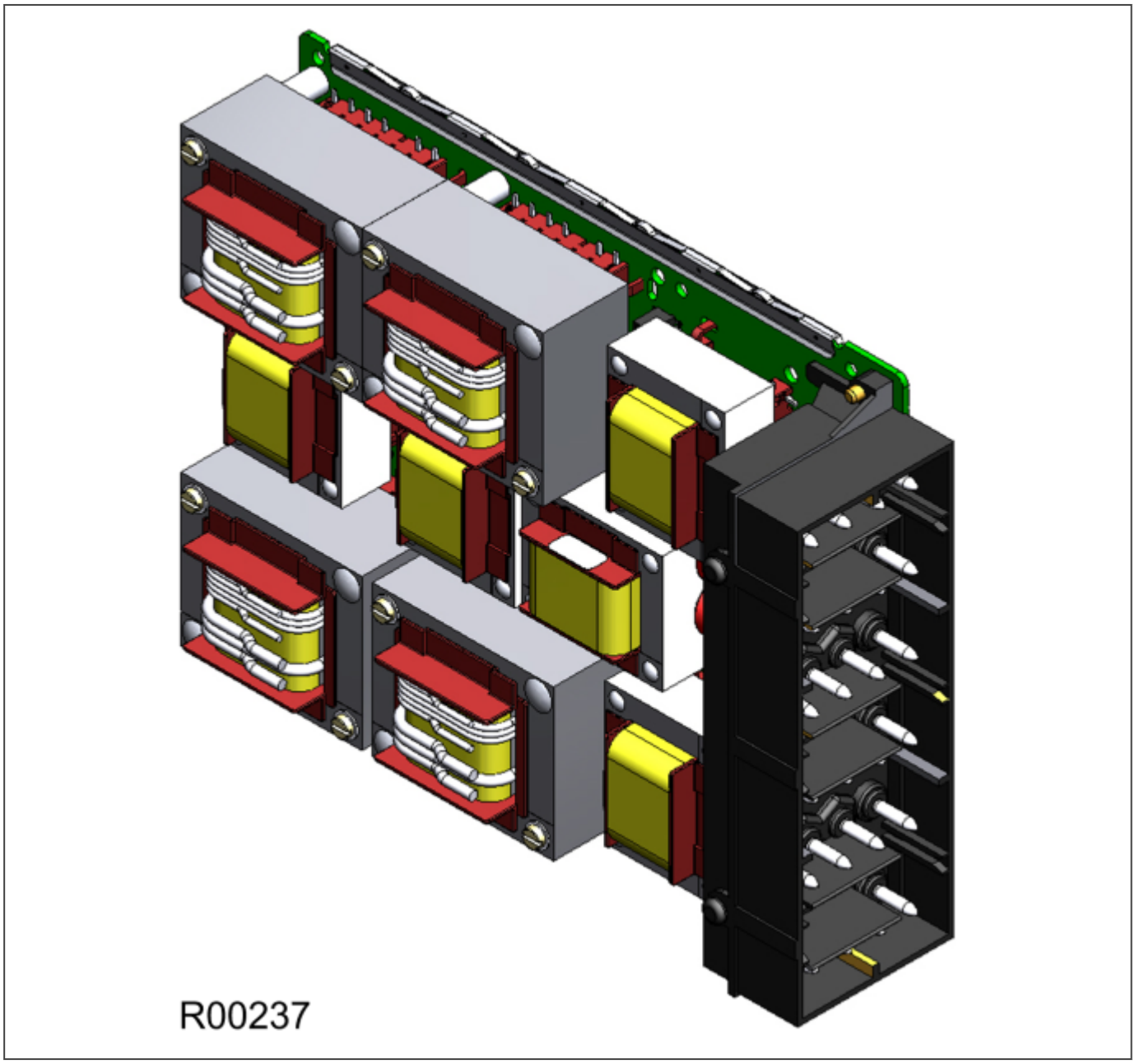



**Figure 21: Transformer board**

The transformer board hosts the current and voltage transformers. These are used to step down the currents and voltages originating from the power systems' current and voltage transformers to levels that can be used by the devices' electronic circuitry. In addition to this, the on-board CT and VT transformers provide electrical isolation between the unit and the power system.

The transformer board is connected physically and electrically to the input board to form a complete input module.

For terminal connections, please refer to the wiring diagrams.

### 3.6.5.3 INPUT BOARD

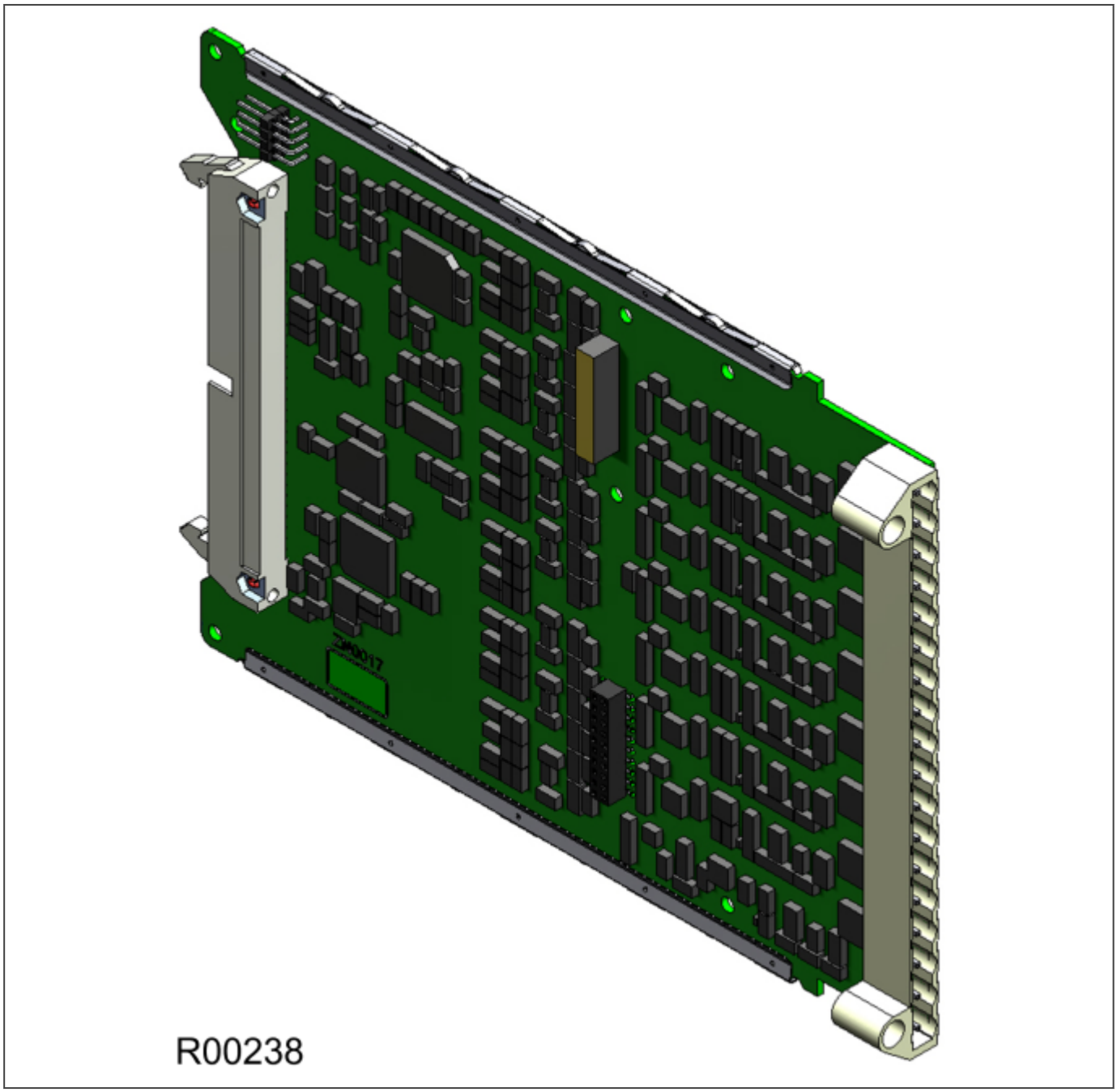



**Figure 22: Input board**

The input board is used to convert the analogue signals delivered by the current and voltage transformers into digital quantities used by the IED. This input board also has on-board opto-input circuitry, providing eight optically-isolated digital inputs and associated noise filtering and buffering. These opto-inputs are presented to the user by means of an MD terminal block, which sits adjacent to the analogue inputs HD terminal block.

The input board is connected physically and electrically to the transformer board to form a complete input module.

The terminal numbers of the opto-inputs are as follows:

| Terminal Number | Opto-input |
|---|---|
| Terminal 1 | Opto 1 -ve |
| Terminal 2 | Opto 1 +ve |
| Terminal 3 | Opto 2 -ve |
| Terminal 4 | Opto 2 +ve |
| Terminal 5 | Opto 3 -ve |
| Terminal 6 | Opto 3 +ve |
| Terminal 7 | Opto 4 -ve |
| Terminal 8 | Opto 4 +ve |
| Terminal 9 | Opto 5 -ve |
| Terminal 10 | Opto 5 +ve |
| Terminal 11 | Opto 6 -ve |
| Terminal 12 | Opto 6 +ve |
| Terminal 13 | Opto 7 –ve |
| Terminal 14 | Opto 7 +ve |
| Terminal 15 | Opto 8 –ve |
| Terminal 16 | Opto 8 +ve |
| Terminal 17 | Common |
| Terminal 18 | Common |

### 3.6.6 STANDARD OUTPUT RELAY BOARD

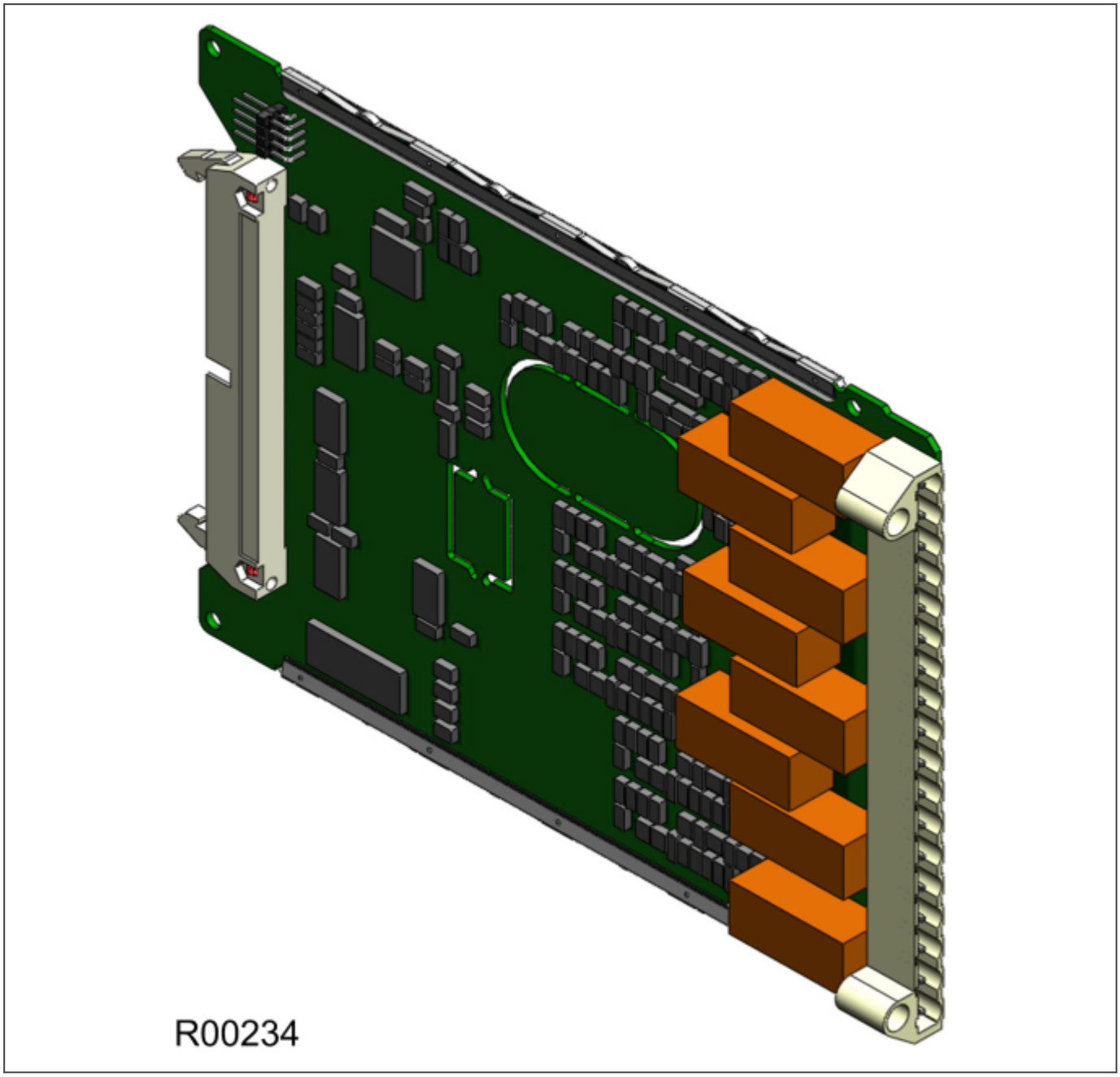



**Figure 23: Standard relay output board - 8 contacts**

This output relay board has 8 relays with 6 Normally Open contacts and 2 Changeover contacts.

The output relay board is provided together with the power supply board as a complete assembly, or independently for the purposes of relay output expansion.

There are two cut-out locations in the board. These can be removed to allow power supply components to protrude when coupling the output relay board to the power supply board. If the output relay board is to be used independently, these cut-out locations remain intact.

The terminal numbers are as follows:

| Terminal Number | Output Relay |
|---|---|
| Terminal 1 | Relay 1 NO |
| Terminal 2 | Relay 1 NO |
| Terminal 3 | Relay 2 NO |
| Terminal 4 | Relay 2 NO |
| Terminal 5 | Relay 3 NO |
| Terminal 6 | Relay 3 NO |
| Terminal 7 | Relay 4 NO |
| Terminal 8 | Relay 4 NO |
| Terminal 9 | Relay 5 NO |
| Terminal 10 | Relay 5 NO |
| Terminal 11 | Relay 6 NO |
| Terminal 12 | Relay 6 NO |
| Terminal 13 | Relay 7 changeover |
| Terminal 14 | Relay 7 changeover |
| Terminal 15 | Relay 7 common |
| Terminal 16 | Relay 8 changeover |
| Terminal 17 | Relay 8 changeover |
| Terminal 18 | Relay 8 common |

### 3.6.7 IRIG-B BOARD

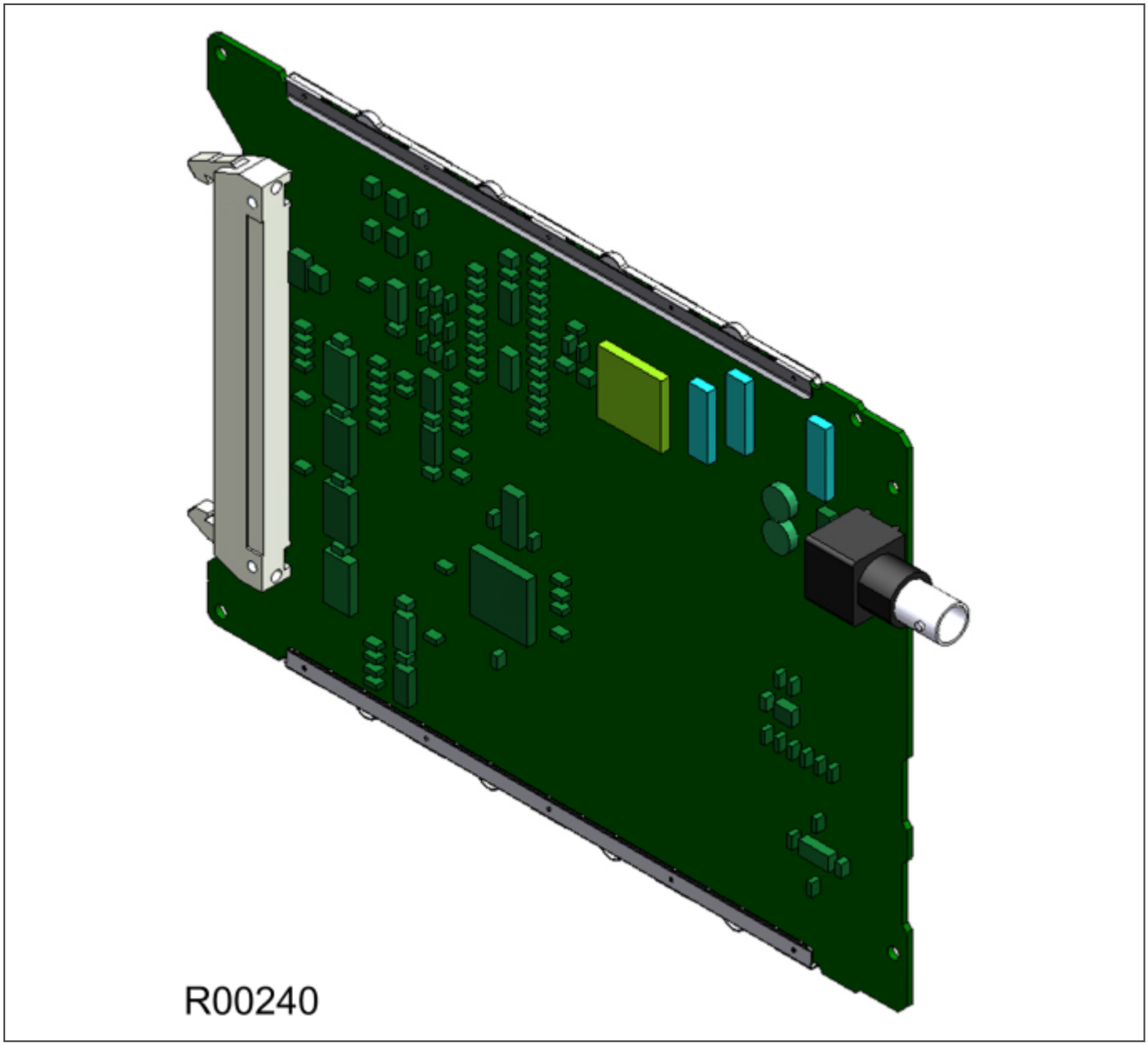



**Figure 24: IRIG-B board**

The IRIG-B board can be fitted to provide an accurate timing reference for the device. The IRIG-B signal is connected to the board via an BNC connector. The timing information is used to synchronise the IED's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for time tagging events, fault, maintenance and disturbance records.

IRIG-B interface is available in modulated or demodulated formats.

The IRIG-B facility is provided in combination with other functionality on a number of additional boards, such as:

- Fibre board with IRIG-B
- Second rear communications board with IRIG-B
- Ethernet board with IRIG-B
- Redundant Ethernet board with IRIG-B

There are three types of each of these boards; one type which accepts a modulated IRIG-B input, one type which accepts a demodulated IRIG-B input and one type which accepts a universal IRIG-B input. The order code will indicate which variant it supports.

### 3.6.8 FIBRE OPTIC BOARD

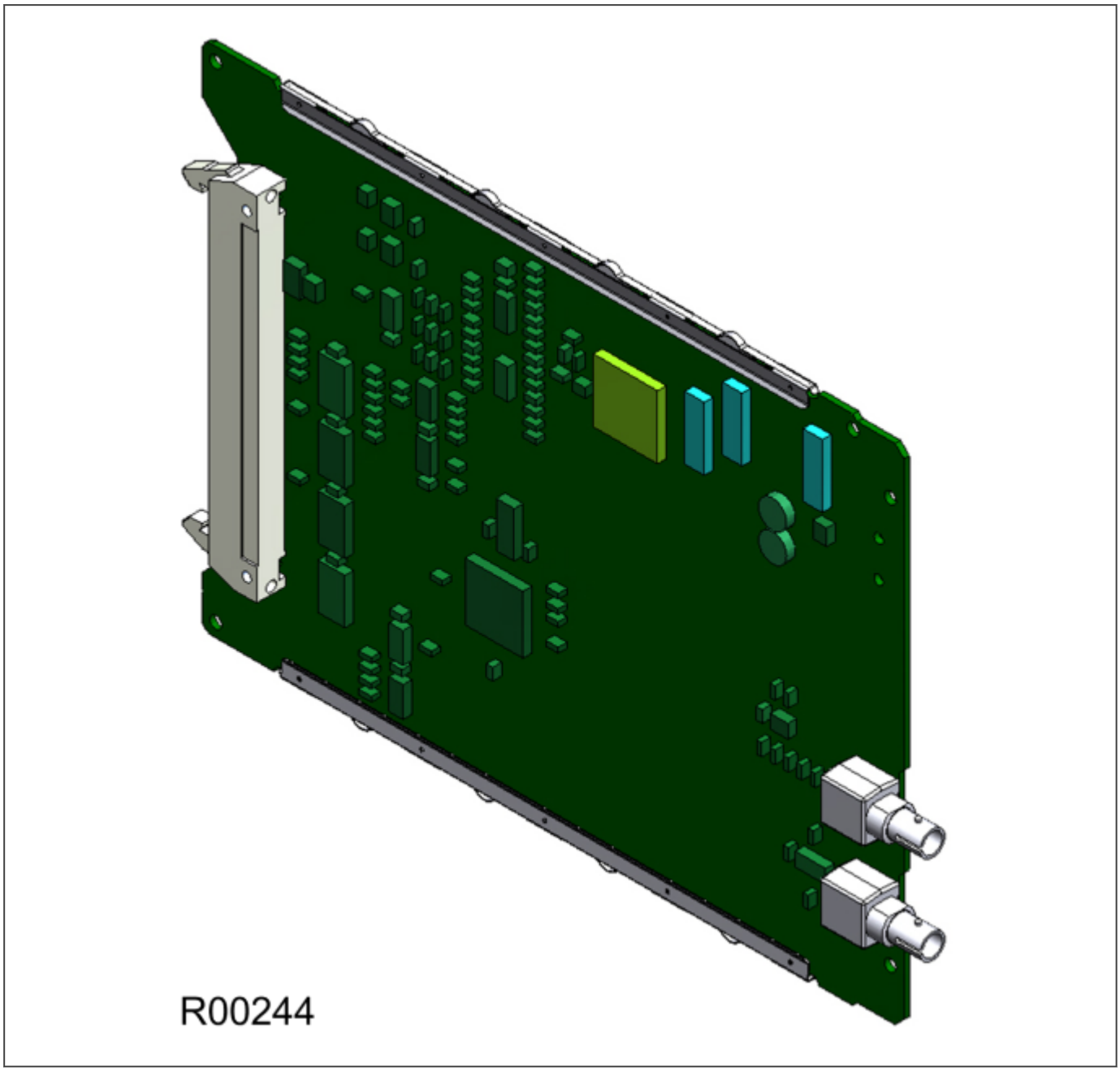



**Figure 25: Fibre optic board**

This board provides an interface for communicating with a master station. This communication link can use all compatible protocols (Courier, IEC 60870-5-103, MODBUS and DNP 3.0). It is a fibre-optic alternative to the metallic RS485 port presented on the power supply terminal block. The metallic and fibre optic ports are mutually exclusive.

The fibre optic port uses BFOC 2.5 ST connectors.

The board comes in two varieties; one with an IRIG-B input and one without:

### 3.6.9 REAR COMMUNICATION BOARD

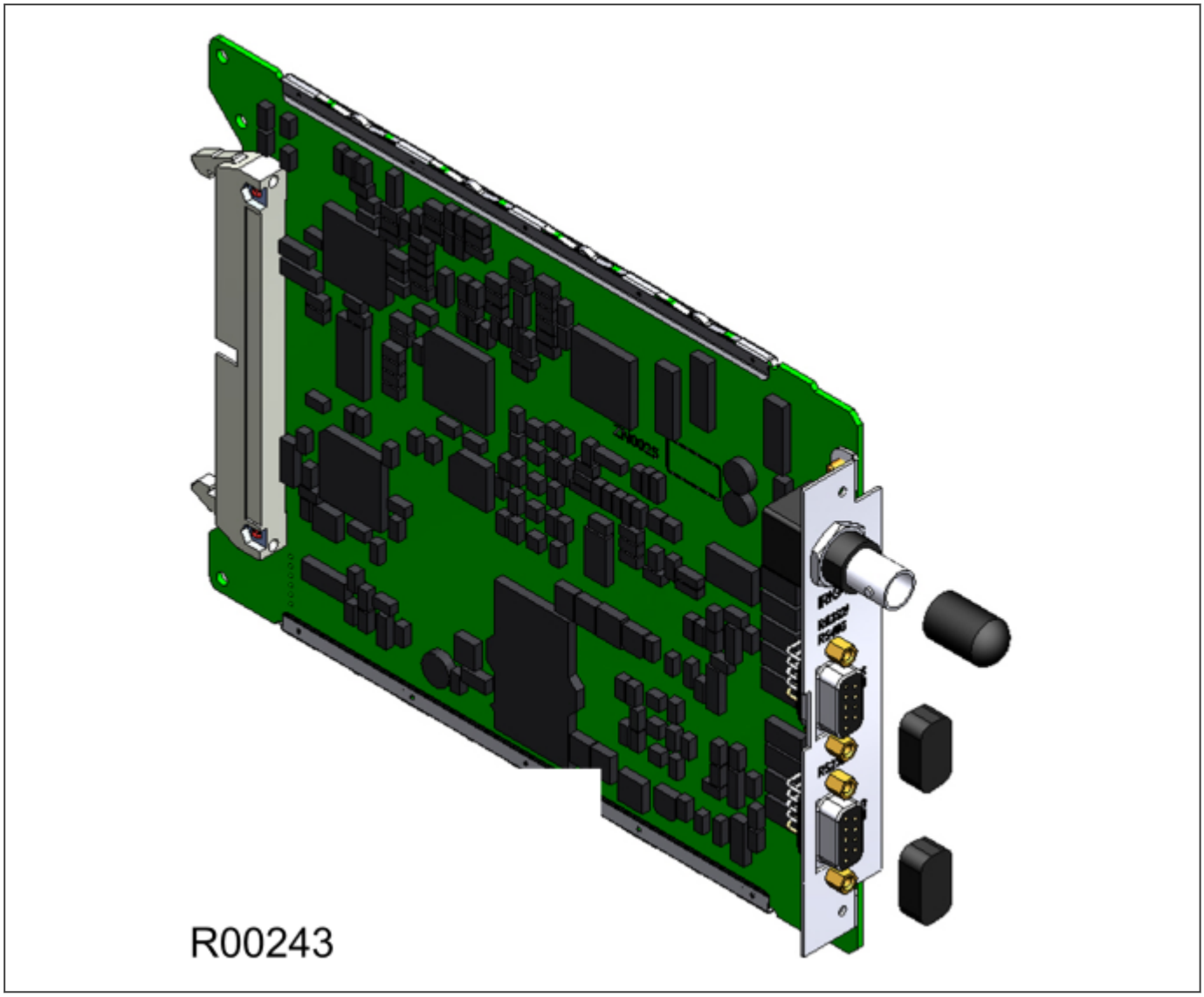



**Figure 26: Rear communication board**

The optional communications board containing the secondary communication ports provide two serial interfaces presented on 9 pin D-type connectors. These interfaces are known as SK4 and SK5. Both connectors are female connectors, but are configured as DTE ports. This means pin 2 is used to transmit information and pin 3 to receive.

SK4 can be used with RS232, RS485 and K-bus. SK5 can only be used with RS232 and is used for electrical teleprotection. The optional rear communications board and IRIG-B board are mutually exclusive since they use the same hardware slot. However, the board comes in two varieties; one with an IRIG-B input and one without.

## 3.6.10 REDUNDANT ETHERNET BOARD (HARDWARE OPTION R/S/T)

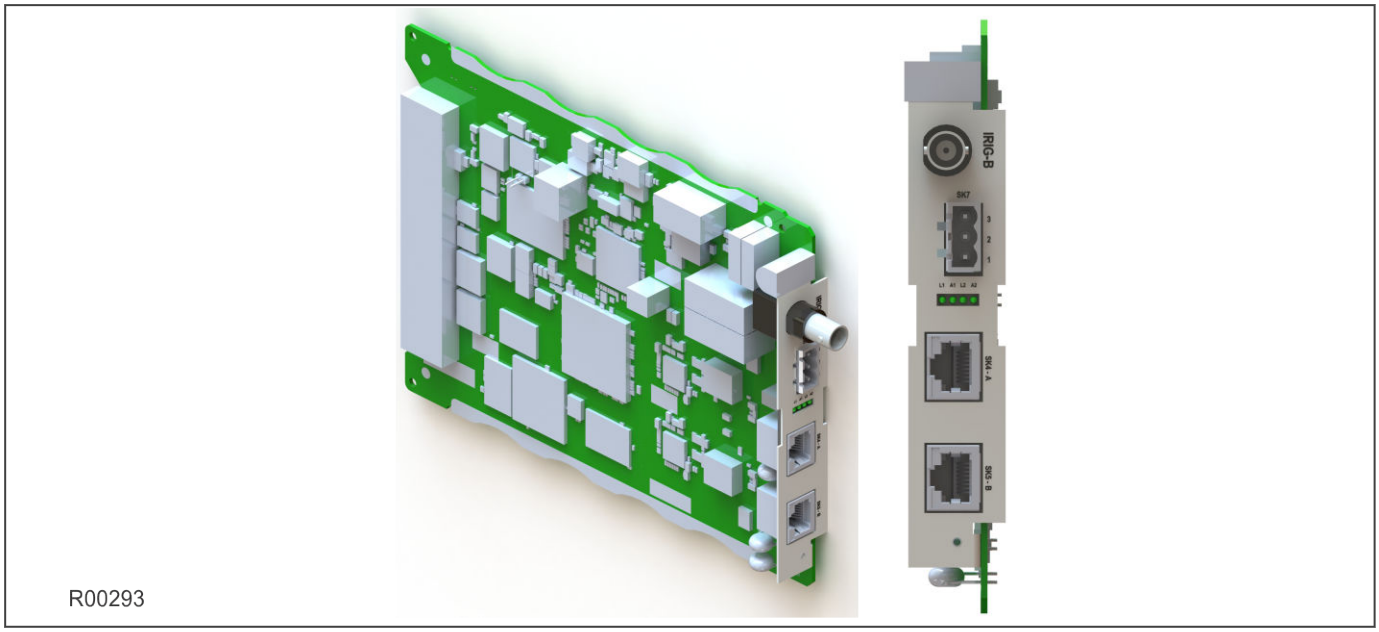



**Figure 27: Redundant Ethernet board**

This board provides dual redundant Ethernet together with an IRIG-B interface for timing.

Different board variants are available, depending on the redundancy protocol and the type of IRIG-B signal (unmodulated and modulated). The available redundancy protocols are:

- RSTP (Rapid Spanning Tree Protocol)
- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- Failover

There are several variants for this board as follows:

- 100 Mbps redundant Ethernet running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B
- 100 Mbps redundant Ethernet running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B
- 100 Mbps redundant Ethernet running RSTP + PRP + HSR + Failover (one copper, one multi-mode fibre), with on-board universal IRIG-B

The Ethernet and other connection details are described below:

### IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

### Link Fail Connector (Ethernet Board Watchdog Relay)

| Pin | Closed | Open |
|---|---|---|
| 1-2 | Link fail Channel 1 (A) | Link ok Channel 1 (A) |
| 2-3 | Link fail Channel 2 (B) | Link ok Channel 2 (B) |

### LEDs

| LED | Function | On | Off | Flashing |
|---|---|---|---|---|
| Green | Link | Link ok | Link broken | |
| Yellow | Activity | Running | | PRP, RSTP traffic |

### Optical Fibre Connectors (ST)

| Connector | RSTP | PRP | HSR |
|---|---|---|---|
| A | RX1 | RXA | RXA |
| B | TX1 | TXA | TXA |
| C | RX2 | RXB | RXB |
| D | TX2 | TXB | TXB |

### RJ45 Connector

| Pin | Signal Name | Signal Definition |
|---|---|---|
| 1 | TXP | Transmit (positive) |
| 2 | TXN | Transmit (negative) |
| 3 | RXP | Receive (positive) |
| 4 | - | Not used |
| 5 | - | Not used |
| 6 | RXN | Receive (negative) |
| 7 | - | Not used |
| 8 | - | Not used |

## 3.6.11 SINGLE ETHERNET BOARD (HARDWARE OPTION U)

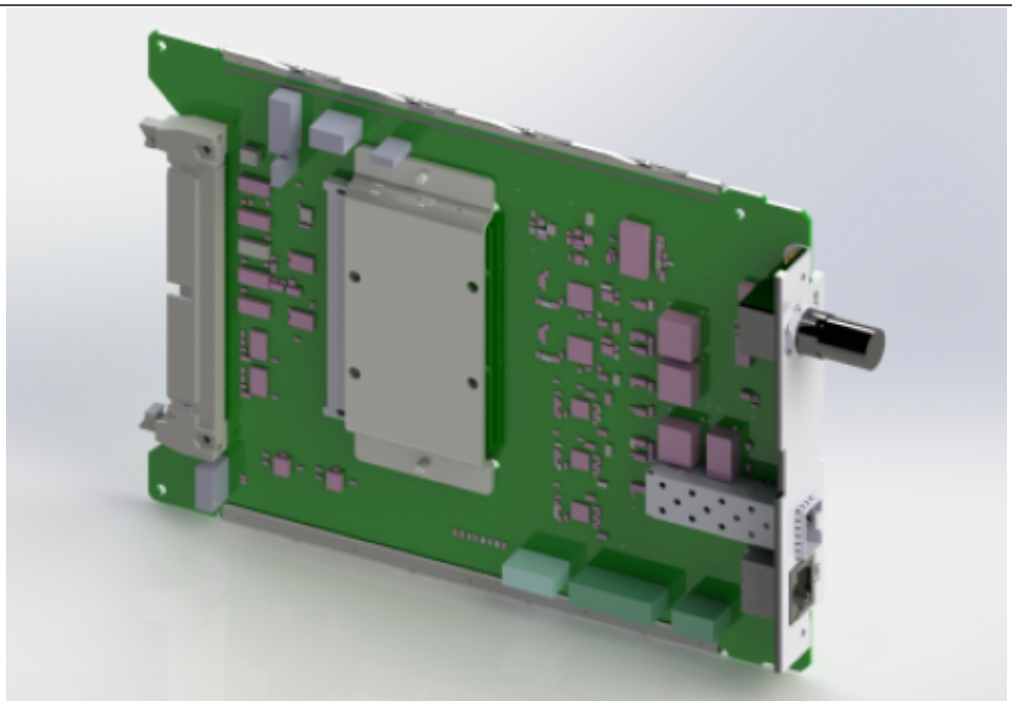


**Figure 28: Ethernet board**

This board provides one optical 100Mbps LC duplex Ethernet port (NP2A) for station bus communications, with a universal IRIG-B interface for time synchronisation. The NP1 Ethernet port is not active.

The Ethernet and other connection details are described below:

### UNIVERSAL IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

### LC Optical Fibre Connector (NP2A only)

| Connector | SFP |
|---|---|
| A | TX |
| B | RX |

### 3.6.12 REDUNDANT ETHERNET BOARD (HARDWARE OPTION W/Y)

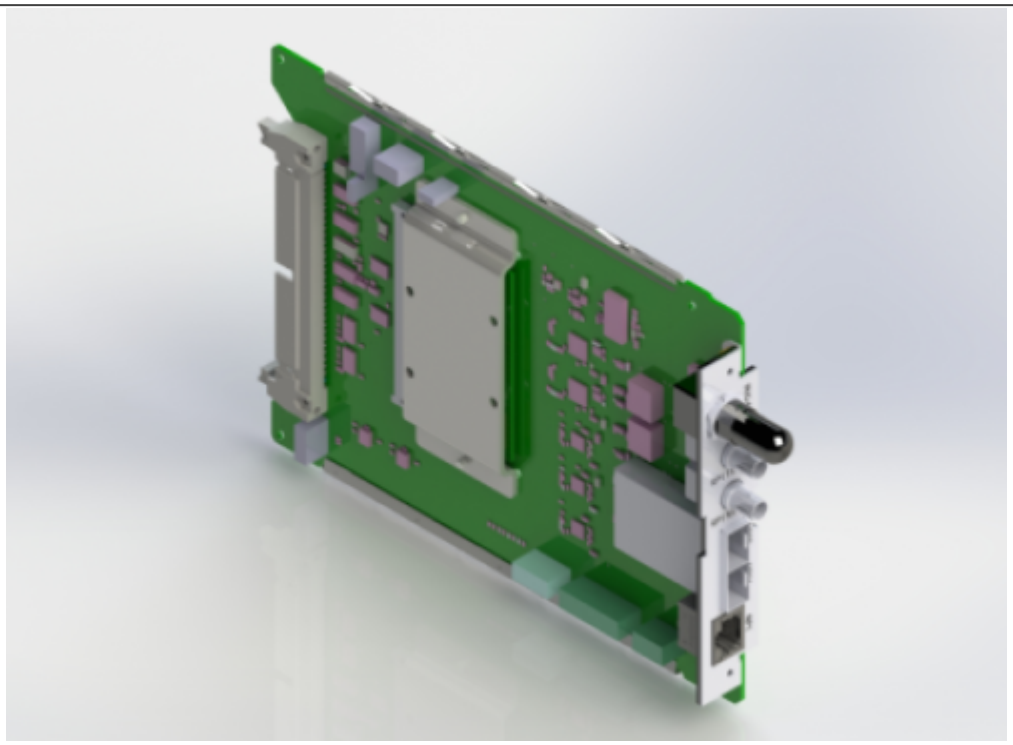


**Figure 29: Redundant Ethernet board**

This board provides dual redundant Ethernet (NP2A and NP2B) for station bus communications, with a universal IRIG-B interface for time synchronisation. The NP1 Ethernet port is not active.

The available redundancy protocols are:

- RSTP (Rapid Spanning Tree Protocol)
- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- Failover

There are several variants for this board as follows:

Two RJ45 duplex redundant 10/100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B.

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B.

The Ethernet and other connection details are described below:

#### UNIVERSAL IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

#### LC Optical Fibre Connector (only for NP2A or NP2B when ordering fibre ports on station bus ports)

| Connector | SFP |
|---|---|
| A | TX |
| B | RX |

#### RJ45 Connector (NP1 or NP2A/NP2B when ordering two copper ports on station bus ports only)

| Pin | Signal Name | Signal Definition |
|---|---|---|
| 1 | TXP | Transmit (positive) |
| 2 | TXN | Transmit (negative) |
| 3 | RXP | Receive (positive) |
| 4 | - | Not used |
| 5 | - | Not used |
| 6 | RXN | Receive (negative) |
| 7 | - | Not used |
| 8 | - | Not used |

## 3.6.13 RETROFIT OF ETHERNET CARDS HARDWARE OPTION R/S/T WITH HARDWARE OPTION U/W/Y

Some Px4x relays with 9x software will continue to support Ethernet boards with CORTEC Hardware options R/S/T, and also a newer version of the Ethernet board with Hardware option U/W/Y. The following information will help customers who want to retrofit existing installations using the new U/W/Y boards.

### General considerations:

- The model number of the IED will change to accommodate the new Ethernet board options U/W/Y if replacing any of the R/S/T Ethernet board options.
- Software 9x requires a new minor software upgrade to support the new Ethernet board options U/W/Y. The same minor software release will support both U/W/Y and R/S/T. Customers ordering 9x software without an Ethernet board option, won't need the upgrade.
- S1 Agile can convert settings and PSL files from hardware with the old R/S/T board to the new U/W/Y Ethernet board options for 9x software.

### Hardware review:

- Ethernet card R is a redundant Ethernet station bus card with 2 fibre optic ports with ST connectors. This card can be replaced with the new redundant Ethernet card Y which has 2 LC connectors.
    - **Impact:** The connectors are now LC, so the entire fibre needs to be replaced with a compatible one for the new connector, or an adaptor and a new small patchcord with the new connector.
- Ethernet card S is a redundant Ethernet station bus card with 2 RJ45 copper ports. This card can be replaced with the new redundant Ethernet card W which has 2 RJ45 copper ports.
    - **Impact:** No impact on port connections.
- Ethernet card T is a redundant Ethernet station bus card with a multi-mode fibre optic (ST) port and a copper RJ45 port. There is no like for like card in the new variant. If redundancy is not being used, the U Ethernet card provides a single multi-mode fibre optic (LC) port. If a single RJ45 copper Ethernet port is required Ethernet card W can be used in Failover mode. If redundancy is needed, either a variant W or a variant Y can be used depending on whether two copper or two fibre ports can be accommodated.
    - **Impact:** The impact depends on the application and the availability of fibre connectors. The new cards provide a solution for different applications except when a copper and fibre pairing in redundant mode are required.

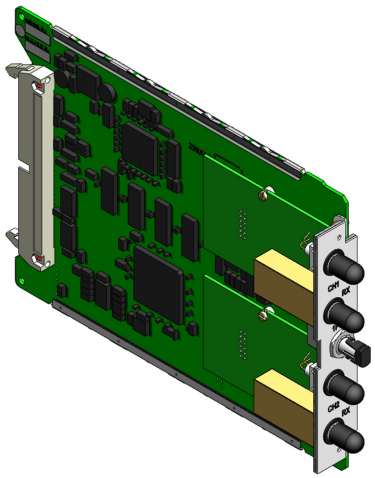
### Link Status monitoring

- Ethernet cards R/S/T have a link status contact (watchdog) and LED. Ethernet cards U/W/Y have no physical contact for the link status because this functionality is fully embedded into the main processor.
    - **Impact:** There are two independent link status contacts (watchdog) in the R/S/T cards, one for each channel.
    - In the 9x software supporting the new U/W/Y Ethernet boards and older R/S/T boards, there is a new IEC 61850 logical node (LCCH) to monitor the 2 redundant channels' link status, with two data attributes (DA), one for each channel, which can be used by the SCADA for monitoring.
    - In the 91_I software supporting the new U/W/Y Ethernet boards there is a new IEC 61850 logical node (LCCH) to monitor the 2 redundant channels' link status, with two data attributes (DA), one for each channel, which can be used by the SCADA for monitoring.
    - There also are 2 new link status DDBs in the PSL. NP2A port status and NP2B port status. NP2A is the LAN A channel, NP2B is the LAN B channel. The DDBs can be connected in the PSL as required, for example they can be linked to LEDs for visual indication or output contacts for connection to RTU (similar to how the fixed contacts worked in the R/S/T cards).
    - A NIC Link Fail DDB is also available for U/W/Y Ethernet boards. This DDB monitors the overall status of the Ethernet communications and is triggered if both channels are disconnected.

**S1 Agile tools and configuration files:**

- **S1 Agile:** A new version of S1 Agile, 3.2.0, is available to support the new hardware options U/W/Y. Configuration of the U/W/Y Ethernet ports can be done using the IED Configurator tool of S1 Agile compared to the configuration of the R/S/T Ethernet ports via the Redundant Ethernet Configurator tool of S1 Agile.
- **MCL Files:** The MCL template has changed to version 5.1 for the U/W/Y Ethernet ports. Should a user want to reuse an existing MCL file, version 5.0 (R/S/T options), they need to reload the new ICD template using the IED Configurator tool.
- **PSL Files:** A new default PSL file is available for the new software release which include the 2 new DDBs described above. For users with previous R/S/T PSL files, they can be converted to include the 2 new DDBs, using the PSL conversion tool in S1 Agile for software version 9x only. New PSL files for the U/W/Y Ethernet hardware options are provided via the Data Model Manager.
- **ICD Files:** A new ICD file to support the new software release is provided via the Data Model Manager.

## 3.6.14 COPROCESSOR BOARD



R00248

**Figure 30: Fully populated Coprocessor board**

*Note:*
*The above figure shows a coprocessor complete with GPS input and 2 fibre-optic serial data interfaces, and is not necessarily representative of the product and model described in this manual. These interfaces will not be present on boards that do not require them.*

Where applicable, a second processor board is used to process the special algorithms associated with the device. This second processor board provides fast access (zero wait state) SRAM for use with both program and data memory storage. This memory can be accessed by the main processor board via the parallel bus. This is how the software is transferred from the flash memory on the main processor board to the coprocessor board on power up. Further communication between the two processor boards is achieved via interrupts and the shared SRAM. The serial bus carrying the sample data is also connected to the co-processor board, using the processor's built-in serial port, as on the main processor board.

There are several different variants of this board, which can be chosen depending on the exact device and model. The variants are:

- Coprocessor board with current differential inputs and GPS input
- Coprocessor board with current differential inputs only
- Coprocessor board with GPS input only

#### 3.6.14.1 COPROCESSOR BOARD WITH 1PPS INPUT

In some applications, where the communication links between two remote devices are provided by a third party telecommunications partner, the transmit and receive paths associated with one channel may differ considerably in length, resulting in very different transmission and receive times.

If, for example, Device A is transmitting to Device B information about the value of its measured current, the information Device A is receiving from Device B about the current measured at the same time, may reach device B at a different time. This has to be compensated for. A 1pps GPS timing signal applied to both devices will help the IEDs achieve this, because it is possible to measure the exact time taken for both transmission and receive paths.

*Note:*
*The 1 pps signal is always supplied by a GPS receiver (such as a RT430).*

*Note:*
*This signal is used to control the sampling process, and timing calculations and is not used for time stamping or real time synchronisation.*

# CHAPTER 4

# SOFTWARE DESIGN

## 4.1 CHAPTER OVERVIEW

This chapter describes the software design of the IED.

This chapter contains the following sections:

Chapter Overview 64
Sofware Design Overview 65
System Level Software 66
Platform Software 69
Protection and Control Functions 70

## 4.2 SOFWARE DESIGN OVERVIEW

The device software can be conceptually categorized into several elements as follows:

- The system level software
- The platform software
- The protection and control software

These elements are not distinguishable to the user, and the distinction is made purely for the purposes of explanation. The following figure shows the software architecture.

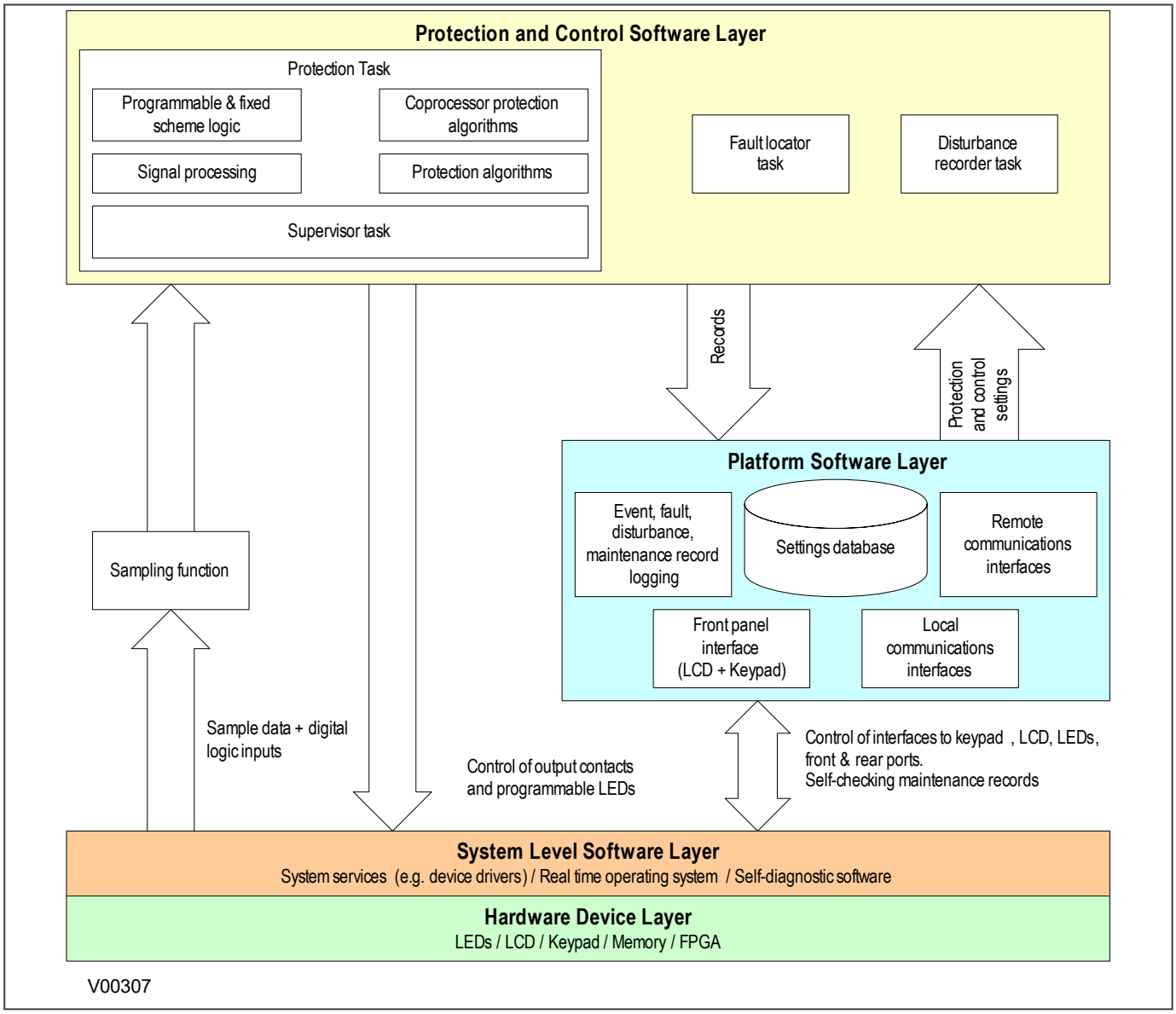



**Figure 31: Software Architecture**

The software, which executes on the main processor, can be divided into a number of functions as illustrated above. Each function is further broken down into a number of separate tasks. These tasks are then run according to a scheduler. They are run at either a fixed rate or they are event driven. The tasks communicate with each other as and when required.

# 4.3 SYSTEM LEVEL SOFTWARE

## 4.3.1 REAL TIME OPERATING SYSTEM

The real-time operating system is used to schedule the processing of the various tasks. This ensures that they are processed in the time available and in the desired order of priority. The operating system also plays a part in controlling the communication between the software tasks, through the use of operating system messages.

## 4.3.2 SYSTEM SERVICES SOFTWARE

The system services software provides the layer between the hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls things like the booting of the processor and the downloading of the processor code into RAM at startup.

## 4.3.3 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the ‘Healthy’ LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the ‘Healthy’ LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

## 4.3.4 STARTUP SELF-TESTING

The self-testing takes a few seconds to complete, during which time the IEDs measurement, recording, control, and protection functions are unavailable. On a successful start-up and self-test, the ‘Healthy' state LED on the front of the device is switched on. If a problem is detected during the start-up testing, the device remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

1. System boot
2. System software initialisation
3. Platform software initialisation and monitoring

### 4.3.4.1 SYSTEM BOOT

The integrity of the Flash memory is verified using a checksum before the program code and stored data is loaded into RAM for execution by the processor. When the loading has been completed, the data held in RAM is compared to that held in the Flash memory to ensure that no errors have occurred in the data transfer and that the two are the same. The entry point of the software code in RAM is then called. This is the IEDs initialisation code.

#### 4.3.4.2 SYSTEM LEVEL SOFTWARE INITIALISATION

The initialization process initializes the processor registers and interrupts, starts the watchdog timers (used by the hardware to determine whether the software is still running), starts the real-time operating system and creates and starts the supervisor task. In the initialization process the device checks the following:

- The status of the supercapacitor
- The integrity of the supercapacitor-backed SRAM that is used to store event, fault and disturbance records
- The operation of the LCD controller
- The watchdog operation

At the conclusion of the initialization software the supervisor task begins the process of starting the platform software. Coprocessor board checks are also made as follows:

- A check is made for the presence of the coprocessor board
- The RAM on the coprocessor board is checked with a test bit pattern before the coprocessor board is transferred from flash memory

If any of these checks produces an error, the coprocessor board is left out of service. The other protection functions provided by the main processor board are left in service.

#### 4.3.4.3 PLATFORM SOFTWARE INITIALISATION AND MONITORING

When starting the platform software, the IED checks the following:

- The integrity of the data held in non-volatile memory (using a checksum)
- The operation of the real-time clock
- The optional IRIG-B function (if applicable)
- The presence and condition of the input board
- The analog data acquisition system (it does this by sampling the reference voltage)

At the successful conclusion of all of these tests the unit is entered into service and the application software is started up.

### 4.3.5 CONTINUOUS SELF-TESTING

When the IED is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software and the results are reported to the platform software. The functions that are checked are as follows:

- The Flash memory containing all program code and language text is verified by a checksum.
- The code and constant data held in system memory is checked against the corresponding data in Flash memory to check for data corruption.
- The system memory containing all data other than the code and constant data is verified with a checksum.
- The integrity of the digital signal I/O data from the opto-inputs and the output relay coils is checked by the data acquisition function every time it is executed.
- The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed. This is done by sampling the reference voltages.
- The operation of the optional Ethernet board is checked by the software on the main processor board. If the Ethernet board fails to respond an alarm is raised and the board is reset in an attempt to resolve the problem.
- The operation of the optional IRIG-B function is checked by the software that reads the time and date from the board.

In the event that one of the checks detects an error in any of the subsystems, the platform software is notified and it attempts to log a maintenance record.

If the problem is with the IRIG-B board, the device continues in operation. For problems detected in any other area, the device initiates a shutdown and re-boot, resulting in a period of up to 10 seconds when the functionality is unavailable.

A restart should clear most problems that may occur. If, however, the diagnostic self-check detects the same problem that caused the IED to restart, it is clear that the restart has not cleared the problem, and the device takes itself permanently out of service. This is indicated by the ‘’health-state’ LED on the front of the device, which switches OFF, and the watchdog contact which switches ON.

## 4.4 PLATFORM SOFTWARE

The platform software has three main functions:

- To control the logging of records generated by the protection software, including alarms, events, faults, and maintenance records
- To store and maintain a database of all of the settings in non-volatile memory
- To provide the internal interface between the settings database and the user interfaces, using the front panel interface and the front and rear communication ports

### 4.4.1 RECORD LOGGING

The logging function is used to store all alarms, events, faults and maintenance records. The records are stored in non-volatile memory to provide a log of what has happened. The IED maintains four types of log on a first in first out basis (FIFO). These are:

- Alarms
- Event records
- Fault records
- Maintenance records

The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software. The platform software is responsible for logging a maintenance record in the event of an IED failure. This includes errors that have been detected by the platform software itself or errors that are detected by either the system services or the protection software function. See the Monitoring and Control chapter for further details on record logging.

### 4.4.2 SETTINGS DATABASE

The settings database contains all the settings and data, which are stored in non-volatile memory. The platform software manages the settings database and ensures that only one user interface can modify the settings at any one time. This is a necessary restriction to avoid conflict between different parts of the software during a setting change.

Changes to protection settings and disturbance recorder settings, are first written to a temporary location SRAM memory. This is sometimes called 'Scratchpad' memory. These settings are not written into non-volatile memory immediately. This is because a batch of such changes should not be activated one by one, but as part of a complete scheme. Once the complete scheme has been stored in SRAM, the batch of settings can be committed to the non-volatile memory where they will become active.

### 4.4.3 INTERFACES

The settings and measurements database must be accessible from all of the interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each of the interfaces (LCD display, keypad and all the communications interfaces).

## 4.5 PROTECTION AND CONTROL FUNCTIONS

The protection and control software processes all of the protection elements and measurement functions. To achieve this it has to communicate with the system services software, the platform software as well as organise its own operations.

The protection task software has the highest priority of any of the software tasks in the main processor board. This ensures the fastest possible protection response.

The protection and control software provides a supervisory task, which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

### 4.5.1 ACQUISITION OF SAMPLES

After initialization, the protection and control task waits until there are enough samples to process. The acquisition of samples on the main processor board is controlled by a ‘sampling function’ which is called by the system services software.

This sampling function takes samples from the input module and stores them in a two-cycle FIFO buffer. These samples are also stored concurrently by the coprocessor. The sample rate is 48 samples per cycle. This results in a nominal sample rate of 2,400 samples per second for a 50 hz system and 2,880 samples per second for a 60 Hz system. However the sample rate is not fixed. It tracks the power system frequency as described in the next section.

In normal operation, the protection task is executed 16 times per cycle.

### 4.5.2 FREQUENCY TRACKING

The device provides a frequency tracking algorithm so that there are always 48 samples per cycle irrespective of frequency drift. The frequency range in which 48 samples per second are provided is between 45 Hz and 66 Hz. If the frequency falls outside this range, the sample rate reverts to its default rate of 2,400 Hz for 50 Hz or 2,880 Hz for 60 Hz.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals. It works by detecting a change in the signal’s measured phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module, in order to achieve a constant sample rate per cycle of the power waveform. The value of the tracked frequency is also stored for use by the protection and control task.

The frequency tracks off any voltage or current in the order VA, VB, VC, IA, IB, IC, down to 10%Vn for voltage and 5%In for current.

### 4.5.3 DIRECT USE OF SAMPLED VALUES

Most of the IED’s protection functionality uses the Fourier components calculated by the device’s signal processing software. However RMS measurements and some special protection algorithms available in some products use the sampled values directly.

The disturbance recorder also uses the samples from the input module, in an unprocessed form. This is for waveform recording and the calculation of true RMS values of current, voltage and power for metering purposes.

In the case of special protection algorithms, using the sampled values directly provides exceptionally fast response because you do not have to wait for the signal processing task to calculate the fundamental. You can act on the sampled values immediately.

### 4.5.4 DISTANCE PROTECTION

The current and voltage inputs are filtered using Finite Impulse Response (FIR) digital filters. This reduces the effects of non-power frequency components in the input signals, such as DC offsets in current waveforms, and

capacitor voltage transformer (CVT) transients in the voltages. The distance protection in this device uses a combination of a 1/4 cycle filter using 12 coefficients, a 1/2 cycle filter using 24 coefficients, and a single cycle filter using 48 coefficients. The device automatically performs intelligent switching in the application of the filters, to select the best balance of removal of transients with fast response. The protection elements themselves then perform additional filtering, implemented for example, by the trip count strategy.

The following figure shows the frequency response of the 12, 24 and 48 coefficient filters, noting that all have a gain of unity at the fundamental frequency:

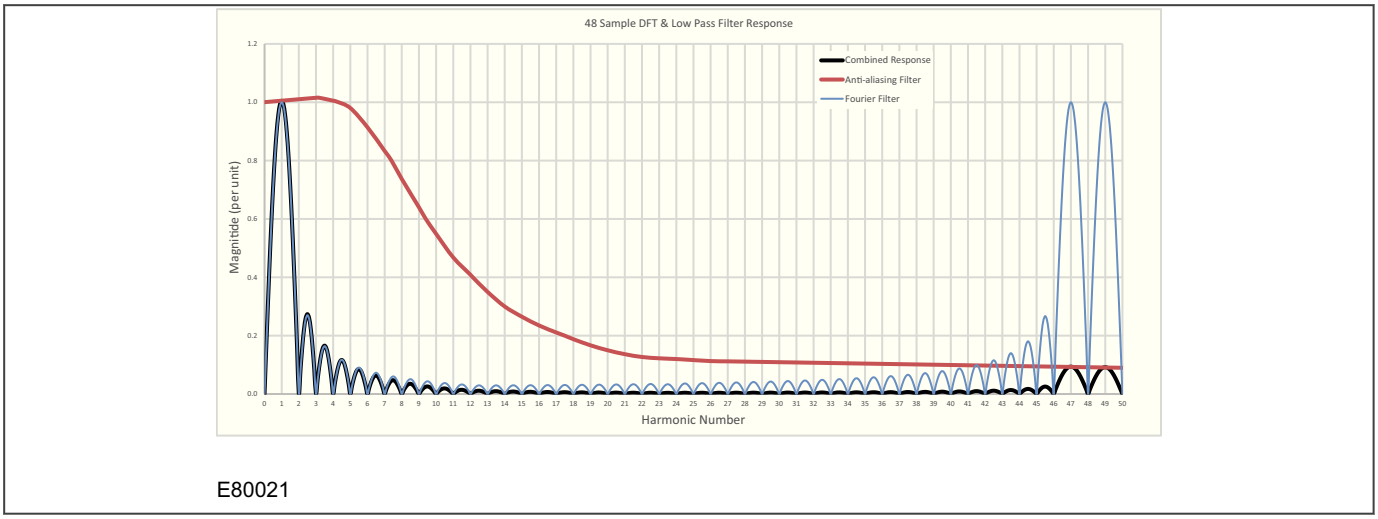



**Figure 32: Frequency response of FIR filters**

## 4.5.5 FOURIER SIGNAL PROCESSING

All backup protection and measurement functions use single-cycle Fourier digital filtering to extract the power frequency component. This filtering is performed on the main processor board.

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. Although some protection algorithms use some Fourier-derived harmonics (e.g. second harmonic for magnetizing inrush), most protection functions are based on the Fourier-derived fundamental components of the measured analog signals. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms.

The Fourier components are calculated using single-cycle Fourier algorithm. This Fourier algorithm always uses the most recent 48 samples from the 2-cycle buffer.

Most protection algorithms use the fundamental component. In this case, the Fourier algorithm extracts the power frequency fundamental component from the signal to produce its magnitude and phase angle. This can be represented in either polar format or rectangular format, depending on the functions and algorithms using it.

The Fourier filter acts as a function with zero gain at DC, unity gain at the fundamental, and with good harmonic rejection for all harmonic frequencies up to the Nyquist frequency. Frequencies beyond this Nyquist frequency appear as alias components and are introduced when the sampling frequency becomes less than twice the frequency component being sampled. The introduction of simple low-pass filters to limit the input frequency spectrum to less than half that of the sampling frequency prevents aliasing.

$$(\text{samples per cycle}) \times (\text{fundamental frequency})/2$$

At 48samples per cycle, this would be nominally 1200 Hz for a 50 Hz system, or 1440 Hz for a 60 Hz system.

The following figure shows the nominal frequency response of the anti-alias filter and the Fourier filter for a 48-sample single cycle fourier algorithm acting on the fundamental component:

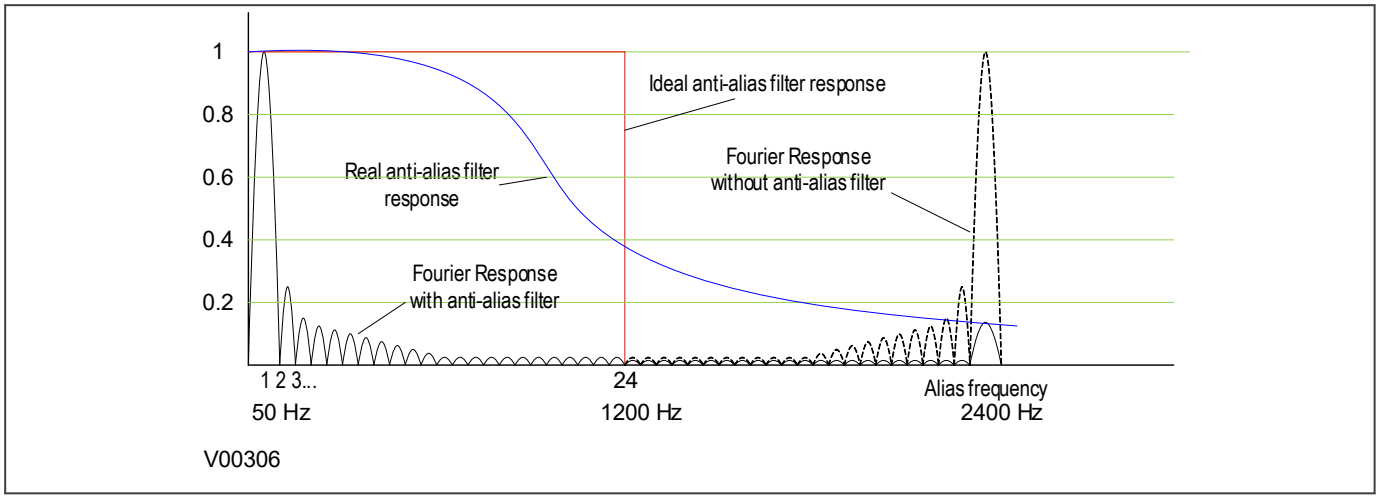



**Figure 33: Frequency Response (indicative only)**

## 4.5.6 PROGRAMMABLE SCHEME LOGIC

The purpose of the programmable scheme logic (PSL) is to allow you to configure your own protection schemes to suit your particular application. This is done with programmable logic gates and delay timers. To allow greater flexibility, different PSL is allowed for each of the four setting groups.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic (FSL). The fixed scheme logic provides the standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven. The logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

The PSL can be configured to create very complex schemes. Because of this PSL design is achieved by means of a PC support package called the PSL Editor. This is available as part of the settings application software MiCOM S1 Agile.

## 4.5.7 EVENT RECORDING

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer controlled by the supervisor task. When the supervisor task receives an event record, it instructs the platform software to create the appropriate log in non-volatile memory (backed-up SRAM). The operation of the record logging to backed-up SRAM is slower than the supervisor buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost, if the supervisor buffer is full before the platform software is able to create a new log in backed-up SRAM. If this occurs then an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner, with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record

may be triggered by a fatal error in the relay in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem.

For more information, see the Monitoring and Control chapter.

### 4.5.8 DISTURBANCE RECORDER

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms for up to 12 calibrated analog channels and the values of up to 32 digital signals. The recording time is user selectable. Up to 50 seconds of data can be recorded. A minimum number of 5 records with a capacity of 10 seconds each, up to a maximum of 50 records with a capacity of 10 seconds each can be set. The disturbance recorder is supplied with data by the protection and control task once per cycle. The disturbance recorder collates the data that it receives into the required length disturbance record. The disturbance records can be extracted by settings application software such as MiCOM S1 Agile, which can also store the data in COMTRADE format, therefore allowing the use of other packages to view the recorded data.

For more information, see the Monitoring and Control chapter.

### 4.5.9 FAULT LOCATOR

The fault locator uses 12 cycles of the analog input signals to calculate the fault location. The result is returned to the protection and control task, which includes it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record. When the fault record is complete, including the fault location, the protection and control task sends a message to the supervisor task to log the fault record.

The Fault Locator is not available on all models.

### 4.5.10 FUNCTION KEY INTERFACE

The function keys interface directly into the PSL as digital input signals. A change of state is only recognized when a key press is executed on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed. It can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up thus allowing the function key state to be reinstated after power-up, should power be inadvertently lost.

# CHAPTER 5

# CONFIGURATION

## 5.1 CHAPTER OVERVIEW

Each product has different configuration parameters according to the functions it has been designed to perform. There is, however, a common methodology used across the entire product series to set these parameters.

Some of the communications setup can only be carried out using the HMI, and cannot be carried out using settings applications software. This chapter includes concise instructions of how to configure the device, particularly with respect to the communications setup, as well as a description of the common methodology used to configure the device in general.

This chapter contains the following sections:

Chapter Overview 75
Settings Application Software 76
Using the HMI Panel 77
Line Parameters 87
Date and Time Configuration 90
Settings Group Selection 93

## 5.2 SETTINGS APPLICATION SOFTWARE

To configure this device you will need to use the Settings Application Software. The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for setting up and managing the IEDs.

Although you can change many settings using the front panel HMI, some of the features cannot be configured without the Settings Application Software; for example the programmable scheme logic, or IEC61850 communications.

If you do not already have a copy of the Settings Application Software, you can obtain it from GE Vernova's contact centre.

To configure your product, you will need a data model that matches your product. When you launch the Settings Application Software, you will be presented with a panel that allows you to invoke the “Data Model Manager”. This will close the other aspects of the software in order to allow an efficient import of the chosen data model. If you don’t have, or can’t find, the data model relating to your product, please call the GE Vernova contact centre.

When you have loaded all the data models you need, you should restart the Settings Application Software and start to create a model of your system using the “System Explorer” panel.

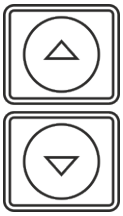
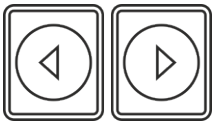
The software is designed to be intuitive, but help is available in an online help system and also the Settings Application Software user guide P40-M&CR-SAS-UG-EN-n, where 'Language' is a 2 letter code designating the language version of the user guide and 'n' is the latest version of the settings application software.

## 5.3 USING THE HMI PANEL

Using the HMI, you can:

- Display and modify settings
- View the digital I/O signal status
- Display measurements
- Display fault records
- Reset fault and alarm indications

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the LCD.

| Keys | Description | Function |
|---|---|---|
|  | Up and down cursor keys | To change the menu level or change between settings in a particular column, or changing values within a cell |
|  | Left and right cursor keys | To change default display, change between column headings, or changing values within a cell |
| | ENTER key | For changing and executing settings |
| | Hotkeys | For executing commands and settings for which shortcuts have been defined |
| | Cancel key | To return to column header from any menu cell |
| | Read key | To read alarm messages |
| | Function keys (not all models) | For executing user programmable functions |

*Note:*
*As the LCD display has a resolution of 16 characters by 3 lines, some of the information is in a condensed mnemonic form.*

## 5.3.1 NAVIGATING THE HMI PANEL

The cursor keys are used to navigate the menus. These keys have an auto-repeat function if held down continuously. This can be used to speed up both setting value changes and menu navigation. The longer the key is held pressed, the faster the rate of change or movement.

The navigation map below shows how to navigate the menu items.

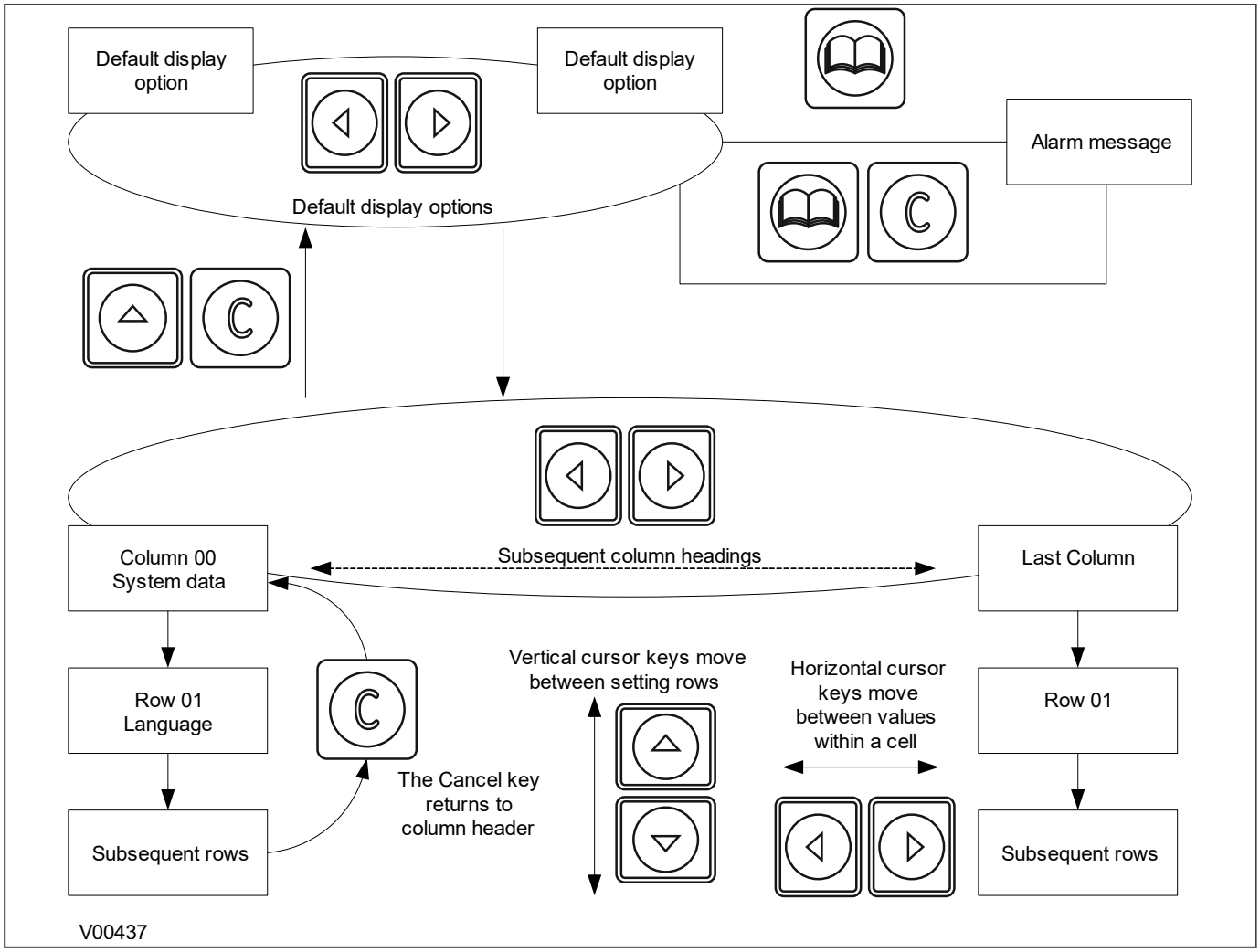



**Figure 34: Navigating the HMI**

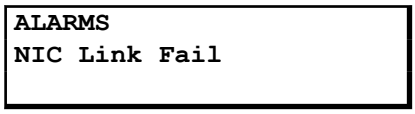
## 5.3.2 GETTING STARTED

When you first start the IED, it will go through its power up procedure. After a few seconds it will settle down into one of the top level menus. There are two menus at this level:

- The Alarms menu for when there are alarms present
- The default display menu for when there are no alarms present.

If there are alarms present, the yellow Alarms LED will be flashing and the menu display will read as follows:

Even though the device itself should be in full working order when you first start it, an alarm could still be present, for example, if there is no network connection for a device fitted with a network card. If this is the case, you can read the alarm by pressing the 'Read' key.




If the device is fitted with an Ethernet card, you will first need to connect the device to an active Ethernet network to clear the alarm and get the default display.

If there are other alarms present, these must also be cleared before you can get into the default display menu options.

## 5.3.3 DEFAULT DISPLAY

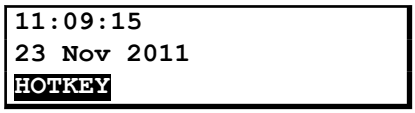
The HMI contains a range of possible options that you can choose to be the default display. The options available are:

### NERC Compliant banner

If the device is a cyber-security model, it will provide a NERC-compliant default display. If the device does not contain the cyber-security option, this display option is not available.

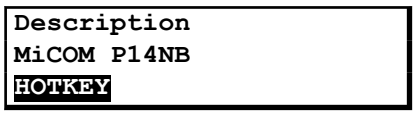
### Date and time

For example:




### Description (user-defined)

For example:




### Plant reference (user-defined)

For example:

```
Plant Reference
MiCOM
HOTKEY
```

### Access Level

For example:

```
Access Level
3
HOTKEY
```

In addition to the above, there are also displays for the system voltages, currents, power and frequency etc., depending on the device model.

## 5.3.4 DEFAULT DISPLAY NAVIGATION

The following diagram is an example of the default display navigation. In this example, we have used a cyber-secure model. This is an example only and may not apply in its entirety to all models. The actual display options available depend on the exact model.

Use the horizontal cursor keys to step through from one display to the next.

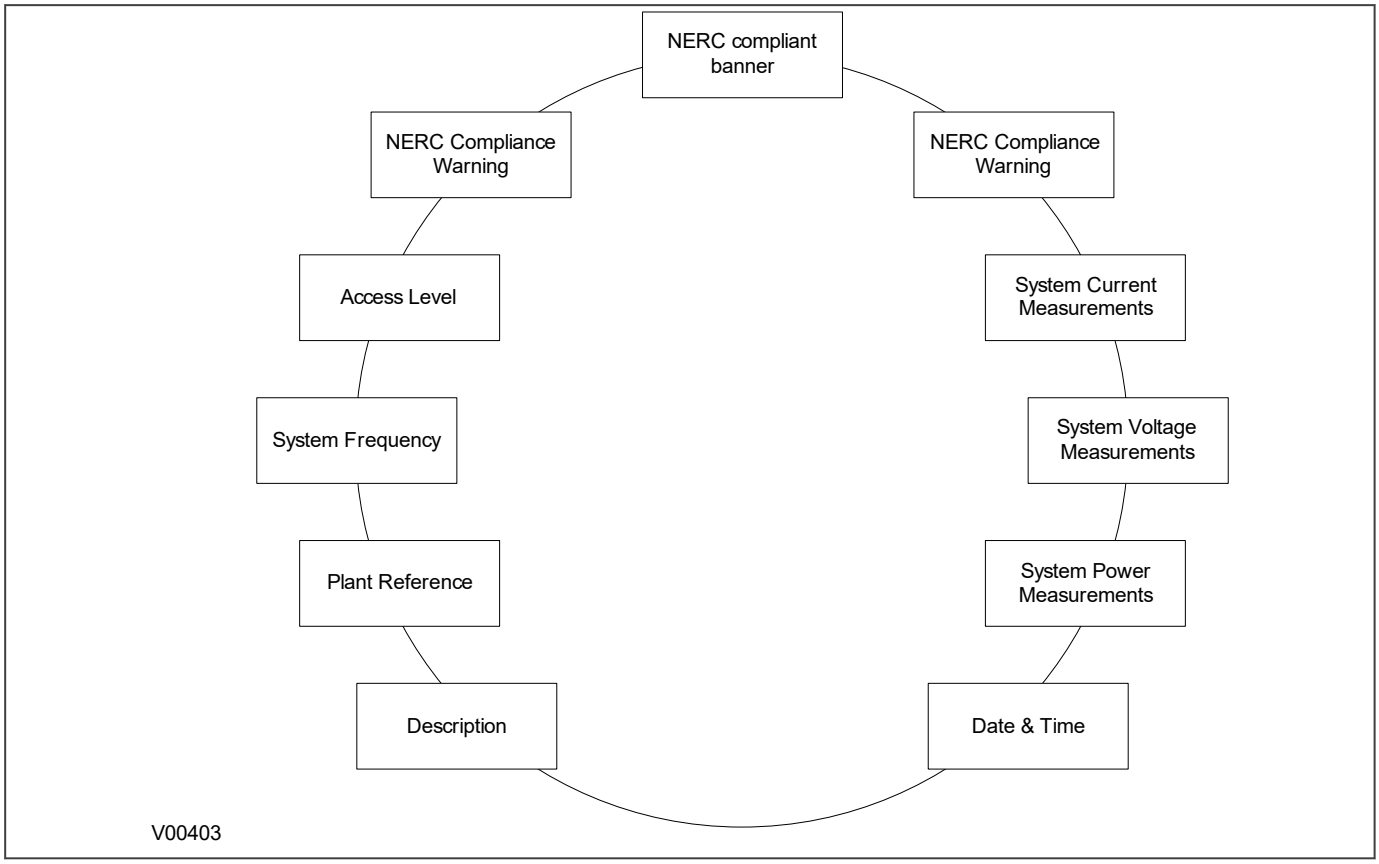



**Figure 35: Default display navigation**

If the device is cyber-secure but is not yet configured for NERC compliance (see Cyber-security chapter), a warning will appear when moving from the "NERC compliant" banner. The warning message is as follows:

```
DISPLAY NOT NERC
COMPLIANT. OK?
```

You will have to confirm with the **Enter** button before you can go any further.

*Note:*
*Whenever the IED has an uncleared alarm the default display is replaced by the text Alarms/ Faults present. You cannot override this default display. However, you can enter the menu structure from the default display, even if the display shows the Alarms/Faults present message.*

### 5.3.5 PASSWORD ENTRY

Configuring the default display (in addition to modification of other settings) requires level 3 access. You will be prompted for a password before you can make any changes, as follows. The default level 3 password is AAAA.

```
Enter Password
```

1. A flashing cursor shows which character field of the password can be changed. Press the up or down cursor keys to change each character (tip: pressing the up arrow once will return an upper case "A" as required by the default level 3 password).
2. Use the left and right cursor keys to move between the character fields of the password.
3. Press the **Enter** key to confirm the password. If you enter an incorrect password, an invalid password message is displayed then the display reverts to ***Enter password***. On entering a valid password a message appears indicating that the password is correct and which level of access has been unlocked. If this level is sufficient to edit the selected setting, the display returns to the setting page to allow the edit to continue. If the correct level of password has not been entered, the password prompt page appears again.
4. To escape from this prompt press the **Clear** key. Alternatively, enter the password using the ***Password*** setting in the *SYSTEM DATA* column. If the keypad is inactive for 15 minutes, the password protection of the front panel user interface reverts to the default access level.

To manually reset the password protection to the default level, select ***Password***, then press the CLEAR key instead of entering a password.

*Note:*
*In the SECURITY CONFIG column, you can set the maximum number of attempts, the time window in which the failed attempts are counted and the time duration for which the user is blocked.*

### 5.3.6 PROCESSING ALARMS AND RECORDS

If there are any alarm messages, they will appear on the default display and the yellow alarm LED flashes. The alarm messages can either be self-resetting or latched. If they are latched, they must be cleared manually.

1. To view the alarm messages, press the **Read** key. When all alarms have been viewed but not cleared, the alarm LED changes from flashing to constantly on, and the latest fault record appears (if there is one).
2. Scroll through the pages of the latest fault record, using the cursor keys. When all pages of the fault record have been viewed, the following prompt appears.

```
Press Clear To
Reset Alarms
```

3. To clear all alarm messages, press the **Clear** key. To return to the display showing alarms or faults present, and leave the alarms uncleared, press the **Read** key.
4. Depending on the password configuration settings, you may need to enter a password before the alarm messages can be cleared.
5. When all alarms are cleared, the yellow alarm LED switches off. If the red LED was on, this will also be switched off.

*Note:*
*To speed up the procedure, you can enter the alarm viewer using the **Read** key and subsequently pressing the **Clear** key. This goes straight to the fault record display. Press the **Clear** key again to move straight to the alarm reset prompt, then press the **Clear** key again to clear all alarms.*

### 5.3.7 MENU STRUCTURE

Settings, commands, records and measurements are stored in a local database inside the IED. When using the Human Machine Interface (HMI) it is convenient to visualise the menu navigation system as a table. Each item in the menu is known as a cell, which is accessed by reference to a column and row address. Each column and row is assigned a 2-digit hexadecimal numbers, resulting in a unique 4-digit cell address for every cell in the database. The main menu groups are allocated columns and the items within the groups are allocated rows, meaning a particular item within a particular group is a cell.

Each column contains all related items, for example all of the disturbance recorder settings and records are in the same column.

There are three types of cell:

- Settings: this is for parameters that can be set to different values
- Commands: this is for commands to be executed
- Data: this is for measurements and records to be viewed, which are not settable

*Note:*
*Sometimes the term "Setting" is used generically to describe all of the three types.*

The table below, provides an example of the menu structure:

| SYSTEM DATA (Col 00) | VIEW RECORDS (Col 01) | MEASUREMENTS 1 (Col 02) | … |
|---|---|---|---|
| Language (Row 01) | "Select Event [0...n]" (Row 01) | IA Magnitude (Row 01) | … |
| Password (Row 02) | Menu Cell Ref (Row 02) | IA Phase Angle (Row 02) | … |
| Sys Fn Links (Row 03) | Time & Date (Row 03) | IB Magnitude (Row 03) | … |
| … | … | … | … |

It is convenient to specify all the settings in a single column, detailing the complete Courier address for each setting. The above table may therefore be represented as follows:

| Setting | Column | Row | Description |
|---|---|---|---|
| **SYSTEM DATA** | **00** | **00** | **First Column definition** |
| Language (Row 01) | 00 | 01 | First setting within first column |
| Password (Row 02) | 00 | 02 | Second setting within first column |
| Sys Fn Links (Row 03) | 00 | 03 | Third setting within first column |
| … | … | … | |
| **VIEW RECORDS** | **01** | **00** | **Second Column definition** |
| Select Event [0...n] | 01 | 01 | First setting within second column |

| Setting | Column | Row | Description |
|---|---|---|---|
| Menu Cell Ref | 01 | 02 | Second setting within second column |
| Time & Date | 01 | 03 | Third setting within second column |
| … | … | … | |
| **MEASUREMENTS 1** | **02** | **00** | **Third Column definition** |
| IA Magnitude | 02 | 01 | First setting within third column |
| IA Phase Angle | 02 | 02 | Second setting within third column |
| IB Magnitude | 02 | 03 | Third setting within third column |
| … | … | … | |

The first three column headers are common throughout much of the product ranges. However the rows within each of these column headers may differ according to the product type. Many of the column headers are the same for all products within the series. However, there is no guarantee that the addresses will be the same for a particular column header. Therefore you should always refer to the product settings documentation and not make any assumptions.

### 5.3.8 CHANGING THE SETTINGS

1. Starting at the default display, press the **Down** cursor key to show the first column heading.
2. Use the horizontal cursor keys to select the required column heading.
3. Use the vertical cursor keys to view the setting data in the column.
4. To return to the column header, either press the Up cursor key for a second or so, or press the **Clear** key once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the Up cursor key or the **Clear** key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
7. To change the setting value, press the **Up** and **Down** cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the horizontal cursor keys.
8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the Down cursor key. Before returning to the default display, the following prompt appears.

```
Update settings?
ENTER or CLEAR
```

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

*Note:*
*For the protection group and disturbance recorder settings, if the menu time-out occurs before the changes have been confirmed, the setting values are discarded. Control and support settings, howeverr, are updated immediately after they are entered, without the* ***Update settings?*** *prompt.*

## 5.3.9 DIRECT ACCESS (THE HOTKEY MENU)

For settings and commands that need to be executed quickly or on a regular basis, the IED provides a pair of keys directly below the LCD display. These so called **Hotkeys** can be used to execute specified settings and commands directly.

The functions available for direct access using these keys are:

- Setting group selection
- Control inputs
- Circuit Breaker (CB) control functions

The availability of these functions is controlled by the ***Direct Access*** cell in the *CONFIGURATION* column. There are four options: *Disabled*, *Enabled*, *CB Ctrl only* and *Hotkey only*.

For the Setting Group selection and Control inputs, this cell must be set to either *Enabled* or *Hotkey only*. For CB Control functions, the cell must be set to *Enabled* or *CB Ctrl only*.

### 5.3.9.1 SETTING GROUP SELECTION USING HOTKEYS

In some models you can use the hotkey menu to select the settings group. By default, only Setting group 1 is enabled. Other setting groups will only be available if they are first enabled. To be able to select a different setting group, you must first enable them in the *CONFIGURATION* column.

To access the hotkey menu from the default display, you press the key directly below the HOTKEY text on the LCD. The following screen will appear.

```
←User32 STG GP→
HOTKEY MENU
            EXIT
```

Use the right cursor keys to enter the *SETTING GROUP* menu.

```
←Menu User01→
SETTING GROUP 1
Nxt Grp Select
```

Select the setting group with ***Nxt Grp*** and confirm by pressing ***Select***. If neither of the cursor keys is pressed within 20 seconds of entering a hotkey sub menu, the device reverts to the default display.

### 5.3.9.2 CONTROL INPUTS

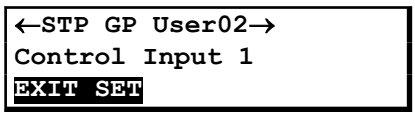
The control inputs are user-assignable functions. You can use the *CTRL I/P CONFIG* column to configure the control inputs for the hotkey menu. In order to do this, use the first setting ***Hotkey Enabled*** cell to enable or disable any of the 32 control inputs. You can then set each control input to latched or pulsed and set its command to *On/Off*, *Set/Reset*, *In/Out*, or *Enabled/Disabled*.

By default, the hotkey is enabled for all 32 control inputs and they are set to *Set/Reset* and are *Latched*.

To access the hotkey menu from the default display, you press the key directly below the HOTKEY text on the LCD. The following screen will appear.

```
←User32 STG GP→
HOTKEY MENU
            EXIT
```

Press the right cursor key twice to get to the first control input, or the left cursor key to get to the last control input.




Now you can execute the chosen function (Set/Reset in this case).

If neither of the cursor keys is pressed within 20 seconds of entering a hotkey sub menu, the device reverts to the default display.

#### 5.3.9.3 CIRCUIT BREAKER CONTROL

You can open and close the controlled circuit breaker with the hotkey to the right, if enabled as described above. By default, hotkey access to the circuit breakers is disabled.

If hotkeyaccess to the circuit breakers has been enabled, the bottom right hand part of the display will read "Open or Close" depending on whether the circuit breaker is closed or open respectively:

For example:

To close the circuit breaker (in this case), press the key directly below CLOSE. You will be given an option to cancel or confirm.

More detailed information on this can be found in the Monitoring and Control chapter.

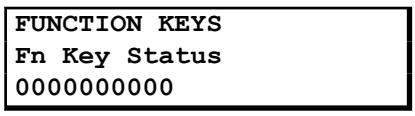
### 5.3.10 FUNCTION KEYS

Most products have a number of function keys for programming control functionality using the programmable scheme logic (PSL).

Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are in the *FUNCTION KEYS* column.

The first cell down in the *FUNCTION KEYS* column is the ***Fn Key Status*** cell. This contains a binary string, which represents the function key commands. Their status can be read from this binary string.




The next cell down (***Fn Key 1***) allows you to activate or disable the first function key (1). The ***Lock*** setting allows a function key to be locked. This allows function keys that are set to *Toggled* mode and their DDB signal active 'high', to be locked in their active state, preventing any further key presses from deactivating the associated function. Locking a function key that is set to the Normal mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

```
FUNCTION KEYS
Fn Key 1
Unlocked
```

The next cell down (***Fn Key 1 Mode***) allows you to set the function key to *Normal* or *Toggled*. In the Toggle mode the function key DDB signal output stays in the set state until a reset command is given, by activating the function key on the next key press. In the Normal mode, the function key DDB signal stays energised for as long as the function key is pressed then resets automatically. If required, a minimum pulse width can be programmed by adding a minimum pulse timer to the function key DDB output signal.

```
FUNCTION KEYS
Fn Key 1 Mode
Toggled
```

The next cell down (***Fn Key 1 Label***) allows you to change the label assigned to the function. The default label is *Function key 1* in this case. To change the label you need to press the enter key and then change the text on the bottom line, character by character. This text is displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

```
FUNCTION KEYS
Fn Key 1 Label
Function Key 1
```

Subsequent cells allow you to carry out the same procedure as above for the other function keys.

The status of the function keys is stored in non-volatile memory. If the auxiliary supply is interrupted, the status of all the function keys is restored. The IED only recognises a single function key press at a time and a minimum key press duration of approximately 200 ms is required before the key press is recognised. This feature avoids accidental double presses.

# 5.4 LINE PARAMETERS

This product requires information about the circuit to which it is applied. This includes line impedance, residual compensation, and phase rotation sequence. For this reason circuit parameter information must be input using the *LINE PARAMETERS* settings. These *LINE PARAMETERS* settings are used by protection elements as well as by the fault locator.

## 5.4.1 TRIPPING MODE

The ***Tripping Mode*** setting selects whether the product should trip single-phase or three-phase when instantaneous protection elements detect single-phase faults.

Selecting `1 and 3 Pole` means that the product will only trip the affected phase for a single-phase fault. For faults involving more than one phase the product will always trip all three phases.

Selecting `3 Pole` means that the product will always trip all three phases.

For products controlling more than one circuit breaker, the tripping mode is independent for each circuit breaker.

The product features an autorecloser that can be used for single-phase autoreclose. In that case, if a single-phase fault evolves into a multi-phase fault during the autoreclose cycle, the product will switch to three-phase tripping.

### 5.4.1.1 CB TRIP CONVERSION LOGIC DIAGRAM

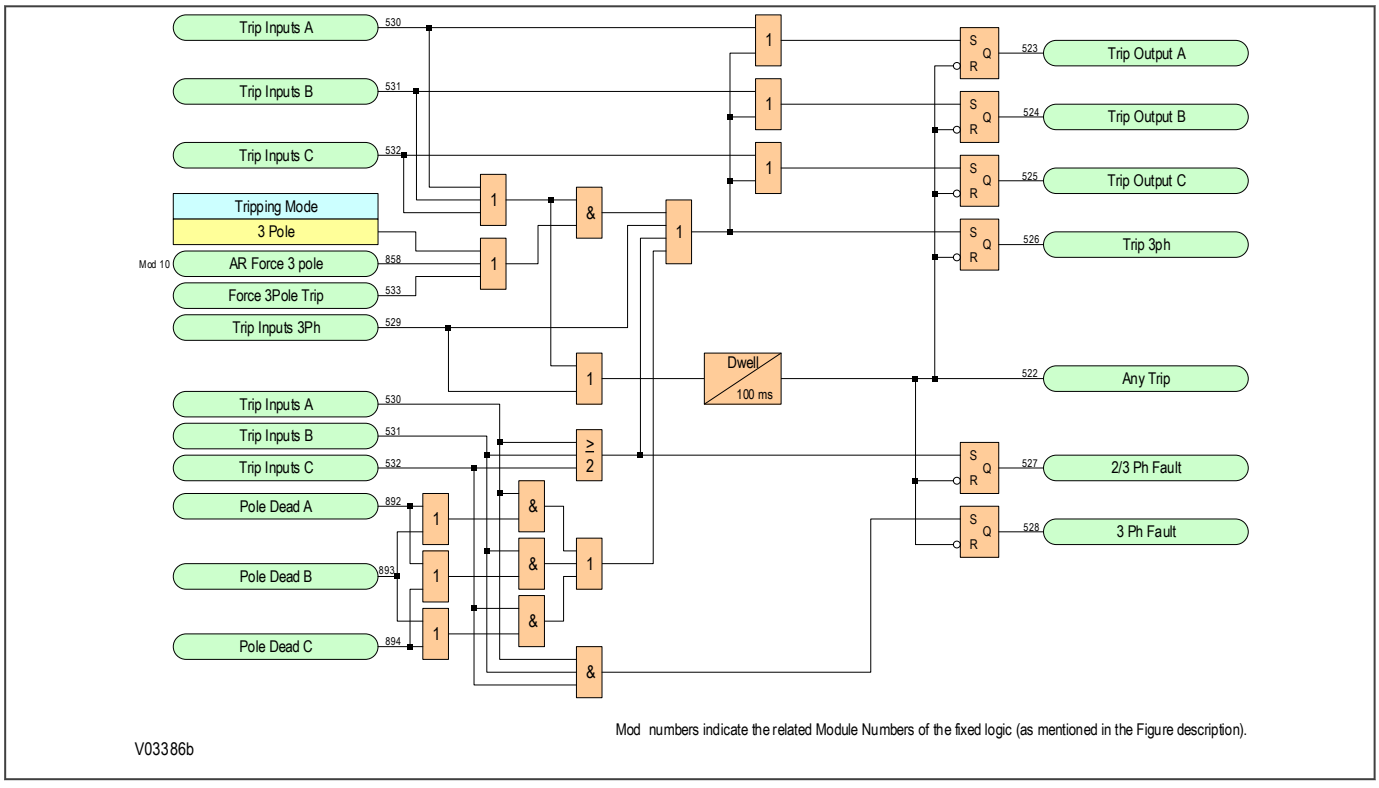



**Figure 36: Circuit Breaker Trip Conversion Logic Diagram (Module 63)**

## 5.4.2 RESIDUAL COMPENSATION

To improve accuracy of impedance measuring elements such as those used in distance protection and fault locators, the total loop impedance calculation $Z_{LP}/I_A$ can be calibrated by the positive sequence impedance between the relaying point and the fault ($Z_{F1}$) using the following equation:

$$\mathbf{Z}_{F1} = \frac{\mathbf{V}_A}{\mathbf{I}_A + \mathbf{k}_{ZN} \cdot \mathbf{I}_N}$$

where:

- $V_A$ is the phase A voltage
- $I_A$ is the phase A current
- $I_N$ is the residual current, derived from the phase currents by the equation:

$$\mathbf{I}_N = \mathbf{I}_A + \mathbf{I}_B + \mathbf{I}_C$$

- $k_{ZN}$ is the residual compensation coefficient given by the complex equation:

$$\mathbf{k}_{ZN} = \frac{\mathbf{Z}_{L0} - \mathbf{Z}_{L1}}{3\mathbf{Z}_{L1}}$$

where:

- $Z_{L0}$ is the total zero sequence impedance of the line (a complex value)
- $Z_{L1}$ is the total positive sequence impedance of the protected line (a complex value)

The complex residual compensation coefficient is defined by two settings: ***kZN Res Comp*** (the absolute value) and ***kZN Res Angle*** (the angle in degrees).

**Caution:**
**The *kZN Res Angle* is different to that in LFZP, SHNB, and LFZR products: If importing settings from these products, you must subtract angle $\angle Z_{L1}$**

## 5.4.3 MUTUAL COMPENSATION

On parallel circuits, mutual flux coupling can alter the impedance seen by fault locators and distance zones. A current input (the Mutual Compensation input) is provided to compensate.

If you want to use Mutual Compensation, the connection polarity must match that shown in the connection diagram and the element must be `Enabled` in the settings.

Consider for example an A-phase to earth fault on one circuit of a parallel circuit. The positive sequence impedance between the relaying point and the fault can be calculated using the following equation:

$$\boldsymbol{Z}_{F1} = \frac{\boldsymbol{V}_A}{\boldsymbol{I}_A + \boldsymbol{k}_{ZN} \cdot \boldsymbol{I}_N + \boldsymbol{k}_{Zm} \cdot \boldsymbol{I}_M}$$

where:

- $V_A$ is the phase A voltage
- $I_A$ is the phase A current
- $I_N$ is the residual current of the protected line (derived from phase currents)
- $I_M$ is the residual current of the parallel line (measured)
- $k_{ZN}$ is the residual compensation coefficient
- $k_{Zm}$ is the mutual compensation coefficient

In the above equation:

$$\mathbf{I}_N = \mathbf{I}_A + \mathbf{I}_B + \mathbf{I}_C$$

$$\mathbf{k}_{ZN} = \frac{\mathbf{Z}_{L0} - \mathbf{Z}_{L1}}{3\mathbf{Z}_{L1}}$$

$$\mathbf{k}_{Zm} = \frac{\mathbf{Z}_{m0}}{3\mathbf{Z}_{L1}}$$

where:

- $Z_{L0}$ is the total zero sequence impedance of the line (a complex value)
- $Z_{L1}$ is the total positive sequence impedance of the protected line (complex value)
- $Z_{m0}$ is the zero sequence mutual impedance between the two circuits (complex value).

If used, you must set the mutual compensation feature $k_{Zm}$ using the settings:

- ***kZm Mutual Set*** (the absolute value) and
- ***kZm Mutual Angle*** (the angle in degrees).

*Note:*
*The following paragraph applies only to distance products and so may not be applicable to your model*

In applications where the Mutual Compensation is used to reduce errors in the distance elements, a third setting, ***Mutual Cut Off***, is used for a fast dynamic control. The ratio $I_M/I_N$ is compared with the ***Mutual Cut Off*** setting. If the ratio is higher, mutual compensation is suppressed to prevent false-tripping for faults on the parallel line.

Typically a ***Mutual Cut Off*** factor of 1.5 is chosen to give a good margin of safety between the requirements of correct mutual compensation for faults on the protected circuit whilst avoiding maloperations for faults on the parallel circuit.

# 5.5 DATE AND TIME CONFIGURATION

The date and time setting will normally be updated automatically by the chosen UTC (Universal Time Co-ordination) time synchronisation mechanism when the device is in service. You can also set the date and time manually using the ***Date/Time*** cell in the *DATE AND TIME* column.

## 5.5.1 USING AN SNTP SIGNAL

When using SNTP to maintain the clock, the IED must first be connected to the SNTP server, which should be energized and functioning.

1. In the *DATE AND TIME* column, check that either the ***Primary Source*** or ***Secondary Source*** setting is set to `SNTP`.
2. Ensure that the IED is receiving valid time synchronisation messages by checking that the ***SNTP Status*** cell reads `Server 1 OK` or `Server 2 OK`.
3. Check that the ***Act. Time Source*** cell reads `SNTP`. This indicates that the IED is using PTP as the source for its time. Note that If IRIG-B or PTP have been selected as the Primary Source, these must first be disconnected before the device can switch to SNTP as the active source.
4. Once the IED is using SNTP as the active time source, adjust the time offset of the universal coordinated time on the SNTP Server equipment, so that local time is displayed.
5. Check that the time, date and month are correct in the ***Date/Time*** cell.

## 5.5.2 USING AN IRIG-B SIGNAL

When using IRIG-B to maintain the clock, the IED must first be connected to the timing source equipment (usually a P594/RT430), which should be energized and functioning.

1. In the *DATE AND TIME* column, check that either the ***Primary Source*** or ***Secondary Source*** setting is set to `IRIG-B`.
2. Ensure the IED is receiving the IRIG-B signal by checking that ***IRIG-B Status*** cell reads `Active`
3. Check that the ***Act. Time Source*** cell reads `IRIG-B.` This indicates that the IED is using IRIG-B as the source for its time. Note that If SNTP or PTP have been selected as the Primary Source, these must first be disconnected before the device can switch to IRIG-B as the active source.
4. Once the IED is using IRIG-B as the active time source, adjust the time offset of the universal coordinated time (satellite clock time) on the satellite clock equipment, so that local time is displayed.
5. Check that the time, date and month are correct in the ***Date/Time*** cell. The IRIG-B signal does not contain the current year so this also needs to be set manually in this cell.
6. If the auxiliary supply fails, the time and date are maintained by the supercapacitor. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energized for approximately 30 seconds. On re-energization, the time should be correct.
7. Reconnect the IRIG-B signal.

## 5.5.3 USING AN IEEE 1588 PTP SIGNAL

When using IEEE 1588 PTP to maintain the clock, the IED must first be connected to the PTP Grandmaster, which should be energized and functioning.

1. In the *DATE AND TIME* column, check that either the ***Primary Source*** or ***Secondary Source*** setting is set to `PTP`.
2. Set the ***Domain Number*** setting. The domain defines which clocks the IED will use for synchronisation. Therefore this number must match the domain used by the other clocks on the network.

3. Ensure that the IED is receiving valid time synchronisation messages by checking that the ***PTP Status*** cell reads `Valid Master`.
4. Check that ***Act. Time Source*** cell reads `PTP`. This indicates that the IED is using PTP as the source for its time. Note that If IRIG-B or SNTP have been selected as the Primary Source, these must first be disconnected before the device can switch to PTP as the active source.
5. Once the IED is using PTP as the active time source, adjust the time offset of the universal coordinated time on the Master Clock equipment, so that local time is displayed.
6. Check that the time, date and month are correct in the ***Date/Time*** cell.

### 5.5.4 WITHOUT A TIMING SOURCE SIGNAL

If the time and date is not being maintained by an IRIG-B, PTP or SNTP signal, in the *DATE AND TIME* column, ensure that both the ***Primary Source*** and ***Secondary Source*** are set to `NONE`.

1. Check that ***Act. Time Source*** cell reads `Free Running`.
2. Set the date and time to the correct local time and date using the Date/Time cell or the serial protocol.
3. If the auxiliary supply fails, the time and date are maintained by the supercapacitor. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the auxiliary supply. Leave the device de-energized for approximately 30 seconds. On re-energization, the time should be correct.

### 5.5.5 TIME ZONE COMPENSATION

The UTC time standard uses Greenwich Mean Time as its standard. Without compensation, the date and time would be displayed on the device irrespective of its location.

You may wish to display the local time corresponding to its geographical location. You can do this with the settings ***LocalTime Enable*** and ***LocalTime Offset***.

The ***LocalTime Enable*** has three setting options; `Disabled`, `Fixed`, and `Flexible`.

With `Disabled`, no local time zone is maintained. Time synchronisation from any interface will be used to directly set the master clock. All times displayed on all interfaces will be based on the master clock with no adjustment.

With `Fixed`, a local time zone adjustment is defined using the ***LocalTime Offset*** setting and all non-IEC 61850 interfaces, which uses the Simple Network Time Protocol (SNTP), are compensated to display the local time.

With `Flexible`, a local time zone adjustment is defined using the ***LocalTime Offset*** setting. The non-local and non-IEC 61850 interfaces can be set to either the UTC zone or the local time zone. The local interfaces are always set to the local time zone and the Ethernet interface is always set to the UTC zone.

The interfaces where you can select between UTC and Local Time are the serial interfaces RP1, RP2 and Tunnelled Courier (if applicable). This is achieved by means of the following settings, each of which can be set to UTC or Local.:

- RP1 Time Zone
- RP2 Time Zone
- Tunnel Time Zone

The ***LocalTime Offset*** setting allows you to enter the local time zone compensation from -12 to + 12 hours at 15 minute intervals.

### 5.5.6 DAYLIGHT SAVING TIME COMPENSATION

It is possible to compensate for Daylight Saving time using the following settings

- DST Enable
- DST Offset

- DST Start
- DST Start Day
- DST Start Month
- DST Start Mins
- DST End
- DST End Day
- DST End Month
- DST End Mins

These settings are described in the *DATE AND TIME* settings table in the configuration chapter.

## 5.6 SETTINGS GROUP SELECTION

You can select the setting group using opto inputs, a menu selection, and for some models the hotkey menu or function keys. You choose which method using the Setting Group setting in the *CONFIGURATION* column. There are two possibilities; Select via Menu, or Select via PSL. If you choose ***Select via Menu***, you set the settings group using the ***Active Settings*** setting or with the hotkeys. If you choose ***Select via PSL*** , you set the settings group with DDB signals according to the following table:

| SG Select 1X | SG Select X1 | Selected Setting Group |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

Each setting group has its own PSL. Once a PSL configuration has been designed it can be allocated to any one of the 4 setting groups. When downloading or extracting a PSL configuration, you will be prompted to enter the required setting group to which it will allocated.

CHAPTER 6

# DISTANCE PROTECTION

## 6.1 CHAPTER OVERVIEW

This chapter introduces the principles and theory behind the protection and describes how it is implemented in this product. Guidance for applying this protection is also provided.

This chapter contains the following sections:

Chapter Overview 95
Introduction 96
Distance Measuring Zones Operating Principles 98
Phase and Earth Fault Distance Protection Implementation 130
Distance Isolated and Compensated Systems 141
Application Notes 155

# 6.2 INTRODUCTION

Amongst protection engineers, the basic principles of Distance Protection are widely documented and understood. If you are reading this chapter, we assume that you are familiar with the principles of distance protection and associated components such as Aided Schemes. However, to help you choose suitable settings, some of the principles of operation of the Distance Measuring Zones is included in this chapter.

## 6.2.1 DISTANCE PROTECTION PRINCIPLE

The principle behind Distance protection is based on using measured values of voltage and current to calculate impedance seen from a relaying point. If the impedance calculated is an unexpected value, this may indicate a fault.

The impedance of a transmission line is proportional to its length. If voltage and current signals are available at a relaying point, they can be used to calculate the impedance value seen from the relaying point. Impedance values looking forward into the line, as well as values looking in the reverse direction behind the relaying point can be calculated. The calculated impedance is compared with so called 'Reach Points'. Reach Points are impedance values, which are used to define zones of protection. The device contains settings by which you can configure these Reach Points. The zones are usually numbered (for example: Zone 1, Zone 2, Zone 3). By comparing the calculated impedance with the zone reach points, the device can determine whether a fault is present and if necessary, trip the associated circuit breakers.

## 6.2.2 PERFORMANCE INFLUENCING FACTORS

As well as the accuracy of the signals presented by the input transducers, an important factor that influences the performance of distance protection is the relationship between the source and line impedance. This is the System Impedance Ratio (SIR), and is defined by $Z_S/Z_L$.

The following figure represents a fault condition on an electrical power system, and can be used to demonstrate the relationship.

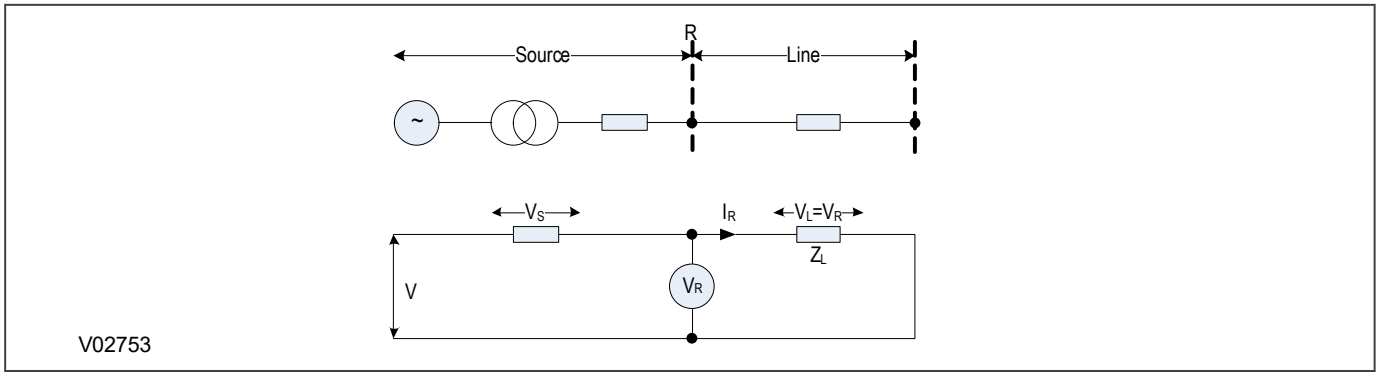



**Figure 37: System Impedance Ratio**

The voltage V applied to the impedance loop is the open circuit voltage of the power system. Point R represents the protection location; $I_R$ and $V_R$ are the current and voltage measured by the relay, respectively.

The impedances $Z_s$ and $Z_L$ are described as source and line impedances because of their position with respect to the protection location. Source impedance $Z_s$ is a measure of the fault level at the relaying point. For faults involving earth it is dependent on the method of system earthing behind the relaying point. Line impedance $Z_L$ is a measure of the impedance of the protected section. The voltage $V_R$ applied to the relay is, therefore, $I_RZ_L$. For a fault at the reach point, this may be expressed in terms of the System Impedance Ratio, using the following expression:

$$V_R = V/(SIR+1)$$

where SIR = $Z_S/Z_L$

From the equation above, it can be seen that the measured voltage has a significant impact on the decision making process.

The ability of distance protection to measure accurately for a given reach point fault, depends on the voltage at the relaying location being above a minimum value at the time of the fault. If the voltage is above this minimum value, it is generally used to polarize the distance protection and indicate the direction of the fault. This is called self-polarization.

If the voltage collapses below the minimum threshold necessary to make a sensible decision, alternative methods of polarization to determine the direction of the fault are needed. Two methods that are applied are cross-polarization and memory polarization. If a fault doesn't affect all phases, the voltage signals on the healthy phases can be used for the directional decision. This is called cross-polarization. If the fault causes all phase voltages to collapse, a stored record of the pre-fault voltage can be used to make the directional decision. This is called memory polarization. Memory polarization, cross-polarization, and self-polarization can sometimes be used in combination.

## 6.2.3 IMPEDANCE CALCULATION

Careful selection of the reach settings and tripping times for the various measurement zones enables correct coordination between Distance protection devices. Basic Distance protection will comprise instantaneous directional Zone 1 protection and one or more time delayed zones. A basic distance protection scheme is likely to feature 3 zones of protection, but numerical distance protection devices may have several more zones, some set to measure in the forward direction and some set to measure in the reverse direction.

Some numerical distance protection devices measure the fault voltage and current directly then calculate the impedance, after which they determine whether operation is required according to impedance boundaries defined on an R/X diagram. Many numerical IEDs emulate their traditional electro-mechanical counterparts. Rather than calculating the absolute impedance, they compare the measured fault voltage with a replica voltage derived from the fault current and the zone impedance setting to determine whether the fault is within zone or out-of-zone.

Typically, a comparator will compare either the relative amplitude or relative phase of input quantities to determine impedance limits. Limits may be either straight line characteristics (quadrilaterals), or circular characteristics (Mhos).

## 6.2.4 IMPLEMENTATION WITH COMPARATORS

The distance protection in this product uses measured values of voltage and current, together with setting values such as line impedance, to determine whether fault conditions exist. The determination as to whether a fault condition exists is performed by so-called ‘comparators’. These comparators use voltage and current inputs in conjunction with impedance settings to decide whether a fault is in a particular zone. Multiple zones can provide protection for the protected line as well as providing back-up protection for connected lines.

All distance zone calculations in this product are constructed using one or more comparators. Each comparator uses two vector quantities which are generally referenced as S1 and S2. S1 and S2 comparators are used to construct either circular (Mho) and/or Quadrilateral characteristics. In the case of Mho characteristics, a single comparator is used to make a tripping decision. In the case of Quadrilateral characteristics, multiple comparators are used to make a tripping decision.

## 6.2.5 POLARIZATION OF DISTANCE CHARACTERISTICS

The distance zone characteristics are polarized (directionalized) to reflect the characteristic angle of the line. Some of the zones of the distance protection are forward looking, some are reverse looking, and some are of the offset type. Polarization is generally achieved by directional self-polarization, but memory-polarization, or cross-polarization, might be adopted for close-up zero-voltage faults.

## 6.3 DISTANCE MEASURING ZONES OPERATING PRINCIPLES

All distance zone characteristics in this product are constructed with one or more comparators. The comparators are used to construct either Mho, or Quadrilateral characteristics. This section outlines the principles behind the construction of the characteristics in order to provide an understanding of how best to set them.

The following table details signal definitions used to construct the measuring zone characteristics.

| Name | Description |
|---|---|
| $I$ | Current |
| $I$ | Current used by the Distance protection measuring element |
| $I_M$ | Residual current of parallel line (mutual current) |
| $I_N$ | Neutral Current (derived) |
| $I_{ph}$ | Faulted phase current (for example IA for A-N fault) |
| $j$ | The complex operator |
| $k_M$ | Mutual compensation co-efficient |
| $k_{ZN}$ | Residual compensation co-efficient |
| $p$ | Distance polarizing factor. A percentage of the memory voltage polarizing signal that is added to the self-polarizing voltage signal to dictate the level of Mho expansion and help establish a directional decision. |
| $R$ | Resistance |
| $R$ | Forward Resistance Reach |
| $R'$ | Reverse Resistance Reach |
| $S$ | A voltage vector value comprising one or more voltage components |
| $S_1$ | A voltage vector input to a comparator |
| $S_2$ | A second voltage vector input to a comparator |
| $V$ | Voltage |
| $V$ | Voltage used by the Distance protection measuring element |
| $V/I$ | Impedance measured by the Distance protection element |
| $V_{mem}$ | Voltage memory signal used for polarization |
| $V_{ph}$ | Faulted phase voltage (for example VA for A-N fault) |
| $V_{ph}/I_{ph}$ | Loop impedance measurement |
| $V_S$ | Source voltage |
| $X$ | Reactance |
| $Z$ | Impedance Reach setting |
| $Z'$ | Reverse Impedance Reach setting |
| $Z_1$ | Positive sequence impedance |
| $Z_{LP}$ | Loop impedance |
| $Z_{replica}$ | Forward replica reach in the loop impedance plane = $Z(1+kZN.IN/Iph+kZM.IM/Iph)$ |
| $Z'_{replica}$ | Reverse replica reach in the loop impedance plane = $Z'(1+kZN.IN/Iph+kZM.IM/Iph)$ |
| $Z_S$ | Source impedance |
| $\sigma$ | An angle (in degrees) usually associated with the tilt of a reactive line on a Quadrilateral characteristic |
| $\angle\sigma$ | A vectorial operator that rotates a vector quantity by an angle of $\sigma^o$ (alternative representation $e^{j\sigma}$) |

*Note:*
*The faulted phase current (I) is generally used as the reference (0º) for the vector diagrams.*

### 6.3.1 MHO CHARACTERISTICS

There are different types of Mho characteristic, but two specific ones are well suited to introducing the defining principles. These are the directional Self-polarized Mho and the Offset Mho. Both types are used for both phase faults and earth faults.

In practice, self-polarized Mhos are rarely used since voltage collapses for close-up faults render self-polarization unreliable. Rather, memory-polarization components and/or cross-polarization components are usually used to provide a polarizing reference. Directional Self-Polarized Mhos, however, are simpler to understand and are used by way of introduction.

Mho characteristics are available for phase and earth-fault protection. A mix of Directional Forward, Directional Reverse, and Offset characteristics are available. Zone 1 and Zone 4 are settable as Forward or Reverse. Zones 2, 3, P and Q are settable as Forward or Reverse or Offset.

**Caution:**
**Zone 1,2 and 4 are required to implement the *PUR*/*POR* and Blocking Aided Schemes. In this case, zone 1 and zone 2 should be forward and zone 4 should be reverse. Therefore, if the relay's *Setting Mode* is set to *Advanced* and any Zone direction has been selected that compromises the Aided Schemes, then the Aided Distance Schemes should be forced to be disabled by the user.**

#### 6.3.1.1 DIRECTIONAL MHO CHARACTERISTIC FOR PHASE FAULTS

The following diagram illustrates how the Directional Self-Polarized Mho characteristic for phase Distance protection is created.

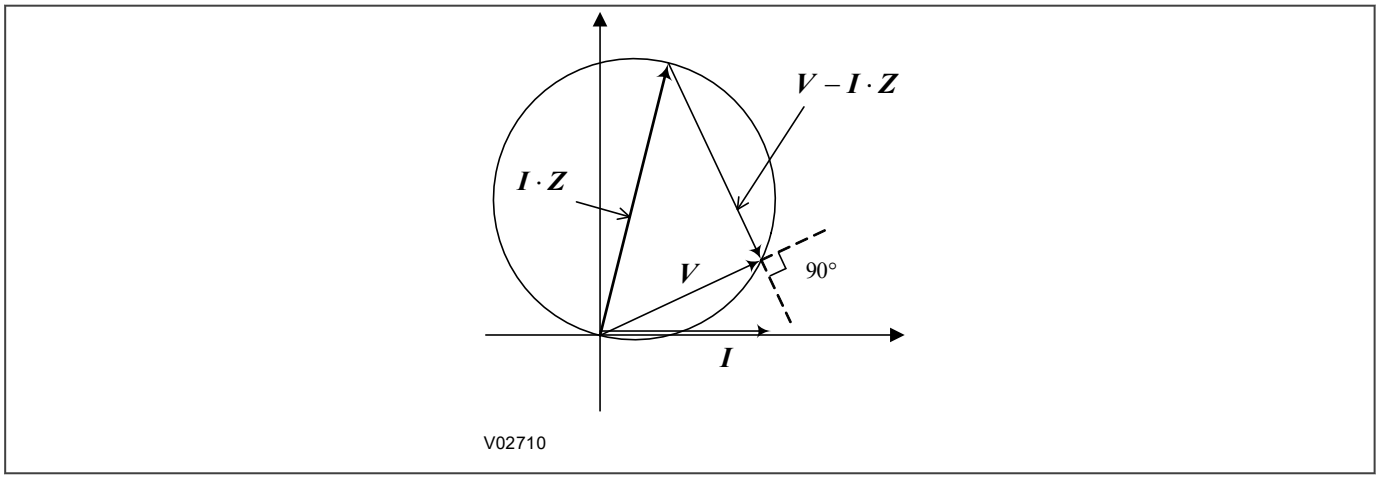



**Figure 38: Directional mho element construction**

The two signals provided to the comparator are:

$S_1 = V$

$S_2 = V - I.Z$

Operation occurs when the angle between the signals is greater than 90°

### 6.3.1.2 OFFSET MHO CHARACTERISTIC FOR PHASE FAULTS

The following diagram illustrates how the Offset Mho characteristic for phase Distance protection is created:

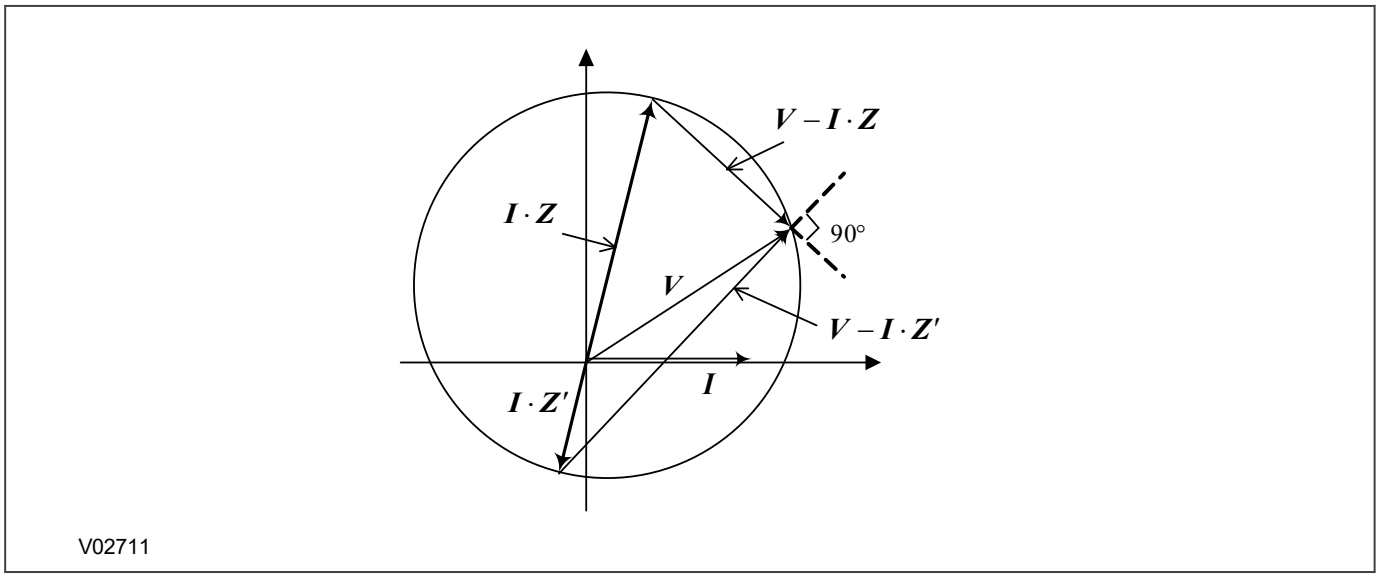



**Figure 39: Offset Mho characteristic**

The two signals provided to the comparator are:

$S_1 = V - IZ'$

$S_2 = V - IZ$

Operation occurs when the angle between the signals is greater than 90°

### 6.3.1.3 DIRECTIONAL SELF-POLARIZED MHO CHARACTERISTIC FOR EARTH FAULTS

Characteristics of earth-fault elements can be represented in two different complex planes - the positive sequence impedance plane ($Z_1$ -plane) and the loop impedance plane ($Z_{LP}$ -plane). The reach impedance setting defines the reach in positive sequence impedance terms. The characteristic in the $Z_{LP}$ -plane is generally dynamic because it depends on fault currents. However, the $Z_{LP}$–plane representation is often more convenient for reference, especially if an injection test kit is used, which cannot apply the residual compensation to the impedance plot, or in the case that the load blinders have to be verified.

The following diagram illustrates how a directional Mho characteristic for earth-faults is created.

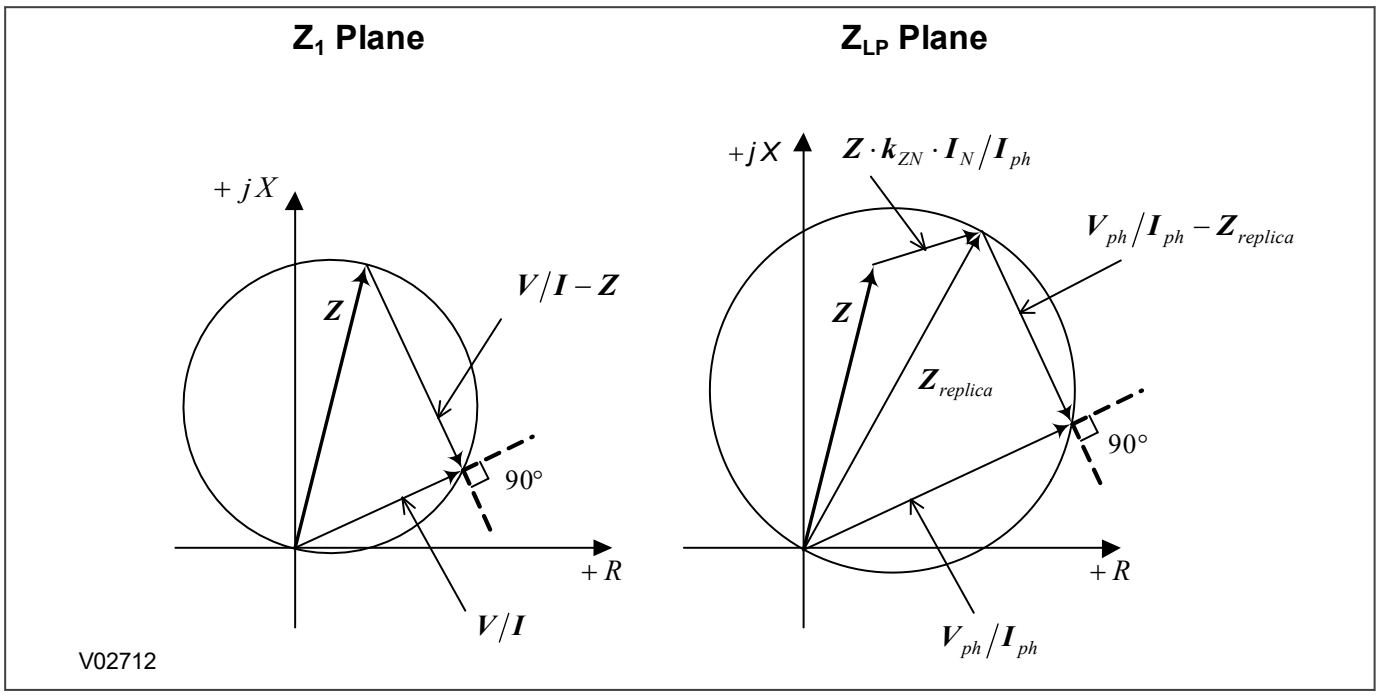



**Figure 40: Directional Mho element construction – impedance domain**

The two signals provided to the comparator are:

$S_1 = V$

$S_2 = V - IZ$

where (for an A-N fault for example) with residual compensation applied:

$V = V_A$

$I = I_A + k_{ZN}.I_N$

where $k_{ZN} = (Z_0 - Z_1) / 3Z_1$ and is defined by two settings: ***kZN Res Comp*** and ***KZN Res Angle***.

and if mutual compensation is applied:

$I = I_A + k_{ZN}.I_N + k_{ZM}.I_M$

where $k_{ZM} = 3Z_M / 3Z_1$ and is defined by two settings: ***kZm Mutual Set*** and ***kZm Mutual Angle***.

Operation occurs when the angle between the signals is greater than 90°.

To obtain a $Z_{LP}$-plane representation in the directional Mho element construction, V is replaced with $V_{ph}$ and I is replaced with $I_{ph} + k_{ZN}.I_N$, where $V_{ph}$ and $I_{ph}$ are the faulty phase voltage and current respectively (assuming no mutual current compensation).

The two signals provided to the comparator in this case are:

$S_1 = V_{ph}$

$S_2 = V_{ph} - I_{ph}.Z(1+k_{ZN}.I_N/I_{ph})$

We can define a replica impedance reach, $Z_{replica}$, as:

$Z_{replica} = Z(1+k_{ZN}.I_N/I_{ph})$

or if mutual compensation is applied:

$$Z(1+k_{ZN}.I_N/I_{ph}+k_{ZM}.I_M/I_{ph})$$

Then if healthy phase currents are much less then the current of the faulty phase and the mutual compensation is disabled:

$$I_N \cong I_{ph}$$

so that

$$Z_{replica} \cong Z(1 + k_{ZN})$$

Thus the $Z_{LP}$ plane representation of the characteristic becomes static.

#### 6.3.1.4 OFFSET MHO CHARACTERISTIC FOR EARTH FAULTS

The diagram below illustrates how the Offset Mho characteristic for earth-fault distance protection is created in the impedance domain.

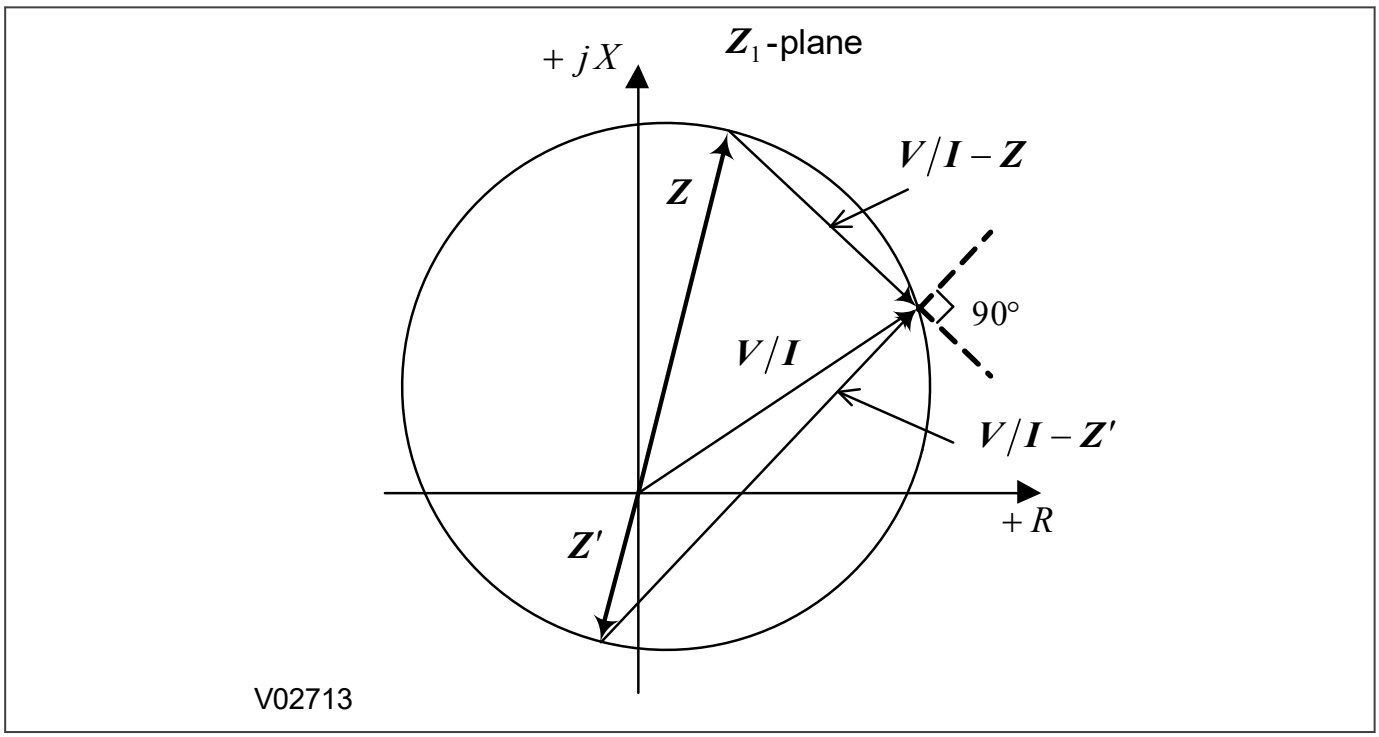



**Figure 41: Offset Mho characteristics – impedance domain**

The two signals provided to the comparator are:

$$S_1 = V - I.Z'$$

$$S_2 = V - I.Z$$

Operation occurs when the angle between the signals is greater than 90°.

The following diagram below how the Offset Mho characteristic for earth-fault distance protection translates to the loop impedance domain.

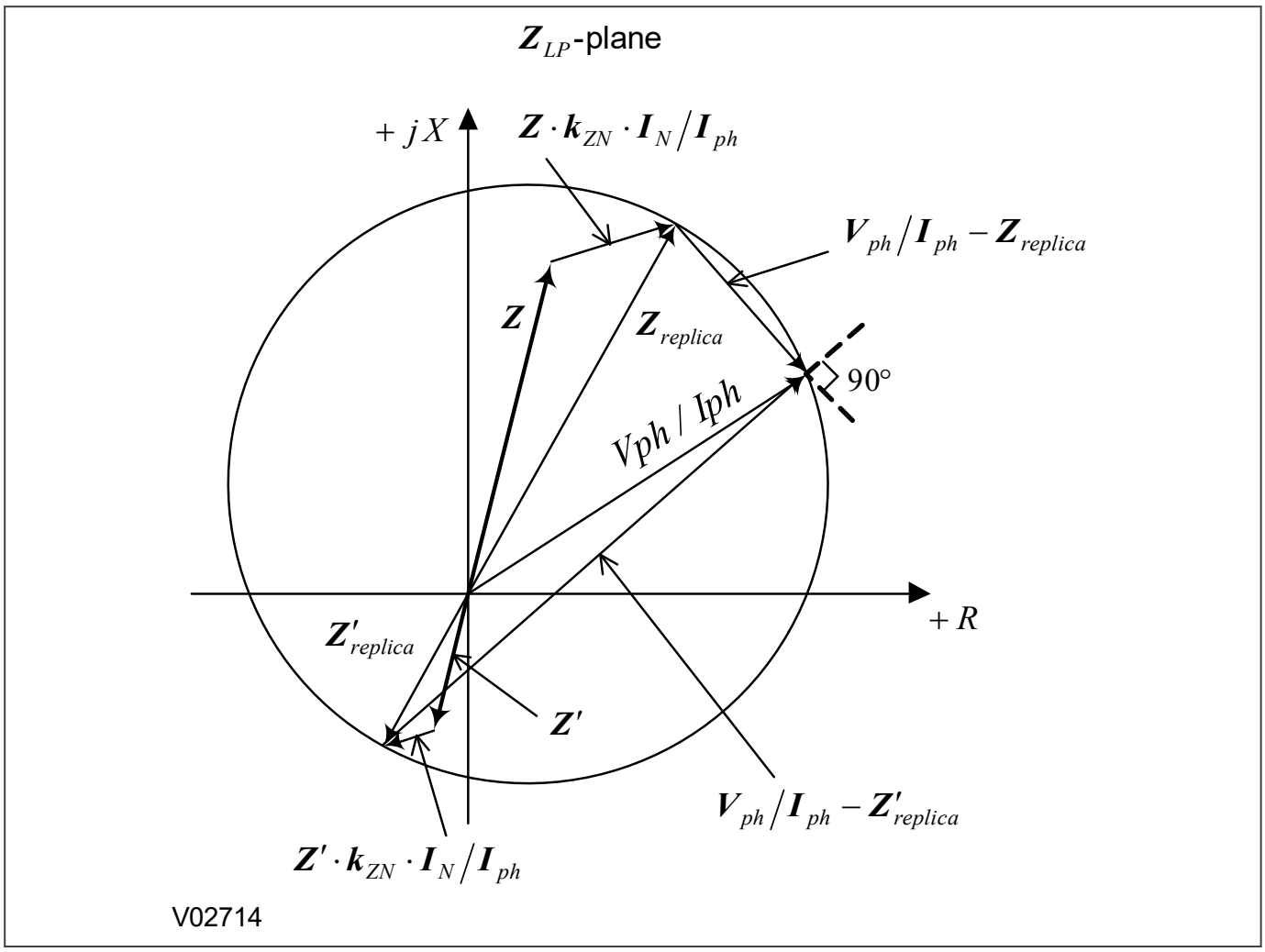



**Figure 42: Offset mho characteristics – voltage domain**

where: $Z_{replica}$ is the replica forward reach and $Z'_{replica}$ is the replica reverse reach.

With mutual compensation applied:

$$Z_{replica} = Z(1+k_{ZN}.I_N/I_{ph} + k_{ZM}.I_M/I_{ph})$$

$$Z'_{replica} = Z'(1+k_{ZN}.I_N/I_{ph} + k_{ZM}.I_M/I_{ph})$$

If the healthy phase currents are much less than the current of the faulty phase, then the neutral current is approximately the same as the phase current, and the terms can be simplified as follows:

$$Z_{replica} = Z(1+k_{ZN} + k_{ZM}.I_M/I_{ph})$$

$$Z'_{replica} = Z'(1+k_{ZN} + k_{ZM}.I_M/I_{ph})$$

If the healthy phase currents are much less than the current of the faulty phase, and mutual current compensation is not applied, then these terms can be simplified as follows:

$$Z_{replica} \cong Z(1+k_{ZN})$$

$$Z'_{replica} \cong Z'(1+k_{ZN})$$

So, as with the Directional Self-Polarized Mho characteristic for earth-faults, the $Z_{LP}$ plane representation of the characteristic becomes static.

### 6.3.1.5 MEMORY POLARIZATION OF MHO CHARACTERISTICS

Self-Polarized Directional Mho characteristics require sufficient polarizing voltage to detect the voltage angle. Therefore such a characteristic is unable to operate for close-up faults where there would be insufficient polarizing voltage. To ensure the correct Mho element response for zero-voltage faults, the protection algorithm adds a percentage of voltage from the memory to the main polarizing voltage as a substitute phase reference.

This technique is called memory polarizing. Not only does it preserve the directional property of the Mho characteristic, it actually enhances it by dynamically expanding or contracting the characteristic.

*Note:*
*The **Force No Mem.** DDB may be used to force the relay to work as if the memory time has elapsed, i.e. a combination of self and cross polarisation voltage.*

*Note:*
*The **Self Pol** DDB indicates when the relay is working with voltage self polarization.*

### 6.3.1.6 DYNAMIC MHO EXPANSION AND CONTRACTION

The signals provided to the Mho comparators for memory polarization are:

$$S_1 = V + pV_{mem}$$

$$S_2 = V - IZ$$

where:

- V is the self-polarization voltage
- $V_{mem}$ is the memory polarization voltage

Operation occurs when the angle between the signals is greater than 90°.

The memory voltage $V_{mem}$ is the pre-fault voltage. Assuming the pre-fault current is close to zero at the relaying point, he pre-fault voltage is equal to the source voltage. Therefore:

$$V_{mem} = V_S$$

#### Dynamic Mho Expansion for Forward Faults

The contribution of additional polarizing input creates dynamic Mho expansion for forward faults and increases the fault arc resistance coverage.

Referring to the diagram below:

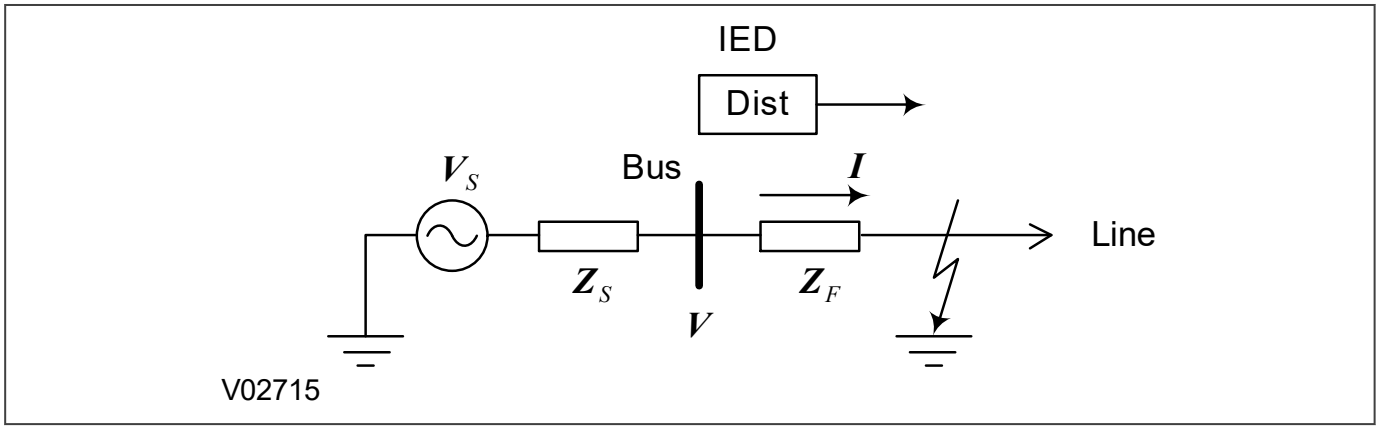



**Figure 43: Simplified forward fault**

For a fault condition we can write the following equations:

$$V_S = V + I.Z_S$$

$$90° \le \angle\left( V/I + \frac{p}{1+p} \cdot Z_s \right) - \angle\left(V/I - Z\right) \le -90°$$

The Mho expansion for a forward fault is illustrated in the following diagram:

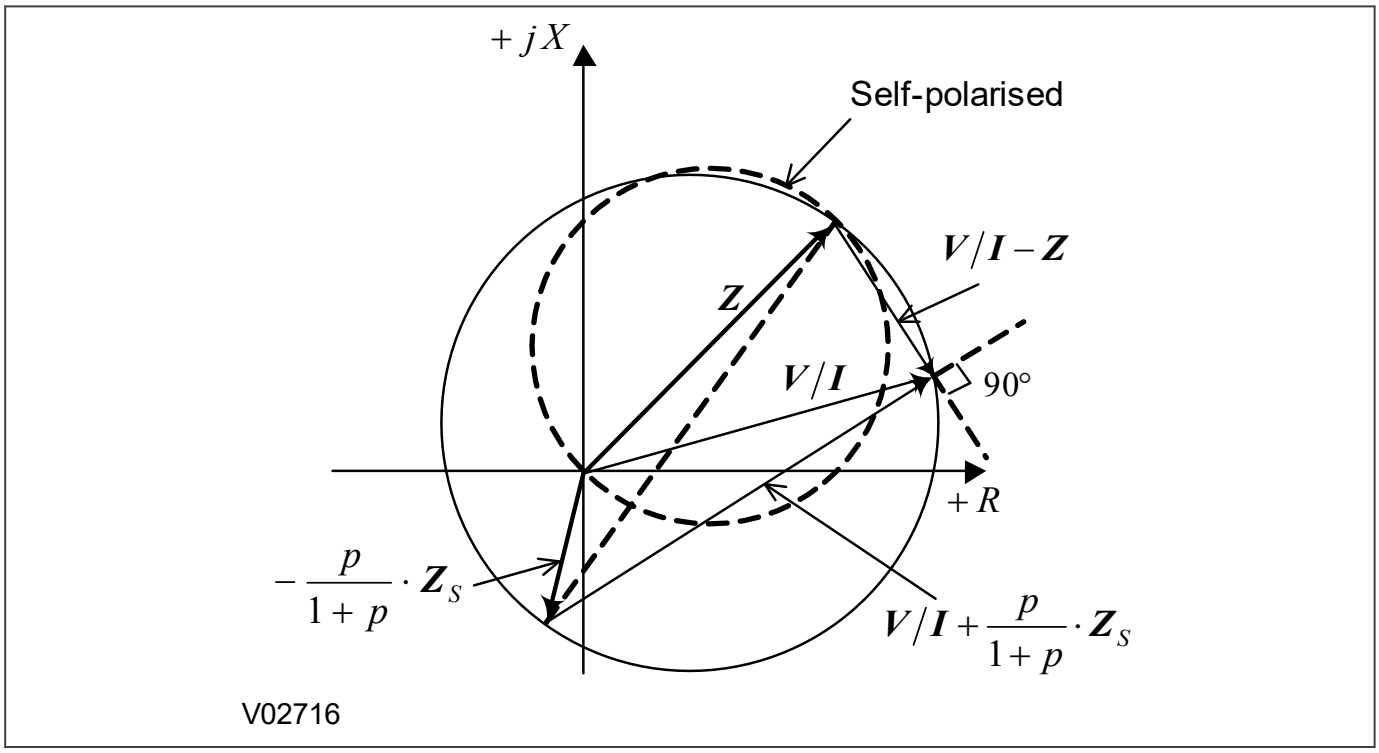



**Figure 44: Mho expansion - forward fault**

The Mho expansion associated with forward faults is as follows:

$$\text{Mho Expansion} = Z_S.p/(1 + p)$$

where $Z_S$ is the impedance of the source behind the relaying point.

Using the source and line impedances is a simple way of representing the Mho expansion. The protection algorithm does not calculate $Z_S$ internally, it only deals with the signals $S_1$ and $S_2$ provided to the Mho comparators. In some cases the source and line impedances are different from their actual values used in various power system studies. This is mainly due to pre-fault current and the residual compensation for phase-to-ground loops. To plot an accurate impedance characteristic, calculate the values of $Z_S$ as follows:

$$Z_S = (V_{mem} - V)/I$$

### Dynamic Mho Contraction for Reverse Faults

The contribution of additional polarizing input creates dynamic Mho contraction for reverse faults and enhances the directional decision

Referring to the following diagram:

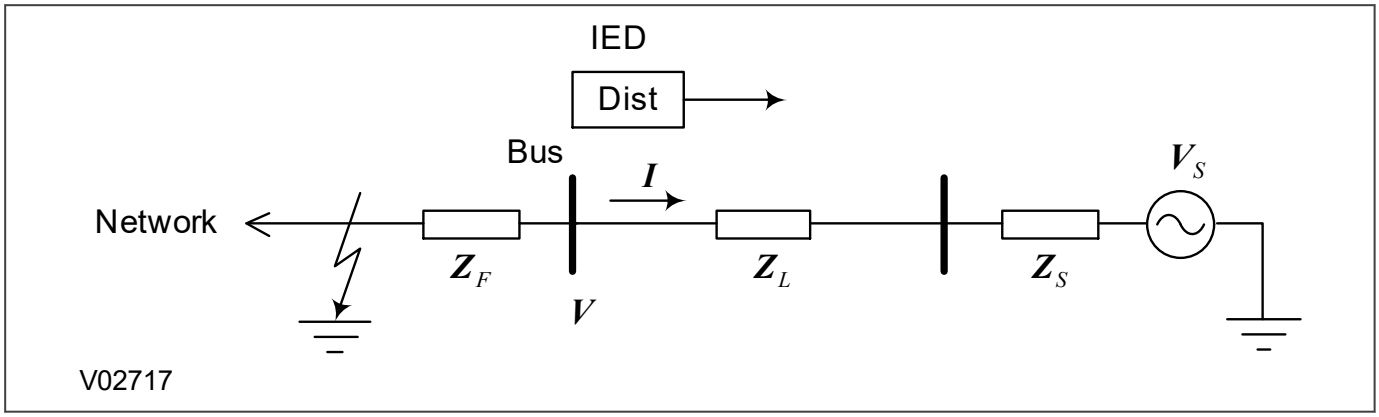



**Figure 45: Simplified Reverse Fault**

For a fault condition we can write the following equations:

$$V_S = V - I(Z_S + Z_L)$$

$$90° \le \angle\left( V/I - \frac{p}{1+p} \cdot (Z_S + Z_L) \right) - \angle(V/I - Z) \le -90°$$

The Mho contraction for a reverse fault is illustrated in the following diagram:

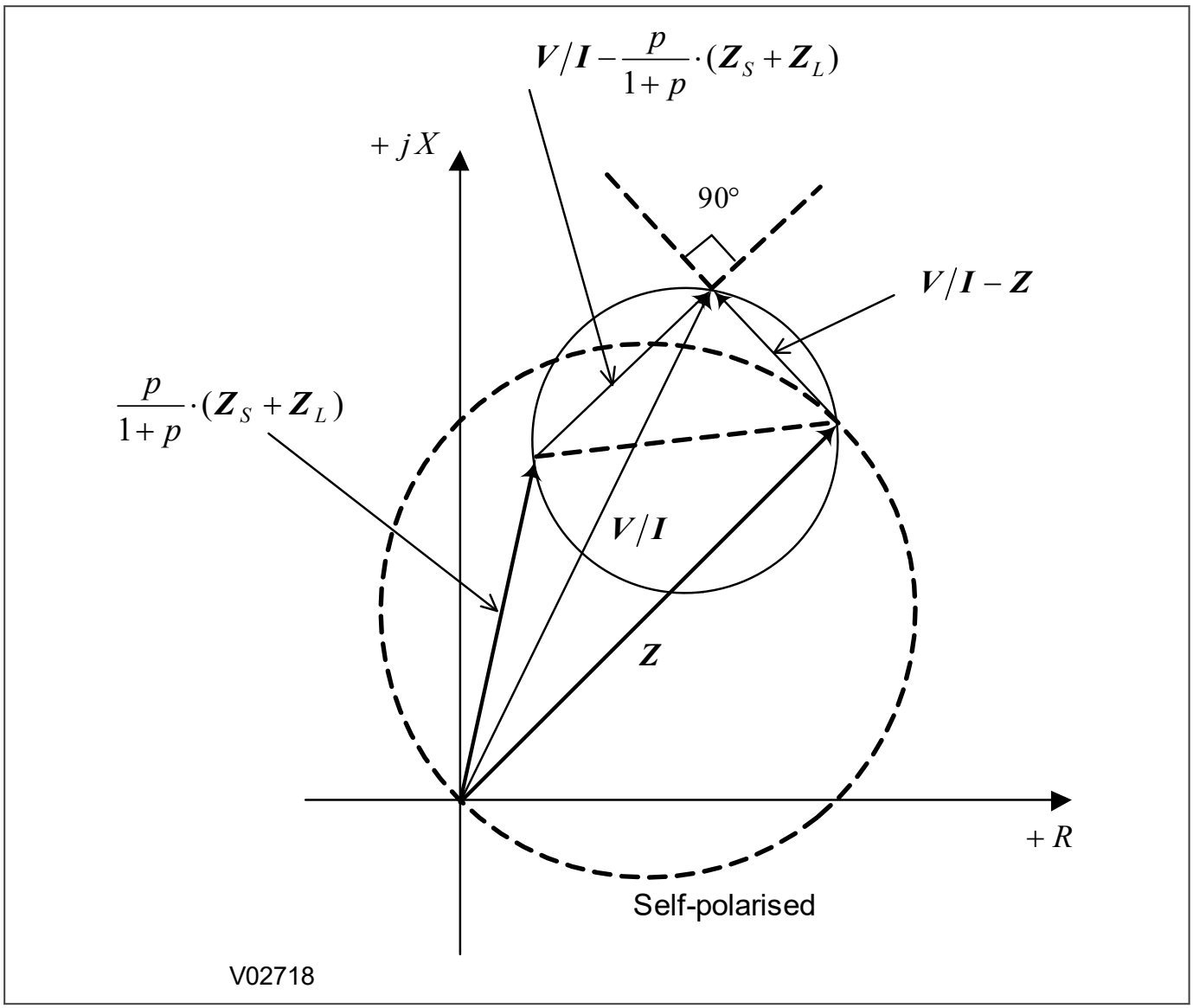



**Figure 46: Mho contraction – reverse fault**

The Mho contraction associated with reverse faults is as follows:

$$\text{Mho Contraction} = (Z_S + Z_L).p/(1 + p)$$

where $Z_S + Z_L$ is the impedance of the line and the source ahead of the relaying point.

Using the source and line impedances is a simple way of representing the Mho contraction. The protection does not calculate $Z_S + Z_L$ internally, it only deals with the signals $S_1$ and $S_2$ provided to the Mho comparators. In some cases the source and line impedances are different from their actual values used in various power system studies. This is mainly due to pre-fault current and the residual compensation for phase-to-ground loops. To plot an accurate impedance characteristic, calculate the values of $Z_S + Z_L$ as follows:

$$Z_S + Z_L = (V - V_{mem})/I$$

### 6.3.1.7 CROSS POLARIZATION OF MHO CHARACTERISTICS

If the voltage collapses on a faulted phase, it may be possible to use healthy phase voltage components to derive a polarizing signal to make the directional decision. This process is called cross-polarization.

The cross-polarization voltage is generated using phase(s) not otherwise used for the particular distance or directional measurement. While one pole is dead, and the memory is not available, the elements associated with the remaining phases are polarized as shown in the following table:

| Loop | Cross Polarizing Signal (No Poles Dead) | Cross Polarizing if a Pole is Dead |
|---|---|---|
| A-N | $0.5(\alpha VB + \alpha^2 VC)$ | $\alpha VB$ if C pole is dead or $\alpha^2 VC$ if B pole is dead |
| B-N | $0.5(\alpha VC + \alpha^2 VA)$ | $\alpha VC$ if A pole is dead or $\alpha^2 VA$ if C pole is dead |
| C-N | $0.5(\alpha VA + \alpha^2 VB)$ | $\alpha VA$ if B pole is dead or $\alpha^2 VB$ if A pole is dead |
| A-B | $\sqrt{3}VC \angle -90°$ | 0 |
| B-C | $\sqrt{3}VA \angle -90°$ | 0 |
| C-A | $\sqrt{3}VB \angle -90°$ | 0 |

Where $\alpha$ is a mathematical operator which rotates a vector through 120° and $\alpha^2$ denotes a rotation of 240°.

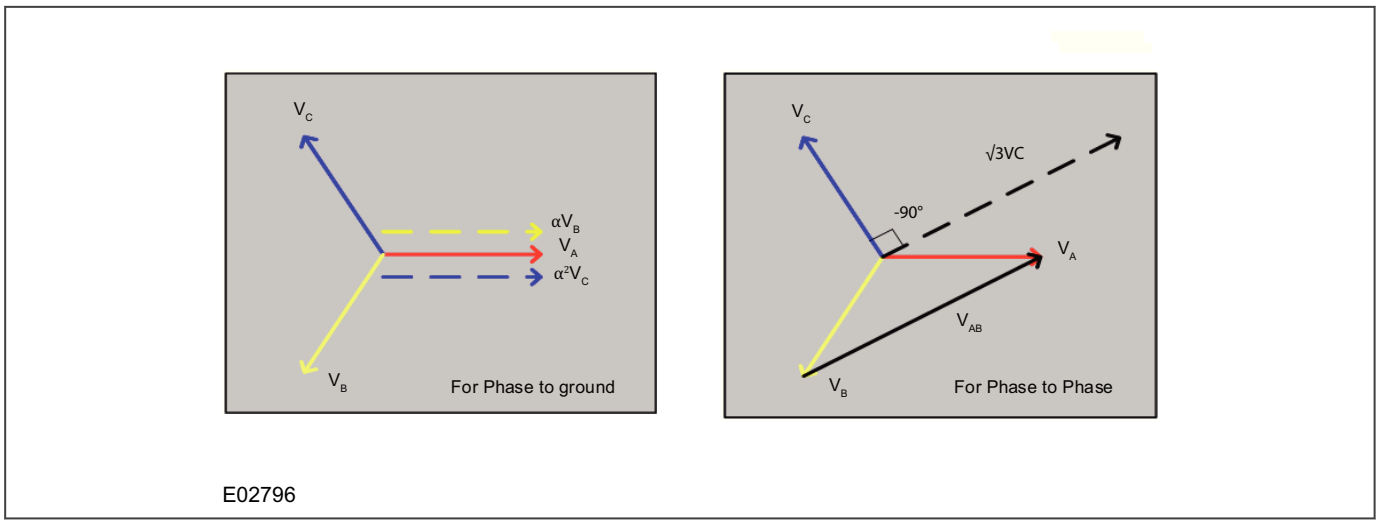



**Figure 47: Cross polarizing voltage for phase to ground and phase to phase faults**

The table and diagram shows polarizing signal contributions for each loop under the different operating conditions. The proportion of cross-polarization voltage used is defined by the ***Dist. Polarizing*** (p) setting.

*Note:*
*Cross polarization is used only when there is no memory polarization quantity available.*

### 6.3.1.8 IMPLEMENTATION OF MHO POLARIZATION

This product does not allow the directional Mho characteristics to be purely self-polarized or purely memory-polarized. The polarizing voltage always contains the directly measured self-polarized voltage, onto which a percentage of the pre-fault memory voltage is added.

*Note:*
*If no memory voltage is available or* ***Force No Mem.*** *is set, then the cross-polarized quantity is used instead.*

The setting ***Dist. Polarizing*** (p) defines the amount of memory polarization (or if need be, cross polarization voltage), which should be added with respect to the existing self-polarizing voltage so that:

$$S_1 = V + pV_{mem}.$$

The value "p" can be set from 0.2 (20%) to 5 (500%).

This will have an affect on the characteristic where operation occurs when the fault impedance lies inside a circle whose diameter is set by the points IZ and $p/(1+p)IZ_{source}$

This means for example:

- If p = 1, the characteristic will have an expansion of 50% $I_{Zsource}$
- If p = 5, the characteristic will have an expansion of 83.3% $I_{Zsource}$

The memory algorithm works as follows:

1. Memory voltage is stored for two cycles after line energisation, whereafter the voltage signals are considered valid and stored in the voltage memory buffers. The voltage memory used for polarizing is taken from a buffer corresponding to a value taken two cycles previously, so the voltage memory can be used after four cycles following line energisation.
2. Following fault inception, voltage signals buffered in the polarizing memory can be recycled and re-used for a period set with the ***Mem Volt Dura*** setting. This can be set between 16 and 32 cycles.
3. If a power swing condition is detected, the voltage memory signal expires after a reduced period of 3.2 cycles.
4. If the fault is cleared before the voltage memory signal expires, the memory algorithm resets and restarts the two/four cycle validation process.
5. If there is no voltage memory available (either because the line has just been energised, or because the memory voltage has expired), cross polarization is used instead. The contribution of cross polarizing signals is only used when memory polarizing is invalid and is only valid for certain pole dead conditions.
6. If neither memory polarization voltage nor cross-polarization voltage is available (pole dead condition for phase-to-phase element), then the phase-to-phase elements are self polarized. If the polarizing voltage is less than 1V, only zone 1 is allowed to operate. In this case a Mho characteristic with a reverse offset of 25% is applied. This ensures operation when closing on to a close-up three-phase fault (SOTF/ TOR condition).

One of the additional benefits of adding memory into the polarizing mix is that Mho characteristics offer dynamic expansion if there is a forward fault, therefore covering greater fault arc resistance

### 6.3.2 QUADRILATERAL CHARACTERISTIC

A number of zones are provided to make up the Quadrilateral characteristics. The following diagram shows examples of Directional Forward, Directional Reverse, and Offset zones. Zone 1 and Zone 4 are settable as Forward or Reverse. Zones 2, 3, P and Q are settable as Forward or Reverse or Offset:

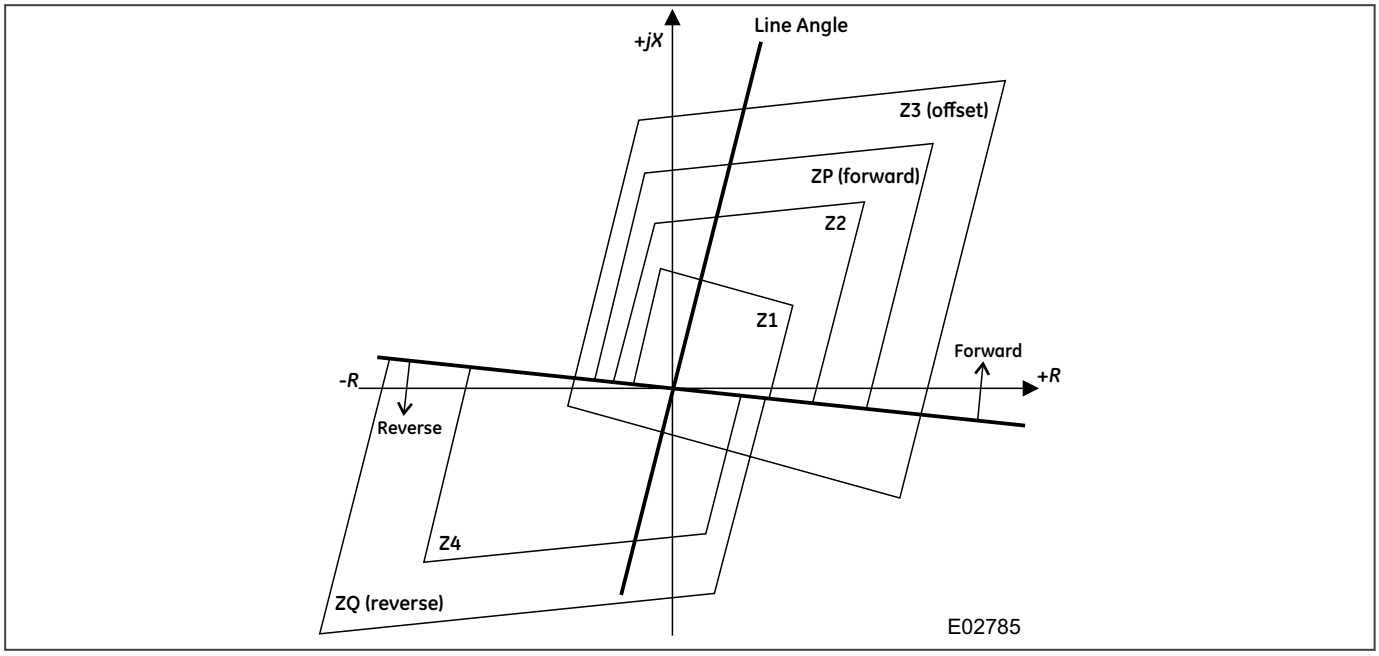



**Figure 48: Simplified quadrilateral characteristics**

Programmable zones (zone P and Q) are also available.

A combination of simple comparators, each using signals derived from measured currents and voltages, determines whether measured impedance is within a tripping zone. A separate comparator is used for each line of each Quadrilateral.

Each tripping zone is constructed from a Quadrilateral based on that depicted in the following diagram:

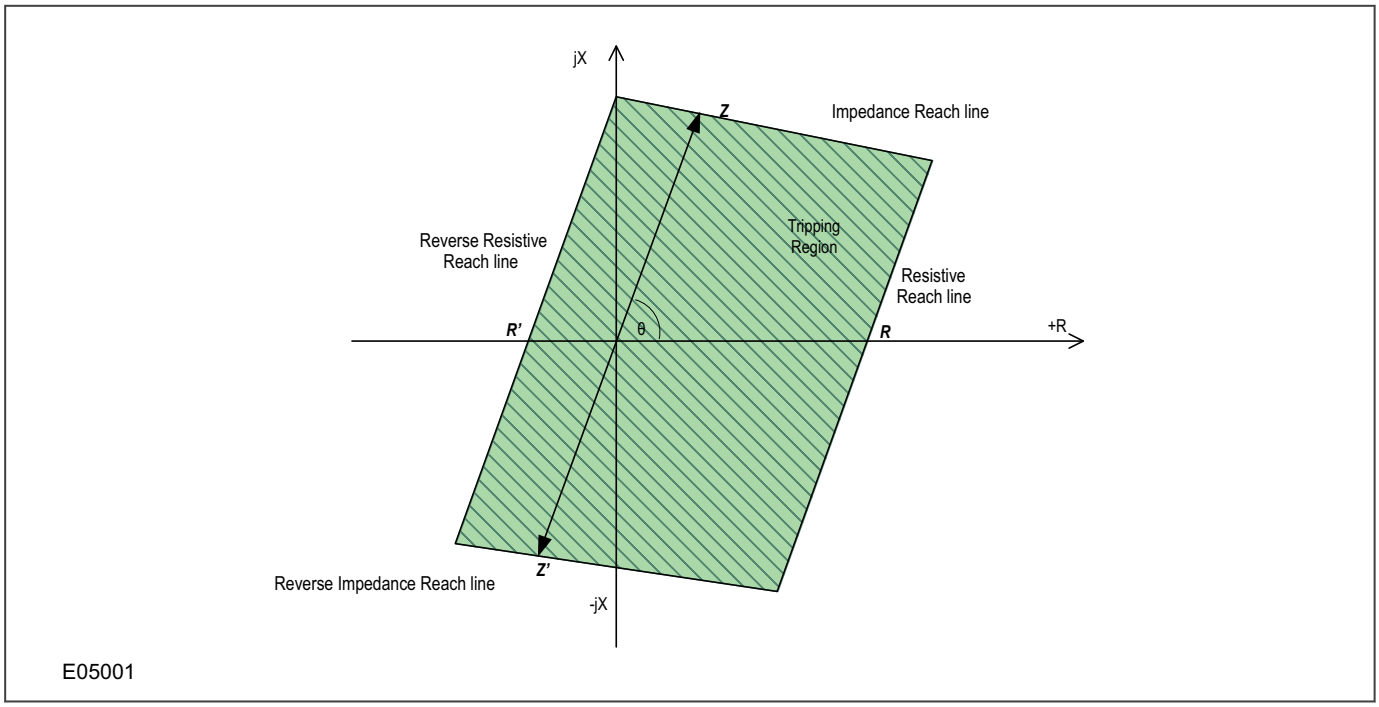



**Figure 49: General Quadrilateral Characteristic Limits**

In the figure, an Offset Quadrilateral characteristic is defined by its Impedance Reach, Z, (and Reverse Impedance Reach, Z'), its Resistive Reach, R, (and Reverse Resistive Reach, R'), and the zone angle (θ).

The two near-horizontal lines (Impedance Reach Line and Reverse Impedance Reach Line) set the reactive impedance limits of the tripping zone. The two near-vertical lines (Resistive Reach Line and Reverse Resistive Reach Line) set the resistive impedance limits.

The Resistive Reach Lines (also called Resistive Blinders) are parallel and set at the angle of the zone's characteristic impedance.

The Impedance Reach Lines exhibit a characteristic tilt (slope). A line that tilts to reduce the reactive reach (negative tilt/tilt down) encourages underreaching; A line that tilts to increase the reactive reach (positive tilt/tilt up) encourages overreaching. The tilt can be used to reinforce the overreaching/underreaching requirements of the zone. For example, for an underreaching Forward zone, a negative tilt will ensure that the measurement continues to underreach, even with increasing fault resistance.

The Impedance Reach, Z, and the Resistive Reach, R, apply in the context of the direction of the protection. For a Forward Zone, or an Offset Zone, Z and R look into the protected plant. For a Reverse Zone, Z and R look behind the protected plant. Reactive Line tilts follow the same convention.

### 6.3.2.1 DIRECTIONAL QUADRILATERALS

A Directional Line overlaid onto an Offset characteristic is used to create a Directional one as shown in the following figure:

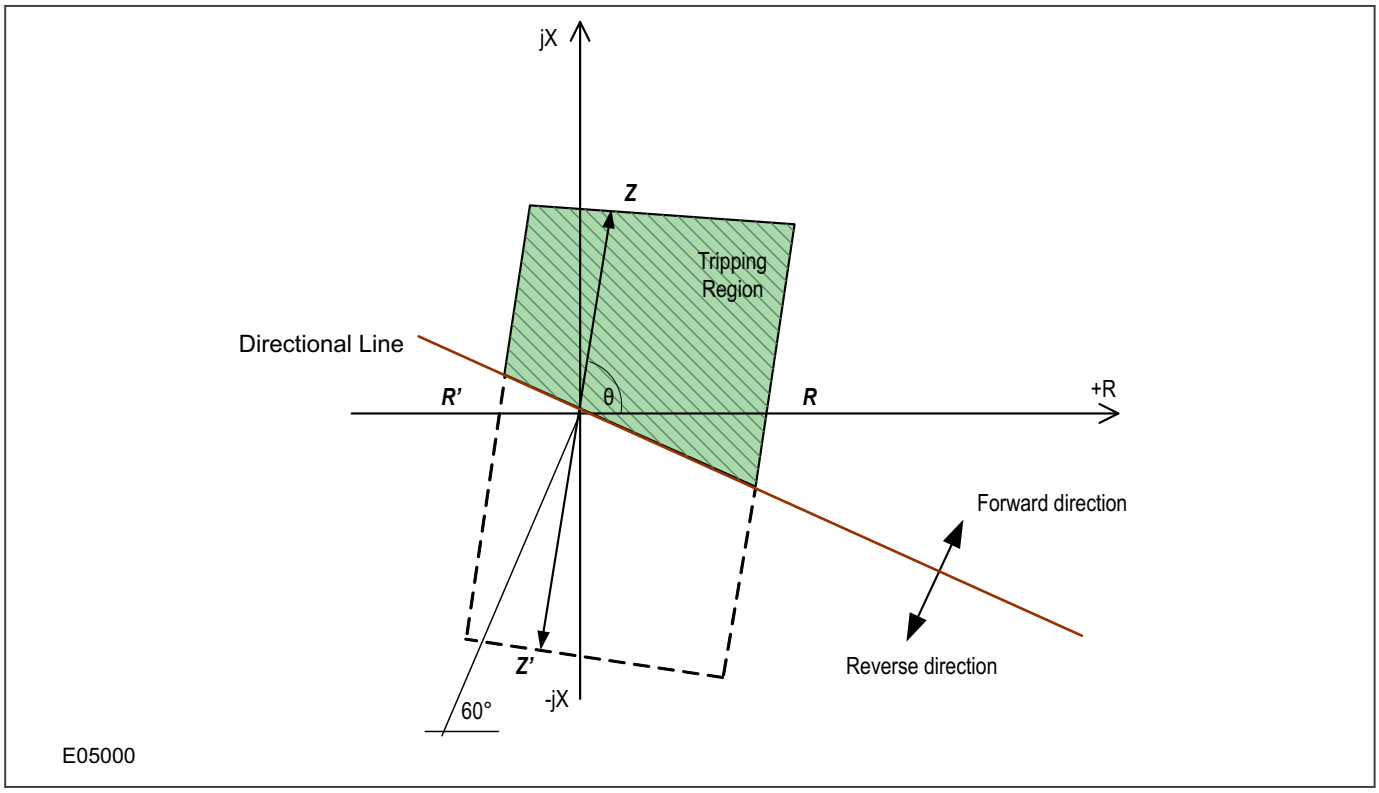



**Figure 50: Directional Quadrilateral Characteristic**

This product has a Delta Directional element that is normally used to directionalise the Distance protection.

By default, the Delta Directional element is enabled (***Dir. Status*** in *DELTADIRECTIONAL* set to `Enabled`). In this case, the Directional Line for the Quadrilateral is derived using superimposed fault-current (Delta I). When using the Delta Directional element, the Directional Line angle has a default value of 60º, but you can change it with the ***Dir. Char Angle*** setting.

If you want to use a conventional directional technique, then you can do this by disabling the Delta Directional element. The protection will then use a conventional directional element with a fixed angle of 60º. If the conventional directional decision is used, the directional elements are polarized by a mix of self (actual) and memory voltage.

The polarizing voltage always contains self-polarized voltage and a percentage of the pre-fault memory voltage. The setting ***Dist. Polarizing*** varies from `0.2` (20%) to `5` (500%) and defines the proportion between self-polarizing voltage and memory-polarizing voltage used for the directional voltage polarization as follows:

V polarising = Vself-polarizing/***Dist. Polarizing*** + V memory-polarizing

As it can be seen from the formula, the higher the setting ***Dist. Polarizing***, the higher the value of memory-polarizing voltage used.

Once the memory expires, the value of V memory-polarising is replaced by V cross-polarising cross as shown in the following table:

| Loop | Cross Polarizing Signal (No poles dead) | Cross Polarizing Signal Lagging Pole Dead | Cross Polarizing Signal Leading Pole Dead |
|---|---|---|---|
| A-N | $0.5(\alpha VB + \alpha^2 VC)$ | αVB | α2VC |
| B-N | $0.5(\alpha VC + \alpha^2 VA)$ | αVC | α2VA |
| C-N | $0.5(\alpha VA + \alpha^2 VB)$ | αVA | α2VB |
| A-B | $\sqrt{3}VC \angle -90°$ | 0 | 0 |
| B-C | $\sqrt{3}VA \angle -90°$ | 0 | 0 |
| C-A | $\sqrt{3}VB \angle -90°$ | 0 | 0 |

If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Disabled`, we recommend a setting of `1` (100%) for correct directionality in typical applications.

The relay has the facility to deter the use of memory, with the ***Force No Mem.*** DDB. This DDB forces the relay to work without voltage memory polarization, making it operate as if the voltage memory timer ***Mem Volt Dura*** has expired.

The following figure illustrates two Offset zones that have been converted into Directional Forward zones by the overlay of a Directional Line. An Offset zone is also shown for reference.

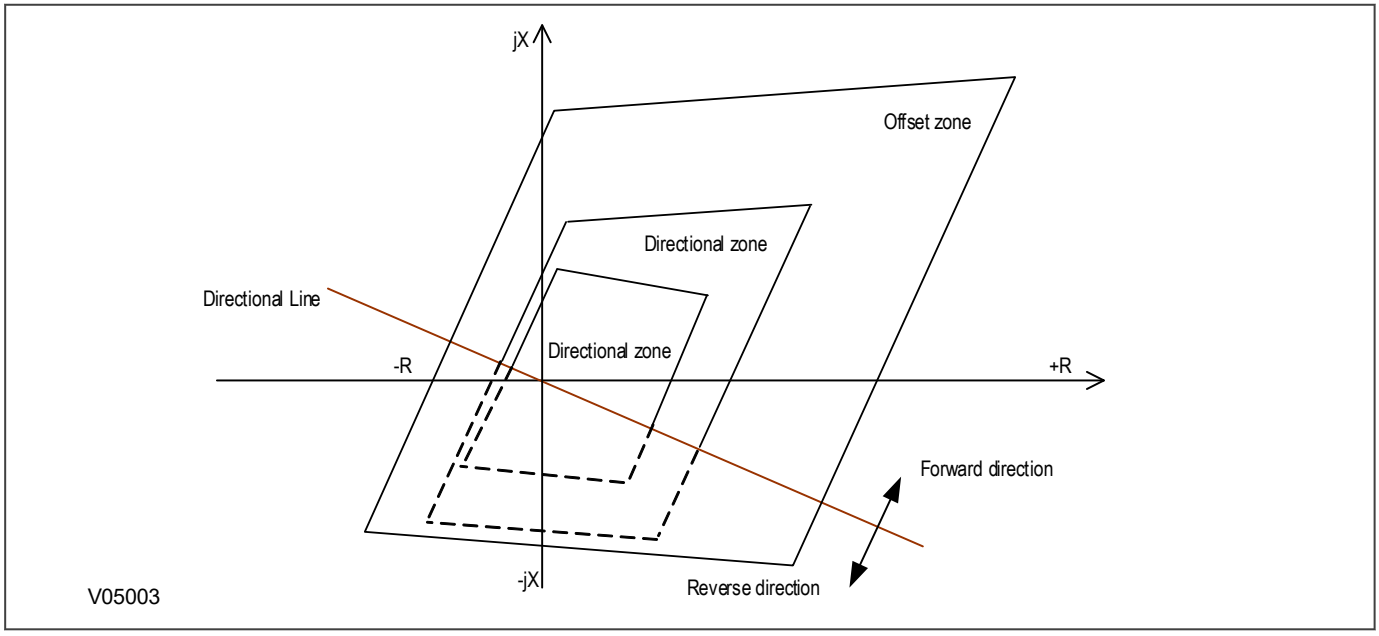



**Figure 51: Quadrilateral Characteristic featuring 2 directional forward zones and 1 offset zone**

### Directional Quadrilateral Limits

The implementation of Directional Quadrilaterals in this product produces Directional Zone characteristics that are formed by the combination of five comparators. Each comparator produces a straight line on the complex impedance plane. The lines produced are:

- Impedance Reach Line
- Reverse Impedance Reach Line
- Resistance Reach Line
- Reverse Resistance Reach Line
- Directional Line.

Each of the lines produced by the comparators defines a tripping limit: Impedance on one side of the line prevents tripping whereas impedance on the other side of the line may, if the other comparators agree, allow tripping. For example, impedance beyond the Impedance Reach Line will not allow tripping.

The combination of the comparator outputs produces a polygon shaped tripping region. The polygon may be either 4-sided or 5-sided. The shape depends according to the settings that are applied by the five comparators and how the Directional Line interacts with the reach lines (usually the Reverse Impedance Reach Line):

- The Directional Line may completely mask a reach line. If that is the case, the polygon will be 4-sided (quadrilateral).
- If the Directional Line intersects a reach line, the polygon will be 5-sided.

Creation of a 5-sided polygon is illustrated in the following figure:

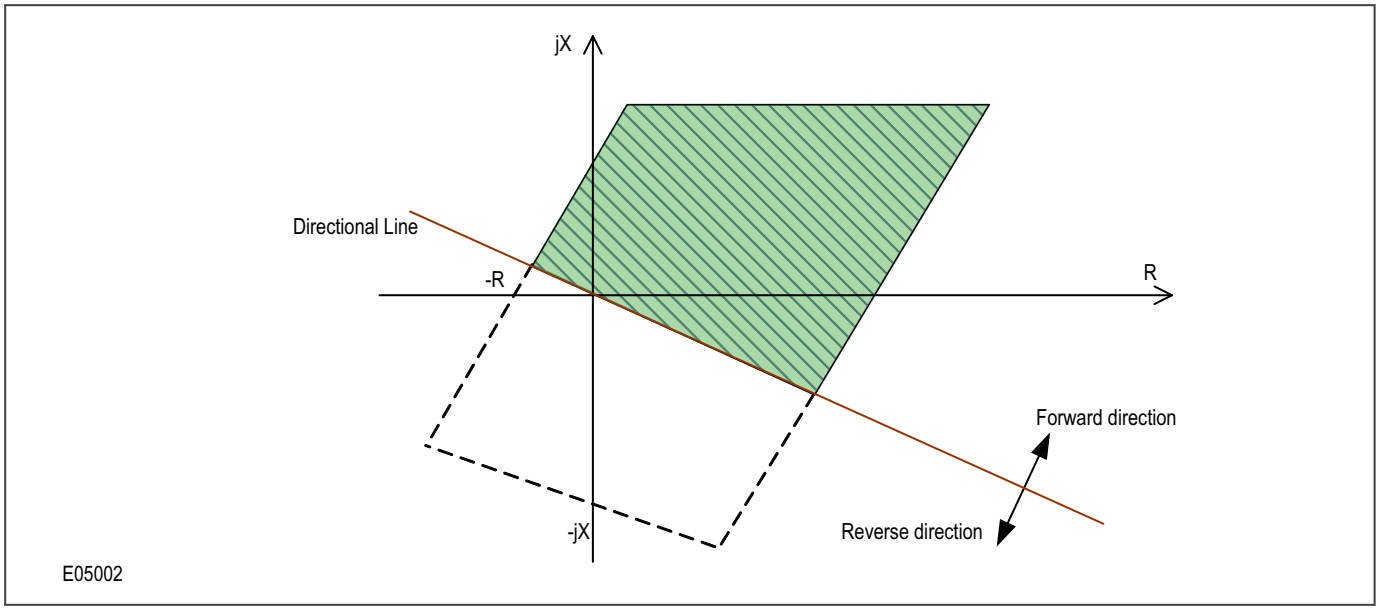



**Figure 52: Five-sided polygon formed by Quadrilateral characteristic with Directional-Line intersection of Reverse Impedance Reach Line**

The applied settings will determine the intersection point. When the settings have been chosen, the following values will affect the line intersection point:

- Impedance Reach
- Reverse Impedance Reach
- Resistive Reach

- Reverse Resistive Reach
- Directional Line Angle
- Zone Characteristic Impedance Angle
- Tilt Angles of Impedance Reach Lines

The Impedance Reach, the Resistive Reach, and the Zone Characteristic Impedance Angle, can be freely assigned. The Directional Line Angle is 60º by default but can be varied if the Delta Directional element is enabled. The Tilt Angle of the impedance lines has a default setting of -3º, but some variation is allowed if the Advanced setting option is chosen.

The Reverse Impedance Reach, and the Reverse Resistive Reach are applied as a fixed ratio of the Impedance Reach and the Resistive Reach for Directional characteristics. The ratios used vary according to the zone type. The following tables present the different values for phase-phase characteristics and phase-earth characteristics. For completion, the reach limit values for Offset zones are also included (although the overlaid Directional line does not apply and the Offset characteristics will always be quadrilateral).

### Phase-to-phase Element Reaches

| Zone | Type | Impedance Reach Z | Reverse Impedance Reach Z' | Resistive Reach R | Reverse Resistive Reach R' |
|---|---|---|---|---|---|
| 1 Ph-Ph | Forward or Reverse | Z1 Ph. Reach | Z | ½*R1 Ph. Resistive | 0.25 R |
| 2 Ph-Ph | Forward or Reverse | Z2 Ph. Reach | Z | ½*R2 Ph. Resistive | 0.25 R |
| 2 Ph-Ph | Offset | Z2 Ph. Reach | Z2' Ph Rev Reach | ½*R2 Ph. Resistive | ½*R2' Ph Res. Rev. |
| 3 Ph-Ph | Forward or Reverse | Z3 Ph. Reach | Z | ½*R3 Ph. Resistive | 0.25 R |
| 3 Ph-Ph | Offset | Z3 Ph. Reach | Z3' Ph Rev Reach | ½*R3 Ph. Resistive | ½*R3' Ph Res. Rev. |
| 4 Ph-Ph | Reverse or Forward | Z4 Ph. Reach | Z | ½*R4 Ph. Resistive | 0.25 R |
| P Ph-Ph | Forward or Reverse | ZP Ph. Reach | Z | ½*RP Ph Resistive | 0.25 R |
| P Ph-Ph | Offset | ZQ Ph. Reach | ZP' Ph Rev Reach | ½*RP Ph Resistive | ½*RP' Ph. Res. Rev. |
| Q Ph-Ph | Forward or Reverse | ZQ Ph. Reach | Z | ½*RQ Ph Resistive | 0.25 R |
| Q Ph-Ph | Offset | ZQ Ph. Reach | ZQ' Ph Rev Reach | ½*RQ Ph Resistive | ½*RQ' Ph. Res. Rev. |

### Phase-to-earth Element Reaches

| Zone | Type | Impedance Reach Z | Reverse Impedance Reach Z' | Resistive Reach R | Reverse Resistive Reach R' |
|---|---|---|---|---|---|
| 1 Ph-Earth | Forward or Reverse | Z1 Gnd. Reach * (1 + $k_{ZN}$) | Z | R1 Gnd Resistive | 0.25 R |
| 2 Ph-Earth | Forward or Reverse | Z2 Gnd. Reach * (1 + $k_{ZN}$) | Z | R2 Gnd Resistive | 0.25 R |
| 2 Ph-Earth | Offset | Z2 Gnd. Reach * (1 + $k_{ZN}$) | Z2' Gnd Rev Rch * (1 + $k_{ZN}$) | R2 Gnd Resistive | R2' Ph Res. Rev |
| 3 Ph-Earth | Forward or Reverse | Z3 Gnd. Reach * (1 + $k_{ZN}$) | Z | R3 Gnd Resistive | 0.25 R |
| 3 Ph-Earth | Offset | Z3 Gnd. Reach * (1 + $k_{ZN}$) | Z3' Gnd Rev Rch * (1 + $k_{ZN}$) | R3 Gnd Resistive | R3' Ph Res. Rev |
| 4 Ph-Earth | Reverse or Forward | Z4 Gnd. Reach * (1 + $k_{ZN}$) | Z | R4 Gnd Resistive | 0.25 R |
| P Ph-Earth | Forward or Reverse | ZP Gnd. Reach * (1 + $k_{ZN}$) | Z | RP Gnd Resistive | 0.25 R |
| P Ph-Earth | Offset | ZQ Gnd. Reach * (1 + $k_{ZN}$) | ZP' Gnd Rev Rch * (1 + $k_{ZN}$) | RP Gnd Resistive | RP' Gnd Res. Rev |
| Q Ph-Earth | Forward or Reverse | ZQ Gnd. Reach * (1 + $k_{ZN}$) | Z | RQ Gnd Resistive | 0.25 R |
| Q Ph-Earth | Offset | ZQ Gnd. Reach * (1 + $k_{ZN}$) | ZQ' Gnd Rev Rch * (1 + $k_{ZN}$) | RQ Gnd Resistive | RQ' Gnd Res. Rev |

where $k_{ZN} = (Z_0 - Z_1) / 3Z_1$ and is defined by two settings: ***kZN Res Comp*** and ***KZN Res Angle***.

*Note:*
*Not all products feature all zones.*

*Note:*
*With default settings applied, Directional Zones 1, 2, and 4 should appear Quadrilateral.*

**Caution:**
**Zone 1,2 and 4 are required to implement the *PUR*/*POR* and Blocking Aided Schemes. In this case, zone 1 and zone 2 should be forward and zone 4 should be reverse. Therefore, if the relay's *Setting Mode* is set to *Advanced* and any Zone direction has been selected that compromises the Aided Schemes, then the Aided Distance Schemes should be forced to be disabled by the user.**

### 6.3.2.2 EARTH FAULT QUADRILATERAL CHARACTERISTICS

Quadrilateral characteristics are available for earth-fault protection. A mix of Directional Forward, Directional Reverse, and Offset characteristics are available. Zone 1 and Zone 4 are settable as Forward or Reverse. Zones 2, 3, P and Q are settable as Forward or Reverse or Offset. Each zone is independent and is defined by an Impedance Reach line, a Reverse Impedance Reach Line, and two resistive blinders. The two resistive blinders (Resistive Reach Line and Reverse Resistive Reach Line) are parallel to the zone characteristic impedance angle.

The two reactance lines of each Phase-Earth Quadrilateral exhibit a characteristic tilt. The tilts of the Impedance Reach Line and the Reverse Impedance Reach Line are independent. The tilt of both may be fixed. Alternatively, the lines may be allowed to vary the tilt angle according to system conditions (dynamic tilting). If the tilt of the Reverse Impedance Reach Line is fixed, the value is -3º. If the tilt of the Impedance Reach Line is fixed, the value is fixed according to the setting, σ, -(user settable between +/- 30º). To use the dynamic tilting option you must enable it. Enabling the dynamic tilt causes the slope of the reactance lines to deviate from the set values to compensate, automatically, for angular difference between fault current and polarizing current.

#### 6.3.2.2.1 EARTH FAULT REACTANCE LINES

Both forward and reverse reach reactance lines feature a fixed tilt. For the Impedance Reach line, the fixed tilt can be set to reinforce underreaching or overreaching preferences for the zone. For the Reverse Impedance Reach line, the fixed tilt is preset at -3º.

The tilting of the reactance lines can be set such that tilting will be affected by the choice of polarizing quantity. If dynamic tilting is selected, the protection automatically chooses the best polarizing quantity from either the phase current or negative sequence current. The choice depends on which line is being polarized and on the relationship of measured currents I2 and Iph. When I2 is used as the polarizing quantity, the tilt can dynamically vary according to the angle of I2. If Iph is used, the tilt remains fixed at the set angle.

Consider polarization of the reactance lines for the case of a phase-earth fault:

For a phase-earth fault:

$$V = Vph$$

and assuming that mutual compensation is not applied:

$$I = Iph + k_{ZN}.IN.$$

To avoid overreaching or underreaching due to the voltage drop in the arc resistance, the top line of the characteristic should be ideally tilted by an angle:

$$\angle (I_{fault} / I)$$

So that the total angle of tilt should be:

$$\angle (I_{fault} / I) + \sigma$$

where $I_{fault}$ is the fault current and σ is the fixed tilt of the reactance line (user setting for the Impedance Reach line, fixed -3º preset for the Reverse Impedance Reach line.

If Z is the zone reach setting then the reactance line is formed by phase comparison between an operating signal V – I Z (S1), and a polarizing quantity, $I_{POL}$ (S2).

$I_{fault}$ should be used to determine S2, but, because the Distance protection cannot measure the fault current directly (due to the unknown infeed from the remote end), $I_{fault}$ cannot be used as the polarizing current. Instead, the angle of $I_{fault}$ must be estimated. Two proven methods to estimate the angle of $I_{fault}$ are:

1. The angle of $I_{fault}$ can be assumed to be close to the angle of Iph
2. The angle of $I_{fault}$ can be assumed to be close to the angle of the negative sequence current I2.

In case 1, the angle of Iph can be used to polarize the Quadrilateral characteristic and so the tilt of the reactance line is fixed.

In case 2 the angle of I2 can be used to polarize the Quadrilateral characteristic. In this case, the reactance line tilt varies dynamically according to the angle of I2.

The reactance line follows the fault resistance impedance and tilts up or down, starting from the set initial tilt angle (σ) to avoid underreaching or overreaching.

For both fixed and dynamic tilting the validity of current polarization is controlled by the following condition:

$$|\angle I2 - \angle Iph| < 45º$$

If this condition is not fulfilled, the assumptions that the angle of $I_{fault}$ is close to the angle of Iph or close to the angle of I2 cannot be considered valid. Under such conditions the Quadrilateral characteristic could significantly overreach or underreach. To avoid this, the distance protection automatically switches from Quadrilateral to Mho characteristics to provide stable operation.

#### 6.3.2.2.2 EARTH FAULT FIXED REACTANCE LINE TILTING

Each zone has an independent setting to set the tilt angle (σ) of the Impedance Reach line of the quadrilateral characteristic. If dynamic tilting is disabled, the characteristic uses this setting to apply a fixed tilt to the top line. The tilting angle is with reference to the fault current I, and is defined by:

$$\text{Tilt angle} = \text{setting } (\sigma) = \angle Iph/I$$

The setting range is +/- 30°. A negative angle sets a downward tilt and a positive angle sets an upward tilt.

Operation occurs when the operating current I lags the polarizing current Iph.

The Impedance Reach line of the characteristic in the Z1 plane is shown in the following diagram:

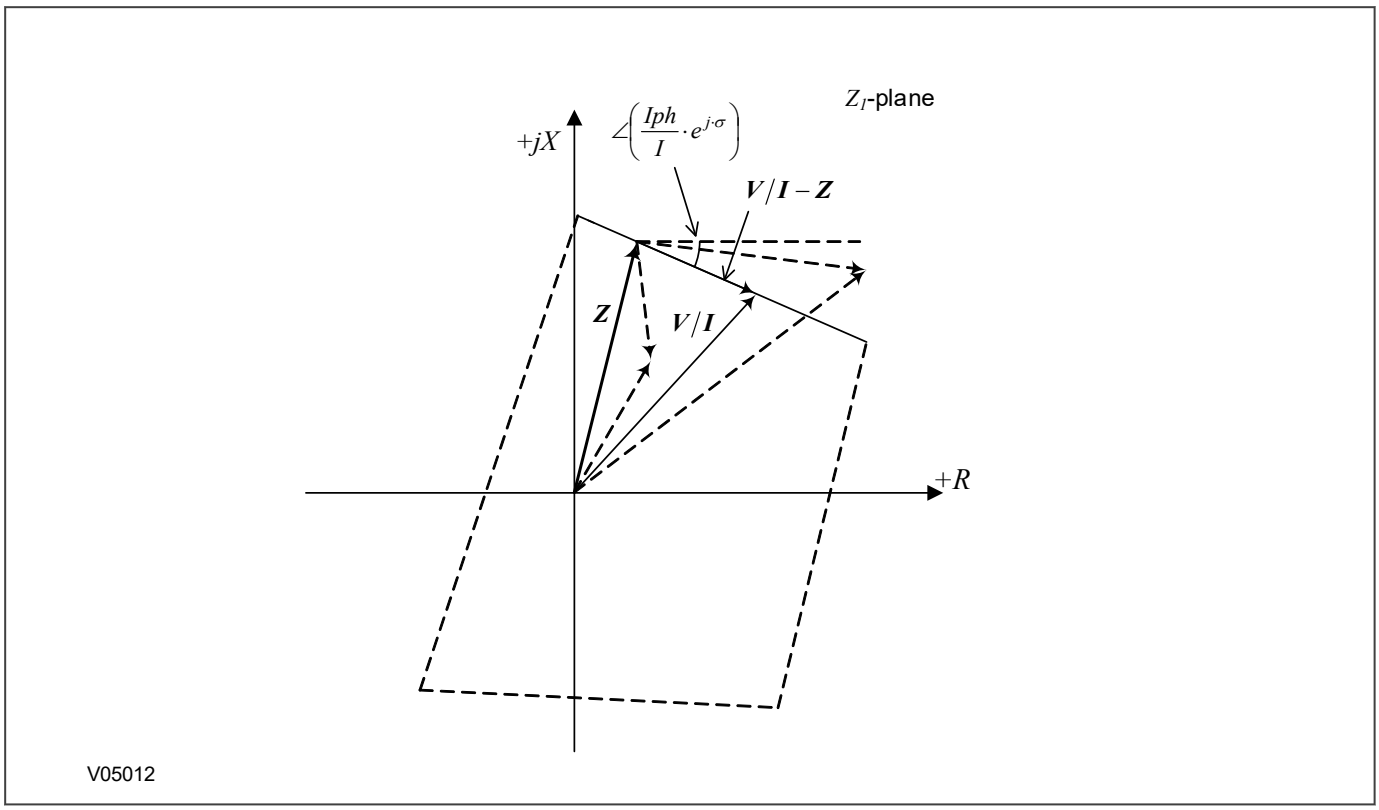



**Figure 53: Impedance Reach line in Z1 plane**

For all V/I vectors below the Impedance Reach line, the following condition is true:

$$\angle (V/I\text{-}Z) \leq \sigma$$

or

$$\angle (V - I.Z) \leq I + \sigma$$

If mutual compensation is not applied, for an earth-fault loop

$$V = Vph$$

and

$$I = Iph + k_{ZN}.IN$$

so the signals fed into comparator are:

$$S1 = Vph - Iph.Z_{replica}$$

$$S2 = Iph \angle \sigma$$

where: $Z_{replica}$ is the replica forward reach

The impedance below the Impedance Reach line is detected when the angle between the signals is less than 0°:

For products that have mutual compensation, if the mutual compensation is applied, then

$$Z_{replica} = Z(1+k_{ZN}.IN/Iph+k_{ZM}.I_M/Iph).$$

The following figure shows the $Z_{LP}$-plane representation of the characteristic:

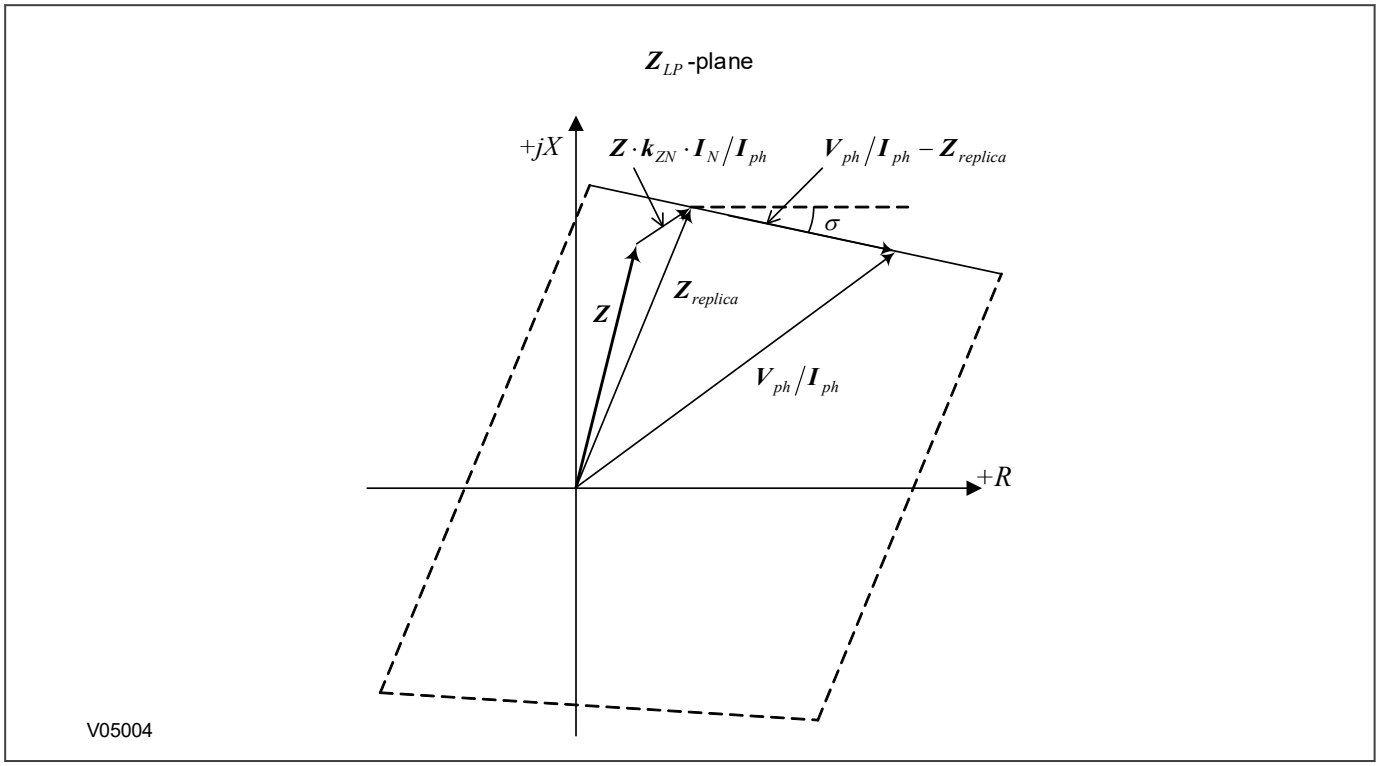



**Figure 54: Impedance Reach line in $Z_{LP}$ plane**

The Impedance Reach line tilting angle in the $Z_{LP}$ plane is fixed at σ (***Zx Tilt Top Line*** setting).

The Impedance Reach line tilting angle in the Z1 plane is defined as follows:

$$\text{Tilt angle} = \angle(\text{Iph/I}) + \sigma = \angle(\text{Iph}/(\text{Iph} + kZ_N.\text{IN})) + \sigma$$

If the healthy phase currents are much less than the current of the faulty phase, then IN ≈ Iph. The tilting angle in this case is fixed at the following value:

$$\text{Tilt angle} = \angle((1/(1 + kZN)) + \sigma$$

For products that have mutual compensation, if the mutual compensation is enabled, the tilting angle is:

$$\text{Tilt angle} = \angle(\text{Iph}/(\text{Iph} + k_{ZN}.\text{IN} + k_{ZM}.I_M)) + \sigma$$

The replica reach $Z_{replica}$ depends on the ratio of IN/Iph. If IN ≈ Iph (and if mutual compensation is not applied) then:

$$Z_{replica} = Z\ (1 + k_{ZN})$$

So the characteristic is static.

The general characteristic in the $Z_{LP}$ plane is shown in the following figure:

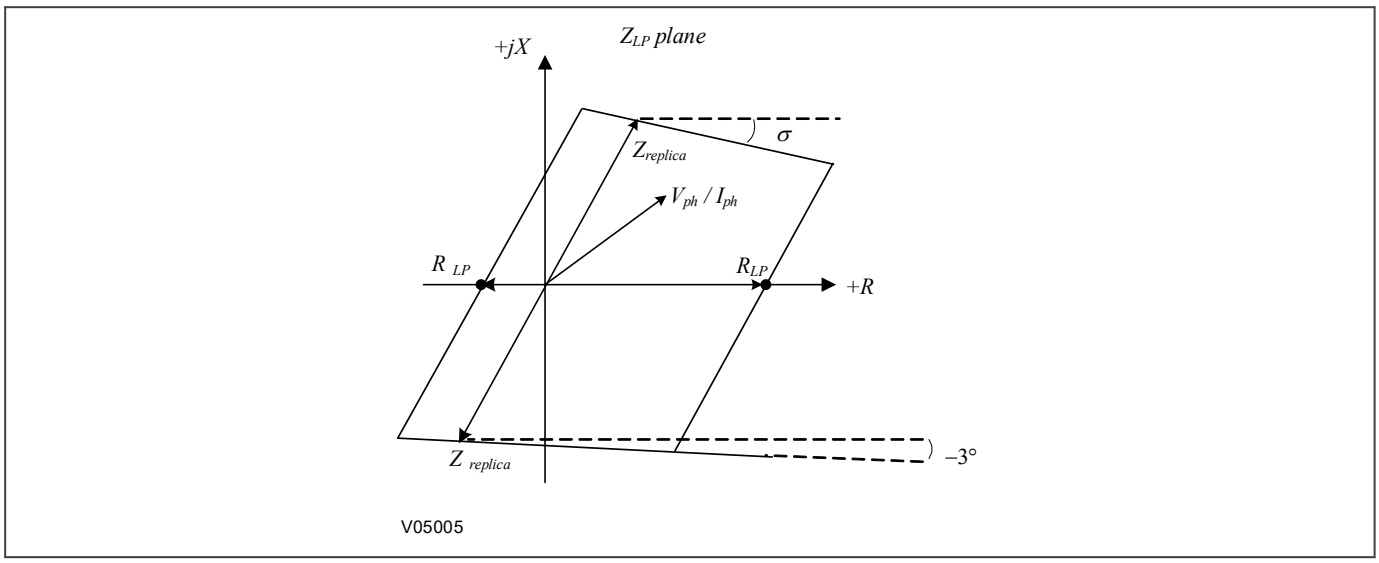



**Figure 55: General characteristic in $Z_{LP}$ plane**

The comparators used for the reactance lines are as per the following table:

| Zone | Line | S1 | S2 | Condition |
|---|---|---|---|---|
| Forward or Offset | Impedance Reach | Vph - Iph.Zreplica | Iph∠σ | ∠S1 -∠S2 < 0º |
| Forward or Offset | Reverse Impedance Reach | Vph - Iph.Z'replica | Iph∠-3º | ∠S1 -∠S2 > 0º |
| Reverse | Impedance Reach | Vph + Iph.Zreplica | -Iph∠σ | ∠S1 -∠S2 < 0º |
| Reverse | Reverse Impedance Reach | Vph + Iph.Z'replica | -Iph ∠-3º | ∠S1 -∠S2 > 0º |

#### 6.3.2.2.3 EARTH FAULT DYNAMIC REACTANCE LINE TILTING

If you enable dynamic tilting, the reactance lines of the earth-fault Distance Quadrilateral characteristic can dynamically tilt on the positive sequence impedance (Z1) plane. If the line is polarized with negative sequence current (I2), the total tilt is made up of the difference between the angle of I2 and the angle of the Distance protection current (I), plus the user-settable fixed tilt angle σ:

$$\text{Dynamic Tilt Angle} = \angle(I2 / I) + \sigma$$

The default value of the fixed tilt is -3°. It is introduced to reduce the possibility of overreach caused by any small differences between the negative sequence source impedances, and general CT/VT angle tolerances.

The tilting of Earth-Fault Quadrilateral characteristic reactance lines are constrained to prevent inappropriate excessive tilting according to the following criteria:

- The Zone 1 Impedance Reach line dynamic tilt can only be applied to bring the Resistive Reach end of the line towards the +R-axis. This ensures that Zone 1 does not overreach and maintains grading/selectivity with downstream protection.
- For the other zones (including Zone 1X and Zone 4) the dynamic tilt of the Impedance Reach line can only act in the sense to prevent underreaching. (This is particularly important for zones used to key channel-aided distance schemes).

- For Forward operating zones (except Zone 1) the Impedance Reach line dynamic tilt is applied to tilt the Resistive Reach end of the line away from the +R axis.
- For Reverse operating zones the dynamically tilting line is in the opposite quadrant of the characteristic compared with Forward/Offset Zones and the dynamic tilt moves the line away from the resistive axis.
- For Offset zones, the Impedance Reach lines tilt away from the R-axis, whilst the Reverse Impedance Reach Lines tilt towards the +R axis. This avoids overreaching in the reverse direction.
- For products that feature single-phase tripping, when one circuit breaker pole is open during a single-pole autoreclose sequence, dynamic tilting is automatically disabled. The fault current is used as the polarizing signal and a fixed -7° tilt is applied. The additional tilt reduces the possibility of overreach caused by using the faulted phase as the reference.

*Note:*
*The tilting of the zones remains unaltered if the default direction is changed.*
*Zone 1 always behaves as an underreaching zone regardless of the zone direction.*
*All other directional zones behave as overreaching zones regardless of zone direction.*

*Note:*
*Zone 1X used in Zone 1 Extension Schemes uses the Zone 2 tilt settings to ensure that it does not underreach.*

Dynamic tilting of reactance lines only occurs when the line is polarized with I2. If Iph is used as the polarizing quantity the tilt of the Impedance Reach line is fixed. If fixed tilting is selected, Iph is always used. If dynamic tilting is enabled, then the protection will decide whether to use I2 or Iph (and hence whether dynamic tilting will apply) according to the angular relationship between I2 and Iph.

The following criteria are applied:

- If the angle between I2 and Iph is more than 45°, the Quadrilateral characteristics are disabled and Mho characteristics are used instead.
- If the angle between I2 and Iph is less than 45°, Leading and lagging polarizing currents are allocated according to the phase relations between I2 and Iph as presented in the diagram below:

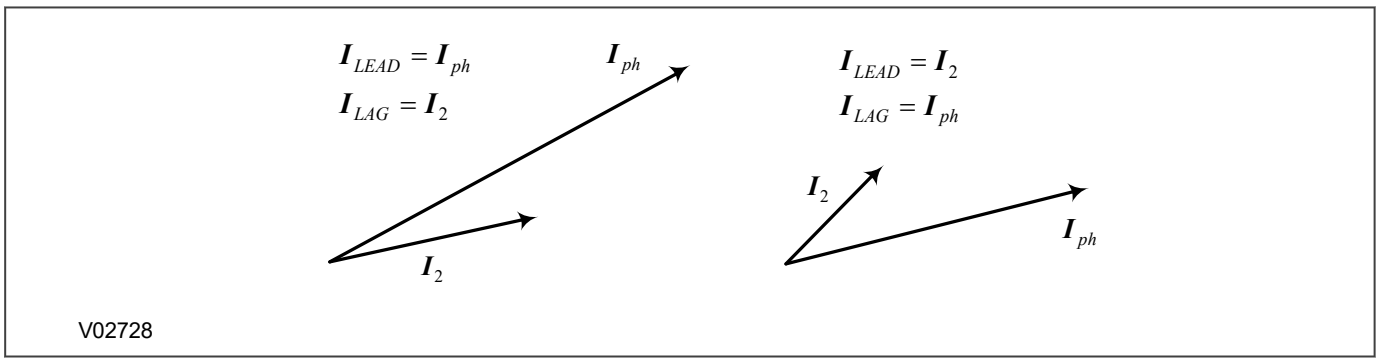



**Figure 56: Phase relations between I2 and Iph for leading and lagging polarizing currents**

The comparators used for the reactance lines are allocated as per the following table:

| Zone | Line | S1 | S2 | Condition |
|---|---|---|---|---|
| Zone 1 | Impedance Reach | Vph - $IphZ_{replica}$ | $I_{LAG}\angle\sigma$ | $\angle S1 - \angle S2 < 0^o$ |
| Zone 1 | Reverse Impedance Reach | Vph - $IphZ'_{replica}$ | $I_{LAG}\angle -3^o$ | $\angle S1 - \angle S2 > 0^o$ |
| Forward or Offset zones (except Zone 1) | Impedance Reach | Vph - $IphZ_{replica}$ | $I_{LEAD}\angle\sigma$ | $\angle S1 - \angle S2 < 0^o$ |
| Forward or Offset zones (except Zone 1) | Reverse Impedance Reach | Vph - $IphZ'_{replica}$ | $I_{LAG}\angle -3^o$ | $\angle S1 - \angle S2 > 0^o$ |

| Zone | Line | S1 | S2 | Condition |
|---|---|---|---|---|
| Reverse | Impedance Reach | Vph + IphZ$_{replica}$ | -I$_{LEAD}$∠σ | ∠S1 -∠S2 < 0º |
| Reverse | Reverse Impedance Reach | Vph + Iph Z'$_{replica}$ | -I$_{LAG}$∠-3º | ∠S1 -∠S2 > 0º |

If $I_{LEAD}$ is I2 the lines are dynamically tilted up from the fixed angle.

If $I_{LEAD}$ is Iph, the fixed tilt applies.

If $I_{LAG}$ is I2, the lines are dynamically tilted down from the fixed angle.

If $I_{LAG}$ is Iph, the fixed tilt applies.

#### 6.3.2.2.4 EARTH FAULT RESISTIVE BLINDERS

The Resistive Reach settings are used to select the resistive limits of the Quadrilaterals.

The Earth Fault reach settings are set according to the positive sequence line impedance, so are generally identical to the settings of the Phase Fault elements.

Since the Earth Fault reach settings are set according to the positive sequence line impedances, the relationship between the positive sequence impedances and the earth-fault loop impedances needs to be understood.

Consider the general characteristic in the Z1 plane shown in the following figure:

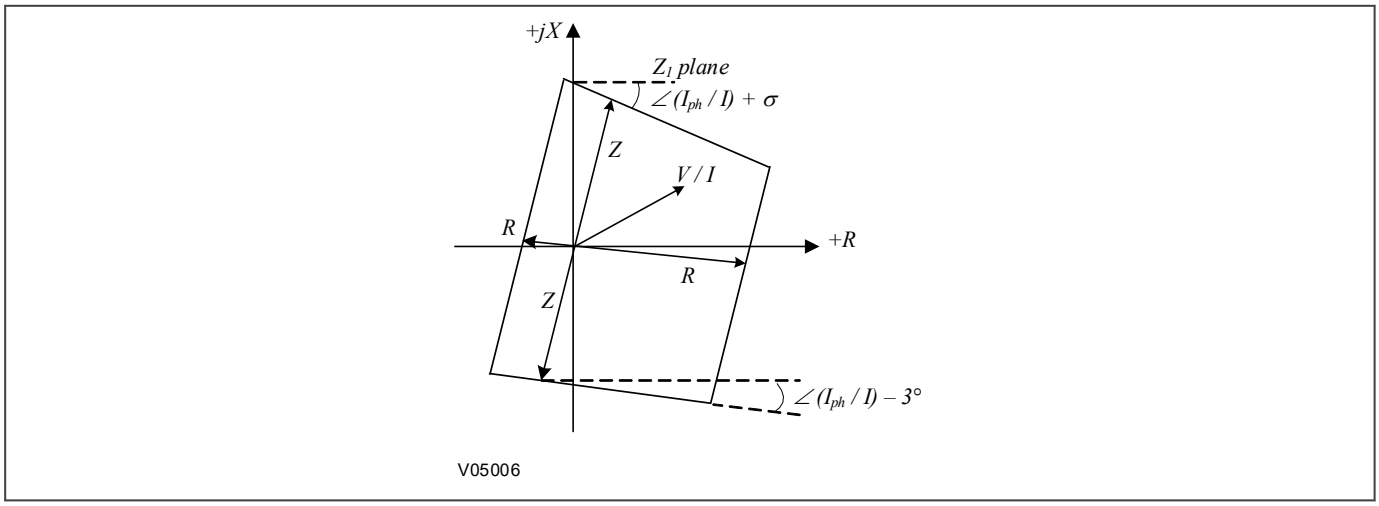



**Figure 57: General characteristic in Z1 plane**

$$R = R_{LP}\ (Iph/I) \text{ and } R' = R'_{LP}.(Iph/I)$$

$$I = Iph + k_{ZN}.IN$$

For products that have mutual compensation, if the mutual compensation is enabled, then

$$I = Iph + k_{ZN}.IN + k_{ZM}.IM$$

If the healthy phase currents are much less than the current of the faulty phase and the mutual compensation is disabled, then IN ≈ Iph (the faulty phase current) and the characteristic in the Z1 plane is simplified:

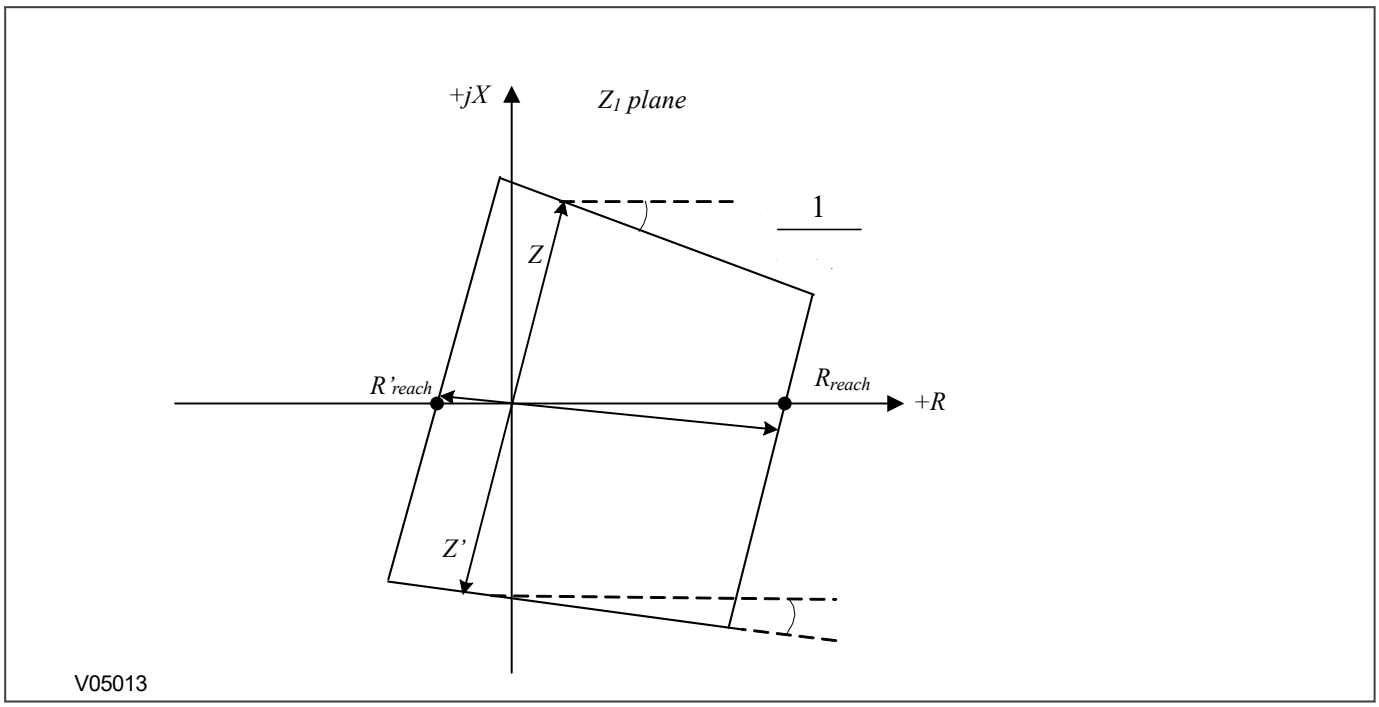



**Figure 58: Simplified characteristic in Z1 plane**

$$R_{reach} = ((RLP./(1 + k_{ZN})).\sin(Z + \alpha)),$$

$$R'reach = ((R'LP./(1 + k_{ZN})).\sin(Z + \alpha)),$$

where: $\alpha$ is the angle of $1/(1 + k_{ZN})$:

$$\alpha = (1/(1 + k_{ZN}))$$

In typical cases the sine ratio coefficient term is close to unity so the simplified equations can be used:

$$R_{reach} = R_{LP} / | (1 + k_{ZN}) |,$$

$$R'_{reach} = R'_{LP} / | (1 + k_{ZN}) |,$$

So in terms of replica impedances and loop resistances, the comparators used for the resistance lines are as per the following table:

| Zone | Line | S1 | S2 | Condition |
|---|---|---|---|---|
| Forward or Offset | Resistive reach | Vph - Iph.$R_{LP}$ | Iph.$Z_{replica}$ | ∠S1 -∠S2 > 0º |
| Forward or Offset | Reverse resistive reach | Vph - Iph.$R'_{LP}$ | Iph.$Z_{replica}$ | ∠S1 -∠S2 < 0º |
| Reverse | Resistive reach | Vph + Iph.$R_{LP}$ | -Iph.$Z_{replica}$ | ∠S1 -∠S2 > 0º |
| Reverse | Reverse resistive reach | Vph + Iph.$R'_{LP}$ | -Iph.$Z_{replica}$ | ∠S1 -∠S2 < 0º |

The Resistive Impedance Reach side of the earth zone is controlled by the Resistive Reach setting applied (***Rx Gnd Resistive***). This defines the fault arc resistance that can be detected for a single phase-earth fault. For such a fault, the fault resistance appears in the total fault loop (out and return loop), in which the line impedance is $Z_1$ x (1 + $k_{ZN}$), if IN ≅ Iph.

Most injection test sets plot impedance characteristics in positive sequence terms, so that the right-hand intercept appears less than the setting applied (***Rn Gnd Resistive*** /(1+ $k_{ZN}$)). The left hand side is set by the ***Rn Gnd Res Rev*** setting and acts similarly.

*Note:*
*The resistive reach lines of earth-fault Quadrilateral characteristics are not affected by the type of tilting used by the reactive lines (fixed or dynamic), nor by the angle values.*

#### 6.3.2.2.5 EARTH FAULT QUADRILATERAL CHARACTERISTICS SUMMARY

The inputs to the comparators used for the earth-fault Quadrilaterals are summarised in the following table:

| Zone | Line | S1 | S2 | Condition |
|---|---|---|---|---|
| Zone 1 | Impedance Reach | $Vph - Iph.Z_{replica}$ | $I_{LAG} \angle \sigma$ | $\angle S1 - \angle S2 < 0°$ |
| Zone 1 | Reverse Impedance Reach | $Vph - Iph.Z'_{replica}$ | $I_{LAG} \angle -3°$ | $\angle S1 - \angle S2 > 0°$ |
| Forward or Offset zones (except Zone 1) | Impedance Reach | $Vph - Iph.Z_{replica}$ | $I_{LEAD} \angle \sigma$ | $\angle S1 - \angle S2 < 0°$ |
| Forward or Offset zones (except Zone 1) | Reverse Impedance Reach | $Vph - Iph.Z'_{replica}$ | $I_{LAG} \angle -3°$ | $\angle S1 - \angle S2 > 0°$ |
| Reverse | Impedance Reach | $Vph + Iph.Z_{replica}$ | $-I_{LEAD} \angle \sigma$ | $\angle S1 - \angle S2 < 0°$ |
| Reverse | Reverse Impedance Reach | $Vph + Iph.Z'_{replica}$ | $-I_{LAG} \angle -3°$ | $\angle S1 - \angle S2 > 0°$ |
| Forward or Offset | Resistive Reach | $Vph - Iph.R_{LP}$ | $Iph.Z_{replica}$ | $\angle S1 - \angle S2 > 0°$ |
| Forward or Offset | Reverse Resistive Reach | $Vph - Iph.R'_{LP}$ | $Iph.Z_{replica}$ | $\angle S1 - \angle S2 < 0°$ |
| Reverse | Resistive Reach | $Vph + Iph.R_{LP}$ | $-Iph.Z_{replica}$ | $\angle S1 - \angle S2 > 0°$ |
| Reverse | Reverse Resistive Reach | $Vph + Iph.R'_{LP}$ | $-Iph.Z_{replica}$ | $\angle S1 - \angle S2 < 0°$ |

If dynamic tilting is selected, then:

If $I_{LEAD}$ is I2 the lines are dynamically tilted up from the fixed angle (Forward sense)

- If $I_{LEAD}$ is Iph, the fixed tilt applies.
- If $I_{LAG}$ is I2, the lines are dynamically tilted down from the fixed angle (Forward sense)
- If $I_{LAG}$ is Iph, the fixed tilt applies.

If fixed tilting is selected, then he current input quantity for S2 is Iph in all cases.

The positive sequence reach settings used for the Earth-Fault Quadrilateral characteristics are summarised in the table below:

| Zone | Type | Impedance Reach Z | Reverse Impedance Reach Z' | Resistive Reach R | Reverse Resistive Reach R' |
|---|---|---|---|---|---|
| 1 Ph-Earth | Forward or Reverse | Z1 Gnd. Reach * (1 + kZN) | Z1 | R1 Gnd Resistive | 0.25 R |
| 2 Ph-Earth | Forward or Reverse | Z2 Gnd. Reach * (1 + kZN) | Z2 | R2 Gnd Resistive | 0.25 R |
| 2 Ph-Earth | Offset | Z2 Gnd. Reach * (1 + kZN) | Z2 Gnd Rev Rch * (1 + kZN) | R2 Gnd Resistive | R2' Ph Res. Rev |
| 3 Ph-Earth | Forward | Z3 Gnd. Reach * (1 + kZN) | Z3 | R3 Gnd Resistive | 0.25 R |
| 3 Ph-Earth | Reverse | Z3 Gnd. Reach * (1 + kZN) | Z3 | R3 Gnd Resistive | 0.25 R |
| 3 Ph-Earth | Offset | Z3 Gnd. Reach * (1 + kZN) | Z3' Gnd Rev Rch * (1 + kZN) | R3 Gnd Resistive | R3' Ph Res. Rev |
| 4 Ph-Earth | Reverse or Forward | Z4 Gnd. Reach * (1 + kZN) | Z4 | R4 Gnd Resistive | 0.25 R |
| P Ph-Earth | Forward or Reverse | ZP Gnd. Reach * (1 + kZN) | ZP | RP Gnd Resistive | 0.25 R |
| P Ph-Earth | Offset | ZQ Gnd. Reach * (1 + kZN) | ZP' Gnd Rev Rch * (1 + kZN) | RP Gnd Resistive | RP' Gnd Res. Rev |
| Q Ph-Earth | Forward or Reverse | ZQ Gnd. Reach * (1 + kZN) | ZQ | RQ Gnd Resistive | 0.25 R |
| Q Ph-Earth | Offset | ZQ Gnd. Reach * (1 + kZN) | ZQ' Gnd Rev Rch * (1 + kZN) | RQ Gnd Resistive | RQ' Gnd Res. Rev |

where $k_{ZN} = (Z_0 - Z_1) / 3Z_1$ and is defined by two settings: ***kZN Res Comp*** and ***KZN Res Angle***.

## 6.3.3 QUADRILATERAL CHARACTERISTIC FOR PHASE FAULTS

Quadrilateral characteristics are available for phase fault protection. A mix of Directional Forward, Directional Reverse, and Offset characteristics are available. Zone 1 and Zone 4 are settable as Forward or Reverse. Zones 2, 3, P and Q are settable as Forward or Reverse or Offset. Each zone is independent and is defined by an Impedance Reach Line, a Reverse Impedance Reach Line, and two resistive blinders. The two resistive blinders (Resistive Reach Line and Reverse Resistive Reach Line) are parallel to the zone characteristic impedance angle. The two reactance lines of each Quadrilateral exhibit a characteristic tilt. In the phase fault characteristics the tilt of the Reverse Impedance Reach Line is preset, whilst you can choose the tilt angle for the Impedance Reach Line.

### 6.3.3.1 PHASE FAULT IMPEDANCE REACH LINE

The tilt of the top line can be set independently for each zone. It is defined by a reach setting, Z, and a tilt angle, σ, as shown in the following diagram:

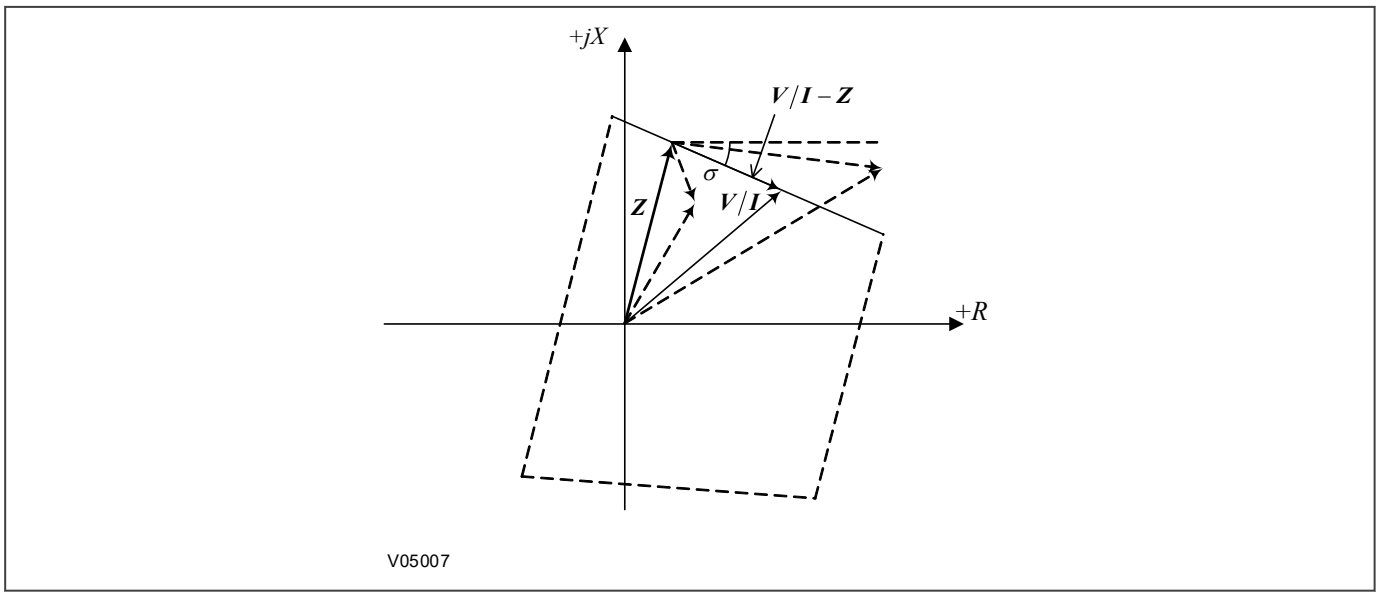



**Figure 59: Impedance Reach line construction**

Referenced to the fault current I, the angle of tilt is equal to the setting σ. A negative angle sets a downward tilt and a positive angle sets an upward tilt. Operation can occur when the operating signal lags the polarizing signal. A negative angle sets a downward tilt and a positive angle sets an upward tilt.

For all V/I vectors below the Impedance Reach line, the following condition is true:

$$\angle (V/I - Z) \leq \sigma$$

or

$$\angle (V - I.Z) \leq \angle I.\angle \sigma$$

The resultant two signals provided to the comparator are:

$$S_1 = V - I.Z$$

$$S_2 = I.\angle \sigma$$

Impedance on the tripping side of the Impedance Reach line is detected when the angle between S1 and S2 is less than 0°.

### 6.3.3.2 PHASE FAULT REVERSE IMPEDANCE REACH LINE

The Reverse Impedance Reach line of the phase quadrilateral elements has a tilt that is fixed at -3° as shown in the following diagram:

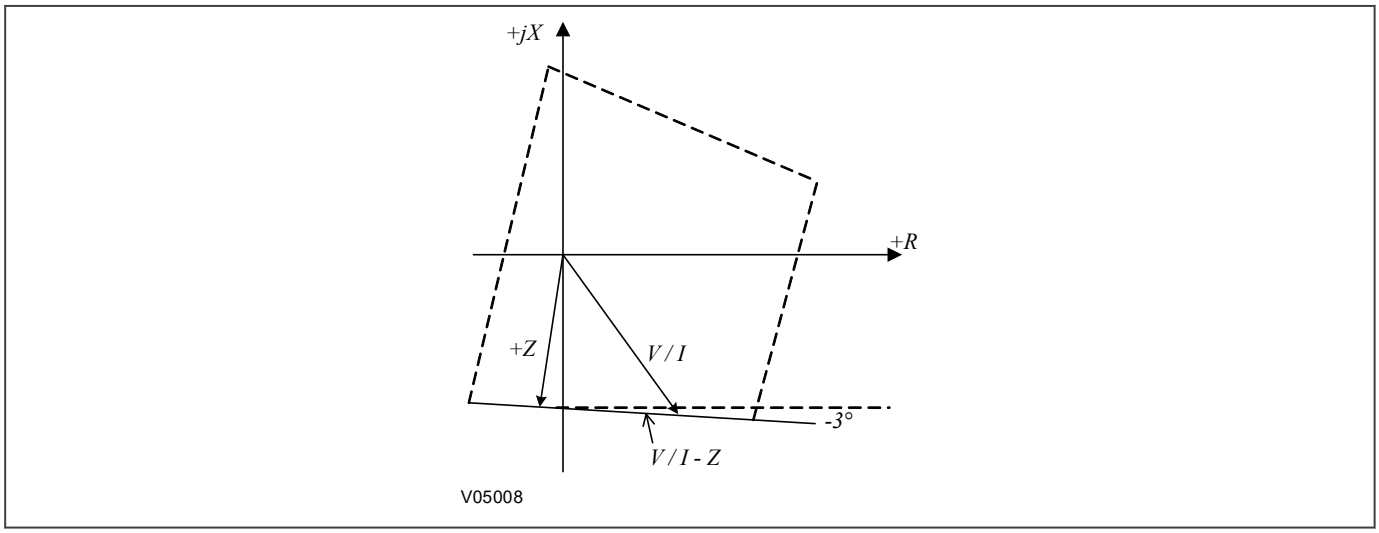



**Figure 60: Reverse impedance reach line construction**

For an Offset zone, Z' is the settable reverse reach. For a directional zone Z' is a fixed percentage (either 25% or 100%) of the forward reach (Z) in the opposite direction.

The signals provided to the comparator are:

$$S_1 = V - I.Z'$$

$$S_2 = I.\angle -3°$$

Impedance on the tripping side of the Reverse Impedance Reach line is detected when the angle between S1 and S2 is greater than 0°.

### 6.3.3.3 PHASE FAULT RESISTIVE REACH LINE

Refer to the following figure:

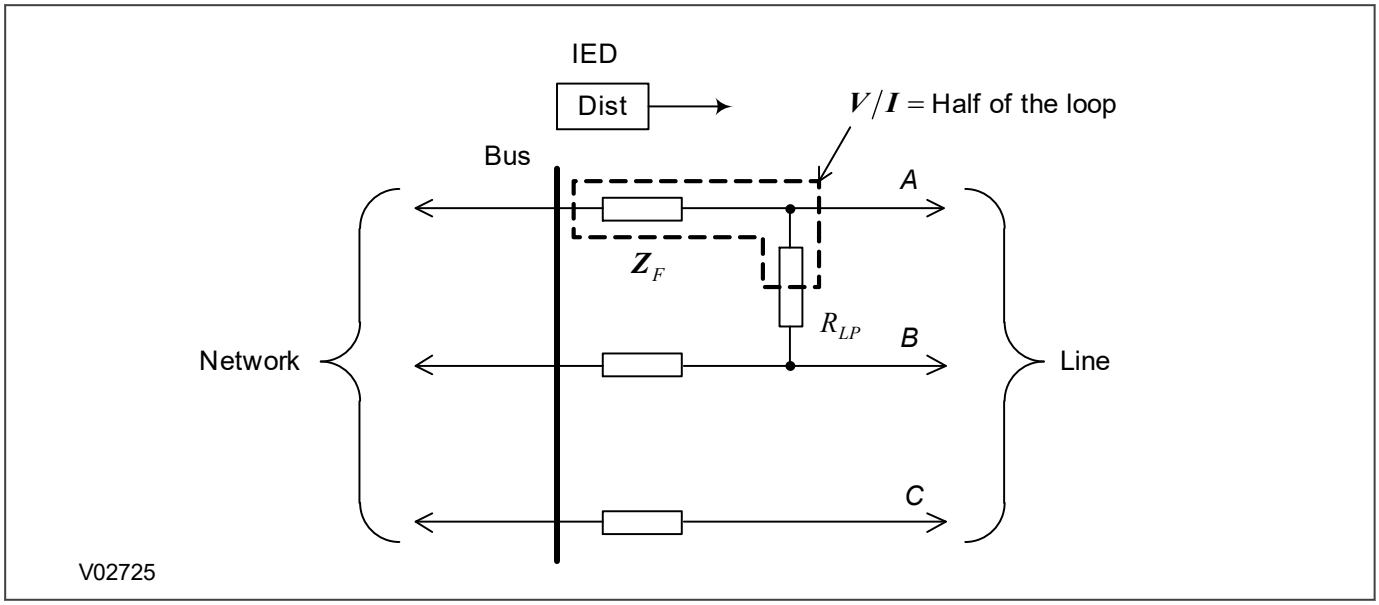



**Figure 61: Resistive reach of phase elements**

The setting ***Rx Ph. Resistive*** defines the complete loop resistive reach $R_{LP}$ of the Distance Protection.

Since a phase-to-phase distance element measures half of the loop, the right-hand resistive reach R, of the characteristic is equal to half of the setting value.

$$R = \tfrac{1}{2}\ \textit{Rx Ph. Resistive}$$

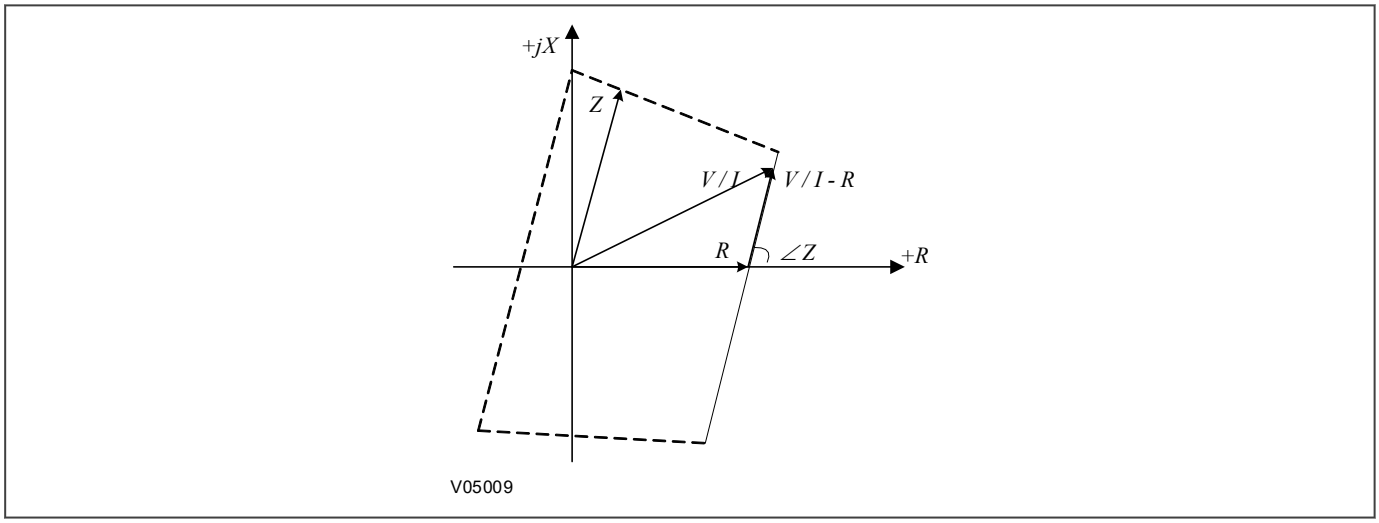



**Figure 62: Resistive Reach line construction**

For all V/I vectors which are on the left side of the right blinder the following condition is true:

$$\angle (V/I - R) \leq Z$$

or

$$\angle (V - I.R) \leq \angle I.\ Z$$

The two signals provided to the comparator are:

$$S_1 = V - I.R$$

$$S_2 = I.Z$$

The impedance on the left side of the right hand resistive line is detected when the angle between S1 and S2 is greater than 0°.

### 6.3.3.4 PHASE FAULT REVERSE RESISTIVE REACH LINE

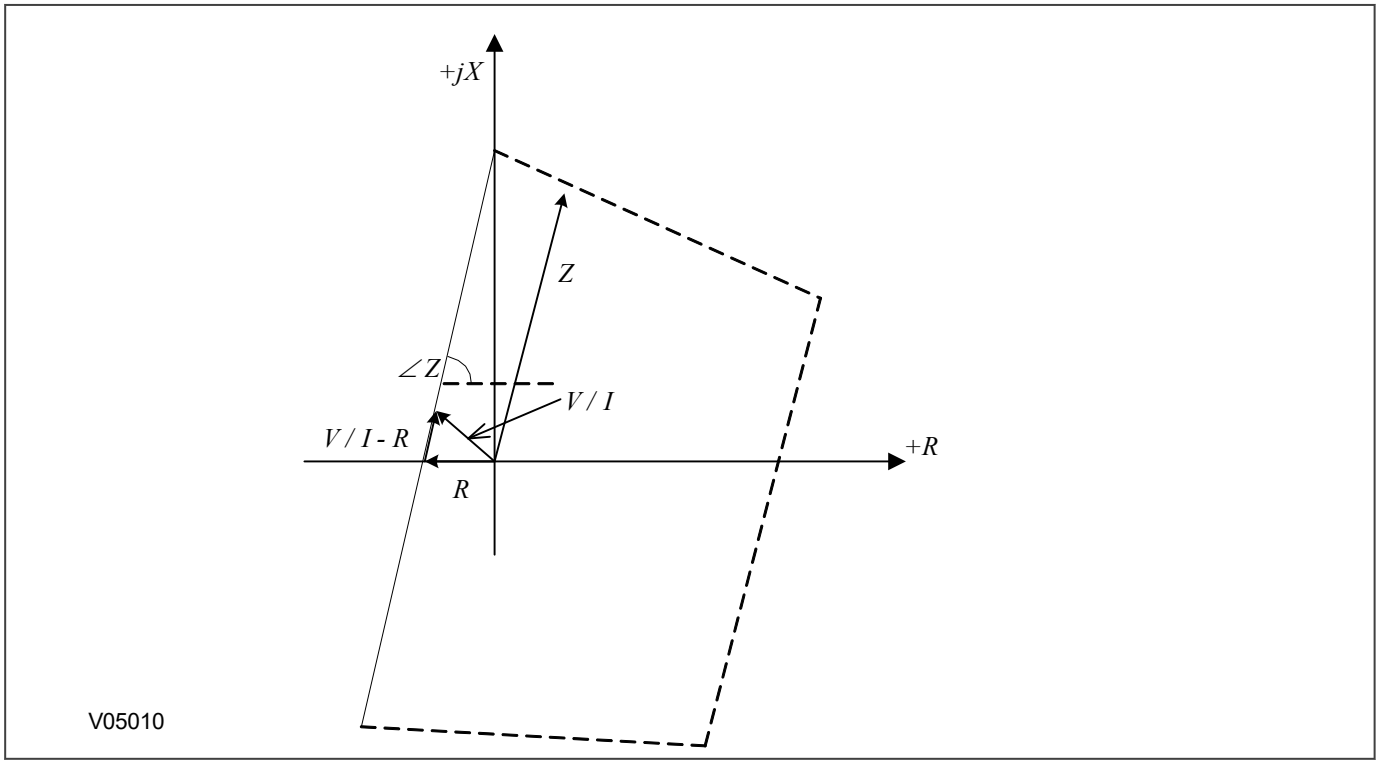



**Figure 63: Reverse resistive reach line construction**

For an offset zone, R' is the settable reverse resistive reach (=½***Rx' Ph Res. Rev.***). . For a directional zone, R' is fixed at 25% of the Resistive Reach (=½***Rx Ph Res. Rev.***), acting in the opposite direction.

The two signals provided to the comparator are:

$$S_1 = V - I.R$$

$$S_2 = I.Z$$

The impedance on the right side of the left hand resistive line is detected when the angle between S1 and S2 is less than 0°.

### 6.3.3.5 PHASE FAULT QUADRILATERAL CHARACTERISTIC SUMMARY

The phase fault Quadrilateral characteristics are summarised in the following figure and tables:

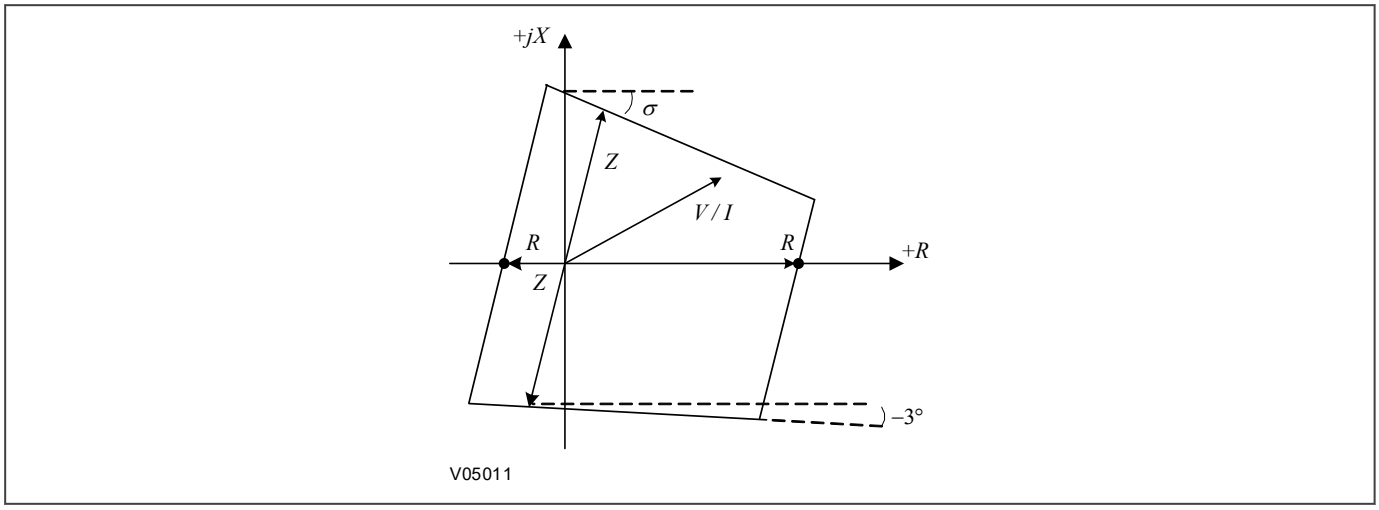



**Figure 64: Phase Fault Quadrilateral characteristic summary**

The comparators used for the Phase-Fault Quadrilateral zones are summarised in the following table:

| Zone | Line | S1 | S2 | Condition (∠S1 - ∠S2) |
|---|---|---|---|---|
| Forward/Offset | Impedance Reach Line | V – I.Z | I.∠ σ° | <0° |
| Forward/Offset | Reverse Impedance Reach Line | V – I.Z' | I.∠ 3° | >0° |
| Forward/Offset | Resistive Reach Line | V – I.R | I.Z | >0° |
| Forward/Offset | Reverse Resistive Reach Line | V – I.R' | I.Z | <0° |
| Reverse | Impedance Reach Line | V + I.Z | -I.∠ σ° | <0° |
| Reverse | Reverse Impedance Reach Line | V + I.Z' | -I.∠ 3° | >0° |
| Reverse | Resistive Reach Line | V + I.R | -I.Z | >0° |
| Reverse | Reverse Resistive Reach Line | V + I.R' | -I.Z | <0° |

The positive sequence reach settings used for the Phase-Fault Quadrilateral characteristics are summarised in the following table:

| Zone | Type | Impedance Reach Z | Reverse Impedance Reach Z' | Resistive Reach R | Reverse Resistive Reach R' |
|---|---|---|---|---|---|
| 1 Ph-Ph | Forward or Reverse | Z1 Ph. Reach | Z1 | ½*R1 Ph. Resistive | 0.25 R |
| 2 Ph-Ph | Forward or Reverse | Z2 Ph. Reach | Z2 | ½*R2 Ph. Resistive | 0.25 R |
| 2 Ph-Ph | Offset | Z2 Ph. Reach | Z2' Ph Rev Reach | ½*R2 Ph. Resistive | ½*R2' Ph Res. Rev |
| 3 Ph-Ph | Forward | Z3 Ph. Reach | Z3 | ½*R3 Ph. Resistive | 0.25 R |
| 3 Ph-Ph | Reverse | Z3 Ph. Reach | Z3 | ½*R3 Ph. Resistive | 0.25 R |
| 3 Ph-Ph | Offset | Z3 Ph. Reach | Z3' Ph Rev Reach | ½*R3 Ph. Resistive | ½*R3' Ph Res. Rev. |
| 4 Ph-Ph | Reverse or Forward | Z4 Ph. Reach | Z4 | ½*R4 Ph. Resistive | 0.25 R |
| P Ph-Ph | Forward or Reverse | ZP Ph. Reach | ZP | ½*RP Ph Resistive | 0.25 R |
| P Ph-Ph | Offset | ZQ Ph. Reach | ZP' Ph Rev Reach | ½*RP Ph Resistive | ½*RP' Ph. Res. Rev. |
| Q Ph-Ph | Forward or Reverse | ZQ Ph. Reach | ZQ | ½*RQ Ph Resistive | 0.25 R |
| Q Ph-Ph | Offset | ZQ Ph. Reach | ZQ' Ph Rev Reach | ½*RQ Ph Resistive | ½*RQ' Ph. Res. Rev. |

*Note:*
*Not all zones feature in all product variations.*

# 6.4 PHASE AND EARTH FAULT DISTANCE PROTECTION IMPLEMENTATION

The Distance protection requires line data to be input to operate correctly. You must first input the data using the settings in the *LINE PARAMETERS* column.

The Distance protection has a Setting Mode which is set to `Simple` by default. We recommend the default for most applications. Instead of entering distance zone impedance reaches in ohms, zone settings are simply entered in terms of percentage of the protected line data specified in the ***Line Impedance*** setting in the *LINE PARAMETERS*. The setting assumes that the residual compensation factor is equal for all zones. The protection calculates the required reach settings from the percentage settings. The calculated zone reaches are available for viewing but you cannot change the values.

An `Advanced` Setting Mode allows individual distance ohmic reaches and residual compensation factors to be entered for each zone. When advanced mode is selected, all 'percentage' settings associated with the `Simple` setting mode are hidden and the Distance zone settings need to be entered for each zone in the *DIST. ELEMENTS* column.

## 6.4.1 PHASE FAULT CHARACTERISTICS

Each phase zone can be `Enabled` or `Disabled` using the ***Zone Ph Status*** settings in the *DISTANCE SETUP* column.

Characteristics can be either 'Quadrilateral' (polygon), or Mho (circular). The chosen characteristic applies to all zones. All distance elements are directionalized and use residual compensation of the corresponding phase fault reach.

## 6.4.2 EARTH FAULT CHARACTERISTICS

Each ground zone can be `Enabled` or `Disabled` using the **Zone Gnd Status** settings in the *DISTANCE SETUP* column.

Characteristics can be either 'Quadrilateral' (polygon), or Mho (circular). The chosen characteristic applies to all zones. All distance elements are directionalized and use residual compensation of the corresponding phase fault reach.

## 6.4.3 DISTANCE PROTECTION TRIPPING DECISION

A fault is detected if the phase voltage drops below 70%, or if the phase selector picks up. When a fault is detected, the protection stores values recorded over the two previous cycles. These are used to provide a reference for memory polarization, etc, as the fault is processed.

For security, a number of criteria must be satisfied before the distance protection issues a trip command. These are as follows:

- The phase selector needs to identify the faulted phases and ensure that only the correct distance measuring zones can issue a trip. Possible phase selections are AN, BN, CN, AB, BC, CA, and ABC. For double phase-earth faults, the selection is AB, BC or CA, with N (neutral) for indication only.
- For the selected phase-earth elements the phase and the neutral currents must exceed the minimum sensitivity threshold. For the selected phase-to-phase elements the loop current must exceed the minimum sensitivity threshold. By default, this sensitivity is 5%In for phase-earth faults and, for phase-to-phase faults both of the faulted phases must exceed 5%In. You can raise this minimum sensitivity if necessary, but this is not normally required.
- For an earth-fault distance element to operate, the corresponding biased neutral current detector must have picked up.
- The faulted phase impedance must appear in a tripping (measuring) zone, corresponding to the phase selection.

- For directional zones, the directionality element must agree with the tripping zone. Zones 1, 2, and 4 are always directional whereas other zones are only directional if set as directional. In directional zones the directionality element must agree with the tripping zone. For example, Zone 1 is a Forward Directional zone and must not trip for Reverse faults. Therefore a Zone 1 trip is only allowed if the directionality element issues a Forward decision. Zone 4 is reverse-looking so needs a Reverse decision by the directionality element.
- The set time delay for the measuring zone must expire, with the measured fault impedance remaining inside the zone characteristic for the duration of the delay time. Typically, Zone 1 has no time delay (instantaneous), whereas all other zones have time delays.
- Where channel-aided distance schemes are used, the time delay tZ2 for overreaching Zone 2 may be bypassed for some of the schemes.

## 6.4.4 DISTANCE PROTECTION PHASE SELECTION

Phase selection allows the product to identify exactly which phases are involved in a fault and enables the correct measuring zones to trip.

Operation of the distance elements is controlled by a Superimposed Current Phase Selector. For a period of two-cycles after pick-up of the phase selector, only elements associated with the fault type selected by the phase selector are allowed to operate. If these elements do not operate, all elements are enabled for the following five cycles, before the phase selector returns to its quiescent state.

Operation of an enabled distance element during the two-cycle, or five-cycle period, causes the phase selector state to be maintained until the element resets. An exception to this is when the phase selector changes decision while an element is operated. In this case, the selected elements are reset and the two cycle period restarts with the new selection.

*Note:*
*Any existing trip decision is not reset under this condition. After the first cycle following a selection, the phase selector is only permitted to change to a selection involving additional phases.*

On double phase-to-earth faults, only the phase-to-phase elements are enabled. This is because they are generally more accurate under these conditions than earth fault elements. A biased neutral current level detector operates to indicate the involvement of earth in the fault.

### 6.4.4.1 FAULTED PHASE SELECTION

The faulted phase or phases are selected by comparing the magnitudes of the three phase-to-phase superimposed currents. A single phase-to-earth fault produces the same superimposed current on two of these signals and zero on the third. A phase-to-phase or double-phase-to-earth fault produces one signal which is larger than the other two. A three phase fault produces three superimposed currents which are the same size. The figure below shows how the change in current can be used to select the faulted phases for a C phase-to-ground (CN) fault.

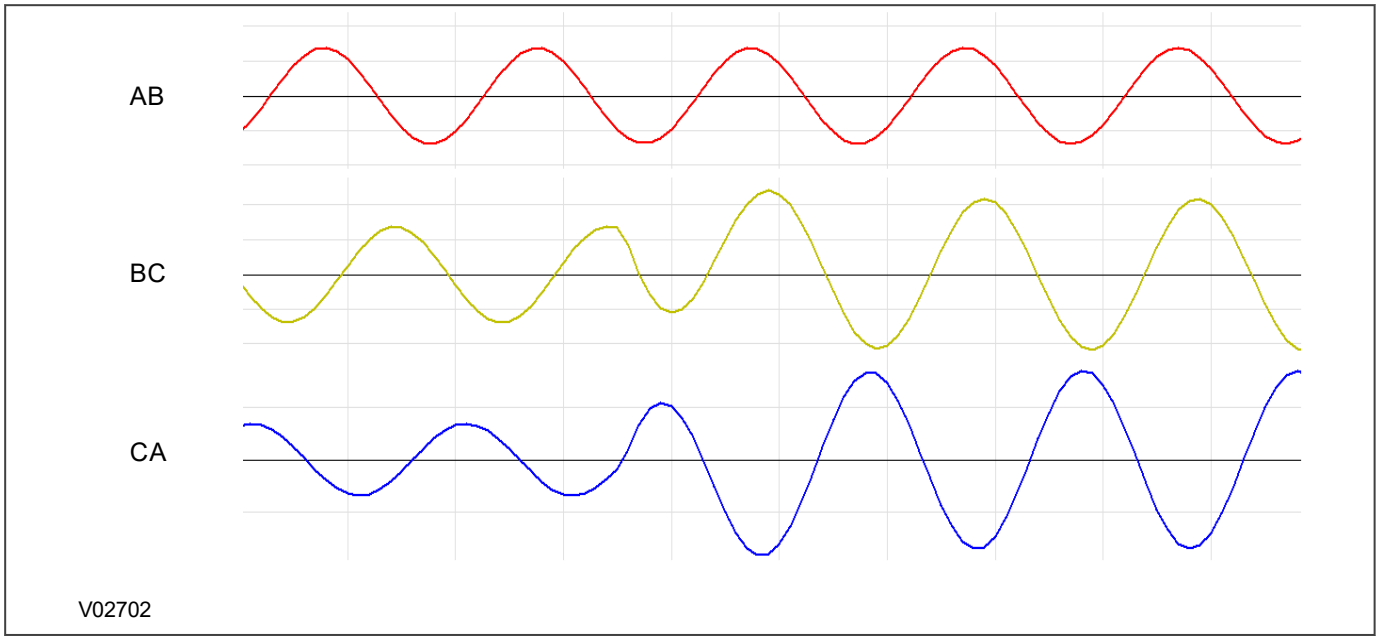



**Figure 65: Phase to phase current changes for C phase-to-ground (CN) fault**

As default, phase selection is made when any superimposed current exceeds 5% of nominal current (0.05 In).

Any superimposed current greater than 80% of the largest superimposed current is included in the phase selection logic.

For applications which might experience high levels of sub-synchronous currents, the phase selector automatically raises the threshold from the default 5% of In, in order to prevent sporadic operation whilst maintaining high sensitivity to faults.

*Note:*
*If you test the distance elements using test sets, which do not provide a dynamic model to generate true fault delta conditions, you need to set* ***Static Test Mode*** *to* `Enabled` *in the COMMISSION TESTS column. This disables phase selector control and forces the distance protection to use a conventional (non-delta) directional line.*

The phase selector picks up on fault detection, and enables Distance protection on all elements which have been selected by the pick-up. These elements are enabled for 2 cycles, and normally this will result in tripping. On double ground-to-phase faults, only appropriate phase elements are enabled. This is because they are generally more accurate than ground elements under these conditions. If, however, tripping is not initiated within the 2 cycles, for the following 5 cycles all Distance elements (including all phase-earth elements) are enabled. During these five cycles, this could lead to incorrect operation of earth-fault elements in case of an out-of-zone double-phase-earth fault. This is because one of the phase-earth elements could demonstrate significant overreach, which may result in maloperation. To help prevent this, a Biased Neutral Current Detector is incorporated.

### 6.4.4.2 BIASED NEUTRAL CURRENT DETECTOR

The Biased Neutral Current Detector permits the earth-fault elements to operate only if sufficient neutral current is detected. The Biased Neutral Current Detector characteristic is illustrated in the following figure.

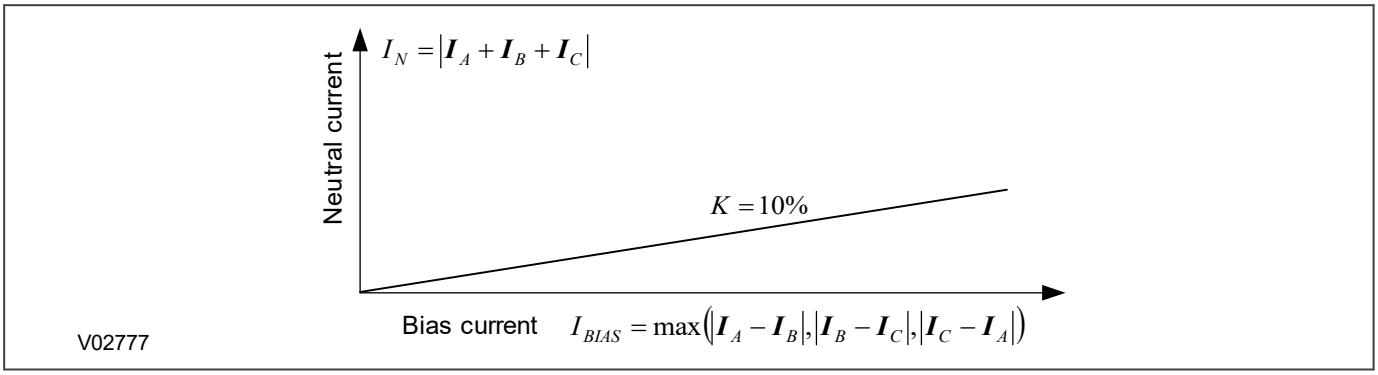



**Figure 66: Biased Neutral Current Detector Characteristic**

The neutral current detector uses the maximum of the three phase current differences as a biasing value. The slope of the characteristic is fixed at 10%.

Biasing the neutral current detector assures that the detector is sensitive enough to operate for any single-phase fault, without the risk of picking up on neutral spill current during phase-to-phase faults. The neutral spill current might arise from mismatched current transformers or current transformer saturation. The biasing also ensures that the earth fault distance elements are generally disabled for double-phase-to-earth faults with high resistance in the neutral. Such faults can occur in resistively earthed systems, or in solidly earthed systems due to high arc resistance. Given that these conditions are very similar to pure phase-to-phase faults, the earth fault distance elements can exhibit high measuring errors which the use of the neutral current detector overcomes.

## 6.4.5 DIRECTIONALIZING THE DISTANCE ELEMENTS

By default a Delta technique is used for directionalizing the Distance protection. It acts on step-changes (Deltas) of current and voltage to determine whether potential fault conditions are in the forward or reverse direction. The Delta voltage and current thresholds used in the Distance Directional decision are fixed for optimum performance. The Directional characteristic angle, (also known as the relay characteristic angle – RCA) is set to 60° by default, but you can change this to suit your application using the ***Dir. Char Angle*** setting in the *DISTANCE SETUP* column.

The Delta Directional technique needs the changes in voltage and current to exceed the preset thresholds, in order to determine forward and reverse decisions. If these thresholds are not exceeded, but a potential fault is detected, the Distance protection reverts to a conventional directional technique with memory polarization of the voltage.

If you don't want to use the Delta directional technique, set ***Dir. Status*** in the *DISTANCE SETUP* column to `Disabled` in which case memory polarization is used.

### 6.4.5.1 DELTA DIRECTIONAL ELEMENT

Where Distance protection is being applied, a 'Delta' algorithm is provided to directionalize all the distance elements; mho and quadrilaterals. If the Delta directional is not used i.e. If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Disabled`, the relay reverts to a conventional directional line for mho and quadrilateral. This conventional line is depicted in the DIRECTIONAL QUADRILATERALS section.

If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Enabled`, the IED will also switch to a conventional line if:

- it is set to `Enabled` in ***Static Test*** under *COMMISSION TESTS*
- if there is not enough Delta V and Delta I measurement
- if the memory has elapsed or is not valid (SOTF condition)

If Delta directional is used in conjunction with aided schemes, this Delta algorithm can also provide additional protection in the form of directional comparison protection.

#### 6.4.5.1.1 DELTA DIRECTIONAL PRINCIPLE AND SETUP

Delta directional looks at the relative phase angle of the superimposed current ΔI (delta I) compared to the superimposed voltage ΔV (delta V), at the instant of fault inception. The delta is only present when a fault occurs and a step change from the pre-fault steady-state load is generated by the fault.

Under healthy network conditions the system voltage is close to Vn nominal and load current flows. Under such steady-state conditions, if the voltage measured on each phase now is compared with a stored memory from exactly two power-system cycles previously, the difference between them is zero. Zero voltage change (ΔV = 0) and zero current change (ΔI = 0), except when there are changes in load current.

When a fault occurs on the system, the delta changes measured are:

ΔV = fault voltage (time "t") - pre-fault healthy voltage (t-2 cycles)

ΔI = fault current (time "t") - pre-fault load current (t-2 cycles)

The delta measurements are a vector difference, resulting in a delta magnitude and angle. Under healthy system conditions the pre-fault values are those measured 2 cycles earlier. When a fault is detected the pre-fault values are retained for the duration of the fault.

The changes in magnitude are used to detect the presence of the fault and the angles are used to determine whether the fault is in the Forward or Reverse direction.

The following figure shows the superimposed (delta) sequence networks fora single phase to earth fault.

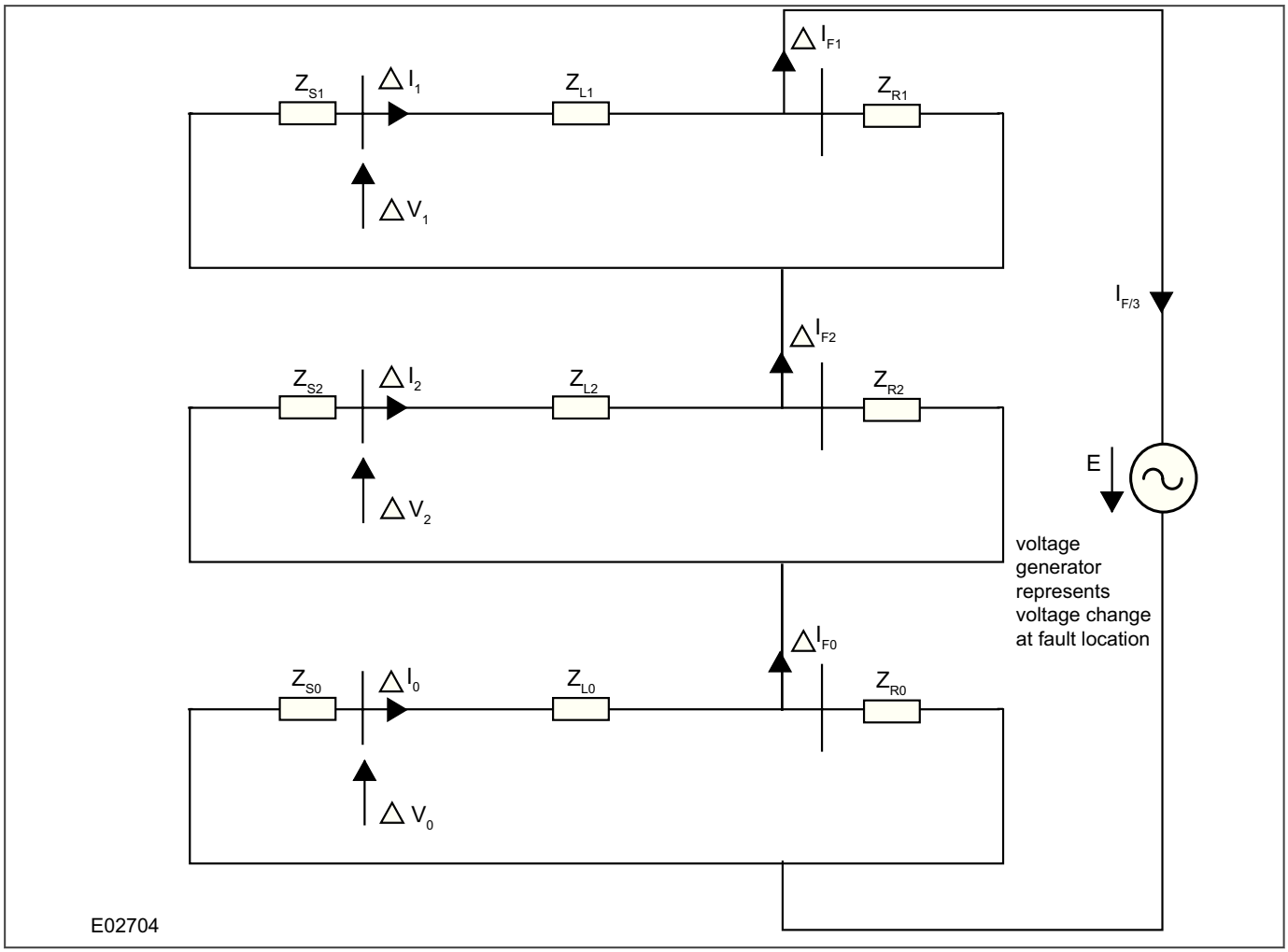



**Figure 67: Superimposed sequence networks connection for an internal A-N fault**

The fault is shown near to the busbar at end R of the line, and results in a connection of the positive, negative, and zero sequence networks in series. The delta diagram shows that any fault is a generator of Δ, connected at the location of the fault inception. The characteristics of the deltas are:

- The ΔI generated by the fault is equal to the total fault arc current.
- The ΔI splits into parallel paths, with part contribution from source “S” and part from remote end “R” of the line. Therefore each element measures a lower proportion of ΔI.
- The ΔV generated by the fault is equal to the fault arc voltage minus the pre-fault voltage, so it is in anti-phase with the pre-fault voltage.
- The ΔV measured by the protection is the voltage drop across the source impedance behind the protection location. This is generally smaller than the DV measured at the fault location, because the voltage collapse is smaller nearer to the source than at the fault.
- For fault detection, the measured ΔI and ΔV associated with the fault must be greater than the ***Dir I Fwd*** and ***Dir V Fwd*** settings respectively.

#### 6.4.5.1.2 DELTA DIRECTIONAL DECISION

Delta quantities are generated when a fault starts. The following criteria characterise the fault direction:

**For a forward fault:**

ΔV is a decrease in voltage, so it is in the negative sense. ΔI is a forward current flow, so it is in the positive sense. Where ΔI and ΔV are approximately in anti-phase, the fault is forward. The exact angle relationship for the forward fault is:

$$\Delta V / \Delta I = -(\text{Source impedance } Zs)$$

where Zs is the source impedance behind the protection.

**For a reverse fault**

ΔV is a decrease in voltage, so it is in the negative sense. ΔI is an outfeed flowing in the reverse direction, so it is in the negative sense. Where ΔI and ΔV are approximately in phase, the fault is reverse. The exact angle relationship for the reverse fault is:

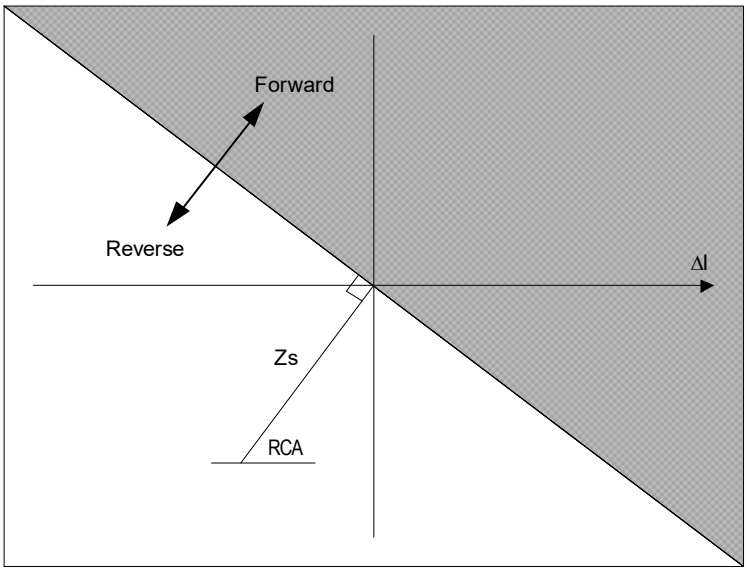
$$\Delta V / \Delta I = (\text{Remote Source impedance } Zr + ZL)$$

where ZL is the protected line impedance and Zr is the remore end source impedance.

A directional characteristic angle (RCA) setting (***Dir. Char Angle***) allows you to set the centre of the directional characteristic according to the amount by which the current nominally lags the reference ΔV. The characteristic boundary is then +/- 90° either side of the set characteristic angle.

*Note:*
*If Delta directional aided scheme is not used, Distance zone directionalizing uses fixed operating thresholds: ΔV=0.5V and ΔI=5%In. If the fault ΔV is below the setting of 0.5V, a conventional distance line ensures correct forward/reverse polarizing. For Delta directional aided schemes, sufficient ΔV must be present for tripping to occur.*

The delta directional element will produce a forward decision when the angle between the delta volts and delta current shifted by the ***Dir. Char Angle*** setting is greater than 90°. The ***Dir. Char Angle*** setting is the characteristic angle of the source impedance, Zs.




RCA = Characteristic angle setting (***Dir. Char Angle***)

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**Figure 68: - ΔV Forward and Reverse tripping regions**

To facilitate testing of the distance elements using test sets, which do not provide a dynamic model to generate true fault delta conditions, set the ***Static Test*** setting in the *COMMISSION TESTS* column to `Enabled`. This disables phase selector control and forces the protection to use a conventional (non-delta) directional line.

*Note:*
*Some test sets with dynamic models have the facility to include a DC offset. We strongly recommend the use of the DC offset because the waveform created with no DC offset sometimes creates a current step that is not realistic and this could cause a problem in the delta algorithm.*

## 6.4.6 DISTANCE ELEMENT ZONE SETTINGS

The settings for the Distance protection are contained in the *DISTANCE SETUP* and *DIST. ELEMENTS* columns of the relevant settings group.

The Distance protection has a ***Setting Mode*** which is set to `Simple` by default. We recommend the default for most applications.. Instead of entering distance zone impedance reaches in ohms, zone settings are simply entered in terms of percentage of the protected line data specified with the ***Line Impedance*** setting in the *LINE PARAMETERS* column. The setting assumes that the residual compensation factor is equal for all zones. The protection calculates the required reach settings from the percentage settings. The calculated zone reaches are available for viewing but you cannot change a value.

An ‘Advanced’ Setting Mode allows individual distance ohmic reaches and residual compensation factors to be entered for each zone. When ‘Advanced’ mode is selected, all ‘percentage’ settings that are associated to ‘Simple’ setting mode in the *DISTANCE SETUP* column will be hidden and the Distance zone settings need to be entered for each zone in the *DIST. ELEMENTS* column.

If you use the ‘Simple’ Settings Mode, the *DIST. ELEMENTS* column contains a list of what settings have been automatically calculated and applied. This list is useful as a reference for commissioning and periodic injection testing. If you use the ‘Advanced’ Setting Mode, however, you must enter all settings for each zone.

*Note:*
*Distance zones are directionalized by a Delta Directional decision. The characteristic angle for this decision is set with the Delta Directional configuration, in the DISTANCE SETUP column. The default setting is 60°.*

### 6.4.6.1 ADVANCED DISTANCE ZONE SETTINGS

The ***Setting Mode*** is set in the *DISTANCE SETUP* column. There are two possible modes; simple and advanced.

If set to `Simple`, you need only to enter the line parameters such as length, impedances and residual compensation found in the *LINE PARAMETERS* column. You set the reach in terms of percentage of the protected line.

We recommend the `Advanced` setting for networks where the protected and adjacent lines are of dissimilar construction, requiring independent zone characteristic angles and residual compensation. In this setting mode all individual distance ohmic reach and residual compensation settings and operating current thresholds per each zone are accessible.

If you use the advanced setting mode, you also need to set the minimum current sensitivity for each zone (***Zn Sensit. Iph>n***, and ***Zn Sensit. Ignd>n***).

The current sensitivity setting for each zone is used to set the minimum current that must flow in each of the faulted phases before a trip can occur. For example, if a phase A-B line fault is present, the protection must measure both currents Ia and Ib above the minimum set sensitivity.

The default setting is 7.5% In for Zones 1 and 2, and 5% In for other zones, ensuring that distance element operation is not constrained, right through to an SIR ratio of 60.

When quadrilateral characteristics are used, you can set the tilt angle of the impedance reach lines.

In `Advanced s`etting mode, the impedance reach lines of the quadrilateral characteristics are fixed, but not as horizontal reactance lines. To account for phase angle tolerances in the current and voltage transformers, etc., the lines are tilted downwards at a droop of -3°.

In `Advanced s`etting mode, the tilt of the top lines can be changed from these values.

### 6.4.6.2 DISTANCE ZONE SENSITIVITIES

In the `Simple` ***Setting Mode*** a minimum current sensitivity applies but the value is automatically calculated and applied based on the data entered in the 'Simple' settings fields. The criteria used to calculate the setting value are needed for a minimum value of current flowing in the faulted loop and for the Zone reach point voltage. For Zones other than 1 or 2, the minimum current must be greater than 5% of the rated current and the minimum voltage at the Zone reach point must be 0.25V. The current equating to the reach point criteria can be expressed as 0.25/Zone reach and the sensitivity can be expressed as:

$$\text{Sensitivity} = \max(5\%\text{In}, (0.25/\text{Zone reach}))$$

Zones 1 and 2 are set less sensitive than the reverse Zone 4. This ensures stability of the protection in either an overreaching or a blocking scheme. For Zones 1 and 2, the same criteria are applied as for the other Zones. Also a minimum sensitivity criterion is applied, depending on the Zone 4 sensitivity. The sensitivity must exceed 1.5 x Zone 4 sensitivity and can be expressed as:-

$$\text{Sensitivity (Z1, Z2)} = \max(5\%\text{In}, (0.25/\text{Zone reach}), (1.5 \times \text{Zone 4 sensitivity}))$$

Or

$$\text{Sensitivity (Z1, Z2)} = \max(5\%\text{In}, (0.25/\text{Zone reach}), (1.5 \times (0.25/\text{Zone 4 reach})))$$

The dependency on the Zone 4 element always applies, even if Zone 4 is disabled.

The default reach setting for Zones 1, 2, and 4 are 80%, 120%, and 150% respectively. For these settings the zone-dependent terms can be reduced to:

$$0.25/\text{Zone 1 reach} = 0.25/(0.8 \times \text{line impedance})$$

0.25/Zone 2 reach = 0.25/(1.2 x line impedance)

1.5 x (0.25/Zone 4 reach) = 0.25/line impedance

In such cases, for Zone 1, the dominant Zone reach term is that of Zone 1 and the equation can be reduced to:

Sensitivity (Z1) = max (5%In, (0.25/(0.8 x line impedance)))

For lines with an impedance of less than 6.25 Ω the Zone 1 reach term dominates and the sensitivity is greater than 5% In. Above this line impedance the sensitivity is 5% In.

Similarly, for Zone 2, the dominant Zone reach term is that of Zone 4 and the equation can be reduced to:

Sensitivity (Z2) = max (5%In, (0.25/line impedance))

For lines with an impedance of less than 5 Ω the Zone reach term dominates and the sensitivity is greater than 5% In. Above this line impedance the sensitivity is 5% In.

In `Advanced` setting mode the same qualifications for distance zone minimum sensitivity as minimum sensitivity should be applied to ensure distance element accuracy.

## 6.4.7 CAPACITOR VT APPLICATIONS

The device provides a setting for capacitor-coupled voltage transformer (CVT) applications. This setting is ***CVT Filters*** and is found in the *DISTANCE SETUP* column. The default setting is `Disabled` which us used for conventional wound voltage transformers. If CVTs are used you can set ***CVT Filters*** to either `Passive`, or `Active` to reduce the effects of transient components caused by close up faults.

### 6.4.7.1 CVTS WITH PASSIVE SUPPRESSION OF FERRORESONANCE

Passive suppression to reduce the effects of transient components that could be caused by close up faults uses an anti-resonance design and the resulting transient distortion is fairly small. Passively suppressed CVTs are sometimes classed as type 2. In passive CVT applications, the effect on characteristic accuracy is generally negligible for source to line impedance ratios of less than 30 (SIR < 30). However, with a high Source-to-Line Impedance Ratio (SIR), it is advisable to set ***CVT Filters*** to `Passive`.

By setting ***CVT Filters*** to `Passive`, the protection can trip at sub-cycle speeds, unless the actual SIR is above that which is set. If the SIR is estimated to be higher than the setting, the instantaneous operating time is increased by about a quarter of a power frequency cycle. The protection estimates the SIR as the ratio of nominal rated voltage Vn to the size of the comparator vector IZ (in volts):

SIR = Vn/IZ

where:

- Vn = Nominal phase to neutral voltage
- I = Fault current
- Z = Reach setting for the zone concerned

Therefore, for slower operation, I needs to be low, as restricted by a relatively weak infeed and Z needs to be small, as for a short line.

### 6.4.7.2 CVTS WITH ACTIVE SUPPRESSION OF FERRORESONANCE

Active suppression to reduce the effects of transient components that could be caused by close up faults uses a tuned L-C circuit in the CVT. The damping of transients is not as efficient as for passive suppression. Active suppression CVTs are often called type 1 CVTs. In active CVT applications, to ensure reach point accuracy, the ***CVT Filters*** setting should be set to `Active`. The protection varies according to the calculated source to line impedance ratio SIR (= Vn / IZ).

where:

- Vn = Nominal phase to neutral voltage
- I = Fault current
- Z = Reach setting for the zone concerned

Sub-cycle tripping is maintained for lower SIRs, up to a ratio of 2. The instantaneous operating time is increased by about a quarter of a power frequency cycle at higher SIRs.

Transients caused by voltage dips, however severe, do not affect the protection's directional measurement because it uses voltage memory.

## 6.4.8 LOAD BLINDING

Load blinders are provided for both phase and earth fault distance elements, to prevent incorrect-tripping for heavy load flow. A blinder envelope which surrounds the expected worst case load limits should be configured to block tripping for any impedance measured in the blinded region. Only a fault impedance which is outside the area bounded by the load blinders is allowed to cause a trip. The blinder characteristics are shown in the following figure:

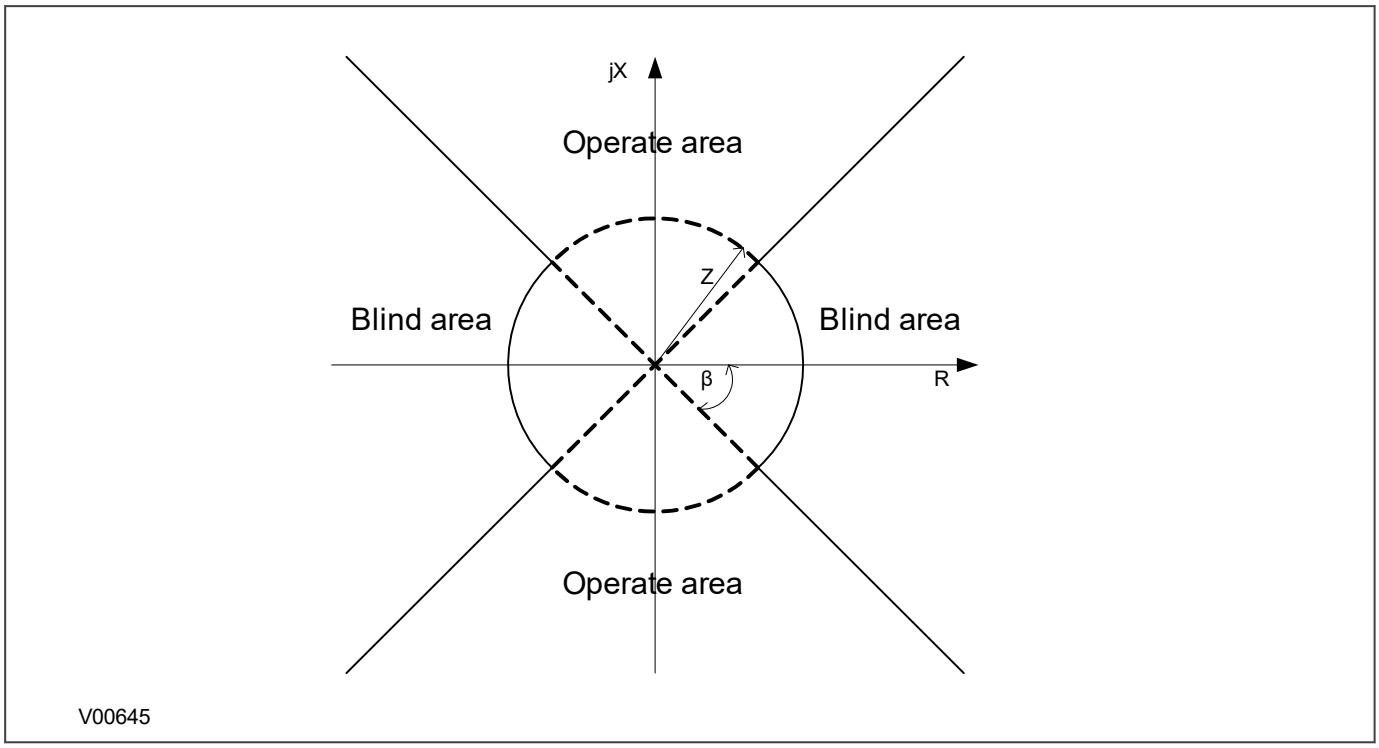



**Figure 69: Load Blinder Characteristics**

- Z denotes the Load/B Impedance setting. This sets the radius of the under-impedance circle.
- ß denotes the Load/B Angle setting. This sets the angle of the two blinder boundary lines - the gradient of the rise or fall with respect to the resistive axis.

The protection can allow the load blinder to be bypassed any time that the measured voltage for the phase in question falls below an undervoltage setting. Under such circumstances, the low voltage could not be attributed to normal voltage excursion tolerances on load. A fault must be present on the phase in question, so it is acceptable to override the blinder action and allow the Distance protection to trip for an in-zone measurement. The advantage of bypassing the load blinders is that the resistive coverage for faults near to the protection location can be higher.

To use the load blinders you must set the ***Load Blinders*** setting to `Enabled`. You then set appropriate values for the blinder impedance using the ***Z< Blinder Imp*** setting, the β value using the ***Load/B Angle*** setting, and the undervoltage threshold using the ***Load Blinder V<*** setting.

### 6.4.9 CROSS COUNTRY FAULT PROTECTION

"Cross country fault" is a term that has been adopted to cover a fault scenario where two separate single-phase faults occur on a system together. For example, where single-pole tripping is employed, if a single phase-to-earth fault occurs, the voltages on the other phases can rise above normal. This may cause a breakdown elsewhere on the system and result in another fault involving a different phase to the one on which the original fault occurred.

The distance protection in this product features cross-country override logic, which is built into the phase selector. The logic is dedicated to providing Cross-Country fault protection for solidly-earthed systems. It ensures correct operation a fault in Zone 1 that may evolve to involve a different phase. For isolated or compensated earthing systems a settable phase preferential logic will be used for cross-country faults instead.

The cross-country override logic:

- Prevents possible false operation of the phase-phase distance elements whilst allowing the appropriate Zone1 phase-earth element to trip.
- Acts when the distance protection makes a multiple phase selection (where more than one phase is involved in the fault), but only one Zone 1 phase-earth element picks up. Only "on-angle" operation of the Zone 1 phase-earth element can activate the logic. this prevents incorrect operation due to impedance encroachment.
- Allows only one Zone 1 phase-earth element to operate. The operation of that element must match the phase pick-up indication of the phase selector. For example, if the original phase selection indicated involvement of only B and C phases, the logic could allow a BN trip or a CN trip to override the phase-phase selection, but override by the AN element is not allowed.
- Does not apply if more than one forward Zone 1 element picks up. In this case the fault is considered multi-phase and the protection trips three-pole.

*Note:*
*Load blinding can be applied for phase and earth characteristics. Residual compensation is not applied. Phase characteristics use phase-to-phase voltage and phase-to-phase current. Earth fault characteristics use phase-to-neutral voltage and phase-to-neutral current.*

# 6.5 DISTANCE ISOLATED AND COMPENSATED SYSTEMS

## 6.5.1 PETERSEN COIL EARTHED SYSTEMS

A Petersen Coil earthing system is used in compensated earthing systems, as well as being used in cases of high impedance earthing. Petersen Coil earthed systems (also called compensated or resonant systems) are commonly found in areas where the system consists mainly of rural overhead lines. They are particularly beneficial in locations which are subject to a high incidence of transient faults. In a Petersen Coil earthed system, the network is earthed via a reactor, whose reactance is tuned to be nominally equal to the total system capacitance to earth. Similar to insulated systems, if a single-phase to earth fault is applied to a Petersen Coil earthed system, under steady state conditions no earth fault current flows. The effectiveness of the method in reducing the current to zero is dependent on the accuracy of the tuning of the reactance value and any changes in system capacitance (for example due to system configuration changes) require changes to the coil reactance. In practice, perfect matching of the coil reactance to the system capacitance is difficult to achieve, so that a small earth fault current will flow.

In isolated and compensated earthed systems, if an earth fault current is below a certain level, then the fault will self-extinguish due to the low current magnitude. It therefore appears as a transient phenomenon. The figure below shows earth fault current levels, below which they self-extinguish on these types of system. Statistics demonstrate that around 80% of earth faults in Petersen Coil earthed systems self-extinguish. This, in part, explains their popularity.

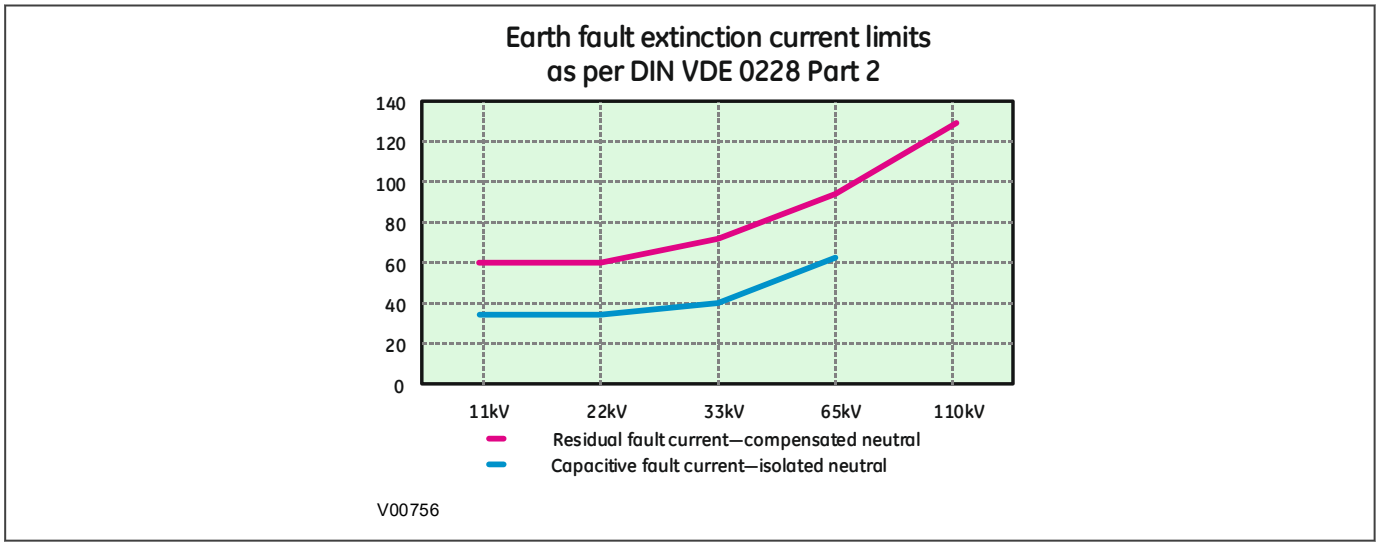



**Figure 70: Current level (amps) at which transient faults are self-extinguishing**

The following figure depicts a simple network earthed through a Petersen Coil reactance. It can be shown that if the reactor is correctly tuned, theoretically no earth fault current will flow.

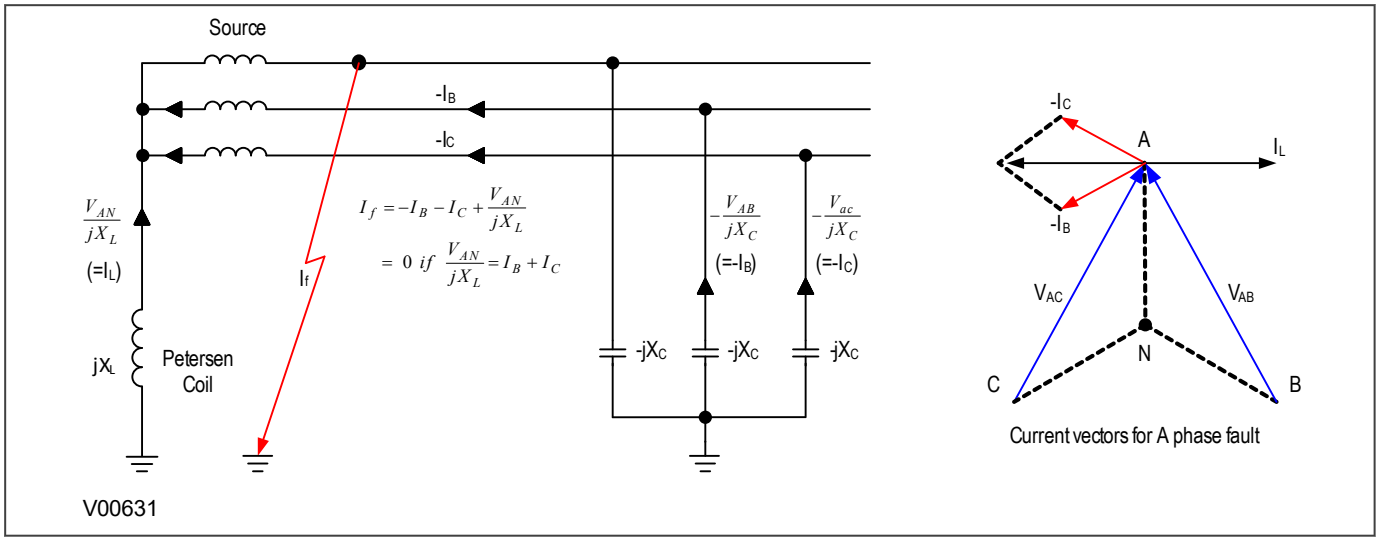



**Figure 71: Earth fault in Petersen Coil earthed system**

Consider a radial distribution system earthed using a Petersen Coil with a phase to earth fault on phase C, shown in the figure below:

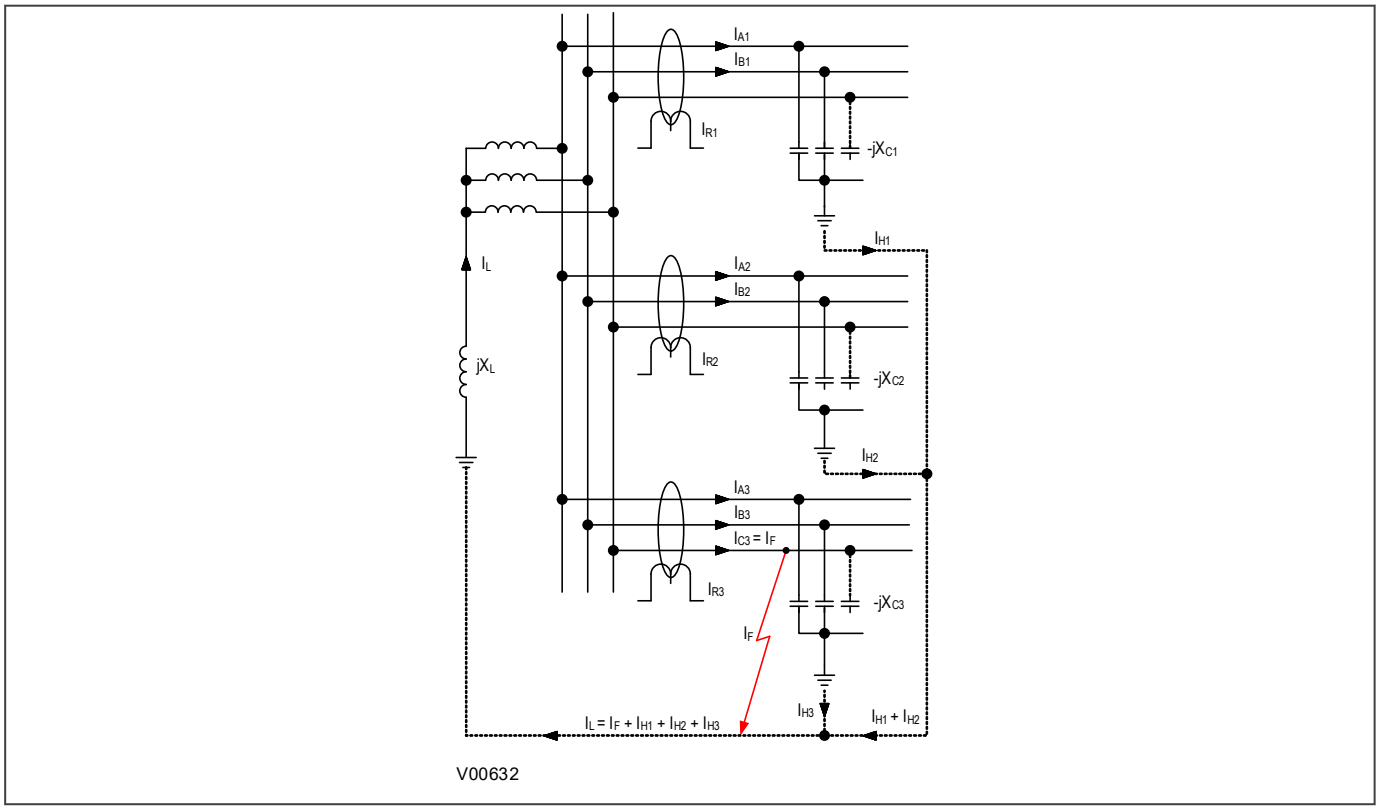



**Figure 72: Distribution of currents during a Phase C fault**

Assuming that no resistance is present in $X_L$ or $X_C$, the resulting phasor diagrams will be as shown in the figure below:

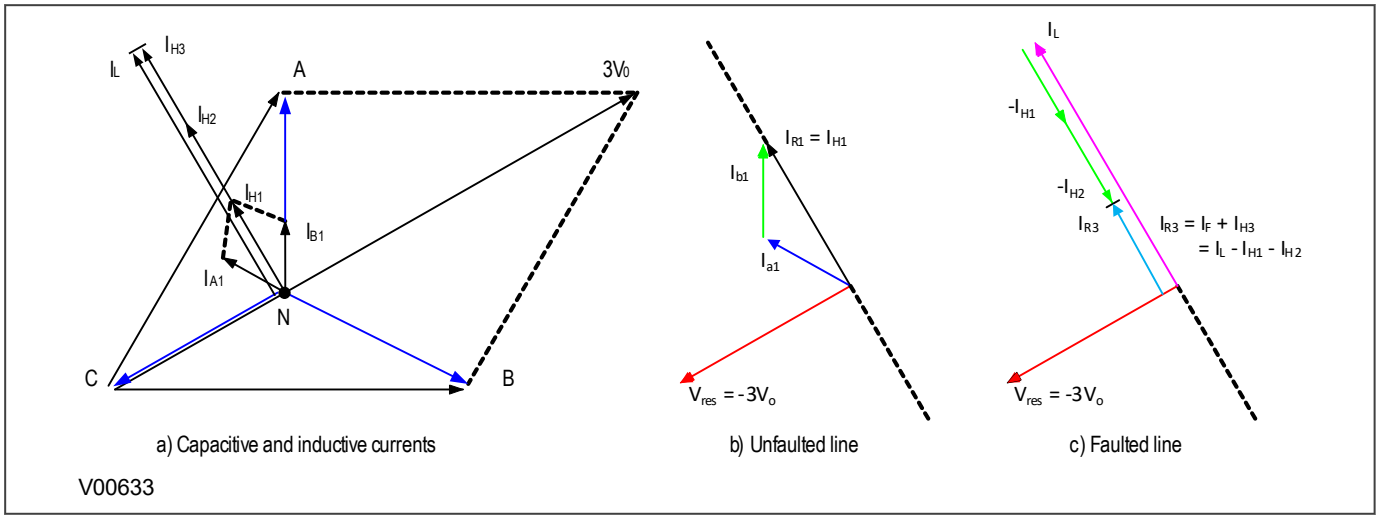



**Figure 73: Phasors for a phase C earth fault in a Petersen Coil earthed system**

It can be seen that:

- The voltage in the faulty phase reduces to almost 0V
- The healthy phases raise their phase to earth voltages by a factor of √3
- The triangle of voltages remains balanced
- The charging currents lead the voltages by 90°

Using a core-balance current transformer (CBCT), the current imbalances on the healthy feeders can be measured. They correspond to simple vector addition of $I_{A1}$ and $I_{B1}$, $I_{A2}$ and $I_{B2}$, $I_{A3}$ and $I_{B3}$, and they lag the residual voltage by exactly 90º.

The magnitude of the residual current $I_{R1}$ is equal to three times the steady-state charging current per phase. On the faulted feeder, the residual current is equal to $I_L$ - $I_{H1}$ - $I_{H2}$ (C). This is shown in the zero sequence network shown in the following figure:

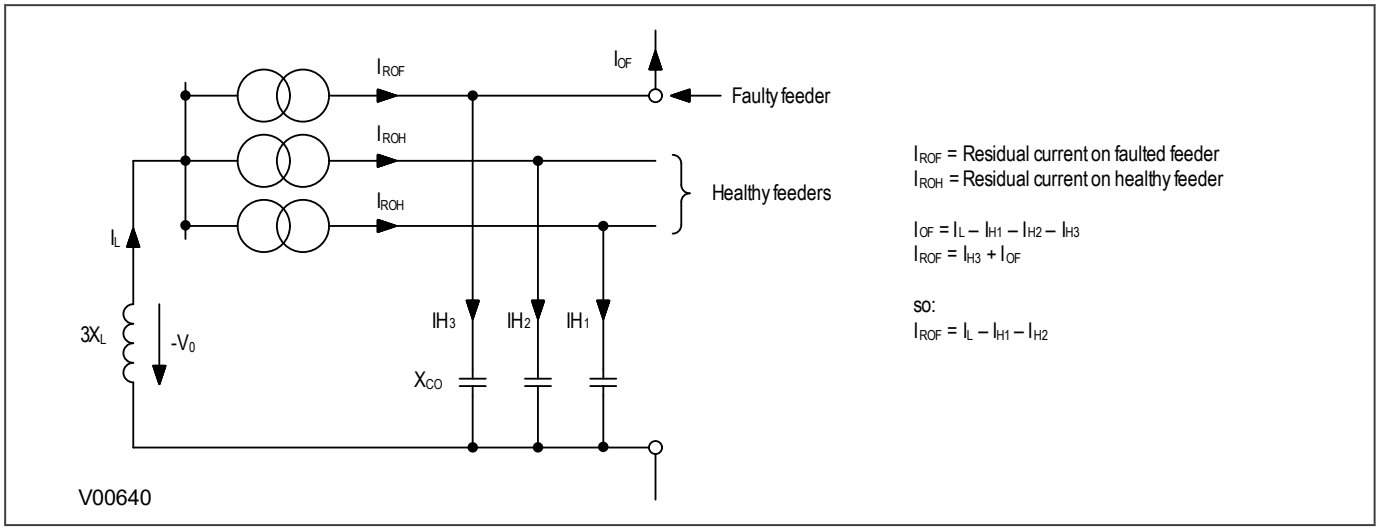



**Figure 74: Zero sequence network showing residual currents**

In practical cases, however, resistance is present, resulting in the following phasor diagrams:

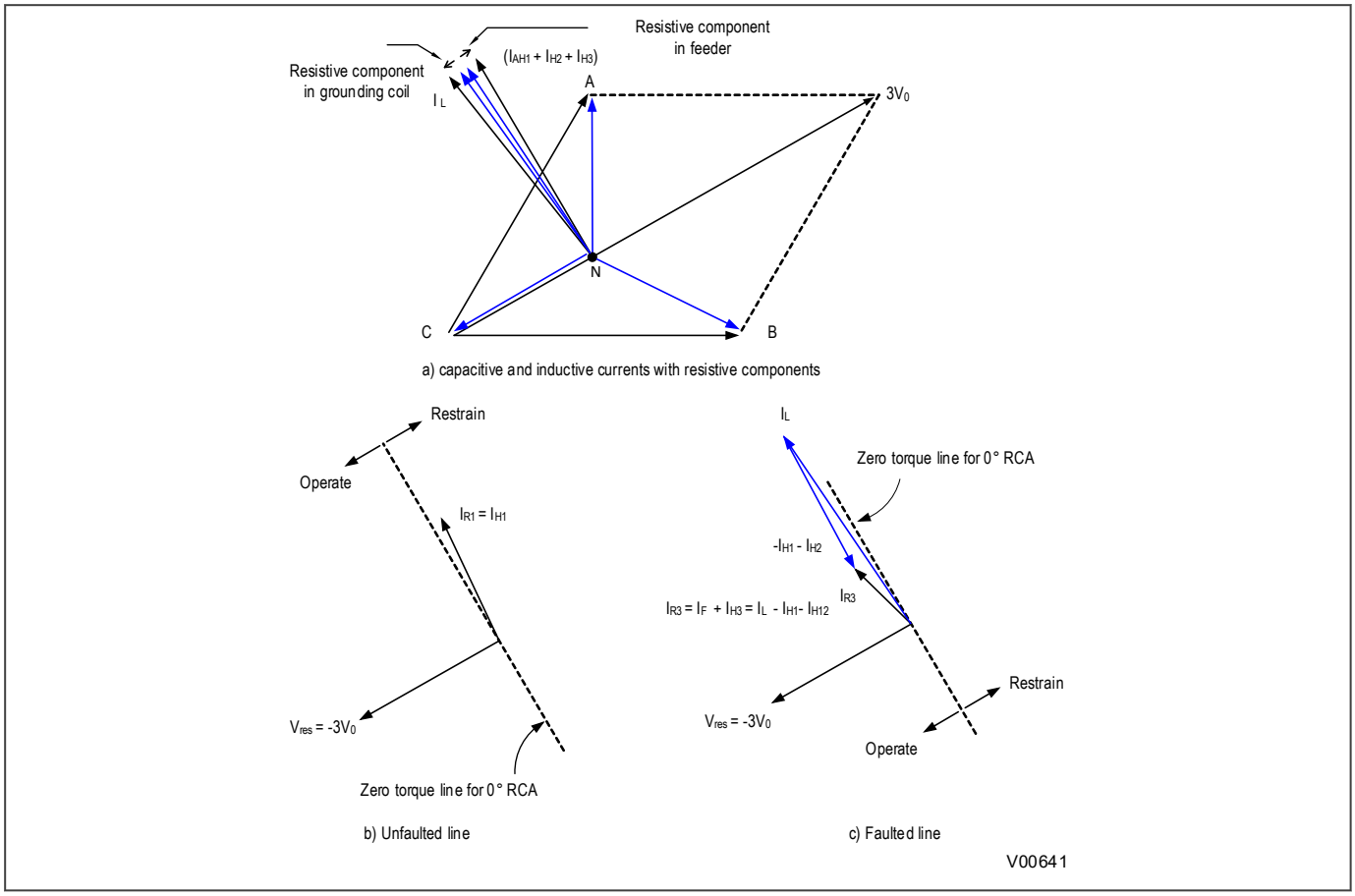



**Figure 75: Phase C earth fault in Petersen Coil earthed system: practical case with resistance present**

If the residual voltage is used as the polarising voltage, the residual current is phase shifted by an angle less than 90° on the faulted feeder, and greater than 90° on the healthy feeders. With an RCA of 0°, the healthy feeder residual current will fall in the ‘restrain’ area of the characteristic while the faulted feeder residual current falls in the ‘operate’ area.

Often, a resistance is deliberately inserted in parallel with the Petersen Coil to ensure a measurable earth fault current and increase the angular difference between the residual signals to reinforce the directional decision.

Directionality is usually implemented using a Wattmetric function, or a transient earth fault detection function (TEFD), rather than a simple directional function, since they are more sensitive. For further information about TEFD, refer to Transient Earth Fault Detection in the Current Protection Functions chapter.

## 6.5.2 EARTH FAULT DISTANCE PROTECTION FOR ISOLATED AND COMPENSATED SYSTEMS

There are four types of fault that need to be considered when providing distance protection for isolated or compensation earthed systems. These are faults involving three phases, phase to phase faults, faults involving just a single-phase to earth, and cross-country faults involving separate single phase to earth faults.

Faults involving three phases and phase to phase faults do not require special attention; tripping is in accordance with zone impedance limits, fault direction, and zone time delay.

Faults on isolated or compensated earthed systems involving single-phase to earth, or cross-country faults do require special attention.

#### 6.5.2.1 SINGLE-PHASE TO EARTH FAULTS ON ISOLATED OR COMPENSATED SYSTEMS

On isolated or compensated earthed systems, a single-phase to earth fault does not lead to a short circuit as only a small capacitive or compensated current flows to earth. In most cases, the earth fault will self-extinguish. In the remaining cases, the system can continue to operate with the earth fault present, until the fault is located and removed by isolating the faulted feeder. Indication of the earth fault can be provided by Wattmetric function, or a Transient Earth Fault Detection function (TEFD).

For a fault on a solidly earthed network, distance protection is required to trip as quickly as possible to isolate the fault. This is for all fault types including a single-phase to earth fault. In isolated or compensation-earthed systems, a single-phase to earth fault needs to be correctly identified for network control, but instantaneous tripping should not happen since the system can be (at least for a certain period of time) remain connected - as the magnitude of the fault current will not be very high - and/or the fault will in most cases self-extinguish.

Moreover, for a solid earth fault, the voltage on the faulted phase may be 0V across the whole of the galvanically connected network. Using a collapsed voltage in conjunction with the load current would give measured impedance values on the faulted phase of 0Ω across the network, causing incorrect, and uncontrolled, tripping.

Since distance protection should not operate for a single-phase to earth fault, pick up of fault detection elements under single-phase to earth fault conditions must not lead to tripping. This can be a particular problem on large isolated networks, where capacitance to earth is large. When a single-phase to earth fault occurs, the voltages on the unfaulted phases increase relative to earth, and so too do the associated capacitive earth currents. During the initial half cycle after fault inception, the arc-ignition earth current amplitude of the disturbance may be much higher than nominal current, with a frequency close to the nominal system frequency. To prevent incorrect detection during single-phase to earth faults, it is common practice to delay single-phase to earth fault detection on isolated or compensation-earthed systems by a short delay. This delay is bypassed if the fault evolves into a double earth fault.

#### 6.5.2.2 CROSS-COUNTRY FAULTS ON ISOLATED OR COMPENSATED SYSTEMS

While a single-phase to earth fault is present on an isolated or compensation earthed system, the phase to earth voltage on the healthy phases rises by a factor of $\sqrt{3}$. Due to this rise, double earth faults (or cross-country faults) may result. The double earth fault is similar to a two-phase fault; however, for the double earth faults, the fault path is from one earth-fault location to another, via earth. The second fault may be anywhere on the system, depending on where the weakest point in the insulation is located.

The likelihood of a double earth fault increases as the size of the network increases. The protection strategy usually applied for cross-country faults is to isolate one of the fault locations, with the expectation that the second fault location will then self-extinguish similar to a single-phase to earth fault. The faulted line can then be tripped manually once the fault location has been identified. Distance protection applied to isolated systems must have a so-called double earth fault phase preference, which selects a predefined phase earth loop for measurement across the entire galvanically connected network.

In the case of cross-country faults, measurements from the phase to phase loops between the two fault locations do not produce useful results as the phase currents belong to different short circuit loops. For the second fault, earth loops will measure the fault impedance more accurately. For a cross-country fault, all devices across the network should follow either a so-called "cyclic" logic or an "acyclic" logic to select a phase preference for the impedance measurement. This is used to determine which part of the system should be isolated by three-phase tripping. Tripping will allow the rest of the network to continue to operate (single earth-fault present, but supply maintained). Then, when the single phase-earth fault has been located, the faulted section can be tripped manually.

The most commonly used phase preference logic is C(A) acyclic (that is C before A before B), but other preferences can be used.

## 6.5.3 IMPLEMENTATION OF DISTANCE PROTECTION FOR ISOLATED AND COMPENSATED NETWORKS

When applying distance protection to compensated or isolated systems, the following key points must be taken into account:

- Distance protection must not trip for a single-phase to earth fault
- In the case of cross-country faults, the protection methods are different from that of solidly earthed systems. In this case either a cyclic or an acyclic logic should be used to select a phase preference for the impedance measurement

### 6.5.3.1 NETWORK EARTHING SYSTEM SETTING

The setting ***Dist.Earth Mode*** in the *DISTANCE SETUP* column defines the behaviour of the distance protection function according to the type of earthing system. The setting options are:

- *Is/Comp Earthing* for isolated or compensated systems
- *Standard* for directly earthed systems

If *Is/Comp Earthing* is selected:

- Distance protection is blocked for a single-phase to earth fault
- A earth fault is detected using the neutral current (IN) and/or the neutral voltage (VN)
- It has no influence on two-phase or three-phase fault performance
- In the case of cross-country faults, either a cyclic or an acyclic logic is invoked to select a phase preference for the impedance measurement
- The DDB signal ***Is/Comp Enabled*** (1983) is asserted

### 6.5.3.2 FIRST EARTH FAULT DETECTION

In isolated or compensated mode, no trip should occur for a single phase to earth fault. Moreover its detection by means of an impedance criteria would lead to false information as voltages around the galvanic network will be 0V for the faulty phase. Instead, an earth fault is detected by comparing $I_N$ and/or $V_N$ with a settable threshold.

You can choose to use $V_N$ only, $I_N$ only, $V_N$ OR $I_N$, or $V_N$ AND $I_N$ as your selection criteria. The mode is set by the setting ***1P Mode*** in the *DISTANCE SETUP* column. The single-phase to earth fault signal (***IS/Comp EF***) is then produced after a time delay set by ***1P Time delay***.

$I_N$> can be set from 0.05In to 1In in steps of 10 mA. $V_N$ can be set from 1V to 80V in steps of 1 V.

A pick-up timer, is available for the detection of the first earth fault. This can be set from 0 to 10 seconds in steps of 10 ms.

The mode selector decides whether the single-phase to earth fault is determined by VN> only, IN> only, VN> or IN>, or VN> and IN>. The mode is set by the setting ***1P Mode*** in the *DISTANCE SETUP* column. The single-phase to earth fault signal (***IS/Comp EF***) is then produced after a time delay set by 1P Time delay.

#### 6.5.3.2.1 NEUTRAL VOLTAGE CRITERIA

The influence of earth current in a fault can be determined by considering the changes in phase to phase and neutral displacement voltages. During earth faults, a significant displacement of the neutral voltage is expected, whilst no imbalance of the voltage triangle is to be expected. The following figure shows a Phase A to earth fault.

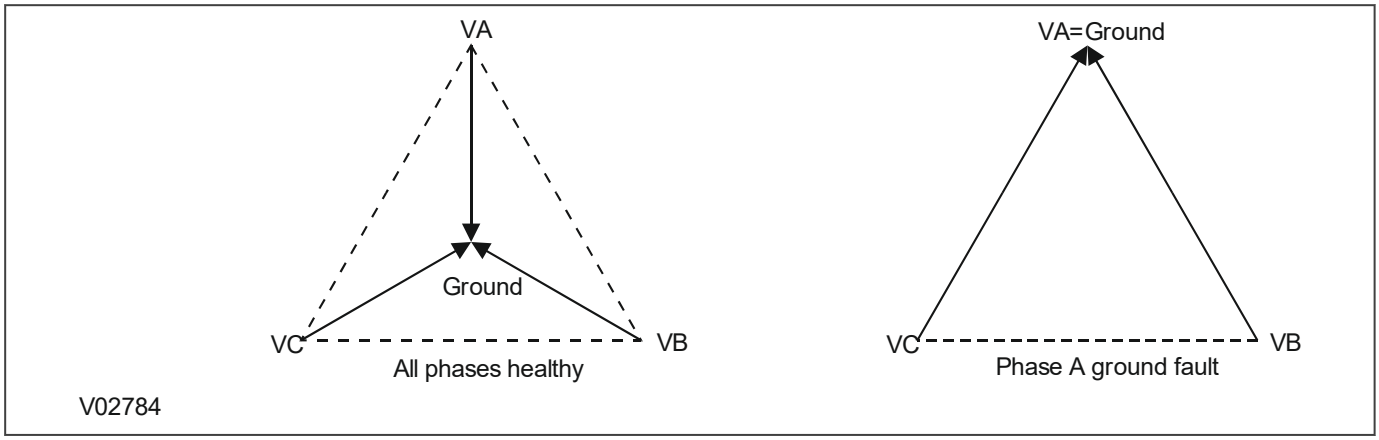



**Figure 76: Voltage distribution in an isolated system for a Phase-A-to-Earth fault**

Therefore, we can establish an earth fault by seeing if the neutral voltage $V_N$ exceeds a settable threshold ***VN> Voltage Set***, and checking whether the phase-phase voltages are still balanced.

0.8(max. $V_{ph-ph}$) < (min. $V_{ph-ph}$)

Neutral displacement is established by comparing the neutral voltage VN with a threshold set by the setting, ***VN> Voltage Set***

#### 6.5.3.2.2 NEUTRAL CURRENT CRITERIA

The bias neutral level detector (LDBN), detailed in the Biased Neutral Current Detector section, is used to improve stability and is complemented with an additional minimum threshold controlled by setting ***IN> Current set*** . A negative sequence current check is also performed for long and heavily loaded lines.

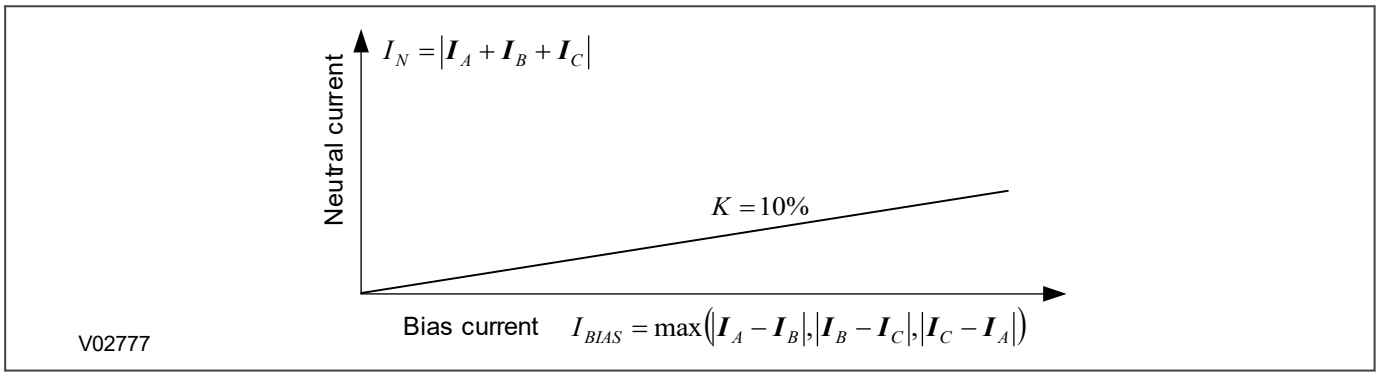



**Figure 77: Biased Neutral Current Detector**

#### 6.5.3.2.3 RELEVANT SETTINGS FOR FIRST EARTH FAULT DETECTION

The following settings are visible if the setting ***Dist.Earth Mode*** is set to `Is/Comp Earthing`.

***IN> Current Set***: Sets the threshold for the first fault earth fault overcurrent (default – 0.1In)

***VN> Voltage Set***: Sets the threshold for the first fault earth fault overvoltage (default – 12V)

***1P Mode***: Sets the first fault detection method (default – VN>)

***1P Time Delay***: Sets the first fault pickup delay (default – 50 ms)

#### 6.5.3.2.4 FIRST EARTH FAULT DETECTION

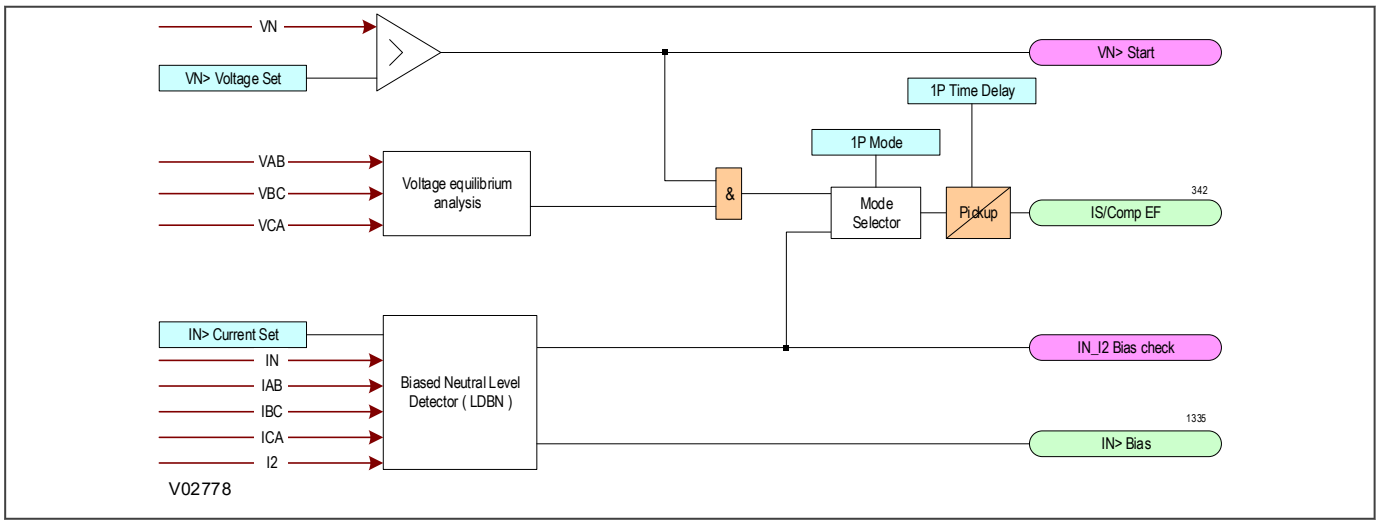



**Figure 78: First earth fault detection**

Detection of the first fault primes the detection of a second earth fault and blocks tripping of phase to phase elements for zones 1,2,3,4 (zones P, Q, R and S do not get blocked). It also creates a DDB signal indicating a single-phase earth fault (***IS/Comp EF***). Typically, with zones P and Q, the external starting zones will be used to detect if a second earth loop converges into the impedance characteristic.

The *VN> Start* signal is established by comparing the neutral voltage *VN* with a threshold set by the setting ***VN> Voltage Set***. This signal is gated with another signal indicating whether the phase voltage triangle is balanced or not and then fed into the mode selector. If the voltage triangle is balanced and there is an overvoltage condition, then a single-phase fault is indicated.

The mode selector decides whether the single phase-to-earth fault is determined by *VN>* only, *IN>* only, *VN>* or *IN>*, or *VN>* and *IN>*. The mode is set by the setting ***1P Mode*** in the *DISTANCE SETUP* column. The single phase-to-earth fault signal (***IS/Comp EF***) is then produced after a time delay set by ***1P Time Delay***.

### 6.5.3.3 FAULT DETECTION LOGIC

It is unlikely that a second fault would occur on the same phase, because the phase to neutral voltage on this phase has collapsed to zero as a result of the first fault. However, a second fault is highly likely in one of the other phases as the voltage has increased by a factor of $\sqrt{3}$ and the extra voltage will put more stress on the insulation, increasing the likelihood of a fault further down the line.

A second earth fault (on a different phase) will cause an imbalance in the voltage triangle. This is used as part of the second fault detection process. The criteria for the detection of a second fault is as follows:

A second earth fault is confirmed if a first earth fault has been detected AND the phase to phase voltage triangle is unbalanced AND the neutral voltage has exceeded the set threshold AND the neutral current has exceeded the level set by the threshold together with the bias neutral level detector (LDBN).

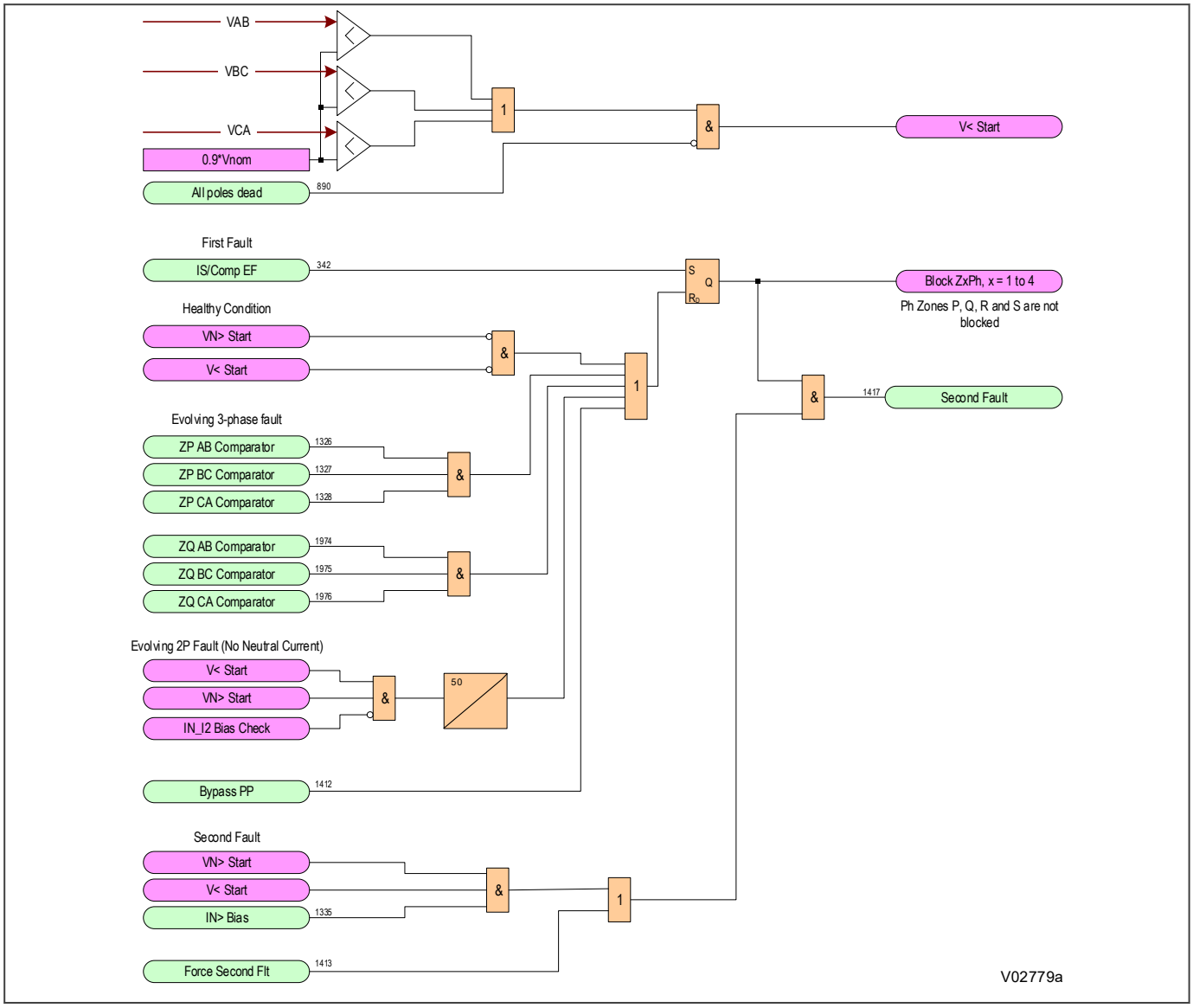



**Figure 79: Second earth fault detection logic**

A second fault is detected if additionally there is a neutral overvoltage, imbalance in the voltage triangle (phase undervoltage) and there is enough neutral overcurrent (a minimum of 50 mA for correct device operation).

### 6.5.3.4 PHASE PREFERENTIAL LOGIC

With double earth faults (cross-country faults), the aim is to isolate one of the fault locations and expect that the fault at the other location will self-extinguish, or will be tripped manually after successful detection. To achieve this for isolated or compensated systems, the distance protection must have a preference as to which phase-to-earth loop to measure.

There are two types of priority criteria; acyclic and cyclic.

Acyclic criteria are such that one of the phases is always the lowest priority. For example, A(B) Acyclic logic means: phase A is higher priority than phase B, phase B is higher priority than phase C, and phase C is the lowest priority and will never be selected, therefore C has the lowest priority. Acyclic criteria are most commonly used for distribution systems.

Cyclic criteria are such that the priorities of the phases are always compared cyclically. For example, C(A) Cyclic logic means: phase C is higher priority than phase A, phase A is higher priority than phase B, but in this case phase B priority is higher than phase C.

The definitions of all acyclic and cyclic combinations are listed in the following table:

| Criterion | Priority | Convergent Loops | Selected Phase |
|---|---|---|---|
| A(B) acyclic | A before B, B before C | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | AN<br>BN<br>AN<br>AN |
| B(A) acyclic | B before A, A before C | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | BN<br>BN<br>AN<br>BN |
| A(C) acyclic | A before C, C before B | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | AN<br>CN<br>AN<br>AN |
| C(A) acyclic | C before A, A before B | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | AN<br>CN<br>CN<br>CN |
| B(C) acyclic | B before C, C before A | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | BN<br>BN<br>CN<br>BN |
| C(B) acyclic | C before B, B before A | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | BN<br>CN<br>CN<br>CN |
| A(C) cyclic | A before C, C before B, B before A | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | BN<br>CN<br>AN<br>AN |
| C(A) cyclic | C before A, A before B, B before C | AN, BN<br>BN, CN<br>CN, AN<br>AN, BN, CN | AN<br>BN<br>CN<br>CN |

You can set the phase preference with the ***Phase prio. 2pG*** setting in the *SCHEME LOGIC* column.

*Note:*
*The **Phase prio. 2pG** setting is visible only when the **Dist.Earth Mode** setting is set to `Is/Comp Earthing` and the **BasicScheme Mode** setting is set to `Alternative`.*

#### 6.5.3.4.1 PRIORITY SETTING ENABLE LOGIC

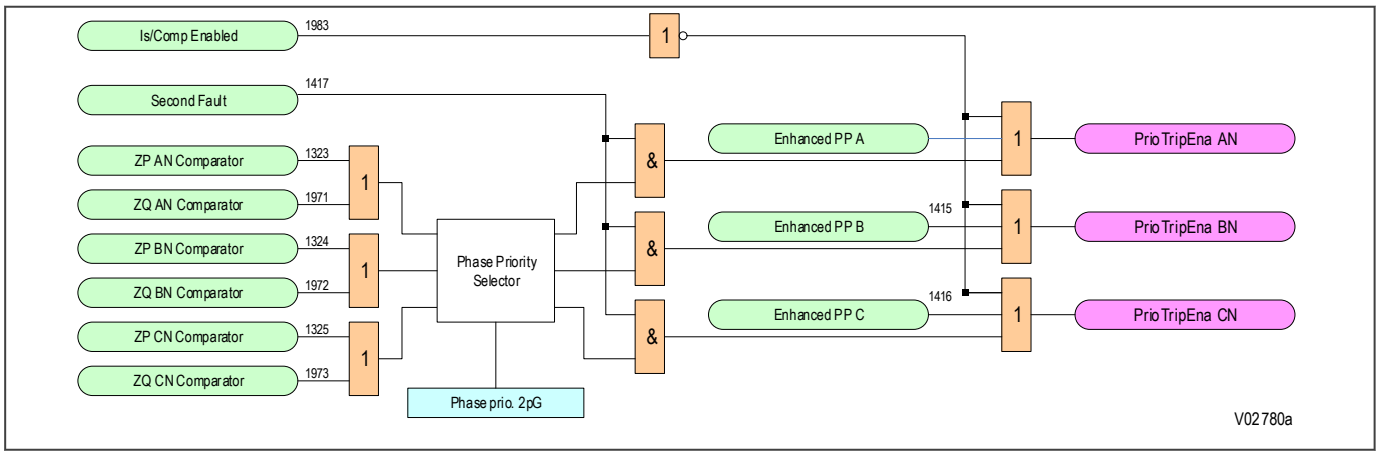



**Figure 80: Priority setting enable logic**

*Note:*
*The phase preference priority selector requires that at least two of the phase to ground loops, as indicated in the table above, are in Zone P or Q.*

In isolated and compensated systems, if the coil is bypassed/faulted and the system becomes effectively solidly earthed, the distance relay shall behave as normal, i.e. no pre-determined phase preference logic to decide which loop will trip. When the coil is in service/not-faulted, the IED shall operate with the phase preference logic. In order to enable this operation and bypass the phase preference logic, an external signal or an internal function can be linked to the DDB 1412 ***ByPass PP*** . This linked input could be an overcurrent start or an external input indicating the coil is bypassed/faulted for example.

### 6.5.3.4.2 ZONE STARTING LOGIC

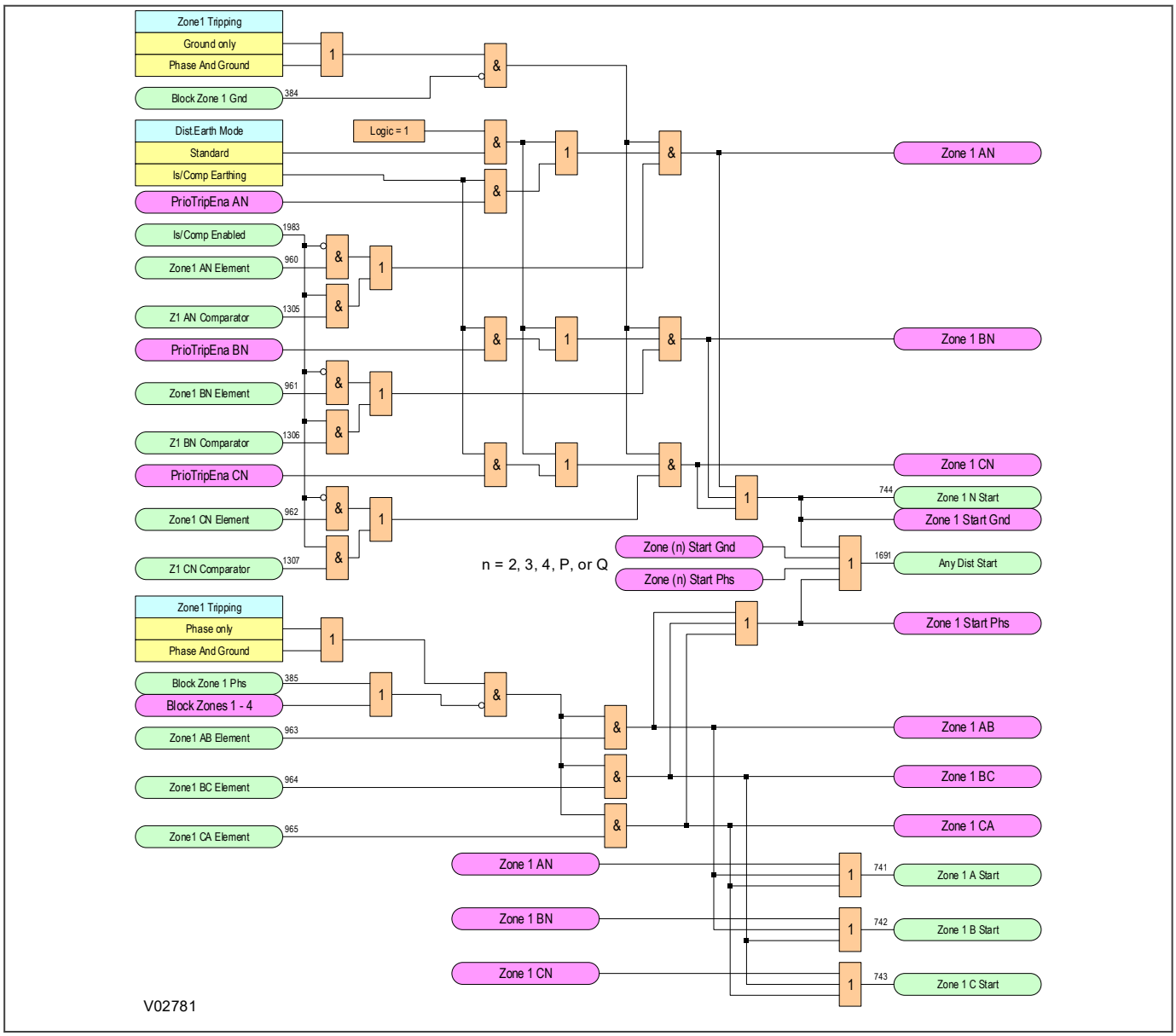



**Figure 81: Zone starting logic**

### 6.5.3.4.3 ZONE TIMER LOGIC

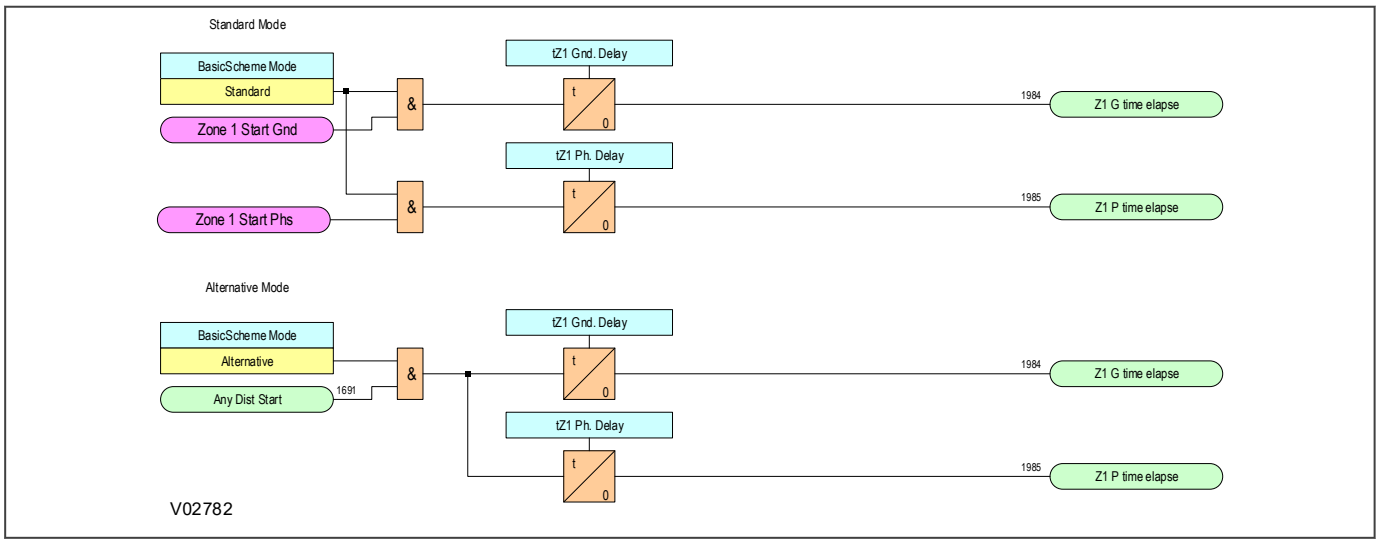



**Figure 82: Zone timer logic**

*Note:*
*Although the diagram above shows zone 1 logic only, the logic for all other zones follows the same principals.*

### 6.5.3.4.4 ZONE TRIP LOGIC

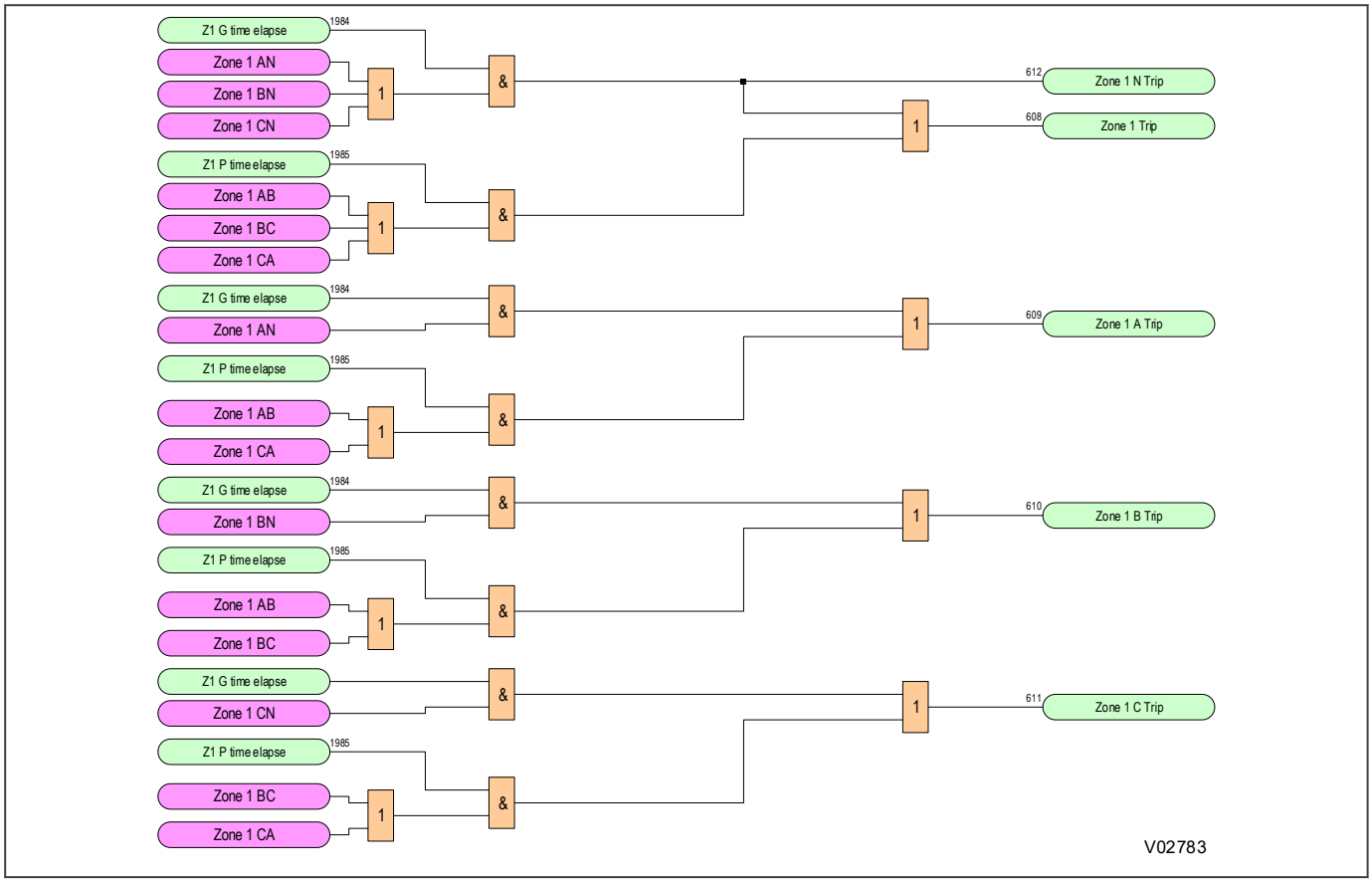



**Figure 83: Zone trip logic**

*Note:*
*Although the diagram above shows zone 1 logic only, the logic for all other zones follows the same principals.*

# 6.6 APPLICATION NOTES

## 6.6.1 SETTING MODE CHOICE

This product has two setting modes for distance protection: *Simple*, or *Advanced*. In the majority of cases, we recommend the *Simple* setting. Using the *Simple mode*, you need only enter the line parameters such as length, impedances and residual compensation. You set the reach in terms of percentage of the protected line.

We recommend the *Advanced* setting mode for networks where the protected and adjacent lines are of dissimilar construction, requiring independent zone characteristic angles and residual compensation. In *Advanced* setting mode all individual distance ohmic reach and residual compensation settings and operating current thresholds are accessible for every zone.

## 6.6.2 OPERATING CHARACTERISTIC SELECTION

In general, we recommend the following characteristics:

- For short line applications: Select Mho for phase fault zones and quadrilateral for earth fault zones.
- For open delta (vee-connected) voltage transformer applications: Set Mho for phase fault distance protection. For Earth Fault protection, disable the Earth Fault Distance elements and use Directional Earth Fault instead.
- For series compensated lines: Select Mho characteristics for both phase- and earth-faults.

### 6.6.2.1 PHASE CHARACTERISTIC

The phase characteristic selection is common to all zones, allowing Mho or quadrilateral selection. Generally, the characteristic chosen matches utility practice. Generally we would recommend a Mho characteristic for line protection and a quadrilateral characteristic for cable applications.

The following figure shows the basic settings needed to configure a forward-looking quadrilateral zone (blinder not shown).

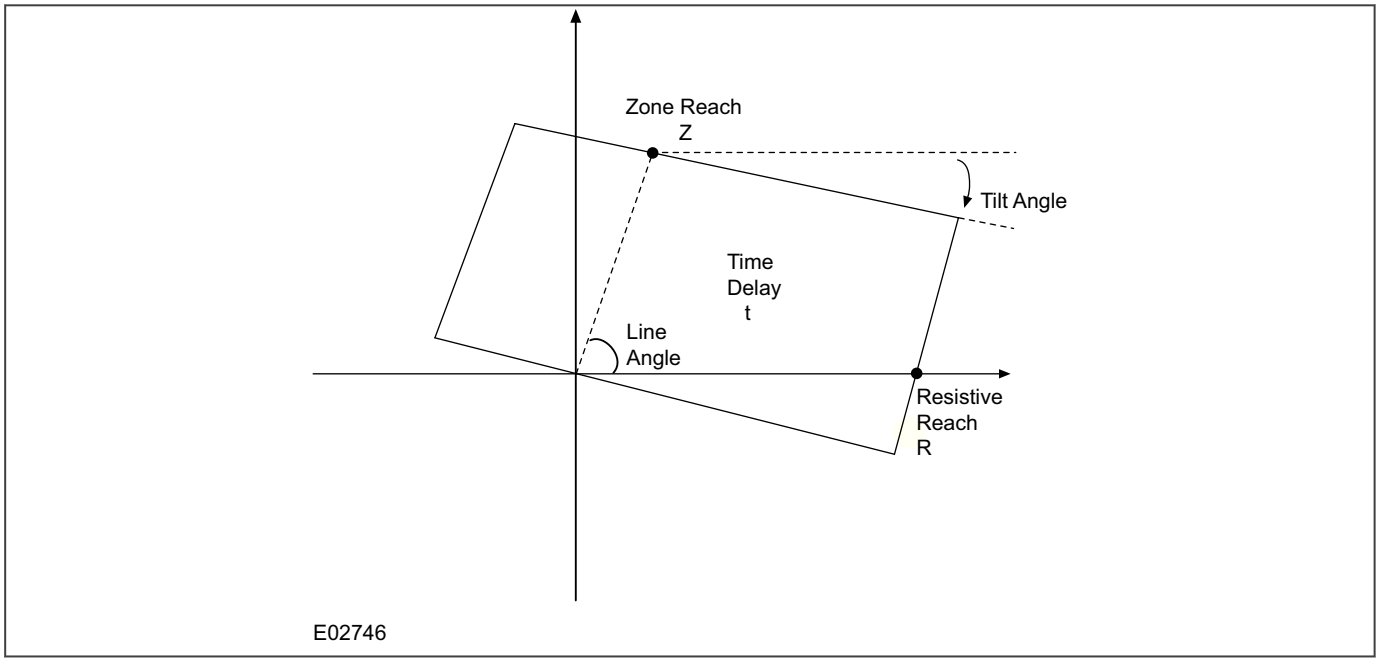



**Figure 84: Settings required to apply a quadrilateral zone**

The following figure shows the basic settings needed to configure a forward-looking mho zone, assuming that the load blinder is enabled.

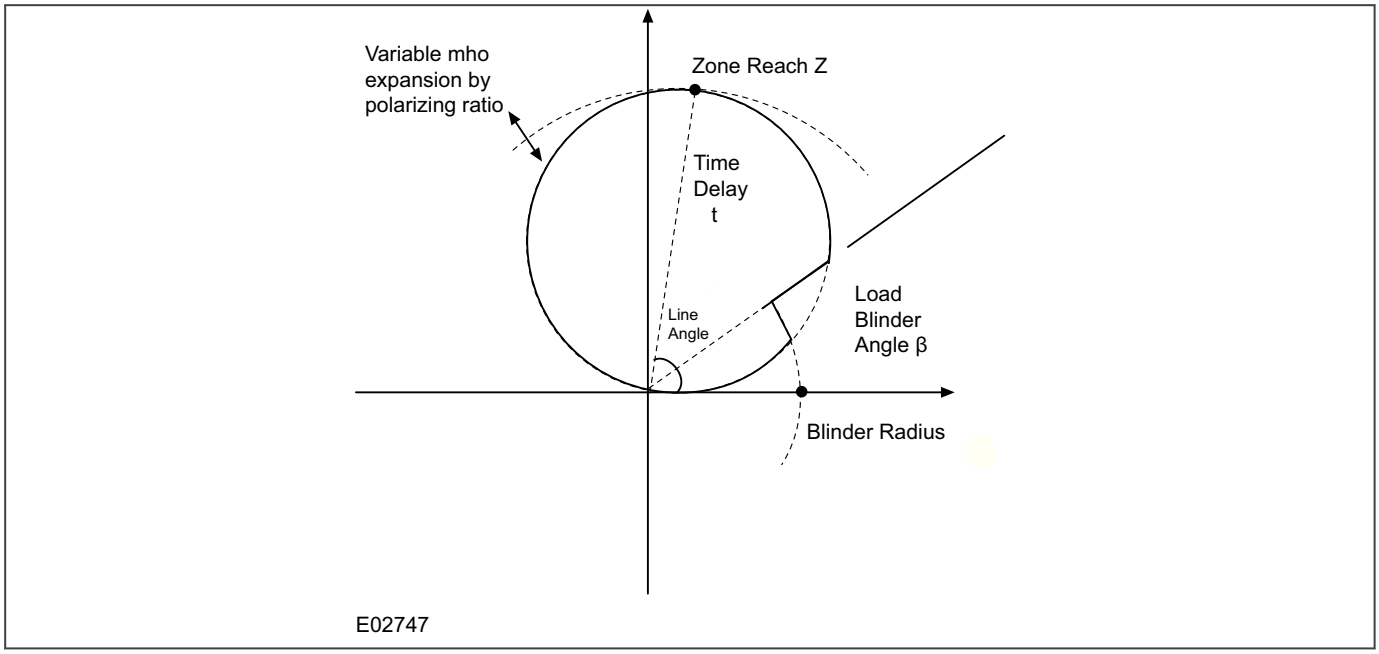



**Figure 85: Settings required to apply a mho zone**

### 6.6.2.2 EARTH FAULT CHARACTERISTIC

The earth fault characteristic selection is common to all zones, allowing Mho or quadrilateral selection. Generally, the characteristic chosen matches utility practice. Generally we would recommend a Mho characteristic for line protection and a quadrilateral characteristic for cable applications.

Quadrilateral earth-fault characteristics are also recommended for all lines shorter than 10miles (16km). This ensures that the resistive fault arc coverage does not depend on Mho circle dynamic expansion and is a known set value.

## 6.6.3 ZONE REACH SETTING GUIDELINES

The Zone 1 elements of a Distance protection should be set to cover as much of the protected line as possible, allowing instantaneous tripping for as many faults as possible. In most applications the Zone 1 reach (Z1) should not be able to respond to faults beyond the protected line. For an underreaching application the Zone 1 reach must therefore be set to account for any possible overreaching errors. These errors come from measuring errors, the current and voltage transformers, and inaccurate line impedance data. We therefore recommend that the reach of the Zone 1 distance elements is restricted to 80% of the protected line impedance (positive phase sequence line impedance), with Zone 2 elements set to cover the final 20% of the line.

The Zone 2 elements should be set to cover the 20% of the line not covered by Zone 1. Allowing for underreaching errors, the Zone 2 reach (Z2) should be set in excess of 120% of the protected line impedance for all fault conditions. Where aided tripping schemes are used, fast operation of the Zone 2 elements is required. It is therefore beneficial to set Zone 2 to reach as far as possible, such that faults on the protected line are well within reach. A constraining requirement is that, where possible, Zone 2 does not reach beyond the Zone 1 reach of adjacent line protection. For this reason the Zone 2 reach should be set to cover up to 50% of the shortest adjacent line impedance, if possible.

The Zone 3 elements would usually be used to provide overall back-up protection for adjacent circuits. The Zone 3 reach (Z3) is therefore set to approximately 120% of the combined impedance of the protected line plus the longest adjacent line. A higher apparent impedance of the adjacent line may need to be allowed where fault current can be fed from multiple sources or flow through parallel paths.

Zone 3 may also be programmed with a slight reverse (“rev”) offset, in which case its reach in the reverse direction is set as a percentage of the protected line impedance too. This would typically provide back-up protection for the local busbar, where the offset reach is set to 20% for short lines (<30km) or 10% for longer lines.

Zone 3 may also be set as a reverse directional zone. The setting chosen for Zone 3, if used, depends on its application. Typical applications include its use as an additional time delayed zone or as a reverse back-up protection zone for busbars and transformers.

Programmable zone elements can be set with the same options as Zone 3 (Forward, Reverse or Offset). A programmable zone can be used as an additional forward protection zone if custom and practice requires using more than three forward zones of Distance protection.

The Zone 4 elements may also provide back-up protection for the local busbar. Where Zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, Zone 4 must reach further behind the protection than Zone 2 for the remote end protection. In such cases the reverse reach should be:

- Mho: Z4 > Remote Zone 2 reach x 120%
- Quadrilateral: Z4 > (Remote Zone 2 reach x 120%) minus the protected line impedance

*Note:*
*In the case of the Mho, the line impedance is not subtracted. This ensures that whatever the amount of dynamic expansion of the circle, the reverse looking zone always detects all solid and resistive faults capable of detection by Zone 2 at the remote line end.*

#### 6.6.3.1 QUADRILATERAL RESISTIVE REACHES

Two setting modes are possible for resistive reach coverage, which can be set by the ***Quad Resistance*** Setting:

`Common`: In this mode, all zones share one common fault resistive reach setting

`Proportional`: With this mode, the ratio of zone reach to resistive reach is the same for all zones. The ***Fault Resistance*** setting defines a reference fault at the remote end of the line. The resistive reach is set at the same percentage of the fault resistance as the Zone Reach setting. For example, if the Zone 1 reach is 80% of the protected line, its resistive reach is 80% of the reference fault resistance.

The `Proportional` setting is used to avoid zones being excessively broad (width of the resistive reach compared to the length of the impedance reach). In general, for easiest injection testing, the aspect ratio of any zone is best within the 1 to 15 range:

$$1/15\text{th} <= \text{Z reach} / \text{R reach setting} <= 15$$

The resistive reach settings should be selected according to utility practice. If no such guidance exists, a starting point for Zone 1 is:

- Cables: Resistive Reach = 3 x Zone 1 reach
- Overhead lines: Resistive Reach = [2.3 - 0.0045 x Line length (km)] x Zone 1 reach
- Lines longer than 400km: 0.5 x Zone 1 reach

*Note:*
*Because the fault current for an earth fault may be limited by tower footing resistance, high soil resistivity, and weak infeeding; any arcing resistance is often higher than for a corresponding phase fault at the same location. It maybe necessary to set the Rn Gnd Resistive settings to be higher than the Rn Ph Resistive setting. A setting of Rn Gnd Resistive three times that of Rn Ph Resistive is not uncommon.*

### 6.6.4 EARTH FAULT RESISTIVE REACHES AND TILTING

The protection allows two different methods of tilting the Impedance Reach line.

- Automatic adjustment of the top reactance line angle (dynamic tilting)
- Fixed setting of the top line that overrides dynamic tilting (fixed tilting)

### 6.6.4.1 DYNAMIC TILTING

The dynamic tilting requirements are different for long lines and short lines:

#### Long lines

In the case of medium and long line applications where quadrilateral distance earth-fault characteristics are used, ***Zn Dynamic Tilt*** should be enabled and the starting tilt angle should be -3° (as per the default settings). This tilt compensates for possible current and voltage transformer and line data errors.

For high resistive faults during power exporting, the underreaching Zone 1 is only allowed to tilt down by the angle difference between the faulted phase and negative sequence current ∠(Iph-I2) starting from the –3° set angle. This ensures stability of Zone 1 for high resistance faults beyond the Zone 1 reach even during heavy load conditions (high load angle between two voltage sources) and sufficient sensitivity for high resistance internal faults. The tilt angle for all other zones (that are by nature overreaching zones) remain at -3°.

In the case of power importing, Zone 1 remains at –3° while all other zones are allowed to tilt up by the ∠(Iph-I2) angle difference, starting from –3°. This increases the Zone 2 and Zone 4 resistive reaches and secures correct operation in permissive overreach and blocking type schemes.

#### Short lines

For very short lines, typically below 10Miles (16km), the ratio of resistive to reactance reach setting (R/X) could easily exceed 10. For such applications the geometrical shape of the quadrilateral characteristic could be such that the top reactance line is close or even crosses the resistive axis as presented in the following figure:

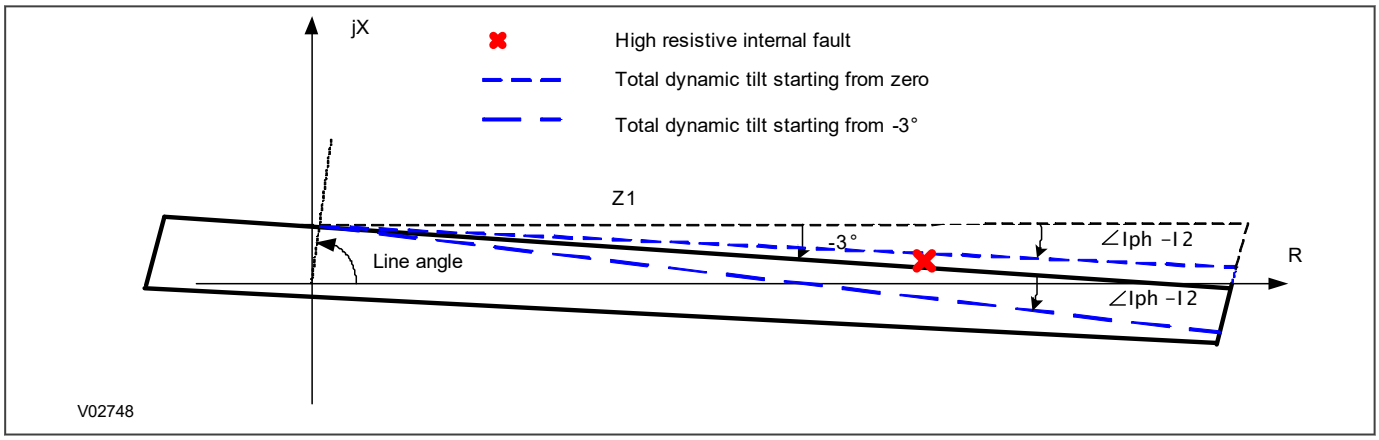



**Figure 86: Over-tilting effect**

In the case of high resistance external faults on a short line, particularly under heavy power exporting conditions, Zone 1 remains stable due to dynamic downwards tilting of the impedance reach line. However, the detection of high resistance internal faults especially towards the end of the line needs consideration. In such applications you can choose to detect high resistance faults using highly sensitive Aided Directional Earth Fault scheme, or to clear the fault with Distance ground protection. For the Distance to operate, it is necessary to eliminate over-tilting for internal faults by reducing the initial -3° tilting angle to zero so that the overall impedance reach line tilt is equal to ∠(Iph-I2) angle only.

As shown in the previous figure, the internal resistive fault then falls in the Zone 1 operating characteristic. However, for short lines the load angle is relatively low when compared to long transmission lines for the same transfer capacity and therefore the impedance reach line dynamic tilting may be moderate. Therefore it may be necessary to reduce the Zone 1 reach to guarantee Zone 1 stability. This is particularly recommended if the distance protection is operating in an aided scheme. To summarise, for very short lines with large R/X setting ratios, we recommend settiing the initial tilt angle to zero and the Zone 1 reach to 70-75% of the line impedance.

The above discussion assumes homogenous networks where the angle of the negative sequence current derived at relaying point is very close to the total fault current angle. If the network is non-homogenous, there is a difference in

angle that causes inaccurate dynamic tilting. Therefore in such networks either quadrilateral with fixed tilt angle or mho characteristic should be considered to avoid Zone 1 overreach.

*Note:*
*You can also use Delta Directional schemes to detect high resistance faults.*

#### 6.6.4.2 FIXED TILTING

As an alternative to dynamic tilting, you can set a fixed tilt angle. This is used for applications where the power flow direction is unidirectional.

##### Exporting End

To secure stability, the tilt angle of Zone 1 at the exporting end has to be set negative and above the maximum angle difference between sources feeding the resistive faults. This data should be known from load flow study, but if unavailable, the minimum recommended setting would be the angle difference between voltage and current measured at local end during the heaviest load condition coupled with reduced Zone 1 reach of 70-75% of the line impedance.

*Note:*
*With a sharp fixed tilt angle, the effective resistive coverage would be significantly reduced. Therefore for short lines, dynamic tilting (with variable tilt angle depending on fault resistance and location) is preferred. For all other overreaching zones, set the tilting angle to zero.*

##### Importing End

Set zone 1 tilt angle to zero and for all other zones the typical setting should be positive and between +5° and +10°.

*Note:*
*The setting accuracy for overreaching zones is not crucial because it does not pose a risk for distance maloperation. The purpose is to boost Zone 2 and Zone 4 reach and improve the performance of Aided Schemes.*

### 6.6.5 PHASE FAULT ZONE SETTINGS

If you use the `Advanced` ***Setting Mode***, in addition to the reach and compensation settings, you have additional settings to enter.

Each zone has a minimum current sensitivity setting (***Zn Sensit. Iph>***) which sets the minimum current that must be flowing in each of the faulted phases before a trip can occur. It is recommended to leave these settings at their default. An exception is where the protection is made less sensitive to match with other protection existing on the power system, or to grade with the pickup setting of any ground overcurrent protection for tee-off circuits.

When quadrilateral characteristics are used, the tilt angles of the impedance reach lines can be set.

By factory default, the impedance reach lines of the quadrilateral characteristics are not fixed as horizontal reactance lines. To account for phase angle tolerances in the line transformers, etc., the lines are tilted downwards at a droop of -3°. This tilt down helps to prevent Zone 1 overreach.

The fixed tilt setting on the phase elements may also be used to compensate for overreach effects when pre-fault heavy load export is flowing. In such cases, fault arc resistance is phase shifted on the impedance polar plot, tilting down towards the resistive axis and not appearing to be fully resistive in nature. For long lines with heavy power flow, the zone 1 top line might be tilted downwards in the range –5° to –15°, mimicking the phase shift of the resistance.

*Note:*
*A negative angle is used to set a downwards tilt gradient, and a positive angle to tilt upwards.*

*Note:*
*Mho characteristics have an inherent tendency to avoid unwanted overreaching, making them very desirable for long line protection.*

## 6.6.6 DIRECTIONAL ELEMENT FOR DISTANCE PROTECTION

Distance zones are directionalized by the Delta decision. For Delta directional decisions, the relay characteristic angle (RCA) settings must be based on the average source + line impedance angle for a fault anywhere internal or external to the line. Typically, the ***Dir Char Angle*** is set to 60°, as it is not essential for this setting to be precise. When a fault occurs, the delta current is never close to the characteristic boundary, so an approximate setting is good enough.

The 60° angle is associated with mainly inductive sources and suits most applications. However, in series compensated line applications where the capacitor is physically located behind the line voltage transformer, the Delta directional characteristic angle needs adjusting. In such applications the capacitor is included in the equivalent source impedance. Then the overall source impedance seen by the protection becomes predominantly capacitive if the inductance of the normally strong source is less than the capacitor value. In this case, the calculated operating angle during an internal fault may not fall within the default 60° Delta directional line operating boundary. This could lead to an incorrect (reverse) directional decision. A zero degree shift is most suitable for such a fault. However, the constraining factor is the case of external faults for which the source is always inductive regardless of the degree of compensation and for which the 60° shift is most appropriate. To ensure correct, reliable and fast operation for both fault locations in the case of predominantly capacitive source, we recommend a ***Dir Char Angle*** setting of 30°.

If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Disabled`, we recommend a setting of `1` (100%). With this setting, a mix of self-polarization and memory-polarization adequate for most applications is applied.

## 6.6.7 DELTA DIRECTIONAL ELEMENT SETTING GUIDELINES

For the Delta directional element, the relay characteristic angle (RCA) settings must be based on the average source + line impedance angle for a fault anywhere internal or external to the line. Typically, the ***Dir Char Angle*** is set to 60°, as it is not essential for this setting to be precise. When a fault occurs, the delta current will never be close to the characteristic boundary, so an approximate setting can be applied.

### 6.6.7.1 DELTA THRESHOLDS

For best performance, set the ***Dir. I Fwd*** current threshold at 10 to 20% In. This ensures detection of all fault types if the fault current contribution to an earth fault at the remote end of the line generates at least this amount of delta. To select the correct Delta V Forward setting, refer to the following table which compares SIR (Source to Line impedance ratio) with recommended Delta V Forward setting (ΔV Fwd).

| Lowest SIR Ratio of the System | Recommended ΔV Fwd (as a % of Vn) |
|---|---|
| >= 0.3 | 4% |
| >= 0.5 | 6% |
| >= 1 | 9% |
| >= 2 | 13% |
| >= 3 | 15% |
| >= 5 | 17% |
| >= 10 | 19% |

| Lowest SIR Ratio of the System | Recommended ΔV Fwd (as a % of Vn) |
|---|---|
| 25 – 60 | 21% |

The reverse fault detectors must be set more sensitively, as they are used to invoke the blocking and current reversal guard elements. We suggest that all reverse detectors are set at 66 to 80% of the setting of the forward detector, typically:

- ***Dir. V Rev*** = ***Dir. V Fwd*** x 0.66
- ***Dir. I Rev*** = ***Dir. I Fwd*** x 0.66

Due to the implementation method, Deltas are present only for 2 cycles on fault inception. If any distance elements are enabled, these will automatically allow the delta forward or reverse decisions to seal-in, until such time as the fault is cleared from the system. Therefore as a minimum, some distance zone(s) must be enabled in the DISTANCE SETUP column as fault detectors. It does not matter what time delay is applied for the zone(s). This can either be the typical distance delay for that zone or set to 'Disabled' in the SCHEME LOGIC column, if no distance tripping is required. As a minimum, Zone 3 must be enabled, with a reverse reach such as to allow seal-in of Dir. Rev, and a forward reach to allow seal-in of Dir. Fwd.

The applicable reaches would be:

- Zone 3 Forward: Set at least as long as a conventional Zone 2 (120-150% of the protected line)
- Zone 3 Reverse: Set at least as long as a conventional Zone 4, or supplement by assigning Zone 4 if a large reverse reach is not preferred for Zone 3.

We generally advise a Mho characteristic in such starter applications, although quadrilaterals are acceptable. As the Mho starter is likely to have a large radius, we strongly advise applying the Load Blinder.

## 6.6.8 FILTERING SETUP

A number of filters and features are provided to help avoid false tripping during conditions that can be challenging to distance protection.

### 6.6.8.1 DISTANCE DIGITAL FILTER

In most applications, we recommend setting the ***Digital Filter*** setting to `Standard`. This ensures that the protection provides fast, sub-cycle tripping. In certain rare cases, such as where lines are immediately adjacent to High Voltage DC (HVDC) transmission, the current and voltage inputs may be severely distorted under fault conditions. The resulting non-fundamental harmonics could affect the reach point accuracy of the protection. To prevent the protection being affected, you should select the `Special Applics` setting to enable the special applications filter.

*Note:*
*When using the Special Applications filter the instantaneous operating time is increased by about a quarter of a power frequency cycle.*

### 6.6.8.2 SETTING UP CVTS

#### CVTs with Passive Suppression of Ferroresonance

Set ***CVT Filters*** to `Passive` for any type 2 CVT (those with an anti-resonance design). You need to apply an SIR cut-off setting, above which the protection operation is deliberately slowed by a quarter of a cycle. A typical SIR setting is 30, below which the protection trips sub-cycle, and if the infeed is weak the CVT filter adapts to slow the protection and prevent transient overreach.

#### CVTs with Active Suppression of Ferroresonance

Set ***CVT Filters*** to `Active` for any type 1 CVT.

## 6.6.9 LOAD BLINDING SETUP

We strongly recommend enabling the load blinder, especially for lines above 150km (90miles) and for any networks where power swings might be experienced. This will prevent non-harmonic low-frequency transients causing load encroachment problems.

The impedance radius must be set lower than the worst-case loading, and this is often taken as 120% overloading in one line, multiplied by two to account for increased loading during outages or fault clearance in an adjacent parallel circuit. Then an additional allowance for measuring tolerances results in a recommended setting typically between a quarter and one third of the rated full load current:

$$Z <= (\text{Rated phase voltage } Vn)/(I_{FLC} \times 3)$$

When the load is at the worst-case power factor, it should remain below the beta (β) setting. So, if we assume a typical worst case 0.85 power factor, then:

$$\beta >= \text{Cos}^{-1}(0.85) + 15° \text{ margin} >= 47°$$

and to ensure that line faults are detected:

$$\beta <= (\text{Line Angle} - 15°).$$

In practice, an angle half way between the worst-case leading load angle, and the protected line impedance angle, is often used.

This product has a facility to allow the load blinder to be bypassed any time that the measured voltage for the phase in question falls below an undervoltage (***Load Blinder V<***) setting. Under such circumstances, the low voltage would not be explained by normal voltage excursion tolerances on-load. A fault must be present on the phase in question, and it is acceptable to override the blinder action and allow the distance zones to trip according to the entire zone shape. The benefit is that the resistive coverage for faults near to the protection location can be higher.

The undervoltage setting must be lower than the lowest phase-neutral voltage under heavy load flow and depressed system voltage conditions. The recommended ***Load Blinder V<*** setting is 70% Vn.

## 6.6.10 POLARIZING SETUP

You can choose how much memory polarization to mix with self-polarization using the ***Dist. Polarizing*** setting. Some recommendations are:

### Cable applications

Use 20% (0.2) memory. This results in minimum Mho expansion and keeps the protected line section well within the expanded Mho, thereby ensuring better accuracies and faster operating times for close-up faults. This matches the guidance previously provided for LFZP123 or LFZR applications for cable feeders

### Series compensated lines

Use a mho with the maximum memory polarization (setting = 5). The large memory content ensures correct operation even with the negative reactance effects of the compensation capacitors seen either within the zones, or within the line impedance.

### Short lines

For lines shorter than 10miles (16km), or with an SIR higher than 15, use the maximum memory polarization (setting = 5). This ensures sufficient characteristic expansion to cover fault arc resistance.

### General line applications

Use any setting between 0.2 and 1.

## 6.6.11 DISTANCE PROTECTION WORKED EXAMPLE

This section presents a worked example of how to set the Distance protection. For this case study, we assume that Zone 1 Extension is not used, and that only three zones are required for basic Distance protection (Zones 1 and 2 Forward Directional, and Zone 3 Forward Offset). The following settings are derived:

- Line Impedance
- Residual Compensation
- Zone 1 reach settings for phase-faults and earth-faults
- Zone 2 reach settings for phase-faults and earth-faults
- Zone 3 reach settings for phase-faults and earth-faults
- Zone 3 reverse reach settings
- Zone 4 reach settings (for use with Permissive Overreach or Blocking schemes if needed)
- Load avoidance

The settings are applicable whether the Distance protection characteristics are set to Mho, or Quadrilateral. If you choose Quadrilateral however, you will need to consider the Resistive reaches of Quadrilaterals.

For this study, we wish to protect one line of a double 230kV, 100km line between a substation at Green Valley and a substation at Blue river. There are generating sources at Tiger Bay, 80 km from Green Valley and at Rocky Bay, 60 km from Blue River.

The single-line diagram for the system is shown in the following figure:

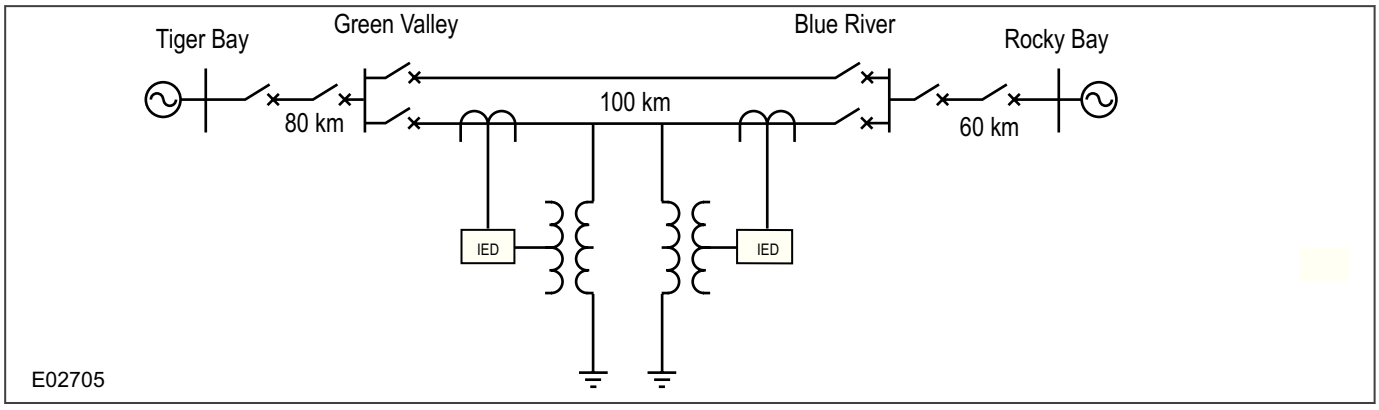



**Figure 87: Example power system**

The system data is as follows:

- System Voltage: 230kV
- System earthing: Solid
- CT ratio: 1200 : 5
- VT ratio: 230 000 : 115
- Line length: 100km
- Positive sequence line impedance (Z1): 0.089 + j0.476 ohms/km = 0.484∠79.4°
- Zero sequence line impedance (Z0): 0.426 + j1.576 ohms/km = 1.632∠74.8°
- Z0/Z1: 3.372∠–4.6°
- Green Valley substation fault level: 2000 MVA to 5000 MVA
- Blue river substation fault level: 1000 MVA to 3000 MVA
- Circuit continuous rating: 400 MVA
- Worst case power factor of load: 0.85

### 6.6.11.1 LINE IMPEDANCE CALCULATION

Ratio of secondary to primary impedance = (1200/5)/(230000/115) = 0.12

Total primary line impedance (for 100 km length) = 100 x 0.484∠79.4° Ω

Total secondary impedance = (0.12 x 100 x 0.484)∠79.4° = 5.81∠79.4° Ω

Therefore set secondary values as follows:

***Line Angle*** = 80°

***Line Impedance*** = 5.81 Ω

### 6.6.11.2 RESIDUAL COMPENSATION FOR EARTH FAULT ELEMENTS

The residual compensation factor can be applied independently to certain zones if required. This is a useful feature where line impedance characteristics change between sections or where hybrid circuits are used. In this example this is not the case, so a common kZN factor can be applied to each zone. This is set as ratio ***kZN Res Comp***, and angle ***KZN Res Angle***:

We know that

$$k_{ZN} = (Z_0 - Z_1)/3Z_1$$

Now, performing the calculations iwht the given values ...

$$|Z_0 - Z_1| = 1.15$$

$$|3Z_1| = 1.452$$

$$\angle(Z_0-Z_1) = 72.9°$$

$$\angle 3Z_1 = 79.4°$$

Thus ...

$$kZ_N = 0.79 \angle -6.5°$$

Therefore set:

***kZN Res Comp*** = 0.79

***KZN Res Angle*** = -6.5°

### 6.6.11.3 ZONE 1 PHASE AND GROUND REACH SETTINGS

For the protection at Green Valley:

The required Zone 1 reach is to be 80% of the line impedance between Green Valley and Blue River substations.

Using the ***Setting Mode*** `Simple`:

- Set ***Zone 1 Ph Status*** and ***Zone 1 Gnd Stat.*** to `Enabled`
- Set ***Zone 1 Ph Reach*** and ***Zone 1 Gnd Reach*** to 80%

From this the protection algorithm automatically calculates the required Ohmic reaches.

Alternatively, using the ***Setting Mode*** `Advanced`, the values can be calculated and entered manually as follows:

Required Zone 1 reach = 0.8 x 100 x 0.484∠79.4° x 0.12 = 4.64∠79.4° Ω secondary

So:

- Set ***Z1 Ph. Reach*** and ***Z1 Gnd. Reach*** = 4.64 Ω
- Set ***Z1 Ph. Angle*** and ***Z1 Gnd. Angle*** = 80°

### 6.6.11.4 ZONE 2 PHASE AND GROUND REACH SETTINGS

For the protection at Green Valley:

In *Advanced* mode:

Required Zone 2 impedance = line impedance of Green Valley to Blue River + 50% line impedance from Blue River to Rocky Bay

= (100+30) x 0.484∠79.4° x 0.12

= 7.56 ∠79.4° Ω secondary

So:

- Set ***Z2 Ph. Reach*** and ***Z2 Gnd. Reach*** = 7.56 Ω
- Set ***Z2 Ph. Angle*** and ***Z2 Gnd. Angle*** = 80°

Alternatively, in *Simple* setting mode, this reach can be set as a percentage of the protected line. Typically a figure of at least 120% of the line between Green Valley and Blue River is used.

### 6.6.11.5 ZONE 3 PHASE AND GROUND REACH SETTINGS

For the protection at Green Valley:

In *Advanced* mode:

Required Zone 3 impedance = 1.2(line impedance of Green Valley to Blue River) + line impedance from Blue River to Rocky Bay

= 1.2*(100+60) x 0.484∠79.4° x 0.12

= 11.15 ∠79.4° Ω secondary

So:

- Set ***Z3 Ph. Reach*** and ***Z2 Gnd. Reach*** = 11.15 Ω
- Set ***Z2 Ph. Angle*** and ***Z2 Gnd. Angle*** = 80°

Alternatively, in *Simple* setting mode, this reach can be set as a percentage of the protected line.

### 6.6.11.6 ZONE 3 REVERSE REACH SETTINGS

For the protection at Green Valley:

In the absence of special requirements, because the protected line length is more than 30km, Zone 3 can be given a small reverse reach – say 10%.

Using *Advanced* mode, in the *DISTANCE SETUP* column, set:

- ***Z3' Ph Rev Reach*** and ***Z3' Gnd Rev Rch*** = 0.1*5.81 = 0.58 Ω

### 6.6.11.7 ZONE 4 REVERSE REACH SETTINGS

For the protection at Green Valley:

Where Zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, Zone 4 must reach further behind the local protection than Zone 2 of the remote protection. This can be achieved by setting Zone 4 ≥ 1.2 x Remote Zone 2 reach, where mho characteristics are used.

Remote Zone 2 Reach = line impedance of Green Valley to Blue River + 50% line impedance from Green valley to Tiger Bay

= (100 + 40) x 0.484∠79.4° x 0.12

$= 8.13\angle 79.4° \Omega$ secondary

Zone 4 Reach $\geq (8.13\angle 79.4° \times 120\%) - 5.81\angle 79.4°$

$= 3.95\angle 79.4° \Omega$ secondary

This is the minimum Zone 4 Reach setting, so:

- ***Set Z4 Ph. Reach*** and ***Z4 Gnd. Reach*** = 3.96 Ω
- ***Set Z4 Ph. Angle*** and ***Z4 Gnd. Angle*** = 80°

### 6.6.11.8 LOAD AVOIDANCE

The maximum full load current of the line can be determined from the calculation:

$$I_{FLC} = [(\text{Rated MVAFLC}) / (\sqrt{3} \times \text{Line kV})]$$

The settings must allow for a level of overloading, typically a maximum current of 120% $I_{FLC}$ prevailing on the system transmission lines. Also, for a double circuit line, during the auto-reclose dead time of fault clearance on the adjacent circuit, twice this level of current may flow on the healthy line for a short period of time. Therefore the circuit current loading could be 2.4 x $I_{FLC}$.

With such a heavy load flow, the system voltage may be depressed, typically with phase voltages down to 90% of Vn nominal.

Allowing for a tolerance in the measuring circuit inputs (line CT error, VT error, protection accuracy, and safety margin), this results in a load impedance which might be 3 times the expected rating.

To avoid the load, the blinder impedance needs to be set:

$$Z \leq (\text{Rated phase-ground voltage Vn}) / (I_{FLC} \times 3)$$

$$= (115/\sqrt{3}) / (I_{FLC} \times 3)$$

Set the V< Blinder voltage threshold at the recommended 70% of Vn = 66.4 x 0.7 = 45 V.

### 6.6.11.9 QUADRILATERAL RESISTIVE REACH SETTINGS

If applying Quadrilateral characteristics, as well as the Impedance Reaches, the Resistive Reaches also need to be considered. The Resistive reaches of the phase-fault elements must be set to cover the maximum expected phase-to-phase fault resistance. The Resistive reaches of the earth-fault elements should take into account the arc-resistance and the tower footing resistance.

#### Phase-Fault Elements

Ideally, the Resistive reach should be set greater than the maximum fault arc resistance for a phase-phase fault (Ra), calculated in terms of the minimum expected phase-phase fault current, the maximum phase conductor separation, according to the formula developed by (van) Warrington as:

$$Ra = (28710 \times L)/If \times 1.4$$

where:

- If = Minimum expected phase-phase fault current (A)
- L = Maximum phase conductor separation (m)

Typical figures for Ra are given, for different values of minimum expected phase fault currents, in the following table:

| Conductor Spacing (m) | Typical System Voltage (KV) | RA FOR IF = 1 KA | RA FOR IF = 2 KA | Ra for If = 3 kA |
|---|---|---|---|---|
| 4 | 110 - 132 | 7.2 Ω (primary) | 2.8 Ω (primary) | 1.6 Ω (primary) |

| Conductor Spacing (m) | Typical System Voltage (KV) | RA FOR IF = 1 KA | RA FOR IF = 2 KA | Ra for If = 3 kA |
|---|---|---|---|---|
| 8 | 220 - 275 | 14.5 Ω (primary) | 5.5 Ω (primary) | 3.1 Ω (primary) |
| 11 | 380 - 400 | 19.9 Ω (primary) | 7.6 Ω (primary) | 4.3 Ω (primary) |

*Note:*
*For circuits with infeed from more than one terminal, the fault resistance will appear greater. This is because the protection cannot measure the current contribution from a remote terminal. The apparent fault resistance increase could be between 2 to 8 times the calculated resistance. For this reason, we recommended setting the zone Resistive reaches to 4 times the calculated arc resistance.*

In this example, the minimum phase fault level is 1000 MVA. This is equivalent to an effective short-circuit fault feeding impedance of:

$$Z = kV^2/MVA = 230^2/1000 = 53\ \Omega \text{ (primary)}$$

The lowest phase fault current level is equivalent to:

$$Ifault = (MVA \times 1000)/(\sqrt{3} \times kV)$$

$$= (1000 \times 1000)/(\sqrt{3} \times 230)$$

$$= 2.5\ kA$$

Giving, according to the (van) Warrington formula, an arc resistance of:

$$Ra = 4\ \Omega$$

Iterative calculations could be performed to refine the expected fault current (which decreases as refined values of Ra are included in the calculation), but as Ra is relatively small compared to the initially calculated value of Z, this value is acceptable.

To compensate for remote infeed a small additional factor can be added to account for the expected fault current being lower than that used in the calculation. So rather than set the zone Resistive reaches to 4 times the calculated arc resistance, a factor of 5 could be used.

Using a factor of 5 gives a minimum setting of:

$$\text{Phase Resistive Reach} = 5 \times Ra = 20\ \Omega \text{ (primary value)}$$

The Phase Resistive Reach could be set higher than this (for example using the rule-of-thumb: [2.3 - 0.0045 x Line length (km)] x Zone 1 reach), so typically it would be set higher than 20Ω but lower than the Load Avoidance setting.

### Earth-Fault Elements

Fault resistance would comprise arc-resistance and tower footing resistance. A typical resistive reach coverage setting would be 40 Ω (primary).

For high resistance earth faults, the situation could arise where no distance elements would operate. In such cases, supplementary earth fault protection (for example Aided DEF protection) should be applied. If supplementary earth fault protection is used, large resistive reaches for Earth-Fault Distance protection do not need to be used so that the Earth-Fault Resistive reach can be set according to the utility practice. In the absence of specific guidance, a recommendation for setting Zone 1 is:

- Cables: Resistive Reach = 3 x Zone 1 reach
- Overhead lines: Choose Resistive Reach in the range [2.3 - 0.0045] x Line length(km) x Zone 1 Reach
- Lines longer than 400 km: Choose Resistive Reach = 0.5 x Zone 1 Reach

## 6.6.12 TEED FEEDER APPLICATIONS

Distance protection can be applied to protect three terminal lines (teed feeders). Interconnecting three terminals, however, affects the apparent impedances seen by the distance elements and creates certain problems.

Consider, as an example, the following figure which represents a teed feeder with terminals A, B, and C, with a fault applied near to terminal B:

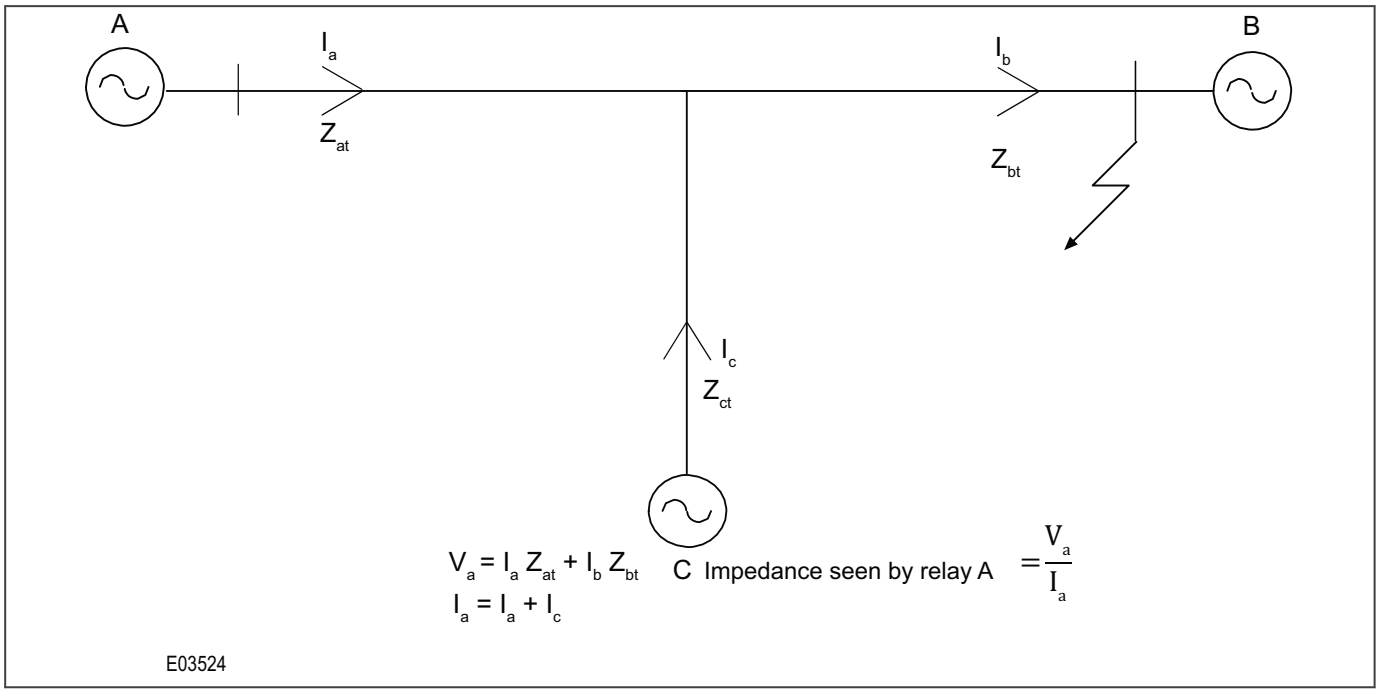



**Figure 88: Apparent Impedances seen by Distance Protection on a Teed Feeder**

The impedance seen by the distance elements at terminal A is given by:

$$Za = Zat + Zbt + [Zbt.(Ic/Ia)]$$

For faults beyond the Tee point, with infeed from terminals A and C, the distance elements at A (and C) will underreach. If terminal C is a relatively strong source, the underreaching effect at A can be substantial. If Zone 2 was set to a typical value of 120% of line AB, the element may fail to operate for internal faults. To compensate, the Zone 2 element must be set to further overreach by a factor which takes into account the effect of the infeed from the tee-point.

So, if infeed is present on a teed circuit, all Zone 2 elements should be set to overreach both of their remote terminals by a factor which takes into account the effect of the infeed from the tee-point.

Like overreaching of Zone 2 elements, underreaching of Zone 1 elements must also be assured. Zone 1 elements at each terminal must be set to underreach the true impedance to their nearest terminal (limiting case = no infeed to the tee-point - hence no overreach contribution).

Changing the reach requirements to match the infeed expectations is possible using the alternative setting group feature. Tailoring setting group contents to the different conditions, coupled with appropriate setting group switching, enables the changing reach requirements to be met.

Carrier aided schemes can also be used in conjunction with distance elements to protect teed feeders. Although Permissive Overreaching and Permissive Underreaching schemes may be used, they suffer some limitations. Blocking schemes are generally considered to be the most suitable.

For a full explanation of Teed Feeders applications in carrier aided schemes, please refer to the Carrier Aided Schemes chapter.

# CHAPTER 7

# CARRIER AIDED SCHEMES

# 7.1 CHAPTER OVERVIEW

This chapter contains the following sections:

Chapter Overview 170
Introduction 171
Aided Distance Scheme Logic 172
Aided DEF Scheme Logic 186
Aided Delta Scheme Logic 197
Application Notes 204

## 7.2 INTRODUCTION

The provision of communication channels between the terminals of a protected transmission line or distribution feeder enables unit protection to be applied.

Protection devices located at different terminals can be configured to communicate with one another in order to implement unit protection schemes. The exchange of simple ON/OFF command signals allows unit protection to be achieved with Distance Protection schemes (Aided Distance), Directional Earth Fault schemes (Aided DEF) and if applicable, Delta Directional Comparison Protection schemes (Aided Delta). Schemes where a communication channel is used to send command signals between line ends are known as Carrier Aided Schemes.

The terms ‘simplex’ and ‘duplex’ are used to describe the type of communication channel used. Simplex communication, also sometimes referred to as half-duplex, requires only a single communication channel between line ends. Signals can be sent in both directions but not at the same time. Duplex communication requires two communication channels between line ends (one in each direction). Duplex communication allows signals to be sent and received at the same time.

## 7.3 AIDED DISTANCE SCHEME LOGIC

When the Carrier Aided schemes are used in conjunction with the Distance protection, you can choose whether to use them with the phase distance elements only, the earth-fault (ground) distance elements only, or for both phase and earth fault elements.

**Caution:**
**Zone 1,2 and 4 are required to implement the *PUR*/*POR* and Blocking Aided Schemes. In this case, zone 1 and zone 2 should be forward and zone 4 should be reverse. Therefore, if the relay's *Setting Mode* is set to *Advanced* and any Zone direction has been selected that compromises the Aided Schemes, then the Aided Distance Schemes should be forced to be disabled by the user.**

### 7.3.1 PERMISSIVE UNDERREACH SCHEME

The simplest Carrier Aided scheme mode for use with distance-type applications is the Permissive Under-reach Protection scheme, variously referred to as PUR, PUP, and PUTT. We normally use the term PUR.

To use this scheme, you need to set the relevant setting (***Aid. 1 Selection*** or ***Aid. 2 Selection***) in the *SCHEME LOGIC* column to *PUR*.

The channel for a PUR scheme is keyed (that means that the aiding signal is asserted) if an under-reaching Zone 1 element operates. If the remote device detects a forward fault and this signal is received, then the remote protection operates without further delay. Faults in the last 20% of the protected line are therefore cleared with minimal time delay.

*Note:*
*This assumes a 20% typical end-zone when Zone 1 is set to 80% of the protected line.*

The following are some of the main features and requirements for a permissive under-reaching scheme.

- Only a simplex channel is required.
- Scheme security is high, because the signalling channel is only keyed for faults in the protected line.
- If the circuit breaker at the remote terminal is open, faults in the remote 20% of the line are cleared using the Zone 2 time delay of the local protection.
- If there is a weak-infeed, or zero-infeed from the remote terminal, (current below the protection sensitivity), faults in the remote 20% of the line are cleared using the Zone 2 time delay of the local protection.
- If the signalling channel fails, basic distance scheme tripping remains available.

The PUR logic is:

- Send logic: Assert signal if Zone 1 element operates
- Permissive trip logic: Trip if the Zone 2 element picks up AND the Carrier Aided signal is received

The figure below shows the simplified scheme logic:

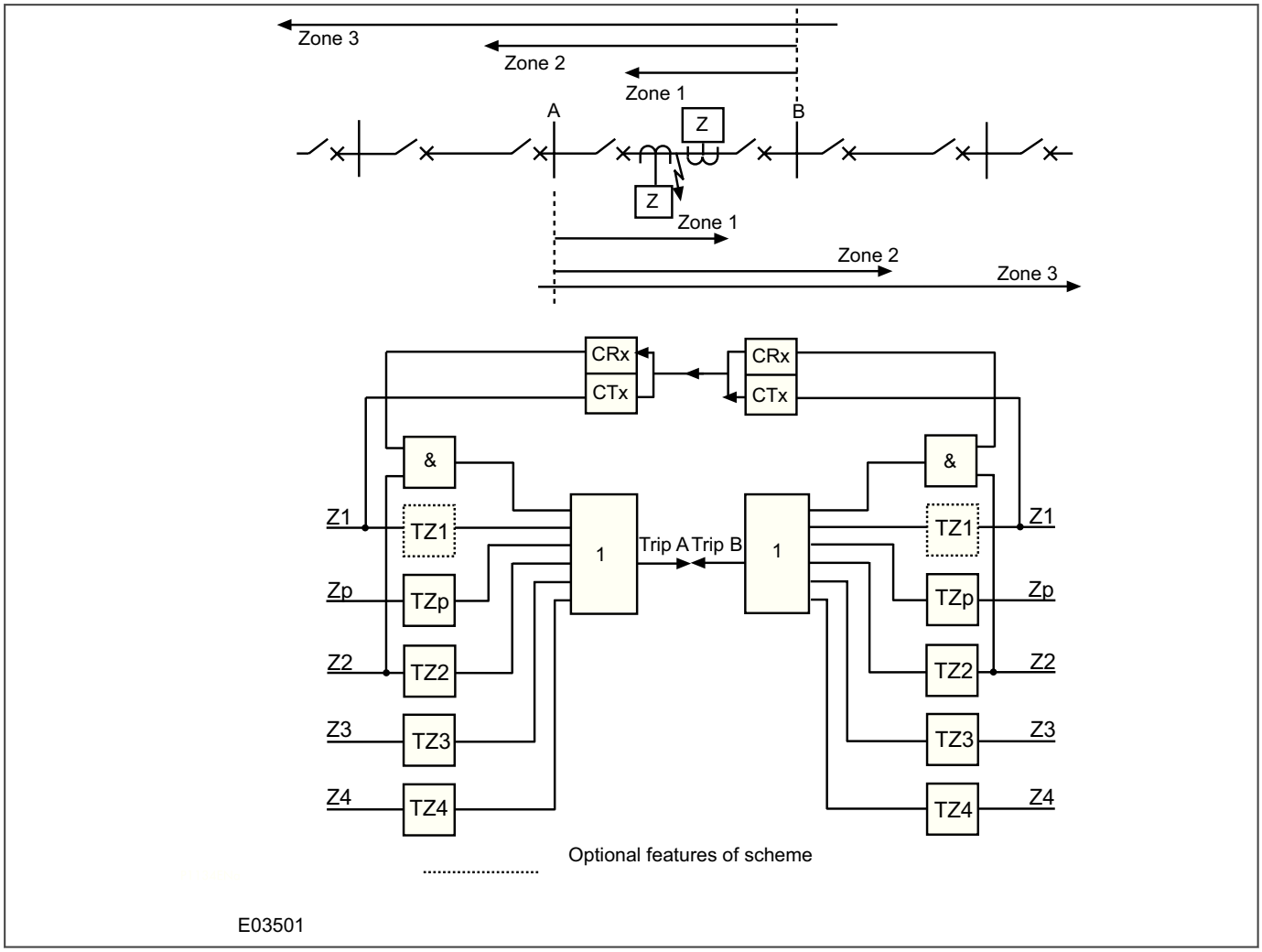



**Figure 89: Aided Distance PUR scheme**

## 7.3.2 CARRIER AIDED SCHEMES IMPLEMENTATION

With Aided Distance protection, tripping schemes are used to connect similar devices at different terminals on the protected line to provide fast clearance for faults anywhere along the line.

For distance protection It is typical to set Zone 1 distance protection elements to cover only 80% of a line from the relaying point. Faults on the other 20% of the line would generally be cleared by a delayed Zone 2 element, which could be hundreds of milliseconds after the fault inception. There is, however, a limit to the amount of arc reistance and tower footing resistance that can be adequately covered by distance IEDs, since the coverage is limited by their ohmic reach. If extremely high values of ground fault resistance are expected, then an optional directional comparison earth fault scheme (Aided DEF) can be used to complement the distance schemes.

Aided distance schemes assure fast clearance for faults on the entire circuit by communicating command signals.

For the the communication between local and remote terminals InterMiCOM 64 (IM64) can be used.

### 7.3.2.1 CARRIER AIDED SCHEME TYPES

This product has two independent Carrier Aided Schemes (Aided Scheme 1 and Aided Scheme 2). The two schemes are independent, but the design of both is the same. Each of the two Carrier Aided Schemes provides the following options:

- Permissive Underreaching Schemes (PUR, PUTT)
- Permissive Overreaching Schemes (POR, POTT)
- Blocking Scheme (Block 1)
- Blocking Scheme (Block 2)
- Unblocking POR Scheme
- Unblocking PUR Schemes
- Programmable
- Programmable Unblocking

The underreaching options can be used to implement Carrier Aided Distance schemes. The other options can be used with any Carrier Aided scheme application.

The following diagram shows how the schemes can be assigned.

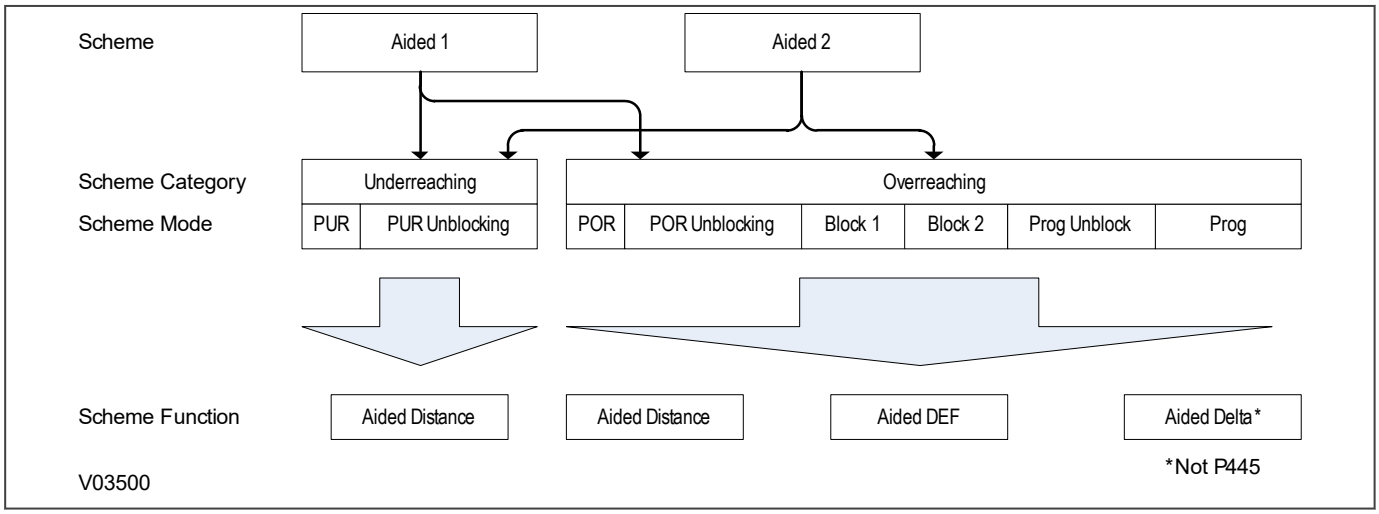



**Figure 90: Scheme Assignment**

### 7.3.2.2 DEFAULT CARRIER AIDED SCHEMES

This product provides support for two Carrier Aided schemes, which can operate in parallel. The schemes are referred to as 'Aided Scheme 1' and 'Aided Scheme 2'. The schemes have been designed to operate independently with a separate communication channel dedicated to each one, but they can share a single communication channel if necessary. If both schemes are used and they share a common channel then, if one of the schemes initiates transmission of a command signal, both schemes will receive the command and act upon it.

If you don't want to use the Aided schemes, you should set the relevant ***Aid. 1 Selection*** and ***Aid.2 Selection*** settings (in the *SCHEME LOGIC* column) to `Disabled`. If the setting(s) are enabled, you are provided with a choice of schemes; standard transfer tripping schemes, blocking schemes, or custom programmable schemes.

You select the type of scheme you want to use, and then you choose whether to use it in conjunction with the Distance protection, and/or the Aided DEF protection.

The scheme options are:

- `Disabled`: No scheme is implemented
- `PUR`: Permissive Underreach Transfer Tripping (PUPP, PUR, or PUTT) scheme

- *PUR Unblocking*: Perrmissive Underreach Unblocking scheme
- *POR*: Permissive Overreach Transfer Tripping (POP, POR, or POTT) scheme
- *POR Unblocking*: Permissive Overreach Unblocking scheme
- *Blocking1*: Current reversal guard signal is sent to qualify reverse looking Zone 4 elements
- *Blocking2*: Received current reversal guard signal qualifies reverse looking Zone 4 elements
- *Prog. Unblocking*: Allows you to define which elements are used to assert signals for Overreach Unblocking.
- *Programmable*: Allows you to define which elements are used to assert signals for Overreach Transfer Tripping, by using a custom send mask

*Note:*
*The PUR schemes are only suitable for Distance protection. Therefore, if a PUR scheme is selected, the option to allocate to other protection is not available.*

### 7.3.3 PERMISSIVE OVER-REACH SCHEME

Permissive Over-reach schemes are variously referred to as POR, POP, POTT. We normally use the term POR.

In a Permissive Overreach scheme the channel is keyed (that means that the aiding signal is asserted) by the pickup of an over-reaching Zone 2 element.

To use this scheme, you need to set the relevant setting (***Aid. 1 Selection*** or ***Aid. 2 Selection***) in the *SCHEME LOGIC* column to *POR*.

If a remote protection element detects a forward fault and receives a POR signal, the protection operates without further delay. Faults in the last 20% of the protected line are therefore cleared with minimal time delay.

*Note:*
*This assumes a 20% typical end-zone when Zone 1 is set to 80% of the protected line.*

The following are some of the main features and requirements for a POR scheme:

- The scheme requires a duplex signalling channel to prevent possible maloperation if a carrier is keyed for an external fault. Because the signalling channel can be keyed for faults external to the protected zone, it is vital that they are only received by, and acted upon by, the intended recipient. A simplex channel cannot assure this.
- A POR scheme may be more advantageous than a PUR scheme for the protection of short transmission lines. This is because the resistive coverage of the Zone 2 elements may be greater than that of the Zone 1 elements (in the case of Mho elements)
- Current reversal guard logic prevents healthy-line protection maloperation for high speed current reversals that can be experienced on double circuit line applications, which can be caused by sequential opening of circuit breakers.
- If the signalling channel fails, basic distance scheme tripping remains available.

The POR logic is:

- Send logic: Assert signal if Zone 2 element picks up.
- Permissive trip logic: Trip if the Zone 2 element operates AND the Channel Aided signal is received.

The POR scheme also uses the reverse looking zone 4 as a reverse fault detector. This is used in the current reversal logic and in the weak infeed echo feature, shown dotted in the figure below:

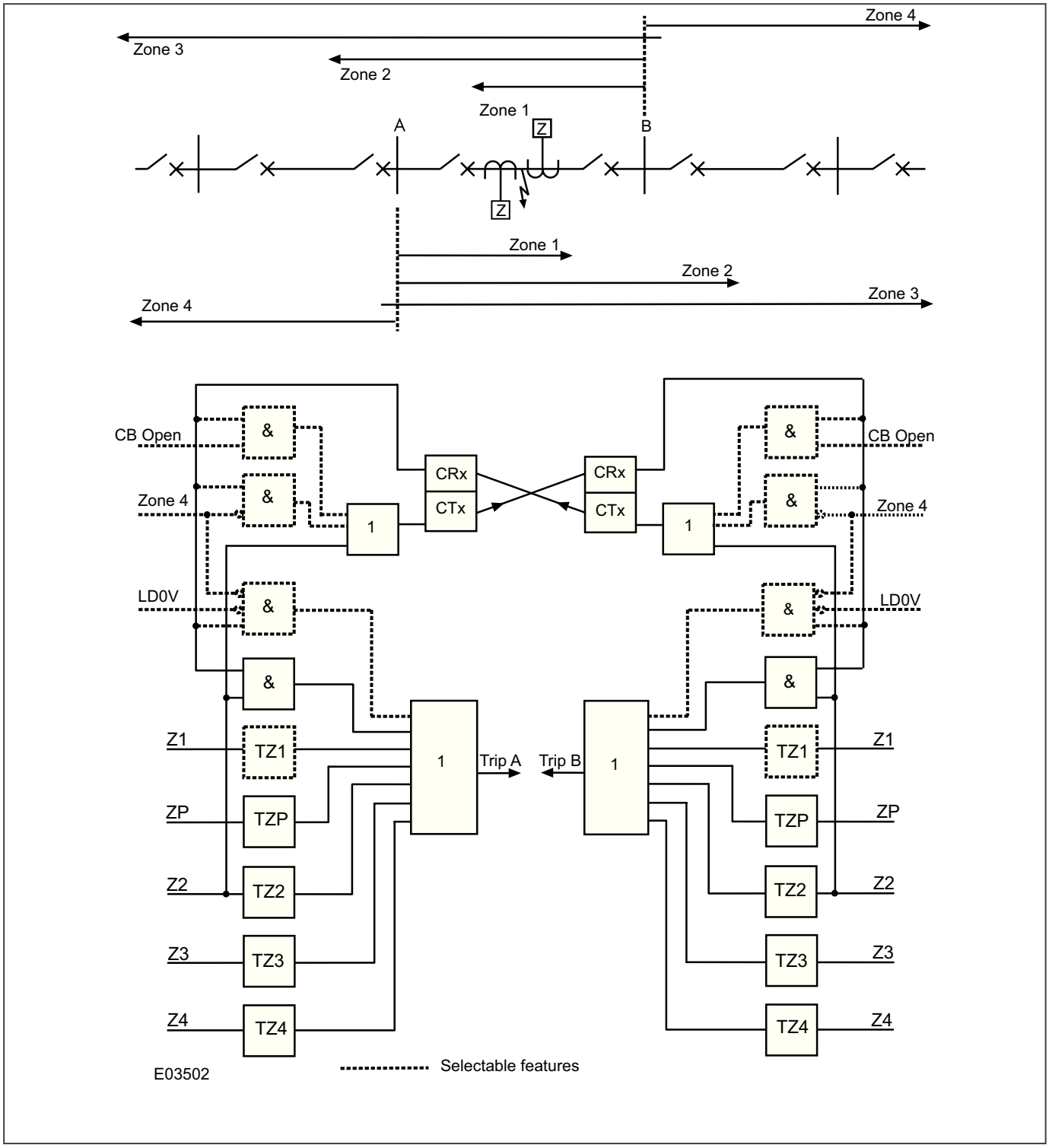



**Figure 91: Aided Distance POR scheme**

The POR scheme is enhanced by POR Trip Reinforcement, and POR Weak Infeed features.

### 7.3.3.1 PERMISSIVE OVERREACH TRIP REINFORCEMENT

The send logic in the POR scheme is arranged so that for any trip command at a local end, the local protection sends a Channel Aided signal to the remote end(s). This facilitates fault isolation at each terminal as quickly as possible. The send signal is generated by the ***Any Trip*** command, and it is sent on any channel that is being used.

This feature is called permissive trip reinforcement. It is designed to ensure that synchronous tripping occurs at all protected terminals.

#### 7.3.3.2 PERMISSIVE OVERREACH WEAK INFEED FEATURES

Special weak infeed logic (WI) can be used with the POR schemes. The ***Weak Infeed*** setting can be found in the *SCHEME LOGIC* column. ***Weak Infeed*** can be set to `Echo`, `Echo and Trip`, or `Disabled`.

##### Weak Infeed Echo

For a POR scheme, a signal is normally sent only if the appropriate signal associated with the pick up of the sending zone detects a fault. However, under some circumstances, the fault current infeed at one line end may be so low that it is insufficient to operate any of the distance zones. In another scenario, if a circuit breaker at one of the terminals is in an open state, the current infeed will be zero. These scenarios are termed Weak Infeed (WI) conditions. Without special attention they could result in slow fault clearance at the terminal that is feeding the fault current (called the 'strong infeed' terminal). This would typically result in tripping after the Zone 2 time delay (tZ2). To avoid Zone 2 delayed tripping, a device subject to Weak Infeed conditions can be set to echo signals received on the Channel Aided link back to the initiating IED without delay. This allows the devices at points of strong infeed to permissively trip instantaneously.

The Weak Infeed Echo Send logic is:

- No Distance Zone Operation has been detected, but a POR Aided signal has been received.

##### Weak Infeed Echo and Trip

The Weak infeed echo logic will produce an aided trip at a strong infeed terminal, but it does not produce a trip at the weak infeed. Setting ***Weak Infeed*** to `Echo and Trip` allows tripping of the weak infeed circuit breaker of a faulted line. Three undervoltage elements, ***Va<***, ***Vb<*** and ***Vc<*** are used to detect the line fault at the weak infeed terminal. This voltage check prevents tripping during spurious operations of the channel or during channel testing.

The Weak Infeed Echo and Trip logic is:

- No Distance Zone Operation has been detected, but a POR signal has been received, AND a V< condition exists.

Weak infeed tripping is time delayed according to the value set in the ***WI Trip Delay*** settingin the *SCHEME LOGIC* column. Due to the use of phase segregated undervoltage elements, single-phase tripping can be enabled for WI trips if required. If single-phase tripping is disabled, under Weak Infeed conditions, three-phase tripping will occur after the ***WI Trip Delay*** time has expired.

### 7.3.4 PERMISSIVE SCHEME LOSS OF GUARD

This scheme is intended for use with frequency shift keyed (FSK) power line carrier (PLC) communications.

When the protected line is healthy, a guard frequency is sent between line ends to verify the channel is in service. However, when a line fault occurs and a permissive trip signal must be sent over the line, the power line carrier frequency is shifted to a different (trip) frequency. Therefore the distance function should receive either the guard frequency or the trip frequency, but not both together. For certain fault types, the line fault can attenuate the PLC signals so the permissive signal is lost and not received at the other line end. To overcome this problem, when the guard is lost and no trip frequency is received, the protection opens a window of time during which the permissive scheme logic acts as though a trip signal had been received. Two opto-isolated inputs need to be assigned: One is for Channel Receive; The second is designated Loss of Guard (the inverse function to guard received).

The Loss of Guard logic is described in the table below:

| System Condition | Permissive Channel Received | Loss of Guard | Permissive Trip Allowed | Alarm Generated |
|---|---|---|---|---|
| Healthy Line | No | No | No | No |
| Internal Line Fault | Yes | Yes | Yes | No |

| System Condition | Permissive Channel Received | Loss of Guard | Permissive Trip Allowed | Alarm Generated |
|---|---|---|---|---|
| Unblock | No | Yes | Yes, during a 150 ms window | Yes, delayed on pickup by 150 ms |
| Signalling Anomaly | Yes | No | No | Yes, delayed on pickup by 150 ms |

The window of time during which the unblocking logic is enabled starts 10ms after the guard signal is lost, and continues for 150ms. The 10ms delay gives time for the signalling equipment to change frequency, as in normal operation. For the duration of any alarm condition, Zone 1 extension logic is invoked if the ***Z1 Ext Scheme*** setting is set to operate for channel failure.

## 7.3.5 CURRENT REVERSAL GUARD LOGIC

For double circuit lines, the fault current direction can change in one circuit when circuit breakers open sequentially to clear the fault on the parallel circuit. The change in current direction causes the overreaching distance elements to see the fault in the opposite direction to the direction in which the fault was initially detected (settings of these elements exceed 150% of the line impedance at each terminal). The race between operation and resetting of the overreaching distance elements at each line terminal can cause permissive overreach, and blocking schemes to trip the healthy line. A system configuration that could result in current reversals is shown in the figure below. For a fault on line L1 close to circuit breaker B, as circuit breaker B trips it causes the direction of current flow in line L2 to reverse. Current reversal guard logic is incorporated in this product to prevent POR and Blocking schemes from tripping incorrectly during current reversal conditions.

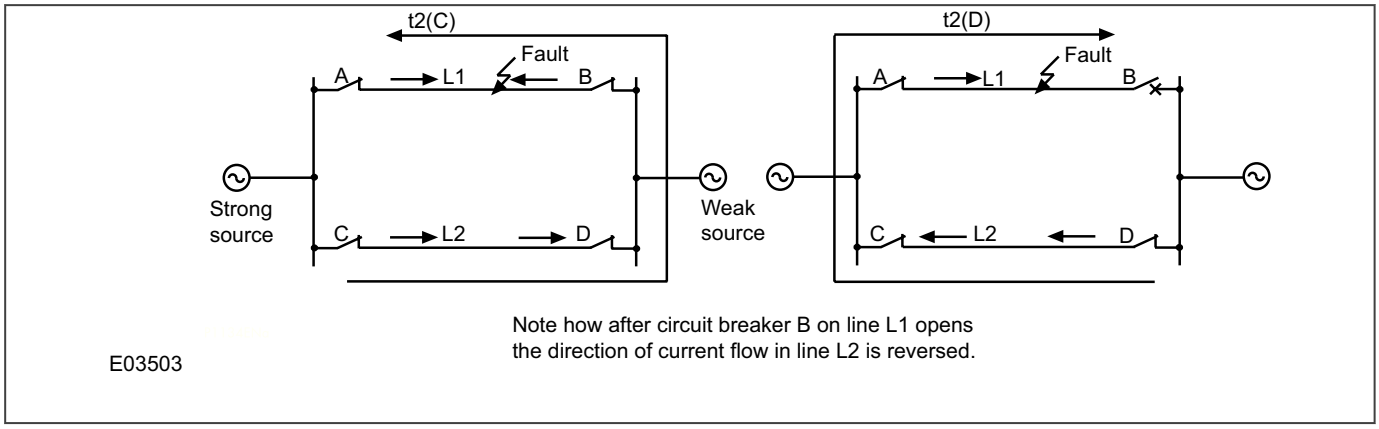



**Figure 92: Example of fault current reversal of direction**

The current reversal guard incorporated in the permissive overreach scheme logic is initiated when the reverse looking Zone 4 elements operate on a healthy line.

Once the reverse looking Zone 4 elements have operated, the permissive trip logic and signal send logic are inhibited at substation D. The reset of the current reversal guard timer is initiated when the reverse looking Zone 4 resets. A time delay ***tReversal Guard*** is required in case the overreaching trip element at end D operates before the signal send from the protection at end C has reset. Otherwise this would cause the product at D to overreach. Permissive tripping for the products at D and C substations is enabled again once the faulted line is isolated and the current reversal guard time has expired.

The current reversal guard incorporated in the blocking scheme logic is initiated when a blocking element picks-up to inhibit the channel-aided trip. When the current reverses and the reverse looking Zone 4 elements reset, the blocking signal is maintained by the timer ***tReversal Guard***. Therefore, the protections in the healthy line are prevented from overreaching due to the sequential opening of the circuit breakers in the faulted line. After the faulted line is isolated, the reverse-looking Zone 4 elements at substation C and the forward looking elements at substation D reset.

Two variants of Blocking scheme are available:

- Blocking 1 (Reversal Guard applied to the Signal Send)
- Blocking 2 (Reversal Guard applied to the Signal Receive)

### 7.3.6 AIDED DISTANCE BLOCKING SCHEMES

Two default Blocking schemes are provided:

- Blocking 1
- Blocking 2

The two schemes are similar. Both schemes feature current reversal guard signals used in conjunction with reverse looking Zone 4 elements. In the Blocking 1 scheme, the current reversal guard signal applies to the send signal, whereas in the Blocking 2 scheme, the current reversal guard signal applies to the receive signal.

The signalling channel is keyed from operation of the reverse-looking Zone 4 elements. If the remote zone 2 element picks up, it operates after the trip delay if no block is received. Listed below are some of the main features and requirements for a Blocking scheme:

- Blocking schemes require only a simplex communication channel.
- Reverse-looking Zone 4 is used to send a blocking signal to the remote end to prevent unwanted tripping.
- When a simplex channel is used, a blocking scheme can easily be applied to a multi-terminal line provided that outfeed does not occur for any internal faults.
- The blocking signal is transmitted over a healthy line, and so problems associated with power line carrier signals failing are avoided.
- Blocking schemes provide similar resistive coverage to the permissive overreach schemes.
- Fast tripping occurs at a strong source line end, for faults along the protected line section, even if there is weak- or zero- infeed at the other end of the protected line.
- If a line terminal is open, fast tripping still occurs for faults along the whole of the protected line length.
- If the signalling channel fails to send a blocking signal during a fault, fast tripping occurs for faults along the whole of the protected line, but also for some faults in the next line section.
- If the signalling channel is taken out of service, the protection operates in the conventional basic mode.
- A current reversal guard timer is included in the logic to prevent unwanted tripping on healthy circuits during current reversal situations on a parallel circuits.

The Blocking scheme logic is:

- Send logic: Assert carrier if Reverse Zone 4 element picks up
- Trip logic: Trip if the Zone 2 element picks up if no carrier is received, but only after the Aided Signal Delay time out

The figure below shows the simplified scheme logic.

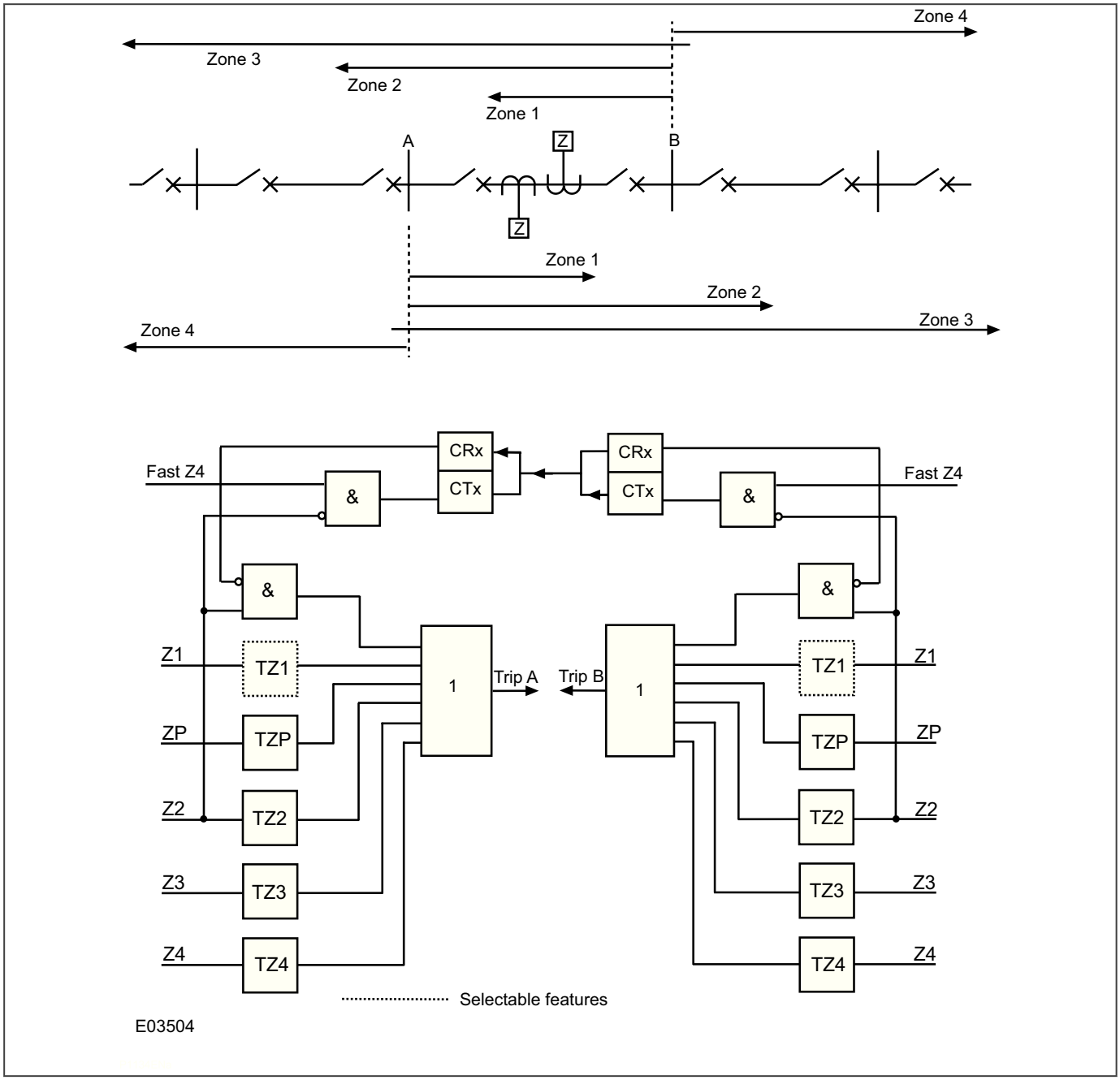



**Figure 93: Aided Distance Blocking scheme (BOP)**

## 7.3.7 AIDED DISTANCE UNBLOCKING SCHEMES

The Unblocking schemes are specifically designed for use with Power Line Carrier (PLC) communications where different frequencies are used to indicate that a guard (no-fault condition) or a trip (fault condition) signal should be transmitted to the remote terminal(s). Normally, either a guard signal or a trip signal should be transmitted and received. Under certain fault conditions however, the PLC signal can be heavily attenuated or even lost completely. In such conditions, Permissive Overreach Unblocking schemes allow the permissive tripping to operate for a short period after the carrier is lost. This ensures fast, selective fault clearance.

To use this scheme you need to assign two inputs. Generally, the inputs are mapped to opto-inputs in the default PSL. The table below shows a default mapping for Aided Scheme 1.

| DDB signal (Opto-input) | DDB signal |
|---|---|
| ***Input L3*** (DDB: 34) | ***Aided 1 Scheme Rx*** (DDB: 493) |
| ***Input L4*** (DDB: 35) | ***Aided 1 COS/LGS*** (DDB: 492) |

The ***Aided 1 Scheme RX*** signal corresponds to a 'channel-receive' signal for scheme 1. The ***Aided 1 COS/LGS*** signal corresponds to a 'channel out of service' or 'loss of guard' signal ('Loss of guard' is the inverse signal to 'guard received').

As well as the default mapping, it is possible to map the signals to other inputs if required.

The window during which the unblocking logic is enabled starts 10ms after the guard signal is lost and continues for 150ms. The 10ms delay gives time for the signalling equipment to change frequency.

*Note:*
*If the **Z1 Ext Scheme** setting is set to operate for channel failure, the Zone 1 extension logic will be invoked if a channel failure is detected.*

This scheme type also provides Loss of Guard logic as described below.

| System condition | Permissive channel received | Loss of guard | Permissive trip allowed | Alarm generated |
|---|---|---|---|---|
| Healthy Line | No | No | No | No |
| Internal Line Fault | Yes | Yes | Yes | No |
| Unblock | No | Yes | Yes, during a 150 ms window | Yes, delayed on pickup by 150 ms |
| Signalling Anomaly | Yes | No | No | Yes, delayed on pickup by 150 ms |

## 7.3.8 AIDED DISTANCE LOGIC DIAGRAMS

### 7.3.8.1 AIDED DISTANCE SEND LOGIC

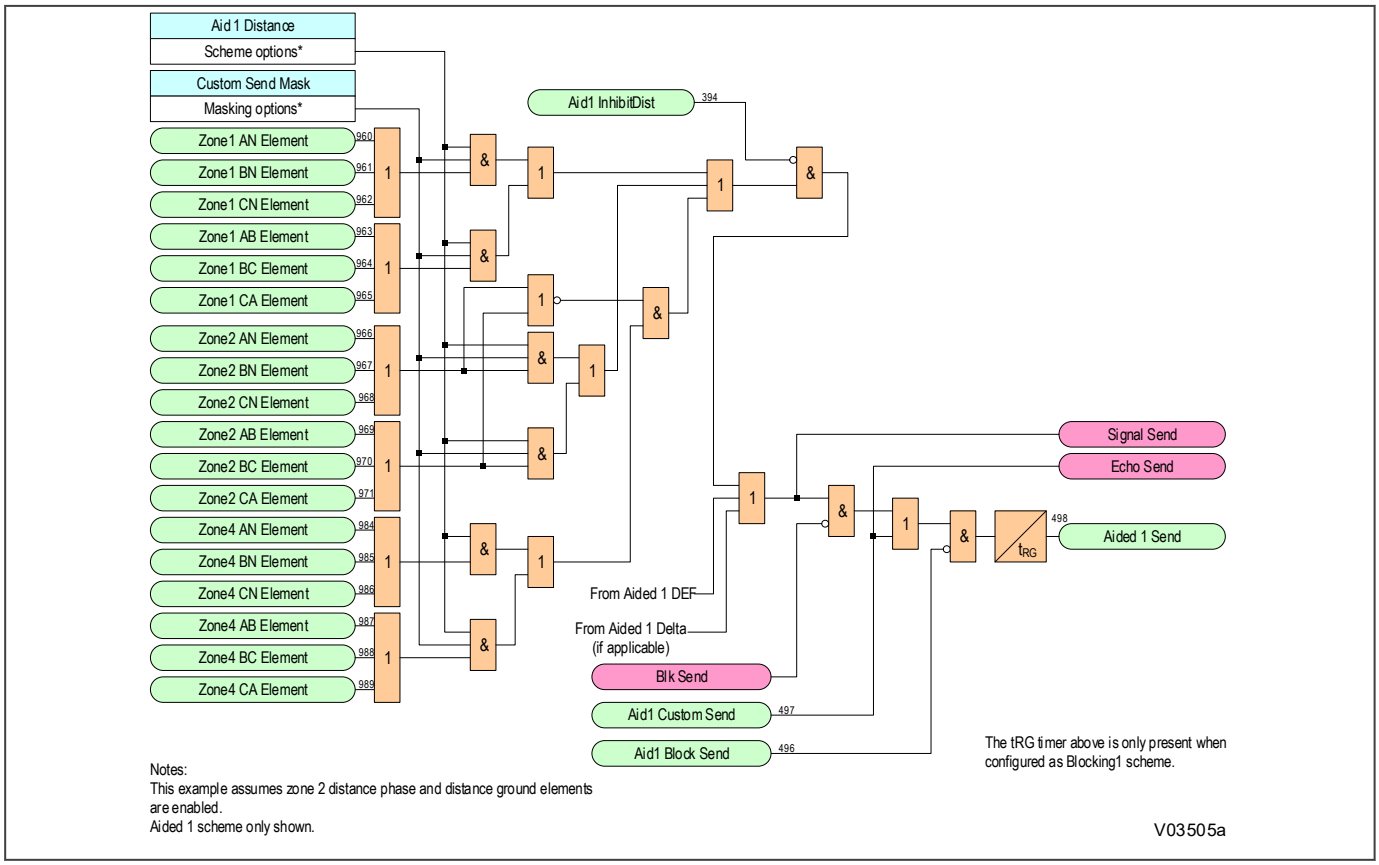



**Figure 94: Aided Distance Send logic**

### 7.3.8.2 CARRIER AIDED SCHEMES RECEIVE LOGIC

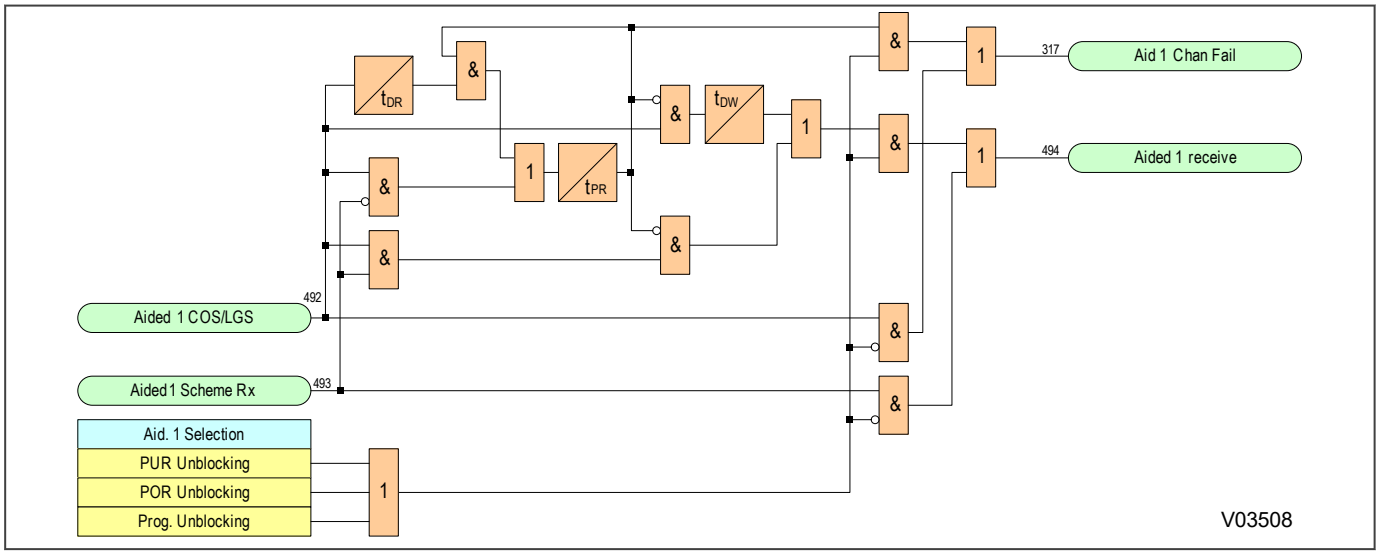



**Figure 95: Carrier Aided Schemes Receive logic**

### 7.3.8.3 AIDED DISTANCE TRIPPING LOGIC

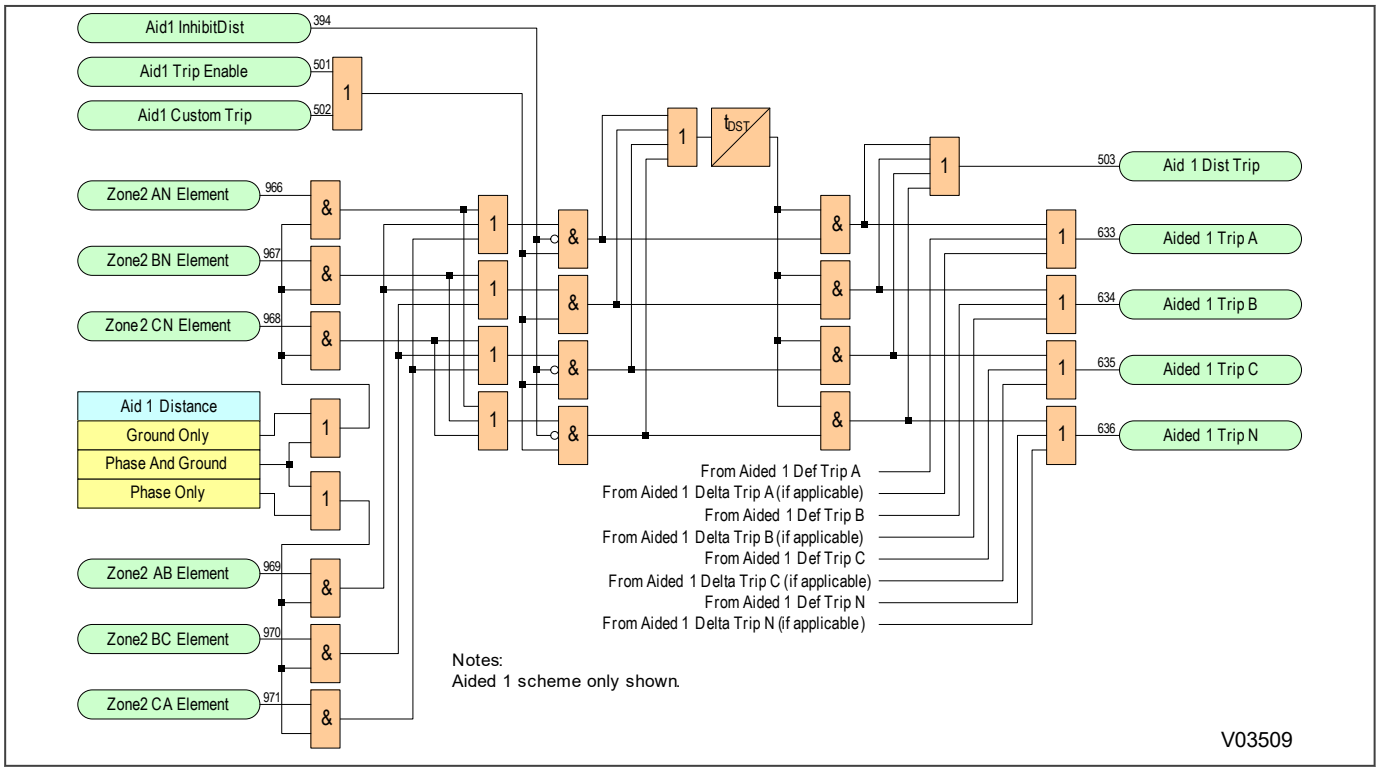



**Figure 96: Aided Distance Tripping logic**

### 7.3.8.4 PUR AIDED TRIPPING LOGIC

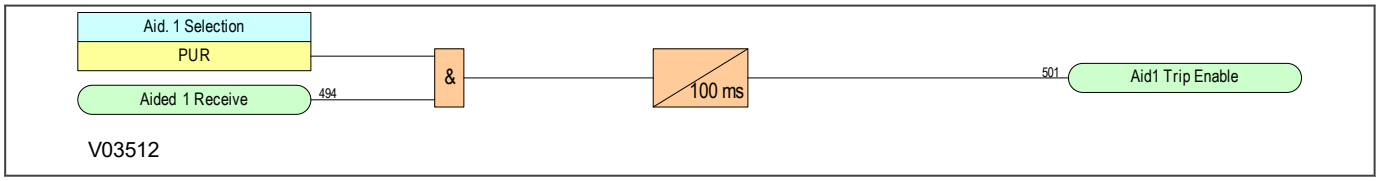



**Figure 97: PUR Aided Tripping logic**

### 7.3.8.5 POR AIDED TRIPPING LOGIC

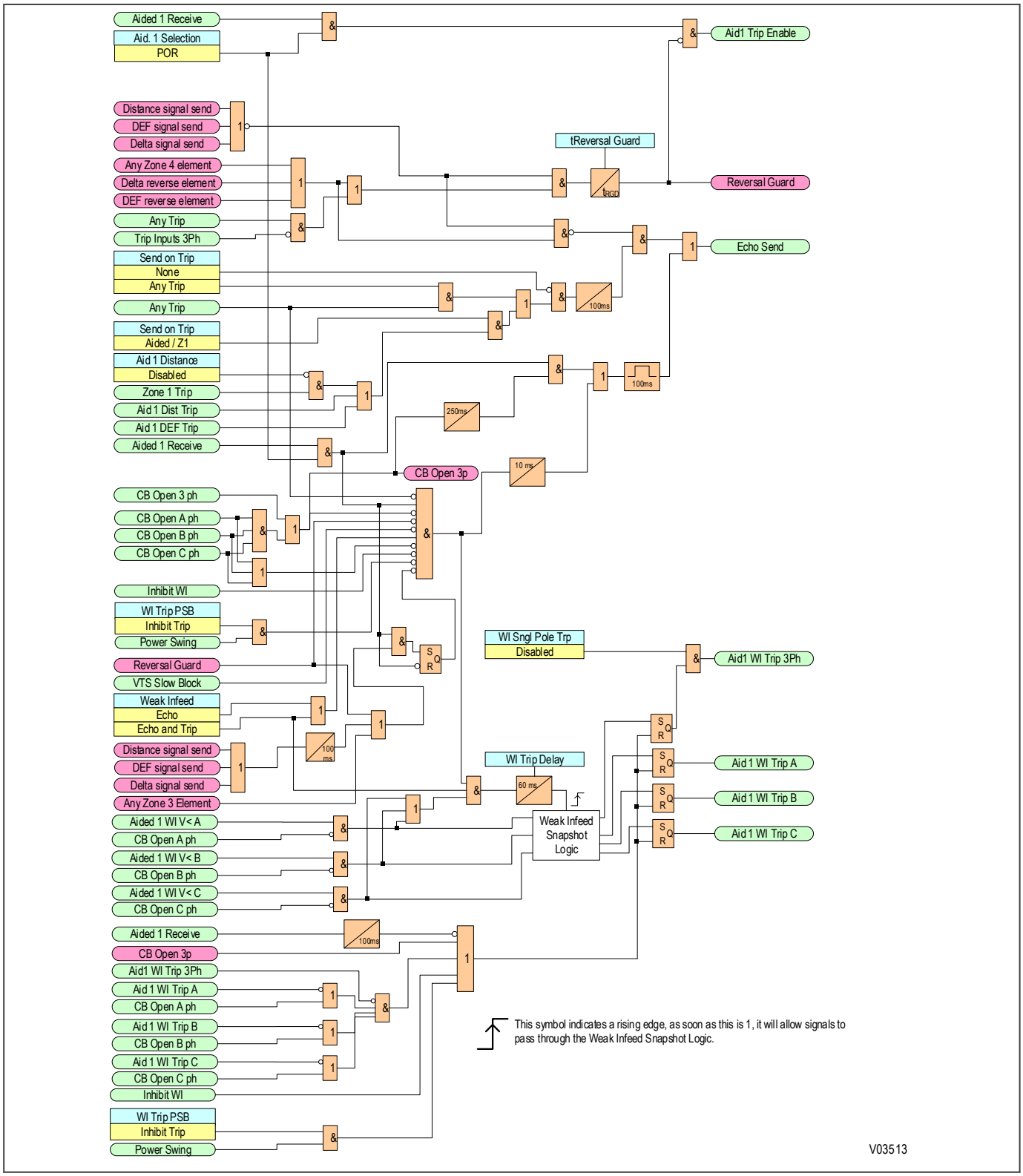



**Figure 98: POR Aided Tripping logic**

### 7.3.8.6 AIDED SCHEME BLOCKING 1 TRIPPING LOGIC

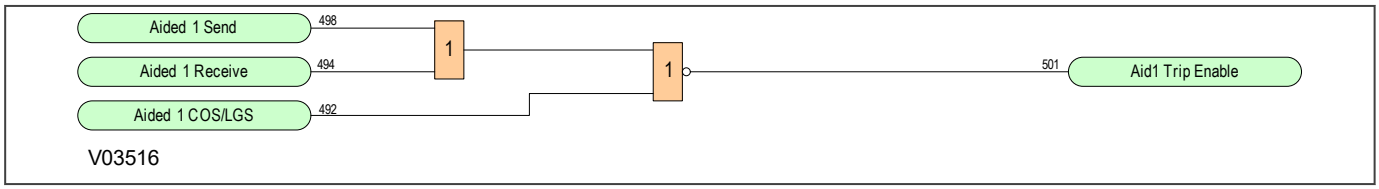



**Figure 99: Aided Scheme Blocking 1 Tripping logic**

### 7.3.8.7 AIDED SCHEME BLOCKING 2 TRIPPING LOGIC

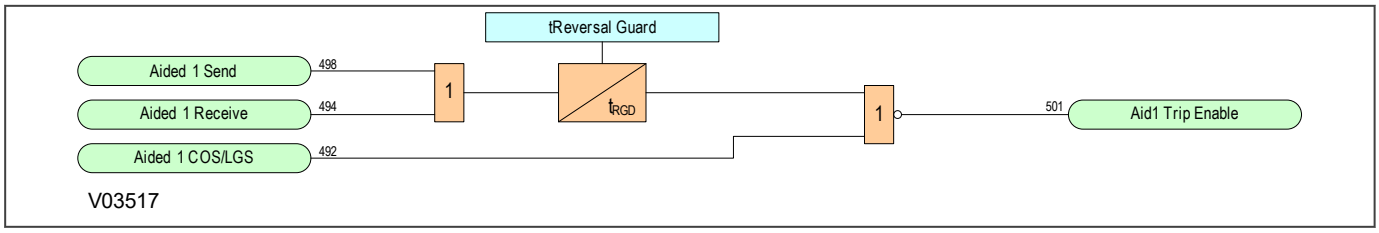



**Figure 100: Aided Scheme Blocking 2 Tripping logic**

# 7.4 AIDED DEF SCHEME LOGIC

## 7.4.1 AIDED DEF INTRODUCTION

High resistance faults may be difficult to detect using distance protection. A Directional Earth Fault DEF element is sometimes used in conjunction with a communication scheme to provide protection against such faults. The use of Aided-Trip logic in conjunction with the DEF element allows faster trip times, and can facilitate single-phase tripping, if needed.

To use the Aided DEF protection you will need appropriate communication channels between terminals in the scheme. The Programmable Scheme Logic (PSL) allows you to map signals for communication over the channels. The signals you map may be signals to be sent to a remote terminal, or signals expected to be received from a remote terminal. Two Aided DEF schemes are available.

With Aided DEF protection, the residual current (earth fault current) is compared with a threshold to determine the presence of a fault, and a directionalising quantity to determine its direction. Directional measurements from protecting terminals are then used in conjunction with teleprotection signals between the terminals, and aided scheme logic to determine whether the fault is within the protected line (and hence trip), or outside the protected line (and hence restrain).

## 7.4.2 IMPLEMENTATION

Aided DEF protection can be used with permissive over-reach schemes or blocking schemes.

The Aided DEF protection is enabled using the ***Directional E/F*** setting in the *CONFIGURATION* column. This makes the settings in the *AIDED DEF* column visible.

The Aided DEF requires a polarizing quantity (selected in the ***DEF Polarizing*** setting) in conjunction with a characteristic angle setting (***DEF Char. Angle***) to make the directional decision.

For all models a signal derived from the phase voltage inputs can be used for polarization. For certain models with more VT inputs, a directly measured input can be used.

You have a choice between Zero Sequence Polarizing or Negative Sequence Polarizing for the Aided DEF element. If you choose Zero Sequence Polarization, you have a choice to enable an innovative feature known as Virtual Current Polarization to enhance the Aided DEF function.

Aided DEF protection is blocked if any of the following conditions are met:

- An ***Any Trip*** signal is asserted by one of the integrated protection functions
- The phase selector picks up on more than one phase
- Any of the signals ***Pole Dead A***, ***Pole Dead B***, or ***Pole Dead C*** are asserted

## 7.4.3 AIDED DEF POLARIZATION

There are essentially two ways of esablishing the direction of an earth fault:

- Zero sequence polarization
- Negative sequence polarization

Zero Sequence polarization normally uses the measurement of residual voltage (VN). This can only be achieved if a 5-limb VT or three single-phase VTs are used. A special form of zero sequence polarization called Virtual Current Polarization is also possible with this device. Virtual Current Polarization allows directionalisation for low levels of polarization voltage.

#### 7.4.3.1 ZERO SEQUENCE POLARIZING

Residual voltage is generated during earth faults. This zero-sequence quantity can be used to polarize the directional decision of Aided DEF protection. This device can derive residual voltage if connected to a suitable voltage transformer (VT) arrangement.

For the Aided DEF to use a derived voltage signal, the three phase voltage inputs must be supplied from a 5-limb VT, or from three single-phase VTs having the primary star-point earthed. These VT arrangements allow the passage of residual flux and hence allow the device to derive the required residual voltage. A 3-limb VT has no path for residual flux and is therefore unsuitable for zero-sequence Polarization.

Small levels of residual voltage may be present under normal system conditions due to system imbalances, VT inaccuracies and device tolerances. You can set a threshold (***DEF VNPol Set***) to provide stability against Aided DEF operation under these conditions. Residual voltage (***Vres***) is nominally 180° out of phase with residual current so Aided DEF elements are polarized from the -Vres quantity. This 180° phase shift is automatically compensated in this device.

##### 7.4.3.1.1 VIRTUAL CURRENT POLARIZING

A technique called Virtual Current Polarizing can allow the Aided DEF protection to operate even if the Polarizing voltage is below the ***DEF VNPol Set*** threshold. If the superimposed current phase selector associated with the Distance protection has identified a faulted phase, for example phase A, it removes that phase voltage from the residual calculation Va + Vb + Vc, leaving only Vb + Vc. The resultant Polarizing voltage has a large magnitude and is in the same direction as –Vres. This allows the protection to be applied even where very solid earthing behind the protection prevents residual voltage from being developed.

This technique of subtracting the faulted phase is described as Virtual Current Polarizing because it removes the need to use current Polarizing from a current transformer (CT) in a transformer star (wye)-earth connection behind the device.

If you don't want to use this feature you should set ***Virtual I Pol*** to `Disabled` so that removal of the faulted phase voltage from the residual voltage calculation does not happen. The Aided DEF protection is then Polarized by the residual voltage only.

The directional criteria with zero sequence (virtual current) Polarization are as follows:

**Directional forward**

$$90° < (\text{angle}(VNpol) + 180°) - (\text{angle}(IN) - RCA) < 90°$$

**Directional reverse**

$$90° > (\text{angle}(VNpol) + 180° - (\text{angle}(IN) - RCA) > 90°$$

This is represented in the following figure:

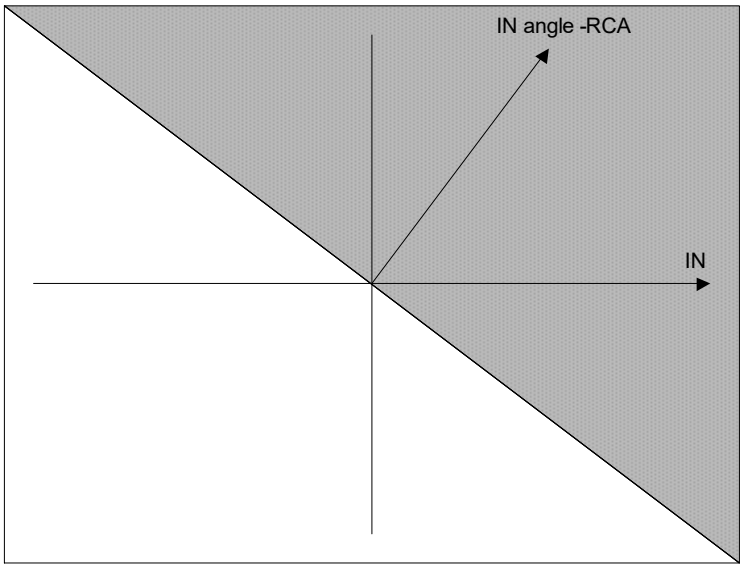



**Figure 101: Virtual Current Polarization**

The Polarizing voltage (VNpol) is as per the table below and RCA is the relay characteristic angle defined by the ***DEF Char. Angle*** setting.

| Phase selector pickup | VNpol |
|---|---|
| A Phase Fault | VB + VC |
| B Phase Fault | VA + VC |
| C Phase Fault | VA + VB |
| No Selection | VN = VA + VB + VC |

*Note:*
*The virtual current polarization works if the **DEF Polarizing** setting is `Zero Sequence`, the **Virtual I Pol** setting is `Enabled`, and the VN voltage is less than the selected value of the **DEF VNpol Set** setting.*

### 7.4.3.2 NEGATIVE SEQUENCE POLARIZING

In certain applications, residual voltage polarization of Aided DEF may not be possible, or it may be problematic. Example cases are:

- Where a 3-limb voltage transformer is fitted, which has no path for residual flux.
- Where the application features a parallel line and zero sequence mutual coupling may exist.

The problems in these applications can be alleviated using negative phase sequence (nps) voltage for polarization. The nps voltage threshold must be set in the cell ***DEF V2pol Set***.

*Note:*
*This setting is 3 times V2.*

*Note:*
*The current quantity used for operation of the Aided DEF when it is nps Polarized is the residual current, not the nps current, i.e. settings **DEF FWD** Set and **DEF REV Set** are for residual current.*

*Note:*
*The minimum negative sequence current required for nps polarisation is the value set by the setting, **DEF REV Set***

The directional criteria with negative sequence polarization are as follows:

**Directional forward**

$$-90° < [(\text{angle}(V2) + 180°) - (\text{angle}(I2) - RCA)] < 90°$$

**Directional reverse**

$$-90° > [(\text{angle}(V2) + 180°) - \text{angle}(I2) - RCA)] > 90°$$

where RCA is the relay characteristic angle set in the ***DEF Char. Angle*** setting.

This is represented in the following figure:

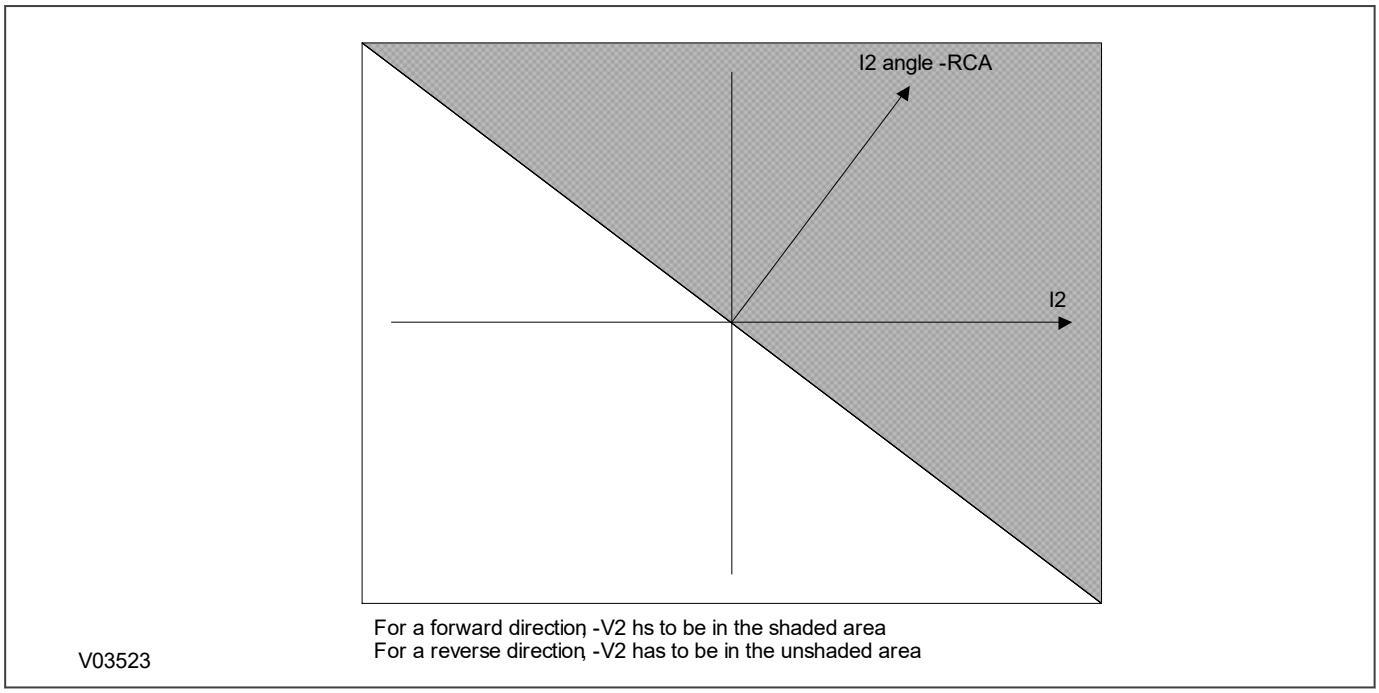



**Figure 102: Directional criteria for residual voltage polarization**

## 7.4.4 AIDED DEF SETTING GUIDELINES

To use Aided DEF protection you need to set the polarization and the thresholds. Polarization can be achieved using either zero sequence signals or negative sequence signals.

For zero sequence polarized Aided DEF, the typical zero sequence voltage on a healthy system can be as high as 1% (i.e.: 3% residual), and the voltage transformer (VT) error could be 1% per phase. A ***VNpol Set*** setting between 1% and 4%.Vn is typical, to avoid spurious detection on standing signals. The residual voltage measurement provided in the *MEASUREMENTS 1* column may assist in determining the required threshold setting during commissioning, as this will indicate the level of standing residual voltage present. The Virtual Current Polarizing feature will create a polarizing voltage, which is always large regardless of whether actual VN is present.

With Aided DEF, the residual current under fault conditions lies at an angle lagging the polarized voltage. Hence, negative characteristic angle settings are required for Aided DEF applications. This is set in cell ***DEF Char. Angle*** in the *EARTH FAULT* settings.

The following angle settings are recommended for a residual voltage polarized device:-

- Solidly earthed distribution systems: -45°
- Solidly earthed transmissions systems: -60°

If ***Virtual I Pol*** is set to 'Disabled' it prevents checking of the faulted phase and subsequent removal of the faulted phase voltage. The aided DEF protection is then polarized by the residual voltage only.

For negative sequence polarization, the relay characteristic angle settings (***DEF Char. Angle***) must be based on the angle of the upstream negative phase sequence source impedance. A typical setting is -60°.

The ***DEF FWD Set*** setting determines the current sensitivity (trip sensitivity) of the aided DEF aided scheme. This setting must be set higher than any standing residual current unbalance. A typical setting will be between 10% and 20% In.

The ***DEF REV Set*** setting determines the current sensitivity for the reverse earth fault. The setting must always be below the aided DEF forward threshold for correct operation of blocking schemes and to provide stability for current reversal in parallel line applications. The recommended setting is 2/3 of the Aided DEF forward setting.

*Note:*
*The **DEF REV Set** setting has to be above the maximum steady state residual current imbalance.*

### 7.4.5 AIDED DEF POR SCHEME

The scheme has the same features and requirements as the corresponding Distance scheme and provides sensitive protection for high resistance earth faults.

The signalling channel is keyed from operation of the forward ***DEF Fwd Set*** element. If the remote device has also detected a forward fault, it operates with no additional delay when it receives this signal.

The logic is:

- Send logic: Key channel if ***DEF Fwd Set*** picks up
- Permissive trip logic: Trip if ***DEF Fwd Set*** picks up AND the channel key is received

The figure below shows the element reaches, and the simplified scheme logic of the Aided DEF POR scheme.

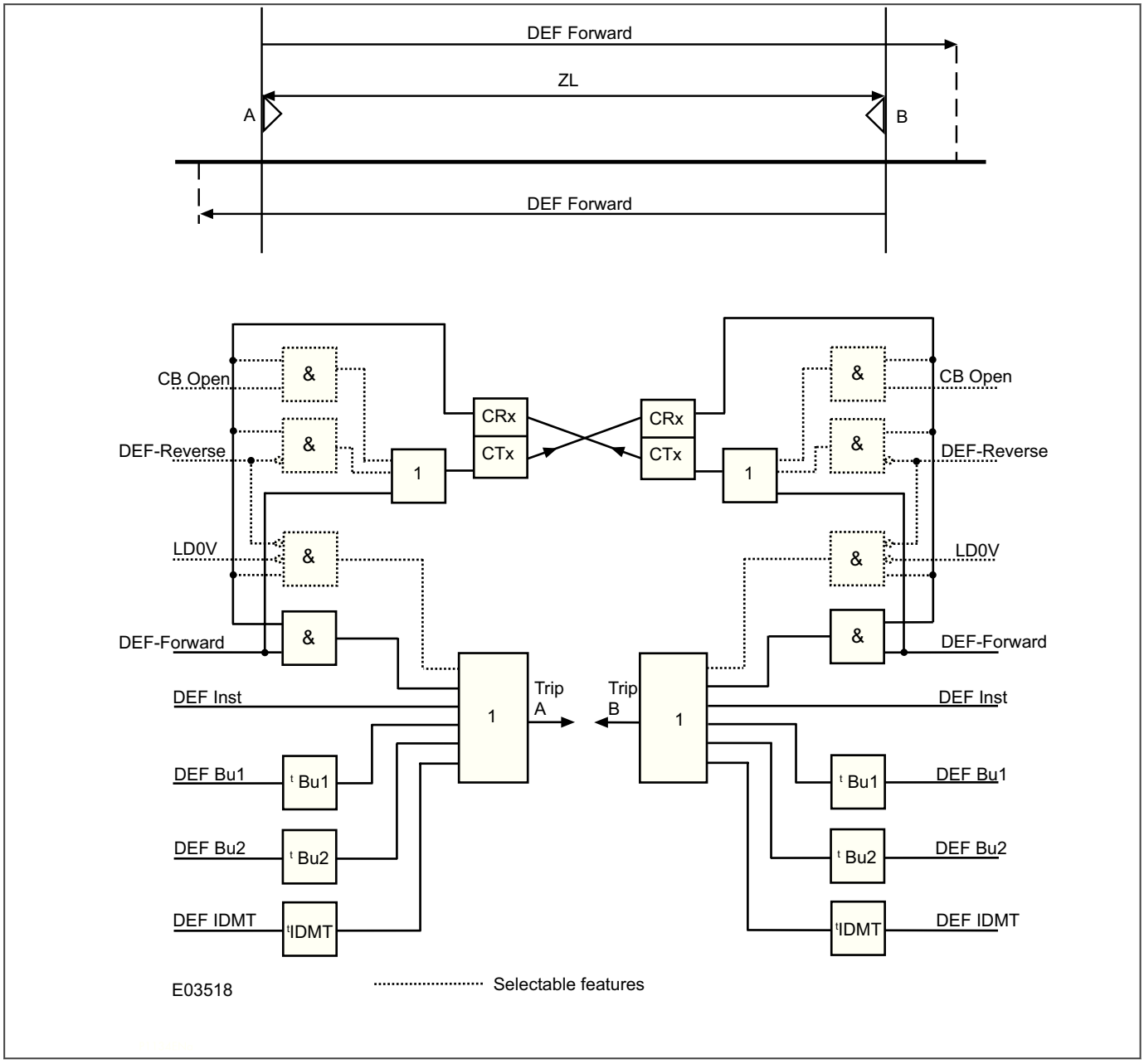



**Figure 103: Aided DEF POR scheme**

## 7.4.6 AIDED DEF BLOCKING SCHEME

The scheme has the same features/requirements as the corresponding Distance scheme and provides sensitive protection for high resistance earth faults.

The signalling channel is keyed from operation of the reverse Aided DEF element (***DEF REV Set***). If the remote device's forward Aided DEF element (***DEF FWD Set***) has picked up, it operates after the ***Aid. 1 DEF Dly.*** expires if no block is received.

Where 't' is shown in the diagram this signifies the time delay associated with an element. To allow time for a blocking signal to arrive, a short time delay on aided tripping must be used.

The logic is:

- Send logic: Key channel if ***DEF REV Set*** picks up
- Trip logic: Trip if ***DEF FWD*** Set AND Channel NOT Received, after ***Aid. 1 DEF Dly.*** expires.

The figures below show the element reaches, and the simplified scheme logic of the Aided Directional Earth Fault (Aided DEF) Blocking scheme.

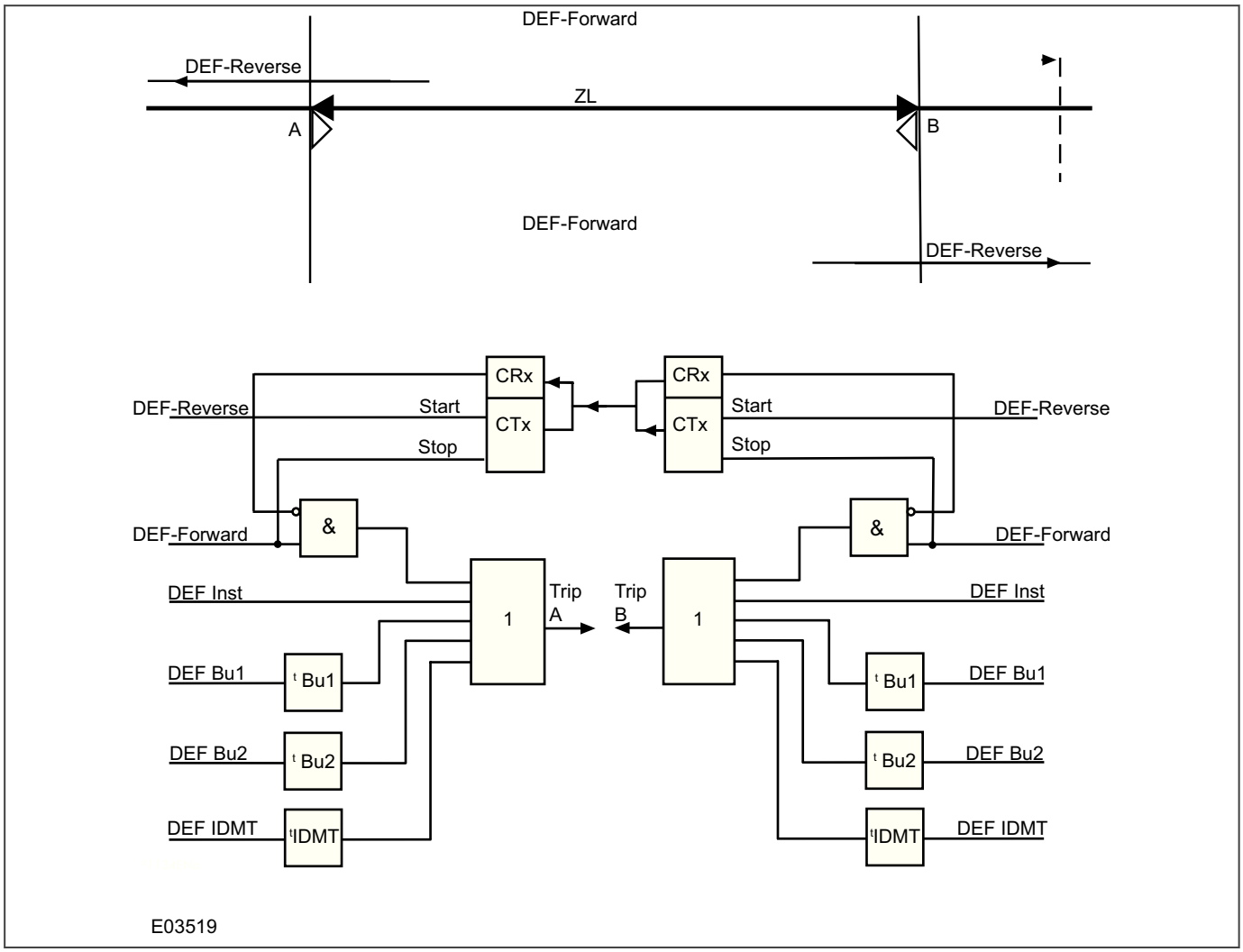



**Figure 104: Aided DEF Blocking scheme**

## 7.4.7 AIDED DEF LOGIC DIAGRAMS

### 7.4.7.1 DEF DIRECTIONAL SIGNALS

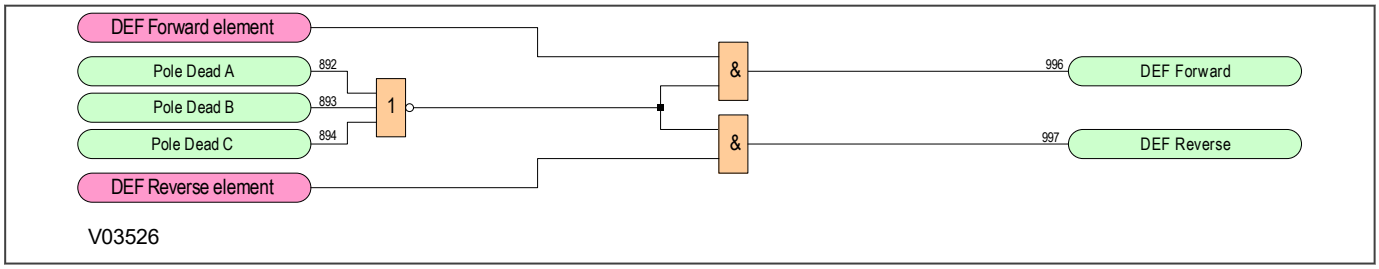



**Figure 105: DEF Directional Signals**

### 7.4.7.2 AIDED DEF SEND LOGIC

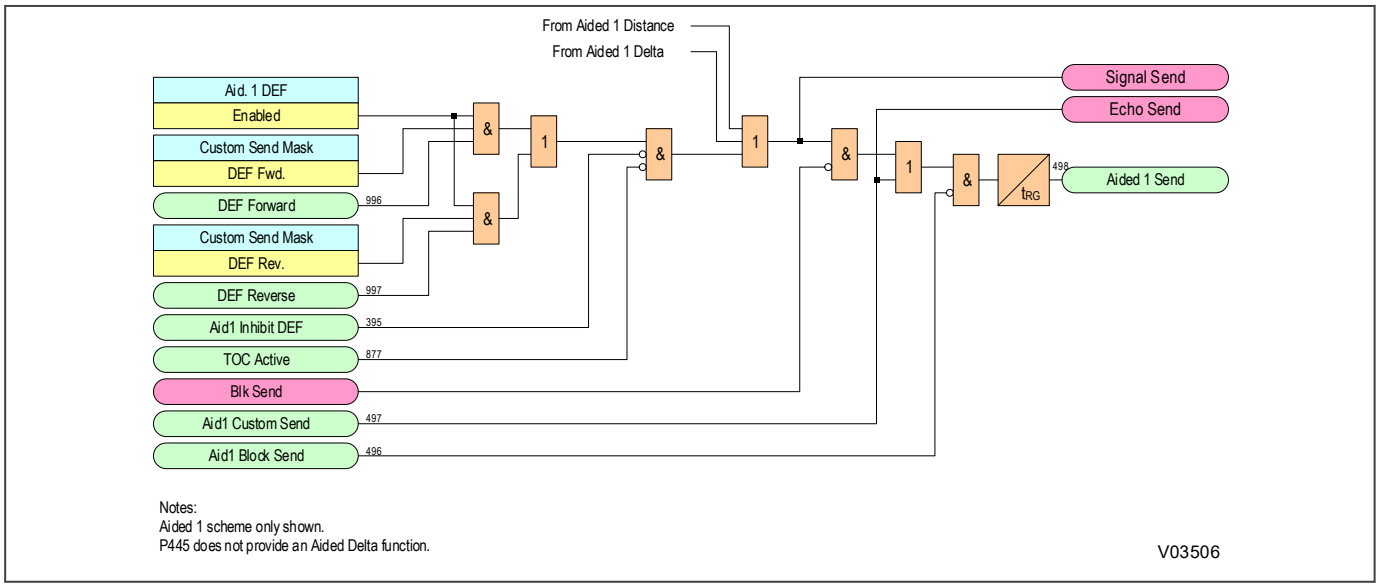



**Figure 106: Aided DEF Send logic**

### 7.4.7.3 CARRIER AIDED SCHEMES RECEIVE LOGIC

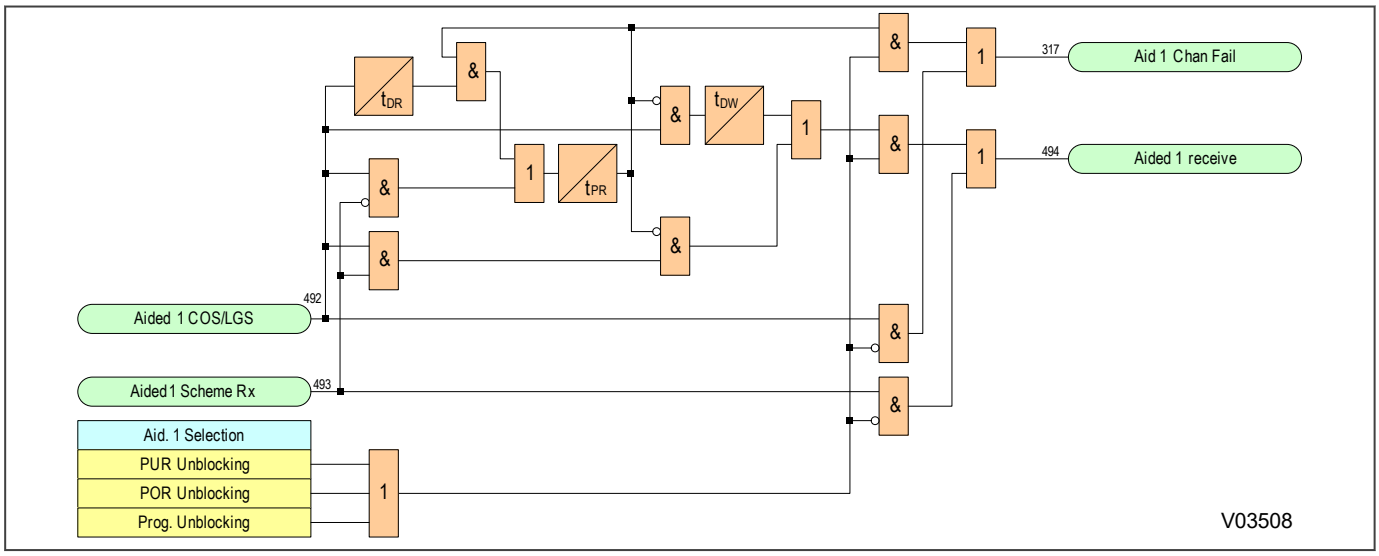



**Figure 107: Carrier Aided Schemes Receive logic**

### 7.4.7.4 AIDED DEF TRIPPING LOGIC

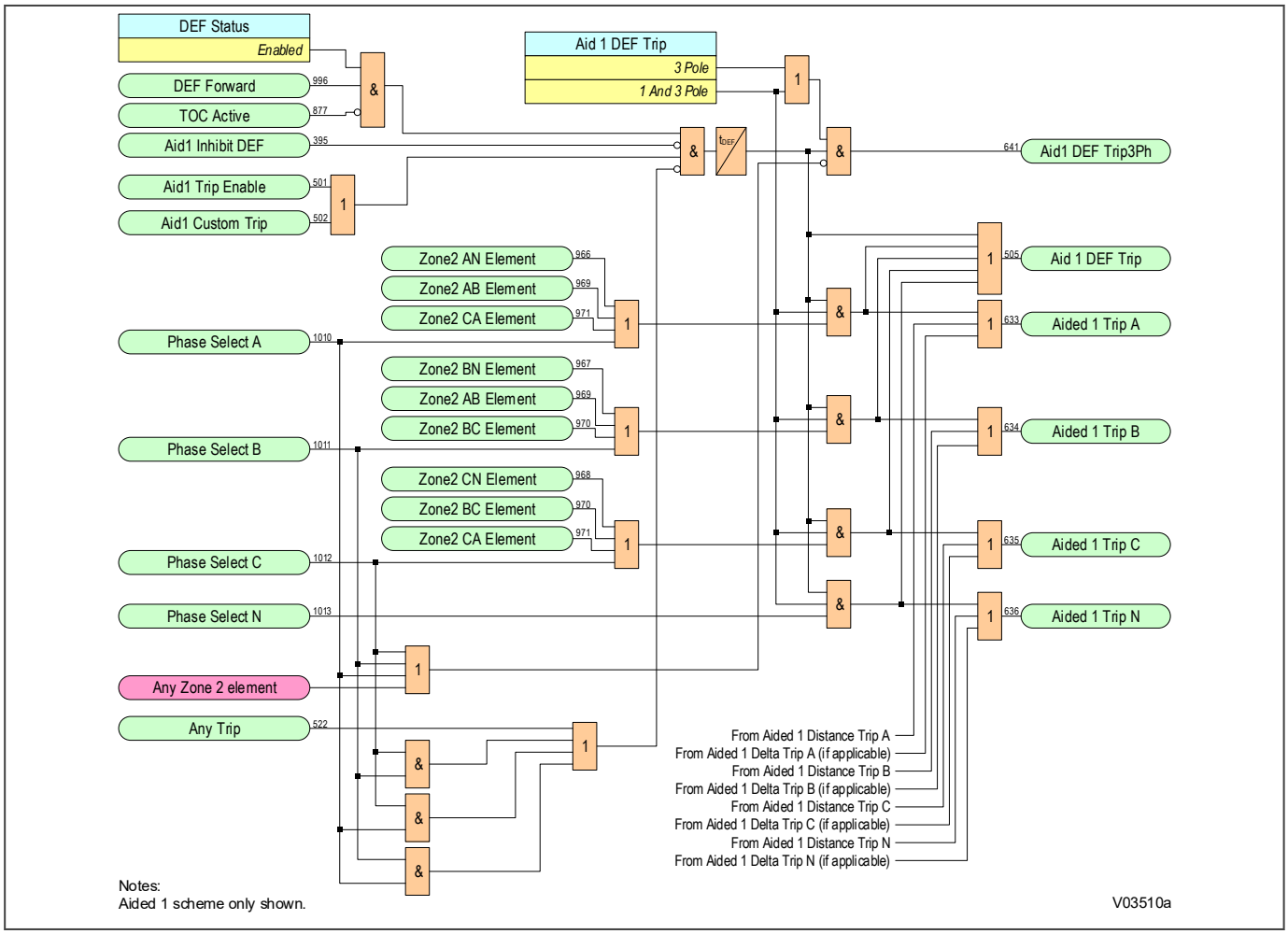



**Figure 108: Aided DEF Tripping logic**

### 7.4.7.5 POR AIDED TRIPPING LOGIC

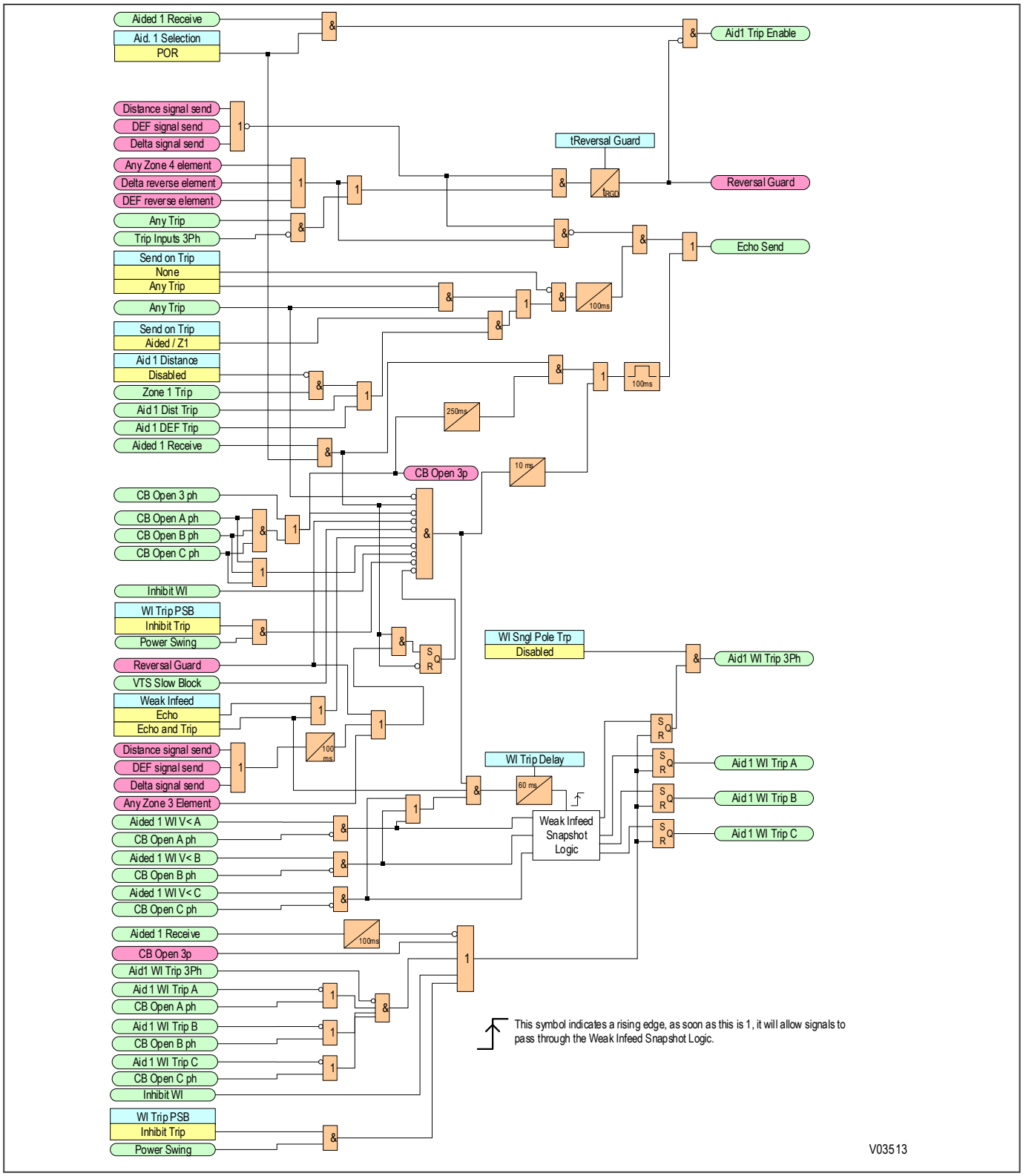



**Figure 109: POR Aided Tripping logic**

### 7.4.7.6 AIDED SCHEME BLOCKING 1 TRIPPING LOGIC

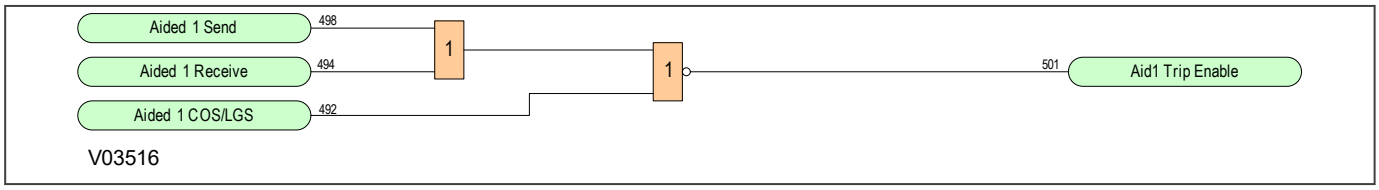



**Figure 110: Aided Scheme Blocking 1 Tripping logic**

### 7.4.7.7 AIDED SCHEME BLOCKING 2 TRIPPING LOGIC

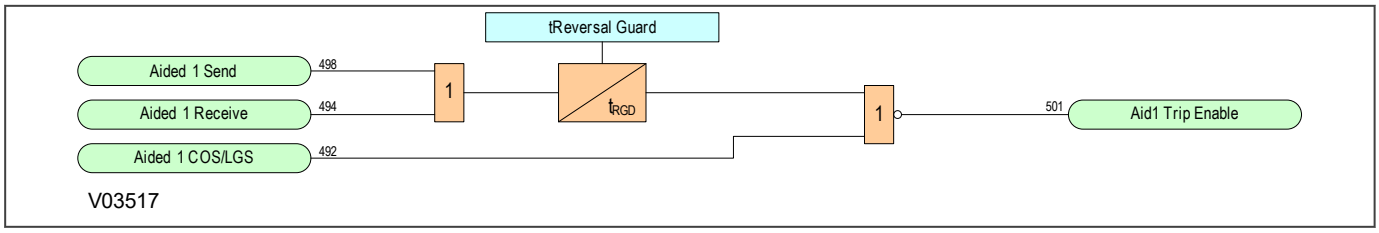



**Figure 111: Aided Scheme Blocking 2 Tripping logic**

## 7.5 AIDED DELTA SCHEME LOGIC

If either a Permissive Overreaching scheme or a Blocking schemes is selected, it can be used to implement Directional Comparison(Aided Delta) protection.

**Caution:**
**Aided Delta should not be used on a communications channel if that channel is being used to implement an Aided Distance Scheme or an Aided DEF scheme. You should ensure that the Aided Distance and Aided DEF elements are disabled if you want to apply the Aided Delta (Directional Comparison Protection).**

### 7.5.1 AIDED DELTA POR SCHEME

The channel for an Aided Delta POR scheme is keyed by operation of the overreaching Delta Forward elements. If the remote device has also detected a forward fault upon receipt of this signal, the protection operates.

If the signalling channel fails, Basic distance scheme tripping is available.

The logic is:

- Send logic: Key channel if a Detla Fault Forward is detected
- Permissive trip logic: Trip if a Delta Fault Forward AND a keyed channel is received.

This scheme is shown in the figure below.

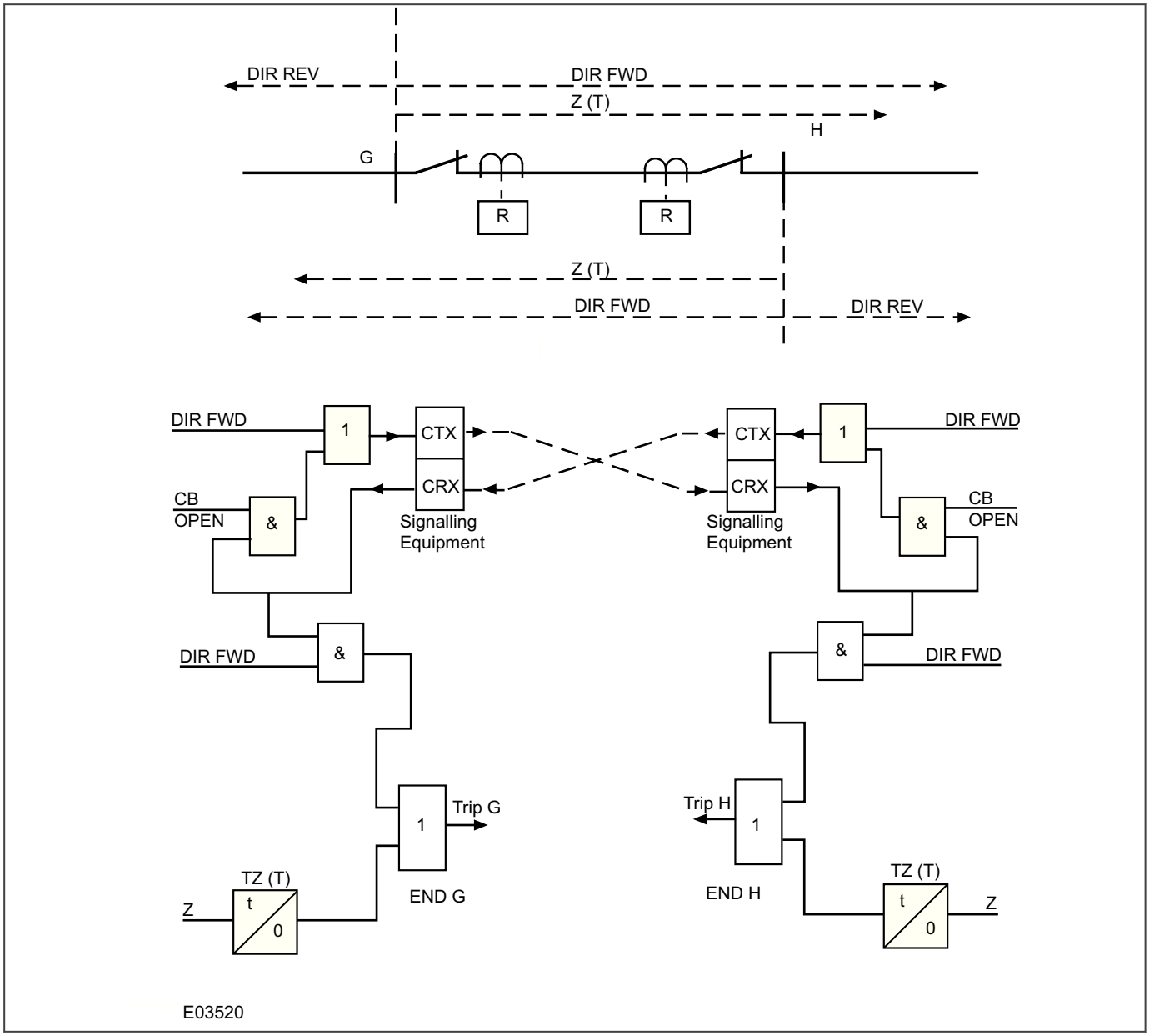



**Figure 112: Aided Delta POR scheme**

## 7.5.2 AIDED DELTA BLOCKING SCHEME

The signalling channel is keyed from operation of the Delta Reverse elements. If the remote device has detected Delta Forward, it operates after the trip delay if no block is received.

The logic is:

- Send logic: Key channel if a Delta Fault Reverse condition is detected
- Trip logic: Trip if a Delta Fault Forward condition is detected, AND a keyed channel signal is NOT received, before the Aided Delta Delay timer expires.

This scheme is shown in the figure below.

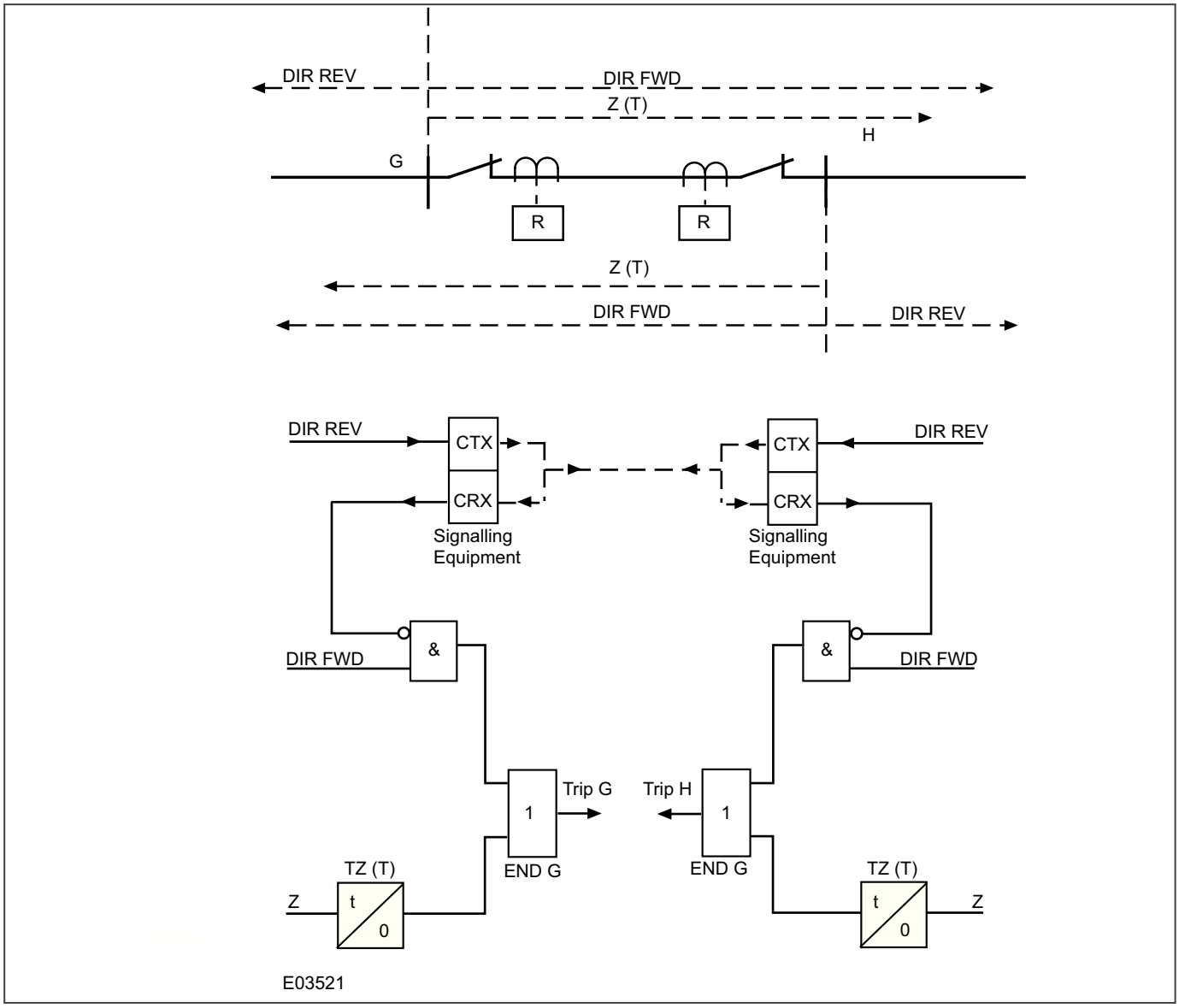



**Figure 113: Aided Delta Blocking scheme**

## 7.5.3 AIDED DELTA LOGIC DIAGRAMS

### 7.5.3.1 AIDED DELTA SEND LOGIC

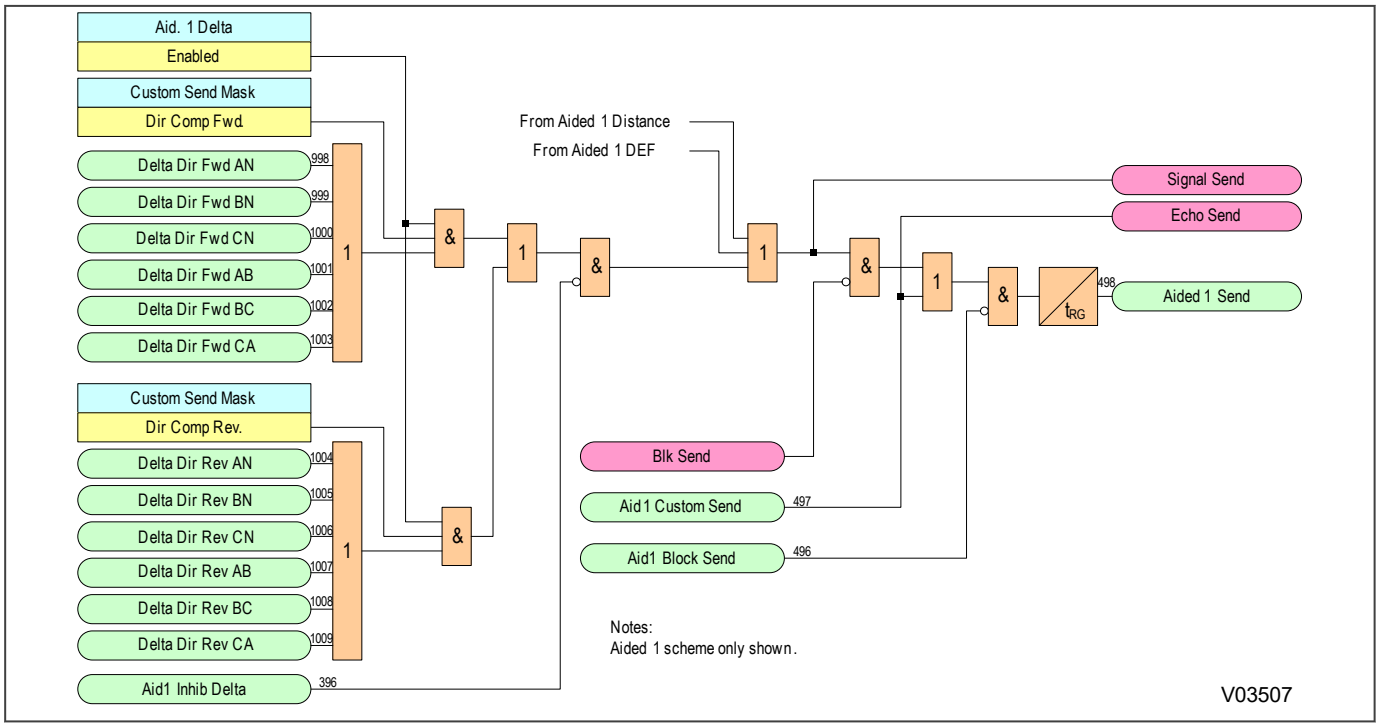



**Figure 114: Aided Delta Send logic**

### 7.5.3.2 CARRIER AIDED SCHEMES RECEIVE LOGIC

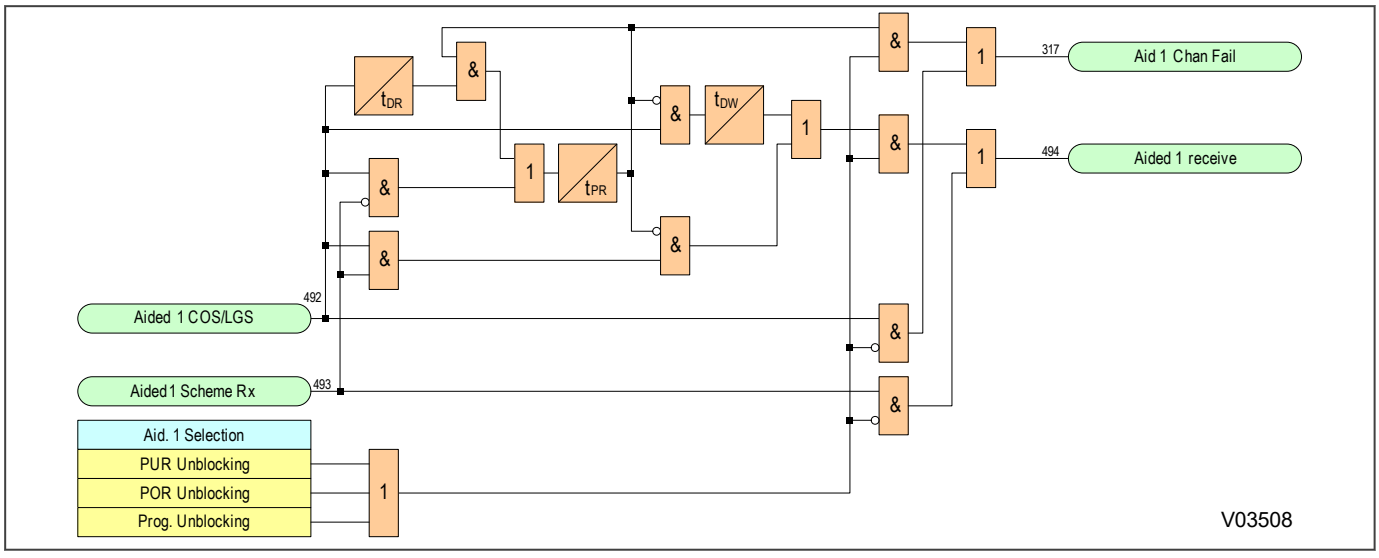



**Figure 115: Carrier Aided Schemes Receive logic**

### 7.5.3.3 AIDED DELTA TRIPPING LOGIC

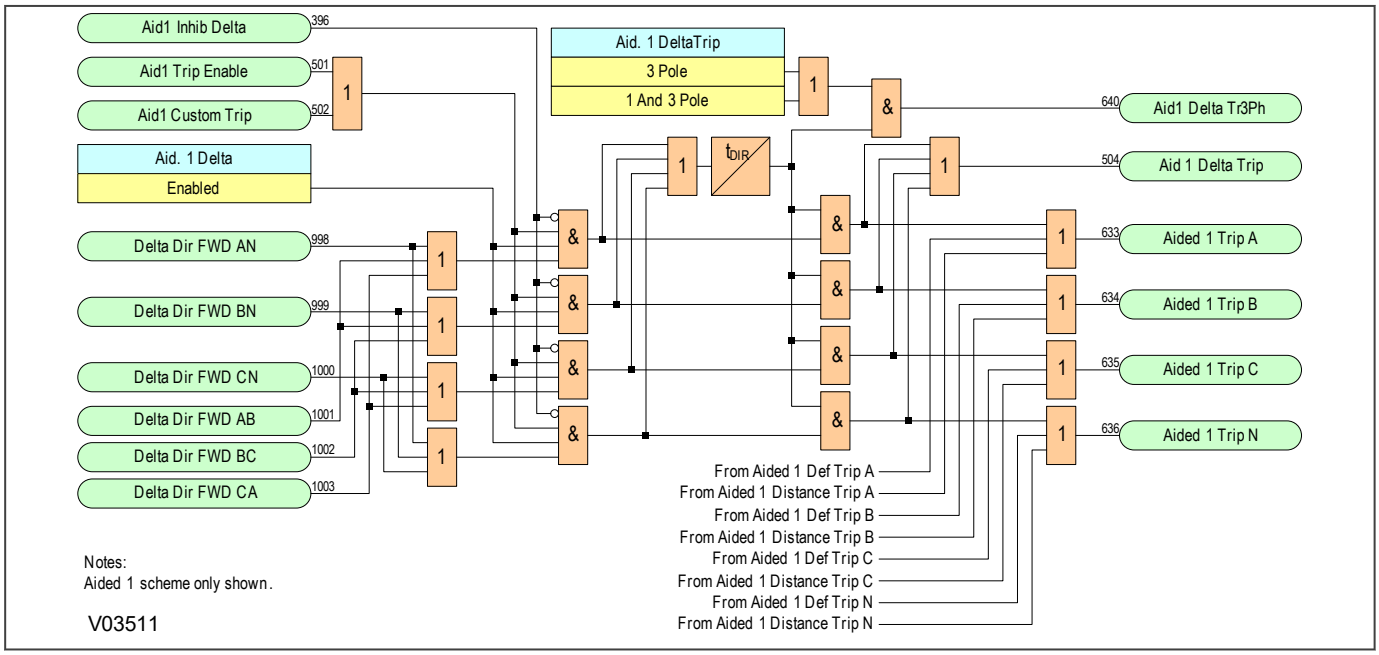



**Figure 116: Aided Delta Tripping logic**

### 7.5.3.4 POR AIDED TRIPPING LOGIC

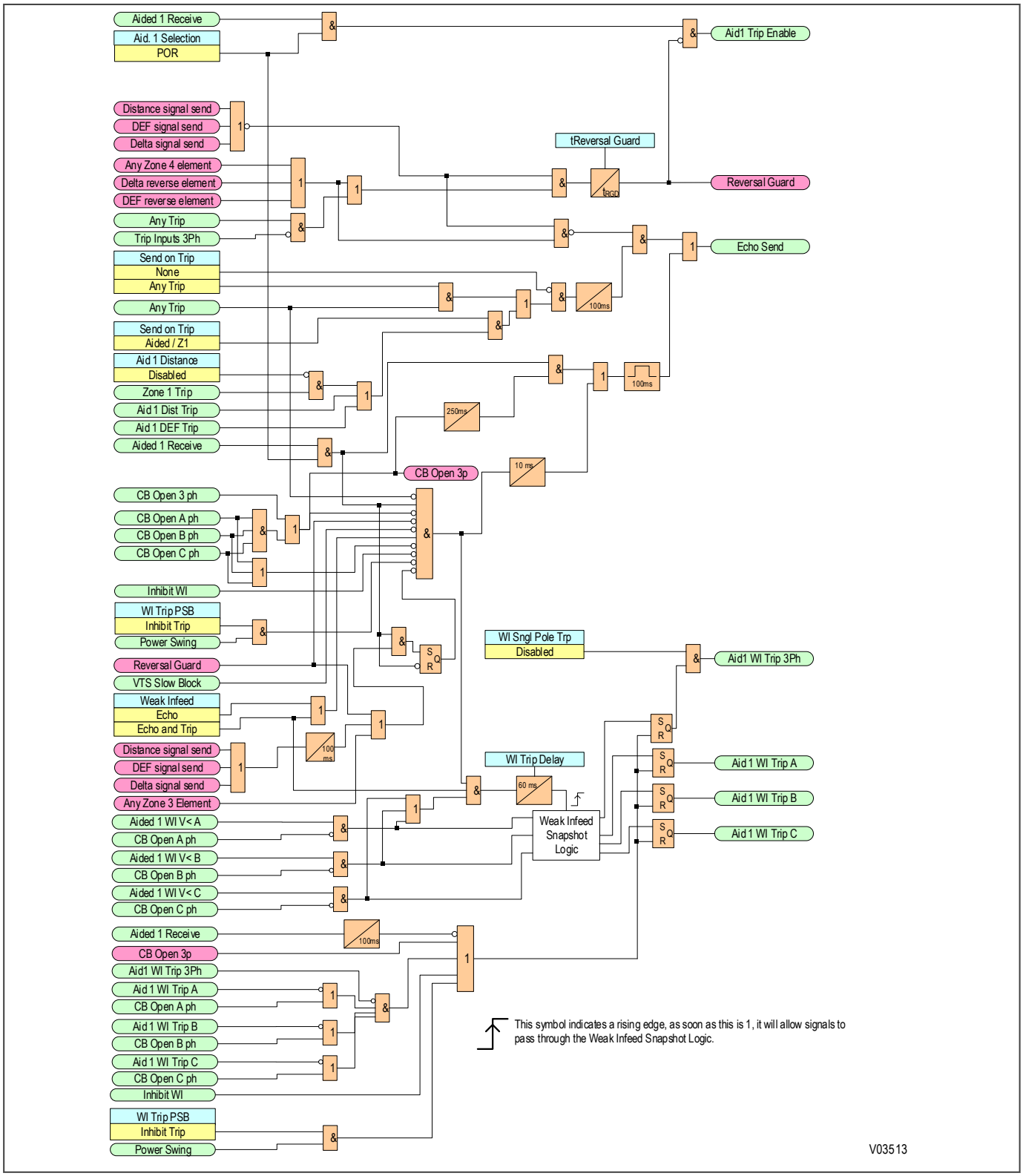



**Figure 117: POR Aided Tripping logic**

### 7.5.3.5 AIDED SCHEME BLOCKING 1 TRIPPING LOGIC

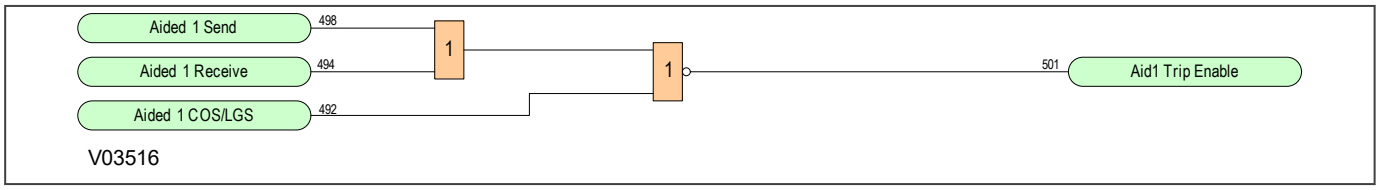



**Figure 118: Aided Scheme Blocking 1 Tripping logic**

### 7.5.3.6 AIDED SCHEME BLOCKING 2 TRIPPING LOGIC

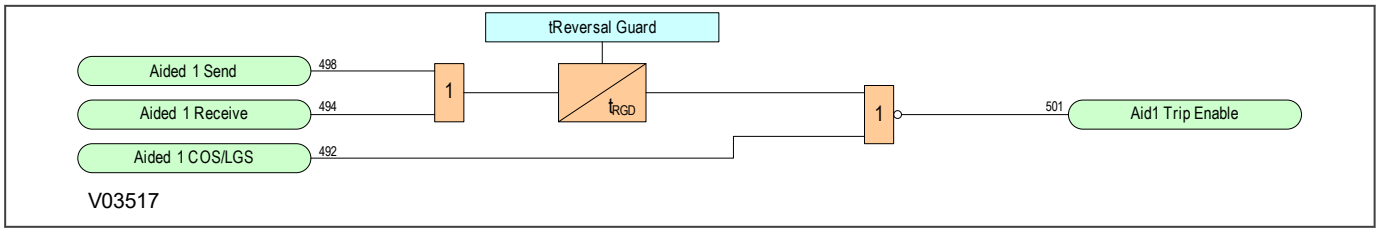



**Figure 119: Aided Scheme Blocking 2 Tripping logic**

# 7.6 APPLICATION NOTES

## 7.6.1 AIDED DISTANCE PUR SCHEME

This scheme allows an instantaneous Zone 2 trip on receipt of the signal from the underreaching element of the remote end protection.

The logic is:

- Send logic: Zone 1
- Permissive Trip logic: Zone 2 plus channel received

The time delay setting (***Aid.1 Dist. Dly***, ***Aid.2 Dist. Dly***) should be set to 0 ms for fast fault clearance.

## 7.6.2 AIDED DISTANCE POR SCHEME

This scheme allows This scheme allows an instantaneous Zone 2 trip on receipt of the signal from the overreaching element of the remote end protection.

The logic is

- Send logic: Zone 2
- Permissive Trip logic: Zone 2 plus channel received

The time delay setting (***Aid.1 Dist. Dly***, ***Aid.2 Dist. Dly***) should be set to 0 ms for fast fault clearance.

The POR scheme also uses the reverse looking zone 4 IED as a reverse fault detector. This is used in the current reversal logic and in the optional weak infeed echo feature.

### Weak Infeed

Where weak infeed tripping is employed, a typical voltage setting is 70% of rated phase-neutral voltage. Weak infeed tripping is time delayed according to the ***WI Trip Delay*** value, usually set at 60ms.

### Current Reversal Guard

The recommended setting is:

- ***tReversal Guard*** = Maximum signalling channel reset time + 60 ms.

## 7.6.3 AIDED DISTANCE BLOCKING SCHEME

This scheme uses a reverse looking zone 4 element to block operation of a forward looking zone 2 element at the remote end protection.

The logic is:

- Send logic: Reverse Zone 4
- Trip logic: Zone 2, plus Channel NOT Received

To allow time for a blocking signal to arrive, a short time delay must be allowed before tripping (***Aid.1 Dist. Dly***, ***Aid. 2 Dist. Dly***). The recommended delay is as follows:

- Recommended setting = Maximum signalling channel operating time + one power frequency cycle.

*Note:*
*Two variants of a Blocking scheme are provided, Blocking 1 and Blocking 2. Both schemes operate similarly, except that the reversal guard timer location in the logic changes. Blocking 2 may sometimes allow faster unblocking when a fault evolves from external to internal, and hence a faster trip.*

### Current Reversal Guard

The recommended settings are as follows:

- Where Duplex signalling channels are used: Set ***tReversal Guard*** to the maximum signalling channel operating time + 20ms.
- Where Simplex signalling channel is used: Set ***tReversal Guard*** to the combination of the maximum signalling channel operating time, minus the minimum signalling channel reset time, and add 20ms.

## 7.6.4 AIDED DEF POR SCHEME

This scheme allows an instantaneous DEF trip of a local terminal if it sees a forward fault AND it receives a signal from the remote end protection indicating that it is too has seen a forward fault.

The logic is:

- Send logic: DEF forward
- Permissive Trip logic: DEF forward plus channel received

The time delay would normally be set to 0 ms.

## 7.6.5 AIDED DEF BLOCKING SCHEME

This scheme prevents DEF tripping of a local terminal if it receives a signal from the remote end protection indicating that the fault is in the reverse direction, and hence out of zone.

The logic is:

- Send logic: DEF reverse
- Trip logic: DEF forward plus channel NOT received, with a small set delay

To allow time for a blocking signal to arrive, a short time delay on aided tripping must be used. The recommended delay time setting (***Aid. 1 DEF Dly.***, ***Aid. 2 DEF Dly.***) is the maximum signalling channel operating time +20 ms.

## 7.6.6 AIDED DELTA POR SCHEME

This scheme allows an instantaneous Delta trip of a local terminal if it sees a forward fault AND it receives a signal from the remote end protection indicating that it is too has seen a forward fault.

- Send logic: Delta fault Forward
- Permissive Trip logic: Delta fault Forward plus channel received

The time delay (***Aid. 1 Delta Dly***, ***Aid. 2 Delta Dly***) should be set to 0 ms for fast fault clearance.

### Current Reversal Guard

Current reversals during fault clearances on adjacent parallel lines need to be treated with care.To prevent maloperation, a current reversal guard timer must be set.

The recommended setting (***tReversal Guard***) is the maximum signalling channel reset time + 35 ms.

## 7.6.7 AIDED DELTA BLOCKING SCHEME

This scheme prevents Delta tripping of a local terminal if it receives a signal from the remote end protection indicating that the fault is in the reverse direction, and hence out of zone.

- Send logic: Delta fault reverse
- Trip logic: Delta fault forward plus channel NOT received, delayed by Tp (a short time delay)

Recommended delay setting (***Aid. 1 Delta Dly***, ***Aid. 2 Delta Dly***): Maximum signalling channel operating time + 6ms.

### Current Reversal Guard

Current reversals during fault clearances on adjacent parallel lines need to be treated with care.To prevent maloperation, a current reversal guard timer must be set.

The recommended setting (***tReversal Guard***) is the maximum signalling channel reset time + 35 ms.

## 7.6.8 TEED FEEDER APPLICATIONS

Distance protection can be applied to protect three terminal lines (teed feeders). Interconnecting three terminals, however, affects the apparent impedances seen by the distance elements and creates certain problems.

Consider, as an example, the following figure which represents a teed feeder with terminals A, B, and C, with a fault applied near to terminal B:

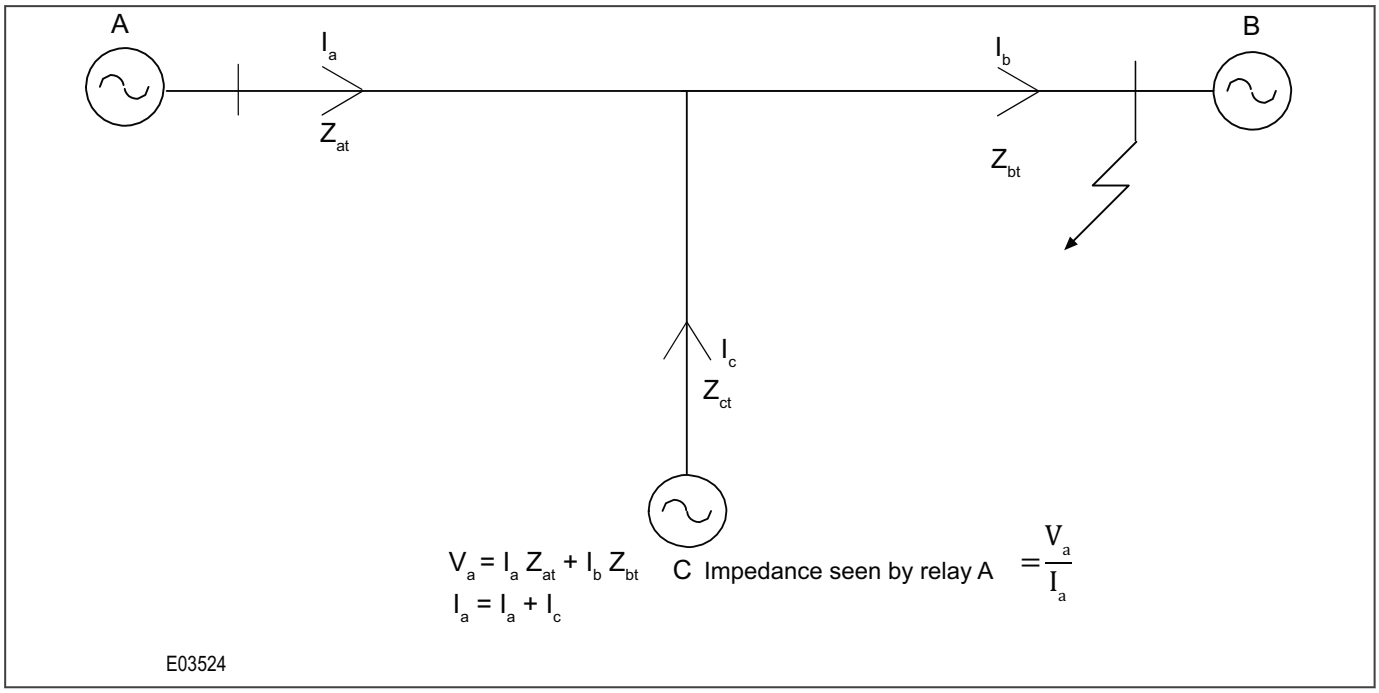



**Figure 120: Apparent Impedances seen by Distance Protection on a Teed Feeder**

The impedance seen by the distance elements at terminal A is given by:

$$Za = Zat + Zbt + [Zbt.(Ic/Ia)]$$

For faults beyond the Tee point, with infeed from terminals A and C, the distance elements at A (and C) will underreach. If terminal C is a relatively strong source, the underreaching effect at A can be substantial. If Zone 2 was set to a typical value of 120% of line AB, the element may fail to operate for internal faults. To compensate, the Zone 2 element must be set to further overreach by a factor which takes into account the effect of the infeed from the tee-point.

So, if infeed is present on a teed circuit, all Zone 2 elements should be set to overreach both of their remote terminals by a factor which takes into account the effect of the infeed from the tee-point.

Like overreaching of Zone 2 elements, underreaching of Zone 1 elements must also be assured. Zone 1 elements at each terminal must be set to underreach the true impedance to their nearest terminal (limiting case = no infeed to the tee-point - hence no overreach contribution).

Changing the reach requirements to match the infeed expectations is possible using the alternative setting group feature. Tailoring setting group contents to the different conditions, coupled with appropriate setting group switching, enables the changing reach requirements to be met.

Carrier aided schemes can also be used in conjunction with distance elements to protect teed feeders. Although Permissive Overreaching and Permissive Underreaching schemes may be used, they suffer some limitations. Blocking schemes are generally considered to be the most suitable.

#### 7.6.8.1 POR SCHEMES FOR TEED FEEDERS

A Permissive Overreach (POR) scheme requires the use of two signalling channels between each pair of terminals. On a teed feeder, a permissive trip is issued only if local Zone 2 operation is accompanied by receipt of signals from both remote terminals. The 'AND' function of received signals can either be implemented using external logic, or within the internal Programmable Scheme Logic (PSL).

To ensure operation for internal faults in a POR scheme, the protection at each of the three terminals should be able to see a fault anywhere on the protected feeder. This may demand very large Zone 2 reach settings to address the apparent impedances seen by the Distance elements.

Although POR schemes are feasible for teed feeders, the signalling requirements and the very large Zone 2 settings can make its use unattractive.

#### 7.6.8.2 PUR SCHEMES FOR TEED FEEDERS

For a Permissive Underrreaching (PUR) scheme, the signalling channel is only keyed for internal faults. The channel is keyed by Zone 1 operation. Aided tripping will occur at a receiving terminal if its overreaching Zone 2 setting requirements have been met.

On teed feeder applications, a permissive trip is issued at a terminal if that terminal’s Zone 2 operation is accompanied by receipt of a signal from EITHER remote terminal. This makes the signalling channel requirements for a PUR scheme less demanding than for a Permissive Overreach (POR) scheme. Either a common power line carrier (PLC) signalling channel or a triangulated signalling arrangement can be used, making a PUR scheme generally more attractive than a POR scheme for protecting for a teed feeder.

It must be recognised, however, that there are cases where instantaneous tripping will not occur with PUR schemes. The following figure illustrates three cases for which delayed tripping will occur:

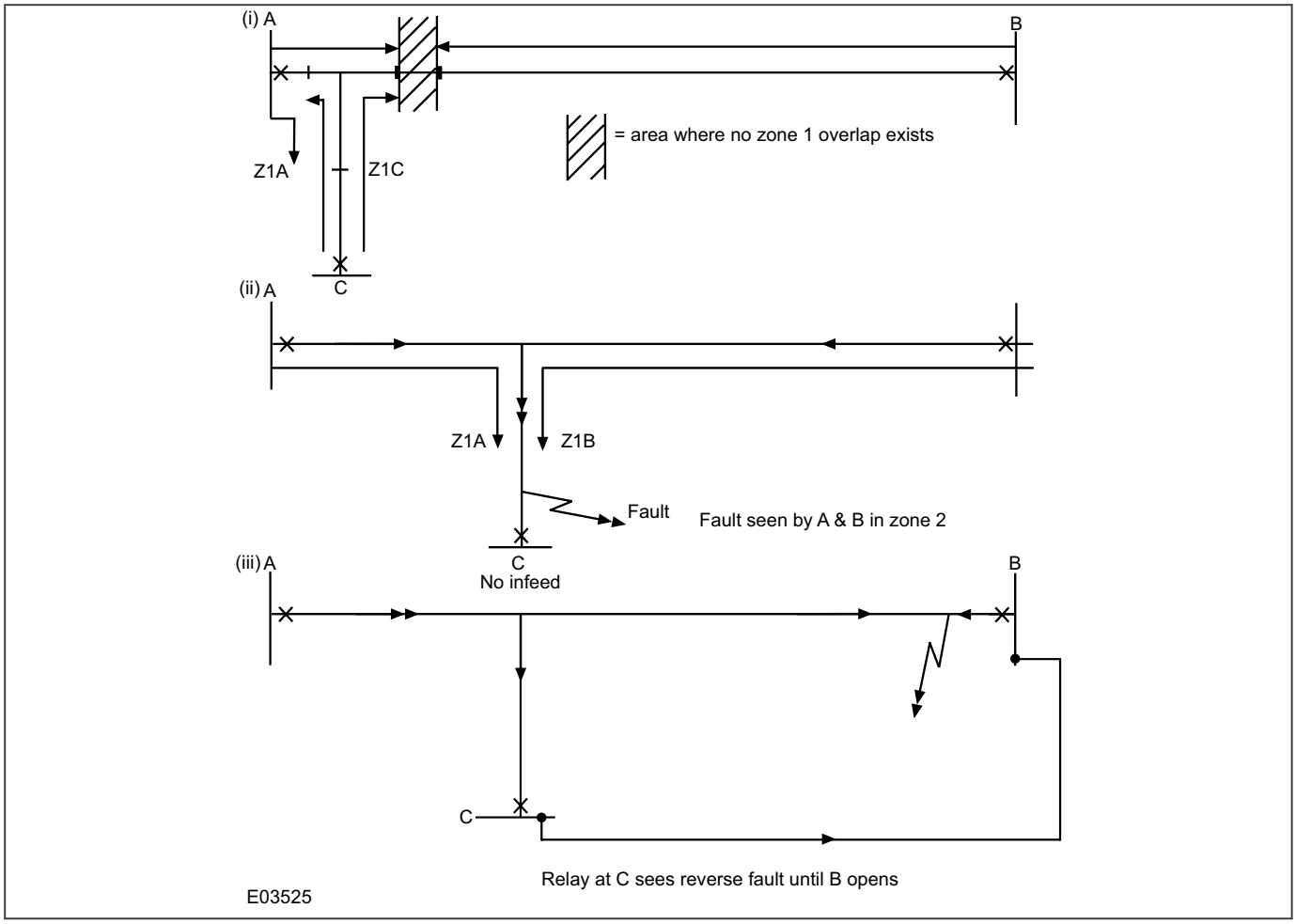



**Figure 121: Problematic Fault Scenarios for PUR Scheme Application to Teed Feeders**

- Scenario (i) shows a short tee connected to one nearby terminal and one distant terminal. In this case, Zone 1 elements set to 80% of the shortest connected feeder length don't all overlap, resulting in a section not covered by any Zone 1 element. Any fault in this section would rely on delayed Zone 2 tripping.
- Scenario (ii) shows an example where terminal C has no infeed. Distance elements at C may not operate for faults close to the terminal. As the fault is outside the Zone 1 reaches of A and B, clearance will rely on delayed Zone 2 tripping at A and B.
- Scenario (iii) shows an example where outfeed from terminal C feeds an internal fault via terminal B. In this case, terminal C will not see the fault until the breaker at B has operated. The result would be sequential (and hence delayed) tripping.

### 7.6.8.3 BLOCKING SCHEMES FOR TEED FEEDERS

With Blocking schemes, high speed operation can be achieved for circuits where there is no current infeed from one or more terminals. This makes Blocking schemes particularly suitable for protection of teed feeders. The scheme also has the advantage that the signalling requirement can be realised with one simplex channel.

*Note:*
*Triangulated simplex channels could be used in place of a common simplex one if prefered.*

As with Permissive Underreaching (PUR) schemes, a limitation of a Blocking scheme implementation is a scenario where outfeed from one terminal feeds an internal fault via another terminal. The terminal with the outfeed sees a

reverse fault condition. This results in a blocking signal being sent to the two remote terminals. Although the fault will be cleared, tripping will be prevented until the Zone 2 time delay has expired.

# CHAPTER 8

# NON-AIDED SCHEMES

# 8.1 CHAPTER OVERVIEW

This chapter describes the distance schemes that do not require communication between the ends (Non-Aided Schemes).

This chapter contains the following sections:

Chapter Overview 211
Non-Aided Schemes 212
Basic Schemes 213
Trip On Close Schemes 217
Zone1 Extension Scheme 222
Loss of Load Scheme 223

## 8.2 NON-AIDED SCHEMES

This product provides Distance protection. The Distance protection has been designed for use as a standalone non-unit protection, or for use with communications systems to provide unit protection (Carrier Aided schemes).

Standalone operation provides basic scheme Distance protection (e.g. instantaneous Zone 1 operation, delayed Zone 2 protection and further delayed Back-up protection, etc.). It also implements some special standalone schemes that don't require communications. These are known as Non-Aided Distance Schemes.

The non-aided schemes provided in this product can be divided into the following categories:

- Basic schemes
- Trip On Close schemes
- Zone 1 Extension scheme
- Loss of Load scheme

The settings for these Non-Aided Distance Schemes are located in the *SCHEME LOGIC* column.

## 8.3 BASIC SCHEMES

Basic Scheme operation is always executed if distance elements are enabled. It is the process by which the measured line impedance is compared against the Distance measuring zone configuration (reach settings and timers). Instantaneous or time delayed tripping or blocking signals may be issued for a specific zone according to its settings and the measured impedance values.

There are six basic scheme zones; Zone 1, Zone 2, Zone 3, Zone 4, Zone P and Zone Q.

The Basic Scheme settings include:

- A mode setting, which is common to all zones
- Zone Tripping settings for each zone
- Zone phase delay settings for each zone
- Zone ground delay settings for each zone

On a per-zone basis, phase and earth-fault elements may be set to have different time delays.

To supplement Basic Scheme operation, there are also standalone scheme designs (Non-Aided Distance Schemes) that provide timely clearance for particular fault scenarios where carrier aided signalling is either not available, or is unnecessary. These scenarios cover Trip on Closure (including Switch On to Fault, and Trip on Reclose), Loss of Load, and Zone1 Extension.

The Basic Scheme is continually executed, regardless of any carrier-aided acceleration schemes which may be enabled.

### 8.3.1 BASIC SCHEME MODES

The operation of distance zones according to their set time delays is called the basic scheme. The basic scheme always runs, regardless of any channel-aided acceleration schemes which may be enabled.

The ***BasicScheme Mode*** setting defines how the timers associated with the different Distance zones in the Basic Scheme are initiated by pick up (start) of zone elements.

In *Standard* mode, a zone timer starts only when the corresponding distance zone start occurs.

In *Alternative* mode, if a condition causes any of the enabled Distance elements to start, then the ***Any Distance Start*** DDB signal is asserted. This starts the timers associated with all enabled zones (phase zone timers and earth zone timers are started). The timers are reset if the ***Any Distance Start*** signal resets. If a Distance zone measuring element is picked up when its associated zone timer times-out, a trip is issued for that zone element.

The *Alternative* mode is especially suitable for evolving faults, since all zone timers will be initiated at initial fault inception, rather than waiting to start a timer as additional phases become faulted. This minimises the overall fault clearance time as the fault develops.

The two modes are described by the following logic diagrams.

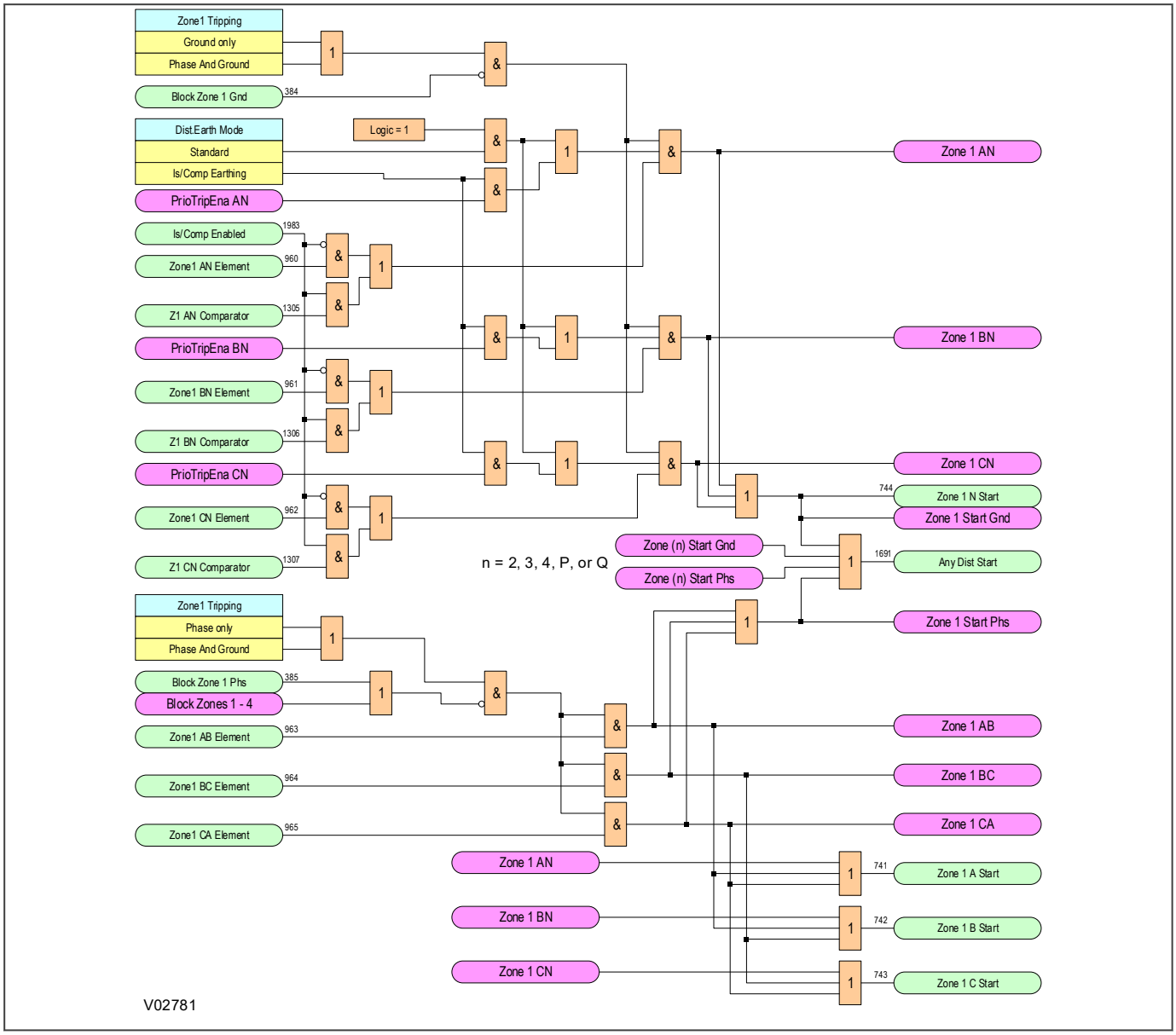



**Figure 122: Zone Starting Logic**

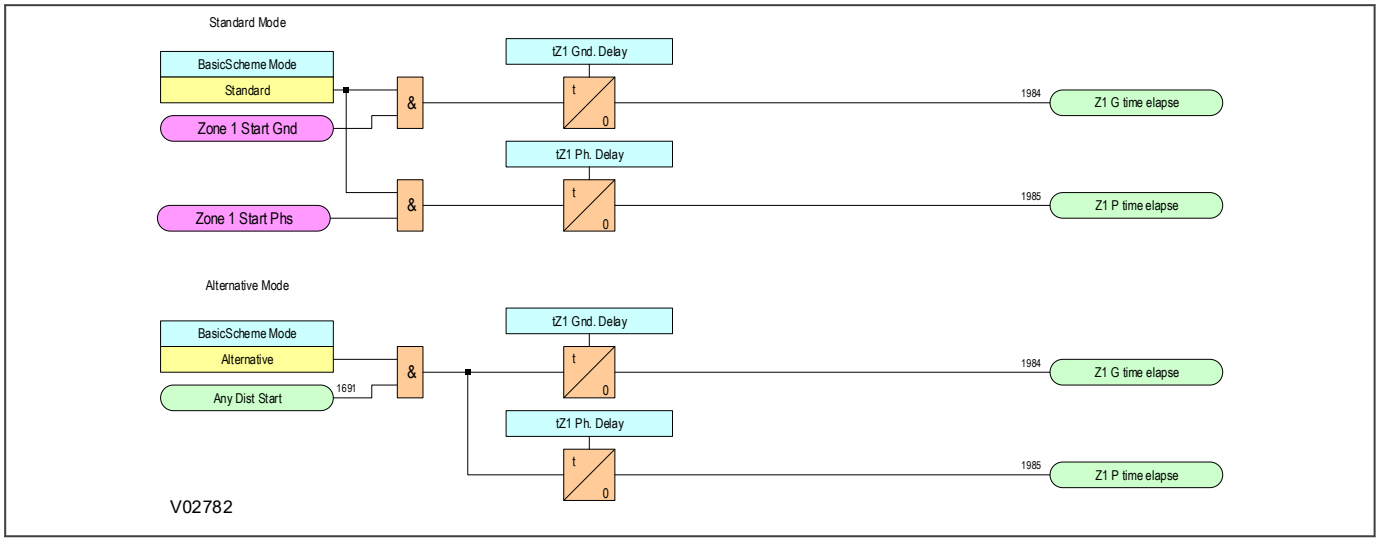



**Figure 123: Zone timer logic**

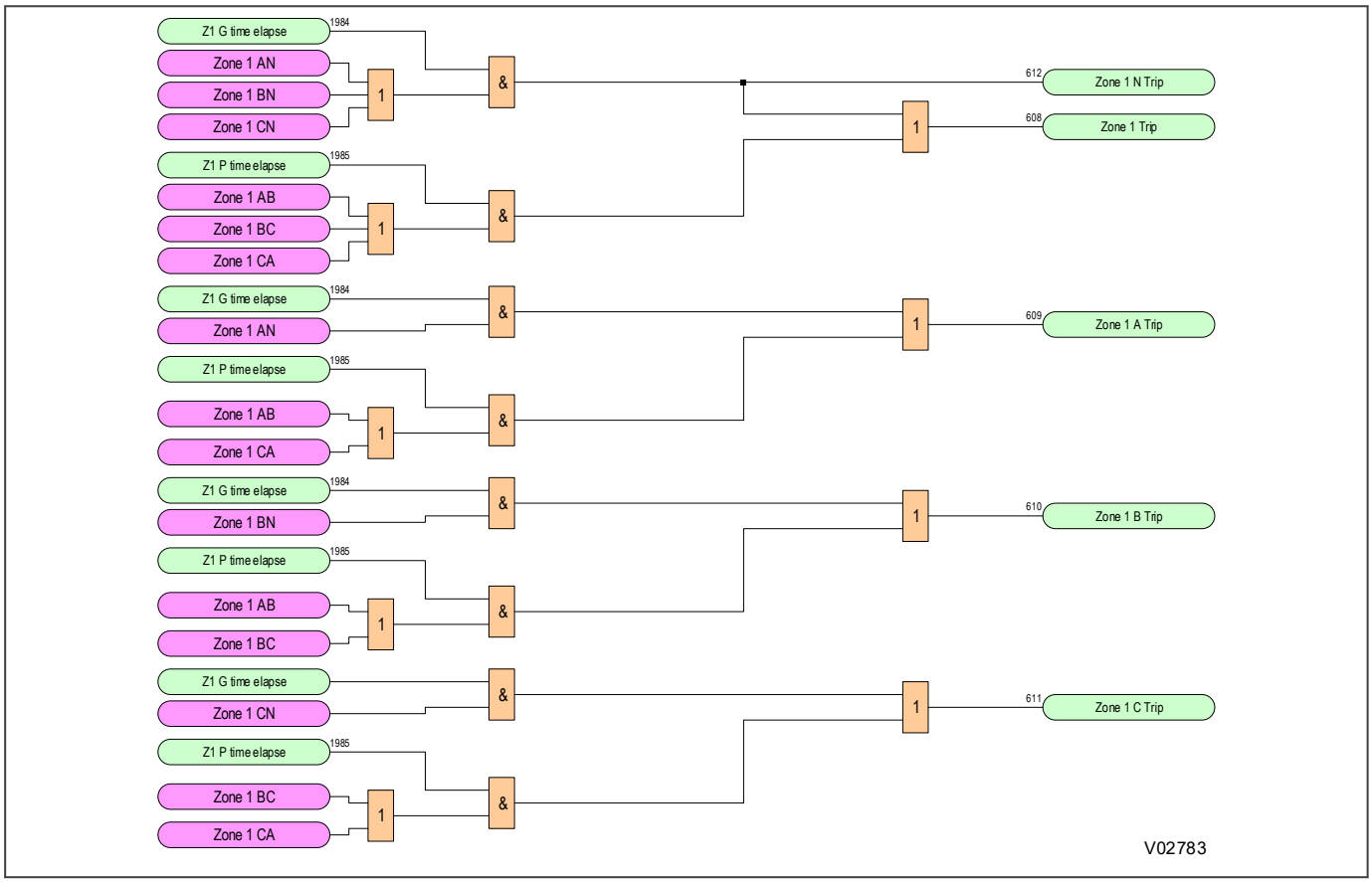



**Figure 124: Zone trip logic**

## 8.3.2 BASIC SCHEME SETTING

The Zone 1 time delay (tZ1) is generally set to zero, giving instantaneous operation.

The Zone 2 time delay (tZ2) is set to co-ordinate with Zone 1 fault clearance time for adjacent lines. The total fault clearance time consists of the downstream Zone 1 operating time plus the associated breaker operating time. Allowance must also be made for the Zone 2 elements to reset following clearance of an adjacent line fault and also for a safety margin. A typical minimum Zone 2 time delay is of the order of 200 ms.

The Zone 3 time delay (tZ3) is typically set with the same considerations made for the Zone 2 time delay, except that the delay needs to co-ordinate with the downstream Zone 2 fault clearance. A typical minimum Zone 3 operating time would be in the region of 400 ms.

The Zone 4 time delay (tZ4) needs to coordinate with any protection for adjacent lines in the protection's reverse direction.

Separate time delays can be applied to both phase and ground fault zones, for example where ground fault delays are set longer to time grade with external ground/earth overcurrent protection.

Any zone (#) which may reach through a power transformer reactance, and measure secondary side faults within that impedance zone should have a small time delay applied. This is to avoid tripping on the inrush current when energizing the transformer.

As a general rule, if the Zone Reach setting is greater than 50% of the transformer reactance, set the Zone delay to be 100 ms or greater. Alternatively, the 2nd harmonic detector output (which is available in the Programmable Scheme Logic) may be used to block zones that may be at risk of tripping on inrush current. Settings for the inrush detector are found in the *SUPERVISION* column.

The figure below shows the typical application of the Basic scheme.

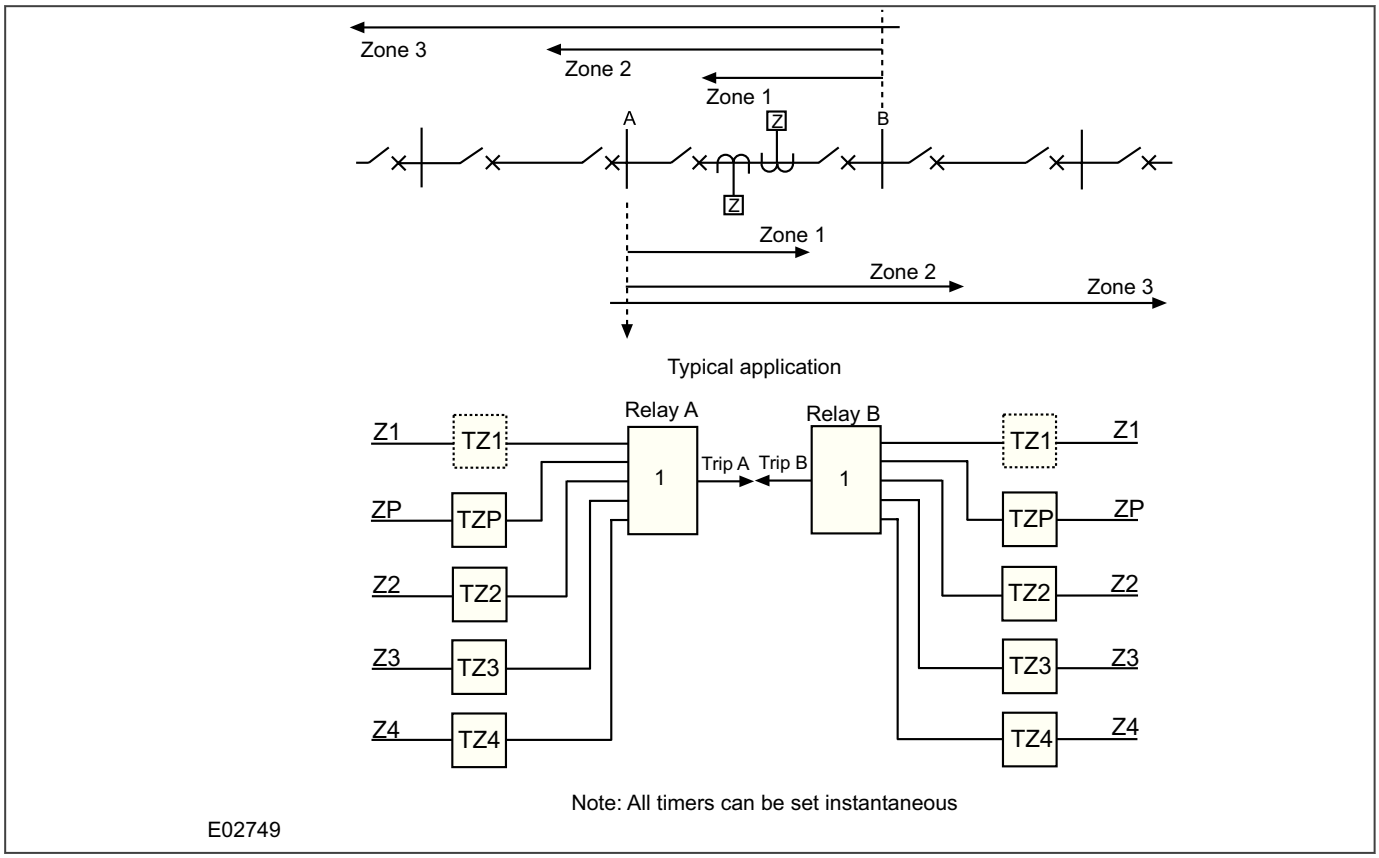



**Figure 125: Basic time stepped distance scheme**

## 8.4 TRIP ON CLOSE SCHEMES

Logic is provided for situations where special tripping may be necessary following closure of the associated circuit breaker. Two cases of Trip on Close (TOC) logic are catered for:

- Switch on to Fault (SOTF)
- Trip on Reclose (TOR)

SOTF provides instantaneous operation of selected elements if a fault is present when manual closure of the circuit breaker is performed.

TOR provides instantaneous operation of selected elements if a persistent fault is present when the circuit breaker attempts autoreclosure

The SOTF and TOR functions are known as Trip on Close logic. Both methods operate in parallel if mapped to the SOTF and TOR Tripping matrix in the setting file.

The settings for Switch on to Fault (SOTF) and Trip on Reclose (TOR) are located in the *TRIP ON CLOSE* section of the *SCHEME LOGIC* column.

SOTF and TOR are complemented by Current No Voltage level detectors (also known as CNV level detectors). These CNV level detectors are set using the voltage and current settings located in the *CB FAIL & P.DEAD* column. The same settings are used for pole dead logic detection. A 10ms time delay in the logic avoids a possible race between very fast overvoltage and undercurrent level detectors.

The following figures show the Trip On Close function in relation to the Distance zones and the Trip On Close function when driven by Current No Volt level detectors.

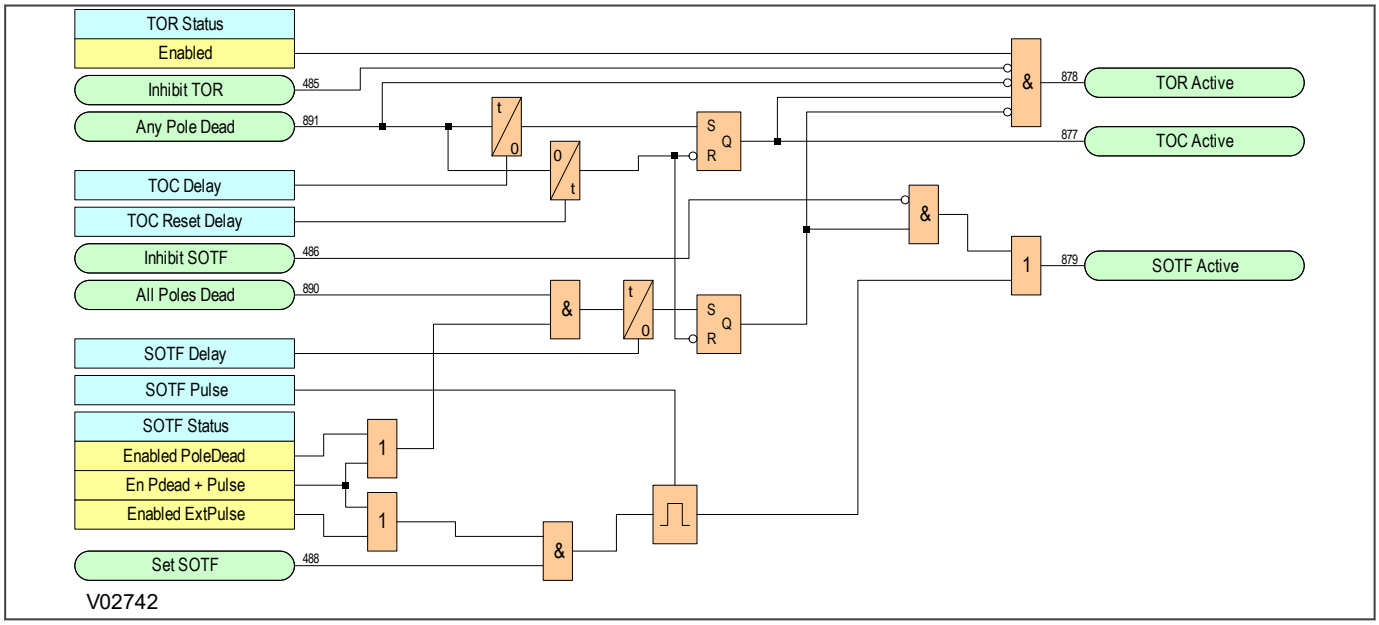



**Figure 126: Trip On Close logic**

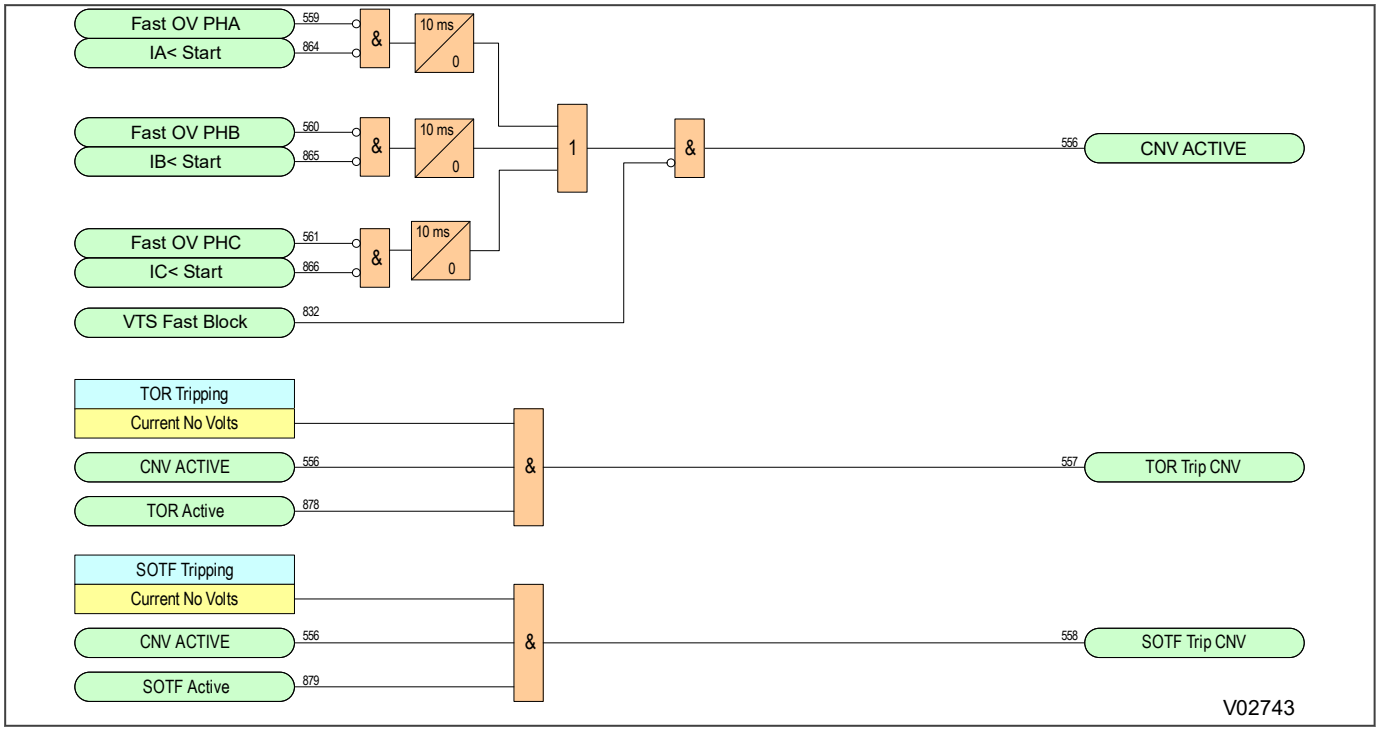



**Figure 127: Trip On Close based on CNV level detectors**

## 8.4.1 SWITCH ON TO FAULT (SOTF)

You can use the ***SOTF Status*** setting to activated SOTF in in three different ways. It can be:

- Enabled using the pole dead detection logic. If an 'All Pole Dead' condition is detected, the ***SOTF Delay*** timer starts. Once this timer expires, SOTF is enabled and stays active for the period set in the ***TOC Reset Delay*** setting.
- Enabled by an external pulse. SOTF is enabled after an external pulse linked to DDB ***Set SOTF*** is ON. The external pulse could be a circuit breaker close command, for example. The function stays active for the duration of the ***SOTF Pulse*** setting.
- Enabled using both pole dead detection logic and an external pulse.

Three pole instantaneous tripping (and auto-reclose blocking) occurs for any fault detected by the selected zones or Current No Volt level detectors when in SOTF mode. Whether this feature is enabled or disabled, the normal time delayed elements or aided channel scheme continues to function and can trip the circuit.

The ***SOTF Delay*** is a pick up time delay that starts after opening all three poles of a circuit breaker (CB). If the CB is then closed after the set time delay has expired, SOTF protection is active. SOTF provides enhanced protection for manual closure of the breaker (not for auto-reclosure). This setting is visible only if `Enabled PoleDead` or `En Pdead + Pulse` are selected to enable SOTF.

While the Switch on to Fault Mode is active, the protection trips instantaneously for pick up of any zone selected in these links. To operate for faults on the entire circuit length, you should select at least Zone 1 and Zone 2 using the SOTF Tripping setting . If no elements are selected, the normal time delayed elements and aided scheme provide the protection.

A user settable time window during which the SOTF protection is available through the ***SOTF Pulse*** setting This setting is visible only if `Enabled ExtPulse` or `En Pdead + Pulse` are selected to enable SOTF.

### 8.4.1.1 SWITCH ONTO FAULT MODE

To ensure fast isolation of faults (for example a closed three phase earthing switch), on energisation enable this feature with appropriate zones or Current No Volt (CNV) level detectors, depending on utility practices.

When busbar voltage transformers are used, the ***Pole Dead*** signal is not produced. Connect circuit breaker auxiliary contacts for correct operation. This is not necessary if the SOTF is activated by an external pulse.

- ***SOTF Delay***: The time chosen should be longer than the slowest delayed-auto-reclose dead time, but shorter than the time in which the system operator might re-energise a circuit once it had opened/tripped. We recommend 110 seconds as a typical setting.
- ***SOTF Pulse***: Typically this could be set to at 500ms. This time is enough to establish completely the voltage memory of distance protection.
- ***TOC Reset Delay***: We recommend 500ms as a typical setting (chosen to be in excess of the 16 cycles length of memory polarizing, allowing full memory charging before normal protection resumes).

### 8.4.1.2 SOTF TRIPPING

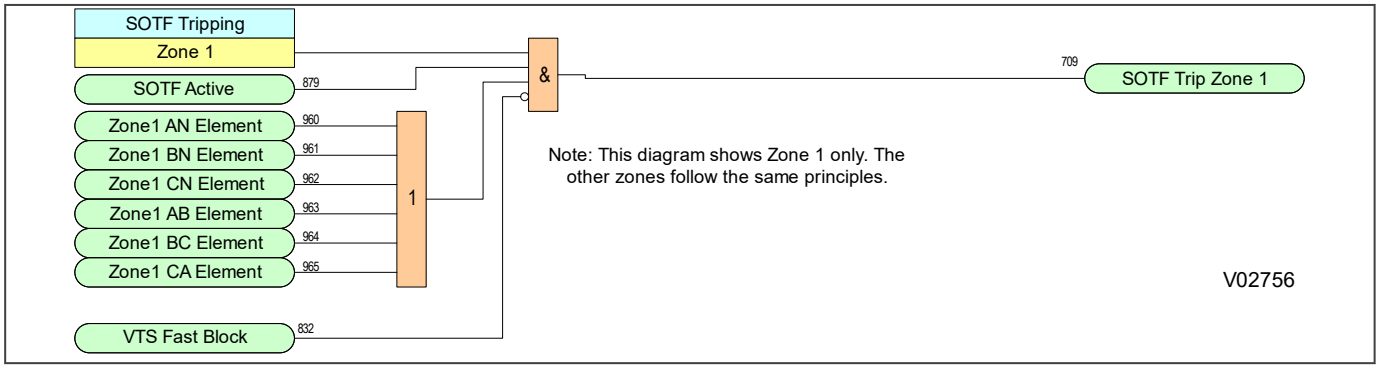



**Figure 128: SOTF Tripping**

### 8.4.1.3 SOTF TRIPPING WITH CNV

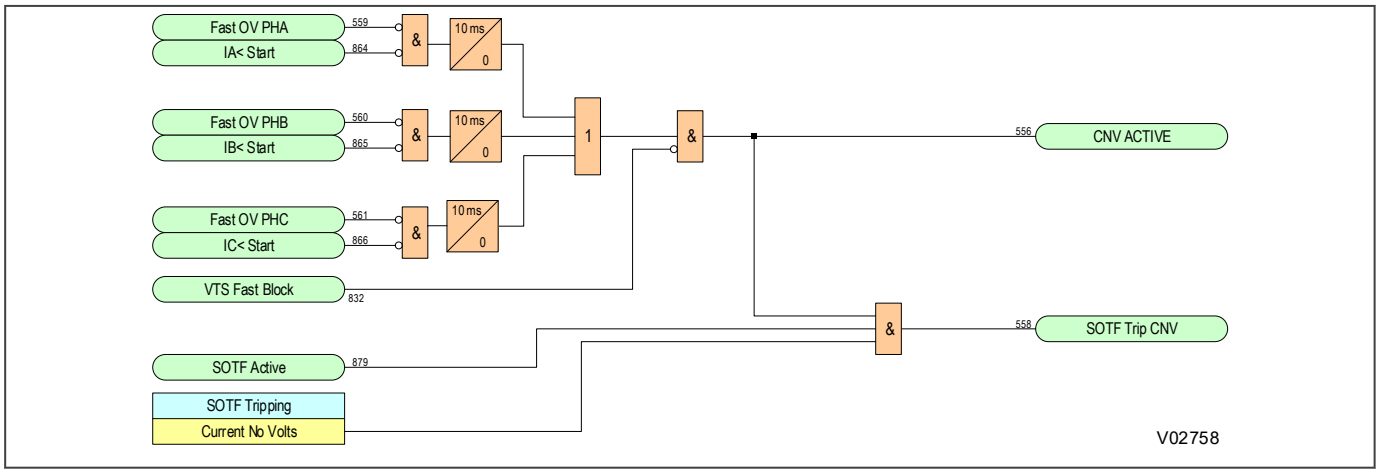



**Figure 129: SOTF Tripping with CNV**

## 8.4.2 TRIP ON RECLOSE (TOR)

Trip On Reclose (TOR) is special protection following auto-reclosure. The ***TOR status*** setting is used to enable or disable TOR. When enabled, TOR is activated after the TOC Delay expires, ready for application when an auto-reclose shot occurs.

When this feature is enabled, the protection operates in 'Trip on Reclose mode' for a period following circuit breaker (CB) closure. Three-phase instantaneous tripping occurs for any fault detected by the selected zones or CNV level detectors. Whether this feature is enabled or disabled, the normal time-delayed elements or aided channel scheme continue to function and can trip the circuit.

The SOTF and TOR features stay in service for the duration of the ***TOC Reset Delay*** time, once the circuit is energised. The delay timer starts on CB closure and is common for SOTF and TOR protection. Once this timer expires after successful closure, all protection reverts to normal.

A user settable time delay (***TOC Delay***) starts when the CB opens, after which TOR is enabled. The time delay must not exceed the minimum Dead Time setting of the auto-reclose because both times start simultaneously and TOR protection must be ready by the time the CB closes on potentially persistent faults.

While the Trip on Reclose Mode is active, the protection trips instantaneously for pick up of any selected Distance zone. You select the zone with the ***TOR Tripping*** setting. For example, Zone 2 could operate without waiting for the usual time delay if a fault is in Zone 2 on CB closure. Also Current No Volts can be mapped for fast fault clearance on line reclosure on a permanent fault. To operate for faults on the entire circuit length, at least Zone 1 and Zone 2 should be selected. If no elements are selected, the normal time delayed elements and aided scheme provide the protection. TOR tripping is three-phase and auto-reclose is blocked.

### 8.4.2.1 TRIP ON RECLOSE MODE

To ensure fast isolation of all persistent faults following the circuit breaker reclosure, enable this feature with appropriate zones selected or Current No Volt (CNV) level detectors.

- ***TOC Delay***: The Trip on Reclose (TOR) is activated after ***TOC Delay*** has expired. The setting must not exceed the minimum autoreclose ***Dead Time*** setting to make sure that the TOR is active immediately on reclose command.
- ***TOC Reset Delay***: We recommend 500ms as a typical setting.

### 8.4.2.2 TOR TRIPPING LOGIC FOR APPROPRIATE ZONES

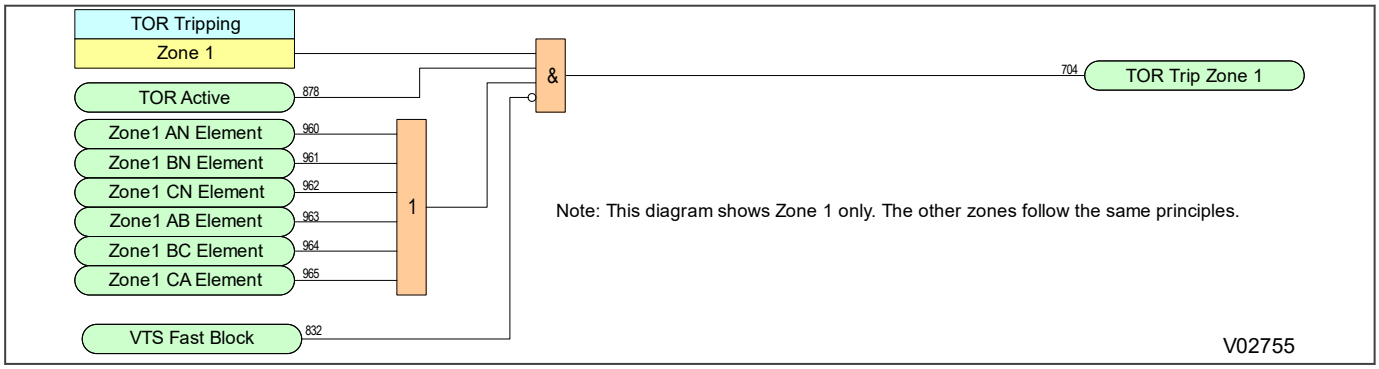



**Figure 130: TOR Tripping logic for appropriate zones**

### 8.4.2.3 TOR TRIPPING LOGIC WITH CNV

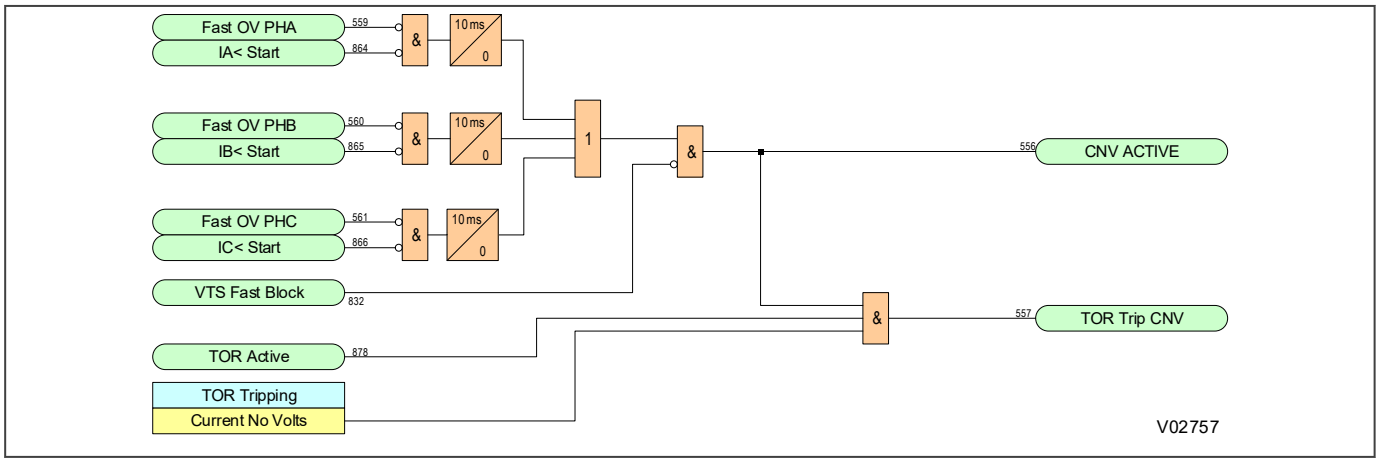



**Figure 131: TOR Tripping logic with CNV**

## 8.4.3 POLARISATION DURING CIRCUIT ENGERGISATION

While the Switch on to Fault (SOTF) and Trip on Reclose (TOR) modes are active, the directionalised distance elements are partially cross polarised from other phases. The same proportion of healthy phase to faulted phase voltage, as given by the ***Dist. Polarizing*** setting in the *DISTANCE SETUP* menu, is used.

Partial cross polarisation is therefore substituted for the normal memory polarising, for the duration of the ***TOC Delay***. If insufficient polarising voltage is available, a slight reverse offset (approximately 25% of the forward reach) is included in the Zone 1 characteristic to enable fast clearance of close up three-phase faults.

## 8.5 ZONE1 EXTENSION SCHEME

Auto-reclosure is widely used on radial overhead line circuits to re-establish supply following a transient fault. A Zone 1 extension scheme may be applied to a radial overhead feeder to provide high speed protection for transient faults along the whole of the protected line. The figure below shows the alternative reach selections for zone 1: Z1 or the extended reach Z1X.

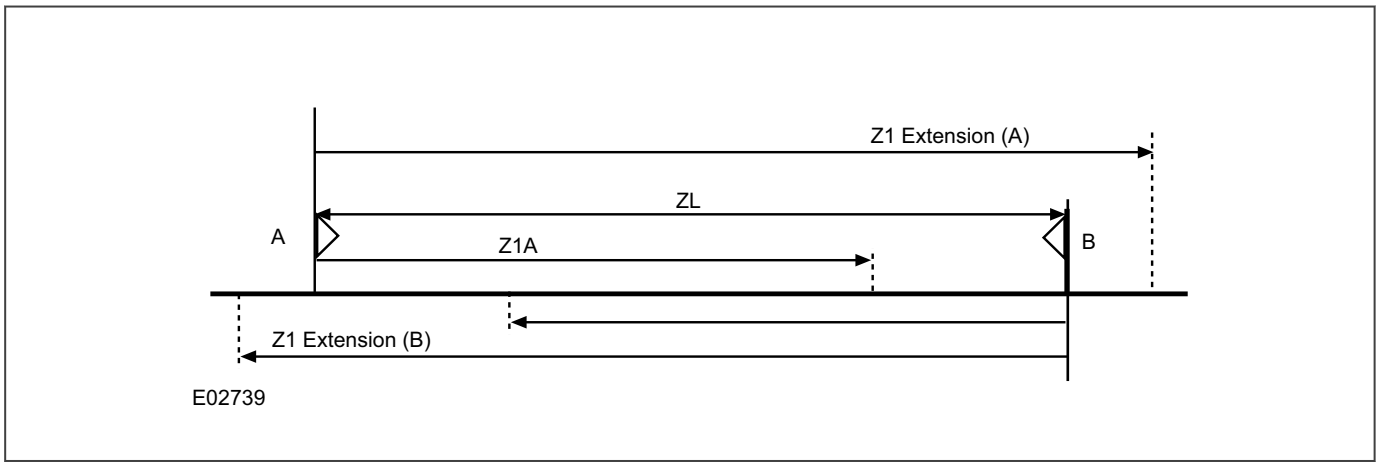



**Figure 132: Zone 1 extension scheme**

In this scheme Zone 1X is enabled and set to overreach the protected line. A fault on the line, including one in the end 20% not covered by Zone 1, results in instantaneous tripping followed by autoreclosure. Zone 1X has resistive reaches and residual compensation similar to Zone 1. The autorecloser is used to inhibit tripping from Zone 1X so that on reclosure the device operates with Basic scheme logic only, to co-ordinate with downstream protection for permanent faults. Therefore transient faults on the line are cleared instantaneously, which reduces the probability of a transient fault becoming permanent. However, the scheme can operate for some faults on an adjacent line, although this is followed by autoreclosure with correct protection discrimination. Increased circuit breaker operations would occur, together with transient loss of supply to a substation.

| Fault trip | Z1X time delay |
|---|---|
| First fault trip | = tZ1 |
| Fault trip for persistent fault on auto-reclose | = tZ2 |

The Zone 1 extension scheme can be disabled, permanently enabled or just brought into service when the communication channel fails and the aided scheme is inoperative. If used in conjunction with a channel-aided scheme, Z1X can be set to be enabled when Ch1 or Ch2 fails, or when all channels fail, or when any channel fails.

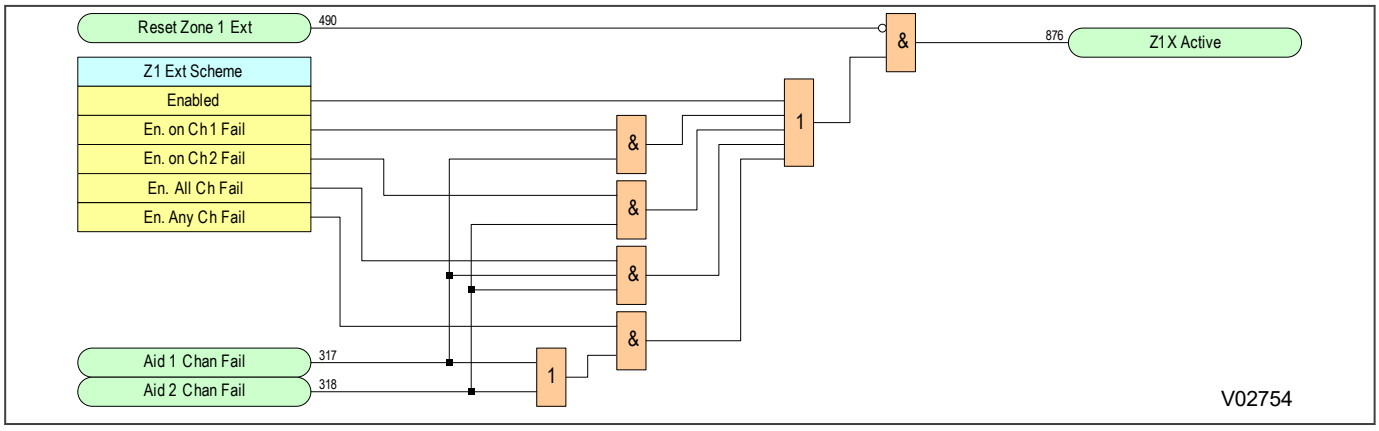



**Figure 133: Zone 1 extension logic**

## 8.6 LOSS OF LOAD SCHEME

The Loss of Load Scheme provides fast unit protection performance for most fault types occurring on a double-end fed line or feeder, but it does not need communications.

It is used on circuits that are designed for three-pole tripping, and provides protection for faults involving one or two phases. It is not suitable for single-pole tripping applications, and it cannot protect against three-phase faults.

The scheme does not require communications, but it can be used alongside carrier aided schemes if communications are available.

The Loss-of-Load scheme can be permanently enabled, permanently disabled, or enabled if communication failure compromises channel-aided scheme operation. If used in conjunction with a channel-aided scheme, loss of load can be set to be enabled if only Channel 1 fails, or if only Channel 2 fails, or if both channels fail, or if either channel fails. Aided scheme communication failure is detected by permissive scheme unblocking logic, or the presence of a Channel Out of Service (COS) input.

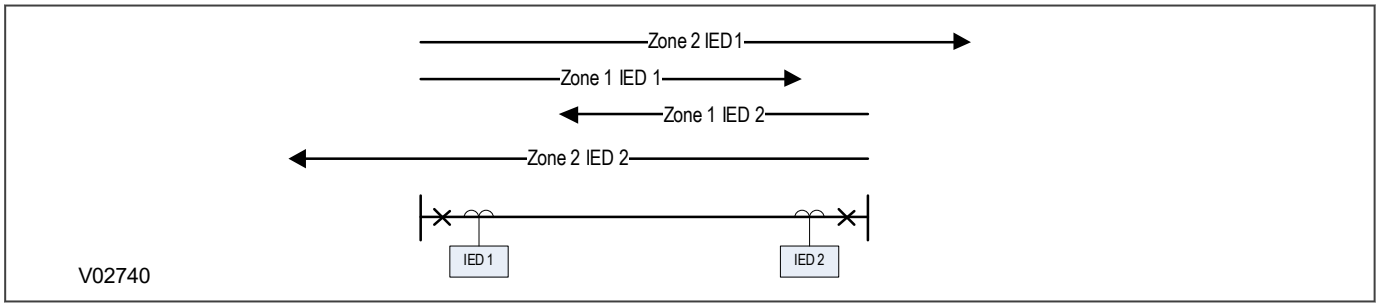



**Figure 134: Loss of load accelerated trip scheme**

Any fault in the reach of Zone 1 results in fast tripping of the local circuit breaker. For an end zone fault for IED 1 (near IED 2) with remote infeed (from IED 2), the remote breaker is tripped in Zone 1 by the remote device at IED 2. The local device (IED 1) can recognise this by detecting loss of load current in the healthy phases. This condition, in conjunction with operation of a Zone 2 comparator at IED 1P, can be used to trip the local circuit breaker.

Before an accelerated trip can occur, load current must be detected before the fault. The loss of load current opens a window during which time a trip occurs if a Zone 2 comparator operates. A typical setting for this window is 40ms as shown in the figure below, although this can be altered in the ***LoL Window*** setting. The accelerated trip is delayed by 18ms to prevent initiation of a loss of load trip due to circuit breaker pole discrepancy occurring for clearance of an external fault. The local fault clearance time can be deduced as follows:

$$t = Z1d + 2CB + LDr + 18ms$$

where:

- Z1d = Maximum downstream zone 1 trip time
- CB = Breaker operating time
- LDr = Upstream level detector (***LOL <1***) reset time

For circuits with load tapped off the protected line, care must be taken in setting the loss of load feature to ensure that the undercurrent level detector setting is above the tapped load current. When selected, the loss of load feature operates with the main distance scheme that is selected. This provides high speed clearance for end zone faults when the Basic scheme is selected or, with permissive signal aided tripping schemes, it provides high speed back up clearance for end zone faults if the channel fails.

*Note:*
*Loss of load tripping is only available where three pole tripping is used.*

*Note:*
*Assertion of the **Any Trip** DDB signal or the **Inhibit LOL** DDB signal will prevent LOL tripping.*

The detailed Loss of Load logic diagram is shown below:

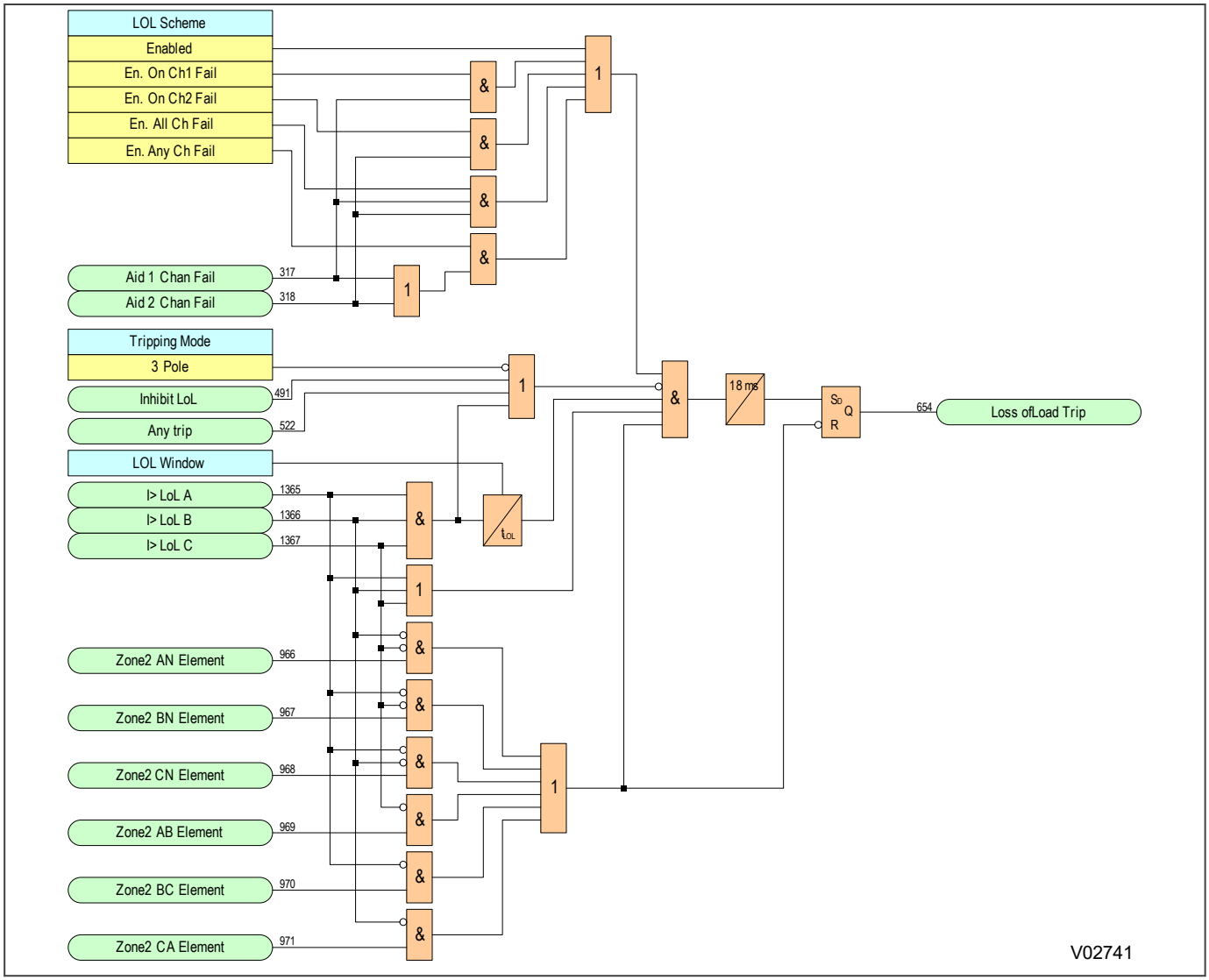



**Figure 135: Loss of Load Logic**

CHAPTER 9

# POWER SWING FUNCTIONS

## 9.1 CHAPTER OVERVIEW

This chapter describes special blocking and protection functions, which use Power swing Analysis.

This chapter contains the following sections:

Chapter Overview 226
Introduction to Power Swing Blocking 227
Power Swing Blocking 229
Out of Step Protection 240

## 9.2 INTRODUCTION TO POWER SWING BLOCKING

Power swings are variations in power flow that occur when the voltage phase angles at different points of generation shift relative to each other. They can be caused by events such as fault occurrences and subsequent clearance. Power swings may be classified as stable or unstable.

A stable power swing is one where, following a disturbance, all sources of generation return to a state where they are all generating synchronous voltages. An unstable power swing is one where at least one source of generation cannot restore operation that is synchronous with the rest of the system. In this case the poles of one source of generation slip with respect to those of another. This condition is known as Pole Slipping.

A power swing may cause the impedance presented to Distance protection to move away from the normal load area and into one or more of its tripping characteristics. Without attention this could lead to unwanted or uncontrolled tripping.

*Note:*
*Power swings do not involve earth, so only phase-phase impedances are affected.*

For stable power swings, distance protection should not trip. To prevent tripping, a Power Swing Blocking (PSB) function is usually provided to compliment Distance protection.

For unstable power swings, there may be a strategy for instigating a controlled system split. In this case, distance protection should not trip during loss of stability. If unstable power swings or Pole-Slipping conditions might be expected, certain points on the network may be designated as split points, where the network should be split if unstable (or potentially unstable) conditions occur. Strategic splitting of the system can be achieved by means of dedicated Out-of-Step Tripping protection (OOS or OST protection). Or it may be possible to achieve splitting by strategically limiting the duration for which the operation of a specific distance protection is blocked during power swing conditions.

A method often used to help understand power system stability and Pole Slipping is called Equal Area Criterion. This is based on a number of operational curves as outlined in the figure below:

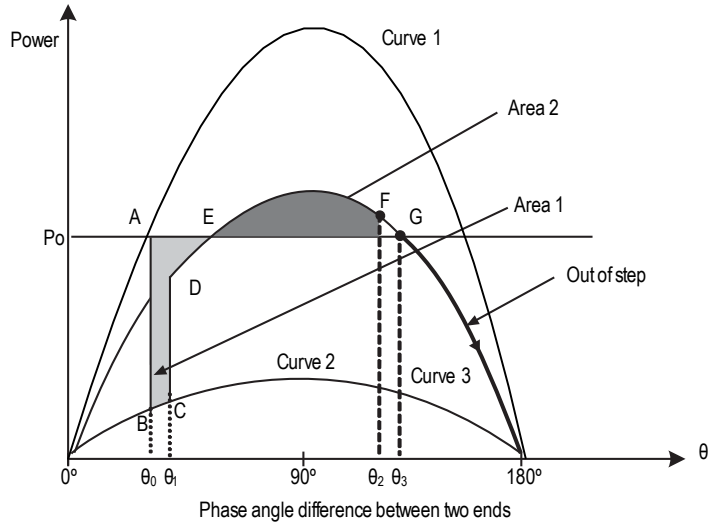



**Figure 136: Power transfer related to angular difference between two generation sources**

The figure describes the behaviour of a power system with parallel lines connecting two sources of generation.

- Curve 1 represents pre-fault system operation through parallel lines where the transmitted power is Po.
- Curve 2 represents transmitted power during a phase-phase-earth fault.
- Curve 3 represents a new power curve when the faulted line is tripped.

At fault inception, the operating point A moves to B, which is a reduced power transfer level. There is, therefore, a surplus of power (A to B) at that sending end and a corresponding deficit of power at the receiving end. The sending end generators start to speed up, and the receiving end generators start to slow down, so the phase angle θ increases, and the operating point moves along curve 2 until the fault is cleared (point C). At this point, the phase angle is θ1. The operating point now moves to point D on curve 3 which represents the power transfer curve when just one line is in service. There is still a power surplus at the sending end and a deficit at the receiving end, so the generators continue to lose synchronism and the operating point moves further along curve 3.

If, at some point between E and G (point F) the generators are rotating at the same speed, the phase angle will stop increasing. According to the Equal Area Criterion, this occurs when Area 2 is equal to Area 1. The sending end will now start to slow down and receiving end to speed up. Therefore, the phase angle starts to decrease and the operating point moves back towards E. As the operating point passes E, the net sending end deficit again becomes a surplus and the receiving end surplus becomes a deficit, so the sending end generators begin to speed up and the receiving end generators begin to slow down. With no losses, the system operating point will oscillate around point E on curve 3, but in practise the oscillation is damped, and the system eventually settles at operating point E.

So, if Area 1 is less than Area 2, the system will oscillate but will stay in synchronism. This swing is usually called a recoverable, or stable, power swing. If, on the contrary, the system passes point G with a further increase in angle difference between sending and receiving ends, the system loses synchronism and becomes unstable. This will happen if the initial power transfer Po is so high that the Area 1 is greater than Area 2. This power swing is not recoverable and is usually called an Out-of-Step condition or a Pole Slip condition. In such a case, only system separation and subsequent re-synchronising of the generators can restore normal system operation.

The point G is shown at approximately 120°, but this can vary. If, for example, the pre-fault transmitted power (Po) was high and the fault clearance was slow, Area 1 would be greater. For the system to recover from this case, the angle θ would be closer to 90º. Similarly, if the pre-fault transmitted power Po was low and fault clearance fast, Area 1 would be small, and the angle θ could go closer to 180º with the system remaining stable.

## 9.3 POWER SWING BLOCKING

A power swing may cause the impedance presented to the distance function to move away from the normal load area and into one or more of its tripping zones. Stable power swings should not cause the distance protection to trip. Therefore, if the power swing is deemed to be stable, the distance protection function for the zone in question is blocked. Unstable power swings should result in either tripping of the relevant protection element, or a system split. Therefore, the distance protection element should also be blocked for unstable power swings if there is a strategy for a controlled system split.

### 9.3.1 POWER SWING DETECTION

There are two power swing detection modes: *Advanced* and *Conventional*. You can set this with the ***Power Swing Mode*** setting.

Advanced mode provides 'settings-free' operation. This uses a superimposed current technique (also known as a delta technique). This technique is suitable for power swings in the normal to fast frequency range (>0.5Hz)

To detect slower power swings (<0.5Hz), a supplementary technique based on impedance characteristics is used. This so called slow swing technique will invoke the power swing blocking function should the power swing be to slow for the delta technique to operate. The impedance method uses zone 7 and zone 8 concentric quadrilateral impedance characteristics. Power swing detection is achieved by measuring the time taken for the impedance trajectory to cross through zone 8 into zone 7 (delta Z). In *conventional* mode, the impedance method is used for all power swings.

Once a power swing is detected the following actions occur:

- Relevant distance elements are blocked (if blocking is enabled).
- All zones are switched to self-polarised mho characteristics with 10% offset reach for maximum stability during the swing.

#### 9.3.1.1 SETTINGS-FREE POWER SWING DETECTION

By "Settings-Free", we mean that there is no need to define any characteristic criteria. The only settings needed are to define what to do in the event of a power swing (Allow trip, block, or unblock with a delay).

The settings-free power swing detection technique uses a superimposed current detector (ΔI), as used in the phase selector. For each phase loop (A-B, B-C, C-A), the actual measured current is compared with the measured current from exactly two cycles earlier (present in a 2-cycle FIFO buffer). If there is a difference between the two (ΔI), this indicates that something is happening on that current loop.

The superimposed current (ΔI) is compared with a set threshold (set at 5%In) to produce a switching signal PH1. This switching signal is used as an input to the power swing blocking function. It also triggers the current sample values in the 2-cycle FIFO butter to be stored in memory for further current comparisons.

Superimposed currents appear during both fault conditions, and power swings. For fault conditions, superimposed components will not normally extend beyond two cycles. Under power swing conditions however, superimposed components persist beyond two cycles. We can use this fact to differentiate between faults and power swings.

During a power swing (in the absence of a fault), the phase selector will indicate a three-phase selection, or a phase-phase selection if one pole is dead. So if superimposed components persist for three cycles, and a “faulted-phase” indication of “three-phase with one pole dead” is present during those three cycles, a power swing has been detected and the relevant signals are asserted.

After a power swing condition has been detected, the ΔI threshold used by the phase selector is increased and the current values present in the two cycle buffer are stored. This provides coverage for faults that might occur whilst a power swing is in progress.

For a fault condition, the superimposed current detector should reset after two cycles, because once the fault current values enter the FIFO buffer, this will be compared with the present fault current and the superimposed current will return to zero. This will allow the power swing detection function to reset.

### Configuring Settings-Free Power Swing Detection

The power swing detection based on superimposed current requires no system study. You just need to decide whether a zone should be blocked or allowed to trip if a power swing is detected. You do this zone by zone using the zone specific settings. For example the zone 1 setting is ***Zone 1 Ph. PSB***. The available options are *Blocking*, *Allow Trip*, or *Delayed Unblock*.

#### 9.3.1.1.1 TIMING OF THE PHASE SELECTOR SIGNALS

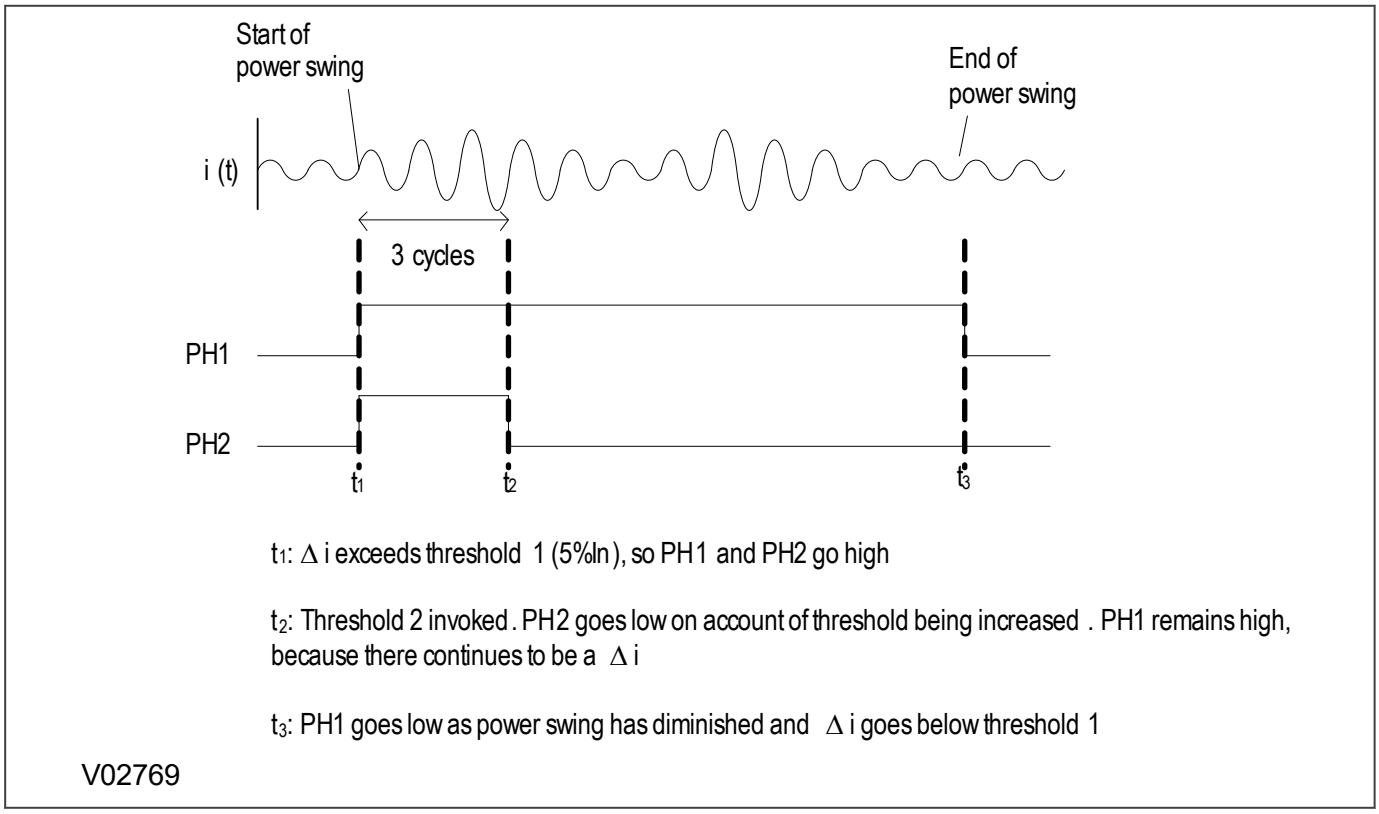
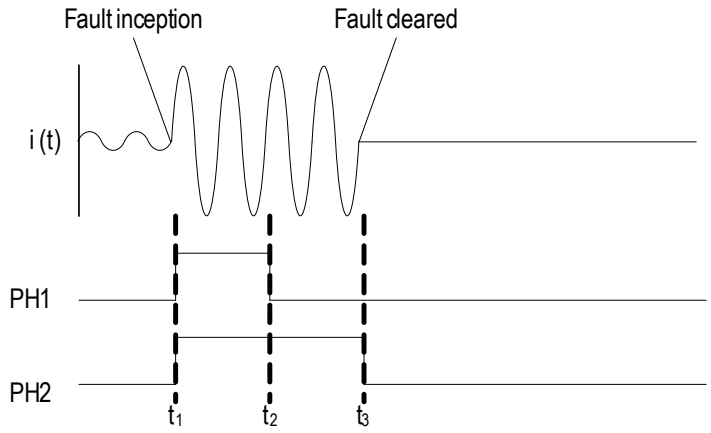



**Figure 137: Phase selector timing for power swing condition**




$t_1$: Δ i exceeds threshold 1 (5%In), so PH1 and PH2 go high

$t_2$: Fault current value appears in 2 cycle buffer . This equals present fault current value so Δ i is reduced to zero. PH1 therefore goes low. PH2 remains high because value in PH 2 memory is a stored value .

$t_3$: Fault is cleared so PH 2 goes low. PH1 stays low even though there is a new Δ I, because the absolute current value is also taken into consideration .

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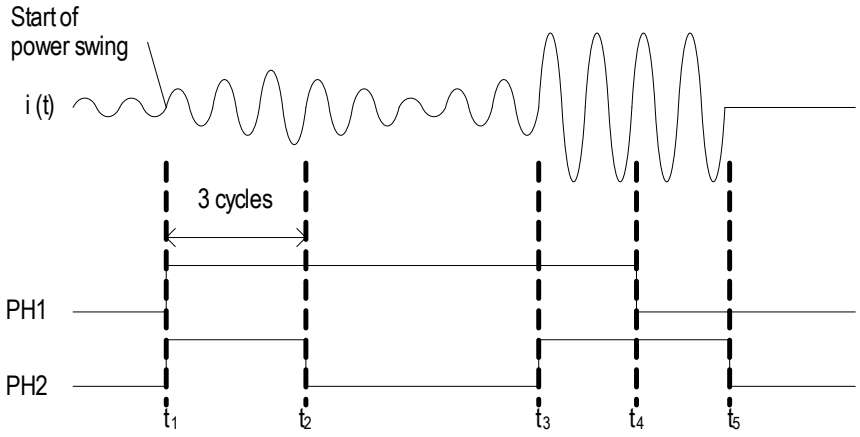
**Figure 138: Phase selector timing for fault condition**




$t_1$: Δ i exceeds threshold 1 (5%In), so PH1 and PH2 go high

$t_2$: Threshold 2 invoked (10%In). PH2 goes low on account of threshold being increased (from 5%IN to 10%In). PH1 remains high, because there continues to be a Δ i

$t_3$: Fault inception . Δ i exceeds threshold 2 (10%In ), so PH2 goes high

$t_4$: 2 cycles after fault inception , PH1 goes low

$t_5$: Fault cleared , so PH2 goes low

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**Figure 139: Phase selector timing for fault during a power swing**

### 9.3.1.2 SLOW POWER SWING DETECTION

For slow power swings (0.5Hz and below) where the superimposed current may remain below the minimum 5%In threshold needed for the superimposed current (ΔI) detector, a different detection method is used. This method is called Slow Swing detection. This method requires the ***Slow Swing*** setting to be enabled.

> *Note:*
> *If the Slow Swing feature is not Enabled, very slow power swings (< 0.5 Hz) may not be detected.*

The Slow Swing method is based on changing impedance measurements and uses a pair of configurable concentric quadrilateral zones on the impedance plane (Zone 7 and Zone 8). Since power swings don't involve earth, the impedance measurements are based on positive sequence quantities and only phase-phase measurements are necessary. The characteristic is shown in the following figure:

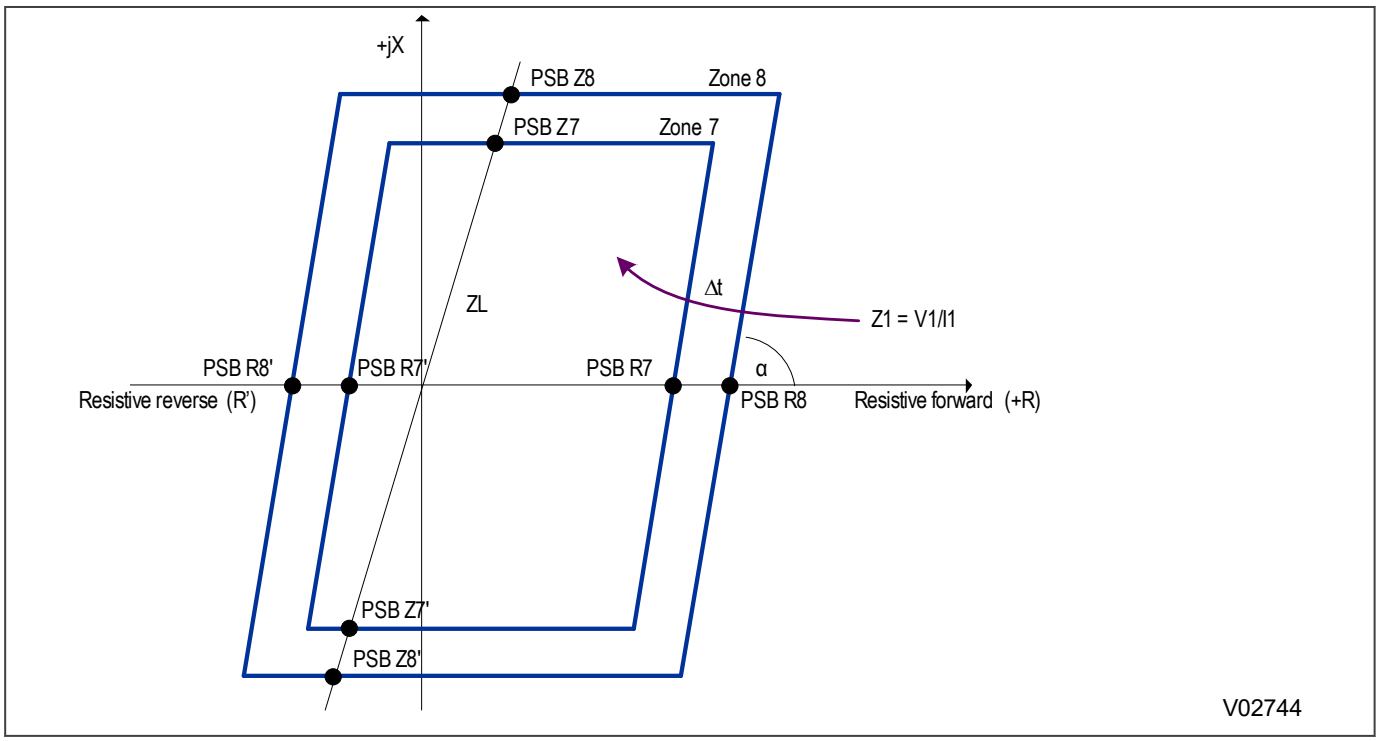


**Figure 140: Slow Power Swing detection characteristic**

The elapsed time defines the rate of change of impedance. If the rate of change is high, the change is due to a fault. If the rate of change is low, the protection indicates a slow power swing. So, if the time taken for the impedance trajectory to pass through zone 8 into zone 7 is greater than the time defined by the PSB timer, a slow power swing is deemed to be in progress. If the time taken for the impedance trajectory to pass through zone 8 into zone 7 is less than that defined by the PSB timer, it is deemed to be a fault.

In other words, a power swing is indicated if the following condition is true:

$\Delta\tau >$ ***PSB Timer***

Both Zone 7 and Zone 8 characteristics are based on the positive sequence impedance measurement; $Z_1 = V_1/I_1$. The minimum current (sensitivity) needed for Zone 7 and Zone 8 measurements is 5%In.

#### Configuring Slow Swing Detection

Slow Swing power swing detection and blocking must first be enabled with the ***Slow Swing*** setting. After this, you need to configure the resistive and impedance reach settings to define the concentric quadrilateral characteristics for zones 7 and 8:

***PSB R7***: forward resistive reach for zone 7

***PSB R7'***: reverse resistive reach for zone 7

***PSB R8***: forward resistive reach for zone 8

***PSB R8'***: reverse resistive reach for zone 8

***PSB Z7***: forward impedance reach for zone 7

***PSB Z7'***: reverse impedance reach for zone 7

***PSB Z8***: forward impedance reach for zone 8

***PSB Z8'***: reverse impedance reach for zone 8

You also need to configure the impedance phase angle $\alpha$. This is the same for zone 7 and zone 8. To do this you need to set ***Alpha*** between 20° and 90°.

The ***PSB timer*** setting defines the minimum time that the impedance trajectory must take to cross through zone 8 into zone 7 ($\Delta\tau$) before a power swing is deemed to have taken place. A power swing is indicated if $\Delta\tau >$ ***PSB Timer***.

## 9.3.2 DETECTION OF A FAULT DURING A POWER SWING

Faults are characterised by step changes in superimposed current (ΔI) rather than more gradual transitions symptomatic of a power swing.

When a power swing is in progress, the threshold for the phase selector is increased to a value twice that of the maximum prevailing superimposed current caused by the swing. A fault will cause a ΔI greater than this raised threshold, so the fault will be detected by the phase selector. Operation of the phase selector in this condition unblocks the PSB function, to allow tripping of Distance elements.

To provide stability for external faults, the blocking signal is only removed from zones that start within two cycles of the phase detector recognising the fault:

Any Distance element measuring an impedance inside its characteristic before the phase selector detects the fault remains blocked. This prevents tripping for a swing impedance that may be coincidentally passing through a fast-acting zone, and which could cause spurious tripping if all elements were unblocked without qualification.

Any Distance element that measures an impedance inside its characteristic after the two cycle ΔI window of the phase selector has expired, remains blocked. This prevents tripping for a continued swing that may pass through a fast acting zone which could cause spurious tripping if the element was allowed to unblock by an unqualified phase selector reset.

## 9.3.3 POWER SWING BLOCKING CONFIGURATION

To use the Power Swing function, you must ensure that the ***PowerSwing Block*** setting in the CONFIGURATION column is set to `Enabled`. You can set Power Swing Blocking to `Indication` (where alarms are raised but no blocking is imposed), or to Blocking (where blocking actions are imposed).

To define what the action the PSB function should take, you need to set the distance zones. The distance power swing zones for phase and earth are available under the *POWER SWING BLK.* column

The following options are available for each of the PSB zones:

`Allow Trip`: If a power swing locus stays in the Distance characteristic for a duration equal to the element time delay, the trip is allowed.

`Blocking`: Prevents tripping for that element, even if a power swing locus enters the element's characteristic.

`Delayed Unblock`: This maintains the block for a set duration after a power swing has been detected. To use it, you must set ***PSB Unblocking*** to `Enabled`, and then set the desired ***PSB Unblock dly*** time for removing the block.

*Note:*
*The **PSB Unblock dly** timer is common to all elements.*

The ***PSB Unblock dly*** is used to time the duration for which the swing is present. The intention is to allow the distinction between a stable and an unstable swing. If after the timeout period the swing has still not stabilised, the block for selected zones can be released (unblocking), giving the opportunity to split the system. If no unblocking is required, set to maximum (10 s).

There is a further timer associated with the PSB function. This is the ***PSB Reset Delay*** timer. This timer is provided to maintain the power swing detection for a period after the superimposed current detection (ΔI) has reset. ΔI naturally tends to zero twice during each power swing cycle (around the current maxima and minima in the swing element). A short time delay ensures continued PSB pick-up during these ΔI minima.

The ***PSB Reset Delay*** is used to maintain the PSB status when ΔI naturally is low during the swing cycle (near the current maxima and minima in the swing envelope). A typical setting of 0.2s is used to seal-in the detection until ΔI has chance to appear again.

The ***WI Trip PSB*** setting determines what will happen if a power swing is detected whilst the Weak Infeed (WI) tripping feature is being used and the WI condition is present for longer than the ***WI Trip Delay*** time. If `Blocking` is selected, the weak infeed operation will be disabled for the duration of the swing. If `Delayed Unblock` is chosen, the weak infeed element block will be removed after drop off timer ***PSB Unblock dly*** has expired, even if the swing is still present. This allows system separation when swings fail to stabilise. In `Allow trip` mode, the weak infeed element is unaffected by power swing detection.

### 9.3.4 POWER SWING LOAD BLINDING BOUNDARY

If the product has load blinding enabled, the following applies for phase-to-phase loops:

Impedance values, which are inside the load blinder boundaries and close to it for more than one cycle, are indicative of a power swing. The power swing region is represented by the shaded area in the following diagram.

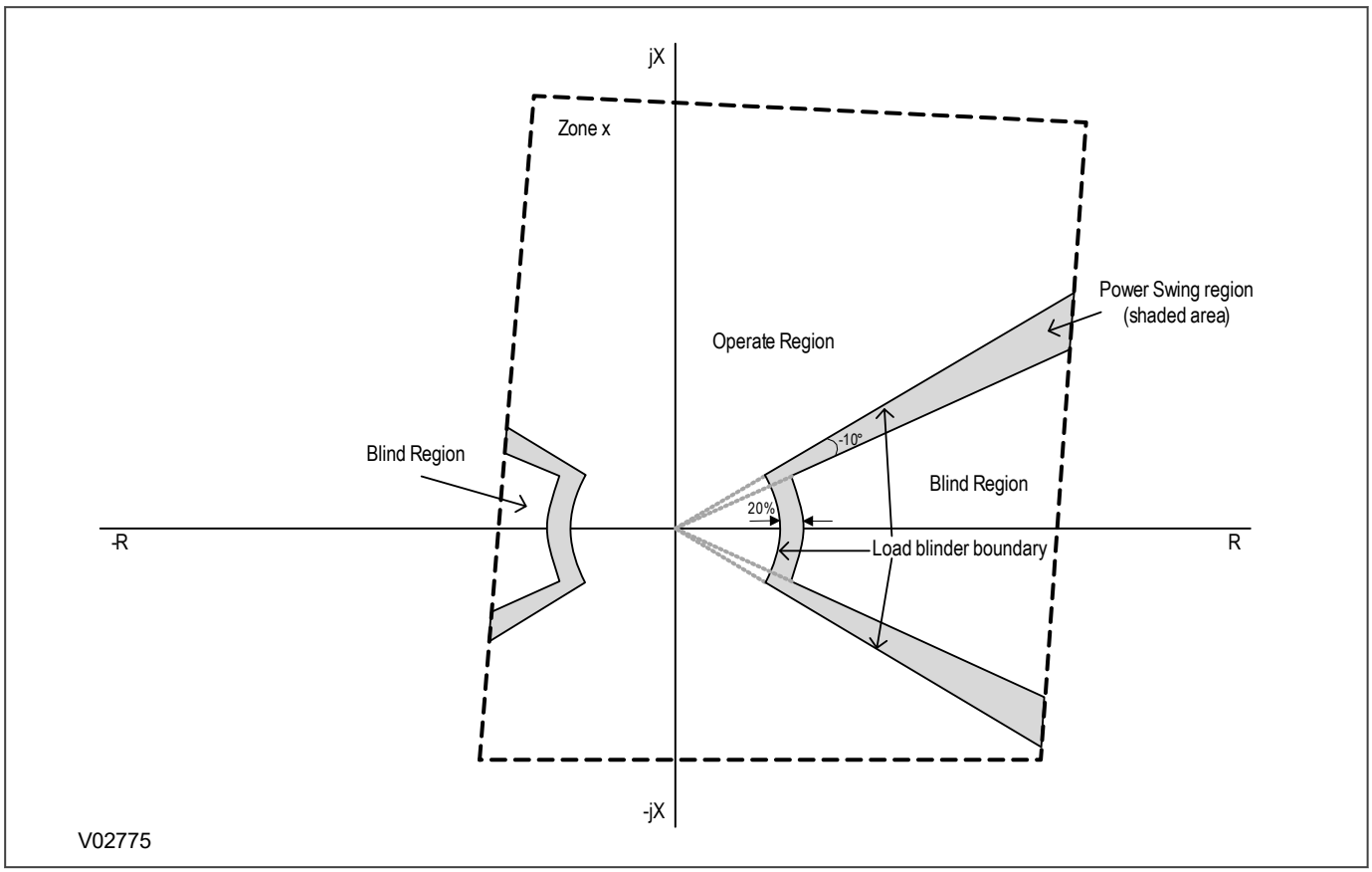


**Figure 141: Load Blinder Boundary Conditions**

The area is defined by lines created with angles fixed at 10° closer to the resistive axis than those created by the load blinder angle setting (***Load/B Angle*** -10°, shown in the shaded Power Swing region in the diagram above) and a circular arc with a radius concentric with, and equivalent to 20% greater than, the load blinder impedance setting (**Z< Blinder Imp** +20%, shown in the shaded Power Swing region in the diagram above).

*Note:*
*This power swing conditions are completely independent of the slow swing associated with Zone 7 and Zone 8.*

## 9.3.5 POWER SWING BLOCKING LOGIC

The Power Swing function follows the logic diagram below:

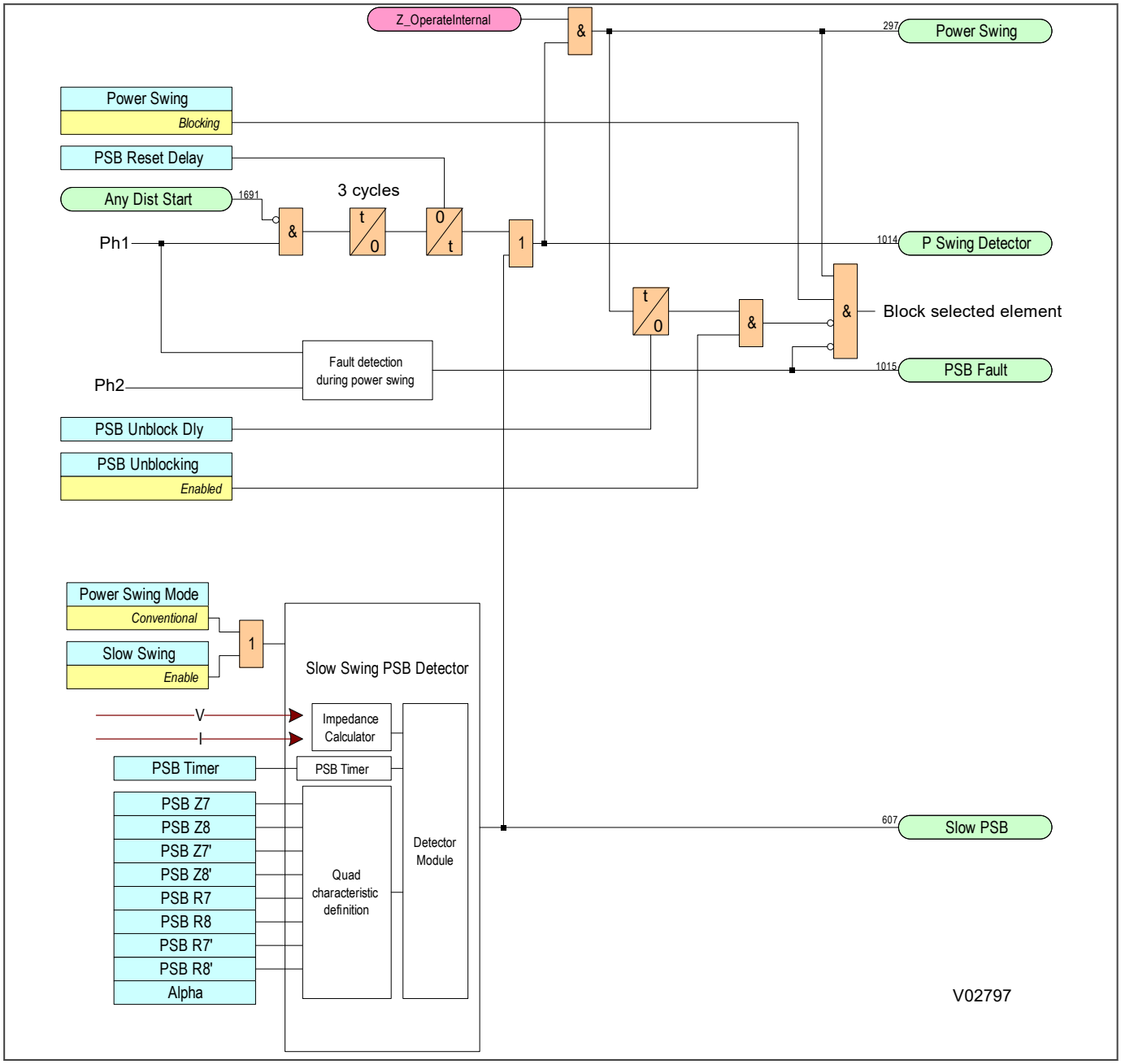


**Figure 142: Power swing blocking logic**

*Note:*
*This is a simplified representation to highlight the outputs of the Power Swing Blocking function.*

## 9.3.6 POWER SWING BLOCKING SETTING GUIDELINES

Power sing blocking (PSB) should normally only be enabled in transmission system applications. Power swings are not expected to occur at distribution level.

The main power swing detection technique used in this product can detect power swings faster than 0.5Hz without you having to set any parameters. This method relies on superimposed current (ΔI) component techniques to automatically detect power swings. The threshold to detect a power swing is 5%In. During power oscillations slower than 0.5Hz the continuous ΔI phase current integral to the detection technique may be less than the 5%In threshold.

So it may not operate. Slow swings usually occur following sudden load changes or single pole tripping on weak systems where the displacement of initial power transfer is not severe. Generally, swings of up to 1Hz are recoverable, but the swing impedance may stay longer inside the Distance characteristics than might be expected before the oscillations are damped by the power system. Therefore, to guarantee system stability during very slow swings, we recommend setting ***Slow Swing*** to `Enabled` to complement the automatic setting-free detection algorithm.

To configure the slow power swing function you need to set the resistive and reactive limits of the Zone 7 and Zone 8 quadrilaterals. You also need to set the ***PSB Timer*** which defines the critical time period of the transition between the two zones and which is characteristic of the slow swing.

Whichever power swing detector is responsible for applying PSB, the removal of PSB is defined by two settings – the ***PSB Reset Delay*** and (if an unblocking philosophy is employed) the ***PSB Unblock dly***.

### 9.3.6.1 SETTING THE RESISTIVE LIMITS

The Zone 7 quadrilateral should encompass all distance elements to be blocked during a power swing condition. The Zone 8 quadrilateral should be set smaller than the minimum possible load impedance. The security margin for both conditions should be at least 20%, also a margin of at least 10% should be provided between Zone 7 and Zone 8:

$$R8 > 1.1(R7)$$

We recommend setting the magnitudes of R7' and R8' equal to R7 and R8 respectively:

$$R7' = -R7,\ R8' = -R8.$$

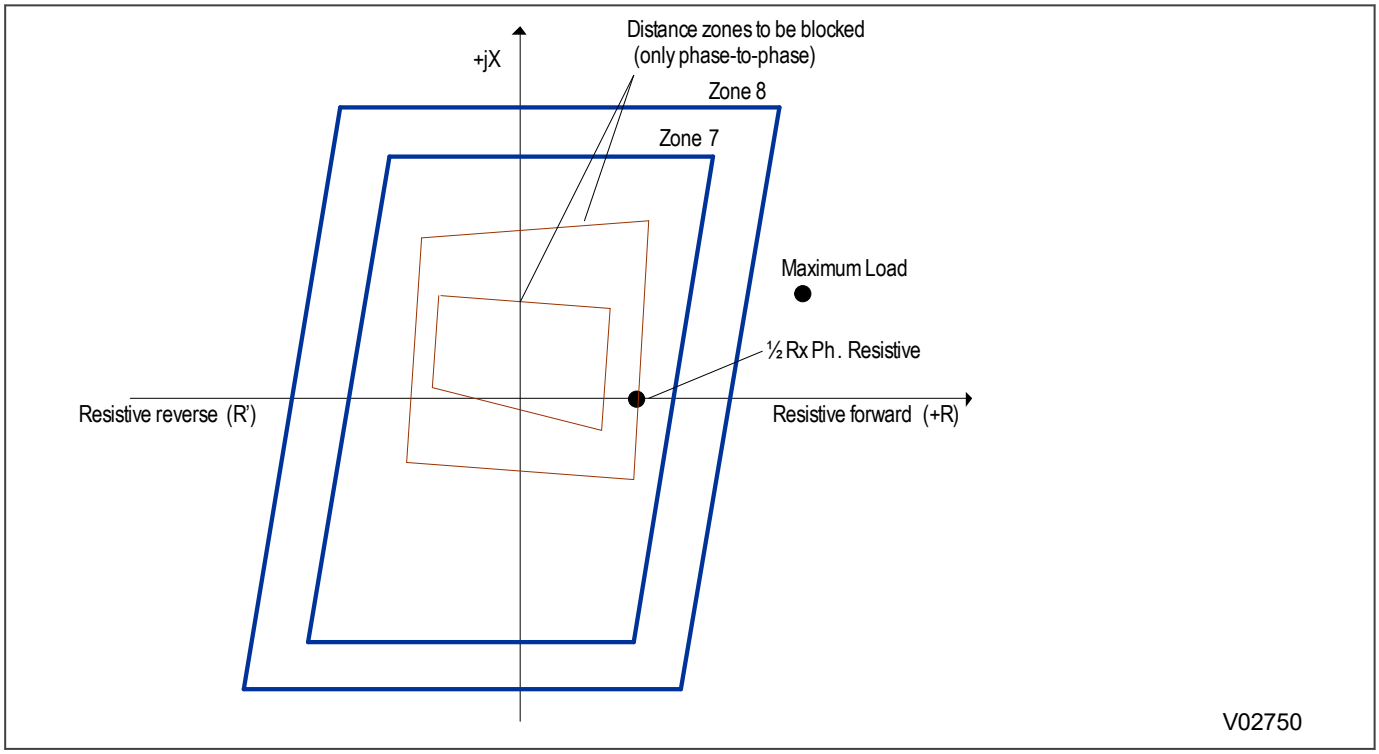


**Figure 143: Setting the resistive reaches**

### 9.3.6.2 SETTING THE REACTIVE LIMITS

The inner Zone 7 should be set in excess of total impedance $Z_T$ , which include local source impedance $Z_S$ , line impedance $Z_L$ and remote source impedance $Z_R$. Only positive sequence impedances should be considered. The security margin for this condition should be at least 20%. The recommended margin between Z7 and Z8 settings is 10%:

$$Z8 = 1.1(Z7)$$

We recommend setting the magnitudes of Z7' and Z8' equal to Z7 and Z8 respectively

$$Z7' = -Z7,\ Z8' = -Z8$$

The angle Alpha should be set equal to the angle of the total impedance $Z_T$:

$$\alpha = \angle Z_T$$

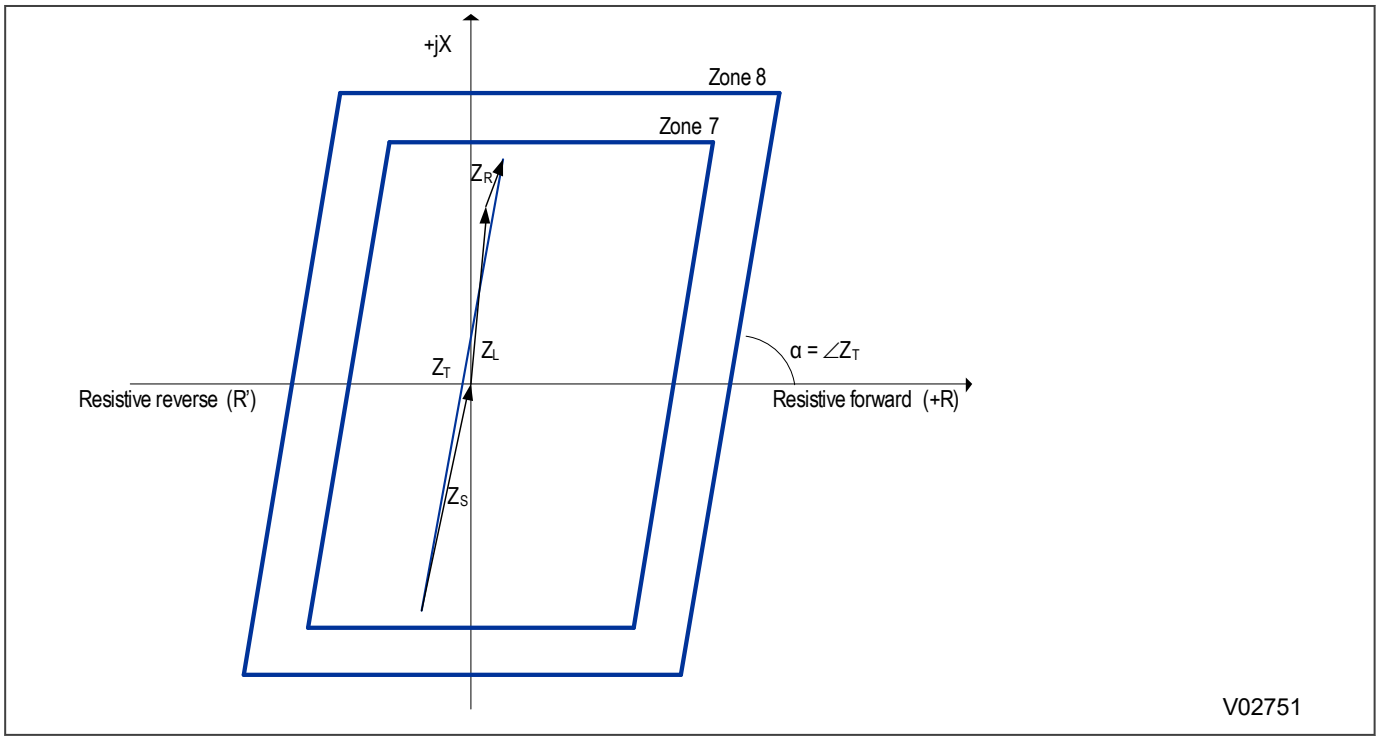


**Figure 144: Reactive reach settings**

### 9.3.6.3 PSB TIMER SETTING GUIDELINES

The Setting PSB Time setting can be calculated as follows:

$$\Delta t = \frac{(\theta_1 - \theta_2) \cdot f_{nom}}{f_{PS}}$$

where

- angles $\theta_1$ and $\theta_2$ are defined in the following figure
- $f_{nom}$ is the nominal frequency
- $f_{PS}$ is the maximum Power Swing frequency to be taken into account

Since any power swing with $f_{PS}$ >= 0.5Hz can be detected by the setting-free delta current algorithm, only power swings with $f_{PS}$ < 0.5Hz Hz need to be considered for Slow Power Swing detection. We recommended setting $f_{PS}$ to 1Hz because this value provides sufficient security margin.

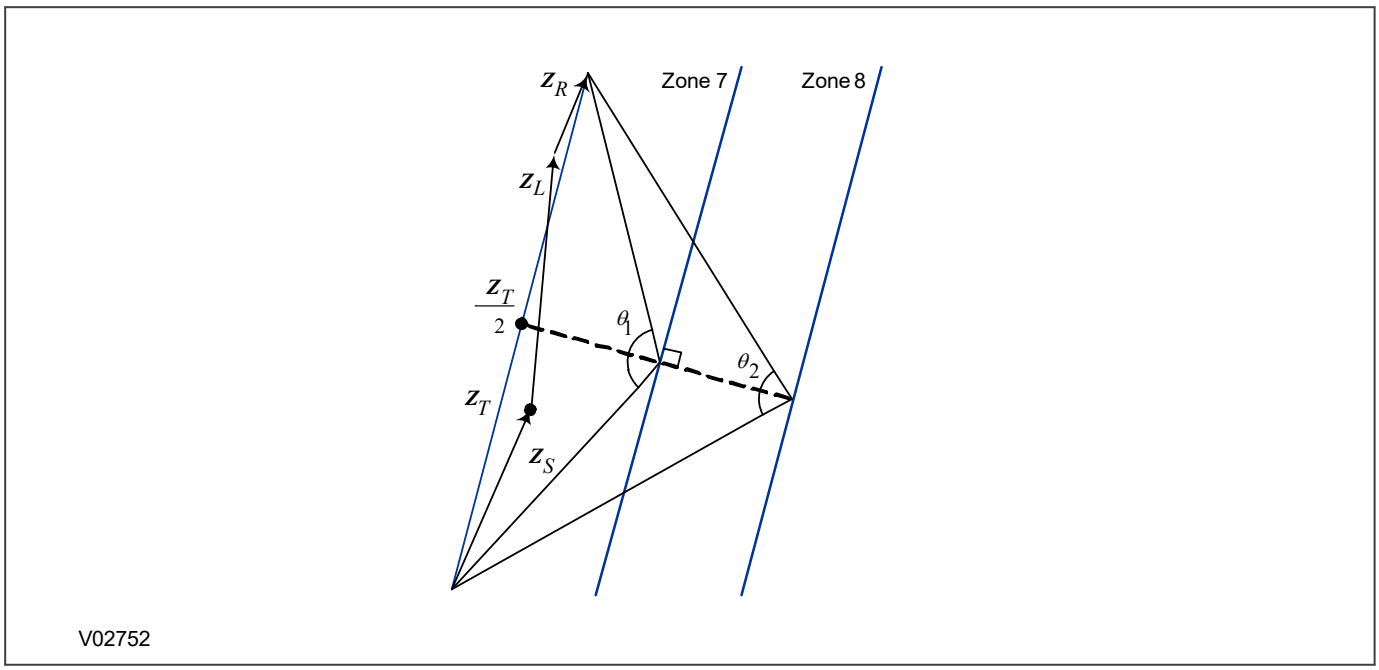


**Figure 145: PSB timer setting guidelines**

## 9.4 OUT OF STEP PROTECTION

Out-of-Step detection is based on the speed and trajectory of measured positive sequence impedance passing through a particular characteristic. During power system disturbances such as faults and power swings, measured impedance moves away from normal load values. Power swings, where the system voltage angles change relative to each other, can be either stable (recoverable) or unstable (non-recoverable). It is the unstable power swings that result in an Out-of-Step condition.

For stable power swings the relative phase angles will oscillate, but these oscillations will fade and synchronism between generating sources will be maintained. Detecting stable power swings is necessary to prevent unwanted tripping of impedance measuring protection elements if the swing impedance transiently passes through the fault impedance zone.

Unstable power swings (which can be destructive) result in sources of generation losing synchronism. This is called pole slipping. Detecting unstable power swings allows controlled tripping to split the systems into stable areas so that synchronism is maintained in each area. This is called Out-of-Step tripping (OOS or OST).

As well as tripping for Out-of-Step conditions, it is possible to predict OST conditions. This allows controlled tripping and consequent splitting of the system to recover stable operation before pole slipping occurs. This is called Predictive Out-of-Step tripping (Predictive OST).

Out-of-Step and Predictive Out-of-Step protection is based on changing impedance measurements, and uses a pair of configurable quadrilateral characteristics in the impedance plane (Zone 5 and Zone 6).

Out of Step protection is used to split the power system into more stable areas of generation and load balance during unstable power oscillations. The points at which the system should be split are determined by detailed system stability studies.

### 9.4.1 OUT OF STEP DETECTION

The Out of Step detection is based on the well proven $\Delta Z/\Delta t$ principle associated with two concentric polygon characteristic, as shown below:

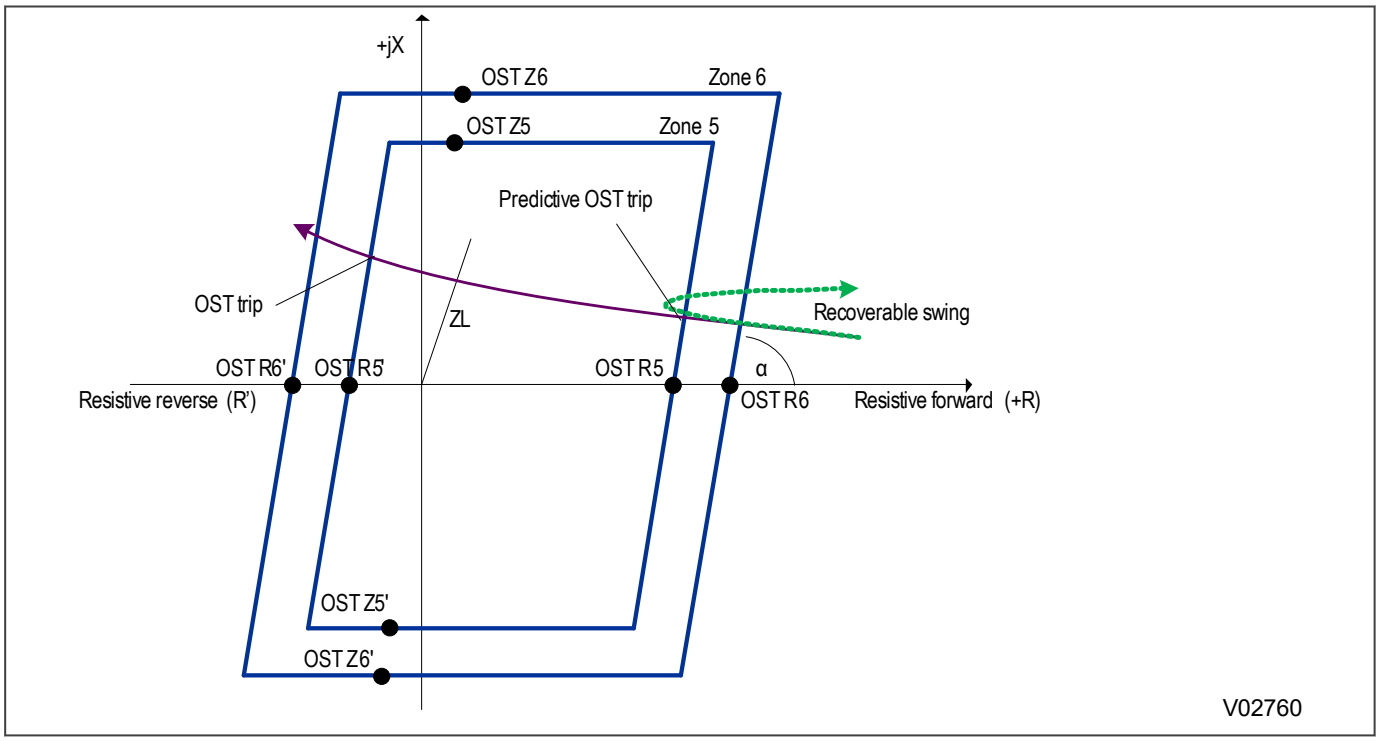


**Figure 146: Out of Step detection characteristic**

The OST principle uses positive sequence impedances. The positive sequence impedance is calculated as $Z_1 = V_1/I_1$, where $V_1$ and $I_1$ are the positive sequence voltage and current quantities derived from the measured phase quantities. The concentric quadrilaterals are designated Zone 5 and Zone 6. Zone 5 encompasses possible system fault impedances and sits within Zone 6. Because OST and Predictive OST quadrilaterals are based on positive sequence impedances, all OST conditions are covered by a single measurement. Both quadrilaterals are independent and have independent reach settings.

All four resistive blinders are parallel, using the common angle setting ($\alpha$) that corresponds to the angle of the total system impedance ($Z_T = Z_S + Z_L + Z_R$), where $Z_S$ and $Z_R$ are equivalent positive sequence impedances at the sending and receiving ends and $Z_L$ positive sequence line impedance. The reactance lines are also parallel as neither reactance line tilting nor esidual compensation is implemented.

In the figure, the purple solid impedance trajectory represents the locus for the non-recoverable power sawing, known as a pole slip or Out Of Step condition. The dotted green impedance trajectory represents a recoverable power swing.

## 9.4.2 OUT OF STEP PROTECTION OPERATING PRINCIPLE

The Out of Step function has four different setting options, which are only visible if the ***PowerSwing Block*** is enabled in the *CONFIGURATION* column:

- `OST Disabled`: Disables the Out of Step function.
- `Pred. OST Trip`: Splits the system in advance. It minimizes the angle shift between two ends and aids stability in the split areas.
- `OST Trip`: Splits the system when an out of step condition is detected, which is when a pole slip occurs.
- `Pred. & OST Trip`: For this mode both methods are available, and the final trip condition is detected based on either of predictive method or OST Trip method.

The Out-of-Step detection algorithm is based on the speed of the positive sequence impedance passing through the characteristic. When the positive sequence impedance enters the outer quadrilateral (Zone 6) a timer is started. The timer is stopped after the positive sequence impedance passes through the inner quadrilateral (zone 5). Let us call this time the zone 6 to zone 5 transition time.

If this time is less than 25 ms, the protection considers this to be a power system fault, not an Out-of-Step condition. This 25 ms time is fixed and cannot be set. During a power system fault, the speed of change from a load impedance to a fault impedance is fast, but the protection may operate slower for marginal faults close to a zone boundary. This is particularly the case for high resistive faults inside the zone operating characteristic and close to the Zone 5 boundary. The fixed time of 25 ms is implemented to provide sufficient time for a distance element to operate and therefore to distinguish between a fault and an extremely fast power swing.

If the zone 6 to zone 5 transition time takes more than 25 ms but less than the set ***delta T*** time, this is treated as a very fast power swing and the protection will trip if either the `Pred. OST Trip` or the `Pred. & OST Trip` options are selected and the Out-of-Step tripping time delay (***Tost***) has expired. The minimum ***delta T*** setting is 30 ms, allowing 5 ms margin with the fixed 25 ms timer.

If the zone 6 to zone 5 transition time takes longer than the set ***delta T*** time, it is considered as a slow power swing. On entering Zone 5, the protection records the polarity of the resistive part of the positive sequence impedance. From this state, two outcomes are possible:

- If the resistive part of the positive sequence impedance leaves Zone 5 with the same polarity as previously recorded on entering Zone 5, it is considered to be a recoverable swing. In this case, the protection does not trip.
- If, when exiting Zone 5, the resistive part of the positive sequence impedance has the opposite polarity to that of the recorded polarity on entering Zone 5, an Out-of-Step condition is recognised. This is followed by tripping if either `Pred. OST Trip` or `Pred. & OST Trip` is selected.

As the tripping mode for the detected Out-of-Step condition is always three-phase, the ***Pred. OST*** and ***OST*** DDB signals are mapped to the three-phase tripping signal in the default programmable scheme logic.

The Out-of-Step tripping time delay (***Tost***), delays the OST tripping command until the angle between internal voltages between the two ends are at 240 degrees closing towards 360 degrees. This limits the voltage stress across the circuit breaker. If a fault occurs during the swing condition, the Out-of-Step tripping function is blocked.

The Out-of-Step algorithm is completely independent from the distance elements and the power swing detection function. The load blinder does not affect the OST characteristics. In common with other similar functions, a minimum positive sequence current of 5%In is needed for Out-of-Step operation.

## 9.4.3 OUT OF STEP LOGIC DIAGRAM

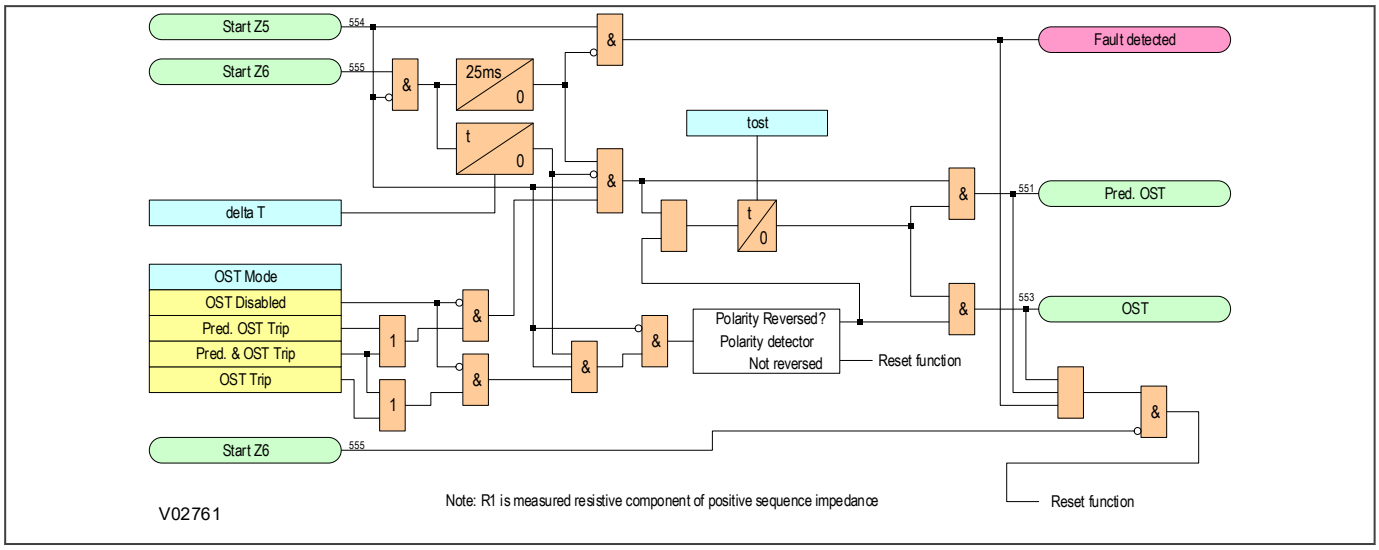


**Figure 147: Out of Step logic diagram**

## 9.4.4 OST APPLICATION NOTES

This product provides integrated Out-of-Step protection, which avoids the need for a separate stand alone Out-of-Step device. This section provides guidance on how to configure Out of Step protection.

If you are going to use either of the *predictive* OST options (*Pred. OST Trip* or *Pred. & OST Trip)* you must conduct detailed system studies to determine accurate settings. This is because high setting accuracy is needed to avoid premature system splitting in the case of severe power oscillations that do not lead to pole slip conditions.

Using the *non-predictive* OST Trip setting is simpler. You can can set it by knowing just the total system impedance, $Z_T$, and the system split points.

### 9.4.4.1 SETTING THE OST MODE

The OST Mode setting provides four options:

- *OST Disabled*
- *Pred. OST Trip*
- *OST Trip*
- *Pred. & OST Trip*

Setting *OST Trip* is the most commonly used approach when this protection is applied. *OST Trip* should be used when Out-of-Step conditions are probable. If Out-of-Step conditions are detected, the OST command will be issued to split the system at the pre-determined points. A disadvantage of the *OST Trip* option compared with the 'Predictive' options is that tripping will take a little longer so that the power oscillations may escalate further after separation and the split parts may become separately unstable. An advantage, however, is that the decision to split the system will always be valid even if the accurate system data and setting parameters cannot be obtained.

The predictive setting options *Pred. OST Trip* and *Pred. & OST Trip* are recommended for systems where Out-of-Step conditions could possibly occur, and where an early system split should minimise the phase shift between generation sources. This should maximise the chances for the separated parts of the system to stabilise as quickly as possible. Special care must be taken when these settings are used to ensure that the circuit breakers at the different terminals do not open when the voltages at different ends are in anti-phase. This is because most circuit breakers are not designed to break current at double the nominal voltage. Attempting to break the current at double the nominal voltage could lead to flash-over and circuit breaker damage.

'Predictive' settings are designed to detect and trip for fast power oscillations. When predictive tripping is used with a circuit breaker capable of operating in typically two-cycles, the two voltages angles may rapidly move in opposite directions at the time of opening the circuit breaker. So, if you use the predictive settings you need to apply settings that will ensure that the circuit breaker opening occurs well before the phase difference between the different terminals approaches 180º. This means that accurate settings can only be determined by exhaustive system studies.

The setting *Pred. & OST Trip* provides two stages of OST. If a power system oscillation is very fast, the combination of ΔR (the difference between the Zone 5 and Zone 6 resistive reaches), and the ***Delta T*** settings, must be set so that *Pred. OST Trip* operates. If the oscillation is slower, the condition for the predictive OST is not met and so tripping is dictated by the OST condition being met. For the OST condition to be met, the resistive component of the impedance must leave Zone 5 with opposite polarity compared with when it entered. If the polarity is opposite when Zone 5 resets, OST will trip. If the polarity is the same when Zone 5 resets, OST will not trip. This distinguishes between a slower non-recoverable oscillation and recoverable swings.

You should disable OST for applications on lines where unrecoverable power oscillations are not expected, or not expected to be severe. This is likely to apply to strong interconnected systems operating with three-phase tripping.

#### 9.4.4.1.1 DETERMINING THE LIMITS OF THE OST CHARACTERISTIC

The figure below shows the OST characteristic in conjunction with the system impedance, ZT, and particularly the relationship with the resistive reach of the Zone 5 element.

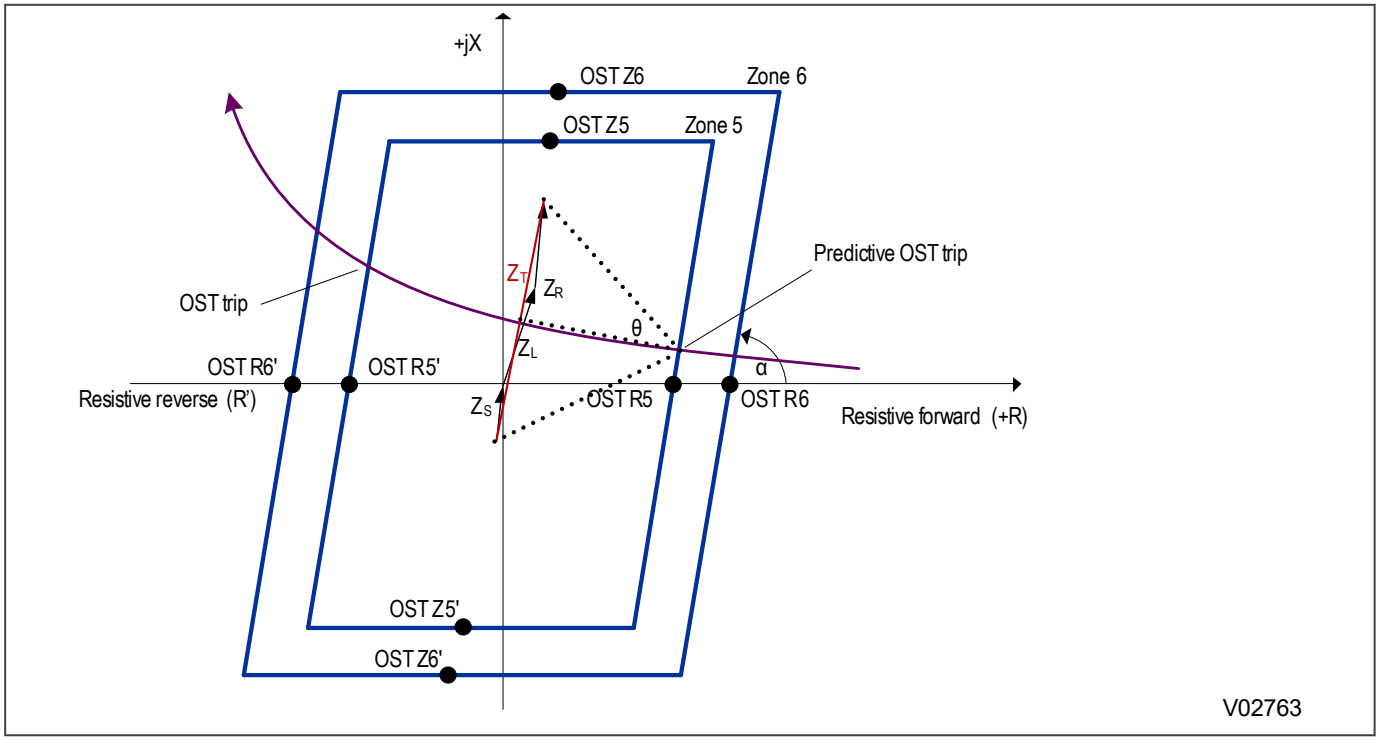


**Figure 148: OST setting determination for the positive sequence resistive component OST R5**

$Z_T$ is the total system positive sequence impedance equal to $Z_S + Z_L + Z_R$, where $Z_S$ and $Z_R$ are the equivalent positive sequence impedances at the sending and receiving ends and $Z_L$ is the positive sequence line impedance.

θ is the angular difference between the voltages at the sending and receiving ends beyond which no system recovery is possible.

To determine the settings for OST, the minimum inner resistive reach of OST R5 (R5min) needs to be calculated.

The figure above shows that:

$$R5min = (Z_T/2) / \tan(\theta/2$$

Next the maximum (limit value) for the outer resistive reach ***OST R6*** (R6 max) needs to be calculated. Referring to the figure below, point A must not overlap with the load area for the worst assumed power factor of 0.85 and the lowest possible $Z_T$ angle α.

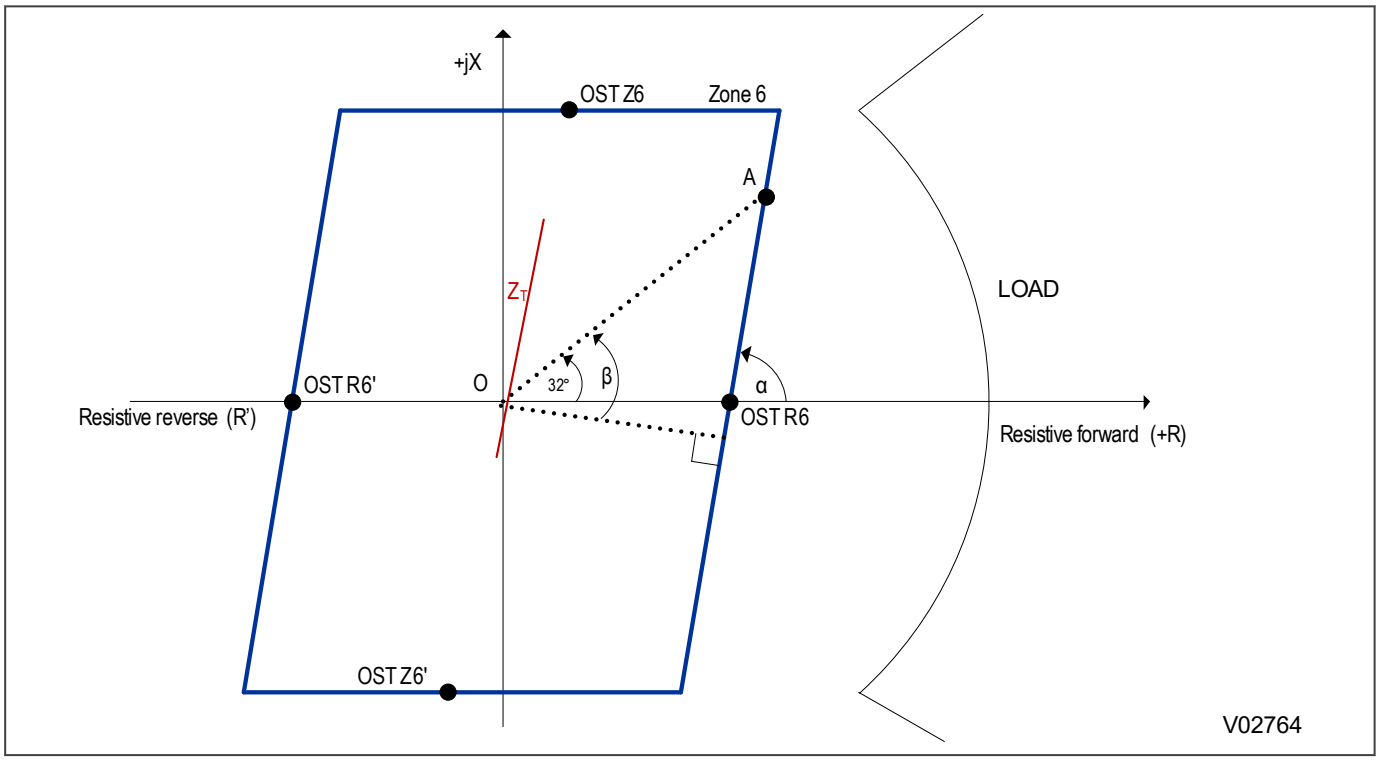


**Figure 149: OST R6max determination**

$$\beta = 32 + 90 - \alpha$$

$$Z \text{ load min} = OA$$

Where:

- Z load min is the minimum load impedance radius
- 32º is the load angle that corresponds to the lower power factor of 0.85
- α is the load blinder angle (Blinder Angle) that matches the $Z_T$ angle

Therefore:

$$R6max < Z \text{ load min}(\text{Cos } \beta)$$

Starting from the limit values R5min and R6max, the actual ***OST R5*** and ***OST R6*** reaches will be set in conjunction with the ***Delta T*** setting.

*Note:*
*The R6max reach must be greater than the maximum resistive reach of any distance zone to ensure correct initiation of the 25 ms and Delta T timers. However, the R5min reach could be set below the distance maximum resistive reach (inside the distance characteristic) if an extensive resistive coverage is required, meaning that Out-of-Step protection does not pose a restriction to the quadrilateral applications.*

For each zone, we receommend setting the positive and negative limits to be the same so, OST R5' = OST R5, OST Z5' = OST Z5, OST R6' = OST R6, and OST Z6' = OST Z6.

#### 9.4.4.1.2 SETTING OST Z5 AND OST Z6

Setting of the reactance lines ***OST Z5*** and ***OST Z6*** depends on how far from the protection location the power oscillations are to be detected. Normally, there is only one point for initial splitting of the system; and that point will be determined by system studies. For that reason, the Out-of-Step protection must be enabled at that location and disabled on all others. To detect the Out-of-Step conditions, the ***OST Z5'***, ***OST Z5***, ***OST Z6'***, and ***OST Z6*** settings must be set to comfortably encompass the total system impedance $Z_T$. A typical setting could be:

$$OST\ Z5 = OST\ Z5' = Z_T$$

The ***OST Z6*** and ***OST Z6'*** settings are not of great importance and could be set to 1.1 x ***OST Z5***.

#### 9.4.4.1.3 SETTING OST R5, OST R6 AND DELTA T

The R5min and R6max settings determined above represent *limit* values. The actual ***OST R5*** and ***OST R6*** values need to be determined in relation to the ***Delta T*** timer.

##### Predictive OST setting

For the `Pred. OST Trip` setting, it is important to:

- Set ***OST R6*** equal to R6max
- Set ***OST R5*** as close as practical to R6max

The aim of pushing the ***OST R5*** setting to the right is to detect fast oscillations as soon as possible, in order to gain sufficient time to operate the breaker before the two source voltages are in opposite directions. The only restriction is the limitation of the ***Delta T*** minimum time delay of 30ms and the speed of oscillation.

You should set ***Delta T*** such that it does not expire after the positive sequence impedance has passed the ***OST R6*** – ***OST R5*** region.

For this setting, you need to know the rate-of-change of swing impedance when crossing the ***OST R6*** – ***OST R5*** region. This must therefore be based on system studies.

*Note:*
*You cannot assume that the rate-of-change of positive sequence impedance while crossing the **OST R6** – **OST R5** region is the same as the average rate-of-change of positive sequence impedance for the whole swing cycle. A false assumumption could lead to incorrect predictive OST operation.*

*Note:*
*For a fault, the **OST R6** – **OST R5** region will be crossed faster than 25ms, therefore even very fast oscillations up to 7Hz will not be mistaken as a fault condition and predictive OST will not operate.*

##### OST setting

For the `OST Trip` setting option, such a precise setting of the blinders and ***Delta T*** is not necessary. This is because for a wide ΔR region and a short ***Delta T*** setting, any oscillation will be successfully detected. However, the fault impedance must pass through the ΔR region faster than the ***Delta T*** setting.

Therefore, for the *OST Trip* setting, assume that θ = 120° and set:

- ***OST R5*** = ***OST R5'*** = R5min = $Z_T$/3.46
- ***OST R6*** = ***OST R6'*** = R6max
- ***Delta T*** = 30 ms

***Delta T*** always expires. Therefore, the setting value given above will secure the detection of a wide range of oscillations, starting from very slow oscillations (caused by recoverable swings) up to a fastest oscillation limit of 7Hz. Note that any fault impedance will pass the ***OST R6*** – ***OST R5*** region faster than the minimum settable ***Delta T*** time of 30ms.

#### Predictive and OST setting

The recommendations for *Pred. & OST Trip* are the same as for *Pred. OST Trip*.

#### 9.4.4.1.4 SETTING THE OST TIME DELAY

For either of the predictive OST settings, the OST time delay setting (***Tost***) must be set zero.

For the *OST Trip* setting, ***Tost*** would normally be set to zero, but if you want to operate the breaker at an angle closer to 360º (when voltages are in phase) you could apply a time delay.

#### 9.4.4.1.5 BLINDER ANGLE SETTING

Set ***Blinder Angle***, α, the same as the total system impedance angle, $Z_T$.

#### 9.4.4.1.6 OST FOR SERIES COMPENSATED LINES

The maximum phase currents during an Out-of-Step condition rarely exceed 2In, which corresponds to the minimum swing impedance passing through Zone 1. Since the Metal-Oxide Varistors (MOV) bypass level is normally set between 2-3In, they will not operate during the power oscillations and therefore in the majority of applications they will not make any impact on Out-of-Step operation.

In the worst case, power oscillations are triggered on fault clearance on a parallel line. Approximately twice the load current starts flowing through the remaining circuit. This increases further and eventually exceeds the MOV threshold. The ***OST R6*** - ***OST R5*** region is usually set far from Zone 1, therefore it is unlikely that the positive sequence impedance's trajectory can traverse in and out of the set ΔR region due to the operation of MOVs. If MOVs do operate in the ΔR region, a timer that has been initiated may reset and be reinitiated, or the impedance may remain in the ΔR region for slightly longer. This is because resistive and capacitive components are added to the measured impedance during MOV operation as shown in the figure below. This effect may have an impact on the ***Delta T*** measurement if the *Pred. OST Trip* setting is used. If the recommendation to set R5min as close as practically possible to R6max is followed, it is unlikely that the swing currents will exceed the MOV threshold in the ΔR region. If a study shows that the MOVs could operate within the ΔR region, we recommend setting *Pred. & OST Trip* operating mode to cover all eventualities.

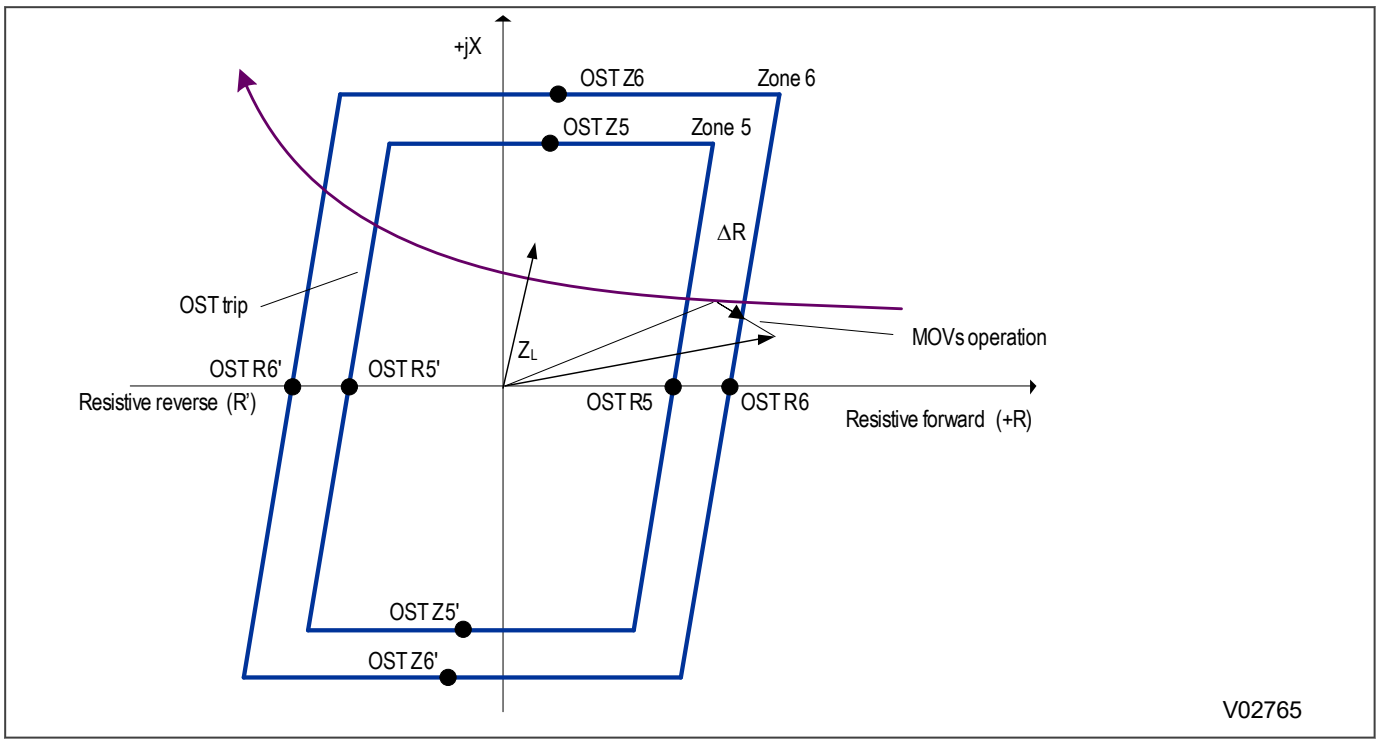


**Figure 150: Example of timer reset due to MOVs operation**

*Note:*
*If the **OST Trip** setting is chosen, the timer when triggered, will eventually expire as the power oscillations progress, therefore the MOV operation will not have any impact on Out-of-Step operation.*

# CHAPTER 10

# AUTORECLOSE

## 10.1 CHAPTER OVERVIEW

Selected models of this product provide sophisticated Autoreclose (AR) functionality. The purpose of this chapter is to describe the operation of this functionality including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 249
Introduction to Autoreclose 250
Autoreclose Implementation 251
Logic Modules 256
Setting Guidelines 286

## 10.2 INTRODUCTION TO AUTORECLOSE

Approximately 80 - 90% of faults on transmission lines and distribution feeders are transient in nature. This means that most faults do not last long, and are self-clearing if isolated. A common example of a transient fault is an insulator flashover, which may be caused, for example, by lightning, clashing conductors, or wind-blown debris. Protection functions detecting the flashover will cause one or more circuit breakers to trip and may also remove the fault. If the source is removed, the fault does not recur if the line is re-energised.

The remaining 10 – 20% of faults are either semi-permanent or permanent. A small tree branch falling onto the line for example, could cause a semi-permanent fault. Here the cause of the fault would not be removed by immediate tripping of the circuit, but could possibly be burnt away during a time-delayed trip. Permanent faults could be broken conductors, transformer faults, cable faults or machine faults, which must be located and repaired before the power supply can be restored. In many fault incidents, if the faulty line is immediately tripped out, and time is allowed for the fault arc to de-ionise, reclosing the circuit breakers will result in the line being successfully re-energised.

Autoreclose schemes are used to automatically reclose a circuit breaker a set time after it has been opened due to operation of a protection element. On EHV transmission networks, Autoreclose is usually characterised by high-speed single-phase operation for the first attempt at reclosure. This is intended to help maintain system stability during a transient fault condition. On HV/MV distribution networks, Autoreclose is applied mainly to radial feeders, where system stability problems do not generally arise, and is generally characterised by delayed three-phase operation with potentially multiple reclosure attempts.

Autoreclosing provides an important benefit on circuits using time-graded protection, in that it allows the use of instantaneous protection to provide a high speed first trip. With fast tripping, the duration of the power arc resulting from an overhead line fault is reduced to a minimum. This lessens the chance of damage to the line, which might otherwise cause a transient fault to develop into a permanent fault. Using instantaneous protection also prevents blowing of fuses in teed feeders, as well as reducing circuit breaker maintenance by eliminating pre-arc heating. When instantaneous protection is used with Autoreclose, the scheme is normally arranged to block the instantaneous protection after the first trip. Therefore, if the fault persists after re-closure, the time-graded protection will provide discriminative tripping resulting in the isolation of the faulted section. However, for certain applications, where the majority of the faults are likely to be transient, it is common practise to allow more than one instantaneous trip before the instantaneous protection is blocked.

Some schemes allow a number of re-closures and time-graded trips after the first instantaneous trip, which may result in the burning out and clearance of semi-permanent faults. Such a scheme may also be used to allow fuses to operate in teed feeders where the fault current is low.

When considering feeders that are partly overhead line and partly underground cable, any decision to install Autoreclose should be subject to analysis of the data (knowledge of the frequency of transient faults). This is because this type of arrangement probably has a greater proportion of semi-permanent and permanent

faults than for purely overhead feeders. In this case, the advantages of Autoreclose are small. It can even be disadvantageous because re-closing on to a faulty cable is likely to exacerbate the damage.

## 10.3 AUTORECLOSE IMPLEMENTATION

Before describing this function it is first necessary to understand the following terminology:

- A **Shot** is an attempt to close a circuit breaker using the Autoreclose function.
- **Multi-shot** is where more than one **Shot** is attempted.
- **Single-shot** is where only one **Shot** is attempted.
- **Dead Time** denotes the time between initiation of the Autoreclose operation and the attempt to close the circuit breaker.
- **Reclaim time** is the time following the initiation of the circuit breaker closing and the resetting of the Autoreclose scheme should the Autoreclose attempt be successful and the protection does not detect a subsequent fault condition.
- **High-speed Autoreclose** is generally regarded as an Autoreclose application where the **Dead Time** is less than 1 second.
- **Delayed Autoreclose** is generally regarded as an Autoreclose application where the **Dead Time** is greater than 1 second.

This product features a multiple-shot Autoreclose function, which is suitable for both High-speed Autoreclose and Delayed Autoreclose.

The Autoreclose function can be set to perform a single-shot, two-shot, three-shot or four-shot cycle. Dead Times for all shots can be adjusted independently.

If a circuit breaker closes successfully at the end of the Dead Time, a Reclaim Time starts. If the circuit breaker does not trip again, the Autoreclose function resets at the end of the Reclaim Time. If the protection trips again during the Reclaim Time, the sequence advances to the next shot in the programmed cycle. If all programmed reclose attempts have been made and the circuit breaker does not remain closed, the Autoreclose function goes into Lockout, whereupon manual intervention is required.

An Autoreclose cycle can be initiated by operation of an internal or external protection element provided it is mapped correctly, and that the circuit breaker is closed when the protection operates.

You can choose to initiate the Dead Time on:

- Protection operation
- A protection reset
- A Line Dead condition
- Circuit breaker operation

At the end of the relevant Dead Time, provided system conditions are suitable, a circuit breaker close signal is given. The system conditions to be met for closing are that:

- the system voltages are in synchronism
- or that the dead line/live bus or live line/dead bus conditions exist as indicated by the internal system check synchronising element
- and that the circuit breaker closing spring, or other energy source, is fully charged as indicated by the circuit breaker healthy input.

The circuit breaker close signal is removed when the circuit breaker closes.

If the protection trips and the circuit breaker opens during the Reclaim Time, the Autoreclose function either advances to the next shot in the programmed cycle, or if all programmed reclose attempts have been made, goes into Lockout. Each time a closure is attempted, a sequence counter is incremented by 1 and the Reclaim Time starts again.

Autoreclose is configured in the *AUTORECLOSE* column of the relevant settings group. The function is disabled by default. If you wish to use it you must enable it first in the *CONFIGURATION* column.

The Autoreclose function is a logic controller implemented in software. It takes inputs and processes them according to defined logic to generates appropriate outputs. The logic is controlled by user prescribed settings and commands. The controlling logic is complex and so, in order to facilitate its design and understanding, it is decomposed into smaller logic functions which, when combined together implement the complete scheme. This section concludes with a summary of:

- the logic inputs to the Autoreclose function,
- the logic outputs from the Autoreclose function
- the Autoreclose operating sequence
- the high-level design of the system logic functionality

## 10.3.1 AUTORECLOSE LOGIC INPUTS FROM EXTERNAL SOURCES

Logic inputs control the operation of the Autoreclose function. The logic inputs are mapped using DDB signals in the PSL.

Generally the inputs are from external equipment connected to opto-isolated inputs. They can also come from communications inputs, and some are internally derived.

This section provides an overview of the logic inputs originating from external sources.

### 10.3.1.1 CIRCUIT BREAKER HEALTHY INPUT

For circuit breakers to close, it needs energy. This energy usually comes from a spring (spring-charged circuit breakers) or from gas pressure (gas pressurised circuit breakers). After closing, it is necessary to re-establish sufficient energy in the circuit breaker before it can be closed again.

DDB signal inputs to the Autoreclose function allow the health of circuit breakers to be mapped to the logic. when asserted, these signals demonstrate that there is sufficient energy available to close and trip the circuit breaker before initiating a circuit breaker close command. If the signal indicating the health of the circuit breaker is low, and remains low for a defined period set in the circuit breaker healthy timer, the circuit breaker locks out and stays open.

If the circuit breaker healthy signal is not mapped in the PSL, the DDB signal defaults to high so that Autoreclose may proceed.

### 10.3.1.2 INHIBIT AUTORECLOSE INPUT

A logic input can be used to inhibit the Autoreclose function. The signal is mapped to the DDB signal ***Inhibit AR*** in the PSL.

Energising the input inhibits any auto-switching of connected circuit breakers. Any Autoreclose in progress is reset and inhibited but not locked out. This function ensures that auto-switching does not interfere with any manual switching. A typical application is on a mesh-corner scheme where manual switching is being performed on the mesh, for which any Autoreclose would cause interference.

For products that are capable of single-phase tripping and Autoreclose, if a single-phase Autoreclose cycle is in progress and a single pole of the circuit breaker is tripped when the inhibit Autoreclose signal is raised, the circuit breaker is instructed to trip all phases, ensuring that all poles are in the same state (and avoiding a pole stuck condition) when subsequent closing of the circuit breaker is attempted.

### 10.3.1.3 BLOCK AUTORECLOSE INPUT

External inputs can be used to block the Autoreclose function. If Autoreclose is in progress when the signal is asserted, it forces a lockout.

Typically this feature is used where Autoreclose may be required for some protections functions but not required for others. An example is on a transformer feeder, where Autoreclose can be initiated from the feeder protection but blocked from the transformer protection.

It can also be used if an Autoreclose cycle is likely to fail for conditions associated with the protected circuit, such as during the Dead Time, if a circuit breaker indicates that it is not healthy to switch.

#### 10.3.1.4 RESET LOCKOUT INPUT

If a condition that forced a lockout has been removed, the lockout can be reset by energising a logic input appropriately mapped in the PSL. Energising the input will also reset any Autoreclose alarms.

#### 10.3.1.5 POLE DISCREPANCY INPUT

Circuit breakers with independent mechanisms for each pole (phase), normally incorporate a mechanism to cater for cases where the phases are not together. This automatically trips all three phases if they are either not all open, or not all closed.

During single-phase Autoreclosing a pole discrepancy condition is necessarily introduced, but the pole discrepancy device should not operate for this condition. This can be achieved using a delayed action pole discrepancy device with a delay longer than the single-pole Autoreclose Dead Time (***SP AR Dead Time*** setting).

Alternatively, an input can be used for external devices to indicate a pole discrepancy condition. The pole discrepancy input is activated by an external device to indicate that all three poles of a circuit breaker are not in the same position. If mapped in the PSL, energising the input forces three-phase tripping (providing there is not a single-phase Autoreclose in progress). Otherwise, a signal indicating single-phase Autoreclose in progress can be used to inhibit the external pole discrepancy device.

#### 10.3.1.6 EXTERNAL TRIP INDICATION

Protection operation from a different device can be used to initiate the Autoreclose function. By default these external trip inputs are mapped to initiate Autoreclose and to initiate breaker failure protection (if the functions are enabled). These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL however, the external device can use this product to trip connected circuit breakers.

### 10.3.2 AUTORECLOSE LOGIC INPUTS

This section provides an overview of the logic inputs, which are derived internally.

#### 10.3.2.1 TRIP INITIATION SIGNALS

The phase A, phase B and phase C trip inputs are used to initiate single-phase and three-phase autoreclose. For the Autoreclose to work, you must ensure that these Trip Input signals remain appropriately mapped in the PSL.

#### 10.3.2.2 CIRCUIT BREAKER STATUS INPUTS

Circuit breaker status information must be available as logic input(s) for Autoreclose to work. You can select whether to use CB open, CB closed, or both, as inputs. The settings are made in the *CB CONTROL* column of the menu, and you need to ensure that the PSL mapping of the chosen input(s) is correct.

#### 10.3.2.3 SYSTEM CHECK SIGNALS

System Check and Check Synchronization functions produce signals which are used by the Autoreclose logic ensure that the Autoreclose function is applied only when the system is in a suitable condition.

### 10.3.3 AUTORECLOSE LOGIC OUTPUTS

Output signals are provided to provide indication of an Autoreclose in progress (ARIP). An ARIP signal is asserted when an Autoreclose sequence starts. It remains high from initiation, either until lockout, or until successful Autoreclose.

An Autoreclose lockout condition resets any ‘Autoreclose in progress’ and associated signals. Signals are available to indicate that Autoreclose is in progress and that a circuit breakers has been successfully closed.

## 10.3.4 AUTORECLOSE OPERATING SEQUENCE

The Autoreclose sequence is controlled by so-called Dead Timers. Dead Time Control settings are used to select the conditions that initiate Dead Timers in the Autoreclose sequence (for example protection operate, protection reset, CB open, etc.). This section describes typical AR operation sequences in which Dead Timers start when protection operation resets.

*Note:*
*In a multi-shot AR sequence, a number of Dead Timers are used (one for each shot). All Dead Timers are enabled when the sequence is initiated, but each timer only starts when the particular shot with which it is associated is triggered.*

### 10.3.4.1 AR TIMING SEQUENCE - TRANSIENT FAULT

The figure below describes the operating sequence for a single-shot Autorecloser for a transient fault that clears when the faulted line is isolated.

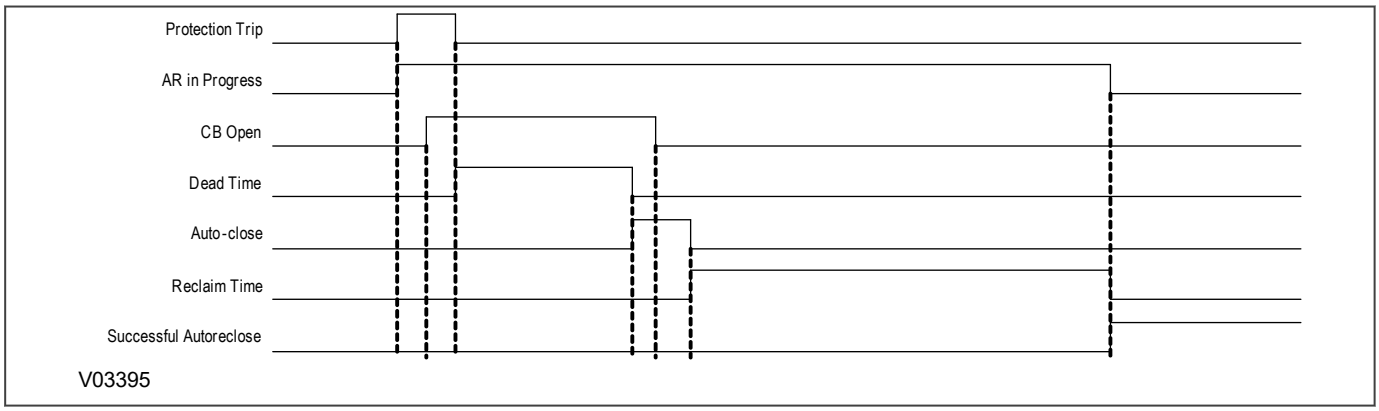


**Figure 151: Autoreclose sequence for a Transient Fault**

Following fault inception, the protection operates and issues a trip signal. At the same time the Autoreclose in Progress signal is asserted. Shortly afterwards the circuit breaker will open as indicated by the CB Open signal. Opening of the CB clears the fault and the protection resets. When this happens, the Dead Timer is started and the output remains high until the Dead Time setting expires, whereupon it resets and the Autorecloser issues the Auto-close command to close the circuit breaker. As the fault has been cleared, the circuit breaker closes and remains closed. When the Auto-close pulse is removed, the Reclaim Timer starts. If no further fault is detected before the Reclaim Timer expires, the Autoreclose is considered to be successful and this is indicated by the Successful Autoreclose signal.

### 10.3.4.2 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT

The figure below shows a single-shot AR operating sequence where the fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows an evolving fault inception occurring before the Reclaim Time has expired. When the Autorecloser recognises that the protection has tripped, the cycle is terminated. The Autorecloser goes into Lockout, and the Autoreclose in Progress signal is reset.

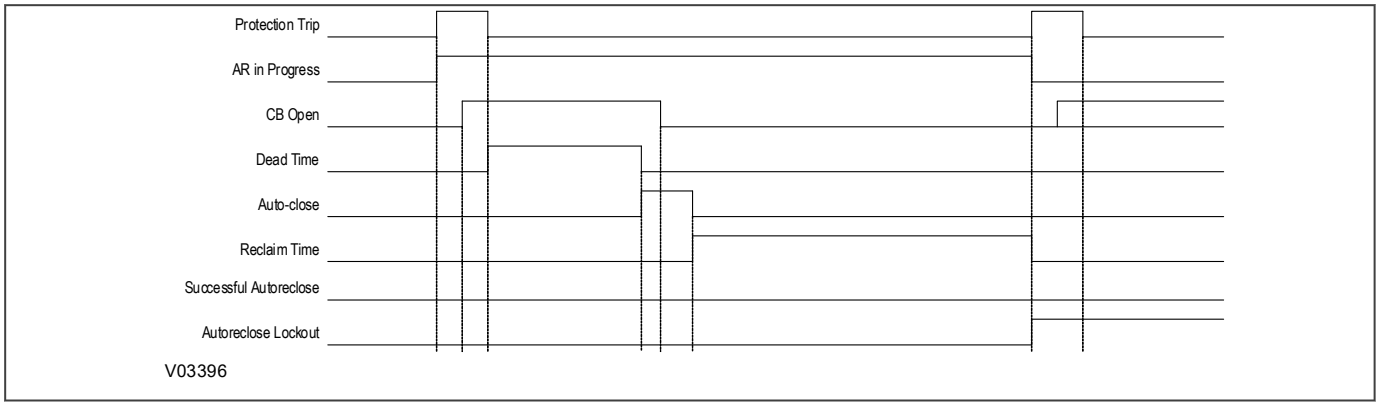


**Figure 152: Autoreclose sequence for an evolving or permanent fault**

### 10.3.4.3 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT SINGLE-PHASE

If the Autorecloser is set for single-phase operation, then single phase operation is only allowed on the first shot. Subsequent tripping will be three-phase only until the AR has been successful or until AR has locked out as shown in the figure below.

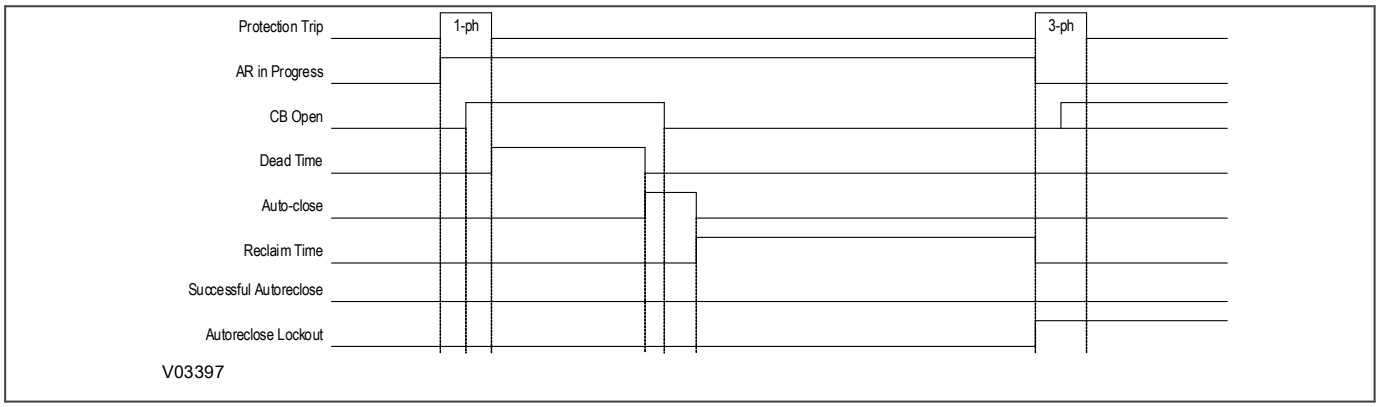


**Figure 153: Autoreclose sequence for an evolving or permanent fault - single-phase operation**

## 10.4 LOGIC MODULES

This section contains a complete set of logic diagrams, which will help to explain the Autoreclose function. Most of the logic diagrams shown are logic modules that comprise the overall Autoreclose system. Some of the diagrams shown are not directly related to Autoreclose functionality, however, they may use some inputs are produce outputs that are used by the Autoreclose system. These diagrams are shown in this section for the sake of completeness.

### 10.4.1 CIRCUIT BREAKER STATUS MONITOR

The Circuit Breaker State Monitor logic is part of the Monitoring and Control functionality and is fully described in that chapter. The logic diagram is repeated in this section because some of the outputs of this logic module are used as inputs to some of the Autoreclose logic modules.

### 10.4.1.1 CB STATE MONITOR LOGIC DIAGRAM

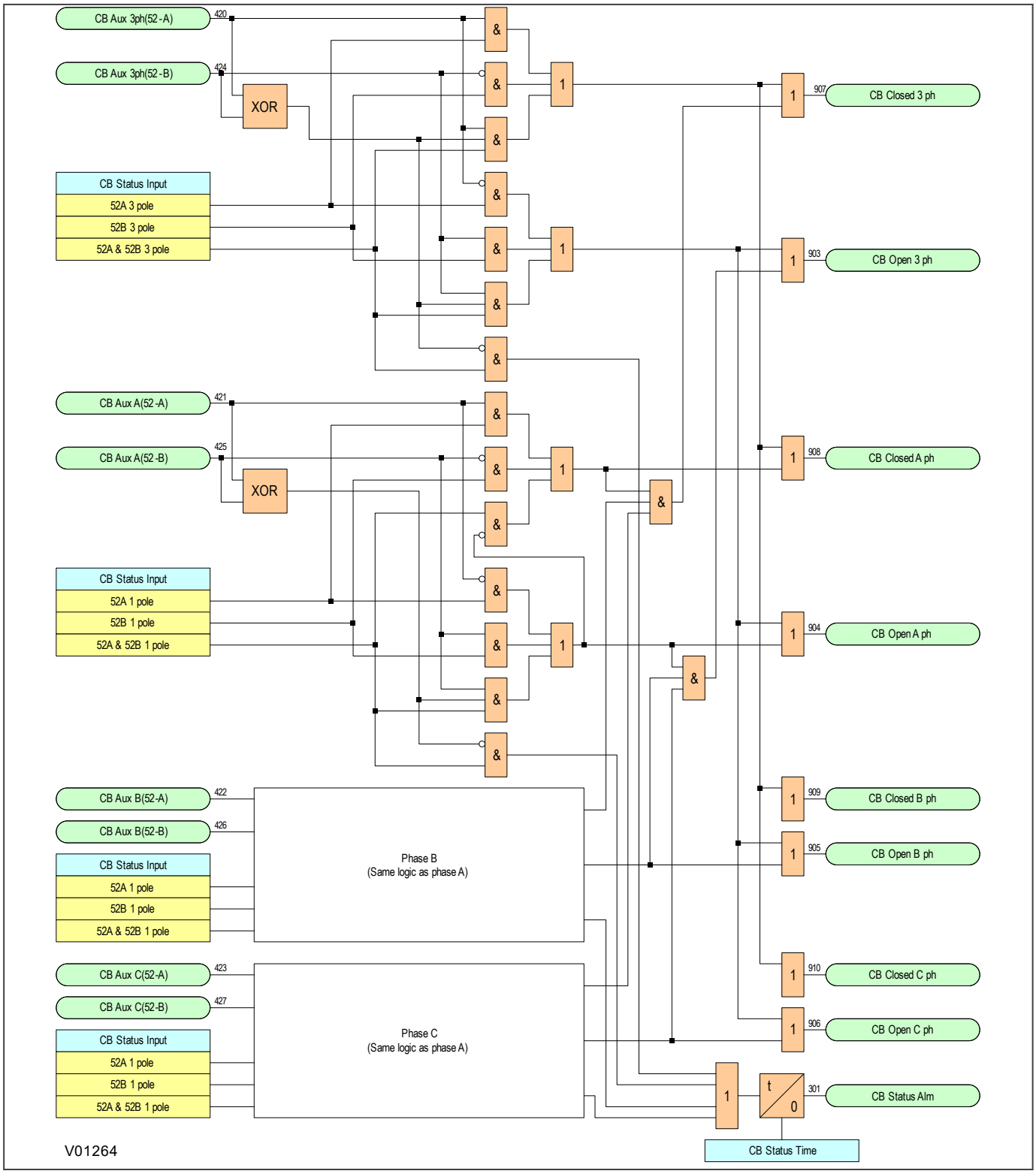


**Figure 154: CB State Monitor logic diagram (Module 1)**

## 10.4.2 CIRCUIT BREAKER OPEN LOGIC

The Circuit Breaker Open logic module produces internal signals indicating the open status of one or more phases. These signals are used by some of the Autoreclose logic modules.

### 10.4.2.1 CIRCUIT BREAKER OPEN LOGIC DIAGRAM

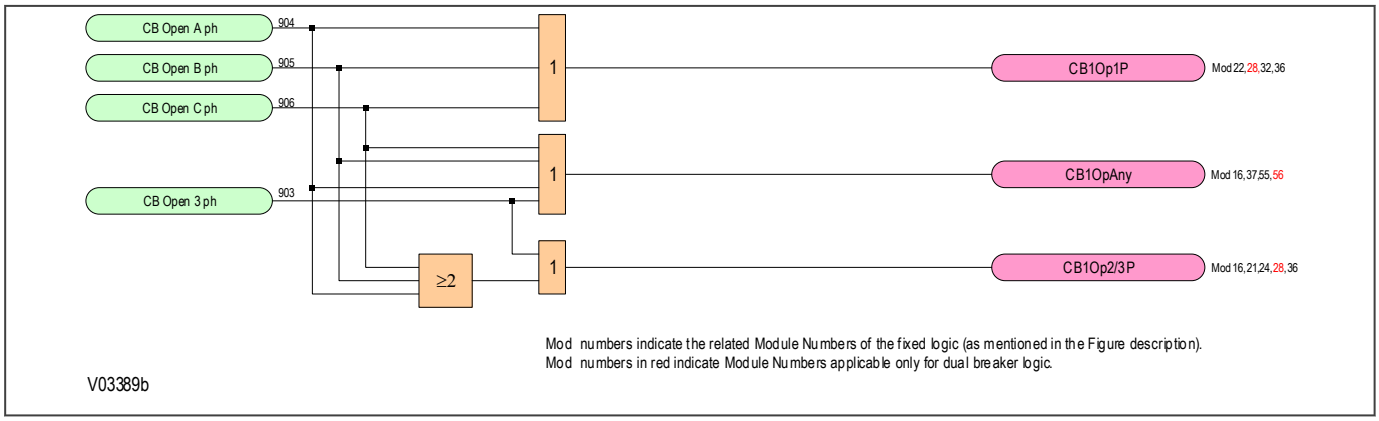


**Figure 155: Circuit Breaker Open logic diagram (Module 3)**

## 10.4.3 CIRCUIT BREAKER IN SERVICE LOGIC

For Autoreclose to proceed, a circuit breaker has to be in service when the Autoreclose is initiated. A circuit breaker is considered to be in service if it has been closed for more than the CB IS Time setting.

For applications with fast-acting circuit breaker auxiliary switches, a time delay setting CB IS Memory Time is provided. This is used to ensure correct operation if a delay between the circuit breaker tripping and recognition by the protection, is expected.

When an Autoreclose cycle starts, the “in service” signal for a circuit breaker stays set until the Autoreclose cycle finishes.

The circuit breaker “in service” signal resets if the circuit breaker opens, or if the corresponding Autoreclose in progress (ARIP) signal resets.

### 10.4.3.1 CIRCUIT BREAKER IN SERVICE LOGIC DIAGRAM

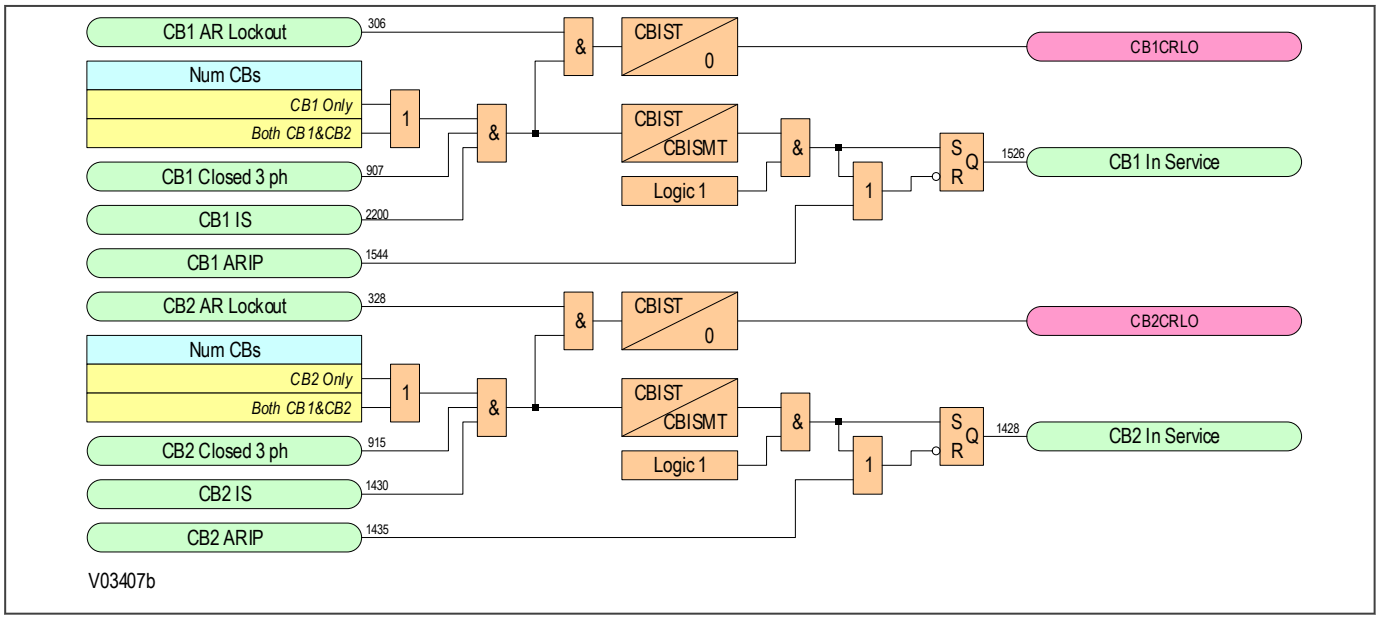


**Figure 156: CB In Service logic diagram (Module 4)**

### 10.4.3.2 AUTORECLOSE OK LOGIC DIAGRAM

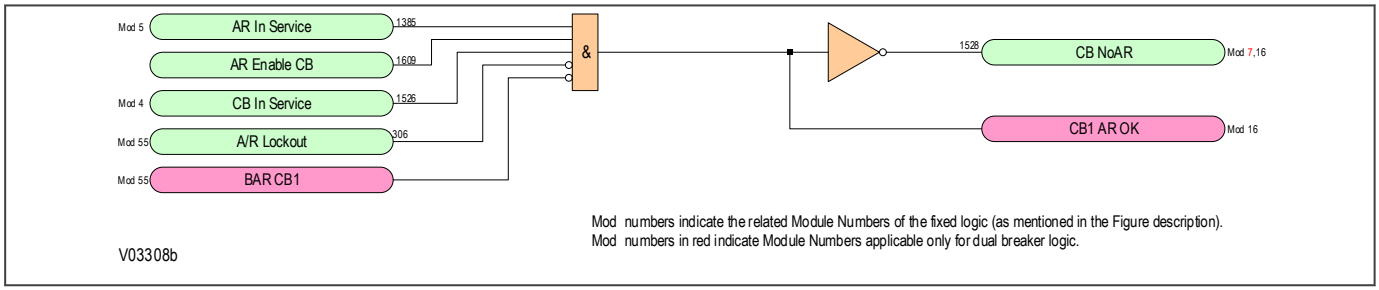


**Figure 157: Autoreclose OK logic diagram (Module 8)**

## 10.4.4 AUTORECLOSE ENABLE

The Autoreclose function must be enabled in the *CONFIGURATION* column before it can be brought into service. It can be brought into service by:

- using an opto-input mapped to the ***AR Enable*** DDB signal
- pulsing the DDB signal ***AR Pulse On*** (use ***AR Pulse Off*** to bring it out of service)
- programming a function key on the HMI.
- if applicable, using IEC 60870-5-103 communications

A further validation signal is also required to switch on Autoreclose. This is the DDB signals ***AR Enable CB***. Once Autoreclose is in service, the ***AR In Service*** DDB signal is asserted and the ***AR Status*** cell in the *CB CONTROL* column is set accordingly.

#### 10.4.4.1 AUTORECLOSE ENABLE LOGIC DIAGRAM

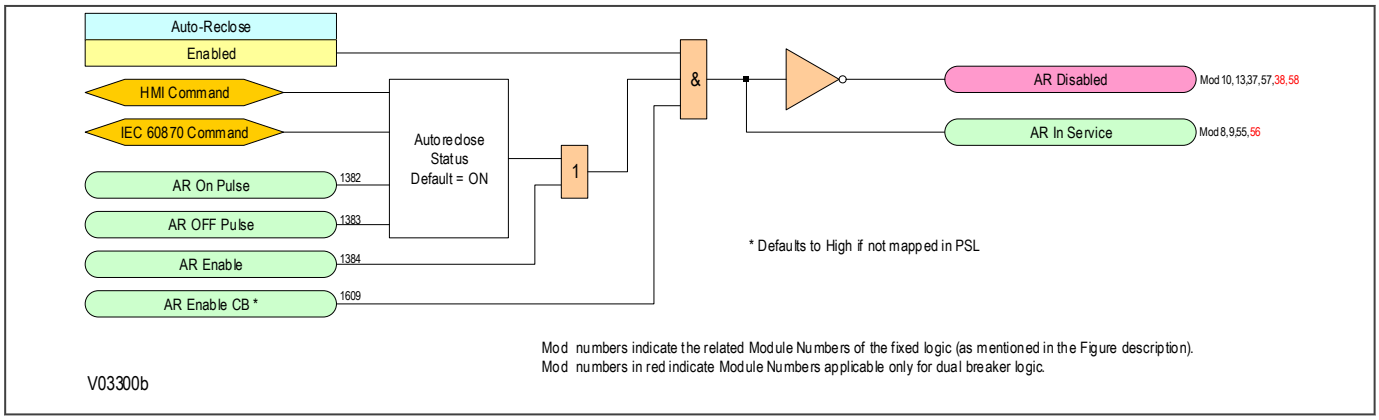


**Figure 158: Autoreclose Enable logic diagram (Module 5)**

## 10.4.5 AUTORECLOSE MODES

The device can provide Single-phase and/or Three-phase Autoreclose. The Autoreclose mode is configured by the ***AR Mode*** setting in the *AUTORECLOSE* column. You can choose from:

- Single-phase (*AR 1P*)
- Three-phase (*AR 3P*)
- Single-phase and Three-phase (*AR 1/3P*)
- Controlled by commands from DDB signals that must be mapped to opto-isolated inputs in the PSL (*AR Opto*).

Single-phase Autoreclosing is permitted only for the first shot of an Autoreclose cycle. In a multi-shot Autoreclose cycle the second and subsequent trips will always be three-phase.

For multi-phase faults, you can use the ***Multi Phase AR*** setting in the *AUTORECLOSE* column to configure the following options:

- Allow Autoreclose for all fault types (*Allow Autoclose*)
- Block Autoreclose for 2-phase and 3-phase faults (*BAR 2 and 3 ph*)
- Block Autoreclose for 3-phase faults (*BAR 3 Phase*)

### 10.4.5.1 SINGLE-PHASE AND THREE-PHASE AUTORECLOSE

#### Single-phase Autoreclose Only

If single-phase Autoreclose is enabled, the logic allows only a single shot Autoreclose. For a single-phase fault, the single phase dead timer ***SP AR Dead Time*** starts, and the DDB signal ***CB AR 1pole in prog*** is asserted, which indicates that single-phase Autoreclose is in progress. In this case, for a multi-phase fault the logic triggers a three-phase trip and goes to lockout.

#### Three-phase Autoreclose Only

During three-phase Autoreclose, for any fault, the three-phase dead timers: ***3P AR DT Shot 1***, ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** are started and the DDB signal ***CB AR 3pole in prog*** is asserted, which indicates that three-phase Autoreclose is in progress.

If three-phase only Autoreclose is enabled, the logic forces a three-phase trip by setting the DDB signal ***AR Force 3 pole*** for any single-phase fault.

### Single-phase and Three-phase Autoreclose

With single-phase and three-phase Autoreclose enabled then, if the first fault is a single-phase fault the single-phase dead time ***SP AR Dead Time*** is started and the single-phase Autoreclose in progress signal is asserted. If the first fault is a multi-phase fault the three phase dead timer ***3P AR DT Shot 1*** is started and the three-phase Autoreclose in progress signal is asserted. If set to allow more than one reclose (***AR Shots*** >'1') then any subsequent faults are converted to three-phase trips by setting the force three-pole tripping signal. The three-phase dead times ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** (Dead Times 2, 3, 4) are started for the 2nd, 3rd and 4th trips (shots) respectively. The DDB signal ***AR 3pole in prog*** is asserted. If a single-phase fault evolves to a multi-phase fault during the single-phase dead time (***SP AR Dead Time***), single-phase Autoreclose is stopped. The single-phase Autoreclose in progress signal is reset, the three-phase Autoreclose in progress signal is set, and the three-phase dead timer ***3P AR DT Shot 1*** is started.

### 10.4.5.2 AUTORECLOSE MODES ENABLE LOGIC DIAGRAM

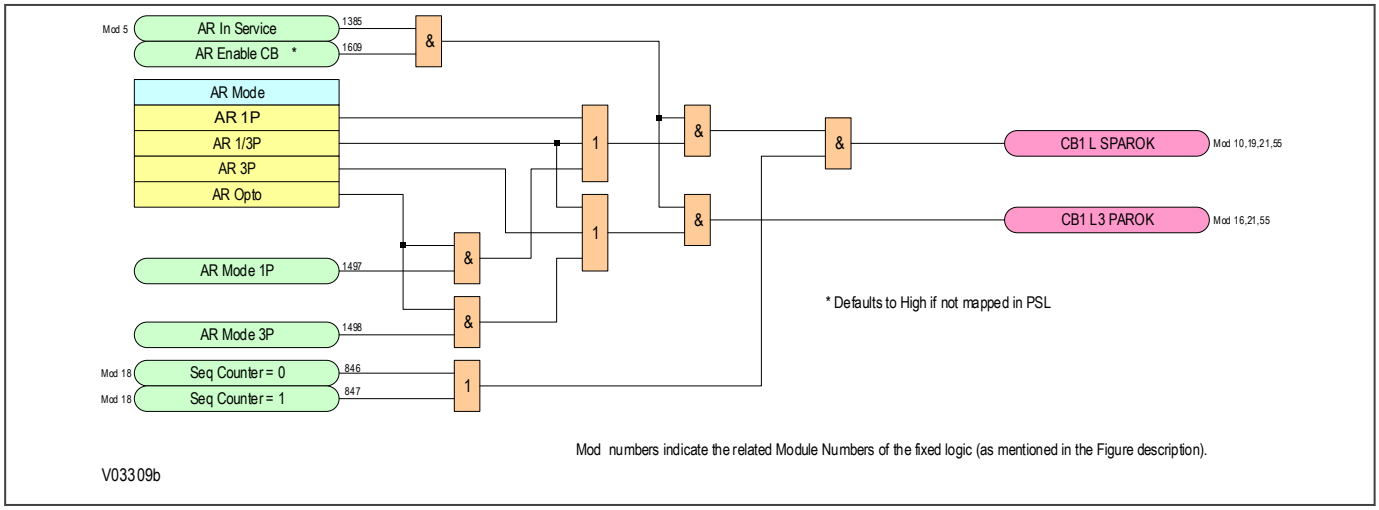


**Figure 159: Autoreclose Modes Enable logic diagram (Module 9)**

## 10.4.6 AR FORCE THREE-PHASE TRIP LOGIC

Following single-phase tripping, while the Autoreclose cycle is in progress, and upon resetting of the protection elements, tripping switches to three-phase.

Any protection operations that occur for subsequent faults while the Autoreclose cycle remains in progress will be tripped three-phase.

### 10.4.6.1 AR FORCE THREE-PHASE TRIP LOGIC DIAGRAM

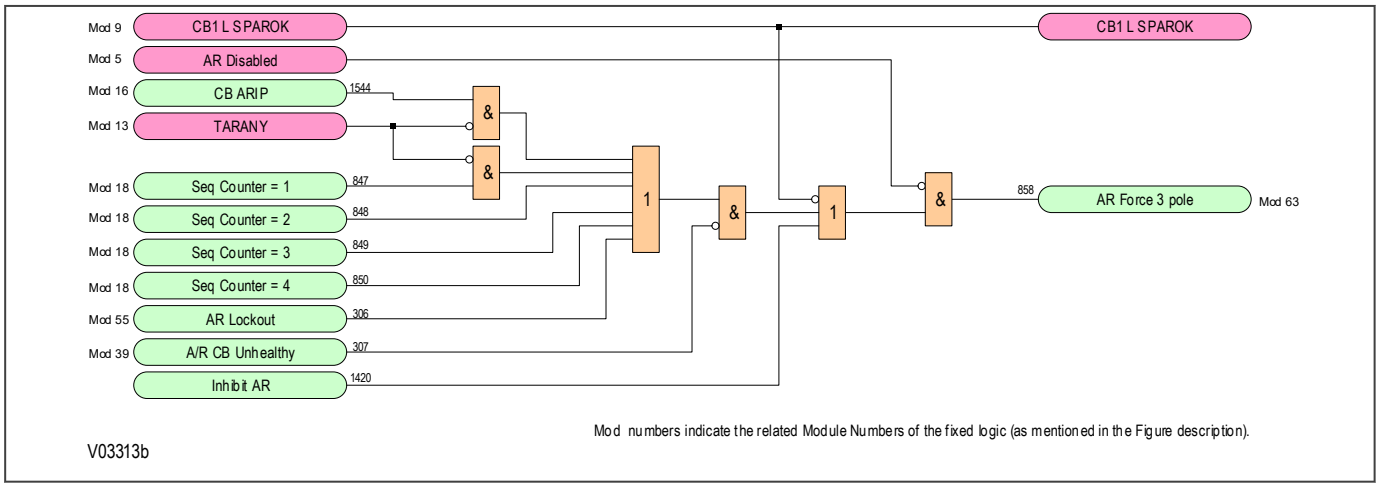


**Figure 160: Force Three-phase Trip logic diagram (Module 10)**

When a three-phase trip is forced, the DDB signal ***AR Force 3 pole*** is asserted.

## 10.4.7 AUTORECLOSE INITIATION LOGIC

Autoreclose initiation starts Autoreclose for a circuit breaker only if Autoreclose is enabled for the circuit breaker, and the circuit breaker is in service. When an Autoreclose cycle is started, Autoreclose in progress (ARIP) is indicated. The indication remains until the end of the cycle. The end of the cycle is signified by successful Autoreclose, or by lockout.

Autoreclose cycles can be initiated by:

- Protection functions internal to the product
- A Trip Test feature
- External protection equipment
- Evolving fault combinations

### Internal Protection Functions

Many of the protection functions in the product can be programmed to initiate or block Autoreclose. The associated settings are found in the Autoreclose column and the available options are `No Action`, `Initiate AR`, or `Block AR`. If set to `Block AR` operation of the protection function blocks the Autoreclose function and forces a lockout.

### Trip Test Feature

The ***Test Autoreclose*** command cell in the *COMMISSION TESTS* column can be used to initiate an Autoreclose cycle. Each option provides a 100 ms pulse output. There is also a 'No Operation' option to exit the command field without initiating a test.

### External Protection Equipment

Protection operation from a different device can be used to initiate Autoreclose via PSL. By default these external trip input signals are mapped to initiate Autoreclose. These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL, however, the external device can use this product to trip connected circuit breakers.

### Evolving Fault Combinations

The Autoreclose function would normally be initiated by a single condition (such as a single-phase fault). If, however, the system conditions evolve such that other conditions that could initiate Autoreclose, then the dynamics of the Autoreclose logic need to adapt. For example, if a single-phase fault evolves into a multi-phase fault, then the operation of the Autorecloser must consequently adapt. To achieve this signals are generated to indicate conditions such as evolving faults, re-operation of protection, combinations of initiation by internal protection, external protection, or test features, which control the Autoreclose sequencing.

Records of initiating conditions are stored and used to control the sequencing. Initiation can be from a protection function integrated in the product, from external protection and internal sources such as the Autoreclose test function. Initiation can be further qualified by the phases causing the initiation. These conditions are stored in signals that generally feature “MEM”- memory, or “AR” – Autoreclose, in the signal name.

## 10.4.7.1 AUTORECLOSE INITIATION LOGIC DIAGRAM

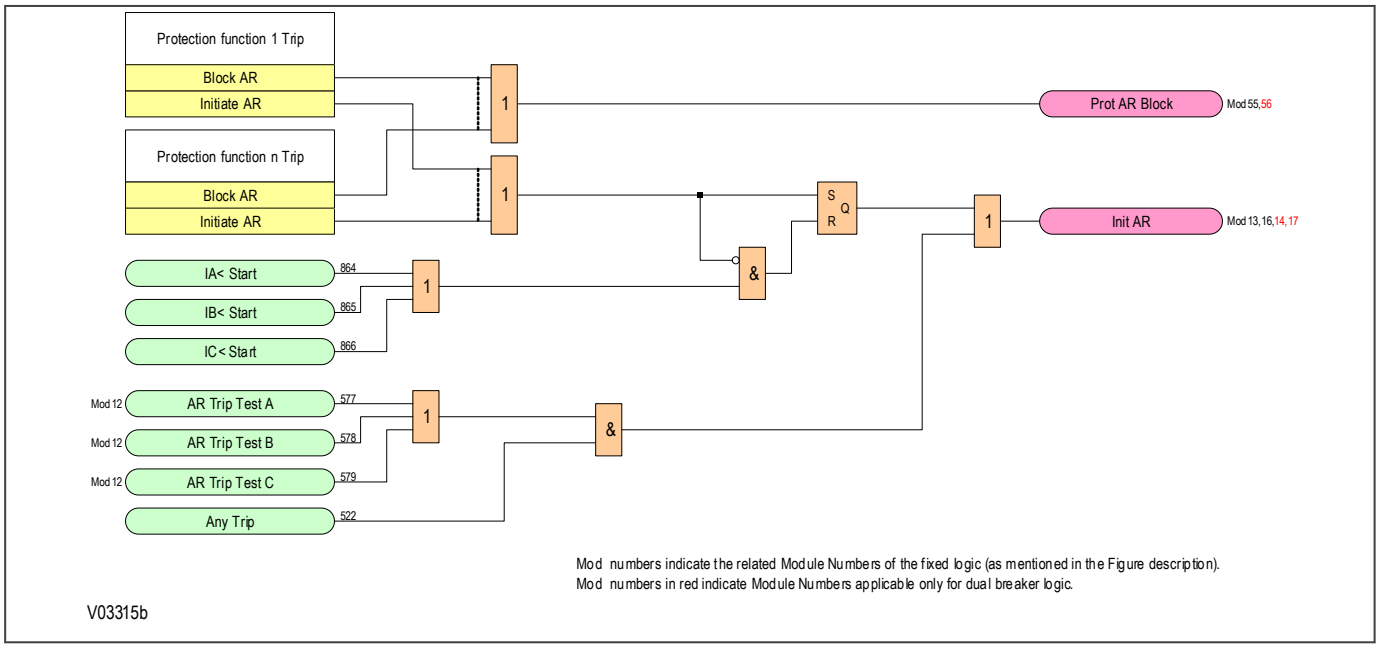


**Figure 161: Autoreclose Initiation logic diagram (Module 11)**

### 10.4.7.2 AUTORECLOSE TRIP TEST LOGIC DIAGRAM

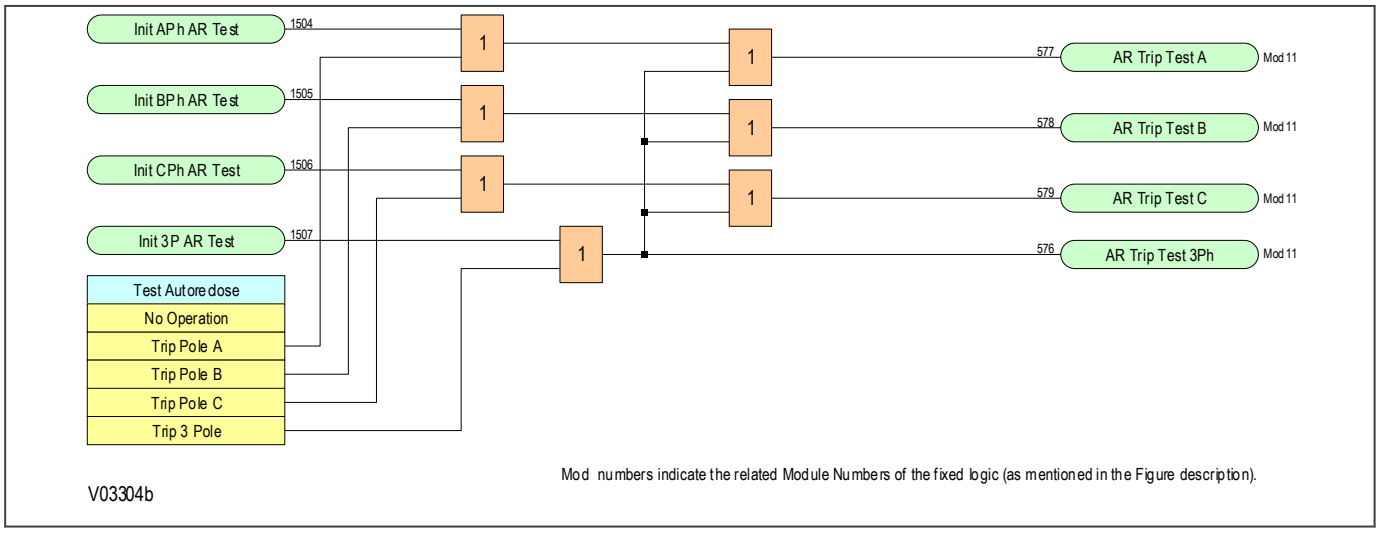


**Figure 162: Autoreclose Trip Test logic diagram (Module 12)**

### 10.4.7.3 AR EXTERNAL TRIP INITIATION LOGIC DIAGRAM

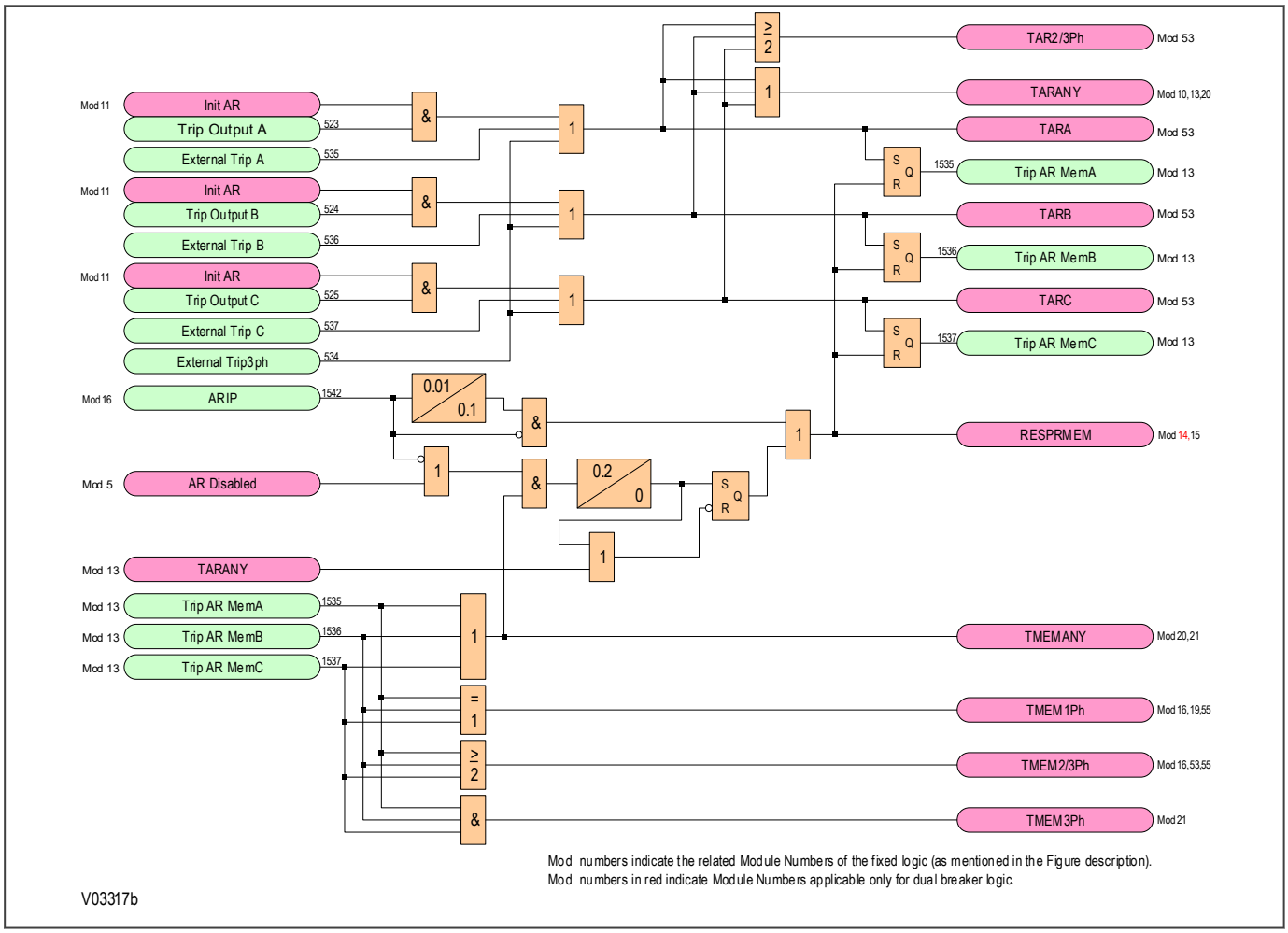


**Figure 163: Autoreclose initiation by external trip or evolving conditions (Module 13)**

*Note:*
*The signals must be mapped as shown in the default PSL scheme.*

### 10.4.7.4 PROTECTION REOPERATION AND EVOLVING FAULT LOGIC DIAGRAM

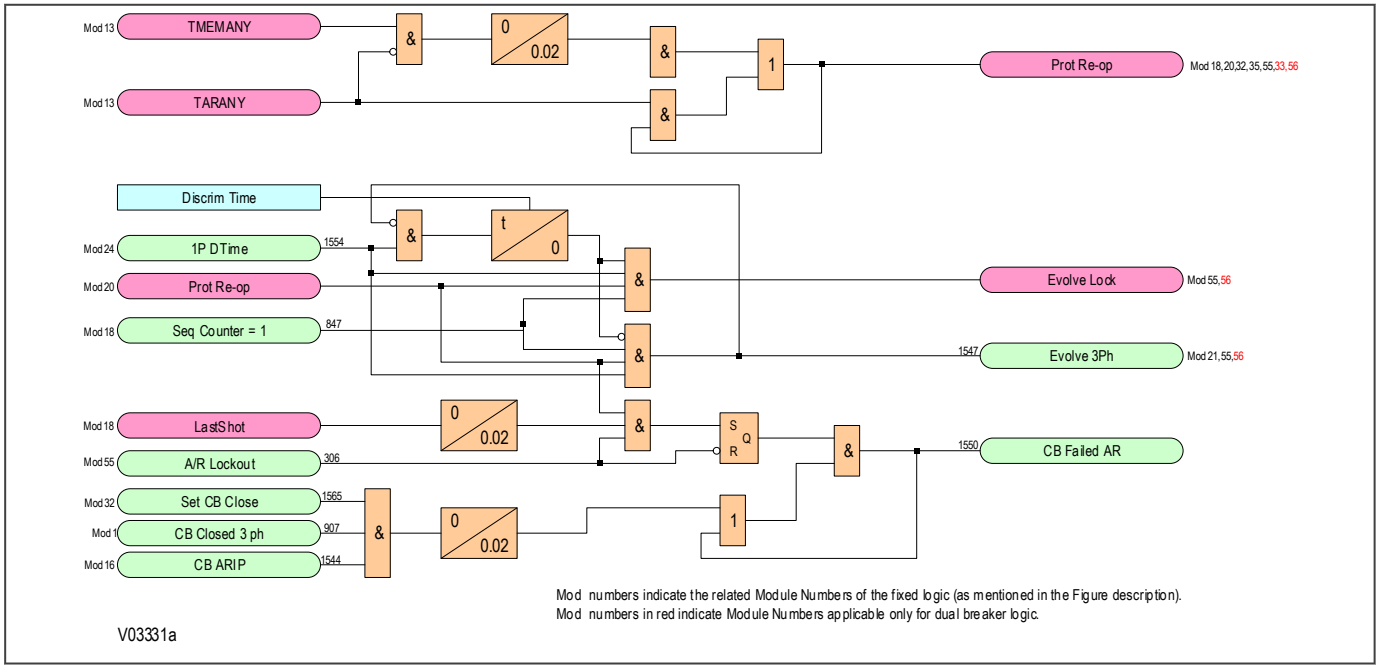


**Figure 164: Protection Reoperation and Evolving Fault logic diagram (Module 20)**

### 10.4.7.5 FAULT MEMORY LOGIC DIAGRAM

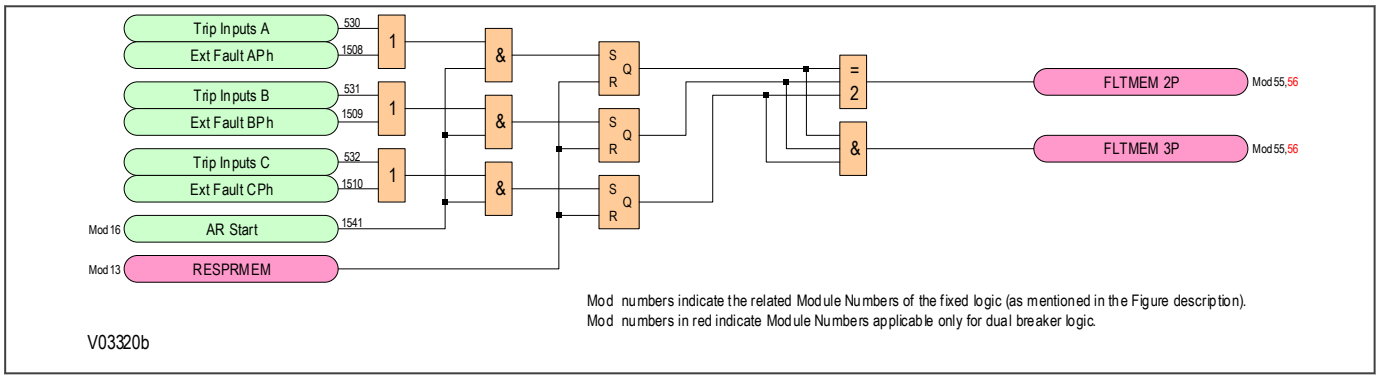


**Figure 165: Fault Memory logic diagram (Module 15)**

## 10.4.8 AUTORECLOSE IN PROGRESS

The AR In Progress module produces various signals to indicate to other modules and functions that an Autoreclose operation is currently in progress.

### 10.4.8.1 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM

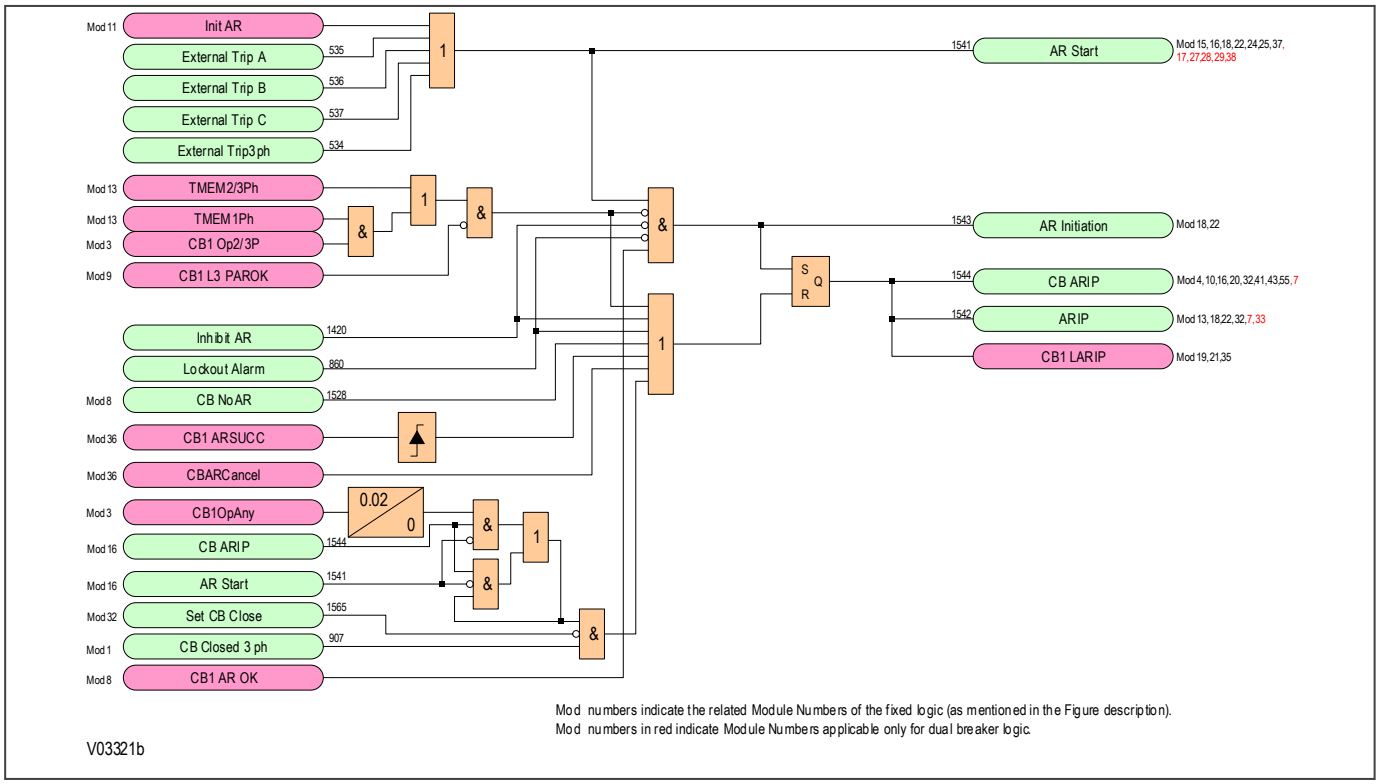


**Figure 166: Autoreclose In Progress logic diagram (Module 16)**

## 10.4.9 SEQUENCE COUNTER

The Autoreclose logic includes a counter for counting the number of Autoreclose shots. This is referred to as the sequence counter. The sequence counter has a value of zero if Autoreclose is not in progress. Following a trip, and subsequent Autoreclose initiation, the sequence counter is incremented. The counter provides output signals indicating how many initiation events have occurred in any Autoreclose cycle. These signals are available as user indications and are used in the logic to select the appropriate dead times or, for a persistent fault, force a lockout.

It is possible to skip the first Autoreclose attempt by enabling the ***AR Skip Shot 1*** setting. If this is set, the sequence counter will skip the first Autoreclose attempt (Shot 1) and move to the second (Shot 2) immediately upon Autoreclose initiation. Each time the protection trips the sequence counter is incremented by 1. The Autoreclose logic compares the sequence counter value to the number of Autoreclose shots setting ***AR Shots***. If the counter value exceeds this setting then the Autoreclose is locked out. If Autoreclose is successful, the sequence counter resets to zero.

### 10.4.9.1 AUTORECLOSE SEQUENCE COUNTER LOGIC DIAGRAM

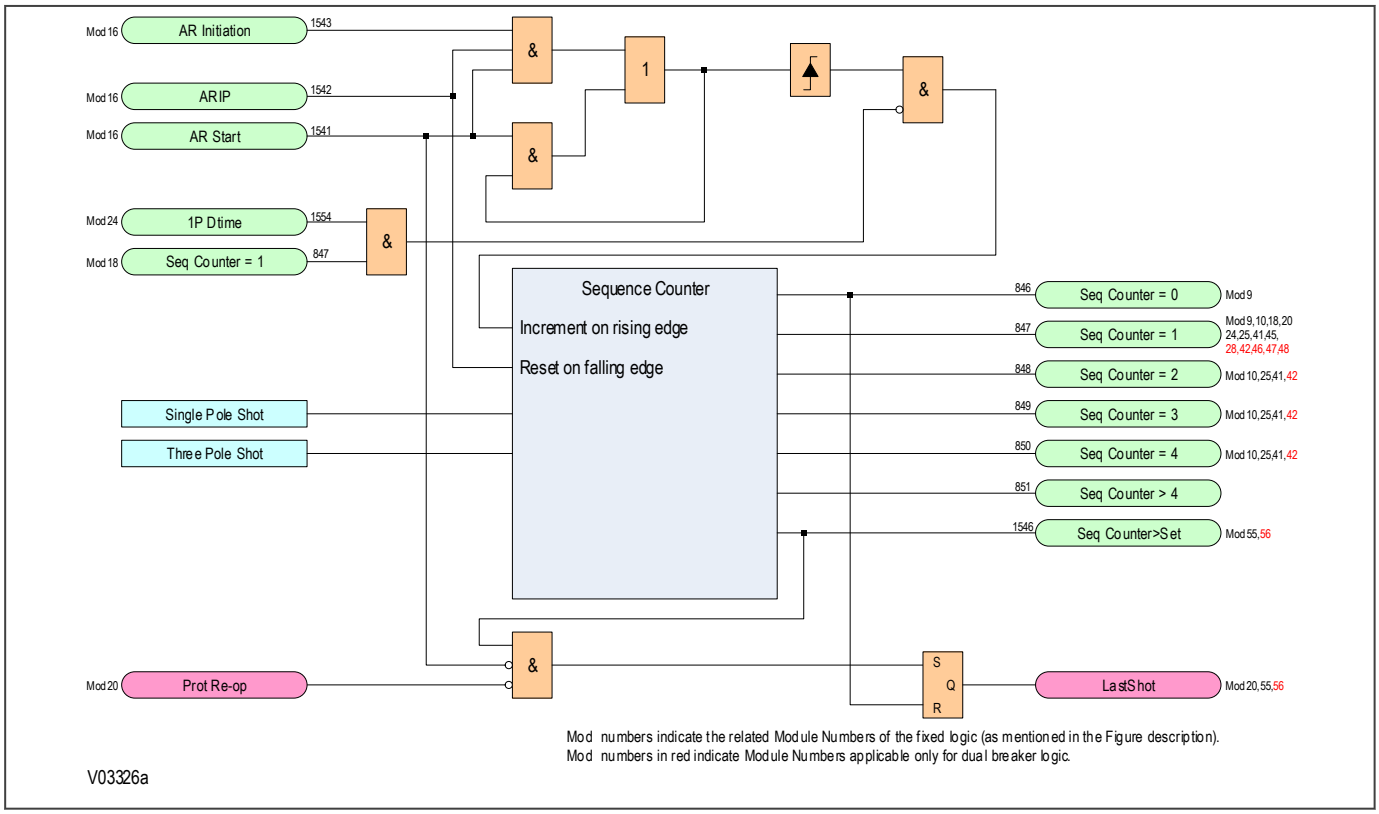


**Figure 167: Autoreclose Sequence Counter logic diagram (Module 18)**

## 10.4.10 AUTORECLOSE CYCLE SELECTION

The Autoreclose cycle selection logic is responsible for determining whether the Autoreclose will start as single-phase or three-phase.

### 10.4.10.1 SINGLE-PHASE AUTORECLOSE CYCLE SELECTION LOGIC DIAGRAM

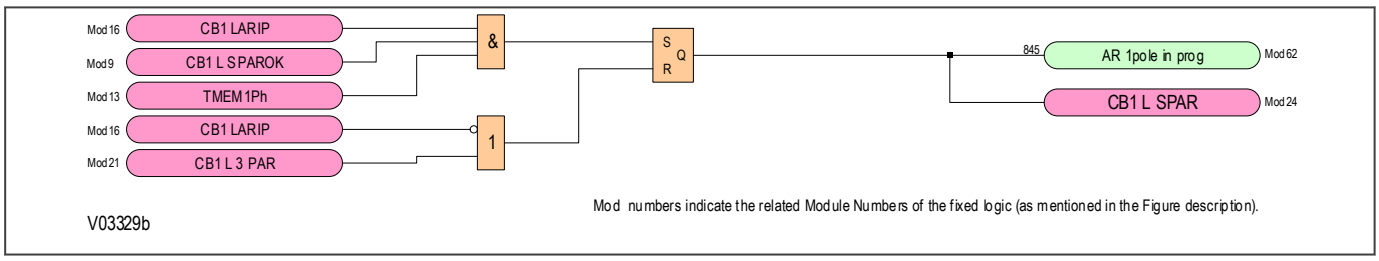


**Figure 168: Single-phase Autoreclose Cycle Selection logic diagram (Module 19)**

### 10.4.10.2 3-PHASE AUTORECLOSE CYCLE SELECTION

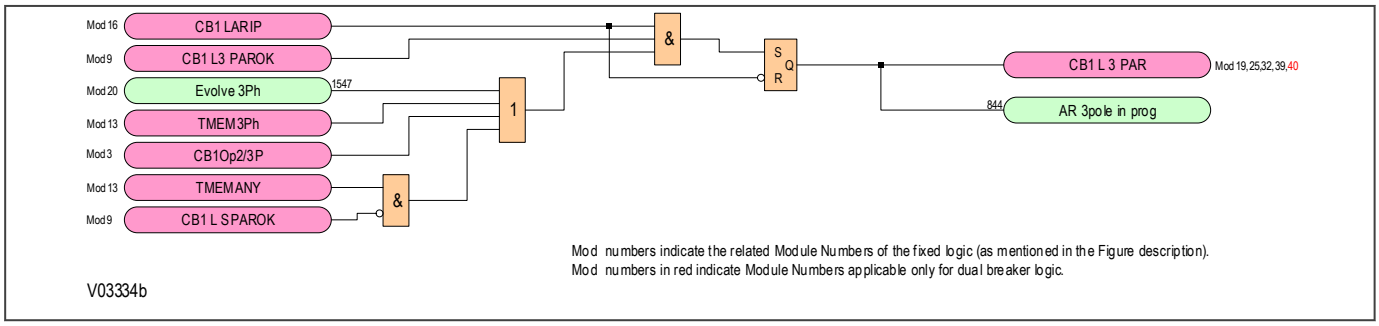


**Figure 169: Three-phase Autoreclose Cycle Selection logic diagram (Module 21)**

## 10.4.11 DEAD TIME CONTROL

Once an Autoreclose cycle has started, the conditions to enable the dead time to run are determined by the menu settings, the circuit breaker status, the protection status, the nature of the AR cycle (single-phase or three-phase), and the opto-isolated inputs from external sources.

Three settings are involved in controlling the dead time start:

- ***DT Start by Prot***
- ***3PDTStart WhenLD***
- ***DTStart by CB Op***

The ***DT Start by Prot*** determines how the protection action will initiate a dead time. The setting is always visible and has three options `Protection Reset`, `Protection Op` (protection operation), and `Disable` which should be selected if you don't want protection action to start the dead time. These options set the basic conditions for starting the dead time.

Selecting protection operation to start the dead time can, optionally, be qualified by a check that the line is dead.

Selecting protection reset to start the dead time can, optionally, be qualified by a check, that the circuit breaker is open (***DTStart by CB Op***) before starting the dead time. For three-phase tripping applications, there is a further option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time.

If ***DT Start by Prot*** is disabled, the circuit breaker must be open for the dead time to start. For three-phase tripping applications, there is an option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time. To check that the line is dead, set ***3PDTStart WhenLD*** to `enabled`. To check that the circuit breaker is open, set ***DTStart by CB Op*** to `Enabled`.

### 10.4.11.1 DEAD TIME START ENABLE LOGIC DIAGRAM

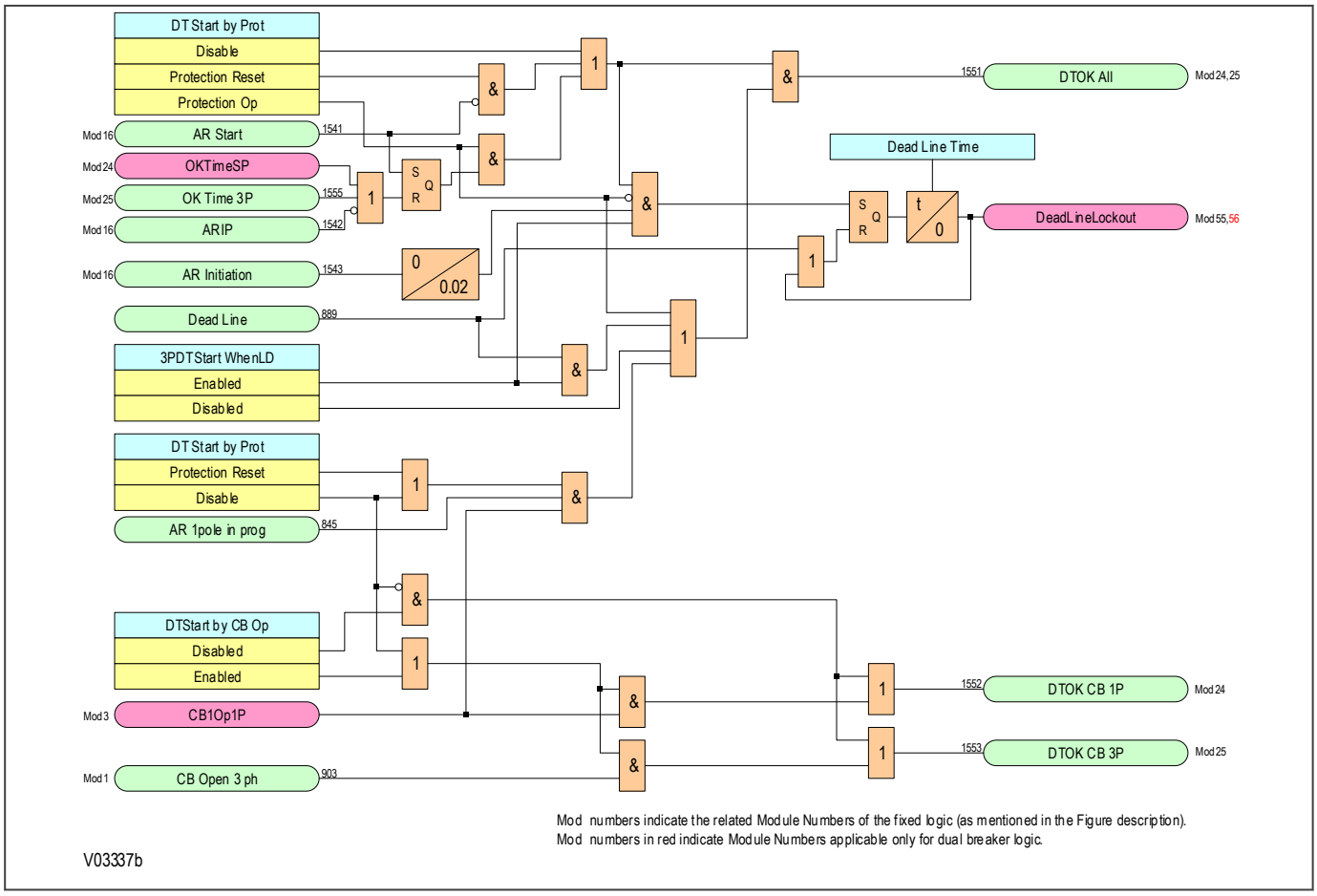


**Figure 170: Dead time Start Enable logic diagram (Module 22)**

### 10.4.11.2 1-PHASE DEAD TIME LOGIC DIAGRAM

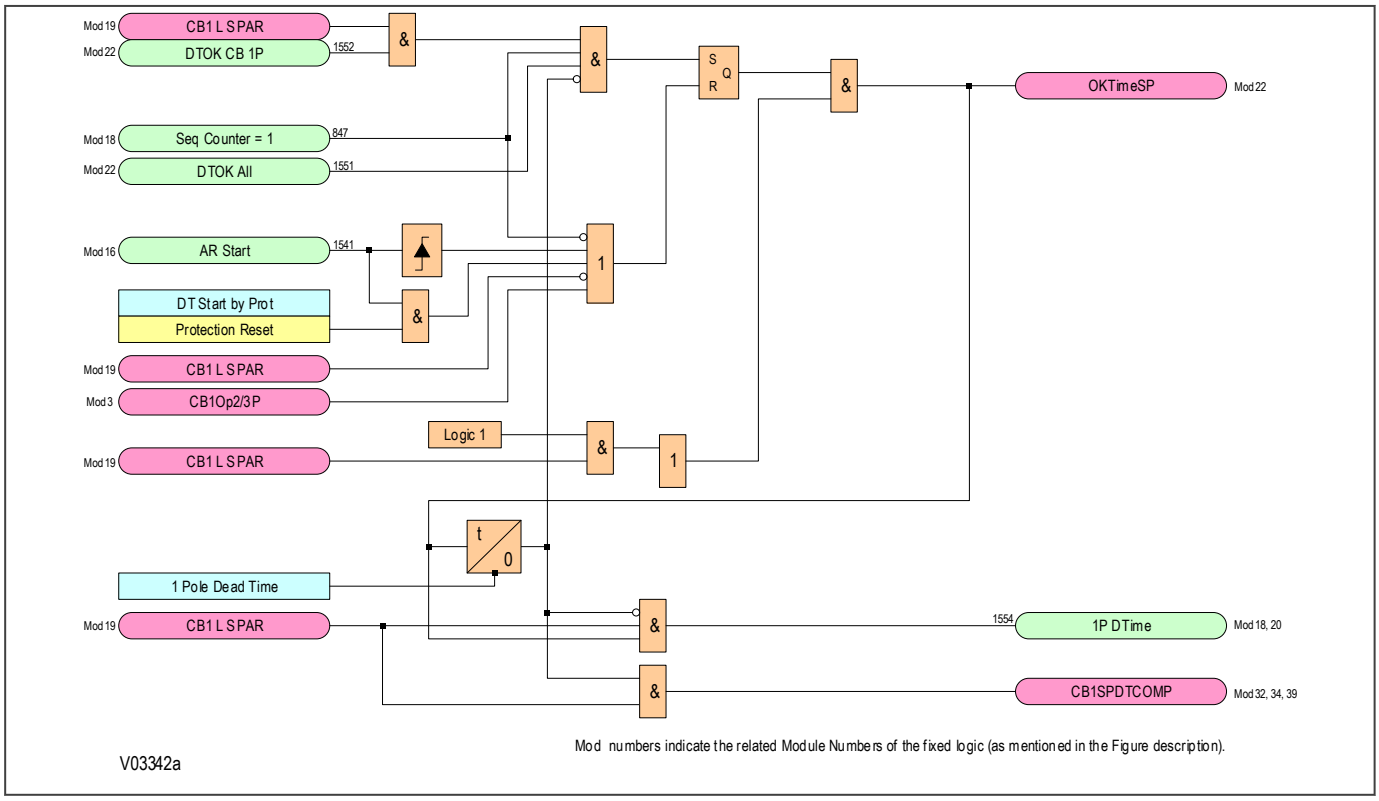


**Figure 171: Single-phase Dead Time logic diagram (Module 24)**

### 10.4.11.3 3-PHASE DEAD TIME LOGIC DIAGRAM

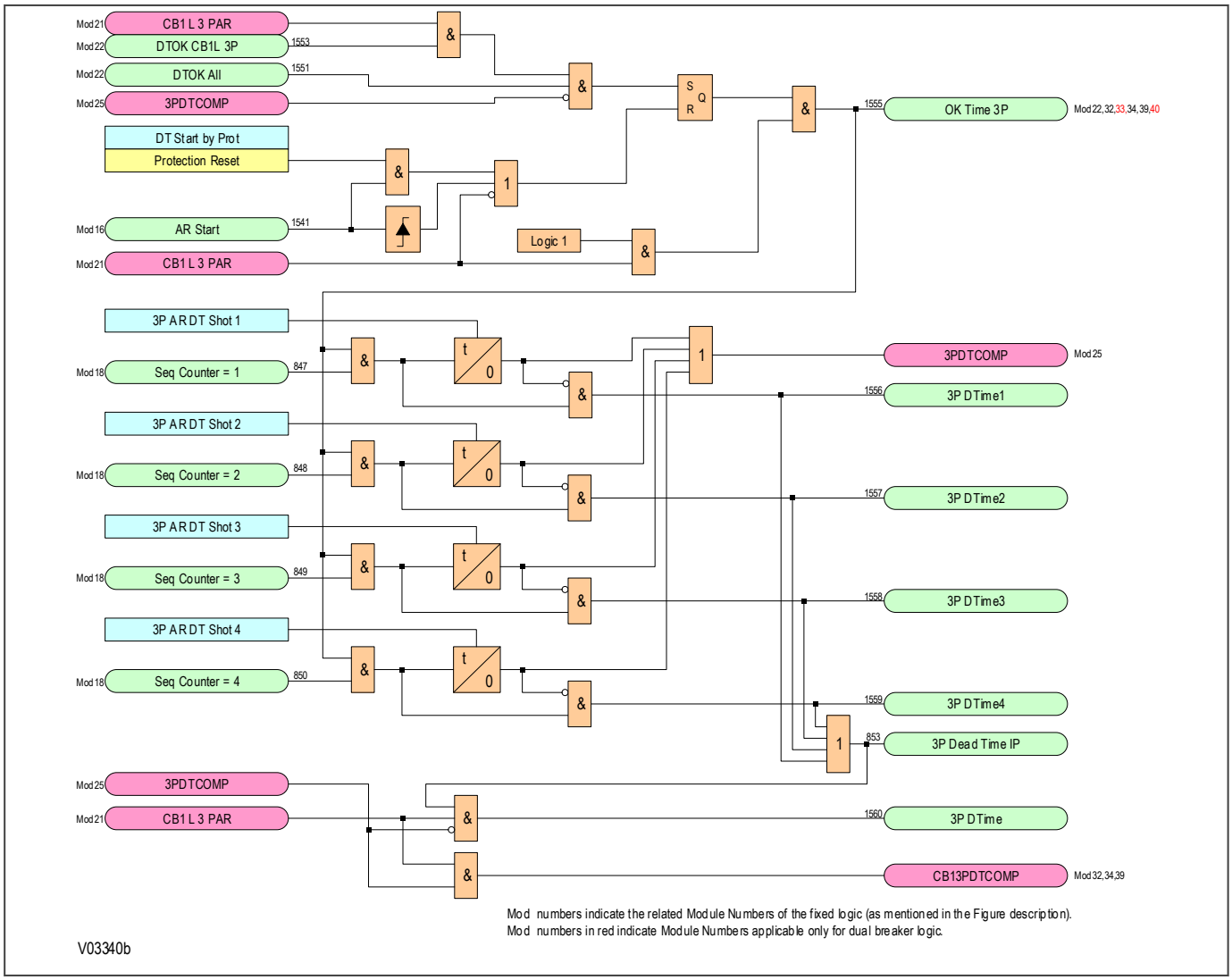


**Figure 172: Three-phase Dead Time logic diagram (Module 25)**

## 10.4.12 CIRCUIT BREAKER AUTOCLOSE

Autoclose logic takes effect when dead times have expired.

The Autoclose logic checks that all necessary conditions are satisfied before issuing an Autoclose command to the circuit breaker control scheme.

Before a circuit breaker can be closed, it must be healthy (sufficient energy to close, and if necessary re-trip) and it must not be in a lockout condition.

For three-phase Autoreclose, the circuit breaker must be open on all three phases and the appropriate system check conditions must be met. For single-phase Autoreclose, the circuit breaker must be open on that phase.

The Autoclose command is a pulse lasting 100 milliseconds. Another command (***Set CB Close***) to set the circuit breaker to close is asserted as well as the Autoclose command. This signal will remain set either until the end of the Autoreclose cycle, or until the next protection operation. These commands are used to initiate the Reclaim Time logic and the Autoreclose Shot Counter logic.

### 10.4.12.1 CIRCUIT BREAKER AUTOCLOSE LOGIC DIAGRAM

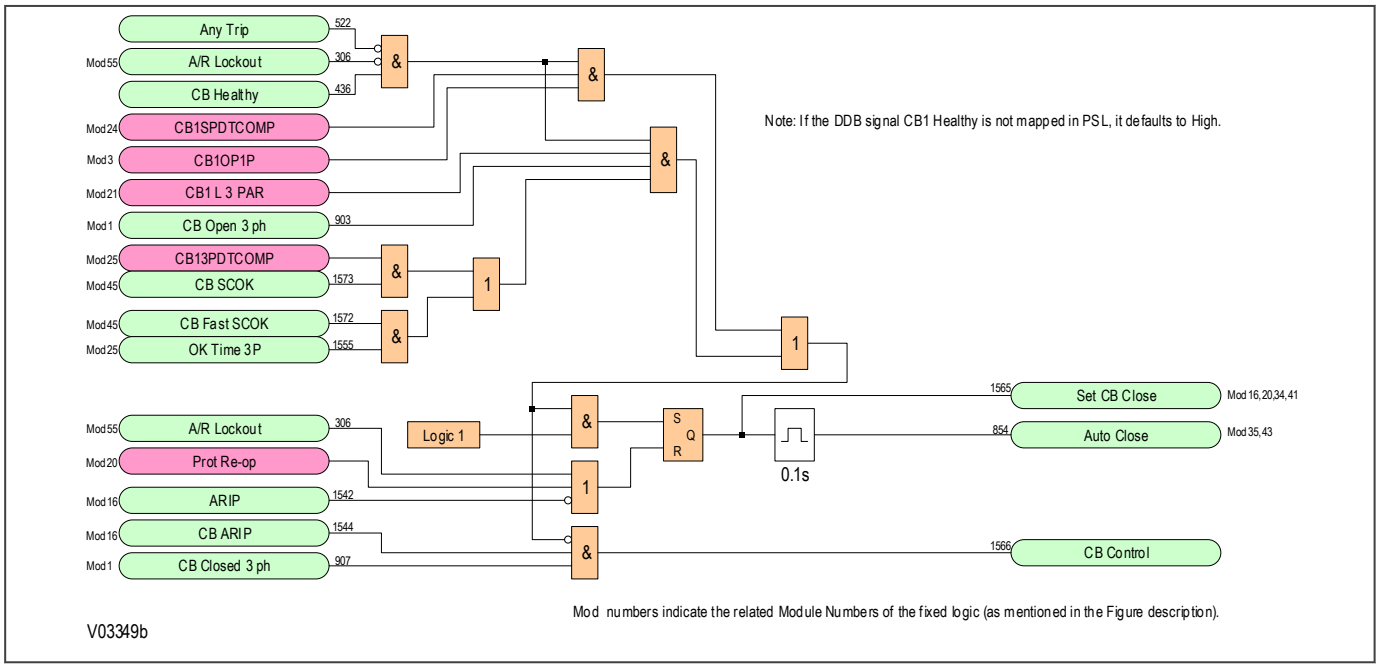


**Figure 173: Circuit Breaker Autoclose Logic Diagram (Module 32)**

## 10.4.13 RECLAIM TIME

If the protection operates again before the reclaim time has expired, the corresponding sequence counter is incremented. At the same time, any “dead time complete” (….DTCOMP) signals are reset and the logic is prepared for the next dead time to start when conditions are suitable. The operation also resets the signal that would set the circuit breaker to close, and stops and resets the reclaim timer. The reclaim time starts again if the signal to set a circuit breaker to close goes high following completion of a dead time in a subsequent Autoreclose cycle.

If the circuit breaker is closed and has not tripped again when the reclaim time expires, signals are generated to indicate successful Autoreclose. These signals increment the relevant circuit breaker successful Autoreclose shot counters and reset the relevant Autoreclose in progress signal.

The “successful Autoreclose” signals generated from the logic can be reset by various commands and settings options available under *CB CONTROL* menu settings as follows:

If ***Res AROK by UI*** is set to `Enabled`, all the signals can be reset by user interface command ***Reset AROK Ind*** from the *CB CONTROL* menu.

If ***Res AROK by NoAR*** is set to `Enabled`, the signals for each circuit breaker can be reset by temporarily generating an Autoreclose disabled signal according to the logic shown.

If ***Res AROK by Ext*** is set to `Enabled`, the signals can be reset by activation of an external input signal appropriately mapped in the PSL.

If ***Res AROK by TDly*** is set to `Enabled`, the signals are automatically reset after a time delay set in ***AROK Reset Time***.

### 10.4.13.1 PREPARE RECLAIM INITIATION LOGIC DIAGRAM

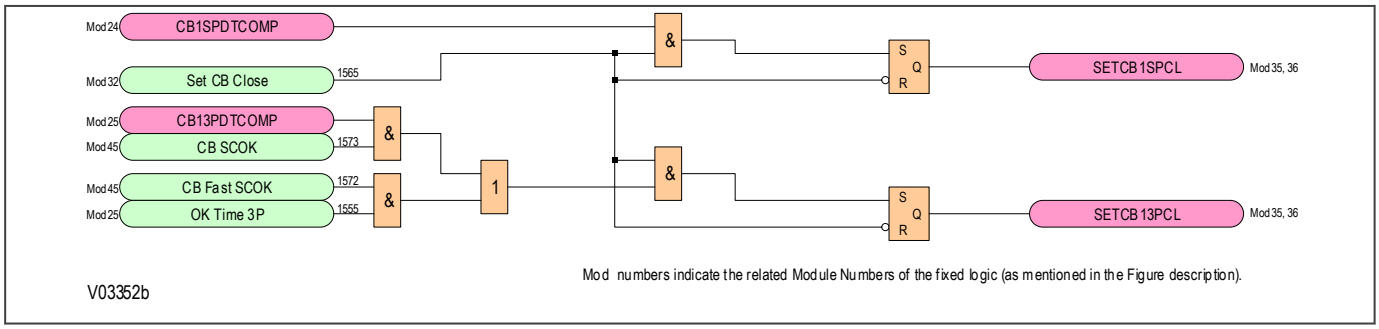


**Figure 174: Prepare Reclaim Initiation Logic Diagram (Module 34)**

### 10.4.13.2 RECLAIM TIME LOGIC DIAGRAM

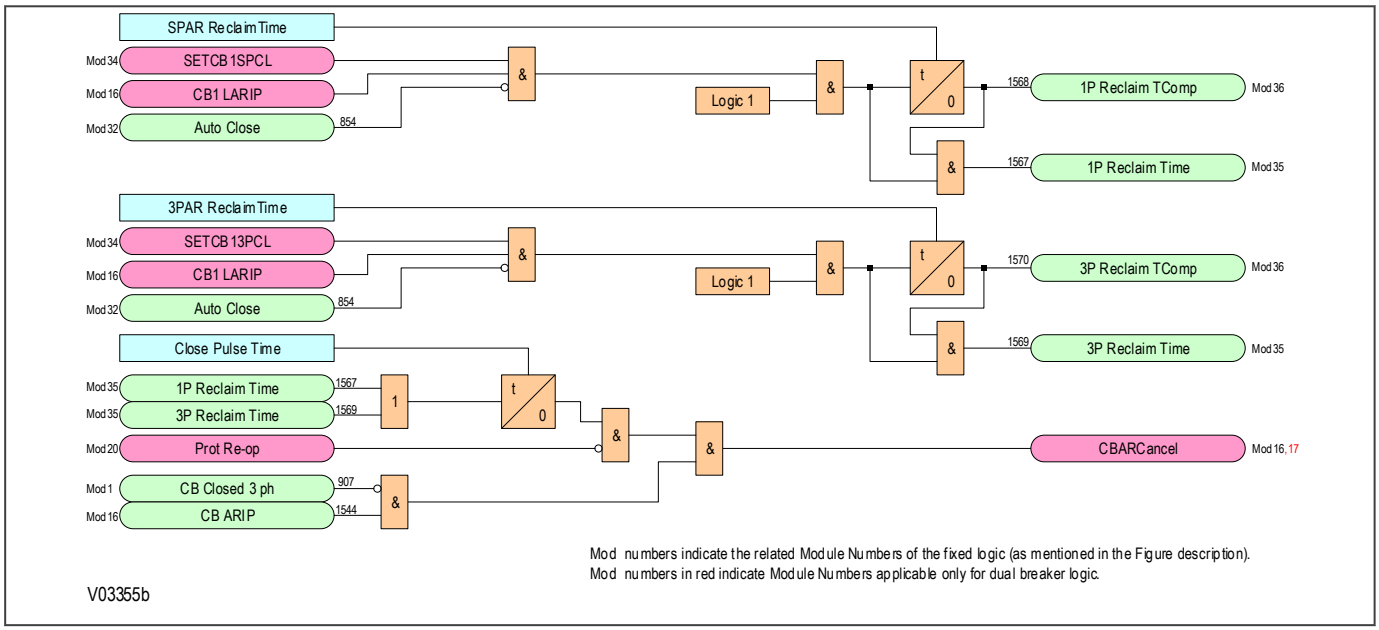


**Figure 175: Reclaim Time logic diagram (Module 35)**

### 10.4.13.3 SUCCESSFUL AUTORECLOSE SIGNALS LOGIC DIAGRAM

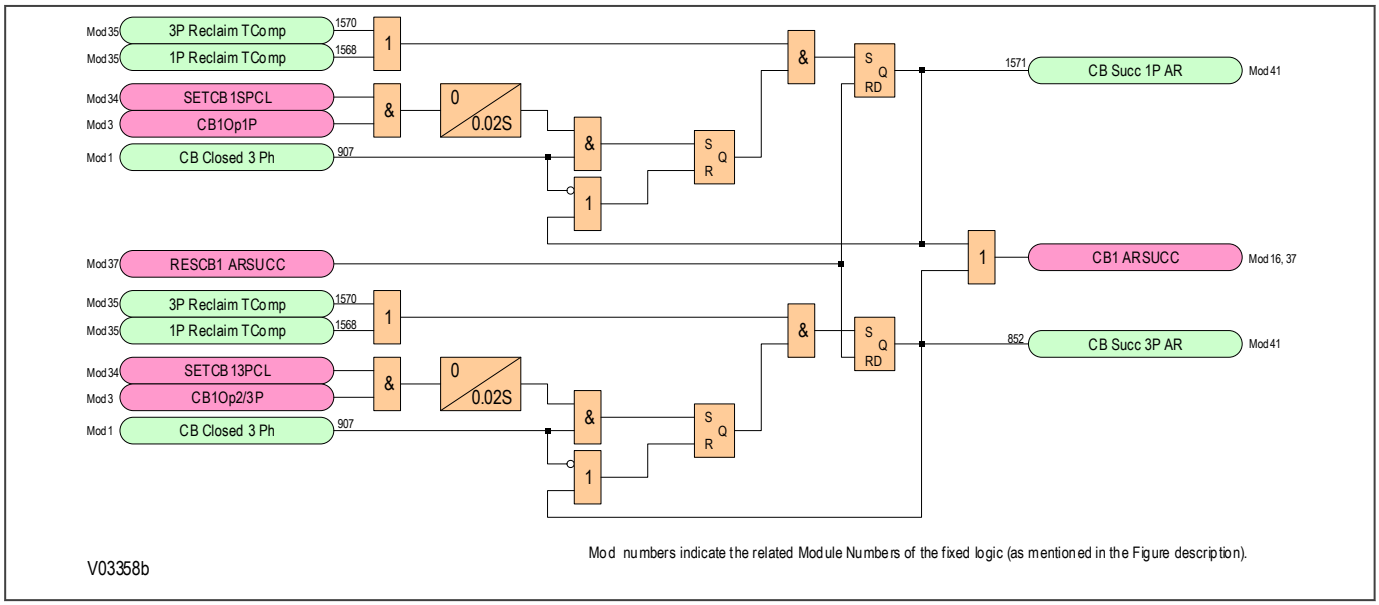


**Figure 176: Successful Autoreclose Signals logic diagram (Module 36)**

### 10.4.13.4 AUTORECLOSE RESET SUCCESSFUL INDICATION LOGIC DIAGRAM

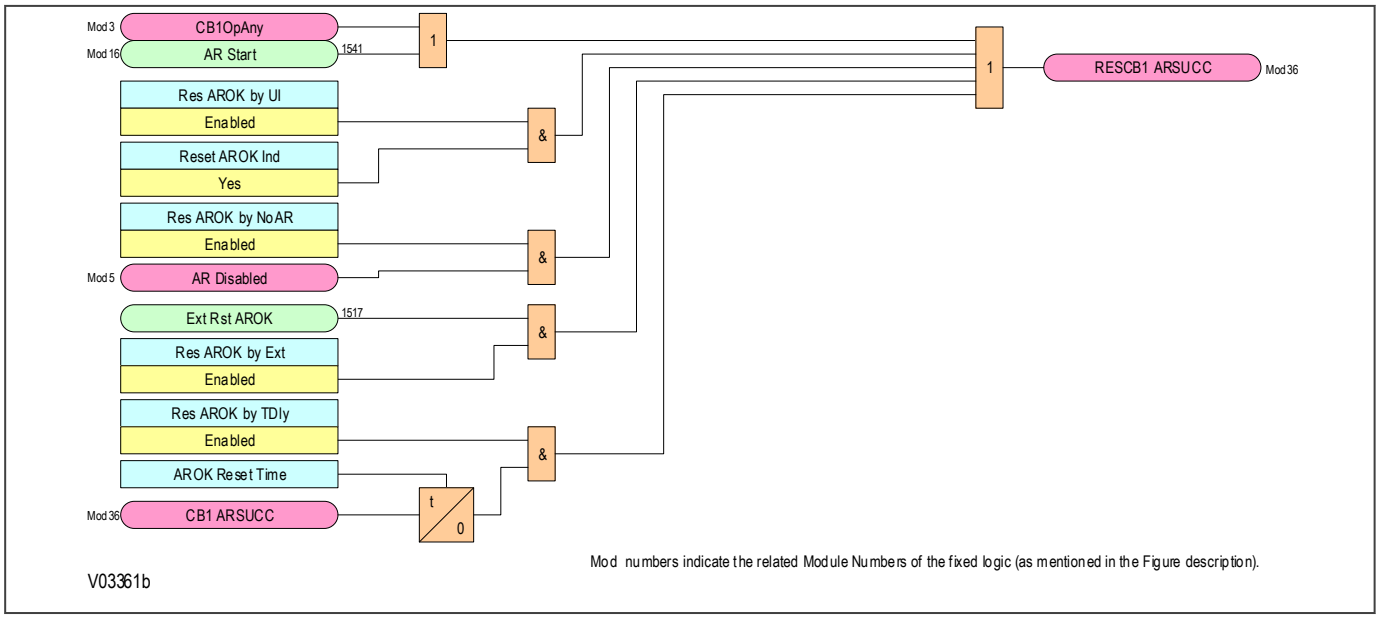


**Figure 177: Autoreclose Reset Successful Indication logic diagram (Module 37)**

## 10.4.14 CB HEALTHY AND SYSTEM CHECK TIMERS

This logic provides signals to cancel Autoreclose if the circuit breaker is not healthy (for example low gas pressure) or system check conditions are not satisfied (for example required line & bus voltage conditions) when the scheme is ready to close the circuit breaker.

At the completion of a dead time, the logic starts an Autoreclose healthy timer. If a circuit breaker healthy signal becomes high before the Autoreclose healthy time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker

healthy signal stays low, then, at the end of the Autoreclose healthy time, a circuit breaker unhealthy alarm is raised. This forces the Autoreclose sequence to be cancelled.

Additionally, at the completion of any three-phase dead time, the logic starts an Autoreclose check synchronism timer. If the circuit breaker synchronism-check OK signal goes high before the time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker synchronism-check OK signal stays low, then when the Autoreclose check synchronism timer expires, an alarm is set to inform that the check synchronism is not satisfied and cancels the Autoreclose cycle.

### 10.4.14.1 CB HEALTHY AND SYSTEM CHECK TIMERS LOGIC DIAGRAM

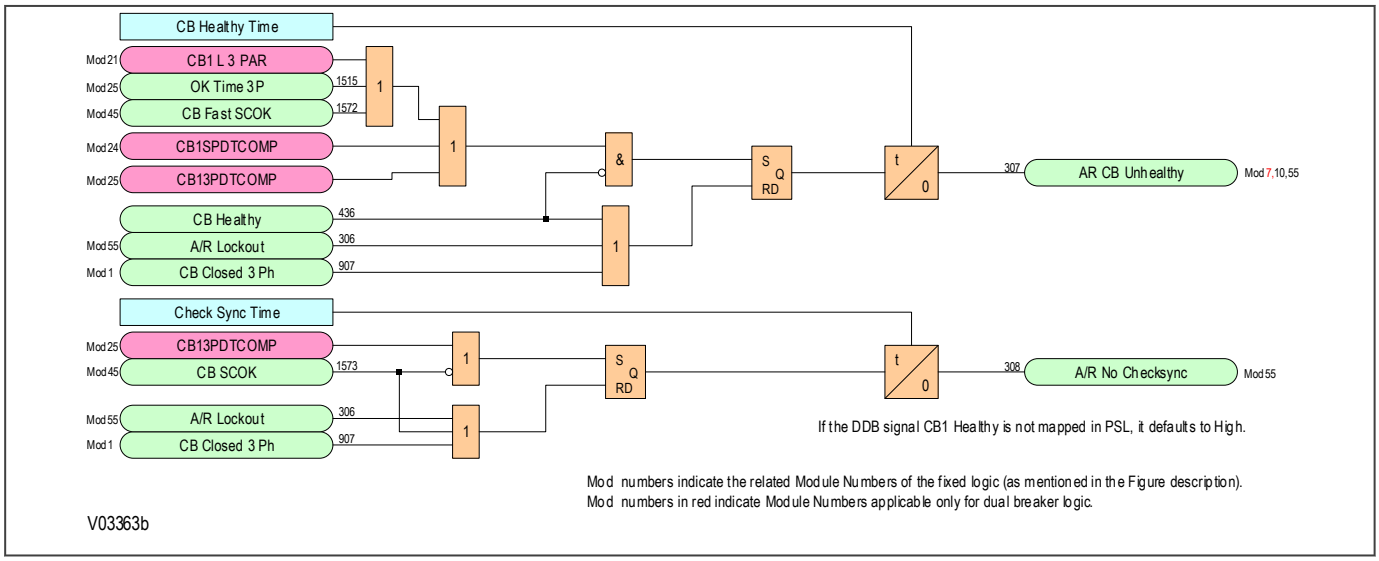


**Figure 178: Circuit Breaker Healthy and System Check Timers Healthy logic diagram (Module 39)**

## 10.4.15 AUTORECLOSE SHOT COUNTERS

A number of counters are provided to enable analysis of circuit breaker Autoreclose history. The counters are stored in non-volatile memory, so that the data is maintained even in the event of a failure of the auxiliary supply. The counter values are accessible through the *CB CONTROL* column. The counters can be reset manually, or by activation of an input appropriately mapped in the PSL.

The logic provides the following summary information for each circuit breaker

- Overall total number of shots (Number of Autoreclose attempts)
- Number of successful 1st shot single-phase Autoreclose sequences
- Number of successful 1st shot three-phase Autoreclose sequences
- Number of successful 2nd shot three-phase Autoreclose sequences
- Number of successful 3rd shot three-phase Autoreclose sequences
- Number of successful 4th shot three-phase Autoreclose sequences
- Number of failed Autoreclose cycles which forced a circuit breaker to lockout

### 10.4.15.1 AUTORECLOSE SHOT COUNTERS LOGIC DIAGRAM

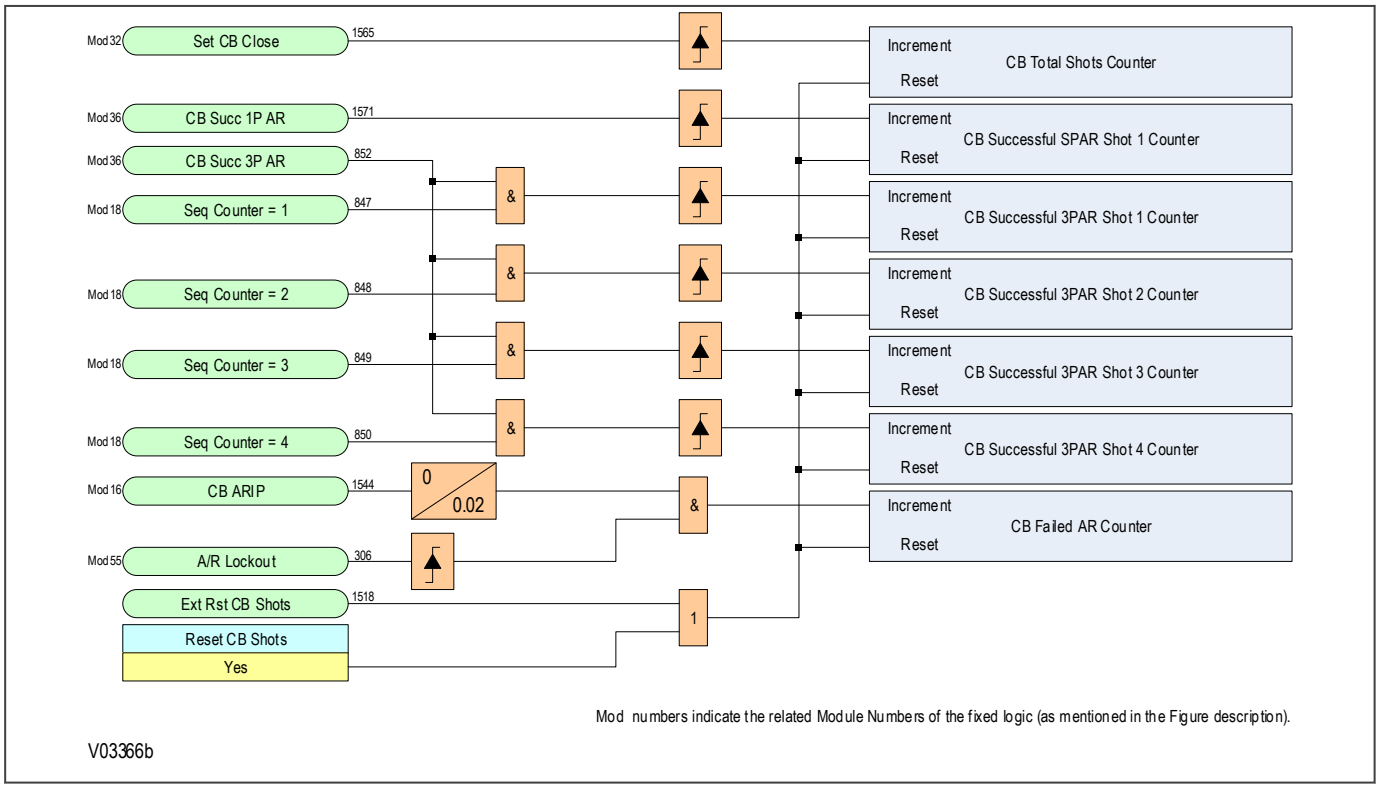


**Figure 179: Autoreclose Shot Counters logic diagram (Module 41)**

## 10.4.16 CIRCUIT BREAKER CONTROL

### 10.4.16.1 CB CONTROL LOGIC DIAGRAM

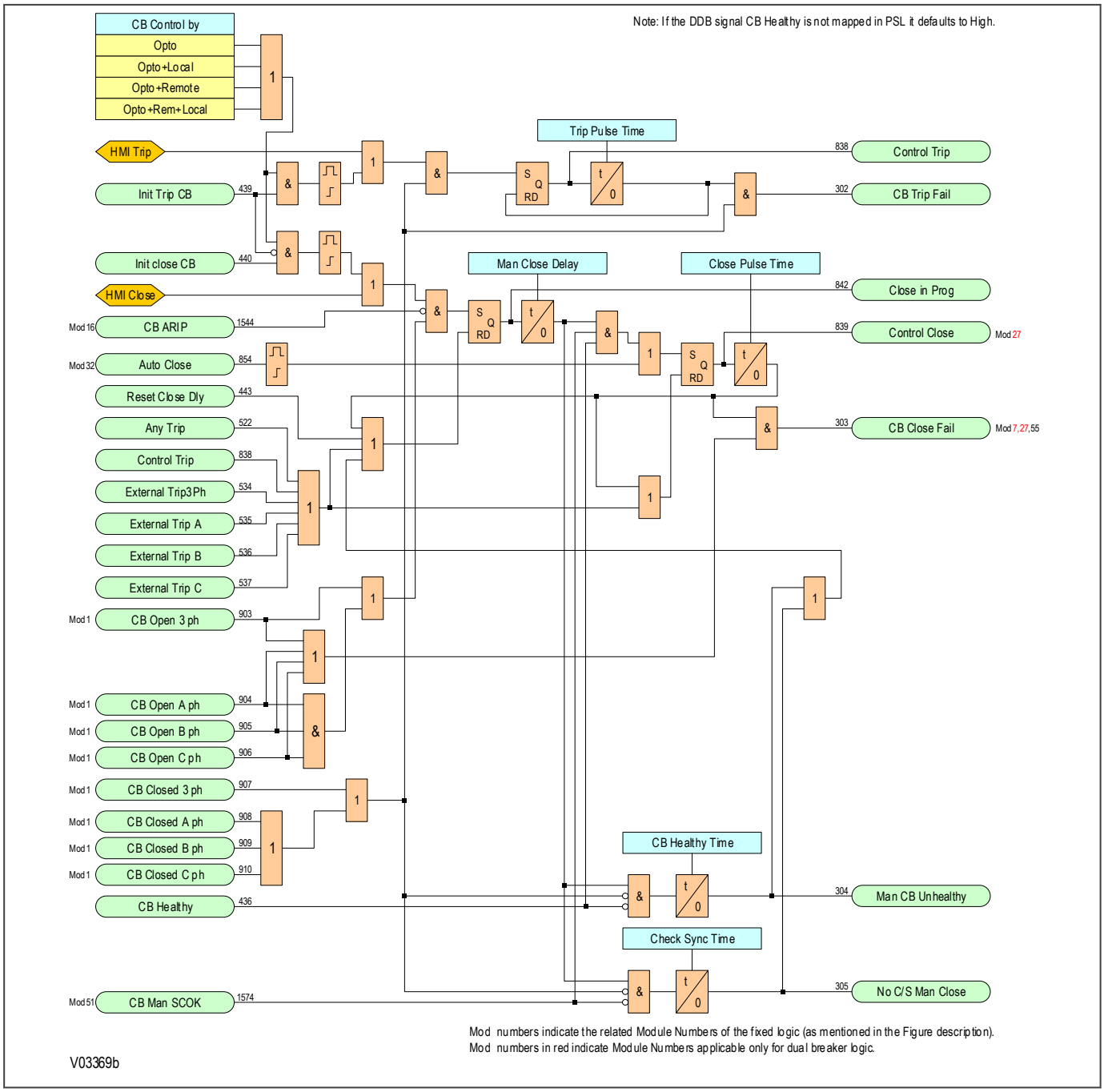


**Figure 180: CB Control logic diagram (Module 43)**

## 10.4.17 CIRCUIT BREAKER TRIP TIME MONITORING

The circuit breaker trip time monitoring logic checks for correct circuit breaker tripping following the issue of a protection trip signal. When the protection trip signal is issued, a timer controlled by the ***Trip Pulse Time*** setting in the *CB CONTROL* column is started.

If the circuit breaker trips correctly the timer resets. If Autoreclose is enabled and the timer resets, the cycle continues. If the circuit breaker fails to trip correctly within the set time, the Autoreclose cycle is forced to lock out and a signal is issued indicating that the circuit breaker failed to trip in response to the protection operation.

### 10.4.17.1 CB TRIP TIME MONITORING LOGIC DIAGRAM

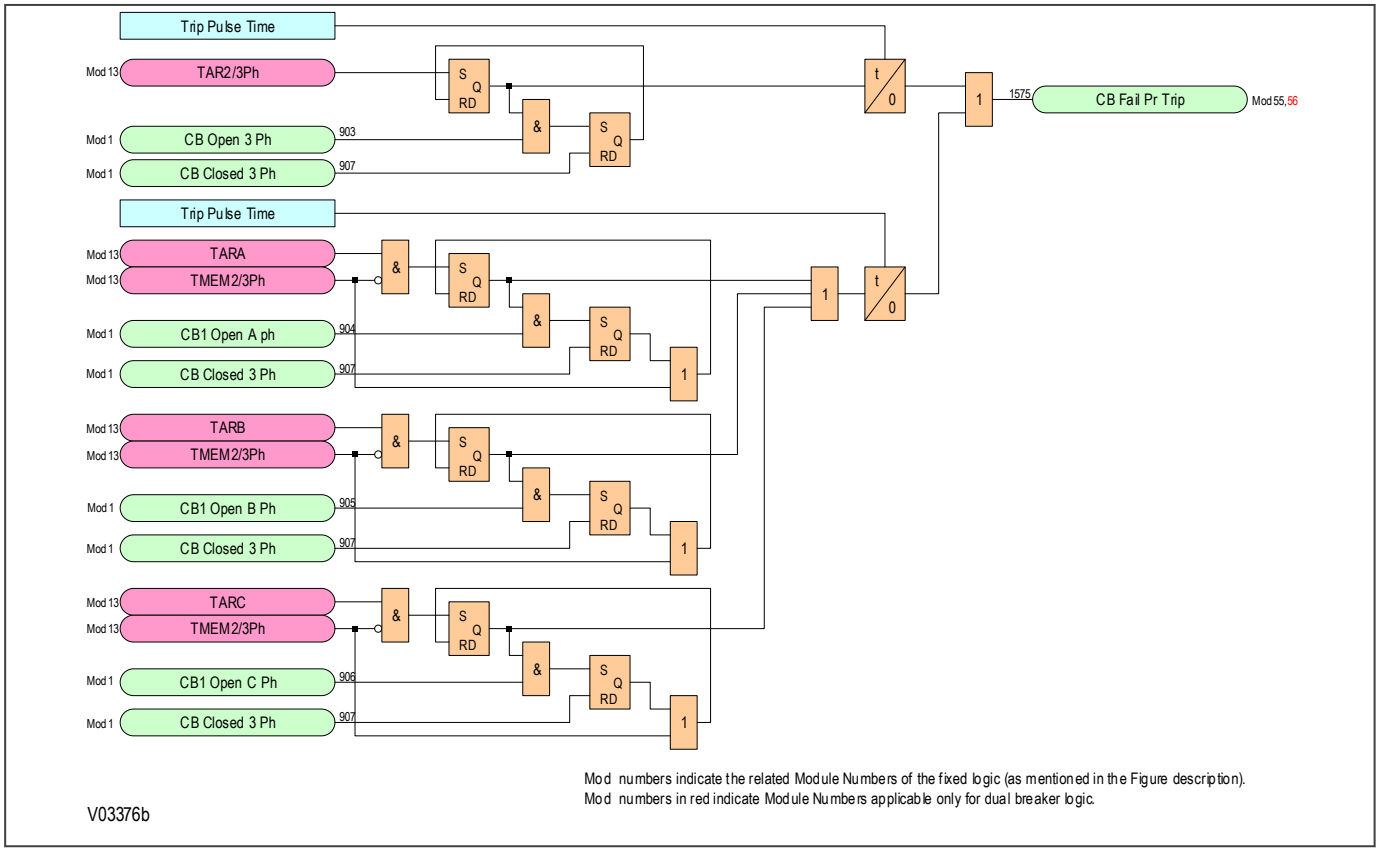


**Figure 181: Circuit Breaker Trip Time Monitoring logic diagram (Module 53)**

## 10.4.18 AUTORECLOSE LOCKOUT

A number of events will cause Autoreclose lockout. If this happens an Autoreclose lockout alarm is raised. In this condition, Autoreclose cannot be initiated until the corresponding lockout has been reset.

The following events force Autoreclose lockout:

- Protection operation during reclaim time. Following the final Autoreclose attempt, if the protection operates during the reclaim time, the AR cycle goes to AR lockout and the Autoreclose function is disabled until the AR lockout condition is reset.
- Persistent fault. A fault is considered persistent if the protection re-operates after the last permitted shot.
- Block Autoreclose. If the block Autoreclose DDB is asserted whilst Autoreclose is in progress, the cycle goes to lockout.
- Protection function selection. Setting ‘Block AR’ against a particular protection function in the AUTORECLOSE column means that operation of the protection will block Autoreclose and force lockout.
- Circuit breaker failure to close. If a circuit breaker fails to close Autoreclose is blocked and forced to lockout.
- Circuit breaker remains open at the end of the reclaim time. An Autoreclose lockout is forced if the circuit breaker is open at the end of the reclaim time.

- Circuit breaker fails to close when the close command is issued.
- Circuit breaker fails to trip correctly.
- Three-phase dead time started by 'line dead' violation. If the line does not go dead within the ***Dead Line Time*** setting, the logic forces the Autoreclose sequence to lockout. Determination of when to start the timer is made in the ***3PDTStart WhenLD*** setting.
- Multi-phase faults. The logic can be set to block Autoreclose either for two-phase or three-phase faults, or to block Autoreclose for three-phase faults only. For this, the setting ***Multi Phase AR*** in the *AUTORECLOSE* column applies.
- Single-phase evolving into multi-phase fault. A discriminating time (***Discrim Time*** in the *AUTORECLOSE* settings) is provided for this feature If, after expiry of the discriminating time, a single-phase fault evolves into a two-phase or three-phase fault, the internal signal 'Evolve Lock' is asserted and the Autoreclose is forced to lockout.

### 10.4.18.1 CB LOCKOUT LOGIC DIAGRAM

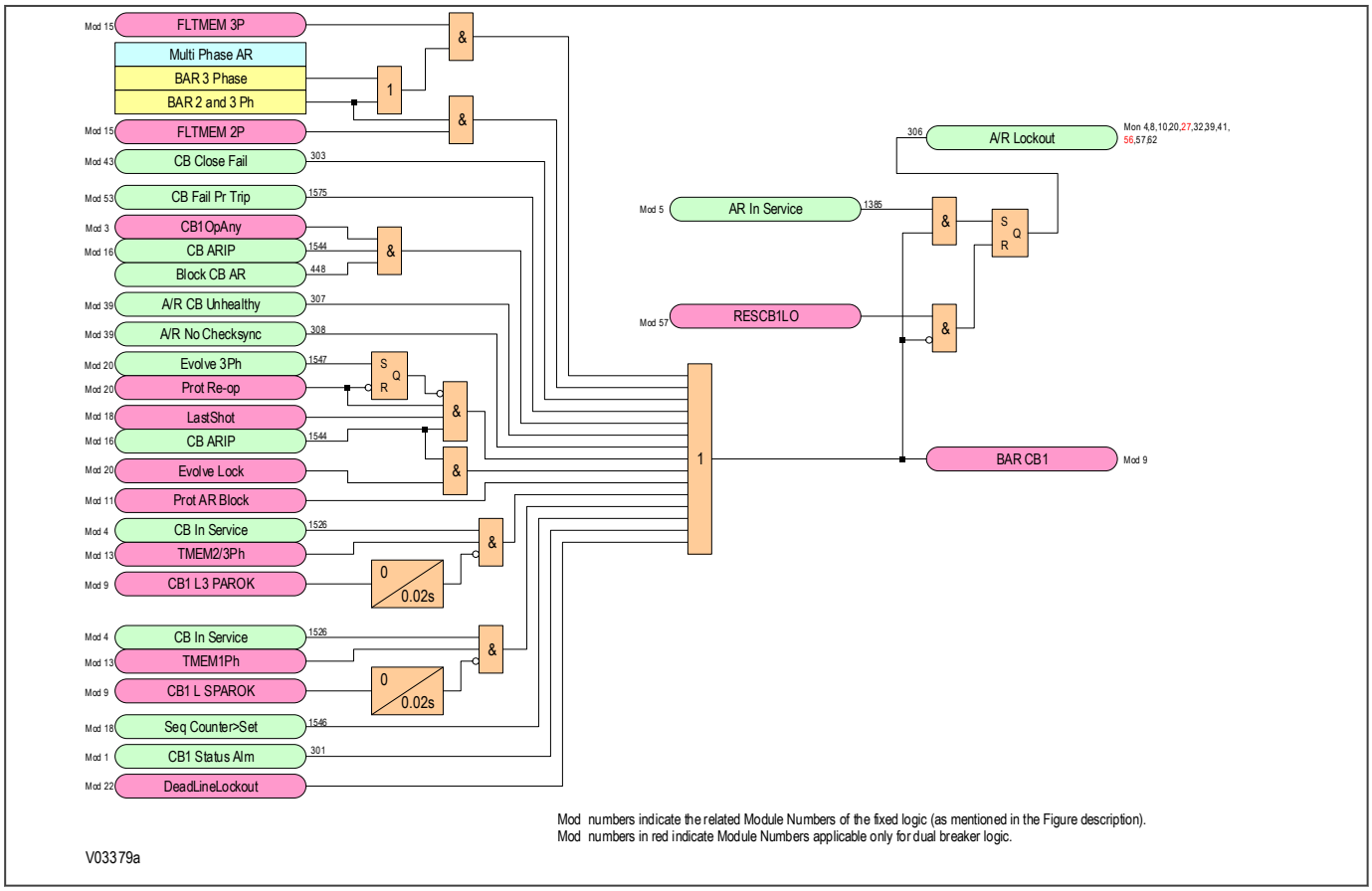


**Figure 182: AR Lockout Logic Diagram (Module 55)**

## 10.4.19 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to `Enabled`, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to `Enabled`, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to `Enabled`, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to `Enabled`, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is `Enabled`, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

### 10.4.19.1 RESET CB LOCKOUT LOGIC DIAGRAM

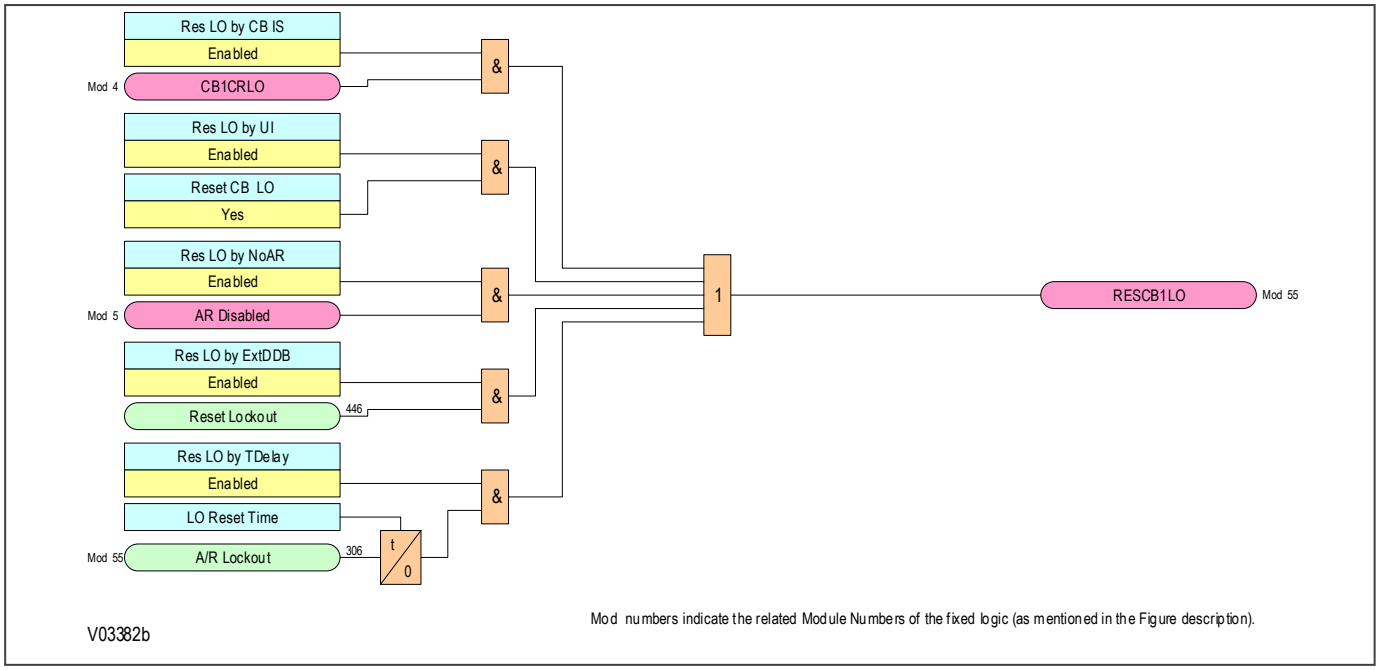


**Figure 183: Reset Circuit Breaker Lockout Logic Diagram (Module 57)**

## 10.4.20 POLE DISCREPANCY

In a three-pole CB, certain combinations of poles open and closed are indicative of a problem. The Pole Discrepancy Logic combines an indication of a Pole Discrepancy condition from the CB Monitoring logic with signals from the internal Autoreclose logic to produce a combined Pole Discrepancy indication for the CB.

### 10.4.20.1 POLE DISCREPANCY LOGIC DIAGRAM

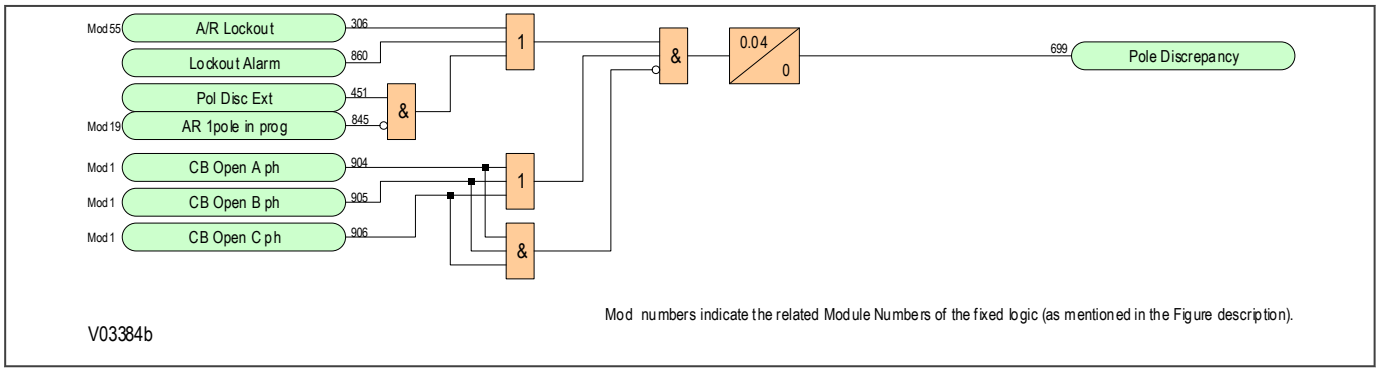


**Figure 184: Pole Discrepancy Logic Diagram (Module 62)**

## 10.4.21 CIRCUIT BREAKER TRIP CONVERSION

Circuit breakers should only trip single-pole or three-pole. The trip conversion logic ensures that the tripping is either single-pole or three-pole. The trip conversion logic ensures that all conditions that should cause three-pole tripping do so. Indication of the number of phases that caused tripping is provided.

### 10.4.21.1 CB TRIP CONVERSION LOGIC DIAGRAM

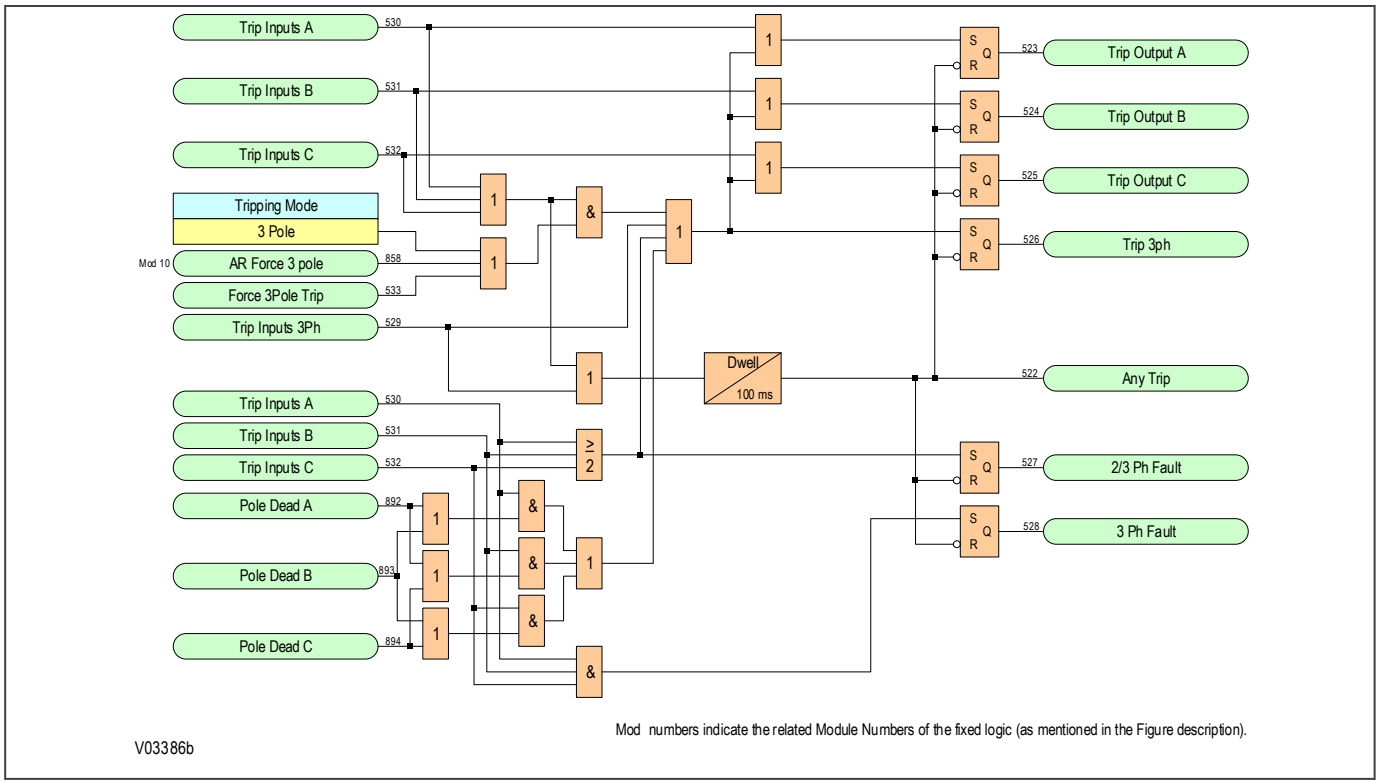


**Figure 185: Circuit Breaker Trip Conversion Logic Diagram (Module 63)**

## 10.4.22 MONITOR CHECKS FOR CB CLOSURE

For single-phase Autoreclose neither voltage nor synchronisation checks are needed as synchronising power should be flowing in the two healthy phases. For three-phase Autorelcose, for the first shot (and only the first shot), you can choose to attempt reclosure without performing a synchronisation check. The setting to permit Autoreclose without checking synchronising conditions is ***CB SC Shot 1***.

Otherwise, synchronising checks on voltages, relative frequencies, and relative phase angles are needed to ensure that sympathetic conditions exist before CB closure is attempted.

The following diagrams detail the Monitor Checks for CB closure.

### 10.4.22.1 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

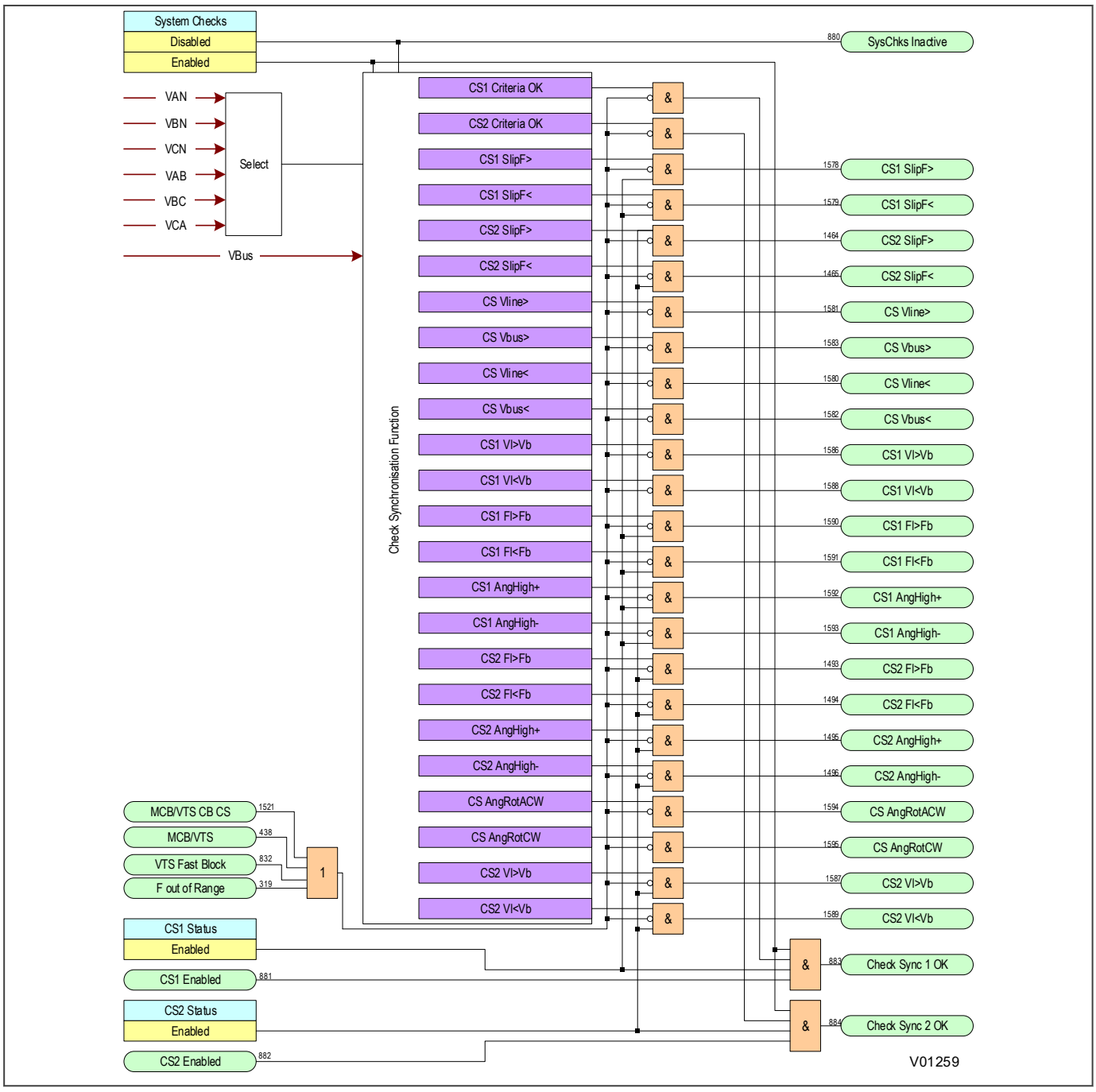


**Figure 186: Check Synchronisation Monitor for CB closure (Module 60)**

### 10.4.22.2 VOLTAGE MONITOR FOR CB CLOSURE

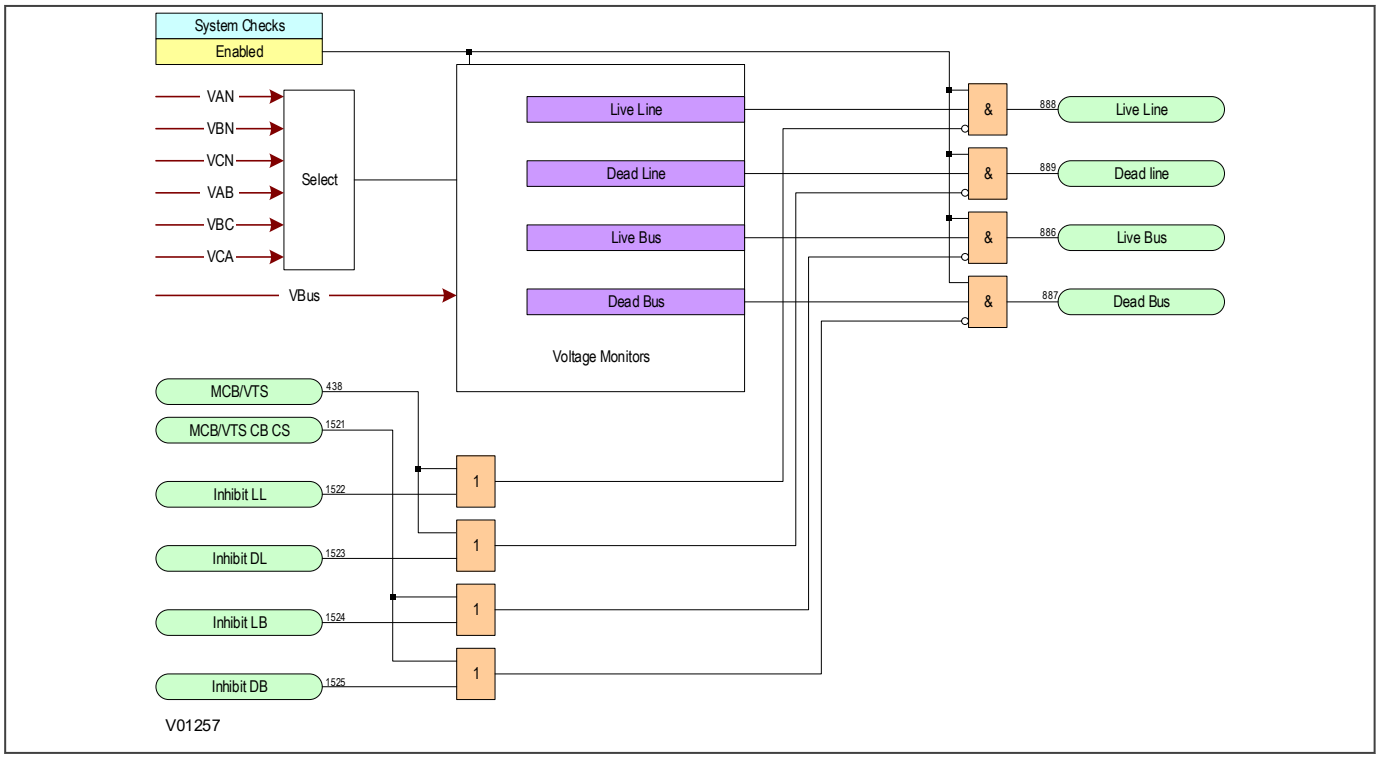


**Figure 187: Voltage Monitor for CB Closure (Module 59)**

## 10.4.23 SYNCHRONISATION CHECKS FOR CB CLOSURE

Logical checking of the outputs from the CB closure monitors is performed to generate signals to indicate that it is OK to close circuit breakers.

Signals are provided to indicate that manual CB closure conditions are OK (***CB Man SCOK***), as are signals to indicate that automatic CB closure conditions are OK (***CB SCOK*** and ***CB Fast SCOK***). The ***CB Fast SCOK*** signal allows CB autoreclosure without waiting for the Dead Time to expire.

For single-phase Autoreclose no voltage or synchronism check is required as synchronising power is flowing in the two healthy phases. Three-phase Autoreclose can be performed without checking that voltages are in synchronism for the first shot (and only the first shot). The settings to permit Autoreclose without checking voltage synchronism on the first shot are:

- ***CB1L SC Shot 1*** for circuit breaker 1 as a leader,
- ***CB1F SC Shot 1*** for circuit breaker 1 as a follower,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a leader,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a follower.

When the circuit breaker has closed, the Autoreclose function asserts a DDB signal ***Set CB1 Close***, which indicates that an attempt has been made to close the circuit breaker. At this point, the Reclaim Time starts. If the circuit breaker remains closed after the reclaim timer expires, the Autoreclose cycle is complete, and signals are generated to indicate that Autoreclose was successful. These are:

- ***CB1 Succ 1P AR*** (Single-phase Autoreclose CB1)
- ***CB2 Succ 1P AR*** (Single-phase Autoreclose CB2)
- ***CB1 Succ 3P AR*** (Three-phase Autoreclose CB1)
- ***CB2 Succ 3P AR*** (Three-phase Autoreclose CB2)

These signals increment the relevant circuit breaker successful Autoreclose shot counters, as well as resetting the Autoreclose in progress signal.

The relevant circuit breaker successful Autoreclose shot counters are:

- ***CB1 SUCC SPAR*** (Single-phase Autoreclose CB1)
- CB1 SUCC 3PAR Shot1 (Three-phase Autoreclose CB1, Shot 1)
- CB1 SUCC 3PAR Shot2 (Three-phase Autoreclose CB1, Shot 2)
- CB1 SUCC 3PAR Shot3 (Three-phase Autoreclose CB1, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB1, Shot 4)
- ***CB2 SUCC SPAR*** (Single-phase Autoreclose CB2)
- CB2 SUCC 3PAR Shot1 (Three-phase Autoreclose CB2, Shot 1)
- CB2 SUCC 3PAR Shot2 (Three-phase Autoreclose CB2, Shot 2)
- CB2 SUCC 3PAR Shot3 (Three-phase Autoreclose CB2, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB2, Shot 4)

### 10.4.23.1 THREE-PHASE AUTORECLOSE SYSTEM CHECK LOGIC DIAGRAM

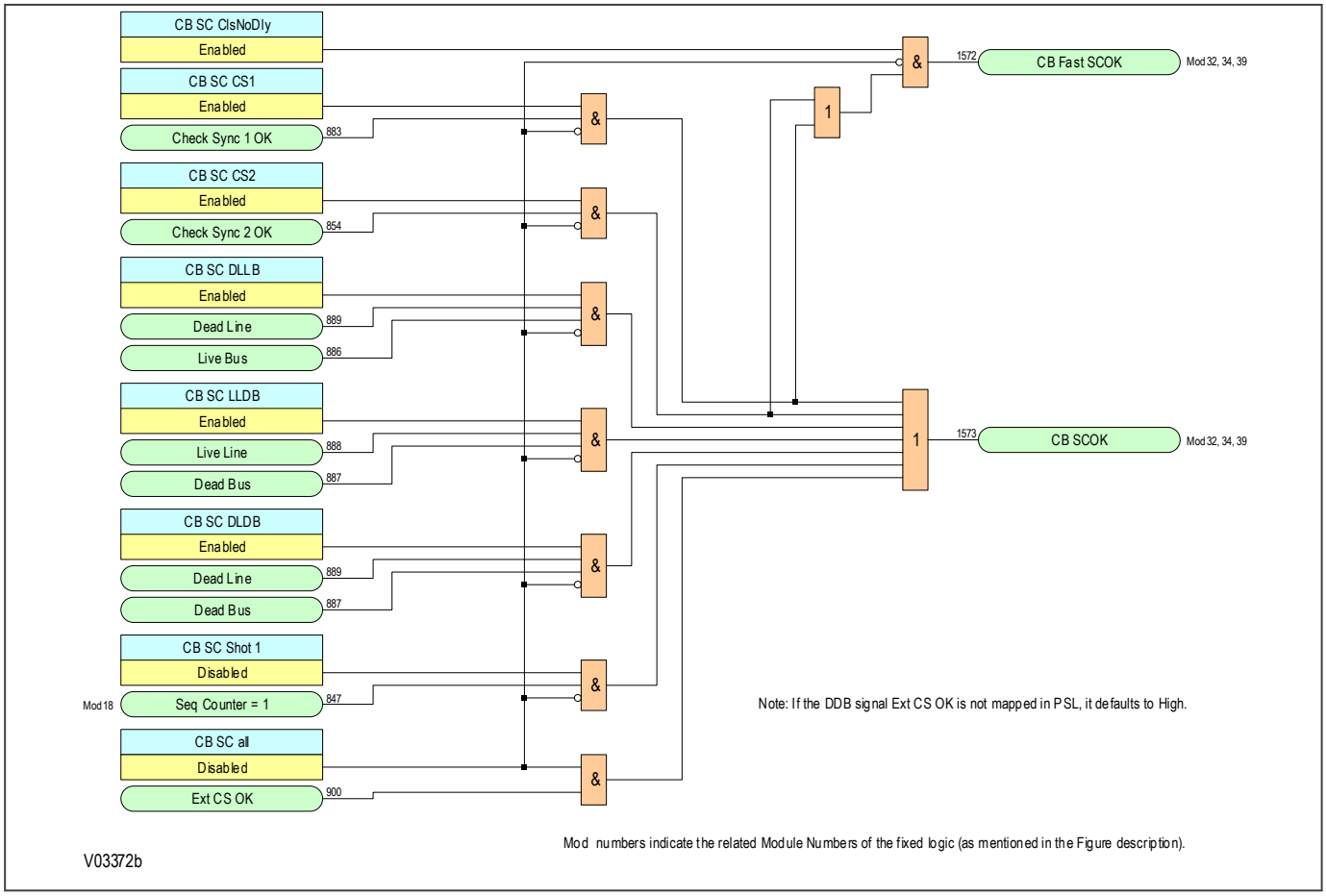


**Figure 188: Three-phase Autoreclose System Check Logic Diagram (Module 45)**

### 10.4.23.2 CB MANUAL CLOSE SYSTEM CHECK LOGIC DIAGRAM

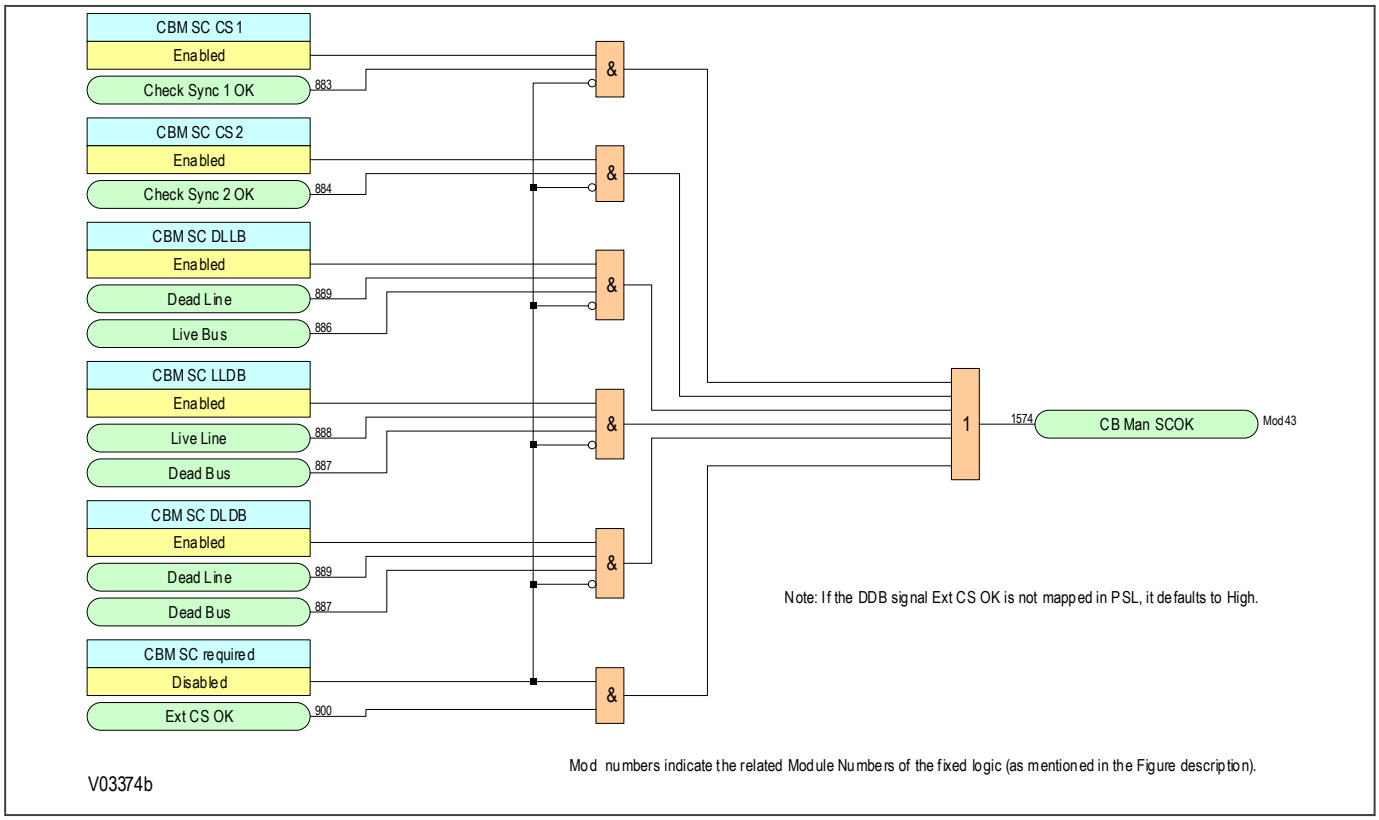


**Figure 189: CB Manual Close System Check Logic Diagram (Module 51)**

# 10.5 SETTING GUIDELINES

## 10.5.1 DE-IONISING TIME GUIDANCE

The de-ionisation time of a fault arc depends on several factors such as circuit voltage, conductor spacing, fault current and duration, atmospheric conditions, wind speed and capacitive coupling from adjacent conductors. For this reason it is difficult to estimate the de-ionisation time. Circuit voltage is, generally the most significant factor and experience tells us that typical minimum de-ionising times for a three-phase fault are as follows:

- 66 kV: 100 ms
- 110 kV: 150 ms
- 132 kV: 170 ms
- 220 kV: 280 ms
- 275 kV: 300 ms
- 400 kV: 500 ms

Where single-pole high speed Autoreclose is used, the capacitive current induced between the healthy phases and the faulty phase tends to maintain the arc. This significantly increases the de-ionisation time and hence required dead time.

Single-pole Autoreclose is generally only used at transmission voltages. A typical de-ionisation time at 220 kV may be as high as 560 ms.

## 10.5.2 DEAD TIMER SETTING GUIDELINES

High speed Autoreclose may need to maintain stability on a network with two or more power sources. For high speed Autoreclose the system disturbance time should be minimised by using fast protection (typically <30 ms) and fast circuit breakers (typically <60 ms). For stability between two sources a system dead time of ≤300 ms may typically be required.

The minimum system dead time (considering just the circuit breaker) is the trip mechanism reset time plus the circuit breaker closing time.

The Autoreclose minimum dead time settings are governed primarily by two factors:

- Time taken for de-ionisation of the fault path
- Circuit breaker characteristics

It is essential that the protection fully resets during the dead time, so that correct time discrimination will be maintained after Autoreclose onto a fault. For high speed Autoreclose instantaneous reset of protection is required.

For highly interconnected systems synchronism is unlikely to be lost by the tripping out of a single line. Here the best policy may be to adopt longer dead times, to allow time for power swings resulting from the fault to settle.

### 10.5.2.1 EXAMPLE DEAD TIME CALCULATION

The following circuit breaker and system characteristics can be used for the minimum dead time calculation:

- a) Circuit breaker Operating time (Trip coil energized to Arc interruption): 50 ms
- b) Circuit breaker Opening + Reset time (Trip coil energized to trip mechanism reset): 200 ms
- c) Protection reset time: < 80 ms
- d) Circuit breaker Closing time (Close command to Contacts make): 85 ms
- e) De-ionisation time (280 ms for 3-phase, or 560 ms for 1-phase)

Three-phase de-ionisation time for 220 kV line is typically 280 ms.

The minimum Autoreclose dead time setting is therefore the greater of:

(a) + (c) = 50 ms + 80 ms = 130 ms, to allow protection reset

(a) + (e) - (d) = 50 ms + 280 ms - 85 ms = 245 ms, to allow de-ionising

In practice a few additional cycles would be added to allow for tolerances, so Dead Time 1 could be set to 300 ms or greater. The overall system dead time is found by adding (d) to the chosen settings then subtracting (a). This gives 335 ms.

A typical de-ionising time value for single-phase trip on a 220 kV line is 560 ms, so the 1 Pole Dead Time could be chosen as 600 ms or greater. The overall system dead time is found by adding (d) to the chosen settings then subtracting (a). This gives 635 ms.

### 10.5.3 RECLAIM TIME SETTING GUIDELINES

Several factors influence the choice of the reclaim timer, such as:

- Fault incidence/Past experience: Small reclaim times may be required where there is a high incidence of recurrent lightning strikes to prevent unnecessary lockout for transient faults.
- Spring charging time: For high speed Autoreclose the reclaim time may be set longer than the spring charging time. A minimum reclaim time of more than 5s may be needed to allow the circuit breaker time to recover after a trip and close before it can perform another trip-close-trip cycle. This time will depend on the duty (rating) of the circuit breaker. For delayed Autoreclose this may not be needed as the dead time can be extended by an extra circuit breaker healthy check / Autoreclose Inhibit Time window time if there is insufficient energy in the circuit breaker.
- Switchgear Maintenance: Excessive operation resulting from short reclaim times can mean shorter maintenance intervals.

When used in conjunction with distance protection, the Reclaim Time setting is generally set greater than the zone 2 delay.

CHAPTER 11

# CURRENT PROTECTION FUNCTIONS

## 11.1 CHAPTER OVERVIEW

The primary purpose of this product is not overcurrent protection. It does however provide a range of current protection functions to be used as backup protection. This chapter assumes you are familiar with overcurrent protection principles and does not provide detailed information here. If you require further information about general overcurrent protection principles, please refer either to GE Vernova's publication, Protection and Automation Application Guide, earlier incarnations of this technical manual, or one of our technical manuals from our P40 Agile Modular distribution range of products such as the P14.

This chapter contains the following sections:

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Phase Fault Overcurrent Protection 290
Negative Sequence Overcurrent Protection 293
Earth Fault Protection 296
Sensitive Earth Fault Protection 301
High Impedance REF 306
Thermal Overload Protection 308
Broken Conductor Protection 312
Transient Earth Fault Detection 314

## 11.2 PHASE FAULT OVERCURRENT PROTECTION

Phase fault overcurrent protection is provided as a form of back-up protection that could be:

- Permanently disabled
- Permanently enabled
- Enabled only in case of VT fuse/MCB failure
- Enabled only in case of protection communication channel failure
- Enabled if VT fuse/MCB or protection communication channel fail
- Enabled if VT fuse/MCB and protection communication channel fail

In addition, each stage may be inhibited/blocked by a DDB signal.

It should be noted that phase overcurrent protection is phase segregated, but the operation of any phase is mapped to 3 phase tripping in the default PSL.

The VTS element of the IED can be selected to either block the directional element or simply remove the directional control.

### 11.2.1 POC IMPLEMENTATION

Phase Overcurrent Protection is configured in the OVERCURRENT column of the relevant settings group.

The product provides four stages of three-phase overcurrent protection, each with independent time delay characteristics. The settings are independent for each stage, but for each stage, the settings apply to all phases.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves based on IEC and IEEE standards
- A range of programmable user-defined curves
- DT (Definite Time) characteristic

This is achieved using the cells:

- ***I>(n) Function*** for the overcurrent operate characteristic
- ***I>(n) Reset Char*** for the overcurrent reset characteristic
- ***I>(n) Usr Rst Char*** for the reset characteristic for user-defined curves

where (n) is the number of the stage.

The IDMT-equipped stages, (1 and 2) also provide a Timer Hold facility. This is configured using the cells ***I>(n) tReset***, where (n) is the number of the stage. This does not apply to IEEE curves.

Stages 3 and 4 have definite time characteristics only.

### 11.2.2 DIRECTIONAL ELEMENT

If fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Once the direction has been determined the device can decide whether to allow tripping or to block tripping. To determine the direction of a phase overcurrent fault, the device must compare the phase angle of the fault current with that of a known reference quantity. The phase angle of this known reference quantity must be independent of the faulted phase. Typically this will be the line voltage between the other two phases.

The phase fault elements of the IEDs are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

| Phase of Protection | Operate Current | Polarising Voltage |
|---|---|---|
| A Phase | IA | VBC |
| B Phase | IB | VCA |
| C Phase | IC | VAB |

Under system fault conditions, the fault current vector lags its nominal phase voltage by an angle depending on the system X/R ratio. The IED must therefore operate with maximum sensitivity for currents lying in this region. This is achieved by using the IED characteristic angle (RCA). This is the is the angle by which the current applied to the IED must be displaced from the voltage applied to the IED to obtain maximum sensitivity.

The device provides a setting ***I> Char Angle***, which is set globally for all overcurrent stages. It is possible to set characteristic angles anywhere in the range –95° to +95°.

A directional check is performed based on the following criteria:

### Directional forward

$$-90° < (\text{angle}(I) - \text{angle}(V) - RCA) < 90°$$

### Directional reverse

$$-90° > (\text{angle}(I) - \text{angle}(V) - RCA) > 90°$$

For close up three-phase faults, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the device includes a synchronous polarisation feature that stores the pre-fault voltage information and continues to apply this to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

## 11.2.3 POC LOGIC

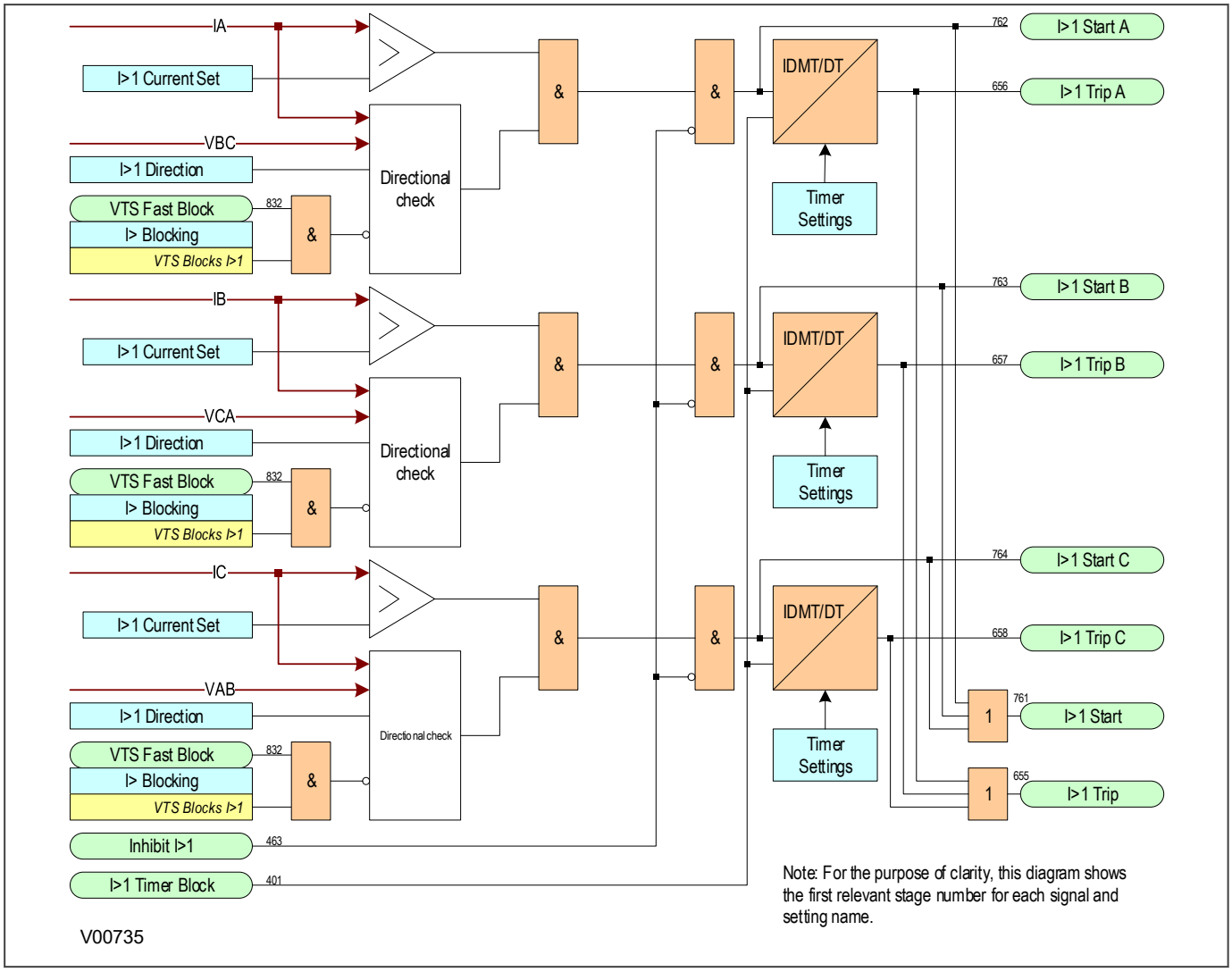



**Figure 190: Phase Overcurrent Protection logic diagram**

# 11.3 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

When applying standard phase overcurrent protection, the overcurrent elements must be set significantly higher than the maximum load current. This limits the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes. Negative Phase Sequence Overcurrent elements can help in such cases.

Any unbalanced fault condition will produce a negative sequence current component. Therefore, a negative phase sequence overcurrent element can be used for both phase-to-phase and phase-to-earth faults. Negative Phase Sequence Overcurrent protection offers the following advantages:

- Negative phase sequence overcurrent elements are more sensitive to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault element due to the system configuration. For example, an earth fault element applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element may be used to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

## 11.3.1 NEGATIVE SEQUENCE OVERCURRENT PROTECTION IMPLEMENTATION

Negative Sequence Overcurrent Protection is implemented in the *NEG SEQ O/C* column of the relevant settings group.

The product provides four stages of negative sequence overcurrent protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***I2>(n) Function*** for the overcurrent operate characteristic
- ***I2>(n) Reset Char*** for the overcurrent reset characteristic

where (n) is the number of the stage.

The IDMT-capable stages, (1 and 2) also provide a Timer Hold. This is configured using the cells ***I2>(n) tReset***, where (n) is the number of the stage. This is not applicable for curves based on the IEEE standard.

Stages 3 and 4 have definite time characteristics only.

## 11.3.2 DIRECTIONAL ELEMENT

Where negative phase sequence current may flow in either direction, directional control should be used.

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. A directional element is available for all of the negative sequence overcurrent stages. This is found in the ***I2> Direction*** cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

A suitable characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (**–V2**), in order to be at the centre of the directional characteristic.

## 11.3.3 NPSOC LOGIC

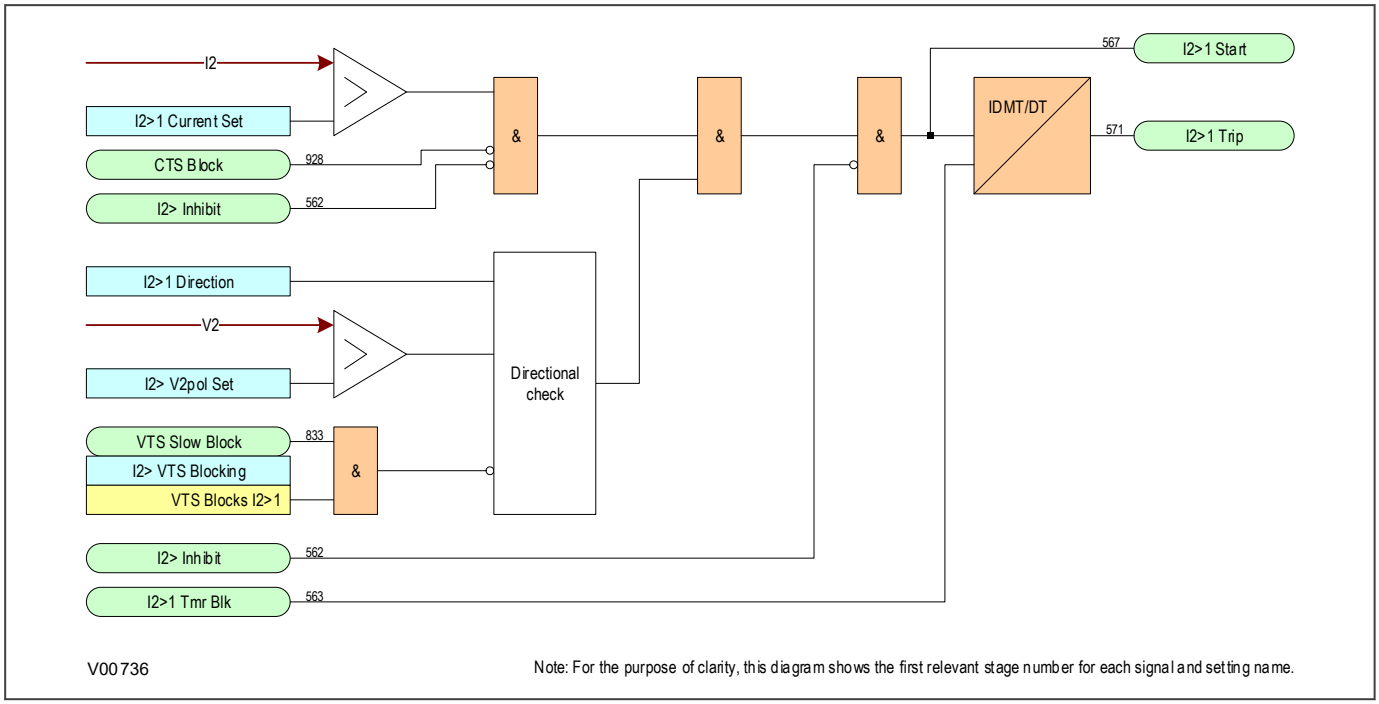



**Figure 191: Negative Phase Sequence Overcurrent Protection logic diagram**

## 11.3.4 APPLICATION NOTES

### 11.3.4.1 SETTING GUIDELINES (CURRENT THRESHOLD)

A negative phase sequence element can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-earth or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and earth elements for phase-to-earth and phase-to-phase faults.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load imbalance. This can be set practically at the commissioning stage, making use of the measurement function to display the standing negative phase sequence current. The setting should be at least 20% above this figure.

Where the negative phase sequence element needs to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

### 11.3.4.2 SETTING GUIDELINES (TIME DELAY)

Correct setting of the time delay for this function is vital. You should also be very aware that this element is applied primarily to provide back-up protection to other protection devices or to provide an alarm. It would therefore normally have a long time delay.

The time delay set must be greater than the operating time of any other protection device (at minimum fault level) that may respond to unbalanced faults such as phase overcurrent elements and earth fault elements.

#### 11.3.4.3 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control of the element should be employed (VT models only).

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the relay characteristic angle (RCA) should be set equal to –60°
- For a distribution system the relay characteristic angle (RCA) should be set equal to –45°

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2> V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

# 11.4 EARTH FAULT PROTECTION

Earth faults are overcurrent faults where the fault current flows to earth. Earth faults are the most common type of fault.

Earth faults can be measured directly from the system by means of:

- A separate current Transformer (CT) located in a power system earth connection
- A separate Core Balance Current Transformer (CBCT), usually connected to the SEF transformer input
- A residual connection of the three line CTs, where the Earth faults can be derived mathematically by summing the three measured phase currents

Depending on the device model, it will provide one or more of the above means for Earth fault protection.

## 11.4.1 EARTH FAULT PROTECTION IMPLEMENTATION

Earth fault protection is implemented in the *EARTH FAULT* column of the relevant settings group. The element uses quantities derived internally from summing the three-phase currents.

The product provides four stages of Earth Fault protection with independent time delay characteristics, for each *EARTH FAULT* column.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells:

- ***IN>(n) Function*** for the overcurrent operate characteristics
- ***IN>(n) Reset Char*** for the overcurrent reset characteristic

where (n) is the number of the stage.

Stages 1 and 2 provide a Timer Hold facility. This is configured using the cells ***IN>(n) tReset***

Stages 3 and 4 can have definite time characteristics only.

Earth fault Overcurrent IN> can be set to:

- Permanently disabled
- Permanently enabled
- Enabled only if VT fuse/MCB fails
- Enabled only if protection communication channel fails
- Enabled if VT fuse/MCB or protection communication channel fail
- Enabled if VT fuse/MCB and protection communication channel fail

Each stage can be individually inhibited with a DDB signal ***Inhibit IN>(n)***, where n is the stage number.

## 11.4.2 IDG CURVE

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

$$t_{op} = 5.8 - 1.35 log_e \left( \frac{I}{IN > Setting} \right)$$

where:

$t_{op}$ is the operating time

I is the measured current

IN> Setting is an adjustable setting, which defines the start point of the characteristic

*Note:*
*Although the start point of the characteristic is defined by the "IN>" setting, the actual current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".*

*Note:*
*When using an IDG Operate characteristic, DT is always used with a value of zero for the Rest characteristic.*

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

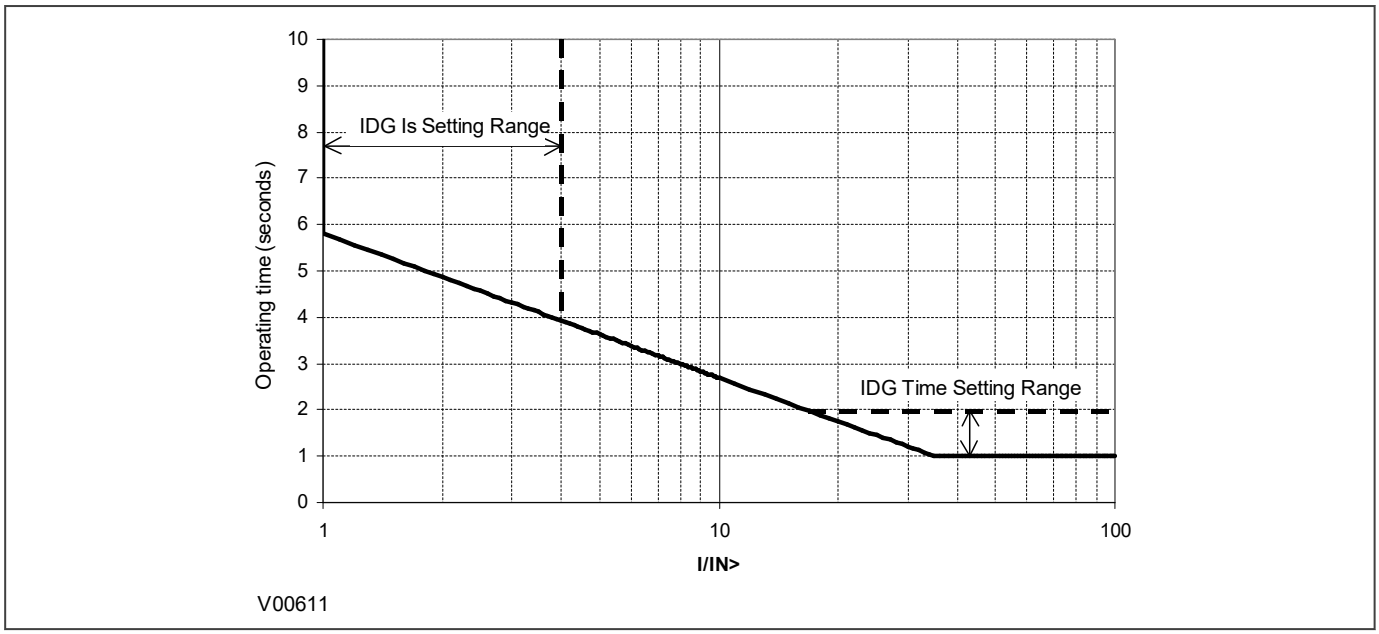



**Figure 192: IDG Characteristic**

## 11.4.3 DIRECTIONAL ELEMENT

If Earth fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Typical systems that require such protection are parallel feeders and ring main systems.

A directional element is available for all of the Earth Fault stages. These are found in the direction setting cells for the relevant stage. They can be set to non-directional, directional forward, or directional reverse.

Directional control can be blocked by the VTS element if required.

For standard earth fault protection, two options are available for polarisation; Residual Voltage (zero sequence) or Negative Sequence.

### 11.4.3.1 RESIDUAL VOLTAGE POLARISATION

With earth fault protection, the polarising signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise directional earth fault

elements. This is known as Zero Sequence Voltage polarisation, Residual Voltage polarisation or Neutral Displacement Voltage (NVD) polarisation.

Small levels of residual voltage could be present under normal system conditions due to system imbalances, VT inaccuracies, device tolerances etc. For this reason, the device includes a user settable threshold (***IN> VNPol set***), which must be exceeded in order for the DEF function to become operational. The residual voltage measurement provided in the *MEASUREMENTS 1* column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

*Note:*
*Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the "-Vres" quantity. This 180° phase shift is automatically introduced within the device.*

The directional criteria with residual voltage polarisation is given below:

- Directional forward: -90° < (angle(IN) - angle(VN + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(IN) - angle(VN + 180°) - RCA) > 90°

#### 11.4.3.2 NEGATIVE SEQUENCE POLARISATION

In some applications, the use of residual voltage polarisation may not be possible to achieve or it can be problematic. For example, a suitable type of VT may be unavailable, or an HV/EHV parallel line application may present problems with zero sequence mutual coupling.

In such situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarisation. This method determines the fault direction by comparing the NPS voltage with the NPS current. The operating quantity, however, is still residual current.

This can be used for both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells ***IN> V2pol set*** and ***IN> I2pol set*** respectively.

Negative phase sequence polarising is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance to negligible levels. If this voltage is less than 0.5 volts the device will stop providing directionalisation.

The directional criteria with negative sequence polarisation is given below:

- Directional forward: -90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

## 11.4.4 EARTH FAULT PROTECTION LOGIC

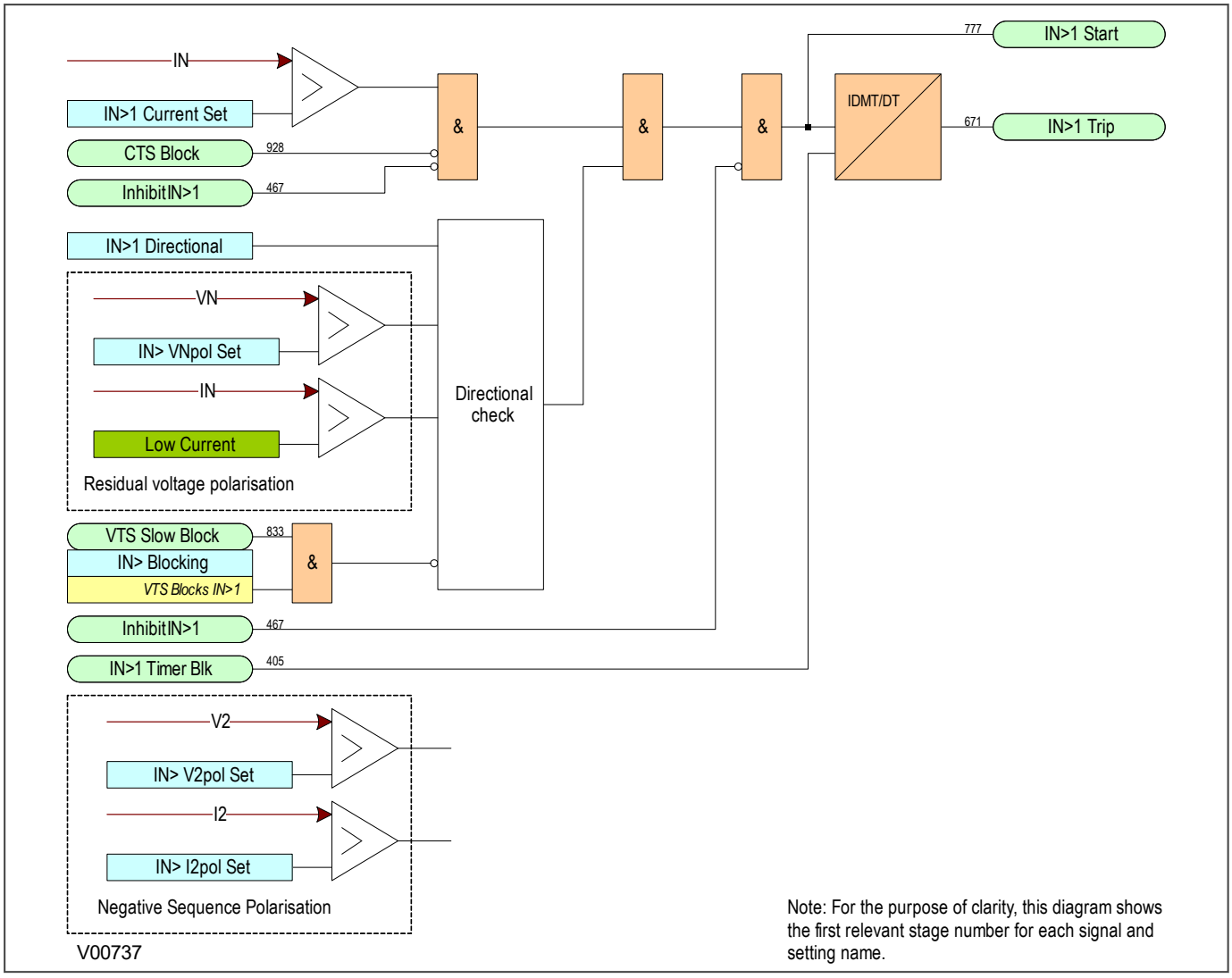



**Figure 193: Earth Fault Protection logic diagram**

## 11.4.5 APPLICATION NOTES

### 11.4.5.1 RESIDUAL VOLTAGE POLARISATION SETTING GUIDELINES

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies, IED tolerances etc. Hence, the IED includes a user settable threshold (***IN> VNPol Set***) which must be exceeded in order for the DEF function to be operational. In practice, the typical zero sequence voltage on a healthy system can be as high as 1% (i.e. 3% residual), and the VT error could be 1% per phase. A setting between 1% and 4% is therefore typical. The residual voltage measurement may assist in determining the required threshold setting during commissioning, as this will indicate the level of standing residual voltage present.

### 11.4.5.2 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

With directional earth faults, the residual current under fault conditions lies at an angle lagging the polarising voltage. Hence, negative RCA settings are required for DEF applications. This is set in the cell ***I> Char Angle*** in the relevant earth fault menu.

We recommend the following RCA settings:

- Resistance earthed systems: 0°
- Distribution systems (solidly earthed): -45°
- Transmission systems (solidly earthed): -60°

# 11.5 SENSITIVE EARTH FAULT PROTECTION

With some earth faults, the fault current flowing to earth is limited by either intentional resistance (as is the case with some HV systems) or unintentional resistance (e.g. in very dry conditions and where the substrate is high resistance, such as sand or rock).

To provide protection in such cases, it is necessary to provide an earth fault protection system with a setting that is considerably lower than for normal line protection. Such sensitivity cannot be provided with conventional CTs, therefore the SEF input would normally be fed from a core balance current transformer (CBCT) mounted around the three phases of the feeder cable. The SEF transformer should be a special measurement class transformer.

## 11.5.1 SEF PROTECTION IMPLEMENTATION

The product provides four stages of SEF protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***ISEF>(n) Function*** for the overcurrent operate characteristic
- ***ISEF>(n) Reset Chr*** for the overcurrent reset characteristic

where (n) is the number of the stage.

Stages 1 and 2 also provide a Timer Hold facility. This is configured using the cells ***ISEF>(n) tReset***.

Stages 3 and 4 have definite time characteristics only.

Each stage can be individually inhibited with a DDB signal Inhibit ISEF>(n), where n is the stage number.

## 11.5.2 EPATR B CURVE

The EPATR B curve is commonly used for time-delayed Sensitive Earth Fault protection in certain markets. This curve is only available in the Sensitive Earth Fault protection stages 1 and 2. It is based on primary current settings, employing a SEF CT ratio of 100:1 A.

The EPATR_B curve has 3 separate segments defined in terms of the primary current. It is defined as follows:

| Segment | Primary Current Range Based on 100A:1A CT Ratio | Current/Time Characteristic |
|---|---|---|
| 1 | ISEF = 0.5A to 6.0A | t = 432 x TMS/ISEF 0.655 secs |
| 2 | ISEF = 6.0A to 200A | t = 800 x TMS/ISEF secs |
| 3 | ISEF above 200A | t = 4 x TMS secs |

where TMS (time multiplier setting) is 0.025 - 1.2 in steps of 0.025.

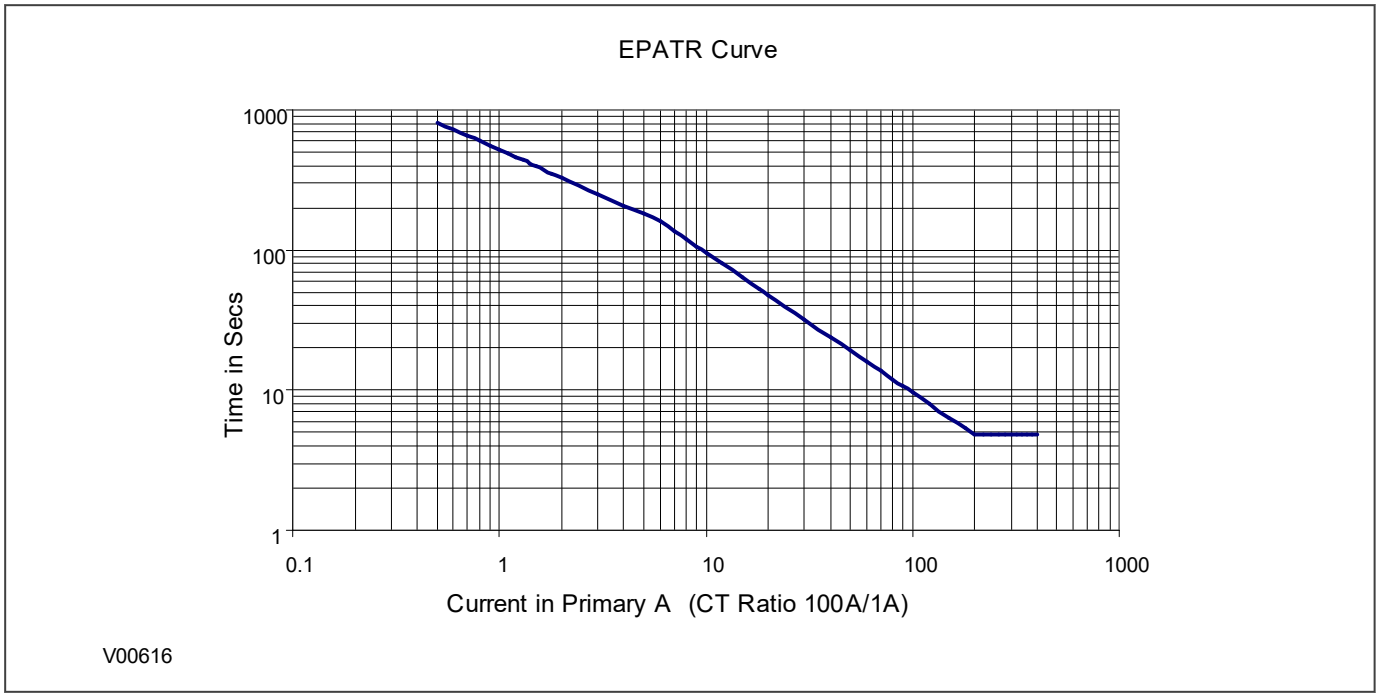



**Figure 194: EPATR B characteristic shown for TMS = 1.0**

## 11.5.3 SENSITIVE EARTH FAULT PROTECTION LOGIC

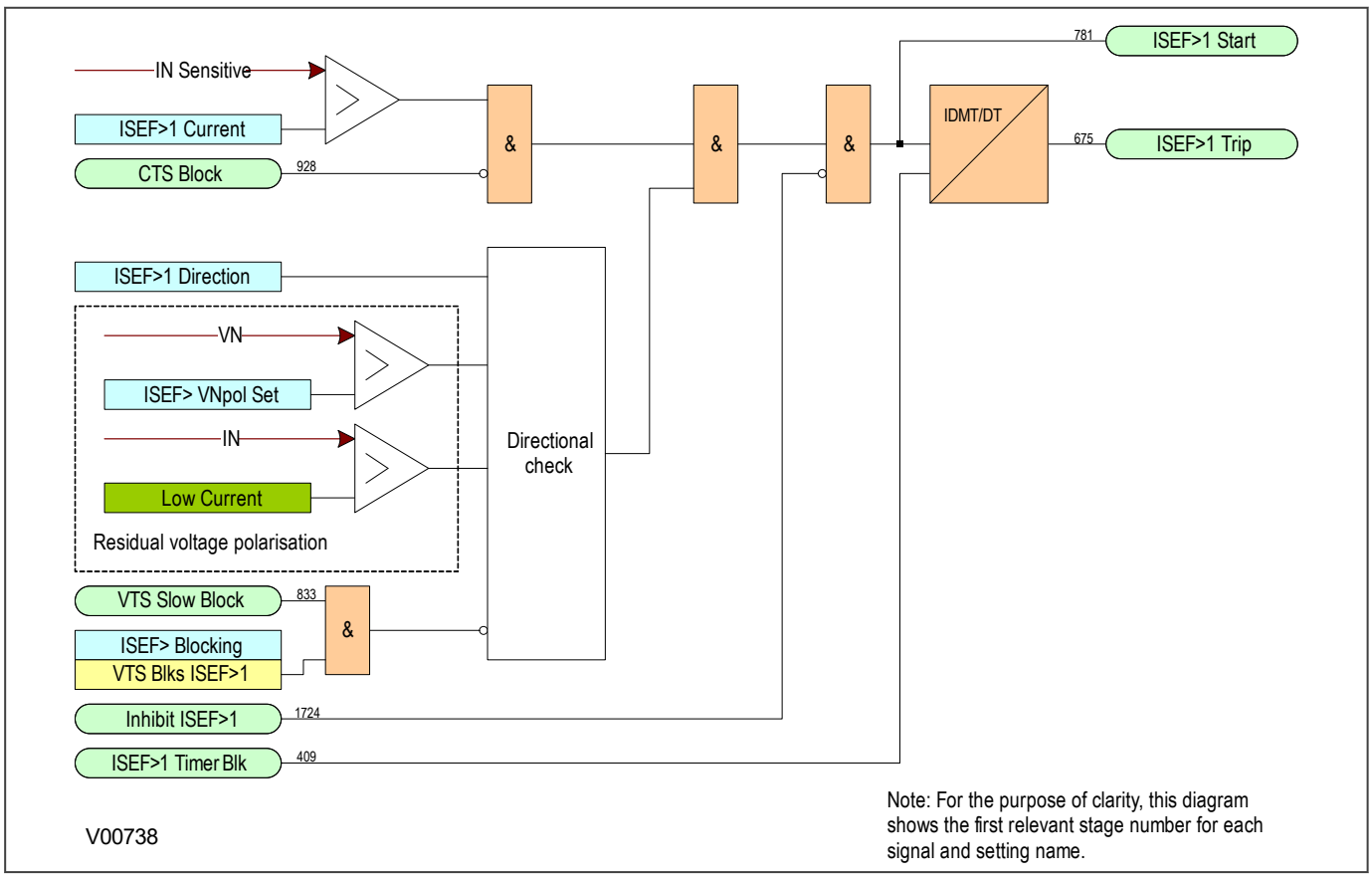



**Figure 195: Sensitive Earth Fault Protection logic diagram**

## 11.5.4 APPLICATION NOTES

### 11.5.4.1 INSULATED SYSTEMS

When insulated systems are used, it is not possible to detect faults using standard earth fault protection. It is possible to use a residual overvoltage device to achieve this, but even with this method full discrimination is not possible. Fully discriminative earth fault protection on this type of system can only be achieved by using a SEF (Sensitive Earth Fault) element. This type of protection detects the resultant imbalance in the system charging currents that occurs under earth fault conditions. A core balanced CT must be used for this application. This eliminates the possibility of spill current that may arise from slight mismatches between residually connected line CTs. It also enables a much lower CT ratio to be applied, thereby allowing the required protection sensitivity to be more easily achieved.

The following diagram shows an insulated system with a C-phase fault.

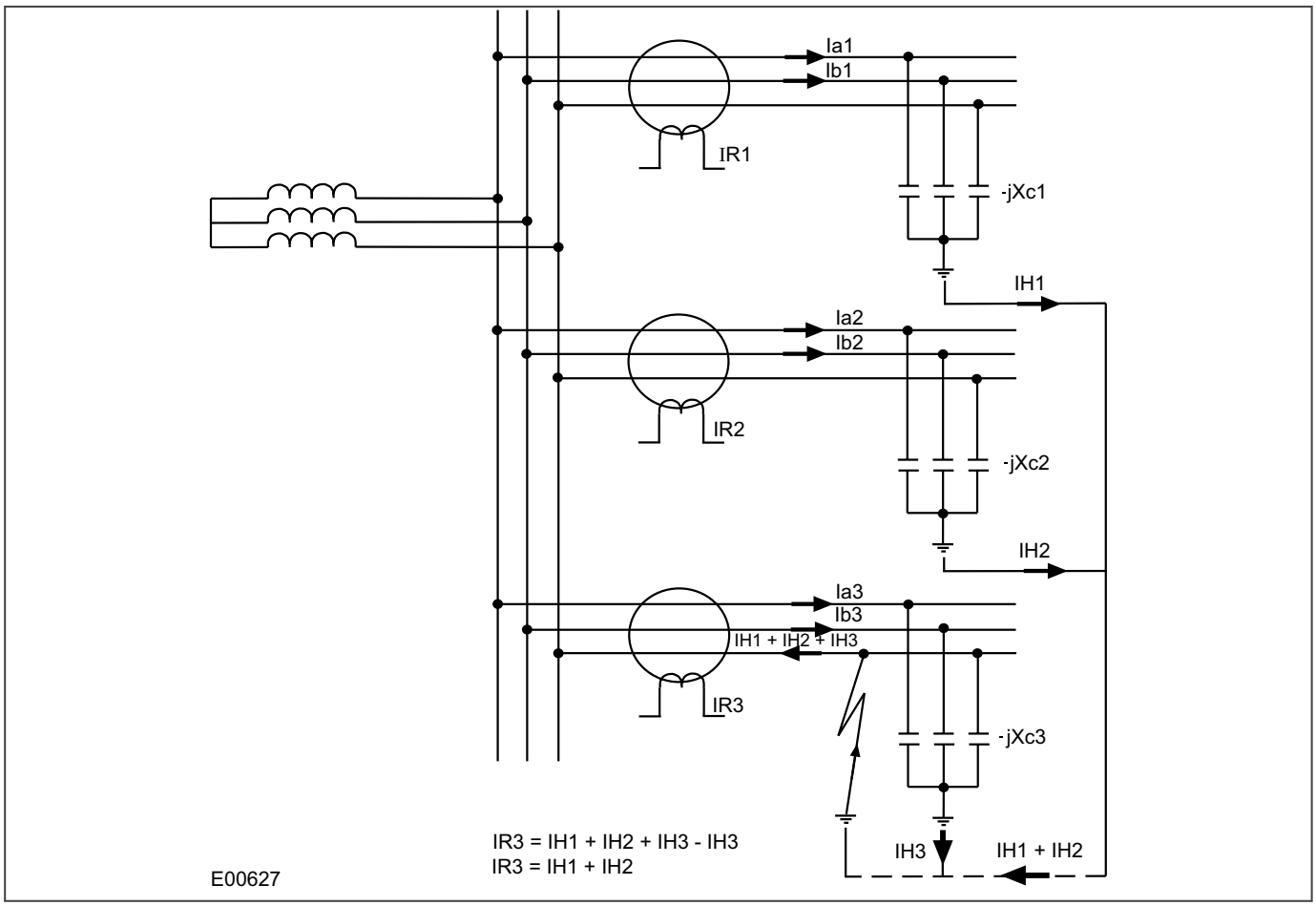



**Figure 196: Current distribution in an insulated system with C phase fault**

The protection elements on the healthy feeder see the charging current imbalance for their own feeder. The protection element on the faulted feeder, however, sees the charging current from the rest of the system (IH1 and IH2 in this case). Its own feeder's charging current (IH3) is cancelled out.

With reference to the associated vector diagram, it can be seen that the C-phase to earth fault causes the voltages on the healthy phases to rise by a factor of √3. The A-phase charging current (Ia1), leads the resultant A phase voltage by 90°. Likewise, the B-phase charging current leads the resultant Vb by 90°.

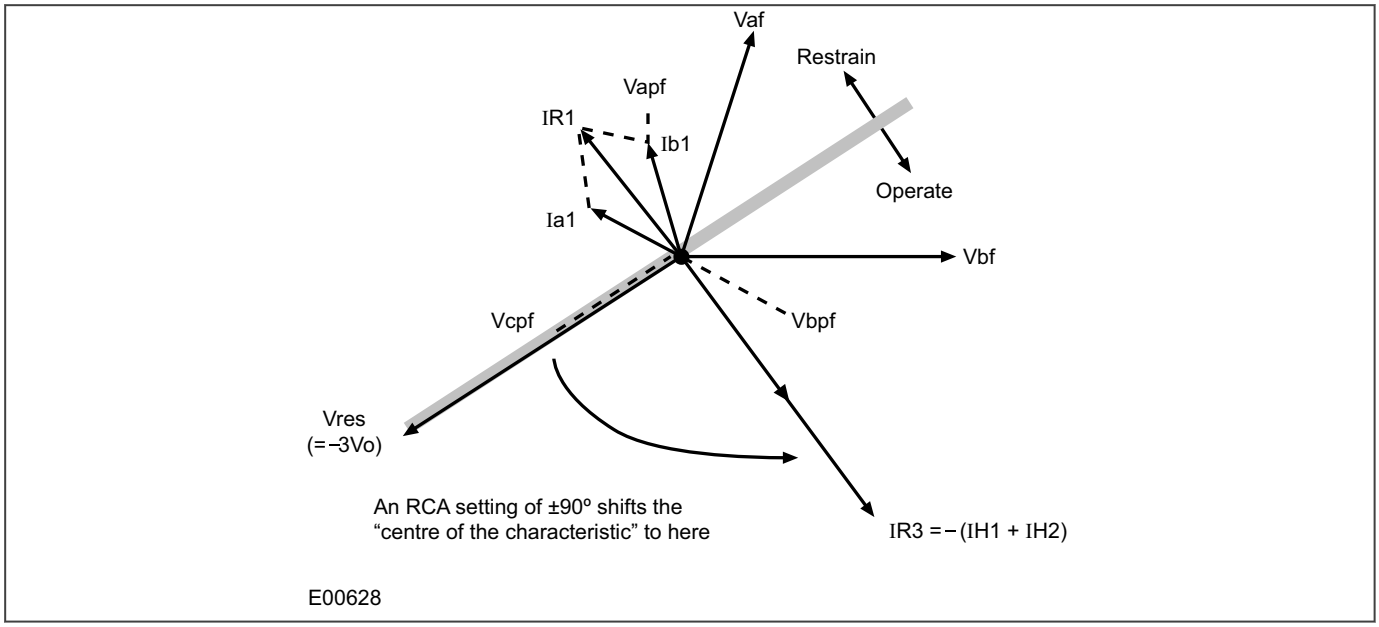



**Figure 197: Phasor diagrams for insulated system with C phase fault**

The current imbalance detected by a core balanced current transformer on the healthy feeders is the vector addition of Ia1 and Ib1. This gives a residual current which lags the polarising voltage (–3Vo) by 90°. As the healthy phase voltages have risen by a factor of √3, the charging currents on these phases are also √3 times larger than their steady state values. Therefore, the magnitude of the residual current IR1, is equal to 3 times the steady state per phase charging current.

The phasor diagram indicates that the residual currents on the healthy and faulted feeders (IR1 and IR3 respectively) are in anti-phase. A directional element (if available) could therefore be used to provide discriminative earth fault protection.

If the polarising is shifted through +90°, the residual current seen by the relay on the faulted feeder will lie within the operate region of the directional characteristic and the current on the healthy feeders will fall within the restrain region.

The required characteristic angle setting for the SEF element when applied to insulated systems, is +90°. This is for the case when the protection is connected such that its direction of current flow for operation is from the source busbar towards the feeder. If the forward direction for operation were set such that it is from the feeder into the busbar, then a –90° RCA would be required.

*Note:*
*Discrimination can be provided without the need for directional control. This can only be achieved, however, if it is possible to set the IED in excess of the charging current of the protected feeder and below the charging current for the rest of the system.*

### 11.5.4.2 SETTING GUIDELINES (INSULATED SYSTEMS)

The residual current on the faulted feeder is equal to the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the per phase value. Therefore, the total imbalance current is equal to three times the per phase charging current of the rest of the system. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the remaining system. Practically though, the required setting may well be determined on site, where suitable settings can be adopted based on practically obtained results.

When using a core-balanced transformer, care must be taken in the positioning of the CT with respect to the earthing of the cable sheath:

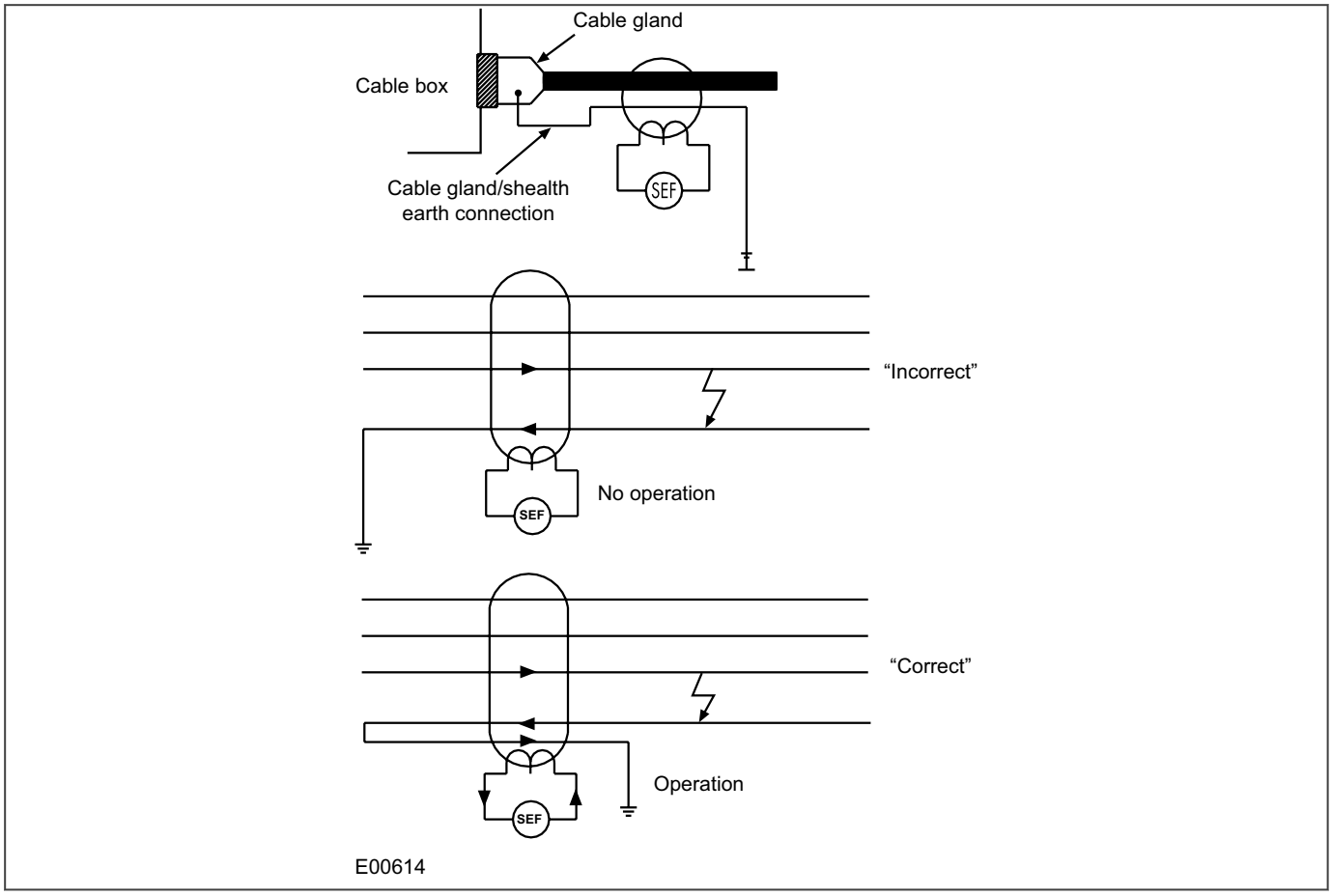



**Figure 198: Positioning of core balance current transformers**

If the cable sheath is terminated at the cable gland and directly earthed at that point, a cable fault (from phase to sheath) will not result in any unbalanced current in the core balance CT. Therefore, prior to earthing, the connection must be brought back through the CBCT and earthed on the feeder side. This then ensures correct relay operation during earth fault conditions.

## 11.6 HIGH IMPEDANCE REF

The device provides a high impedance restricted earth fault protection function. An external resistor is required to provide stability in the presence of saturated line current transformers. Current transformer supervision signals do not block the high impedance REF protection. The appropriate logic must be configured in PSL to block the high impedance REF when any of the above signals is asserted.

### 11.6.1 HIGH IMPEDANCE REF PRINCIPLE

This scheme is very sensitive and can protect against low levels of fault current, typical of winding faults.

High Impedance REF protection is based on the differential principle. It works on the circulating current principle as shown in the following diagram.

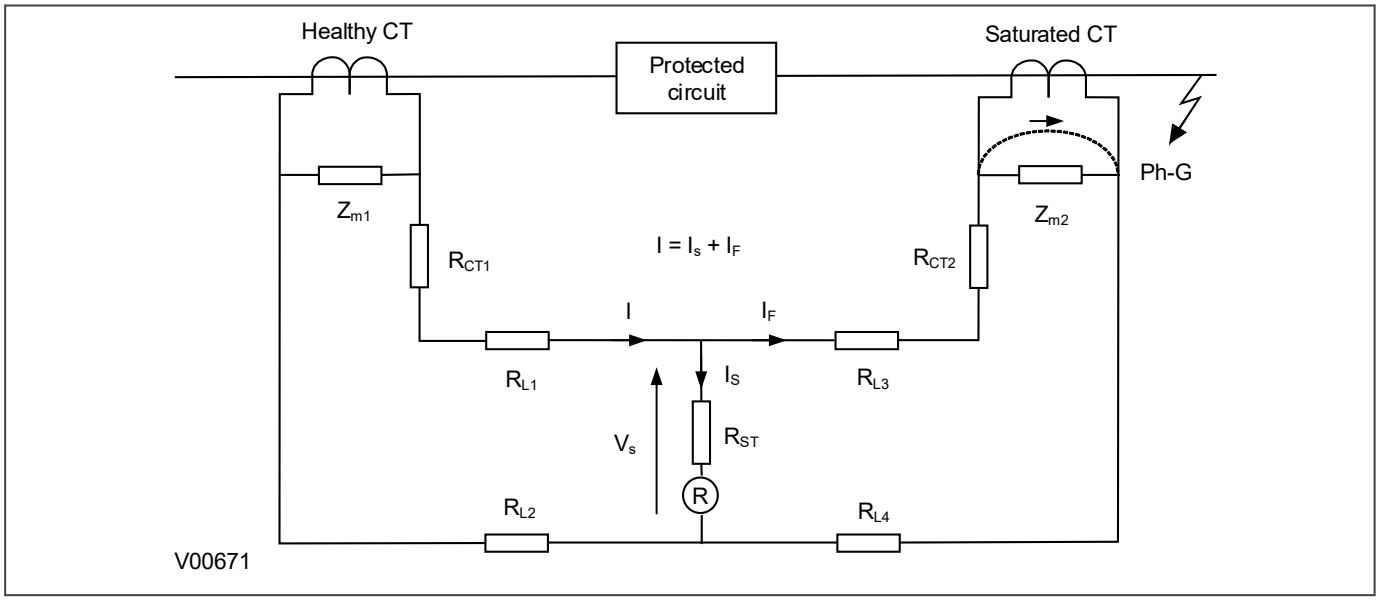



**Figure 199: High impedance REF principle**

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in imbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the device will be less than the setting, therefore maintaining stability during external faults.

Voltage across REF element $V_s = I_F (R_{CT2} + R_{L3} + R_{L4})$

Stabilising resistor $R_{ST} = V_s/I_s - R_R$

where:

- $I_F$ = maximum secondary through fault current
- $R_R$ = device burden
- $R_{CT}$ = CT secondary winding resistance
- $R_{L2}$ and $R_{L3}$ = Resistances of leads from the device to the current transformer
- $R_{ST}$ = Stabilising resistor

High Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED are as follows:

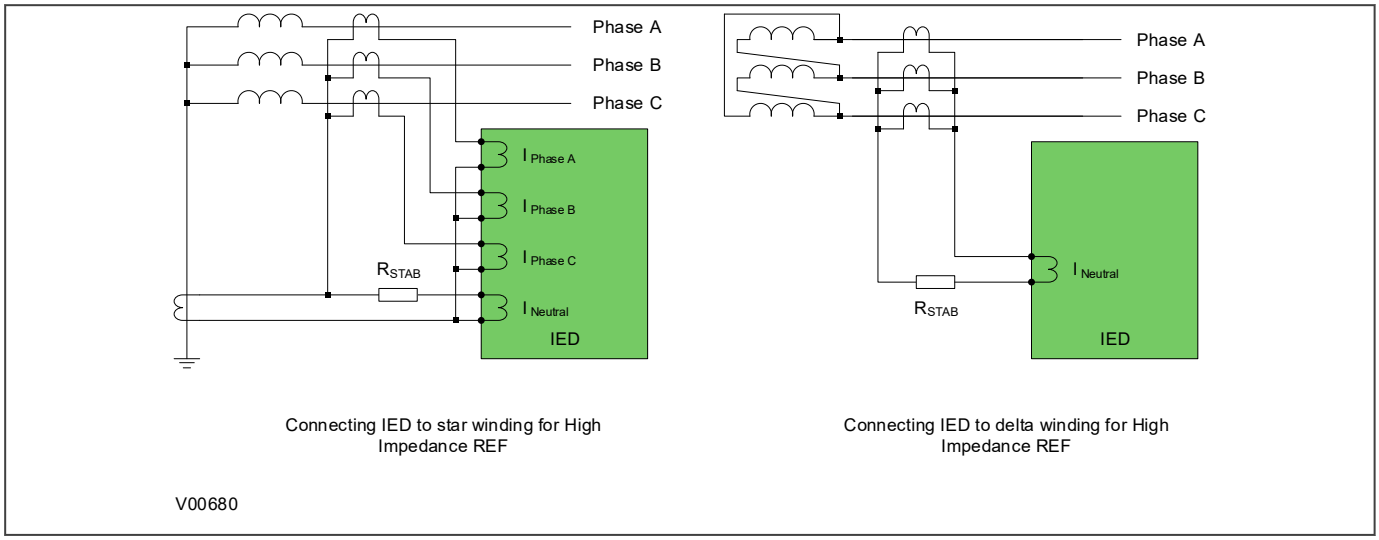



**Figure 200: High impedance REF connection**

# 11.7 THERMAL OVERLOAD PROTECTION

The heat generated within an item of plant is the resistive loss. The thermal time characteristic is therefore based on the equation $I^2Rt$. Over-temperature conditions occur when currents in excess of their maximum rating are allowed to flow for a period of time.

Temperature changes during heating follow exponential time constants. The device provides two characteristics for thermal overload protection; a single time constant characteristic and a dual time constant characteristic. You select these according to the application.

## 11.7.1 SINGLE TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect cables, dry type transformers and capacitor banks.

The single constant thermal characteristic is given by the equation:

$$t = -\tau \log_e \left[ \frac{I^2 - (KI_{FLC})^2}{I^2 - I_p^2} \right]$$

where:

- t = time to trip, following application of the overload current I
- $\tau$ = heating and cooling time constant of the protected plant
- I = largest phase current
- $I_{FLC}$ full load current rating (the Thermal Trip setting)
- K = a constant with the value of 1.05
- $I_p$ = steady state pre-loading before application of the overload

## 11.7.2 DUAL TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect equipment such as oil-filled transformers with natural air cooling. The thermal model is similar to that with the single time constant, except that two timer constants must be set.

For marginal overloading, heat will flow from the windings into the bulk of the insulating oil. Therefore, at low current, the replica curve is dominated by the long time constant for the oil. This provides protection against a general rise in oil temperature.

For severe overloading, heat accumulates in the transformer windings, with little opportunity for dissipation into the surrounding insulating oil. Therefore at high current levels, the replica curve is dominated by the short time constant for the windings. This provides protection against hot spots developing within the transformer windings.

Overall, the dual time constant characteristic serves to protect the winding insulation from ageing and to minimise gas production by overheated oil. Note however that the thermal model does not compensate for the effects of ambient temperature change.

The dual time constant thermal characteristic is given by the equation:

$$0.4e^{(-t/\tau_1)} + 0.6e^{(-t/\tau_2)} = \left[ \frac{I^2 - (KI_{FLC})^2}{I^2 - I_p^2} \right]$$

where:

- $\tau_1$ = heating and cooling time constant of the transformer windings
- $\tau_2$ = heating and cooling time constant of the insulating oil

## 11.7.3 THERMAL OVERLOAD PROTECTION IMPLEMENTATION

The device incorporates a current-based thermal characteristic, using Fourier based load current to model heating and cooling of the protected plant. The element can be set with both alarm and trip stages.

Thermal Overload Protection is implemented in the *THERMAL OVERLOAD* column of the relevant settings group.

This column contains the settings for the characteristic type, the alarm and trip thresholds and the time constants.

## 11.7.4 THERMAL OVERLOAD PROTECTION LOGIC

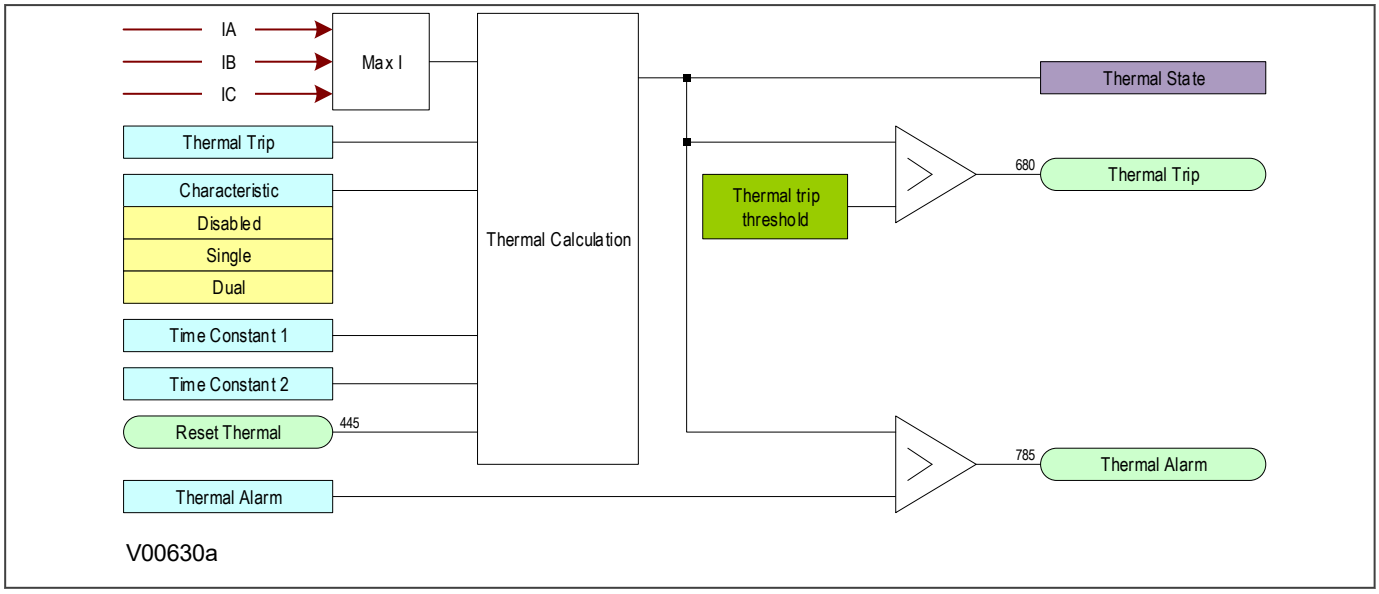



**Figure 201: Thermal overload protection logic diagram**

The magnitudes of the three phase input currents are compared and the largest magnitude is taken as the input to the thermal overload function. If this current exceeds the thermal trip threshold setting a start condition is asserted.

The Start signal is applied to the chosen thermal characteristic module, which has three outputs signals; alarm trip and thermal state measurement. The thermal state measurement is made available in one of the *MEASUREMENTS* columns.

The thermal state can be reset by either a digital signal (Opto, GOOSE, InterMiCOM), if assigned to this function using programmable scheme logic or the HMI panel menu.

## 11.7.5 APPLICATION NOTES

### 11.7.5.1 SETTING GUIDELINES FOR DUAL TIME CONSTANT CHARACTERISTIC

The easiest way of solving the dual time constant thermal equation is to express the current in terms of time and to use a spreadsheet to calculate the current for a series of increasing operating times using the following equation, then plotting a graph.

$$I = \sqrt{\frac{0.4I_p^{\,2}.e^{(-t/\tau 1)} + 0.6I_p^{\,2}.e^{(-t/\tau 2)} - k^2.I_{FLC}^{\,2}}{0.4e^{(-t/\tau 1)} + 0.6e^{(-t/\tau 2)} - 1}}$$

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1 | | | | | | |
| 2 | **Time constant 1 =** | | **300** | seconds | | |
| 3 | **Time constant 2 =** | | **7200** | seconds | | |
| 4 | **Pre-overload current Ip =** | | **0.9** | per unit | | |
| 5 | **Full load current =** | | **1** | Amps | | |
| 6 | | | | | | |
| 7 | **OP Time (t)** | **Overload current (I)** | | | | |
| 8 | 1 | 14.40852032 | | | | |
| 9 | 1.5 | 11.7805774 | | | | |
| 10 | 2 | 10.21617905 | | | | |
| 11 | 2.5 | 9.150045407 | | | | |
| 12 | 3 | 8.364131776 | | | | |
| 13 | 3.5 | 7.754150044 | | | | |
| 14 | 4 | 7.263123888 | | | | |
| 15 | 4.5 | 6.856949012 | | | | |

Figures based on equation

E00728

**Figure 202: Spreadsheet calculation for dual time constant thermal characteristic**

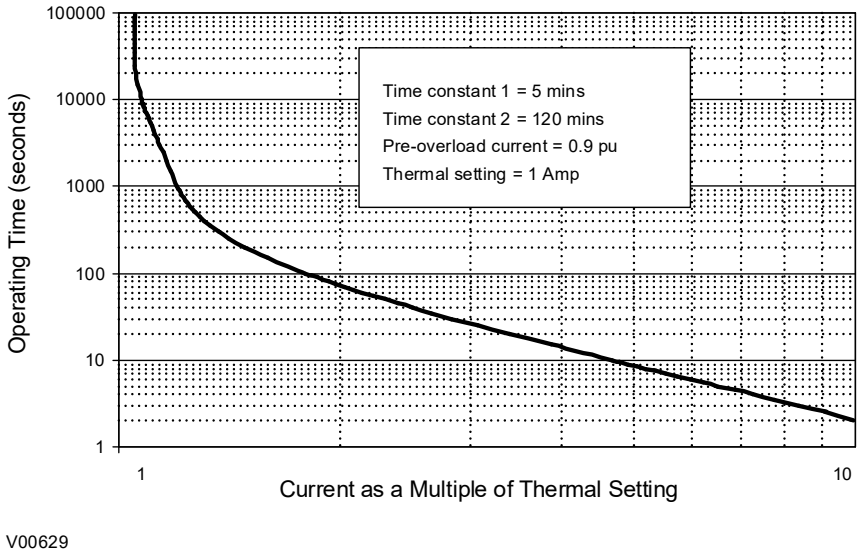



**Figure 203: Dual time constant thermal characteristic**

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the transformer item/CT ratio.

For an oil-filled transformer with rating 400 to 1600 kVA, the approximate time constants are:

- $\tau_1$ = 5 minutes
- $\tau_2$ = 120 minutes

An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be "Thermal Alarm" = 70% of thermal capacity.

*Note:*
*The thermal time constants given in the above tables are typical only. Reference should always be made to the plant manufacturer for accurate information.*

### 11.7.5.2 SETTING GUIDELINES FOR SINGLE TIME CONSTANT CHARACTERISTIC

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from hot or cold.

The thermal time constant characteristic may be rewritten as:

$$e^{(-t/\tau)} = \left[\frac{\theta - \theta_p}{\theta - 1}\right]$$

where:

- $\theta$ = thermal state = $I^2/K^2I_{FLC}^2$
- $\theta_p$ = pre-fault thermal state = $I_p^2/K^2I_{FLC}^2$
- $I_p$ is the pre-fault thermal state
- $I_{FLC}$ is the full load current

*Note:*
*A current of 105%Is ($KI_{FLC}$) has to be applied for several time constants to cause a thermal state measurement of 100%.*

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

The following tables show the approximate time constant in minutes, for different cable rated voltages with various conductor cross-sectional areas, and other plant equipment.

| Area $mm^2$ | 6 - 11 kV | 22 kV | 33 kV | 66 kV |
|---|---|---|---|---|
| 25 - 50 | 10 minutes | 15 minutes | 40 minutes | – |
| 70 - 120 | 15 minutes | 25 minutes | 40 minutes | 60 minutes |
| 150 | 25 minutes | 40 minutes | 40 minutes | 60 minutes |
| 185 | 25 minutes | 40 minutes | 60 minutes | 60 minutes |
| 240 | 40 minutes | 40 minutes | 60 minutes | 60 minutes |
| 300 | 40 minutes | 60 minutes | 60 minutes | 90 minutes |

| Plant Type | Time Constant (Minutes) |
|---|---|
| Dry-type transformer <400 kVA | 40 |
| Dry-type transformers 400 – 800 kVA | 60 - 90 |
| Air-core reactors | 40 |
| Capacitor banks | 10 |
| Overhead lines with cross section > 100 $mm^2$ | 10 |
| Overhead lines | 10 |
| Busbars | 60 |

# 11.8 BROKEN CONDUCTOR PROTECTION

One type of unbalanced fault is the 'Series' or 'Open Circuit' fault. This type of fault can arise from, among other things, broken conductors. Series faults do not cause an increase in phase current and so cannot be detected by overcurrent protection. However, they do produce an imbalance, resulting in negative phase sequence current, which can be detected.

It is possible to apply a negative phase sequence overcurrent element to detect broken conductors. However, on a lightly loaded line, the negative sequence current resulting from a series fault condition may be very close to, or less than, the full load steady state imbalance arising from CT errors and load imbalances, making it very difficult to distinguish. A regular negative sequence element would therefore not work at low load levels. To overcome this, the device incorporates a special Broken Conductor protection element.

The Broken Conductor element measures the ratio of negative to positive phase sequence current (I2/I1). This ratio is approximately constant with variations in load current, therefore making it more sensitive to series faults than standard negative sequence protection.

## 11.8.1 BROKEN CONDUCTOR PROTECTION IMPLEMENTATION

Broken Conductor protection is implemented in the *BROKEN CONDUCTOR* column of the relevant settings group.

This column contains the settings to enable the function, for the pickup threshold and the time delay.

## 11.8.2 BROKEN CONDUCTOR PROTECTION LOGIC

The ratio of $I_2/I_1$ is calculated and compared with the threshold setting. If the threshold is exceeded, the delay timer is initiated. The CTS block signal is used to block the operation of the delay timer.

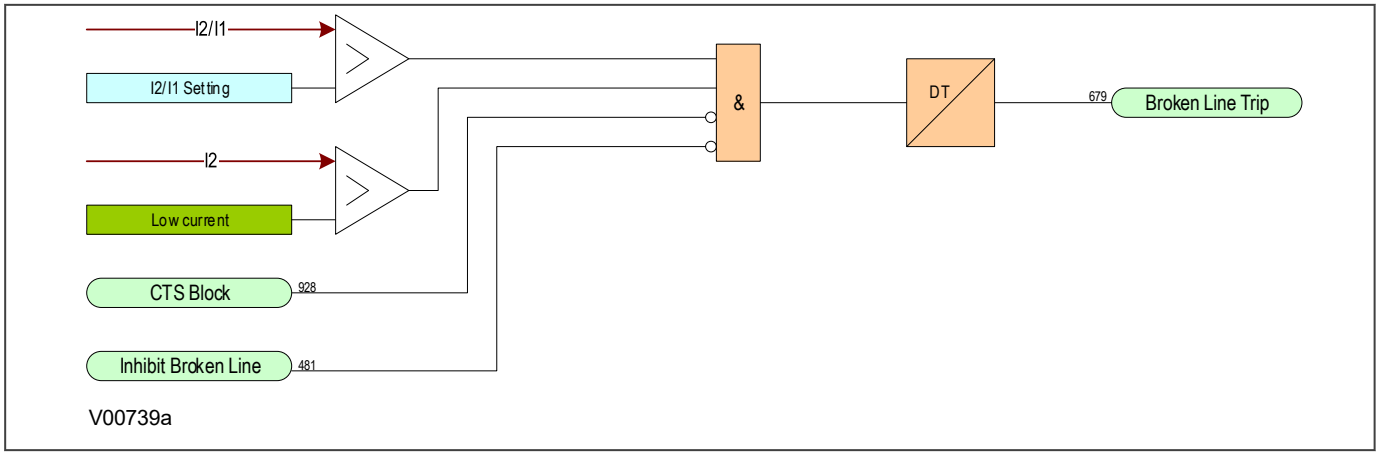



**Figure 204: Broken conductor logic**

## 11.8.3 APPLICATION NOTES

### 11.8.3.1 SETTING GUIDELINES

For a broken conductor affecting a single point earthed power system, there will be little zero sequence current flow and the ratio of $I_2/I_1$ that flows in the protected circuit will approach 100%. In the case of a multiple earthed power system (assuming equal impedance's in each sequence network), the ratio $I_2/I_1$ will be 50%.

In practise, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for.

*Note:*
*A minimum value of 8% negative phase sequence current is required for successful operation.*

Since sensitive settings have been employed, we can expect that the element will operate for any unbalanced condition occurring on the system (for example, during a single pole autoreclose cycle). For this reason, a long time delay is necessary to ensure co-ordination with other protection devices. A 60 second time delay setting may be typical.

The following example was recorded by an IED during commissioning:

$$I_{\text{full load}} = 500\text{A}$$

$$I_2 = 50\text{A}$$

therefore the quiescent $I_2/I_1$ ratio = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical: Therefore set:

$$I_2/I_1 = 0.2$$

In a double circuit (parallel line) application, using a 40% setting will ensure that the broken conductor protection will operate only for the circuit that is affected. A setting of 0.4 results in no pick-up for the parallel healthy circuit.

Set $I_2/I_1$ Time Delay = 60 s to allow adequate time for short circuit fault clearance by time delayed protections.

# 11.9 TRANSIENT EARTH FAULT DETECTION

Some distribution systems run completely insulated from earth. Such systems are called unearthed systems. The advantage of an unearthed system is that a single phase to earth fault does not cause an earth fault current to flow. This means the whole system remains operational and the supply is not interrupted. The system must be designed to withstand high transient and steady state overvoltages, however, and so its use is generally restricted to low and medium voltage distribution systems.

When there is an earth fault in an unearthed 3-phase system, the voltage of the faulted phase is reduced to the earth potential. This causes the phase voltage in the other two phases to increase, which causes a significant charging current between the phase-to-earth capacitances. This can cause arcing at the fault location. Many systems use a Petersen coil to compensate for this, thus eliminating the arcing problem. Such systems are called compensated networks. The network is earthed with an inductive reactor, where its reactance is made nominally equal to the total system capacitance to earth. Under this condition, a single-phase earth fault does not result in any steady state earth fault current.

The introduction of a Petersen coil introduces major difficulties when it comes to determining the direction of the fault. This is because the faulted line current is the sum of the inductive current introduced by the Petersen coil and the capacitive current of the line, which are in anti-phase with each other. If they are equal in magnitude, the current in the faulted line is zero. If the inductive current is larger than capacitance current, the direction of the faulted line current will appear to be in the same direction as that of the healthy line.

Standard directionalizing techniques used by conventional feeder protection devices are not adequate for this scenario, therefore we need a different method for determining the direction of the fault. Two commonly used methods are the First Half Wave method and the Residual Active Power method.

### First Half Wave Method

The initial transient wave, generated at the fault point travels towards the bus along the faulted line, until it reaches the healthy line. For forward faults the high frequency fault voltage and current components are in opposite directions during the first half wave, whereas for reverse faults, they are in phase. This fact can be used to determine the fault direction. This method, however, is subject to the following disadvantages:

- The time duration of the characteristic is very short, in most cases not more than 3 ms. Because of this, it requires a high sampling frequency (3000Hz or even higher)
- It requires an analogue high pass filter, necessitating special hardware
- It is affected by the fault inception angle. For example, when the fault inception angle is 0°, there are no initial travelling waves.

### Residual Active Power Method

Residual Active power, which is sometimes used to detect the instance of a fault can also in some cases be used for detecting the fault direction. Although the capacitive currents can be compensated by an inductive current generated by a Petersen coil, the active (instantaneous) current can never be compensated for and this is still opposite to that of the healthy line. This fact can also be used to directionalise the fault.

For a forward directional fault, the zero-sequence active power is the power loss of Petersen's coil, which is negative. For a reverse fault, the zero-sequence active power is the power loss of the transmission line, which is positive. This method, however, is subject to the following disadvantages:

- The zero-sequence active power will be very small in magnitude for a reverse directional fault. Its value depends on the power loss of transmission line.
- The zero-sequence active power may be too small in magnitude to be detected for a forward directional fault. Its value depends on the power loss of Petersen coil.
- High resolution CTs are required

Due to the low magnitude of measured values, reliability is compromised

This product does not use the above techniques for directionalisation. This product uses an innovative patented technique called Transient Reactive Power method to determine the fault direction of an earth fault in a compensated network.

## 11.9.1 TRANSIENT EARTH FAULT DETECTION IMPLEMENTATION

Transient Earth Fault Detection (TEFD) in this device comprises three modules:

- Transient Earth Fault Detection module (TEF)
- Fault Type Detector (FTD)
- Direction Detector (DD)

*Note:*
*In this product, TEFD is implemented for 50Hz only.*

### 11.9.1.1 TRANSIENT EARTH FAULT DETECTOR

To establish if there is an earth fault on the system somewhere is straightforward. A simple residual overvoltage comparison can determine this. Therefore, a TEF> Start signal is produced by comparing the neutral voltage with a threshold voltage set by ***TEF VN> Start*** in the *TEF DETECTION* column. The difficulty comes with establishing the type of fault and its direction.

### 11.9.1.2 FAULT TYPE DETECTOR

The FTD uses a Fundamental analysis (FA) technique to establish whether the fault is an intermittent fault or a steady state faults. For Transient Earth Fault Detection, the detector counts the Residual Voltage bursts within a specified time window. With some clever signal processing the detector module creates pulses by comparing the bursts with a settable threshold, then counts these pulses. If the number of pulses equals or exceeds the number specified by the ***FTD> Fault Count*** setting, within the time window specified by ***FTD> Time Window***, the fault is deemed to be intermittent and the ***TEF> Intermit DDB*** signal is asserted. If there are fewer pulses than this number, this indicates either a disturbance or a permanent fault. To establish which, we need to look at the RMS value of the residual voltage.

If there are fewer pulses than specified and the RMS value does not drop below setting within the specified time window, the fault is deemed to be permanent. In this case the ***TEF> Steady*** DDB signal is asserted.

If there are fewer pulses than specified and the RMS value does drop below setting, this indicates that a disturbance has been detected but it is not a fault. In this case, the ***TEF> Steady*** DDB signal is not asserted.

The user can map the signals ***TEF>Steady***, ***TEF>Intermit***, ***TEF>DIR FWD*** or ***TEF> DIR REV*** to the TEF Alarm Logic DDB to generate a TEF Alarm.

The inputs to this module are:

- The residual voltage
- ***FTD> VN*** (defines the threshold which converts the residual voltage burst into a pulse
- ***FTD> Time Window*** (defines the time window - default is 2 seconds)
- ***FTD> Fault Count*** (defines the fault count)

The FTD outputs two signals to indicate whether the fault is steady state or intermittent.

### 11.9.1.3 DIRECTION DETECTOR

The Direction Detector (DD) uses a patented technique based on Transient Reactive Power (TRP) to establish the direction of the fault. Unlike traditional methods, this TRP method does not require high resolution CTs or special analogue filtering hardware and is therefore cheaper to implement.

It can be shown that the residual voltage and residual current components can be reliably used as discriminative criteria between a faulty and healthy feeder at 220Hz.

The admittance response of a healthy distributed feeder is shown below using a Pi model:

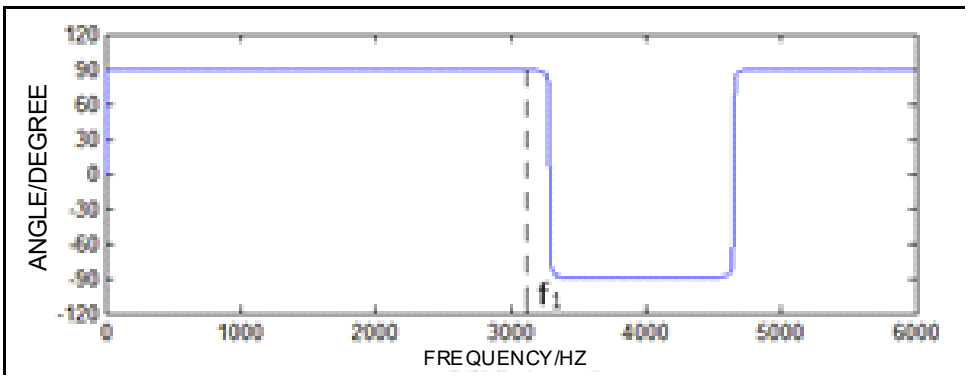



**Figure 205: Healthy line response**

In the above figure, the phase response of the admittance is consistent at 90o up to frequency f1 (approximately 3000Hz). For a compensated faulty feeder, the admittance response is shown below using a Pi model:

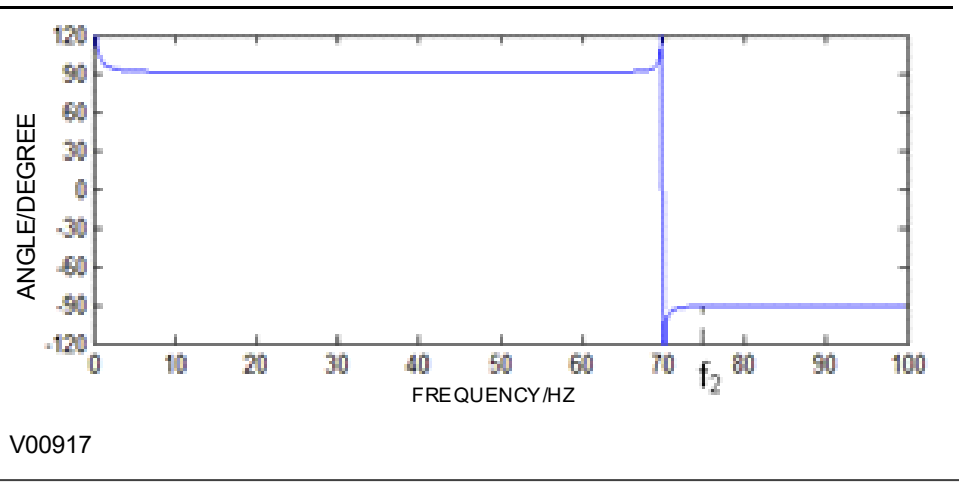



**Figure 206: Faulty line response**

We can observe that the phase angle (and thus, the reactive power flow) changes from 90o to -90o at frequencies higher than f2. Based on the above, we have clear direction discrimination between a healthy and faulted feeder at any frequency between f2 and f1 approximately.

*Note:*
*The resonant frequency in the above system is 70Hz. For a perfectly compensated system, this will be 50Hz.*

MiCOM relays use an anti-aliasing band pass filter with cut-off frequency of 150Hz. Furthermore, at 220Hz the post-filter magnitude is approximately 0.5pu, and at 330Hz, it is less than 0.2pu. To avoid any integer harmonics, and to avoid severely attenuated quantities due to the filter, we have chosen 220Hz as the most suitable frequency for direction determination.

In the forward direction, the residual voltage leads the residual current by 90°, and in the reverse direction the residual voltage lags the residual current by 90°. These criteria can be used to directionalise the fault.

The residual voltage (Vres) after passing through the bandpass filter tuned to 220 Hz, has 90° added to its phase. The residual current (Ires) is also passed through a 220 Hz bandpass filter, but no phase shift is applied. The resulting components which we shall call VH1 and IH2 are therefore in antiphase with each other for forward faults and in phase if the forward line is not faulted.

The VH1 and IH2 components are passed through a sign filter and multiplied to create a reactive power component in the range of -1 to +1. This is the transient reactive power $Q_{tran}$. If $Q_{tran} > 0$, then there forward line is healthy. If $Q_{tran} < 0$, then the forward line is faulty.

There are two modes of operation for the direction detector; Standard and Advanced. Standard mode is used in most cases and is described here. Advanced mode is for special applications that deviate from the standard model of two or more geographically close feeders outgoing from a power transformer. The following default settings are recommended for majority of applications:

- Dir>Vnf Thresh 8.000 V
- Dir>Inf Thresh 50.00 mA
- Dir>Qn Thresh 100.0e-3
- Dir>Qr Thresh 40.00e-3

When ***TEF>Dir Mod*** is set to ***Advance***, the following settings become visible:

- ***Dir>Qs Thresh*** 50.00e-3
- ***Qn Smooth fct*** 20.00e-3
- ***Operate.Cycles*** 6

Here, Qs is an integration of $Q_n$, with the window of integration being the first ***Operate cycles*** setting after the start signal is triggered. $Q_s$ is used as a further discriminative directional feature if direction cannot be determined by $Q_n$ only. $Q_S$ is calculated by the following formula:

$$Q_S = \int_{(t=0)}^{(t=K*T)} (Q_{N(t)})$$

Where 'K' is the setting Operate Cycles. Operate Cycles affects Qs only.

Qn Smooth fact is a smoothing factor for consecutive Qn values which prevents sudden changes in the value of Qn. The calculated new value of Qn is:

new_valueQn = old_value*(1-smoothing_factor)+ new_value*smoothing_factor.

It is important to note that all settings for the TGFD function, including those at 220Hz, can be set based on 50Hz nominal secondary values. This is because the gain of the 220Hz transient filter is 1.

The inputs to this module are:

- The residual voltage
- The residual current
- ***Dir> Vnf Thresh*** (defines the threshold for the residual voltage sign filter).
- ***Dir> Inf Thresh*** (defines the threshold for the residual current sign filter

The DD outputs two signals to indicate a forward fault and a reverse fault

### Sign Filter Thresholds

The ***Dir> Vnf Thresh*** setting is used to get the sign of instantaneous voltage value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

The ***Dir> Inf Thresh*** setting is used to get the sign of instantaneous current value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

### $Q_{tran}$ Thresholds

The setting ***Dir>Qn Thresh*** is the forward direction $Q_{tran}$ threshold calculated from the quantised Vnf and Inf values.

The setting ***Dir>Qr*** is the reverse direction $Q_{trans}$ threshold calculated from the quantised Vnf and Inf values.

The following DDBs are also available:

***Timer Block***: used to inhibit the TEF function and reset all associated DDBs

***Reset TEF***: can be configured as a user-defined manual reset alarms

***TEF Alarm Output***: This is the main TEF alarm that can be mapped to a relay output for a trip

## 11.9.2 TRANSIENT EARTH FAULT DETECTION LOGIC

### 11.9.2.1 TRANSIENT EARTH FAULT DETECTION LOGIC OVERVIEW

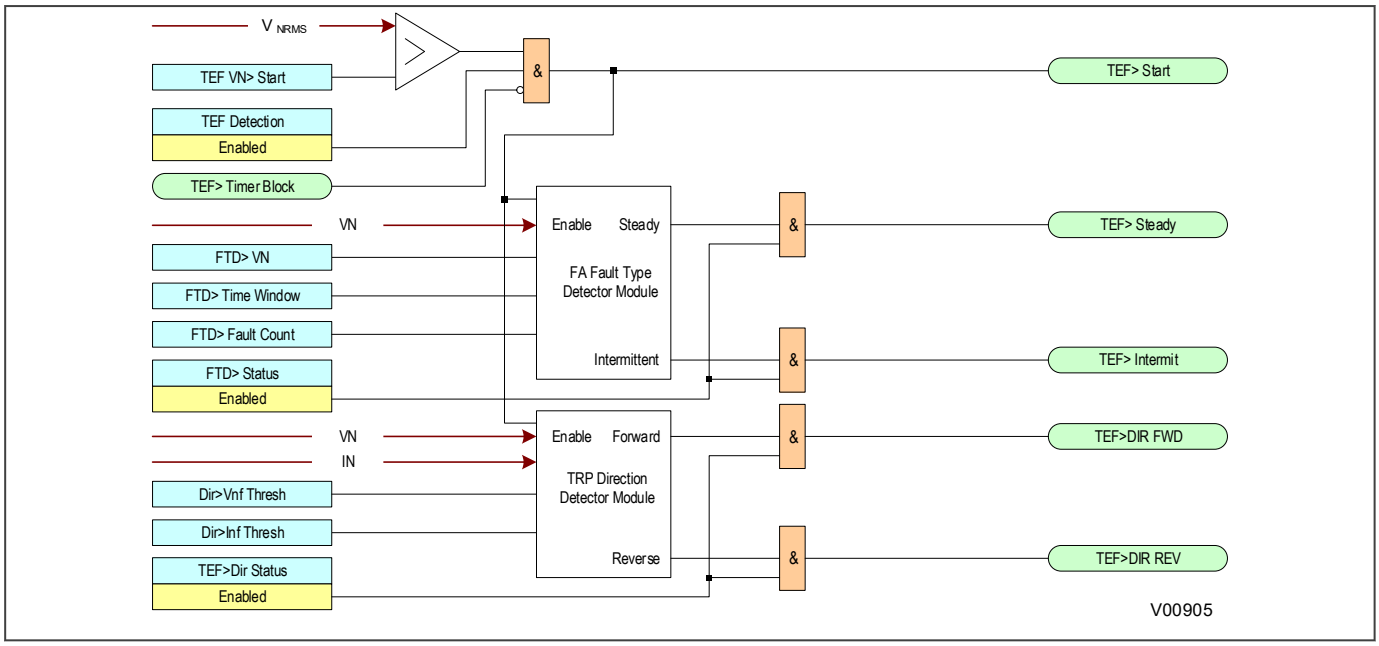



**Figure 207: Transient Earth Fault Logic Overview**

### 11.9.2.2 FAULT TYPE DETECTOR LOGIC

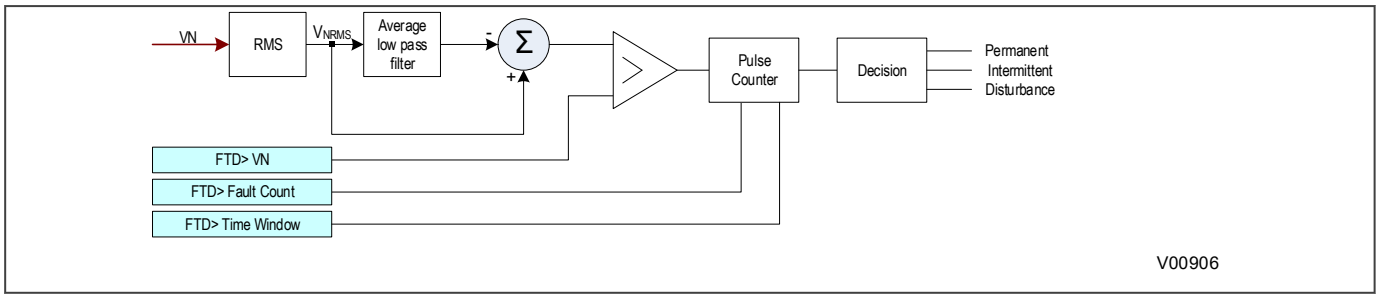



**Figure 208: Fault Type Detector Logic**

### 11.9.2.3 DIRECTION DETECTOR LOGIC - STANDARD MODE

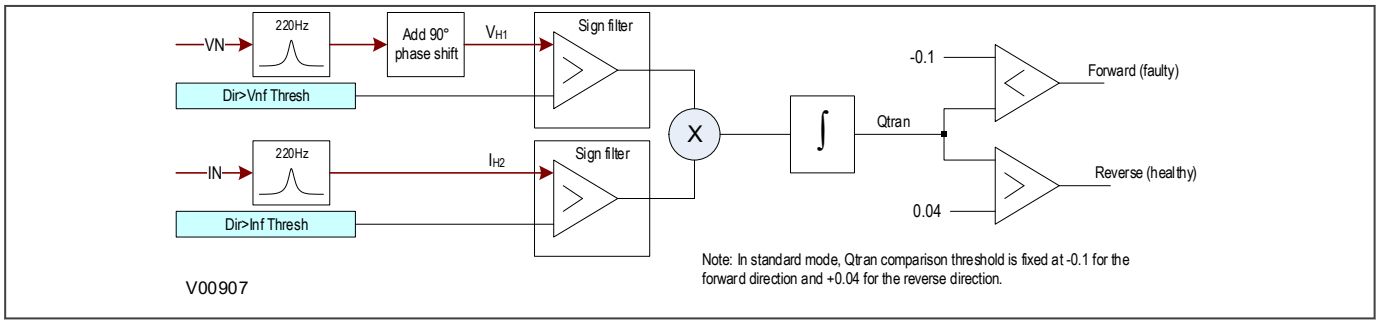



**Figure 209: Direction Detector Logic - Standard Mode**

### 11.9.2.4 TRANSIENT EARTH FAULT DETECTION OUTPUT ALARM LOGIC

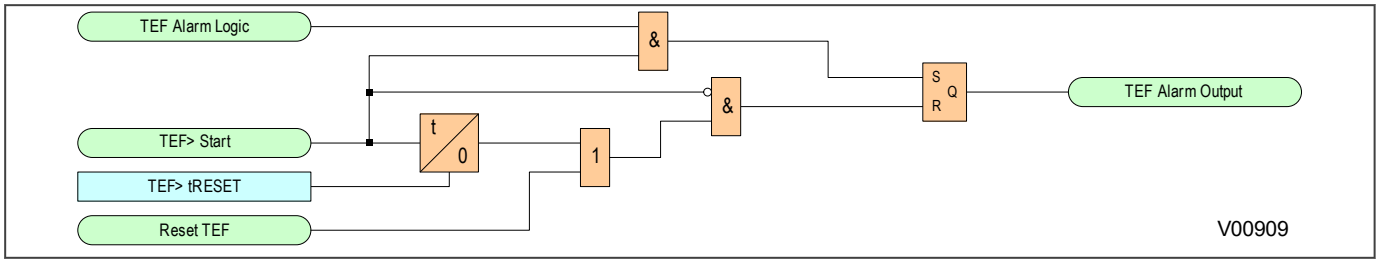



**Figure 210: TEFD output alarm logic**

### 11.9.2.5 APPLICATION NOTES

#### 11.9.2.5.1 TRANSIENT EARTH FAULT DETECTION: ACTIVE POWER CHECK

A preventive measure should be taken in cases when relays are located at the extremities of a radial system, where the charging current component reduces the further the relay is from the source, and the active component remains small but constant. In these cases, the transient active current component can be comparable to the transient reactive current during the directional check of the TEFD algorithm.

To ensure correct directionality for all fault positions and system configurations (radial, ring or meshed), the TEFD algorithm shall be supplemented with an additional element - 'Active Power Check'. This scheme ensures the correct directional decision is raised regardless of residual active power levels present in the system at the time of the fault. Sensitive Directional Earth Fault (SDEF) with Active Power Check shall be applied in parallel with the TEFD algorithm.

The combined logic for the TEFD and SDEF is shown in Figure below. A 'Forward START' (shown as a name modified User Alarm) signal is raised when either TEFD FWD or SDEF FWD signals are active. However, 'Forward START' is inhibited if the SDEF REV signal is ever active. This ensures SDEF takes priority if there is enough residual active power during a fault condition. For cases where the residual active power is low, the TEFD algorithm provides the directional decision.

An additional 100ms delay is included to delay the start conditions, thus ensuring the SDEF protection is not adversely affected by the initial fault transient. The TEFD logic is unaffected by the additional timer as its directional decision is latched for a minimum of 200ms after fault inception.

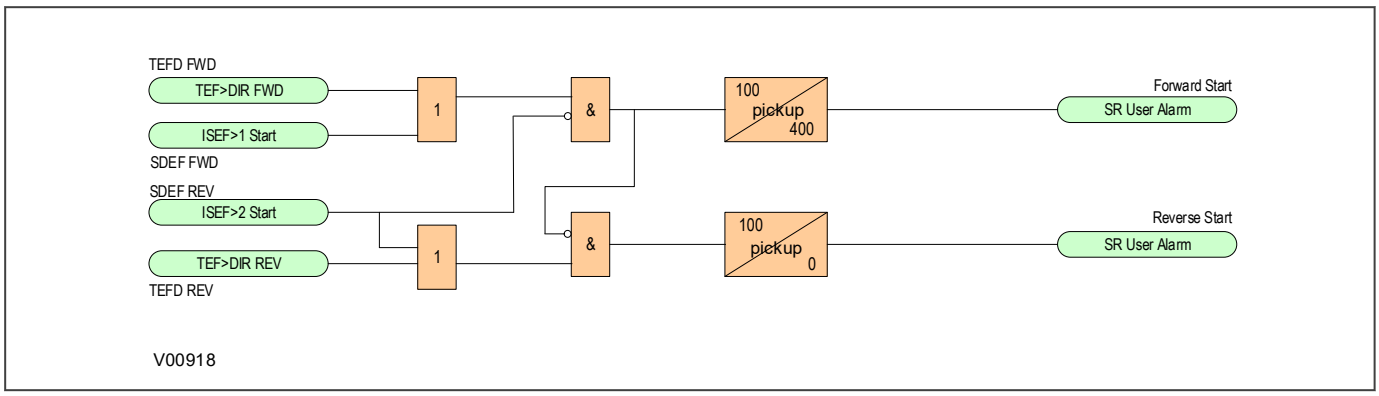



**Figure 211: Combined TEFD and SDEF start PSL logic**

CHAPTER 12

# VOLTAGE PROTECTION FUNCTIONS

## 12.1 CHAPTER OVERVIEW

The device provides a wide range of voltage protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 322
Undervoltage Protection 323
Overvoltage Protection 326
Compensated Overvoltage 329
Residual Overvoltage Protection 330

## 12.2 UNDERVOLTAGE PROTECTION

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Undervoltage conditions can be related to increased loads, whereby the supply voltage will decrease in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an undervoltage condition, which must be cleared.
- If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping by means of an undervoltage element is required.
- Faults occurring on the power system result in a reduction in voltage of the faulty phases. The proportion by which the voltage decreases is dependent on the type of fault, method of system earthing and its location. Consequently, co-ordination with other voltage and current-based protection devices is essential in order to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be necessary to isolate each of the outgoing circuits, such that when supply voltage is restored, the load is not connected. Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This can be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions that last longer than a pre-determined time.

### 12.2.1 UNDERVOLTAGE PROTECTION IMPLEMENTATION

Undervoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Undervoltage parameters are contained within the sub-heading *UNDERVOLTAGE*.

The product provides two stages of Undervoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V<1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage (***V<(n) Voltage Set***)

The undervoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V< Measur't Mode*** cell.

There is no Timer Hold facility for Undervoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V<2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V< Operate Mode*** cell for each stage.

## 12.2.2 UNDERVOLTAGE PROTECTION LOGIC

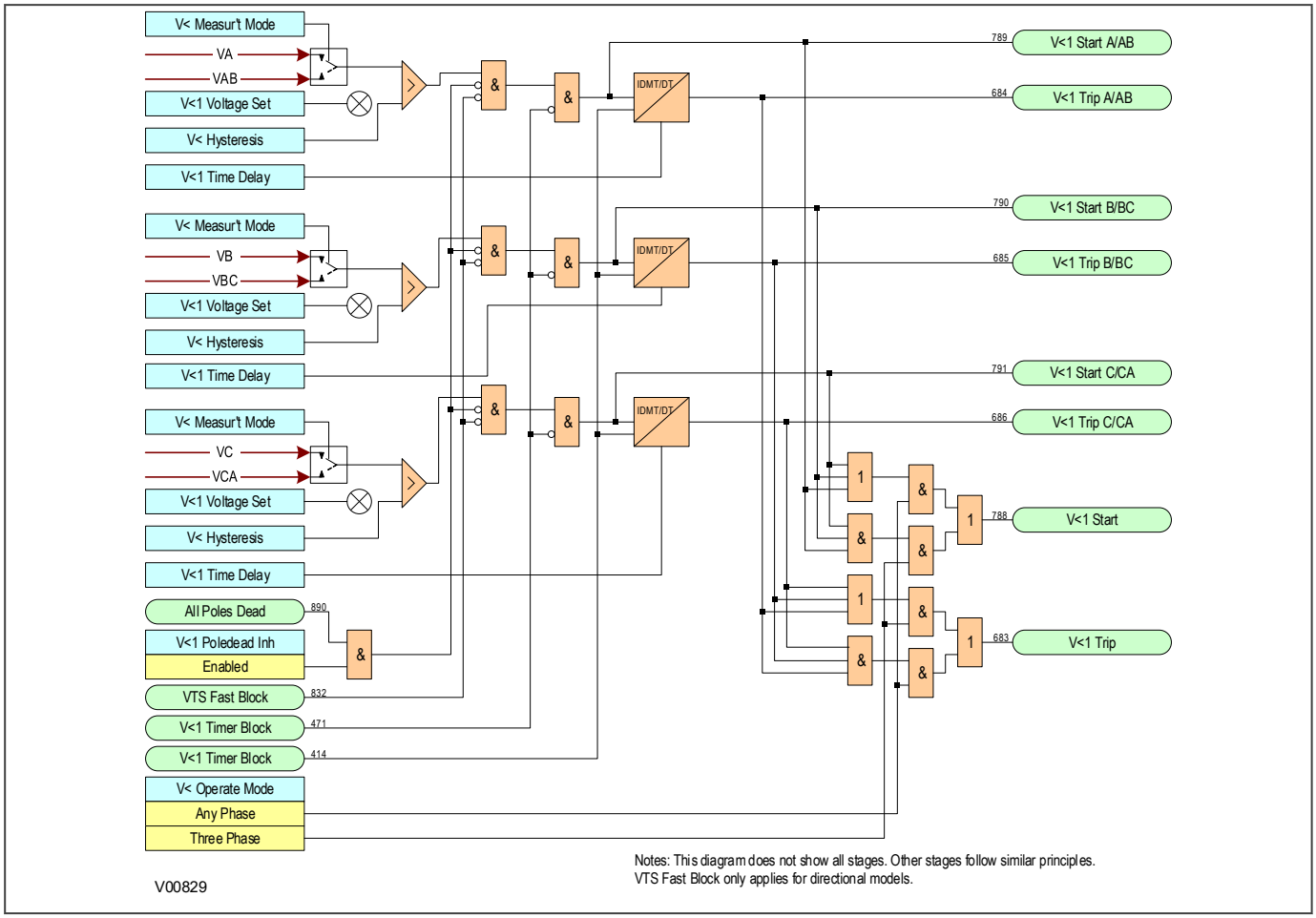



**Figure 212: Undervoltage - single and three phase tripping mode (single stage)**

The Undervoltage protection function detects when the voltage magnitude for a certain stage falls short of a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal and an ***All Poles Dead*** signal. This ***Start*** signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the undervoltage timer block signal (***V<(n) Timer Block***). For each stage, there are three Phase undervoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V<(n) Start***), which can be be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V< Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V< Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

In some cases, we do not want the undervoltage element to trip; for example, when the protected feeder is de-energised, or the circuit breaker is opened, an undervoltage condition would obviously be detected, but we would not want to start protection. To cater for this, an ***All Poles Dead*** signal blocks the ***Start*** signal for each phase. This is controlled by the ***V<Poledead Inh*** cell, which is included for each of the stages. If the cell is enabled, the relevant stage will be blocked by the integrated pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the opto-inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***V< Hysteresis*** setting. For example, where the ***V<Hysteresis*** default setting is *2*, relay pick-up will be at set voltage and drop-off will be at 102% of set voltage.

## 12.2.3 APPLICATION NOTES

### 12.2.3.1 UNDERVOLTAGE SETTING GUIDELINES

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case you should select phase-to-phase voltage measurement, as this quantity is less affected by single-phase voltage dips due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependent on the system in question but typical healthy system voltage excursions may be in the order of 10% of nominal value.

The same applies to the time setting. The required time delay is dependent on the time for which the system is able to withstand a reduced voltage.

If motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

## 12.3 OVERVOLTAGE PROTECTION

Overvoltage conditions are generally related to loss of load conditions, whereby the supply voltage increases in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an overvoltage condition which must be cleared.

*Note:*
*During earth fault conditions on a power system there may be an increase in the healthy phase voltages. Ideally, the system should be designed to withstand such overvoltages for a defined period of time.*

### 12.3.1 OVERVOLTAGE PROTECTION IMPLEMENTATION

Overvoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Overvoltage parameters are contained within the sub-heading *OVERVOLTAGE*.

The product provides two stages of overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V>1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/( M - 1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage setting voltage (***V>(n) Voltage Set***)

The overvoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V> Measur't Mode*** cell.

There is no Timer Hold facility for Overvoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V>2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V> Operate Mode*** cell for each stage.

## 12.3.2 OVERVOLTAGE PROTECTION LOGIC

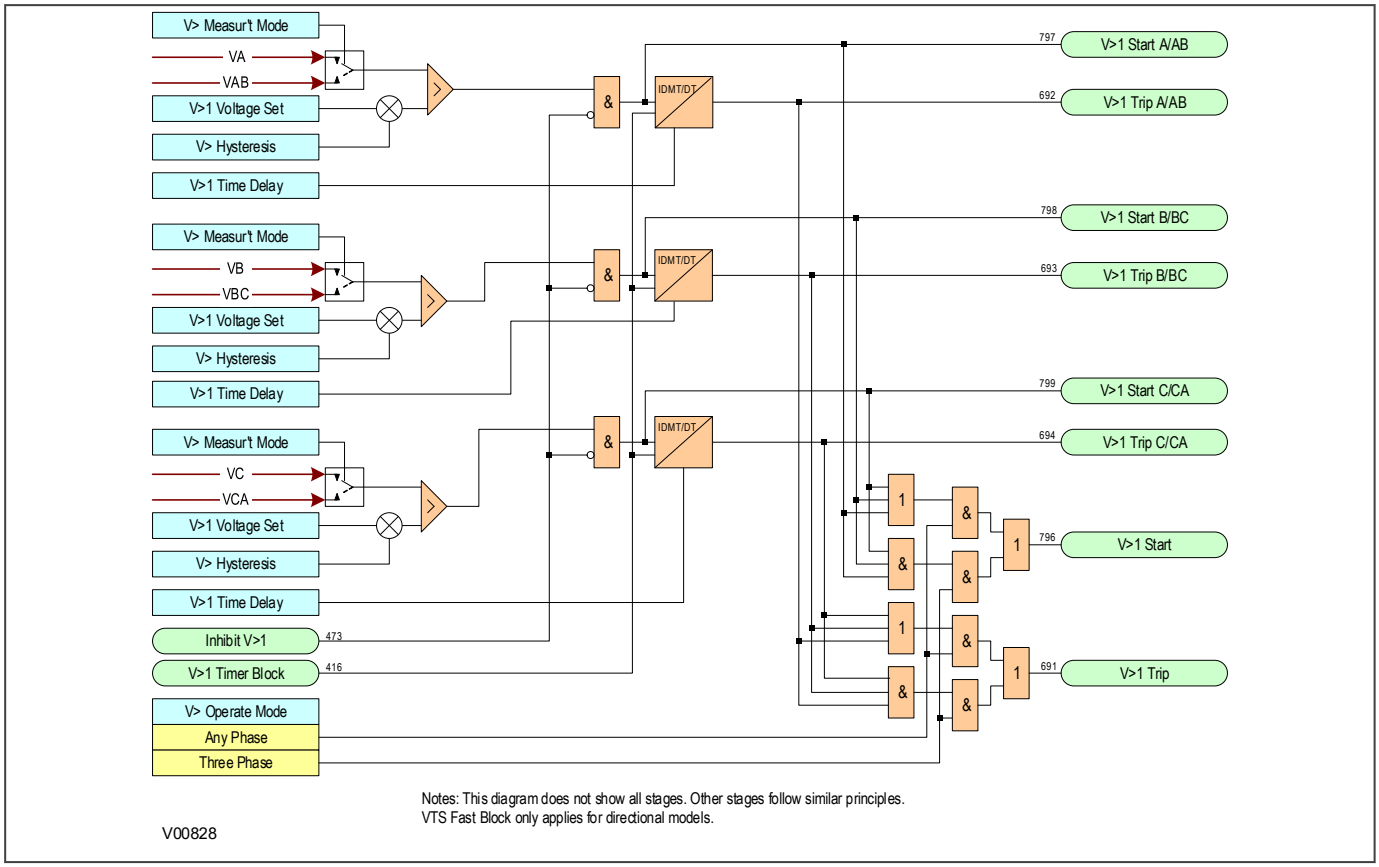



**Figure 213: Overvoltage - single and three phase tripping mode (single stage)**

The Overvoltage protection function detects when the voltage magnitude for a certain stage exceeds a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal. This start signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the overvoltage timer block signal (***V>(n) Timer Block***). For each stage, there are three Phase overvoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V>(n) Start***), which can then be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V> Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V> Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***V> Hysteresis*** setting. For example, where the ***V>Hysteresis*** default setting is *2*, relay pick-up will be at set voltage and drop-off will be at 98% of set voltage.

## 12.3.3 APPLICATION NOTES

### 12.3.3.1 OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

## 12.4 COMPENSATED OVERVOLTAGE

The Compensated Overvoltage function calculates the positive sequence voltage at the remote terminal using the positive sequence local current and voltage and the line impedance and susceptance. This can be used on long transmission lines where Ferranti Overvoltages can develop under remote circuit breaker open conditions.

The Compensated overvoltage protection function can be set in the *VOLT PROTECTION* column under the sub heading COMP OVERVOLTAGE. The remote voltage is calculated using line impedance settings and the line charging admittance in the *LINE PARAMETERS* column.

The IED uses the [A,B,C,D] transmission line equivalent model given the following parameters:

- Total Impedance Z = $z\angle\theta$ ohms
- Total Susceptance Y = $y\angle -90°$
- Line Length l

The remote voltage is calculated using the following equations:

$$\begin{bmatrix} \bar{V}r \\ \bar{I}r \end{bmatrix} = \begin{bmatrix} D & -C \\ -BA & \end{bmatrix} \times \begin{bmatrix} \bar{V}s \\ \bar{I}s \end{bmatrix}$$

where

- $V_r$ is the voltage at the receiving end
- $I_r$ is the current at the receiving end
- $V_s$ is the measured voltage at the sending end
- $I_s$ is the measured current at the sending end
- A= D = cosh(y.l)
- B = $Z_c$.sinh(y.l)
- C = $Y_c$.sinh(y.l)
- y.l = $\sqrt{}$(Z.Y)
- $Z_c$ = 1/$Y_c$ = $\sqrt{}$(Z/Y)
- Y = total line capacitive charging susceptance
- $Z_c$ = characteristic impedance of the line (surge impedance)

There are two stages to provide both alarm and trip stages where required. Both stages can be set independently.

Stage 1 can be set to `IDMT`, `DT` or `Disabled`, in the ***V1>1 Cmp Funct*** cell. Stage 2 is DT only and is enabled or disabled in the ***V1>2 Cmp Status*** cell.

The IDMT characteristic on the first stage is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t =Operating time in seconds
- M = Remote Calculated voltage / IED setting voltage

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***Cp V Hysteresis*** setting. For example, where the ***Cp V Hysteresis*** default setting is `2`, relay pick-up will be at set voltage and drop-off will be at 98% of set voltage.

## 12.5 RESIDUAL OVERVOLTAGE PROTECTION

On a healthy three-phase power system, the sum of the three-phase to earth voltages is nominally zero, as it is the vector sum of three balanced vectors displaced from each other by 120°. However, when an earth fault occurs on the primary system, this balance is upset and a residual voltage is produced. This condition causes a rise in the neutral voltage with respect to earth. Consequently this type of protection is also commonly referred to as 'Neutral Voltage Displacement' or NVD for short.

This residual voltage may be derived (from the phase voltages) or measured (from a measurement class open delta VT). Derived values will normally only be used where the model does not support measured functionality (a dedicated measurement class VT). If a measurement class VT is used to produce a measured Residual Voltage, it cannot be used for other features such as Check Synchronisation.

This offers an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balanced current transformers on each feeder may be either impractical, or uneconomic, or for providing earth fault protection for devices with no current transformers.

### 12.5.1 RESIDUAL OVERVOLTAGE PROTECTION IMPLEMENTATION

Residual Overvoltage Protection is implemented in the *RESIDUAL O/V NVD* column of the relevant settings group.

Some applications require more than one stage. For example an insulated system may require an alarm stage and a trip stage. It is common in such a case for the system to be designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The product provides two stages of Derived Residual Overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

The IDMT characteristic is defined by the following formula:

$$t = K/( M - 1)$$

where:

- K= Time multiplier setting
- t = Operating time in seconds
- M = Derived residual voltage setting voltage (***VN> Voltage Set***)

You set this using the ***VN>1 Function*** setting.

Stage 1 also provides a Timer Hold facility.

Stage 2 can have definite time characteristics only. This is set in the ***VN>2 status*** cell

The device derives the residual voltage internally from the three-phase voltage inputs supplied from either a 5-limb VT or three single-phase VTs. These types of VT design provide a path for the residual flux and consequently permit the device to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. Three-limb VTs have no path for residual flux and are therefore unsuitable for this type of protection.

## 12.5.2 RESIDUAL OVERVOLTAGE LOGIC

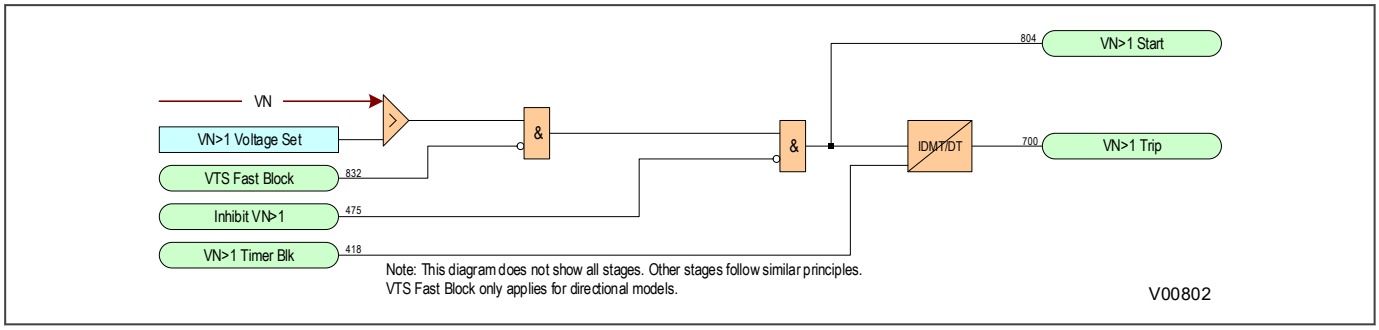



**Figure 214: Residual Overvoltage logic**

The Residual Overvoltage module (VN>) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***VN>(n) Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***VN> (n) Trip*** signal which is used to drive the tripping output relay.

## 12.5.3 APPLICATION NOTES

### 12.5.3.1 CALCULATION FOR SOLIDLY EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

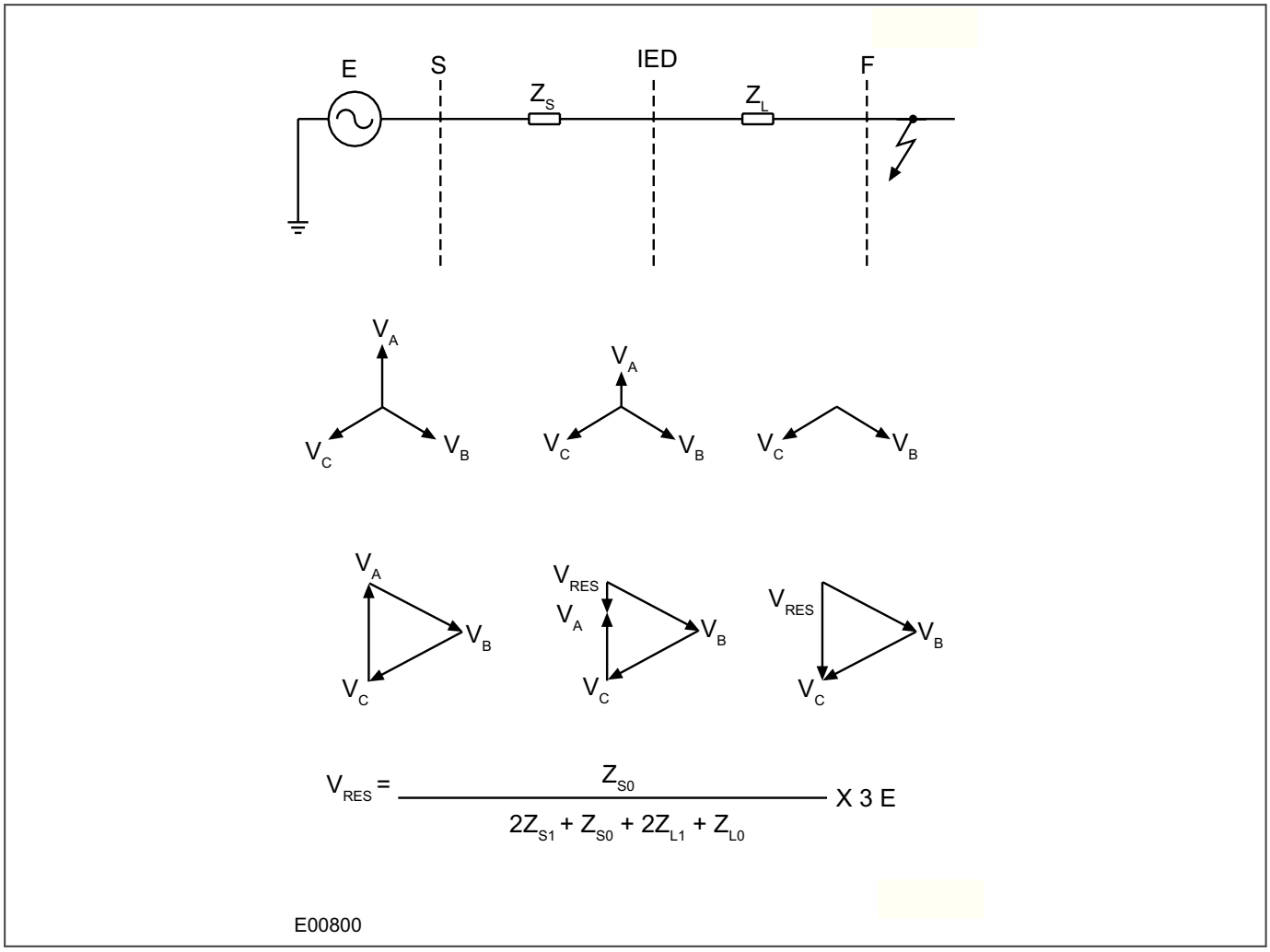



**Figure 215: Residual voltage for a solidly earthed system**

As can be seen from the above diagram, the residual voltage measured on a solidly earthed system is solely dependent on the ratio of source impedance behind the protection to the line impedance in front of the protection, up to the point of fault. For a remote fault far away, the $Z_S/Z_L$: ratio will be small, resulting in a correspondingly small residual voltage. Therefore, the protection only operates for faults up to a certain distance along the system. The maximum distance depends on the device setting.

### 12.5.3.2 CALCULATION FOR IMPEDANCE EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

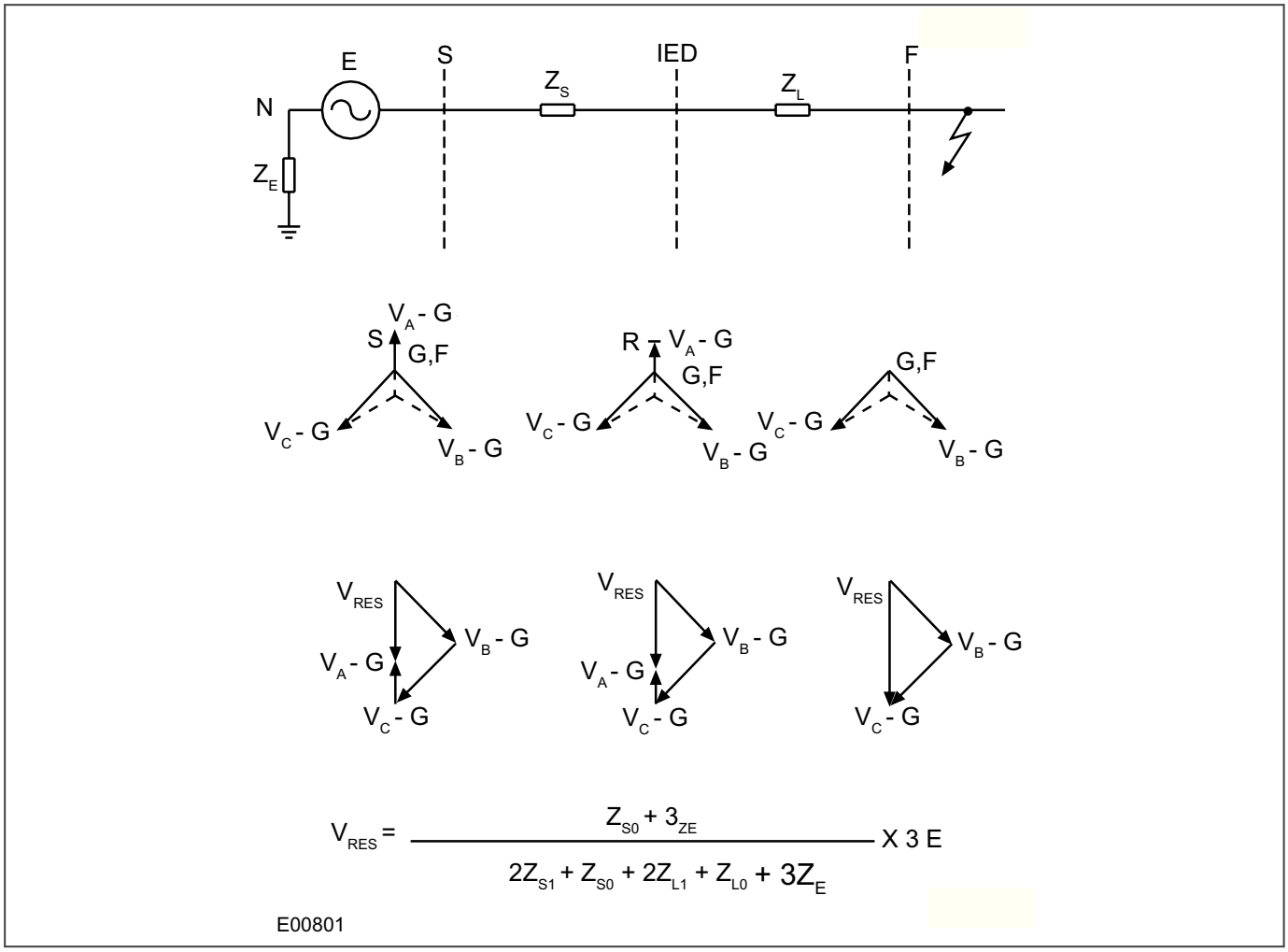



**Figure 216: Residual voltage for an impedance earthed system**

An impedance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

### 12.5.3.3 SETTING GUIDELINES

The voltage setting applied to the elements is dependent on the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependent on the method of system earthing employed.

Also, you must ensure that the protection setting is set above any standing level of residual voltage that is present on the system.

CHAPTER 13

# FREQUENCY PROTECTION FUNCTIONS

## 13.1 CHAPTER OVERVIEW

The device provides a range of frequency protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 335

Frequency Protection 336

Independent R.O.C.O.F Protection 339

## 13.2 FREQUENCY PROTECTION

Power generation and utilisation needs to be well balanced in any industrial, distribution or transmission network. These electrical networks are dynamic entities, with continually varying loads and supplies, which are continually affecting the system frequency. Increased loading reduces the system frequency and generation needs to be increased to maintain the frequency of the supply. Conversely decreased loading increases the system frequency and generation needs to be reduced. Sudden fluctuations in load can cause rapid changes in frequency, which need to be dealt with quickly.

Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse, which has dire consequences.

Normally, generators are rated for a particular band of frequency. Operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken. This type of protection can be used for operator alarms or turbine trips in case of severe frequency decay.

Clearly a range of methods is required to ensure system frequency stability. The frequency protection in this device provides both underfrequency and overfrequency protection.

Frequency Protection is implemented in the *FREQ PROTECTION* column of the relevant settings group.

### 13.2.1 UNDERFREQUENCY PROTECTION

A reduced system frequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the capacity of the generators in that particular subsystem. Industrial plants that are dependent on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

Many types of industrial loads have limited tolerances on the operating frequency and running speeds (e.g. synchronous motors). Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may damage equipment and even lead to blackouts. It is therefore essential to provide protection for underfrequency conditions.

#### 13.2.1.1 UNDERFREQUENCY PROTECTION IMPLEMENTATION

Simple underfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 4 stages of underfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F<1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F<1 Setting***: defines the frequency pickup setting
- ***F<1 Time Delay***: sets the time delay

### 13.2.1.2 UNDERFREQUENCY PROTECTION LOGIC

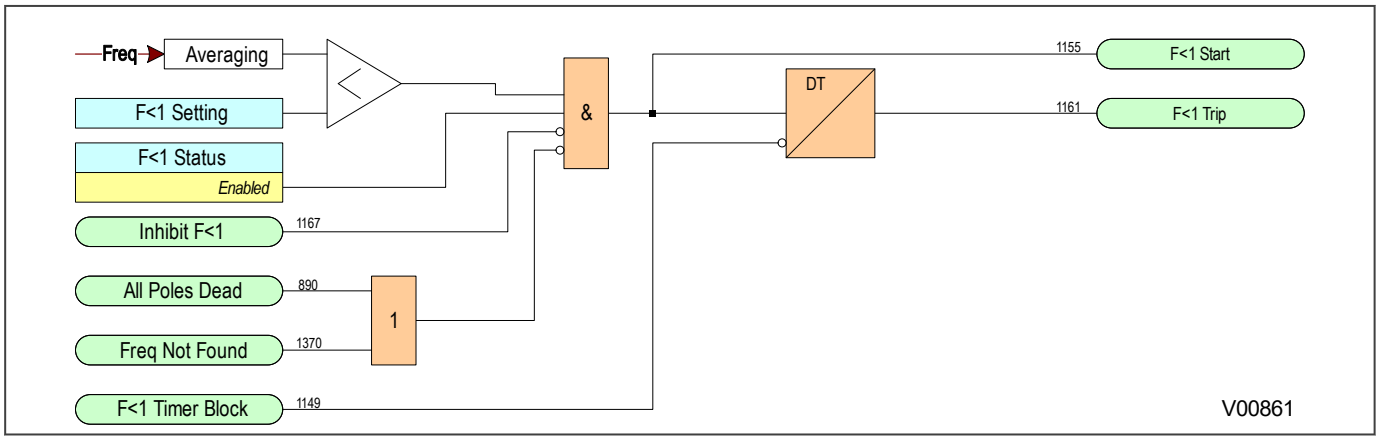



**Figure 217: Underfrequency logic (single stage)**

If the frequency is below the setting and not blocked the DT timer is started. If the frequency cannot be determined, the function is blocked.

### 13.2.1.3 APPLICATION NOTES

#### 13.2.1.3.1 SETTING GUIDELINES

In order to minimise the effects of underfrequency, a multi-stage load shedding scheme may be used with the plant loads prioritised and grouped. During an underfrequency condition, the load groups are disconnected sequentially, with the highest priority group being the last one to be disconnected.

The effectiveness of each load shedding stage depends on the proportion of power deficiency it represents. If the load shedding stage is too small compared with the prevailing generation deficiency, then there may be no improvement in the frequency. This should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. These should not be excessive as this could jeopardize system stability. Time delay settings of 5 - 20 s are typical.

The protection function should be set so that declared frequency-time limits for the generating set are not infringed. Typically, a 10% underfrequency condition should be continuously sustainable.

## 13.2.2 OVERFREQUENCY PROTECTION

An increased system frequency arises when the mechanical power input to a generator exceeds the electrical power output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such conditions, the governor would normally respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Overfrequency protection is required as a backup to cater for cases where the reaction of the control equipment is too slow.

### 13.2.2.1 OVERFREQUENCY PROTECTION IMPLEMENTATION

Simple overfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 2 stages of overfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F>1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F>1 Setting***: defines the frequency pickup setting
- ***F>1 Time Delay***: sets the time delay

### 13.2.2.2 OVERFREQUENCY PROTECTION LOGIC

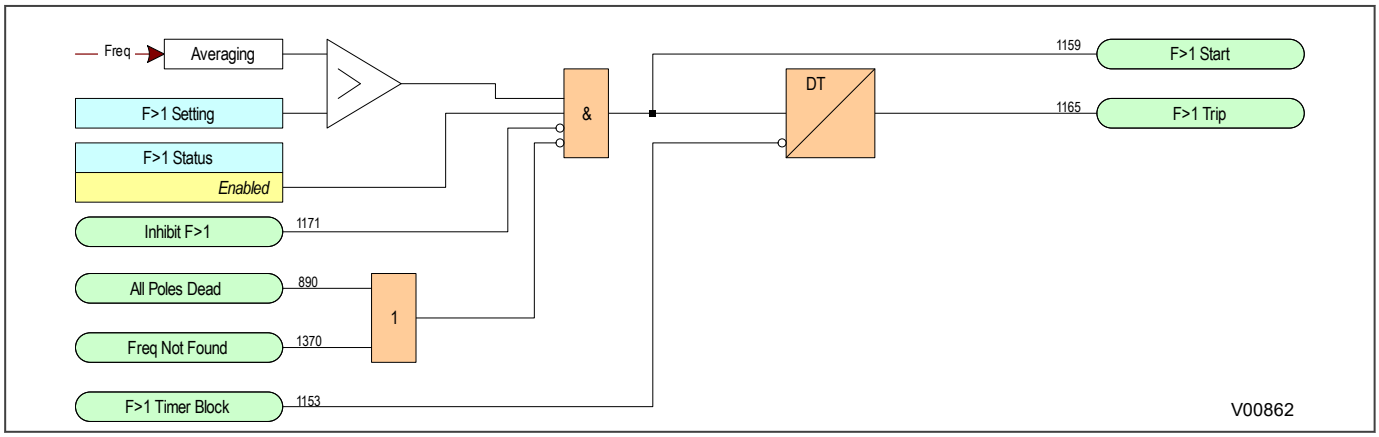



**Figure 218: Overfrequency logic (single stage)**

If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out, the trip is produced. If the frequency cannot be determined, the function is blocked.

### 13.2.2.3 APPLICATION NOTES

#### 13.2.2.3.1 SETTING GUIDELINES

Following changes on the network caused by faults or other operational requirements, it is possible that various subsystems will be formed within the power network. It is likely that these subsystems will suffer from a generation/ load imbalance. The "islands" where generation exceeds the existing load will be subject to overfrequency conditions. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element can be suitably set to sense this contingency.

## 13.3 INDEPENDENT R.O.C.O.F PROTECTION

Where there are very large loads, imbalances may occur that result in rapid decline in system frequency. The situation could be so bad that shedding one or two stages of load is unlikely to stop this rapid frequency decline. In such a situation, standard underfrequency protection will normally have to be supplemented with protection that responds to the rate of change of frequency. An element is therefore required which identifies the high rate of decline of frequency, and adapts the load shedding scheme accordingly.

Such protection can identify frequency variations occurring close to nominal frequency thereby providing early warning of a developing frequency problem. The element can also be used as an alarm to warn operators of unusually high system frequency variations.

### 13.3.1 INDEPENDENT R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides four independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***df/dt Avg.Cycles*** calculates the rate of change of frequency over a fixed period of several cycles.
- ***df/dt>1 Status***: determines whether the stage is for falling or rising frequency conditions
- ***df/dt>1 Setting***: defines the rate of change of frequency pickup setting
- ***df/dt>1 Time***: sets the time delay
- ***df/dt>1 Dir'n***: sets the direction of change you wish to check (positive, negative, or both)

In addition, start, trip and timer block DDB signals are available for each stage, as well as an inhibit signal to inhibit all four stages.

*Note:*
*It is recommended to only use **df/dt** settings <8Hz/s to maintain the claimed performance accuracy for pick-up and operating time, and to ensure the relay is within the frequency operating range, 45-65Hz.*

## 13.3.2 INDEPENDENT R.O.C.O.F PROTECTION LOGIC

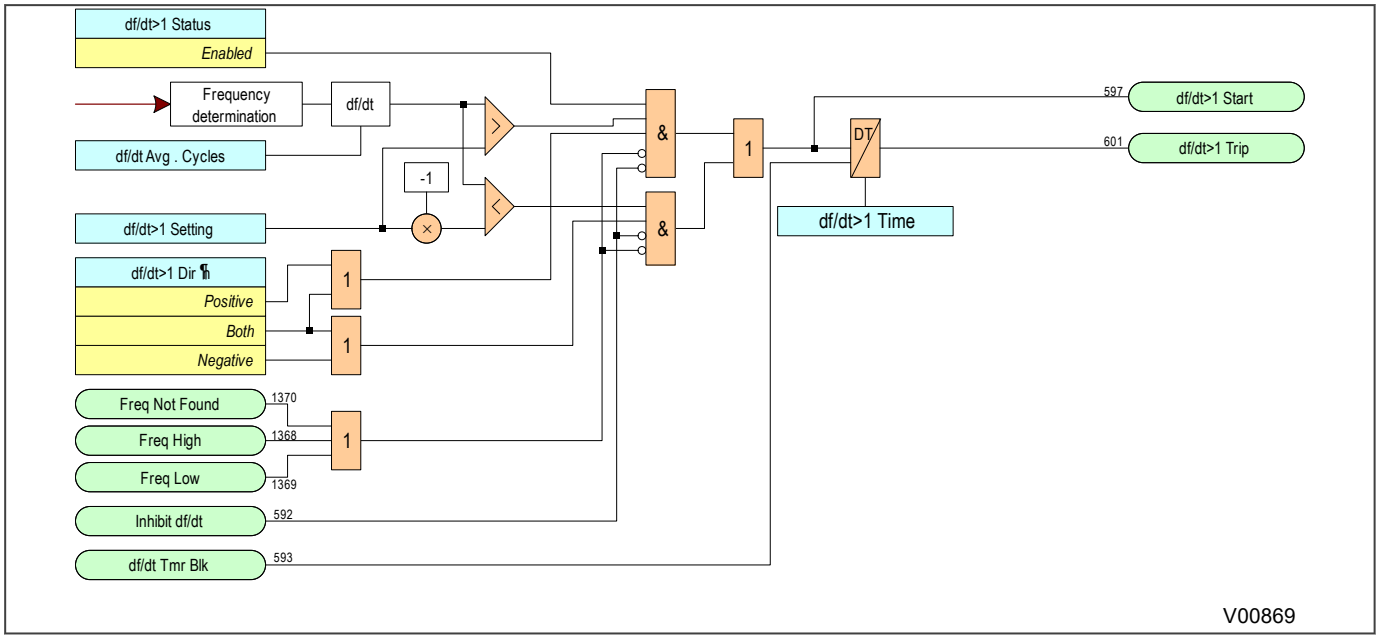



**Figure 219: Rate of change of frequency logic (single stage)**

CHAPTER 14

# POWER PROTECTION FUNCTIONS

## 14.1 CHAPTER OVERVIEW

Power protection is used for protecting generators. Although the main function of this device is for feeder applications, it can also be used as a cost effective alternative for protecting small distributed generators, typically less than 2 MW.

This chapter contains the following sections:

Chapter Overview 342

Overpower Protection 343

Underpower Protection 346

## 14.2 OVERPOWER PROTECTION

With Overpower, we should consider two distinct conditions: Forward Overpower and Reverse Overpower.

A forward overpower condition occurs when the system load becomes excessive. A generator is rated to supply a certain amount of power and if it attempts to supply power to the system greater than its rated capacity, it could be damaged. Therefore overpower protection in the forward direction can be used as an overload indication. It can also be used as back-up protection for failure of governor and control equipment. Generally the Overpower protection element would be set above the maximum power rating of the machine.

A reverse overpower condition occurs if the generator prime mover fails. When this happens, the power system may supply power to the generator, causing it to motor. This reversal of power flow due to loss of prime mover can be very damaging and it is important to be able to detect this with a Reverse Overpower element.

### 14.2.1 OVERPOWER PROTECTION IMPLEMENTATION

Overpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group.

The Power Protection elements provide 4 stages of directional power for both active and reactive power, any of which can be configured as Overpower by selecting the `Over` value in the ***Power1 Function*** (or other stage) setting. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power and single phase power measurements (based on A, B and/or C phases) as the energising quantities. A Start condition occurs when two consecutive measurements exceed the setting threshold. A trip condition occurs if the Start condition is present for the set time delay. This can be inhibited by the VTS Slow Block and Pole Dead logic if desired.

The Start and Trip timer resets if the power falls below the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

## 14.2.2 OVERPOWER LOGIC

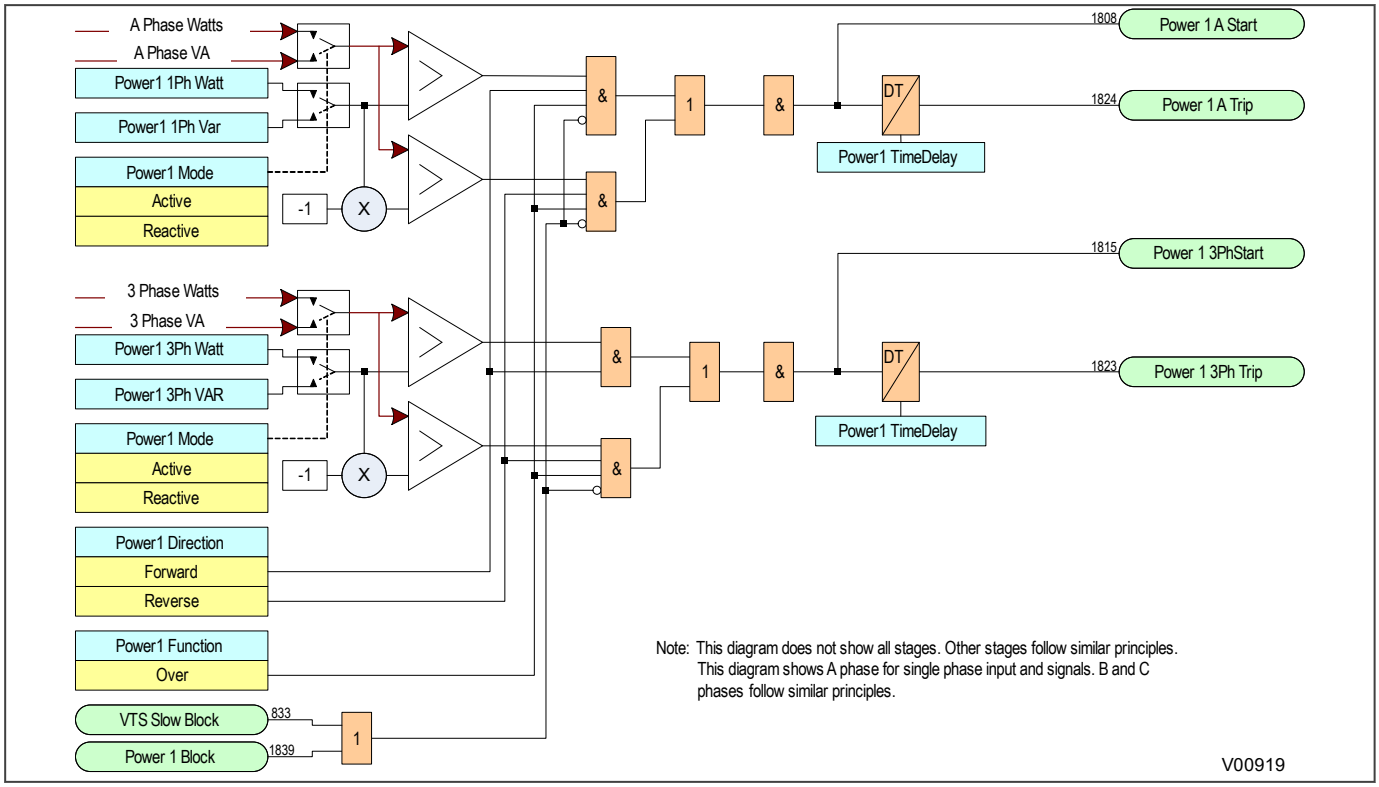



**Figure 220: Overpower logic**

## 14.2.3 APPLICATION NOTES

### 14.2.3.1 FORWARD OVERPOWER SETTING GUIDELINES

The relevant power threshold settings should be set greater than the full load rated power.

The operating mode should be set to Forward.

A time delay setting, ***Power1 TimeDelay*** (or other stage) should be applied. This setting is dependant on the application. The delay on the reset timer, ***Power1 tRESET*** (or other stage) setting, would normally be set to zero.

### 14.2.3.2 REVERSE POWER CONSIDERATIONS

A generator is expected to supply power to the connected system in normal operation. If the generator prime mover fails, it will begin to take motoring power from the power system (if the power system to which it is connected has other generating sources). The consequences of this reversal of power and the level of power drawn from the power system will be dependent on the type of prime mover.

Typical levels of motoring power and possible motoring damage that could occur for various types of generating plant are given in the following table.

| Prime Mover | Motoring Power | Possible Damage (Percentage Rating) |
|---|---|---|
| Diesel Engine | 5% - 25% | Risk of fire or explosion from unburned fuel |
| Motoring level depends on compression ratio and cylinder bore stiffness. Rapid disconnection is required to limit power loss and risk of damage. | | |
| Gas Turbine | 10% - 15% (Split-shaft)<br>>50% (Single-shaft) | With some gear-driven sets, damage may arise due to reverse torque on gear teeth. |

| Prime Mover | Motoring Power | Possible Damage (Percentage Rating) |
|---|---|---|
| Compressor load on single shaft machines leads to a high motoring power compared to split-shaft machines. Rapid disconnection is required to limit power loss or damage. | | |
| Hydraulic Turbines | 0.2 - >2% (Blades out of water)<br>>2.0% (Blades in water) | Blade and runner damage may occur with a long period of motoring |
| Power is low when blades are above tail-race water level. Hydraulic flow detection devices are often the main means of detecting loss of drive. Automatic disconnection is recommended for unattended operation. | | |
| Steam Turbines | 0.5% - 3% (Condensing sets)<br>3% - 6% (Non-condensing sets) | Thermal stress damage may be inflicted on low-pressure turbine blades when steam flow is not available to dissipate losses due to air resistance. |
| Damage may occur rapidly with non-condensing sets or when vacuum is lost with condensing sets. Reverse power protection may be used as a secondary method of detection and might only be used to raise an alarm. | | |

In some applications, the level of reverse power in the case of prime mover failure may fluctuate. This may be the case for a failed diesel engine. To prevent cyclic initiation and reset of the main trip timer, an adjustable reset time delay is provided. You will need to set this time delay longer than the period for which the reverse power could fall below the power setting. This setting needs to be taken into account when setting the main trip time delay.

*Note:*
*A delay in excess of half the period of any system power swings could result in operation of the reverse power protection during swings.*

### 14.2.3.3 REVERSE OVERPOWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a reverse power stage by setting the ***Power1 Direction*** (or other stage) cell to `Reverse`.

The relevant power threshold settings should be set to less than 50% of the motoring power.

The operating mode should be set to Reverse.

The reverse power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation.

A time delay setting, of approximately 5 s would be typically applied.

The delay on the reset timer, ***Power1 tRESET*** (or other stage), would normally be set to zero.

When settings of greater than zero are used for the reset time delay, the pick-up time delay setting may need to be increased to ensure that false tripping does not result in the event of a stable power swinging event.

Reverse overpower protection can also be used for loss of mains applications. If the distributed generator is connected to the grid but not allowed to export power to the grid, it is possible to use reverse power detection to switch off the generator. In this case, the threshold setting should be set to a sensitive value, typically less than 2% of the rated power. It should also be time-delayed to prevent false trips or alarms being given during power system disturbances, or following synchronisation. A typical time delay is 5 seconds.

## 14.3 UNDERPOWER PROTECTION

Although the Underpower protection is directional and can be configured as forward or reverse, the most common application is for Low Forward Power protection.

When a machine is generating and the circuit breaker connecting the generator to the system is tripped, the electrical load on the generator is cut off. This could lead to overspeeding of the generator if the mechanical input power is not reduced quickly. Large turbo-alternators, with low-inertia rotor designs, do not have a high over speed tolerance. Trapped steam in a turbine, downstream of a valve that has just closed, can rapidly lead to over speed. To reduce the risk of over speed damage, it may be desirable to interlock tripping of the circuit breaker and the mechanical input with a low forward power check. This ensures that the generator circuit breaker is opened only after the mechanical input to the prime mover has been removed, and the output power has reduced enough such that overspeeding is unlikely. This delay in tripping the circuit breaker may be acceptable for non-urgent protection trips (e.g. stator earth fault protection for a high impedance earthed generator). For urgent trips however (e.g. stator current differential protection), this Low Forward Power interlock should not be used.

### 14.3.1 UNDERPOWER PROTECTION IMPLEMENTATION

Underpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group..

The Power Protection element provides 4 stages of directional power for both active and reactive power, any of which can be configured as Underpower by selecting the `Under` value in the ***Power1 Function*** (or other stage) setting. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power or single phase power measurements (based on A, B or/and or C phases) as the energising quantity. A start condition occurs when two consecutive measurements fall below the setting threshold. A trip condition occurs if the start condition is present for the set trip time. This can be inhibited by the VTS slow block and pole dead logic if desired.

The Start and Trip timer resets if the power exceeds the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

## 14.3.2 UNDERPOWER LOGIC

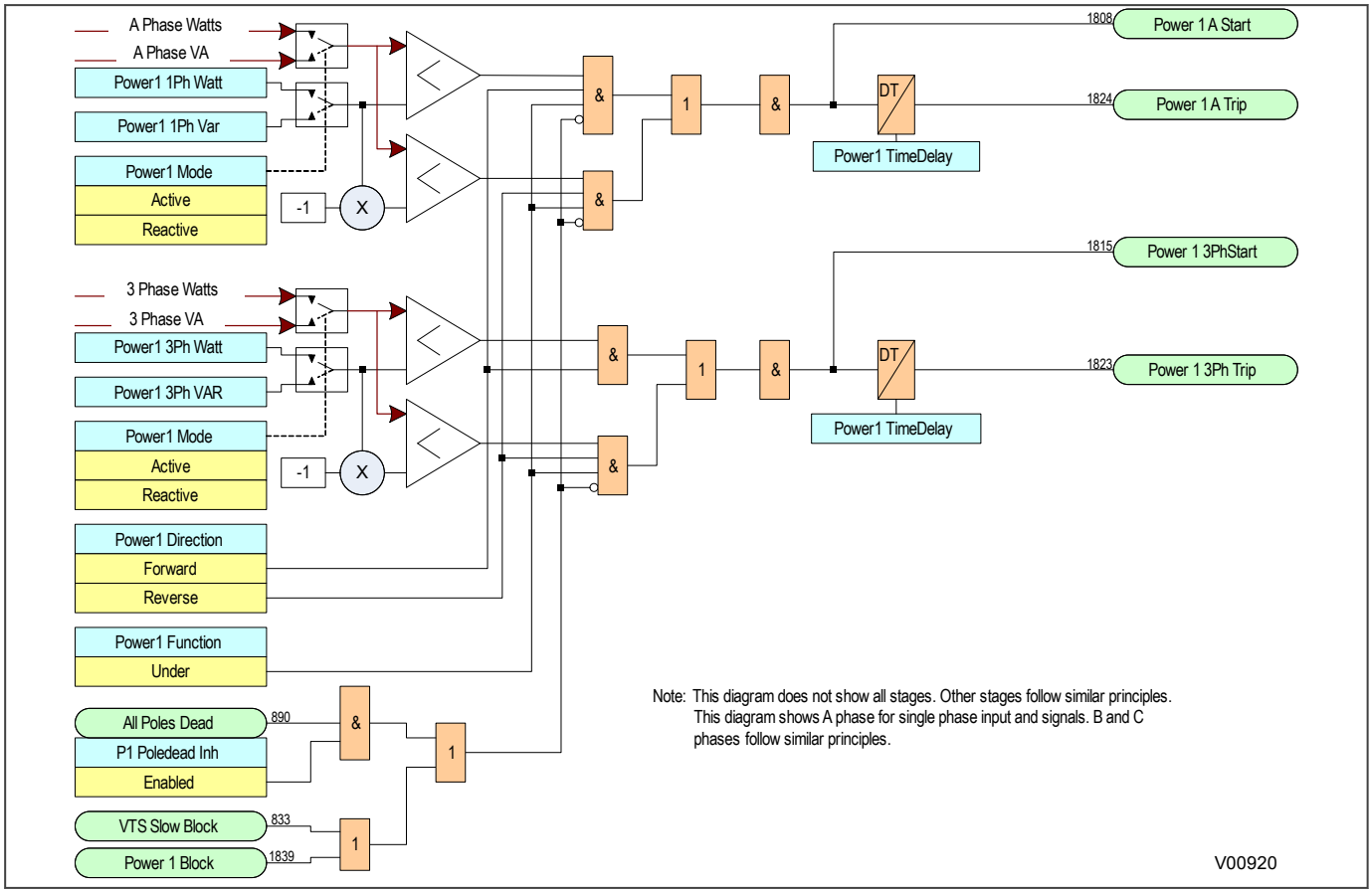



**Figure 221: Underpower logic**

## 14.3.3 APPLICATION NOTES

### 14.3.3.1 LOW FORWARD POWER CONSIDERATIONS

The Low Forward Power protection can be arranged to interlock 'non-urgent' protection tripping using the Flexlogic Equation Editor. It can also be arranged to provide a contact for external interlocking of manual tripping. To prevent unwanted alarms and flags, a Low Forward Power protection element can be disabled when the circuit breaker is opened via Pole Dead logic.

The Low Forward Power protection can also be used to provide loss of load protection when a machine is motoring. It can be used for example to protect a machine which is pumping from becoming unprimed, or to stop a motor in the event of a failure in the mechanical transmission.

A typical application would be for pump storage generators operating in the motoring mode, where there is a need to prevent the machine becoming unprimed which can cause blade and runner damage. During motoring conditions, it is typical for the protection to switch to another setting group with the low forward power enabled and correctly set and the protection operating mode set to `Reverse`.

A low forward power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

### 14.3.3.2 LOW FORWARD POWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a forward power stage by setting the ***Power1 Direction*** (or other stage) cell to `Forward`.

When required for interlocking of non-urgent tripping applications, the threshold setting of the low forward power protection function should be less than 50% of the power level that could result in a dangerous overspeed condition on loss of electrical loading.

When required for loss of load applications, the threshold setting of the low forward power protection function, is system dependent, however, it is typically set to 10 - 20% below the minimum load. The operating mode should be set to operate for the direction of the load current, which would typically be reverse for a pump storage machine application where *Forward* is the Generating direction and *Reverse* is the motoring direction.

For interlocking non-urgent trip applications the time delay associated with the low forward power protection function could be set to zero. However, some delay is desirable so that permission for a non-urgent electrical trip is not given in the event of power fluctuations arising from sudden steam valve/throttle closure. A typical time delay is 2 seconds.

For loss of load applications the pick-up time delay is application dependent but is normally set in excess of the time between motor starting and the load being established. Where rated power cannot be reached during starting (for example where the motor is started with no load connected) and the required protection operating time is less than the time for load to be established then it will be necessary to inhibit the power protection during this period. This can be done in the PSL using AND logic and a pulse timer triggered from the motor starting to block the power protection for the required time.

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse power protection function, should be set to a sensitive value, typically <2% of the rated power.

The low forward power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation. A time delay setting, of 5 s should be applied typically.

The delay on the reset timers would normally be set to zero.

To prevent unwanted alarms and flags, the protection element can be disabled when the circuit breaker is open via Pole Dead logic.

#### 14.3.3.3 REACTIVE POWER PROTECTION

Some applications provide underexcitation protection using negative reactive power elements. This is popular for synchronous motors and small generators.

A reverse reactive power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

##### Setting guidelines

Each stage of power protection can be selected to operate as a reverse reactive power stage by selecting the ***Power1 Function*** (or other stage) cell to *Over* and the ***Power1 Direction*** (or other stage) cell to *Reverse*.

The power threshold setting of the negative reactance power protection, ***Power1 3Ph VAr*** or ***Power1 1Ph VAr*** (or other stage) should be set to supervise the steady state and dynamic stability limits for under excitation protection. The following figure shows an example of the typical settings, Q1 and Q2.

The disadvantage of this method is that the measurement is not very sensitive during low voltage operation of the generator. The reactive power elements can be blocked in the PSL from an undervoltage start signal if this is a problem. This method is less secure than the impedance method and so is often used just to alarm.

If the static limit characteristic Q1 is exceeded, the voltage regulator must first have the opportunity of increasing the excitation. For this reason, a time delayed trip of typically 5-10s is used ***Power1 TimeDelay*** (or other stage). A shorter delay of 0.5s can be used for Q2.

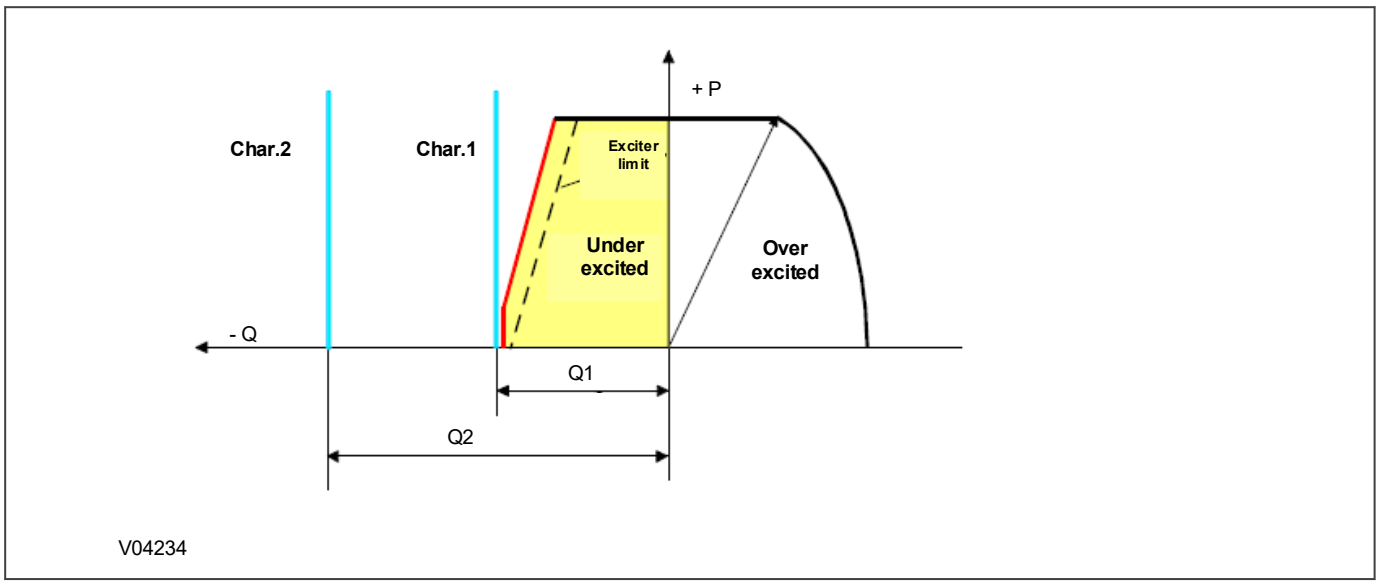



**Figure 222: Reactive power protection for underexcitation protection**

$Q1 = VN^2/Xd$

$Q2 > = 2\ VN^2/Xd$

Where:

VN = Machine nominal voltage

Xd = Generator direct-axis synchronous reactance in ohms

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse reactive power protection function, ***Power1 3Ph VAr*** or ***Power1 1Ph VAr*** (or other stage), should be set to a suitable value, typically <2% of the rated reactive power. The reverse reactive power protection function should be time-delayed, to prevent false trips or alarms being given during power system disturbances or following synchronization, a typical time delay is 5 s.

CHAPTER 15

# CB FAIL PROTECTION

## 15.1 CHAPTER OVERVIEW

The device provides a Circuit Breaker Fail Protection function. This chapter describes the operation of this function including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 351
Circuit Breaker Fail Protection 352
Circuit Breaker Fail Implementation 353
Circuit Breaker Fail Logic 355
Application Notes 359

## 15.2 CIRCUIT BREAKER FAIL PROTECTION

When a fault occurs, one or more protection devices will operate and issue a trip command to the relevant circuit breakers. Operation of the circuit breaker is essential to isolate the fault and prevent, or at least limit, damage to the power system. For transmission and sub-transmission systems, slow fault clearance can also threaten system stability.

For these reasons, it is common practice to install Circuit Breaker Failure protection (CBF). CBF protection monitors the circuit breaker and establishes whether it has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, the CBF protection will operate, whereby the upstream circuit breakers are back-tripped to ensure that the fault is isolated.

CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

# 15.3 CIRCUIT BREAKER FAIL IMPLEMENTATION

Circuit Breaker Failure Protection is implemented in the *CB FAIL & P.DEAD* column of the relevant settings group.

## 15.3.1 CIRCUIT BREAKER FAIL TIMERS

The circuit breaker failure protection incorporates two timers, ***CB Fail 1 Timer*** and ***CB Fail 2 Timer***, allowing configuration for the following scenarios:

- Simple CBF, where only ***CB Fail 1 Timer*** is enabled. For any protection trip, the **CB Fail 1** ***Timer*** is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, the CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to back-trip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A retripping scheme, plus delayed back-tripping. Here, ***CB Fail 1 Timer*** is used to issue a trip command to a second trip circuit of the same circuit breaker. This requires the circuit breaker to have duplicate circuit breaker trip coils. This mechanism is known as retripping. If retripping fails to open the circuit breaker, a back-trip may be issued following an additional time delay. The back-trip uses ***CB Fail 2 Timer***, which was also started at the instant of the initial protection element trip.

You can configure the CBF elements ***CB Fail 1 Timer*** and ***CBF Fail 2 Timer*** to operate for trips triggered by protection elements within the device. Alternatively you can use an external protection trip by allocating one of the opto-inputs to the ***External Trip*** DDB signal in the PSL.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***NonIProt Rst*** and ***Ext Prot Rst***.

The resetting options are summarised in the following table:

| Initiation (Menu Selectable) | CB Fail Timer Reset Mechanism |
|---|---|
| Current based protection (e.g.50/51/46/21/87) | IA< operates AND IB< operates AND IC< operates AND IN< operates or through Ext Rst DDB in PSL |
| Sensitive Earth Fault element | ISEF< Operates or Ext Rst SEF DDB |
| Non-current based protection (e.g. 27/59/81/32L) | Three options are available:<br>• All I< and IN< elements operate or Ext Rst CBF DDB<br>• Protection element reset AND (all I< and IN< elements operate or Ext Rst DDB<br>• CB open (all 3 poles) AND all I< and IN< elements operate |
| External protection | Three options are available.<br>• All I< and IN< elements operate<br>• External trip reset AND all I< and IN< elements operate<br>• CB open (all 3 poles) AND all I< and IN< elements operate |

## 15.3.2 ZERO CROSSING DETECTION

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is to its saturation point, the higher the subsidence current.

The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the protection clears the fault, the CB Fail function should reset fast to avoid maloperation due to the subsidence current. To compensate for this the device includes a zero-crossing detection algorithm, which ensures that the CB Fail re-trip and back-trip signals are not asserted while subsidence current is flowing. If all the samples within half a cycle are greater than or smaller than 0 A (10 mS for a 50 Hz system), then zero crossing detection is asserted, thereby blocking the operation of the CB Fail function. The zero-crossing detection algorithm is used after

the circuit breaker in the primary system has opened ensuring that the only current flowing in the AC secondary circuit is the subsidence current.

# 15.4 CIRCUIT BREAKER FAIL LOGIC

## 15.4.1 CIRCUIT BREAKER FAIL LOGIC - PART 1

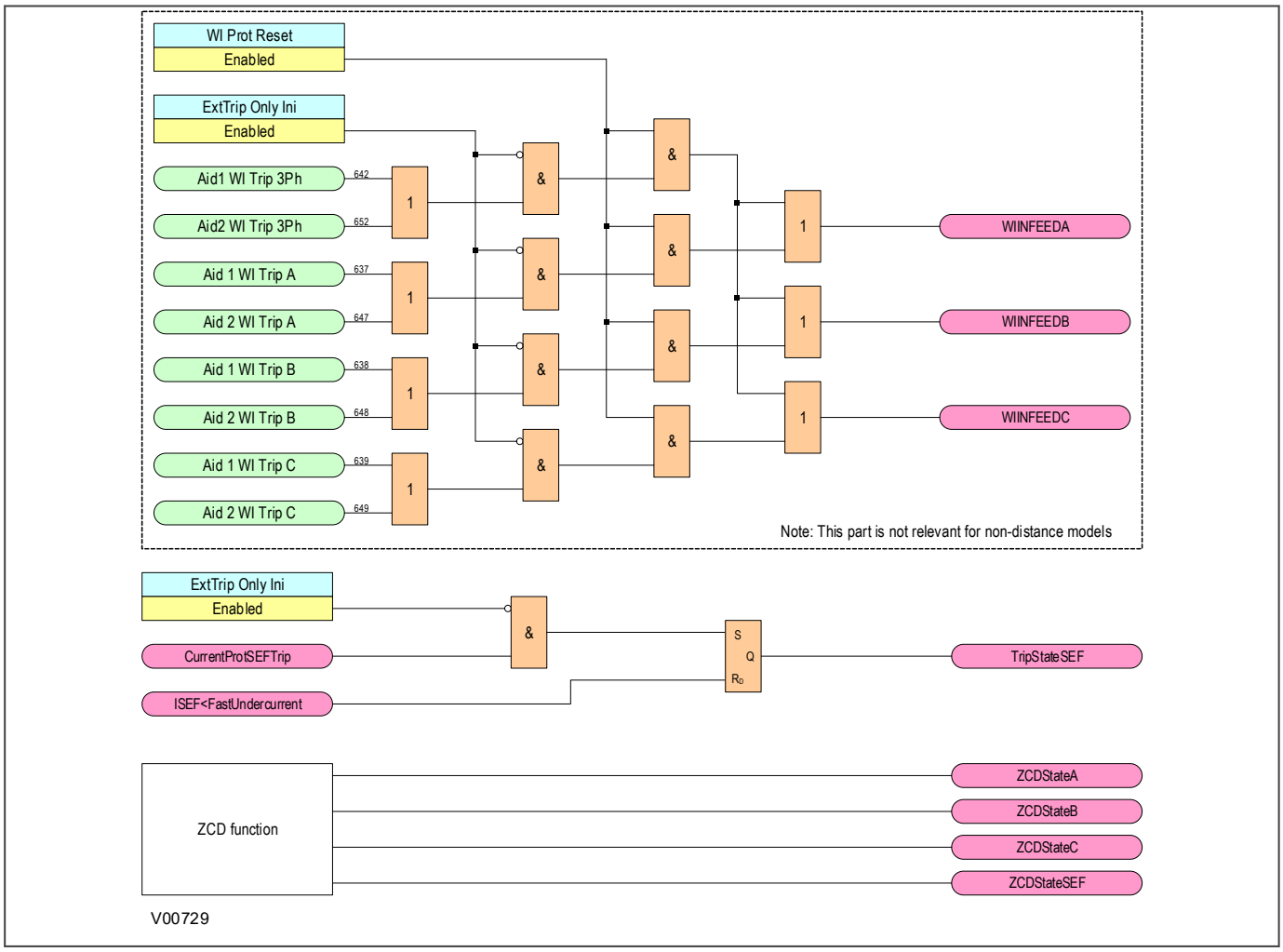



**Figure 223: Circuit Breaker Fail logic - part 1**

## 15.4.2 CIRCUIT BREAKER FAIL LOGIC - PART 2

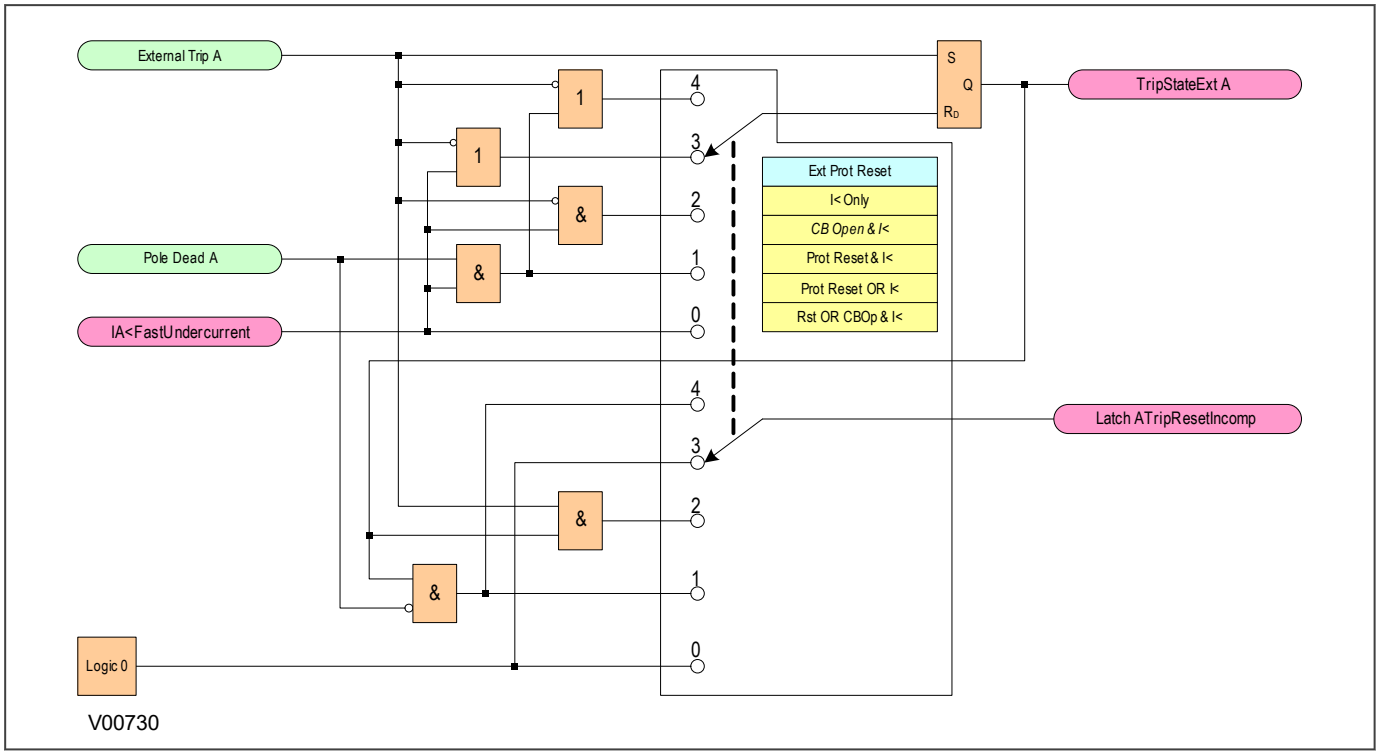



**Figure 224: Circuit Breaker Fail logic - part 2**

*Note:*
*This diagram shows only phase-A for a single-CB device. The diagrams for phases B and C follow the same principle and are not repeated here.*

## 15.4.3 CIRCUIT BREAKER FAIL LOGIC - PART 3

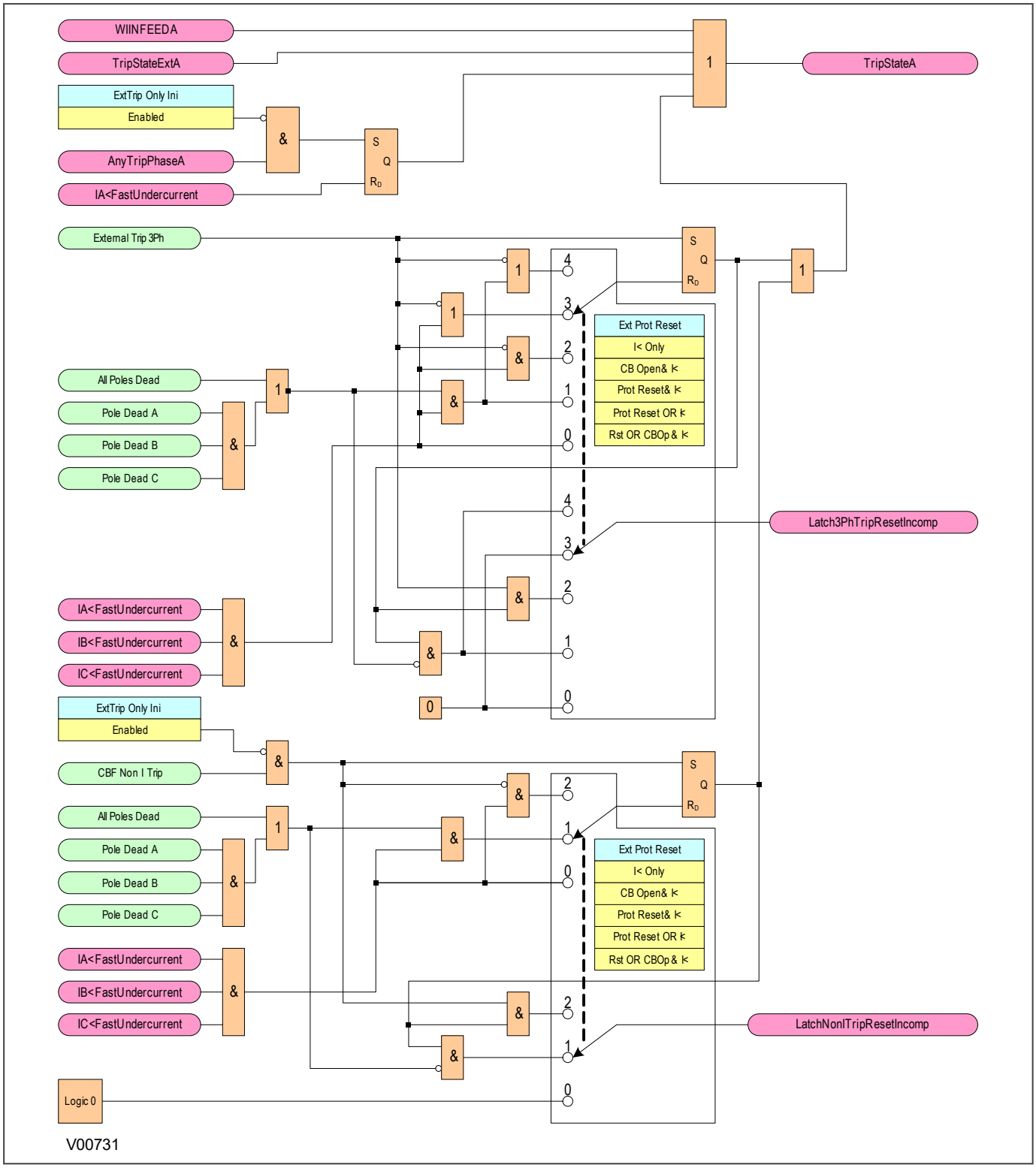



**Figure 225: Circuit Breaker Fail logic - part 3**

## 15.4.4 CIRCUIT BREAKER FAIL LOGIC - PART 4

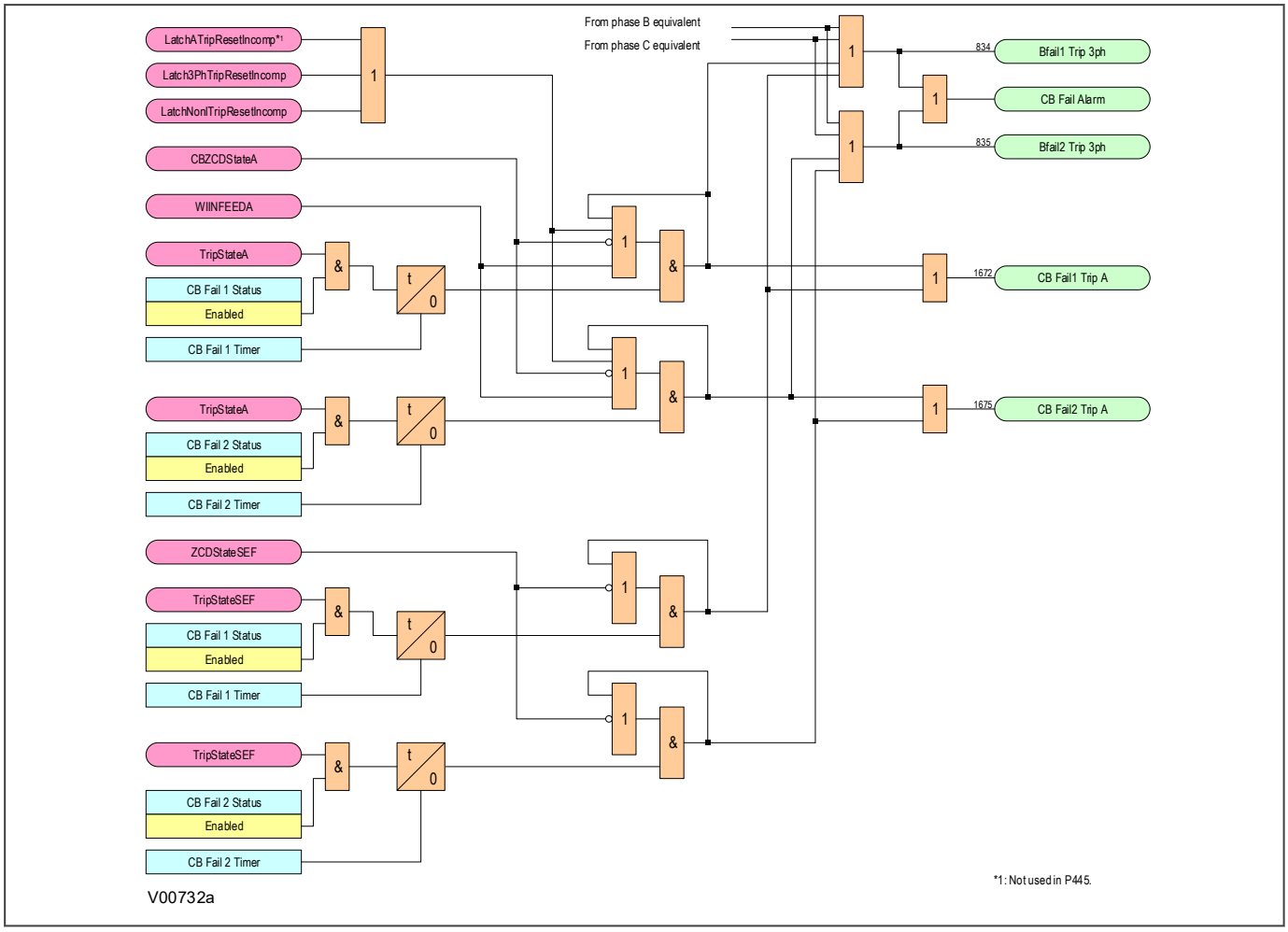



**Figure 226: Circuit Breaker Fail logic - part 4**

*Note:*
*This diagram shows only phase-A for a single-CB device. The diagrams for phases B and C follow the same principle and are not repeated here.*

# 15.5 APPLICATION NOTES

## 15.5.1 RESET MECHANISMS FOR CB FAIL TIMERS

It is common practise to use low set undercurrent elements to indicate that circuit breaker poles have interrupted the fault or load current. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the device uses operation of undercurrent elements to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting CBF in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. In this case, detecting drop-off of the initiating protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

## 15.5.2 SETTING GUIDELINES (CB FAIL TIMER)

The following timing chart shows the CB Fail timing during normal and CB Fail operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CB Fail back-up trip time delay considers the maximum CB clearing time, the CB Fail reset time plus a safety margin. Typical CB clearing times are 1.5 or 3 cycles. The CB Fail reset time should be short enough to avoid CB Fail back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CB Fail to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit.

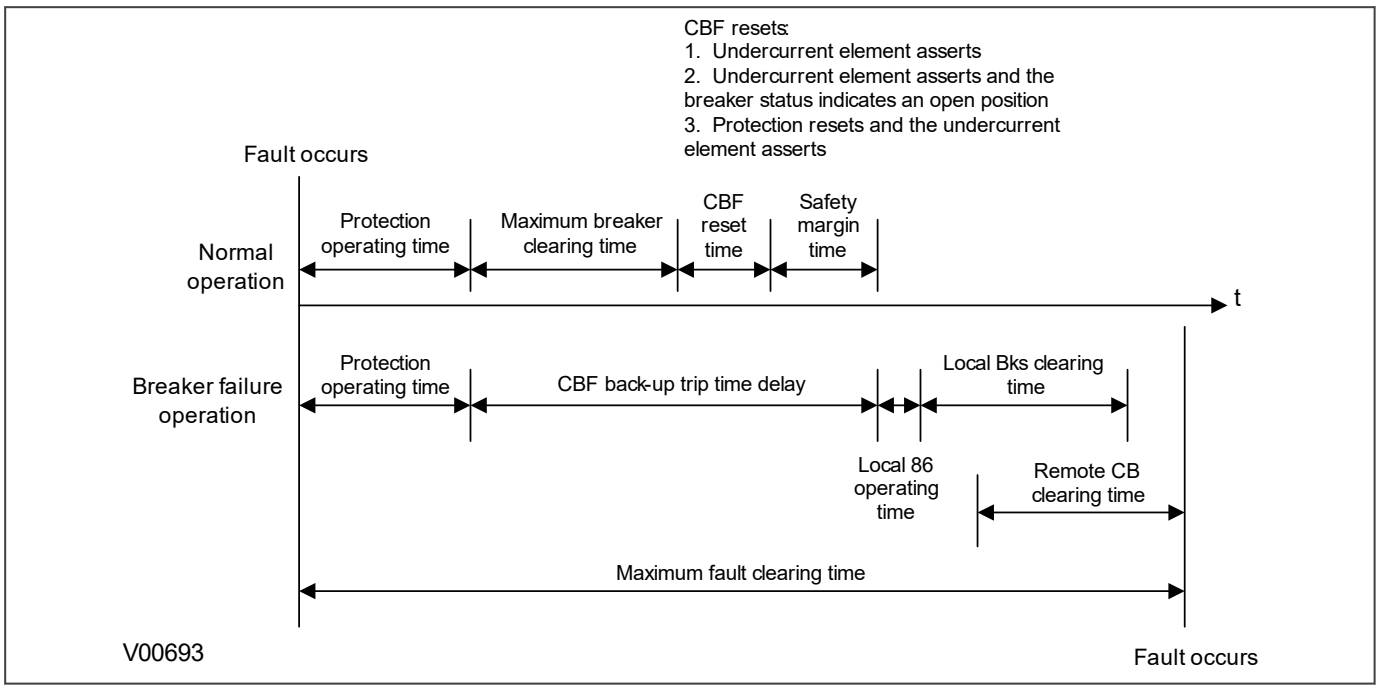



**Figure 227: CB Fail timing**

The following examples consider direct tripping of a 2-cycle circuit breaker. Typical timer settings to use are as follows:

| CB Fail Reset Mechanism | tBF Time Delay | Typical Delay For 2 Cycle Circuit Breaker |
|---|---|---|
| Initiating element reset | CB interrupting time + element reset time (max.) + error in tBF timer + safety margin | 50 + 50 + 10 + 50 = 160 ms |
| CB open | CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin | 50 + 10 + 50 = 110 ms |
| Undercurrent elements | CB interrupting time + undercurrent element (max.) + safety margin operating time | 50 + 25 + 50 = 125 ms |

*Note:*
*All CB Fail resetting involves the operation of the undercurrent elements. Where element resetting or CB open resetting is used, the undercurrent time setting should still be used if this proves to be the worst case.*
*Where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.*

## 15.5.3 SETTING GUIDELINES (UNDERCURRENT)

The phase undercurrent settings (I<) must be set less than load current to ensure that I< operation correctly indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20%In. Settings of 5% of In are common for generator CB Fail.

The earth fault undercurrent elements must be set less than the respective trip. For example:

$$IN< = (IN> \text{ trip})/2$$

# CHAPTER 16

# CURRENT TRANSFORMER REQUIREMENTS

## 16.1 CHAPTER OVERVIEW

This chapter contains the following sections:

Chapter Overview 362
Recommended CT Classes 363
Distance Protection Requirements 364
Determining Vk for IEEE C-class CT 365
Worked Examples 366

## 16.2 RECOMMENDED CT CLASSES

You can use Class X current transformers with a knee point voltage greater or equal to that calculated. You can also use class 5P protection CT. These have a knee-point voltage equivalent, which can be approximated from the following calculations:

$$V_k = (VA \times ALF)/I_n + (R_{CT} \times ALF \times I_n)$$

where:

- $V_k$ = Knee-point voltage
- VA = Voltampere burden rating
- ALF = Accuracy limit factor
- $I_n$ = CT nominal secondary current
- $R_{CT}$ = CT resistance

## 16.3 DISTANCE PROTECTION REQUIREMENTS

### Zone 1 Reach Point Accuracy (RPA)

$$V_k \geq K_{RPA\ x}\ I_{fZ1\ x}\ (1+ X/R)(R_{CT} + R_L)$$

where:

- $V_k$ = Required CT knee point voltage (volts)
- $I_{fZ1}$ = Maximum secondary phase fault current at Zone 1 reach point (A)
- X/R = Primary system reactance/resistance ratio
- $R_{CT}$ = CT secondary winding resistance
- $R_L$ = Single lead resistance from CT to IED
- $K_{RPA}$ = Fixed dimensioning factor:
  - = 0.6 for all overhead line applications, or where sub-cycle tripping times are required for Zone 1 element
  - = 0.35 for power cable applications, where sub-cycle tripping times are not required for Zone 1 element

### Zone 1 Close-up Fault Operation

An additional calculation must be performed for all cables and lines where the source impedance ratio (SIR) may be less than SIR = 2.

$$V_k \geq K_{max\ x}\ I_{fmax\ x}\ (R_{CT} + R_L)$$

where:

$K_{max}$ = Fixed dimensioning factor = 1.4

$I_{fmax}$ = Maximum secondary phase fault current

Then, the highest of the two calculated knee points must be used.

*Note:*
*It is not necessary to repeat the calculation for earth faults, as the phase reach calculation is the worst-case for CT dimensioning.*

## 16.4 DETERMINING VK FOR IEEE C-CLASS CT

Where IEEE standards are used to specify CTs, the C class voltage rating can be checked to determine the equivalent $V_k$ (knee point voltage according to IEC).

The equivalence formula is:

$$V_k = 1.05(\text{C rating in volts}) + 100R_{CT}$$

## 16.5 WORKED EXAMPLES

The power system and the line parameters used in these examples are as follows:

- Single circuit operation between Green Valley and Blue River
- System voltage = 230 kV
- System frequency = 50 Hz
- System grounding = solid
- CT ratio = 1200/1
- Line length = 100 km
- Line positive sequence impedance Z1 = 0.089 + j 0.476 ohm per km
- Bus fault level = 40 kA
- Primary time constant = 120 ms

**Important notes to be considered**

- For calculating the CT requirements, the bus bar short time symmetrical fault rating should be considered as the bus fault level.
- If only indicative X/R ratios are available, the circuit breaker's DC breaking capacity is used to derive the primary time constant and therefore the primary system X/R. It is derived from the circuit breaker manufacturer's practical primary time constants. These vary between 50 ms (66 kV and 132 kV breakers) and 120 ms (220 kV and 400 kV breakers). 150 ms is a practical figure for generator circuit breakers.
- Distance Zone1 reach point case: Both If and X/R are to be calculated for a fault at Zone1 reach point

### 16.5.1 CALCULATION OF PRIMARY X/R RATIO

Primary X/R up to the Green Valley busbar:

$= 2\pi f \times \text{primary time constant}$

$= 2\pi \times 50 \times 0.12 = 37.7$

### 16.5.2 CALCULATION OF SOURCE IMPEDANCE

Source impedance magnitude:

$= 230\ \text{kV}/(1.732 \times 40\ \text{kA}) = 3.32\ \text{ohms}$

Source angle:

$= \tan^{-1}(37.7) = 88.48°$

Hence:

$Zs = 0.088 + j3.317$

### 16.5.3 CALCULATION OF FULL LINE IMPEDANCE

Z1:

$= 0.089 + j0.476\ \text{ohms/km}$

$Z_L$:

$= 8.9 + j47.6 = 48.42\ \text{ohms angle}\ 79.4°$

### 16.5.4 CALCULATION OF TOTAL IMPEDANCE UP TO REMOTE BUSBAR

$Z_T = Z_S + Z_L$:

= 8.988+ j50.917 ohms =51.7 ohms angle 80°

### 16.5.5 CALCULATION OF THROUGH FAULT X/R RATIO

$X/R_{\text{through}} = 50.917/8.988 = 5.66$

### 16.5.6 CALCULATION OF THROUGH FAULT CURRENT

$I_{f\,\text{through}} = 230\text{kV}/(1.732 \times 51.7) = 2568.5$ A primary = 2.14 A secondary

### 16.5.7 CALCULATION OF LINE IMPEDANCE TO ZONE 1 REACH POINT

$Z_{\text{zone 1}} = 0.8ZL = 7.12 + j\,38.08 = 38.73$ ohms angle 79.4°

### 16.5.8 CALCULATION OF TOTAL IMPEDANCE TO ZONE 1 REACH POINT

$Z_{T\,\text{zone 1}} = Z_S + Z\ \text{zone 1} = 7.208 + j\,41.397 = 42.019$ ohms angle 80°

### 16.5.9 CALCULATION OF X/R TO ZONE 1 REACH POINT

$X/R_{\text{zone 1}} = 41.397/7.208 = 5.74$

### 16.5.10 CALCULATION OF FAULT CURRENT TO ZONE 1 REACH POINT

$I_{f\,\text{zone 1}} = 230\text{kV}/(1.732 \times 42.019) = 3160.34$ A primary = 2.63 A secondary

### 16.5.11 CALCULATION OF VK FOR DISTANCE ZONE 1 REACH POINT

Using: $V_k \geq K_{RPA} \times I_{fZ1} \times (1+ X/R)(R_{CT} + R_L)$

$V_k > 0.6 \times 2.63 \times (1 + 5.74)(R_{CT} + R_L)$, therefore:

$V_k > 10.65(R_{CT} + R_L)$

### 16.5.12 CALCULATION OF VK FOR DISTANCE ZONE 1 CLOSE-UP FAULT

SIR = $Z_s/Z_{zone1}$ =3.32/38.73, which is less than 2, so we need to calculate Vk.

Close-up fault current = 40kA primary, = 33.33A secondary

$V_k \geq K_{max} \times I_{fmax} \times (R_{CT} + R_L)$

$V_k > 1.4 \times 33.3 \times (R_{CT} + R_L)$, therefore:

$V_k > 46.67(R_{CT} + R_L)$

### 16.5.13 CALCULATION OF VK FOR DISTANCE TIME DELAYED ZONES

$V_k > I_f(R_{CT} + R_L)$

$V_k > I_{fthrough} \times (R_{CT} + R_L)$, therefore:

$V_k > 2.14(R_{CT} + R_L)$

CHAPTER 17

# MONITORING AND CONTROL

## 17.1 CHAPTER OVERVIEW

As well as providing a range of protection functions, the product includes comprehensive monitoring and control functionality.

This chapter contains the following sections:

Chapter Overview 369
Event Records 370
Disturbance Recorder 374
Measurements 375
CB Condition Monitoring 383
CB State Monitoring 390
Circuit Breaker Control 392
Pole Dead Function 397
System Checks 399

## 17.2 EVENT RECORDS

GE Vernova devices record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

The event records are detailed in the *VIEW RECORDS* column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

If viewing the event with the settings application software, simply open the extracted event file. All the events are displayed chronologically. Each event is summarised with a time stamp obtained from the ***Time & Date*** cell) and a short description relating to the event obtained from the ***Event Text*** cell). You can expand the details of the event by clicking on the **+** icon to the left of the time stamp.

The following table shows the correlation between the fields in the setting application software's event viewer and the cells in the menu database.

| Field in Event Viewer | Equivalent cell in menu DB | Cell reference | User settable? |
|---|---|---|---|
| Left hand column header | VIEW RECORDS → Time & Date | 01 03 | No |
| Right hand column header | VIEW RECORDS → Event Text | 01 04 | No |
| Description | SYSTEM DATA → Description | 00 04 | Yes |
| Plant reference | SYSTEM DATA → Plant Reference | 00 05 | Yes |
| Model number | SYSTEM DATA → Model Number | 00 06 | No |
| Address | Displays the Courier address relating to the event | N/A | No |
| Event type | VIEW RECORDS → Menu Cell Ref | 01 02 | No |
| Event Value | VIEW RECORDS → Event Value | 01 05 | No |
| Evt Unique Id | VIEW RECORDS → Evt Unique ID | 01 FE | No |

The device is capable of storing up to 1024 event records.

In addition to the event log, there are two logs which contain duplicates of the last 5 maintenance records and the last 5 fault records. The purpose of this is to provide convenient access to the most recent fault and maintenance events.

### 17.2.1 EVENT TYPES

There are several different types of event:

- Opto-input events (Change of state of opto-input)
- Contact events (Change of state of output relay contact)
- Alarm events
- Fault record events
- Standard events
- Security events

Standard events are further sub-categorised internally to include different pieces of information. These are:

- Protection events (starts and trips)
- Maintenance record events
- Platform events

*Note:*
*The first event in the list (event 0) is the most recent event to have occurred.*

#### 17.2.1.1 OPTO-INPUT EVENTS

If one or more of the opto-inputs has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all opto-inputs. You can tell which opto-input has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Logic Inputs #` where # is the batch number of the opto-inputs. This is '1', for the first batch of opto-inputs and '2' for the second batch of opto-inputs (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the opto-inputs, where the Least Significant Bit (LSB), on the right corresponds to the first opto-input `Input L1`.

The same information is also shown in the ***Opto I/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

#### 17.2.1.2 CONTACT EVENTS

If one or more of the output relays (also known as output contacts) has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all output relays. You can tell which output relay has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Output Contacts #` where # is the batch number of the output relay contacts. This is '1', for the first batch of output contacts and '2' for the second batch of output contacts (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the output relays, where the LSB (on the right) corresponds to the first output contact `Output R1`.

The same information is also shown in the ***Relay O/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

#### 17.2.1.3 ALARM EVENTS

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event.

The description of this event type, as shown in the ***Event Text*** cell is cell dependent on the type of alarm and will be one of those shown in the following tables, followed by `OFF` or `ON`.

The event value shown in the ***Event Value*** cell for this type of event is a 32 bit binary string. There are one or more banks 32 bit registers, depending on the device model. These contain all the alarm types and their logic states (`ON` or `OFF`).

The same information is also shown in the ***Alarm Status (n)*** cells in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

### 17.2.1.4 FAULT RECORD EVENTS

An event record is created for every fault the IED detects. This is also known as a fault record.

The event type description shown in the ***Event Text*** cell for this type of event is always `Fault Recorded`.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the ***Select Fault*** setting, where fault number 0 is the latest fault.

A fault record is triggered by the ***Fault REC TRIG*** signal DDB, which is assigned in the PSL. The fault recorder records the values of all parameters associated with the fault for the duration of the fault. These parameters are stored in separate Courier cells, which become visible depending on the type of fault.

The fault recorder stops recording only when:

The Start signal is reset AND the undercurrent is ON OR the Trip signal is reset, as shown below:

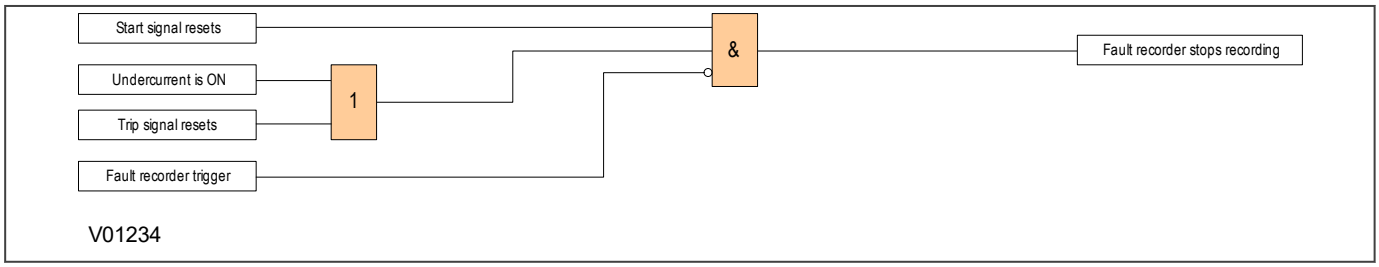



**Figure 228: Fault recorder stop conditions**

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The timestamp assigned to the fault record event corresponds to the time when the fault recorder stops.

*Note:*
*We recommend that you do not set the triggering contact to latching. This is because if you use a latching contact, the fault record would not be generated until the contact has been fully reset.*

### 17.2.1.5 MAINTENANCE EVENTS

Internal failures detected by the self-test procedures are logged as maintenance records. Maintenance records are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is always `Maint Recorded`.

The ***Event Value*** cell also provides a unique binary code.

The IED contains a separate register containing the latest maintenance records. This provides a convenient way of viewing the latest maintenance records and saves searching through the event log. You access these fault records using the ***Select Maint*** setting.

The maintenance record has a number of extra menu cells relating to the maintenance event. These parameters are ***Maint Text***, ***Maint Type*** and ***Maint Data***. They contain details about the maintenance event selected with the ***Select Maint*** cell.

### 17.2.1.6 PROTECTION EVENTS

The IED logs protection starts and trips as individual events. Protection events are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is dependent on the protection event that occurred. Each time a protection event occurs, a DDB signal changes state. It is the name of this DDB signal followed by 'ON' or 'OFF' that appears in the ***Event Text*** cell.

The ***Event Value*** cell for this type of event is a 32 bit binary string representing the state of the relevant DDB signals. These binary strings can also be viewed in the *COMMISSION TESTS* column in the relevant DDB batch cells.

Not all DDB signals can generate an event. Those that can are listed in the *RECORD CONTROL* column. In this column, you can set which DDBs generate events.

#### 17.2.1.7 SECURITY EVENTS

An event record is generated each time a setting that requires an access level is executed.

The event type description shown in the ***Event Text*** cell displays the type of change.

#### 17.2.1.8 PLATFORM EVENTS

Platform events are special types of standard events.

The event type description shown in the ***Event Text*** cell displays the type of change.

## 17.3 DISTURBANCE RECORDER

The disturbance recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals. The digital signals may be inputs, outputs, or internal DDB signals. The disturbance records can be extracted using the disturbance record viewer in the settings application software. The disturbance record file can also be stored in the COMTRADE format. This allows the use of other packages to view the recorded data.

The integral disturbance recorder has an area of memory specifically set aside for storing disturbance records. The number of records that can be stored is dependent on the recording duration. The minimum duration is 0.1 s and the maximum duration is 10.5 s.

When the available memory is exhausted, the oldest records are overwritten by the newest ones.

Each disturbance record consists of a number of analogue data channels and digital data channels. The relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities.

The fault recording times are set by a combination of the ***Duration*** and ***Trigger Position*** cells. The ***Duration*** cell sets the overall recording time and the ***Trigger Position*** cell sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

With the ***Trigger Mode*** set to *Single*, if further triggers occurs whilst a recording is taking place, the recorder will ignore the trigger. However, with the ***Trigger Mode*** set to *Extended*, the post trigger timer will be reset to zero, extending the recording time.

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

You may choose any of the digital channels to trigger the disturbance recorder on either a low to high or a high to low transition, via the ***Input Trigger*** cell. The default settings are such that any dedicated trip output contacts will trigger the recorder.

It is not possible to view the disturbance records locally via the front panel LCD. You must extract these using suitable setting application software such as MiCOM S1 Agile.

# 17.4 MEASUREMENTS

## 17.4.1 MEASURED QUANTITIES

The device measures directly and calculates a number of system quantities, which are updated every second. You can view these values in the relevant MEASUREMENT columns or with the Measurement Viewer in the settings application software. Depending on the model, the device may measure and display some or more of the following quantities:

- Measured and calculated analogue current and voltage values
- Power and energy quantities
- Peak, fixed and rolling demand values
- Frequency measurements
- Thermal measurements
- Teleprotection channel measurements

## 17.4.2 MEASUREMENT SETUP

You can define the way measurements are set up and displayed using the *MEASURE'T SETUP* column and the measurements are shown in the relevant MEASUREMENTS tables.

## 17.4.3 FAULT LOCATOR

Some models provide fault location functionality. It is possible to identify the fault location by measuring the fault voltage and current magnitude and phases and presenting this information to a Fault Locator function. The fault locator is triggered whenever a fault record is generated, and the subsequent fault location data is included as part of the fault record. This information is also displayed in the ***Fault Location*** cell in the *VIEW RECORDS* column. This cell will display the fault location in metres, miles ohms or percentage, depending on the chosen units in the ***Fault Location*** cell of the *MEASURE'T SETUP* column.

The Fault Locator uses pre-fault and post-fault analogue input signals to calculate the fault location. The result is included it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record.

When applied to parallel circuits, mutual flux coupling can alter the impedance seen by the fault locator. The coupling contains positive, negative and zero sequence components. In practise the positive and negative sequence coupling is insignificant. The effect on the fault locator of the zero sequence mutual coupling can be eliminated using the mutual compensation feature provided.

### 17.4.3.1 FAULT LOCATOR OPERATION

The P443 fault locator uses an algorithmic method to provide a distance to fault location feature with metering capabilities. The data input to the algorithm is filtered using established digital signal processing techniques.

The data processed by the algorithm is first acquired by performing analogue to digital conversion on signals provided by the relays internal analogue bus and then performing the necessary calculations.

The metering values are continuously calculated, regularly updated and passed to the relays processor when requested.

Acquired data is written to a buffer until a fault condition is notified by the processor. This input buffer data is held pending the fault calculation and input data is redirected to an alternative buffer.

The fault calculation is initiated by a signal from the relay main processor. When the fault calculation is complete the output information is stored in non-volatile memory and made available to the processor for display on the relay front panel.

Where parallel circuits are hung on opposite sides of a route of towers, mutual flux coupling alters the impedance seen by the fault locator. In practice the positive and negative sequence coupling is insignificant and the effect on

the fault locator of the zero sequence mutual coupling can be eliminated by using the mutual compensation feature provided.

It should be noted that in relays fitted with both a ***DEF*** element and a fault locator, the mutual compensation current input terminals are shared with the ***DEF*** zero sequence current polarising input. And so, ***DEF*** zero sequence current polarising cannot be used at the same time as fault locator mutual compensation.

The fault locator is optional on the underground cable version of the relay, where it is recommended that it is used for metering purposes only (see the Metering section, below) as fault location accuracy cannot be relied upon for this application.

### 17.4.3.2 EARTH FAULT BASIC THEORY

A two-machine equivalent circuit of a faulted power system is shown in the figure below:

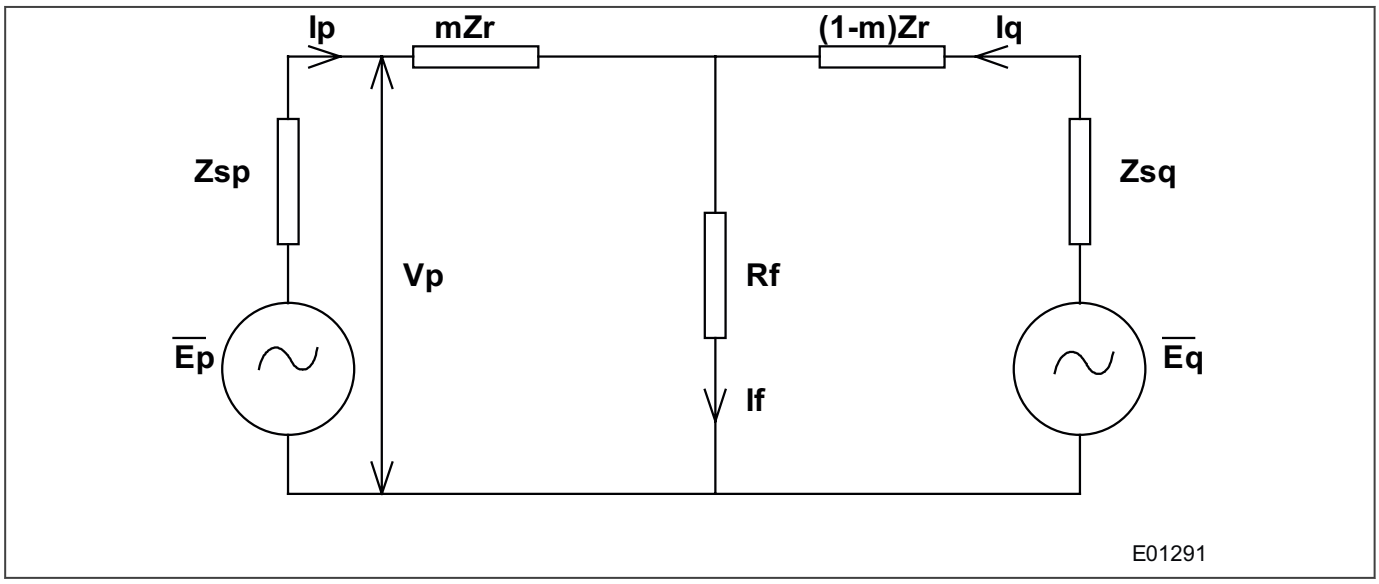



**Figure 229: Two machine equivalent circuit**

From the above figure:

$$Vp = mIpZr + IfRf$$

This equation shows that the calculation of m, the distance to fault, based on measurements of Vp and Ip at the local relay terminals is distorted by the IfRf term. This term is related to the current infeed from the remote terminal and cannot be readily measured. However its effect can be minimised as follows:

The real and imaginary components of these vectors (with respect to an arbitrary vector reference) vary with time as:

$$|Vp|[\cos(\omega t + s) + j\sin(\omega t + s)] = m|Zr|\,|Ip|\,[\cos(\omega t + e) + j\sin(\omega tt + e)] + Rf\,|If|\,[\cos(\omega t + d) + j\sin(\omega t + d)].$$

where:

d is the angle of the fault current.

s is the angle of Vp.

e is the angle of IpZr.

By evaluating equation *Vp = mIpZr + IfRf* at the instant in time when the fault current passes through zero and considering only the real components, then the Rf |If| term becomes zero i.e. t = (( $\pi$/2)-d)/ $\omega$ and the equation simplifies to:

$$|Vp|\cos(((\pi/2)-d) + s) = m\,|Zr|\,|Ip|\,\cos(((\pi/2)-d) + e)$$

Therefore, the fault location m can be calculated if the angle of the fault current d is known.

Estimating d the phase of the fault current If:

The fault vector If is obtained from an algorithm which uses superimposed currents, that is, the change of currents following the instant of fault.

Superimposed currents are indicated with an apostrophe ( ' ).

The sequence diagram for superimposed currents for an A-G fault is shown in the figure below:

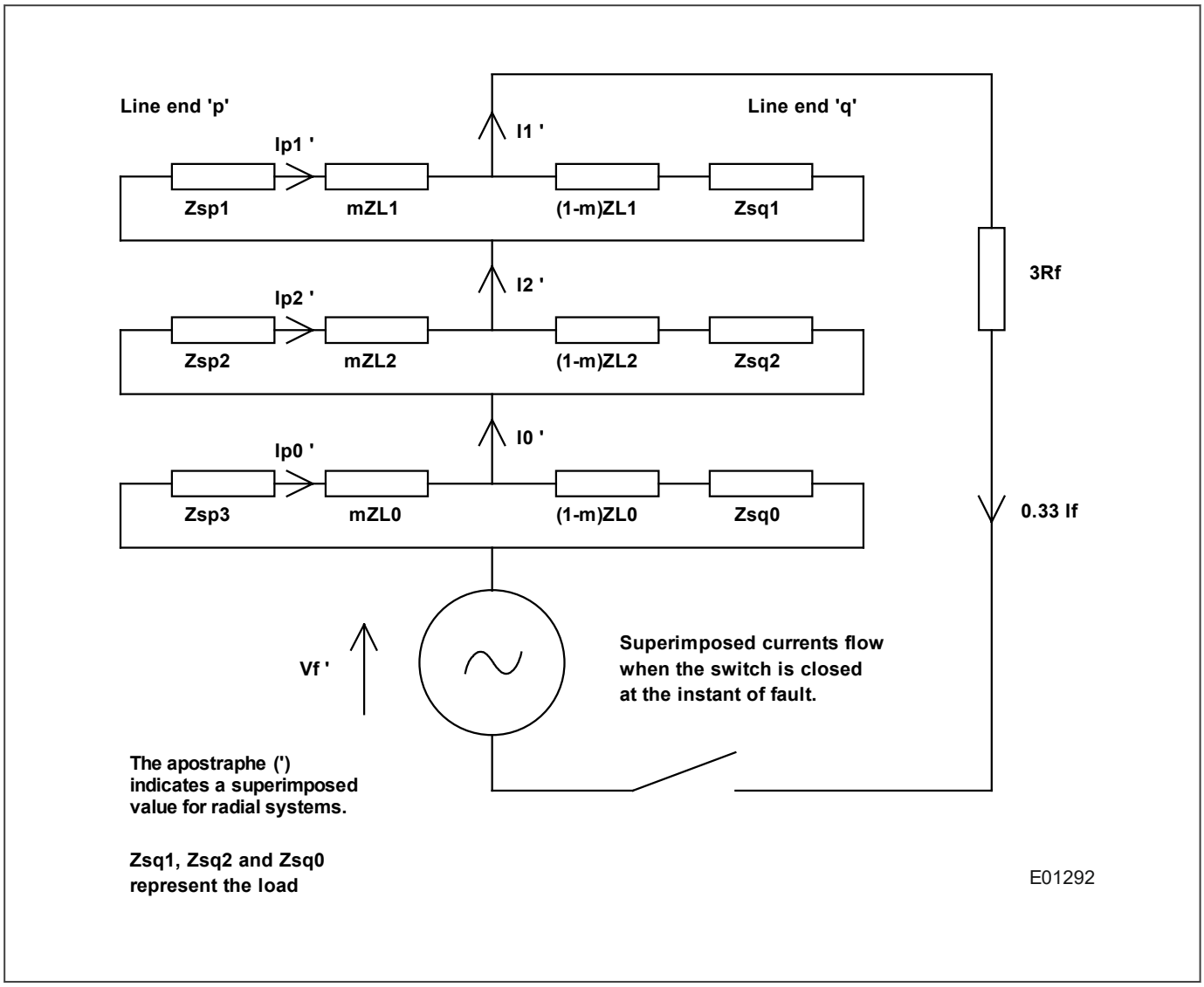



**Figure 230: Superimposed symmetrical component sequence for A - N fault**

For an A phase to earth fault:

$$0.33If = I1' = I2' = I0'$$

from which:

$$0.66If = I1' + I2'$$

$$= Ip1'D1 + Ip2'D2$$

where:

$$D1 = I1' / Ip1' \text{ and } D2 = I2' / Ip2'$$

and:

D2 approximately = D1 (assuming that the power system source and line positive and negative sequence impedances are approximately equal)

therefore:

$$0.66If = D1(Ip1' + Ip2')$$

also:

$$Ip' = Ip1' + Ip2' + Ip0'$$

therefore:

$$Ip1' + Ip2' = Ip' - Ip0'$$

from the equations above:

$$0.66If = D1\ (Ip' - Ip0')$$

Hence:

$$\text{angle } If = \text{angle } D1 + \text{angle } (Ip' - Ip0')$$

where:

D1 = A SCALAR factor - assuming that the power system is homogeneous
$= (Zsp1 + Zl1 + Zsq1) / ((1-m)Zl1 + Zsq1)$

The angle of D1 depends upon the fault position but for the purposes of this algorithm this angle is assumed to be zero.

Thus:

$$\text{angle } If = d = \text{angle } (Ip' - Ip0')$$

The equation above, shows that the phase angle of the fault current d can be estimated from the superimposed phase and neutral currents measured at the relay terminals.

therefore for an earth fault:

$$|If|(\cos(d) + j\sin(d))$$
$$= kD1(Ip'-Ip0')$$
$$= kD1[(Ia(fault) - Ia(prefault))$$
$$- 0.33(In(fault) - In(prefault))]$$

where:

k is a scalar factor and d is the required phase angle of If at the instant of time that the faulted vectors are calculated.

similarly, for a phase to phase fault:

$$|If|\ (\cos(d) + j\sin(d)) = kD1[(Ia(fault) - Ia(prefault))- (Ib(fault) - Ib(prefault))]$$

Thus, using the calculated pre-fault and faulted vectors the fault locator is able to calculate the angle of the fault current vector d at the instant of time that the faulted vectors are calculated.

#### 17.4.3.3 DATA ACQUISITION AND BUFFER PROCESSING

The fault locator stores the sampled data within a 12 cycle cyclic buffer at a resolution of 48 samples per cycle. When the fault recorder is triggered the data in the buffer is frozen such that the buffer contains 6 cycles of pre-trigger data and 6 cycles of post-trigger data. Fault calculation commences shortly after this trigger point.

The trigger for the fault recorder is user selectable via the programmable scheme logic.

The fault locator can store data for up to four faults. This ensures that fault location can be calculated for all shots on a typical multiple reclose sequence.

### 17.4.3.4 FAULTED PHASE SELECTION

Phase selection is derived from the superimposed current phase selector.

Phase selection and fault location calculations can only be made if the current change exceeds 5% In.

### 17.4.3.5 FAULTED PHASE CALCULATION

The fault location calculation works by:

1. First obtaining the vectors
2. Selecting the faulted phase(s)
3. Estimating the phase of the fault current If for the faulted phase(s)
4. Solving the below equation for the fault location m at the instant of time where f = 0

$$Vp = mIpZr + IfRf$$

### 17.4.3.6 DISTANCE TO FAULT CALCULATION

#### Replica impedance Zr

The fault location calculation needs vectors derived from the line voltage (Vp) and from the relay's "replica impedance" voltage (IpZr) under fault conditions. The replica impedance is derived from the relay settings and is effectively set to the same value as the total line impedance. i.e.

$$Zr = Zline / \theta\ line + Zresidual / / \theta\ residual$$

This "replica impedance" is modified using the mutual compensation factor when the mutual compensation feature is used. i.e.

$$Zr = Zline / \theta\ line + Zresidual / / \theta\ residual + Zmutual / / \theta\ mutual$$

Where :

$$Zresidual = kZN*Zline$$
$$Zmutual = kZm*Zline$$

### The fault location calculation

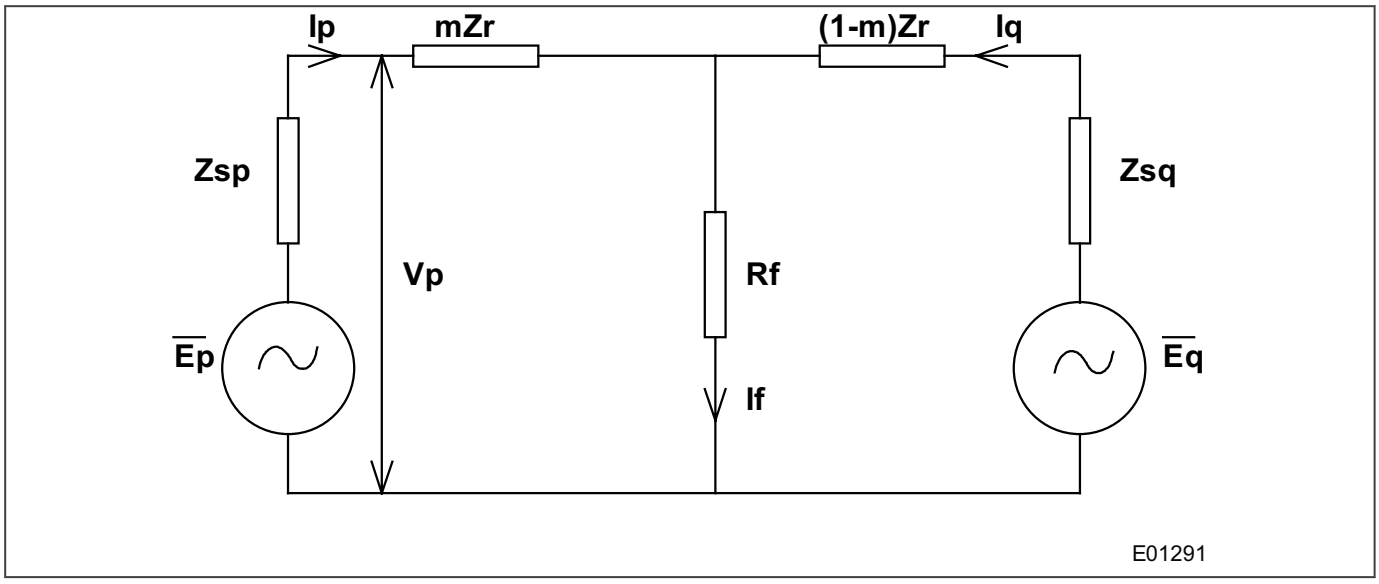



**Figure 231: Two machine equivalent circuit**

Fault location equation:

$$Vp = mIpZr + IfRf$$

Referring to the figure and equation, above.

The fault location calculation works by:

1. First obtaining the vectors to satisfy the above equation for the fault type specified by the phase selector.
2. Then estimating the phase of the fault current If.
3. Finally solving the above equation for the fault location m at the instant of time where If = 0.

### Obtaining the vectors

Different sets of vectors are chosen depending on the type of fault identified by the phase selection algorithm. The calculation using fault location equation, above is applied for either a phase to earth fault or a phase to phase fault.

Thus, for a A phase to earth fault:

$$IpZr = Ia\ (Zline / \theta\ line) + In\ (Zresidual / / \theta\ residual)$$

and

$$Vp = VA$$

And for a A phase to B phase fault:

$$IpZr = Ia\ (\ Zline / \theta\ line\ ) - Ib\ (Zline / \theta\ line)$$

and

$$Vp = VA - VB$$

The calculation for an earth fault (A phase to earth fault equation, above) is modified when mutual compensation is used :

$$IpZr = Ia\ (Zline / \theta\ line) + In(Zresidual / / \theta\ residual\ ) + Im(Zmutual / / \theta\ mutual)$$

### Solving the equation for the fault location

As the sine wave of If passes through zero, the instantaneous values of the sine waves Vp and □p can be used to solve the below equation for the fault location m. (The term IfRf being zero).

$$Vp = mIpZr + IfRf$$

This is determined by shifting the calculated vectors of Vp and IpZr by the angle (90° - angle of fault current) and then dividing the real component of Vp by the real component of IpZr. (See figure, below).

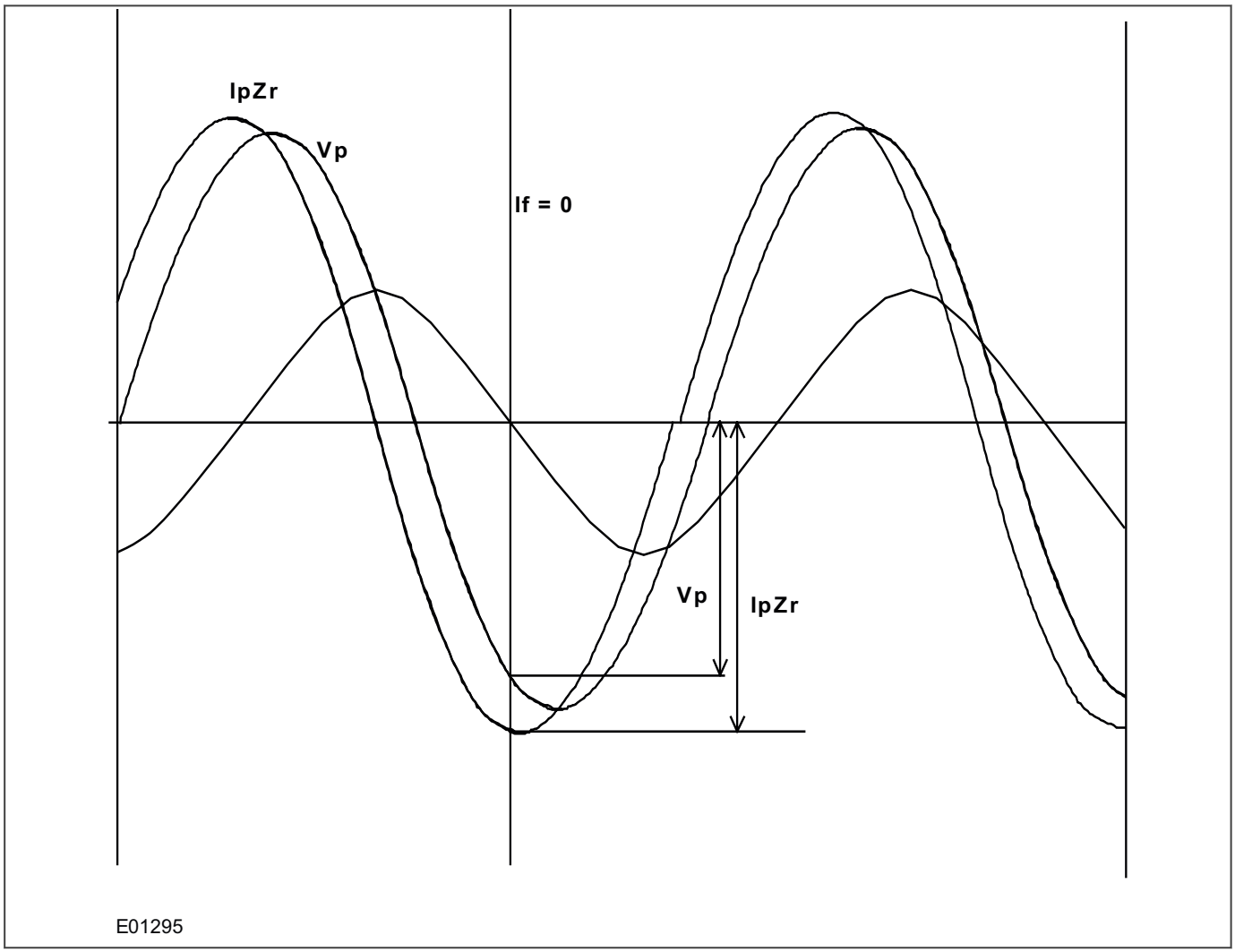



**Figure 232: Fault locator selection of fault current zero**

i.e.:

Phase advanced vector Vp

$$= |Vp| [\cos(s) + j\sin(s)] * [\sin(d) + j\cos(d)]$$

$$= |Vp| [-\sin(s-d) + j\cos(s-d)]$$

Phase advanced vector IpZr

$$= ||pZr| [\cos(e) + j\sin(e)] * [\sin(d) + j\cos(d)]$$

$$= ||pZr| [-\sin(e-d) + j\cos(e-d)]$$

Therefore, from equation 1:

$$m = Vp \div (Ip * Zr) \text{ at } If = 0$$

$$= Vp \sin(s-d)/(IpZr * \sin(e-d))$$

Where:

d = Angle of fault current If

s = Angle of Vp

e = Angle of IpZr

Thus, the relay evaluates m which is the fault location as a percentage of the fault locator line impedance setting and then calculates the output fault location by multiplying this by the line length setting. When calculated the fault location can be found in the fault record under the *VIEW RECORDS* column in the ***Fault Location*** cells. Distance to fault is available in kilometers, miles, impedance or percentage of line length.

#### 17.4.3.7 MUTUAL COMPENSATION

Analysis of a ground fault on one circuit of a parallel over-head line shows that a fault locator positioned at one end of the faulty line will tend to over-reach while that at the other end will tend to under-reach. In cases of long lines with high mutual inductance, mutual zero sequence compensation can be used to improve the fault locator accuracy. The compensation is achieved by taking an input to the relay from the residual circuit of the current transformers in the parallel line.

The P443 provides mutual compensation for both the fault locator function, AND the distance protection zones.

#### 17.4.3.8 METERING

The metering calculations are continuously performed using the same fourier technique used by the fault locator. The results of these calculations are continuously updated and can be viewed using the relay user interface.

### 17.4.4 OPTO-INPUT TIME STAMPING

Each opto-input sample is time stamped within a tolerance of +/- 1 ms with respect to the Real Time Clock. These time stamps are used for the opto event logs and for the disturbance recording. The device needs to be synchronised accurately to an external clock source such as an IRIG-B signal or a master clock signal provided in the relevant data protocol.

For both the filtered and unfiltered opto-inputs, the time stamp of an opto-input change event is the sampling time at which the change of state occurred. If multiple opto-inputs change state at the same sampling interval, these state changes are reported as a single event.

## 17.5 CB CONDITION MONITORING

The device records various statistics related to each circuit breaker trip operation, allowing an accurate assessment of the circuit breaker condition to be determined. These statistics are available in the *CB CONDITION* column. The menu cells are register values only and cannot be set directly. They may be reset, however, during maintenance. The statistics monitored are:

- Total Current Broken: A register stores the total amount of current that the CB has broken is stored in an accumulator, giving at any time a measure of the total amount of current that the CB has broken since the value was last reset.
- Number of CB operations: A counter registers the number of CB trips that have been performed for each phase, giving at any time the total number of trips that the CB has performed since the value was last reset.
- CB Operate Time: A register stores the total amount of time the CB has transitioned from closed to open is stored in an accumulator, giving at any time a measure of the total time that the CB has spent tripping since the values was last reset.
- Excessive Fault Frequency: A counter registers the number of CB trips that have been performed for all phases, giving at any time the total number of trips performed since the value was last reset.

These statistics are available in the *CB CONDITION* column. The menu cells are register values only and cannot be set directly. They may be reset, however, during maintenance.

*Note:*
*When in Commissioning test mode the CB condition monitoring registers are not updated.*

Circuit breaker lockout, can be caused by the following circuit breaker condition monitoring functions:

- Maintenance lockout
- Excessive fault frequency lockout
- Broken current lockout

If the circuit breaker is locked out, the logic generates a lockout alarm

## 17.5.1 BROKEN CURRENT ACCUMULATOR

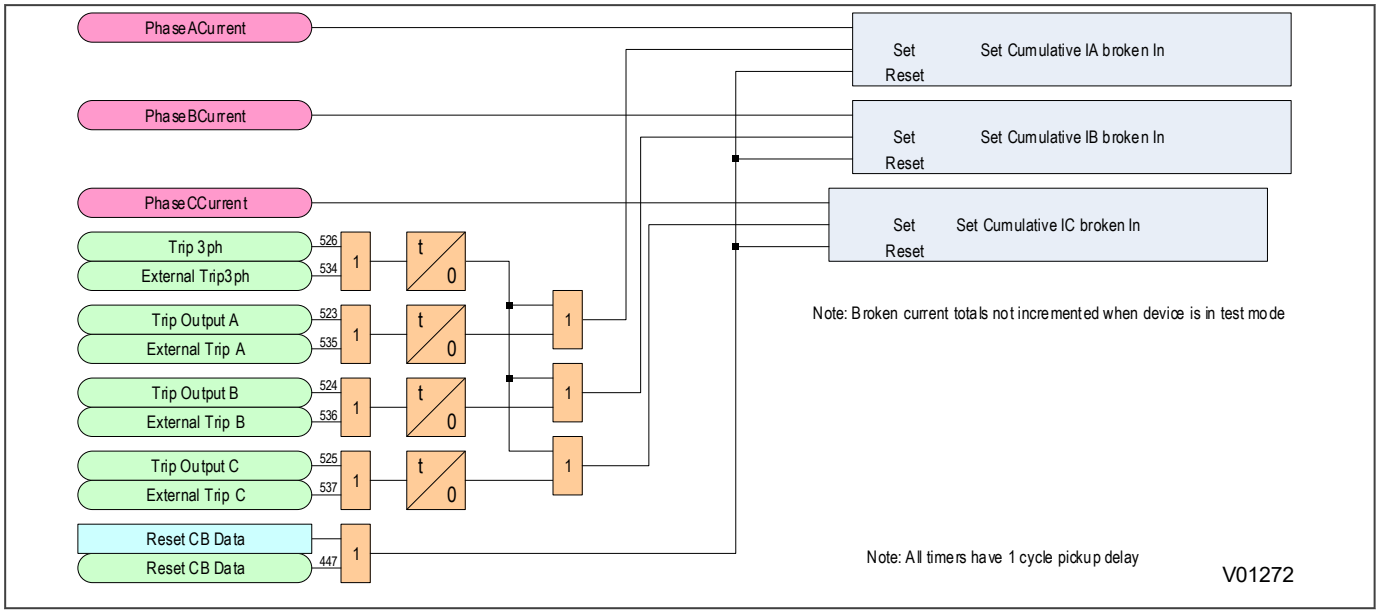



**Figure 233: Broken Current Accumulator logic diagram**

## 17.5.2 CB TRIP COUNTER

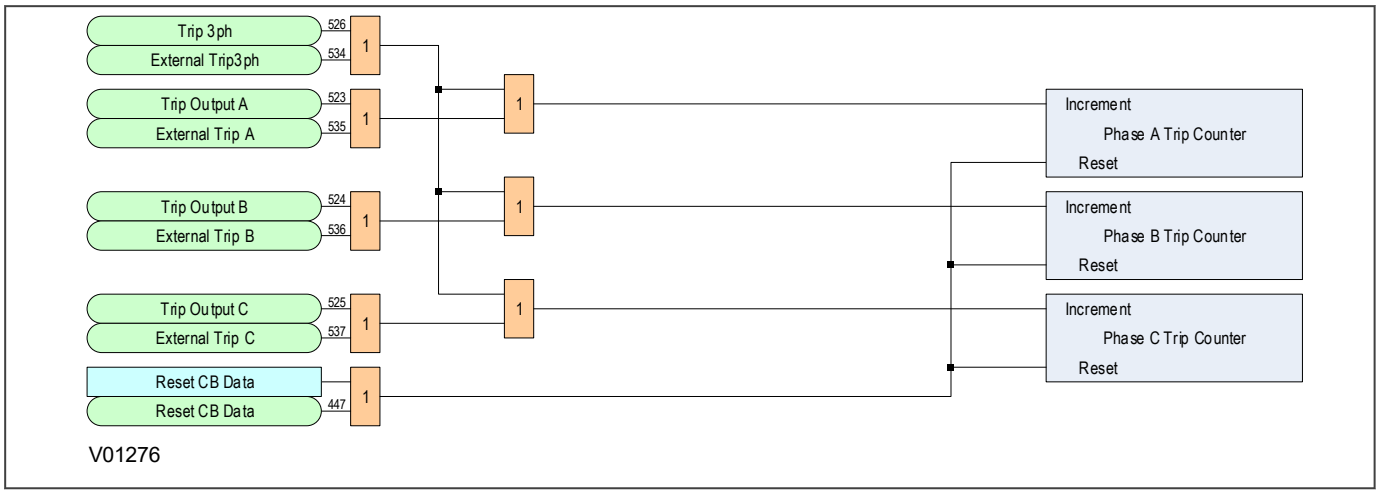



**Figure 234: CB Trip Counter logic diagram**

## 17.5.3 CB OPERATING TIME ACCUMULATOR

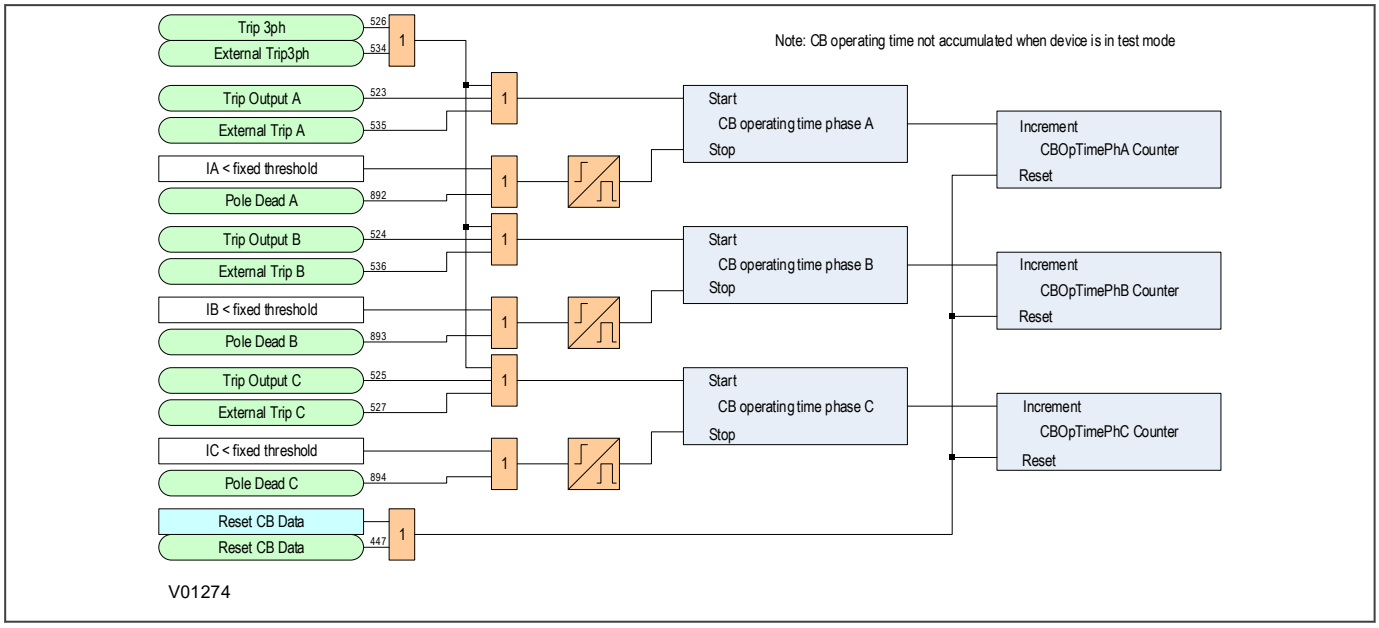



**Figure 235: Operating Time Accumulator**

## 17.5.4 EXCESSIVE FAULT FREQUENCY COUNTER

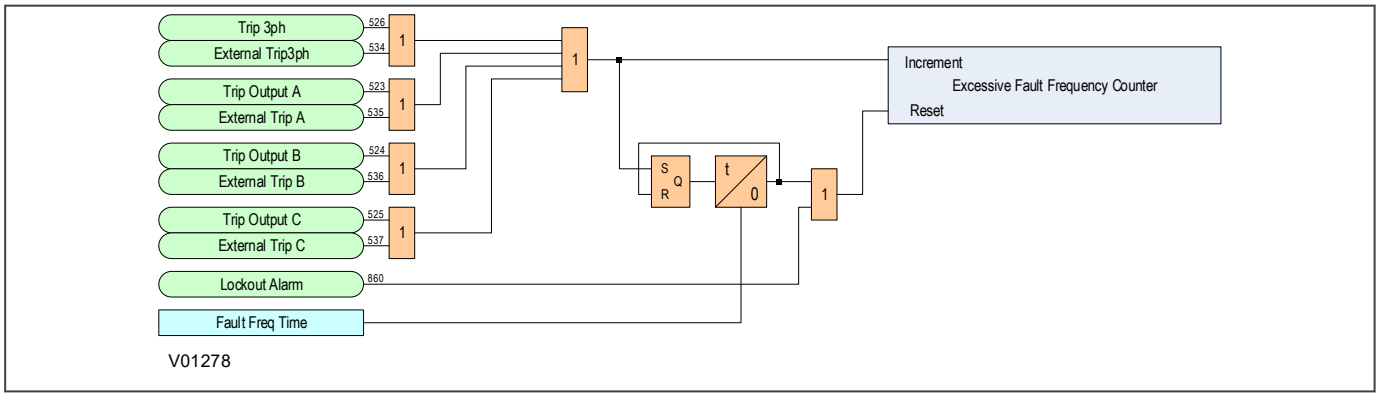



**Figure 236: Excessive Fault Frequency logic diagram**

## 17.5.5 RESET LOCKOUT ALARM

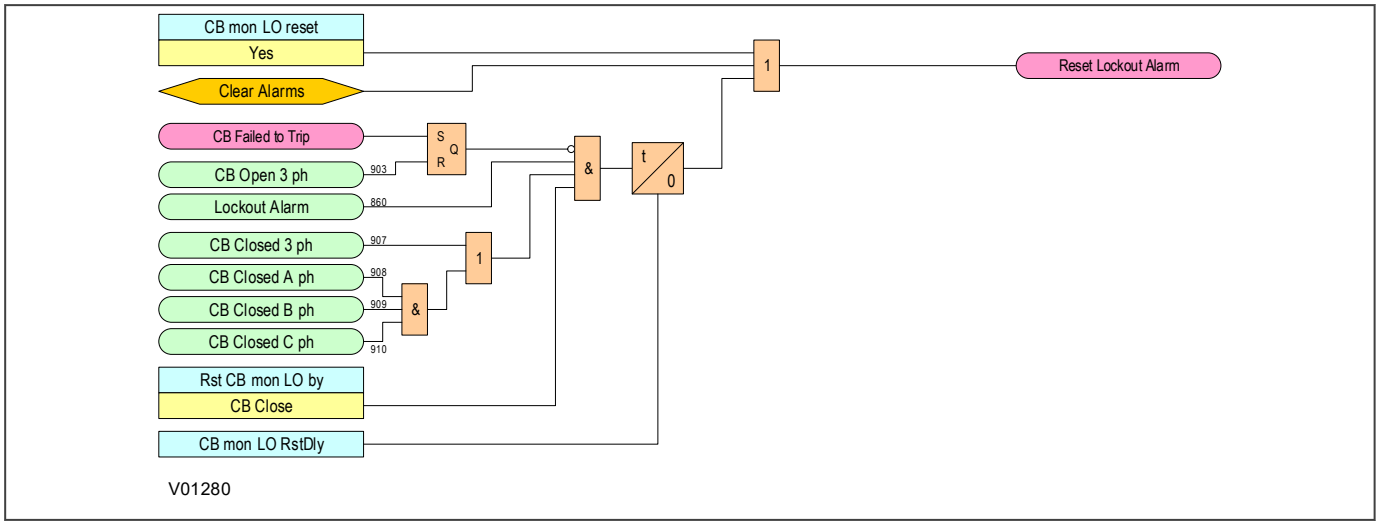



**Figure 237: Reset Lockout Alarm logic diagram**

## 17.5.6 CB CONDITION MONITORING LOGIC

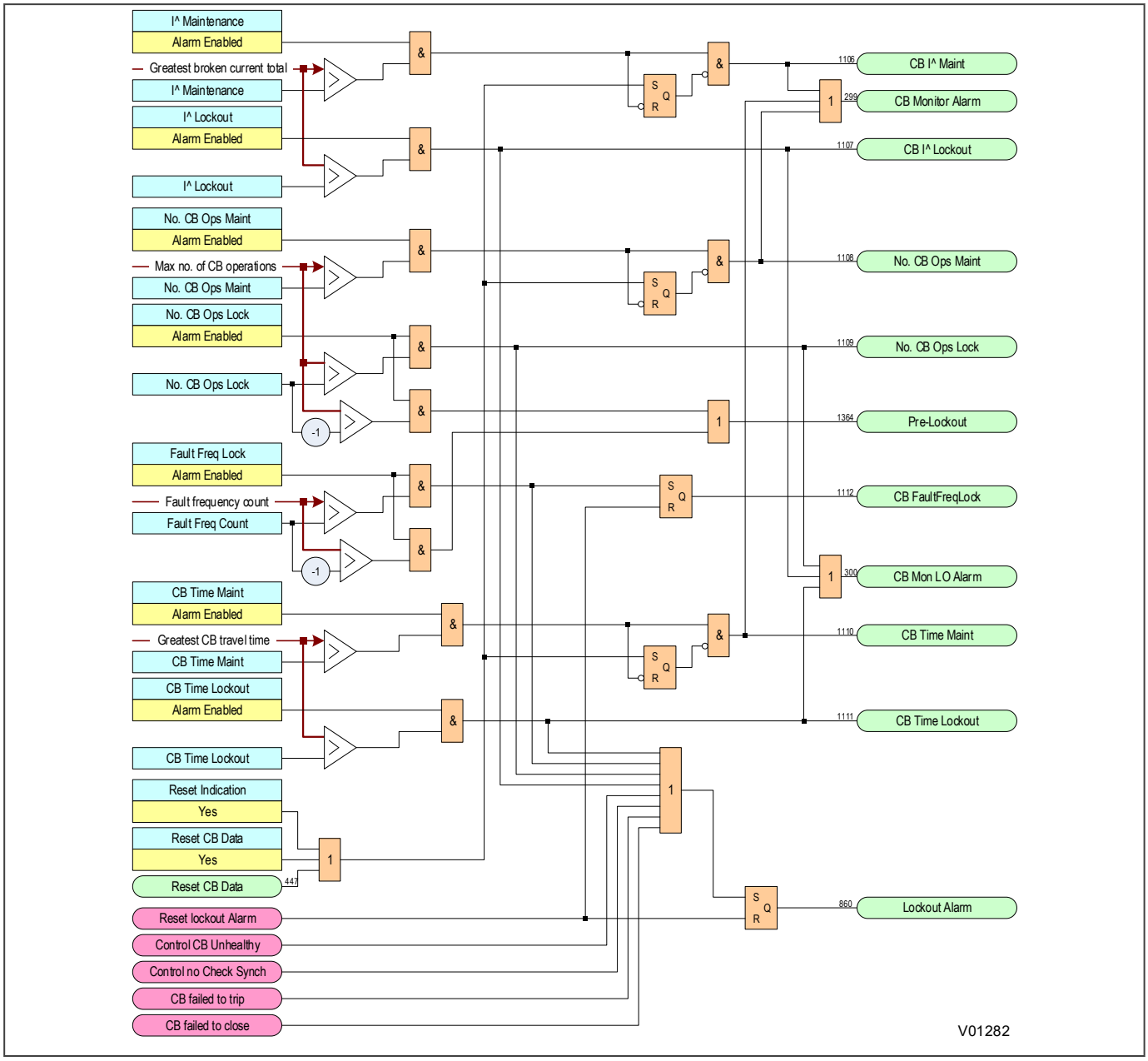



**Figure 238: CB Condition Monitoring logic diagram**

## 17.5.7 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to `Enabled`, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to `Enabled`, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to `Enabled`, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to `Enabled`, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is `Enabled`, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

### 17.5.7.1 RESET CB LOCKOUT LOGIC DIAGRAM

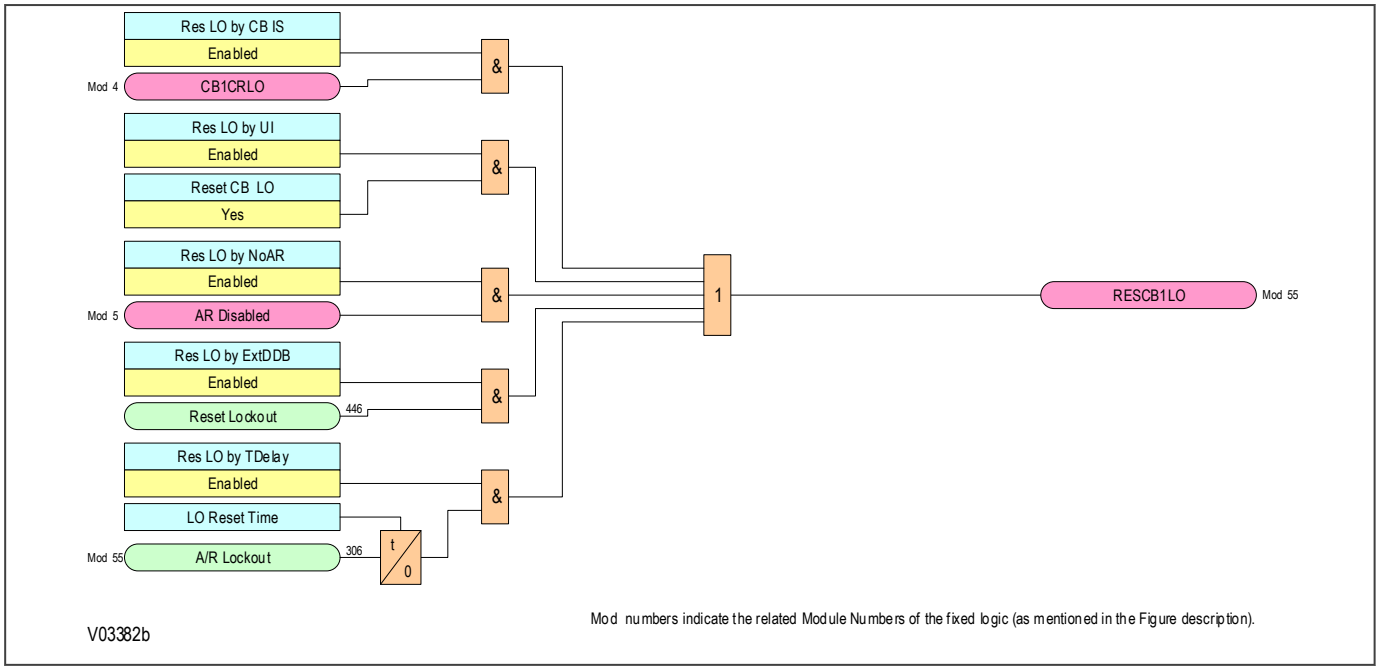



**Figure 239: Reset Circuit Breaker Lockout Logic Diagram (Module 57)**

## 17.5.8 APPLICATION NOTES

### 17.5.8.1 SETTING THE THRESHOLDS FOR THE TOTAL BROKEN CURRENT

Where power lines use oil circuit breakers (OCBs), changing of the oil accounts for a significant proportion of the switchgear maintenance costs. Often, oil changes are performed after a fixed number of CB fault operations. However, this may result in premature maintenance where fault currents tend to be low, because oil degradation may be slower than would normally be expected. The Total Current Accumulator (I^ counter) cumulatively stores the total value of the current broken by the circuit breaker providing a more accurate assessment of the circuit breaker condition.

The dielectric withstand of the oil generally decreases as a function of $I^2t$, where ‘I’ is the broken fault current and ‘t’ is the arcing time within the interrupter tank. The arcing time cannot be determined accurately, but is generally dependent on the type of circuit breaker being used. Instead, you set a factor (***Broken I^***) with a value between 1 and 2, depending on the circuit breaker.

Most circuit breakers would have this value set to '2', but for some types of circuit breaker, especially those operating on higher voltage systems, a value of 2 may be too high. In such applications ***Broken I^*** may be set lower, typically 1.4 or 1.5.

The setting range for ***Broken I^*** is variable between 1.0 and 2.0 in 0.1 steps.

*Note:*
*Any maintenance program must be fully compliant with the switchgear manufacturer's instructions.*

### 17.5.8.2 SETTING THE THRESHOLDS FOR THE NUMBER OF OPERATIONS

Every circuit breaker operation results in some degree of wear for its components. Therefore routine maintenance, such as oiling of mechanisms, may be based on the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventative maintenance is due. Should maintenance not be carried out, the device can be set to lockout the autoreclose function on reaching a second operations threshold (***No. CB ops Lock***). This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Some circuit breakers, such as oil circuit breakers (OCBs) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonising of the oil, degrading its dielectric properties. The maintenance alarm threshold (setting ***No. CB Ops Maint***) may be set to indicate the requirement for oil dielectric testing, or for more comprehensive maintenance. Again, the lockout threshold ***No. CB Ops Lock*** may be set to disable autoreclosure when repeated further fault interruptions could not be guaranteed. This minimises the risk of oil fires or explosion.

### 17.5.8.3 SETTING THE THRESHOLDS FOR THE OPERATING TIME

Slow CB operation indicates the need for mechanism maintenance. Alarm and lockout thresholds (***CB Time Maint*** and ***CB Time Lockout***) are provided to enforce this. They can be set in the range of 5 to 500 ms. This time relates to the interrupting time of the circuit breaker.

### 17.5.8.4 SETTING THE THRESHOLDS FOR EXCESSSIVE FAULT FREQUENCY

Persistent faults will generally cause autoreclose lockout, with subsequent maintenance attention. Intermittent faults such as clashing vegetation may repeat outside of any reclaim time, and the common cause might never be investigated. For this reason it is possible to set a frequent operations counter, which allows the number of operations ***Fault Freq Count*** over a set time period ***Fault Freq Time*** to be monitored. A separate alarm and lockout threshold can be set.

## 17.6 CB STATE MONITORING

CB State monitoring is used to verify the open or closed state of a circuit breaker. Most circuit breakers have auxiliary contacts through which they transmit their status (open or closed) to control equipment such as IEDs. These auxiliary contacts are known as:

- 52A for contacts that follow the state of the CB
- 52B for contacts that are in opposition to the state of the CB

This device can be set to monitor both of these types of circuit breaker state indication. If the state is unknown for some reason, an alarm can be raised.

Some CBs provide both sets of contacts. If this is the case, these contacts will normally be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5 s time delay. An output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

In the CB CONTROL column there is a setting called ***CB Status Input***. This cell can be set at one of the following four options:

- None
- 52A
- 52B
- Both 52A and 52B

Where *None* is selected no CB status is available. Where only 52A is used on its own then the device will assume a 52B signal opposite to the 52A signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52B is used. If both 52A and 52B are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table:

| Auxiliary Contact Position | | CB State Detected | Action |
|---|---|---|---|
| 52A | 52B | | |
| Open | Closed | Breaker open | Circuit breaker healthy |
| Closed | Open | Breaker closed | Circuit breaker healthy |
| Closed | Closed | CB failure | Alarm raised if the condition persists for greater than 5 s |
| Open | Open | State unknown | Alarm raised if the condition persists for greater than 5 s |

## 17.6.1 CB STATE MONITOR LOGIC DIAGRAM

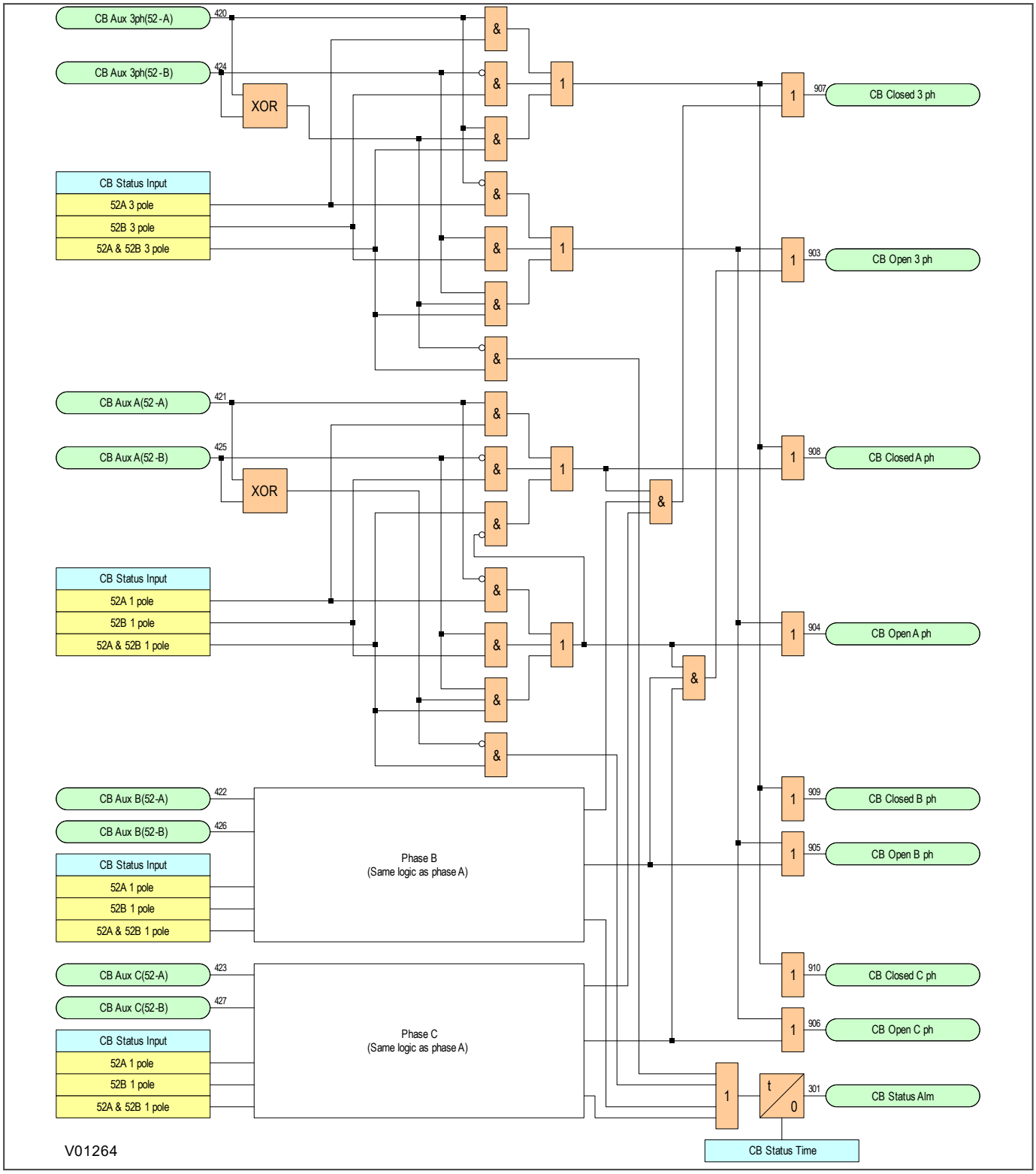



**Figure 240: CB State Monitor logic diagram (Module 1)**

## 17.7 CIRCUIT BREAKER CONTROL

Although some circuit breakers do not provide auxiliary contacts, most provide auxiliary contacts to reflect the state of the circuit breaker. These are:

- CBs with 52A contacts (where the auxiliary contact follows the state of the CB)
- CBs with 52B contacts (where the auxiliary contact is in the opposite state from the state of the CB)
- CBs with both 52A and 52B contacts

Circuit Breaker control is only possible if the circuit breaker in question provides auxiliary contacts. The ***CB Status Input*** cell in the *CB CONTROL* column must be set to the type of circuit breaker. If no CB auxiliary contacts are available then this cell should be set to `None`, and no CB control will be possible.

For local control, the ***CB control by*** cell should be set accordingly.

The output contact can be set to operate following a time delay defined by the setting ***Man Close Delay***. One reason for this delay is to give personnel time to safely move away from the circuit breaker following a CB close command.

The control close cycle can be cancelled at any time before the output contact operates by any appropriate trip signal, or by activating the ***Reset Close Dly*** DDB signal.

The length of the trip and close control pulses can be set via the ***Trip Pulse Time*** and **Close Pulse Time** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

The ***Reset Lockout by*** setting is used to enable or disable the resetting of lockout automatically from a manual close after the time set by ***Man Close RstDly***.

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) an alarm is generated after the relevant trip or close pulses have expired. These alarms can be viewed on the LCD display, remotely, or can be assigned to output contacts using the programmable scheme logic (PSL).

*Note:*
*The **CB Healthy Time** and **Sys Check time** set under this menu section are applicable to manual circuit breaker operations only. These settings are duplicated in the AUTORECLOSE menu for autoreclose applications.*

The ***Lockout Reset*** and ***Reset Lockout by*** settings are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example) and autoreclose lockouts.

The device includes the following options for control of a single circuit breaker:

- The IED menu (local control)
- The Hotkeys (local control)
- The function keys (local control)
- The opto-inputs (local control)
- SCADA communication (remote control)

### 17.7.1 CB CONTROL USING THE IED MENU

You can control manual trips and closes with the ***CB Trip/Close*** command in the *SYSTEM DATA* column. This can be set to `No Operation`, `Trip`, or `Close` accordingly.

For this to work you have to set the ***CB control by*** cell to option 1 *Local*, option 3 *Local + Remote*, option 5 *Opto+Local*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

## 17.7.2 CB CONTROL USING THE HOTKEYS

The hotkeys allow you to manually trip and close the CB without the need to enter the *SYSTEM DATA* column. For this to work you have to set the ***CB control by*** cell to option 1 *Local*, option 3 *Local+Remote*, option 5 *Opto +Local*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

CB control using the hotkey is achieved by pressing the right-hand button directly below LCD screen. This button is only enabled if:

- The ***CB Control by*** setting is set to one of the options where local control is possible (option 1,3,5, or 7)
- The ***CB Status Input*** is set to '52A', '52B', or 'Both 52A and 52B'

If the CB is currently closed, the command text on the bottom right of the LCD screen will read *Trip*. Conversely, if the CB is currently open, the command text will read *Close*.

If you execute a *Trip*, a screen with the CB status will be displayed once the command has been completed. If you execute a *Close*, a screen with a timing bar will appear while the command is being executed. This screen also gives you the option to cancel or restart the close procedure. The time delay is determined by the ***Man Close Delay*** setting in the *CB CONTROL* menu. When the command has been executed, a screen confirming the present status of the circuit breaker is displayed. You are then prompted to select the next appropriate command or exit.

If no keys are pressed for a period of 5 seconds while waiting for the command confirmation, the device will revert to showing the CB Status. If no key presses are made for a period of 25 seconds while displaying the CB status screen, the device will revert to the default screen.

To avoid accidental operation of the trip and close functionality, the hotkey CB control commands are disabled for 10 seconds after exiting the hotkey menu.

The hotkey functionality is summarised graphically below:

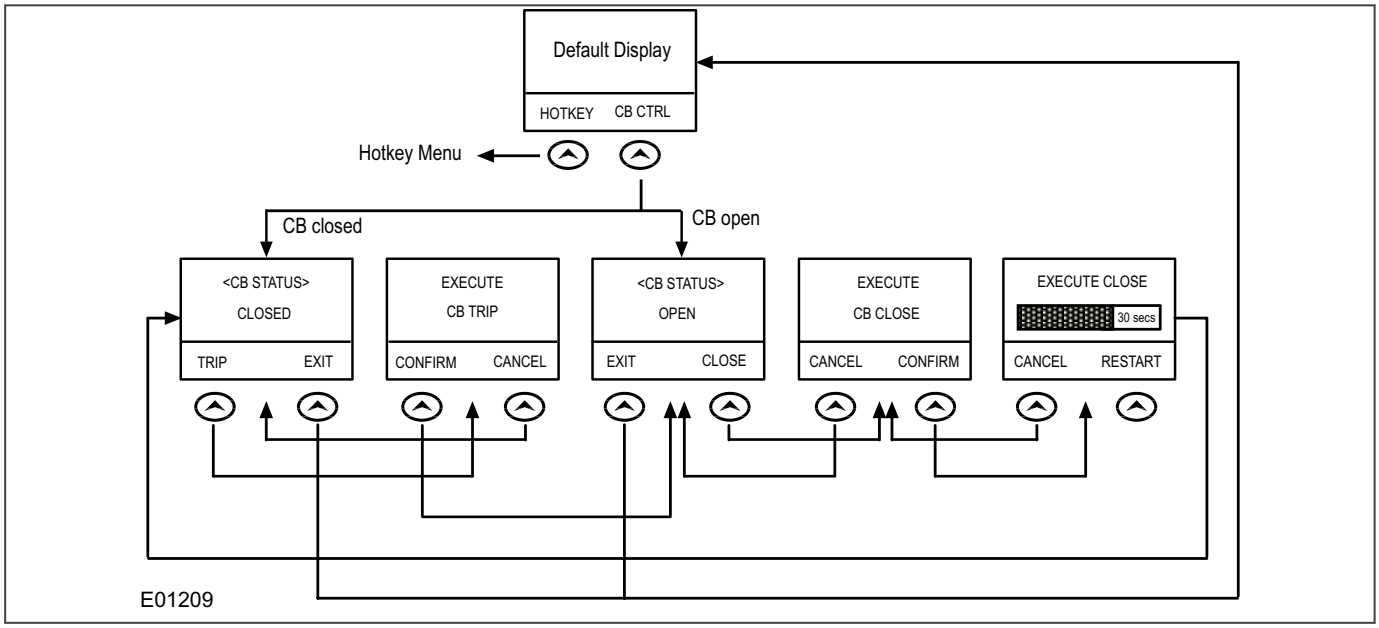



**Figure 241: Hotkey menu navigation**

## 17.7.3 CB CONTROL USING THE FUNCTION KEYS

For most models, you can also use the function keys to allow direct control of the circuit breaker. This has the advantage over hotkeys, that the LEDs associated with the function keys can indicate the status of the CB. The

default PSL is set up such that Function key 2 initiates a trip and Function key 3 initiates a close. For this to work you have to set the CB control by cell to option 5 *Opto+Local*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

As shown below, function keys 2 and 3 have already been assigned to CB control in the default PSL.

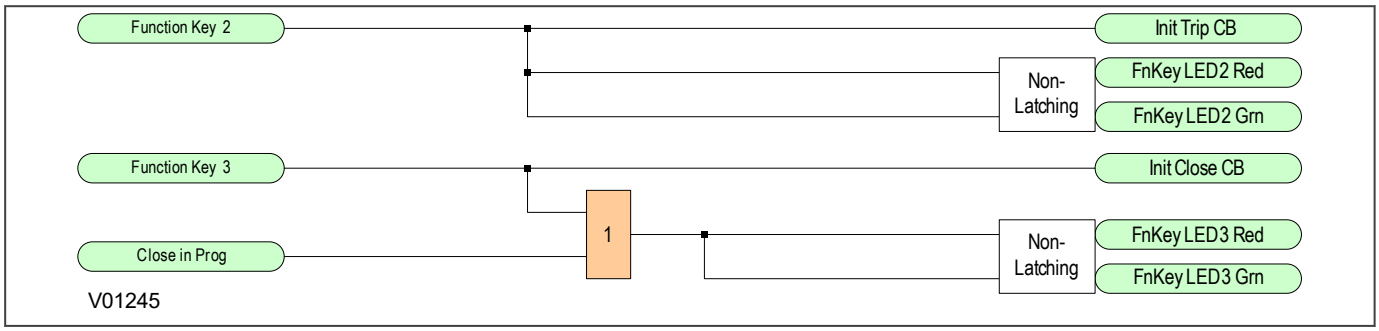



**Figure 242: Default function key PSL**

The programmable function key LEDs have been mapped such that they will indicate yellow whilst the keys are activated.

*Note:*
*Not all models provide function keys.*

## 17.7.4 CB CONTROL USING THE OPTO-INPUTS

Certain applications may require the use of push buttons or other external signals to control the various CB control operations. It is possible to connect such push buttons and signals to opto-inputs and map these to the relevant DDB signals.

For this to work, you have to set the ***CB control by*** cell to option 4 *opto*, option 5 *Opto+Local*, option 6 *Opto +Remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

## 17.7.5 REMOTE CB CONTROL

Remote CB control can be achieved by setting the ***CB Trip/Close*** cell in the *SYSTEM DATA* column to trip or close by using a command over a communication link.

For this to work, you have to set the ***CB control by*** cell to option 2 *Remote*, option 3 *Local+Remote*, option 6 *Opto+remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

We recommend that you allocate separate relay output contacts for remote CB control and protection tripping. This allows you to select the control outputs using a simple local/remote selector switch as shown below. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

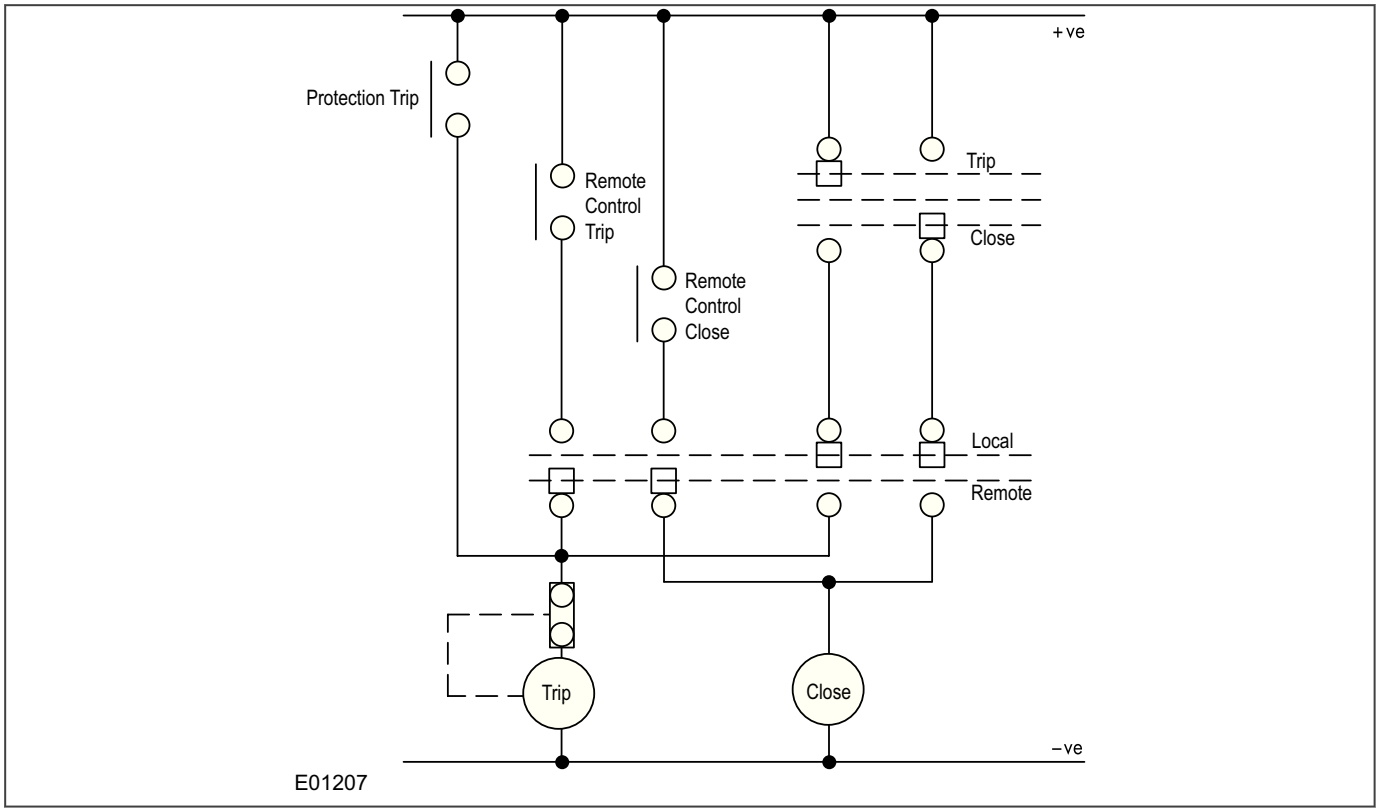



**Figure 243: Remote Control of Circuit Breaker**

## 17.7.6 CB HEALTHY CHECK

A CB Healthy check is available if required. This facility accepts an input to one of the opto-inputs to indicate that the breaker is capable of closing (e.g. that it is fully charged). A time delay can be set with the setting ***CB Healthy Time***. If the CB does not indicate a healthy condition within the time period following a Close command, the device will lockout and alarm.

## 17.7.7 SYNCHRONISATION CHECK

Where the check synchronism function is set, this can be enabled to supervise manual circuit breaker Close commands. A circuit breaker Close command will only be issued if the Check Synchronisation criteria are satisfied. A time delay can be set with the setting ***Sys Check time.*** If the Check Synchronisation criteria are not satisfied within the time period following a Close command the device will lockout and alarm.

## 17.7.8 CB CONTROL AR IMPLICATIONS

An ***Auto Close CB*** signal from the Auto-close logic bypasses the ***Man Close Delay*** time, and the ***CB Close*** output operates immediately to close the circuit breaker.

If Autoreclose is used it may be desirable to block its operation when performing a manual close. In general, the majority of faults following a manual closure are permanent faults and it is undesirable to allow automatic reclosure.

To ensure that Autoreclose is not initiated for a manual circuit breaker closure on to a pre-existing fault, the ***CB IS Time*** (circuit breaker in service time) setting in the *AUTORECLOSE* menu should be set for the desired time window. This setting ensures that Autoreclose initiation is inhibited for a period equal to setting ***CB IS Time*** following a manual circuit breaker closure. If a protection operation occurs during the inhibit period, Autoreclose is not initiated.

Following manual circuit breaker closure, if either a single phase or a three phase fault occur, the circuit breaker is tripped three phase, but Autoreclose is not locked out for this condition.

## 17.7.9 CB CONTROL LOGIC DIAGRAM

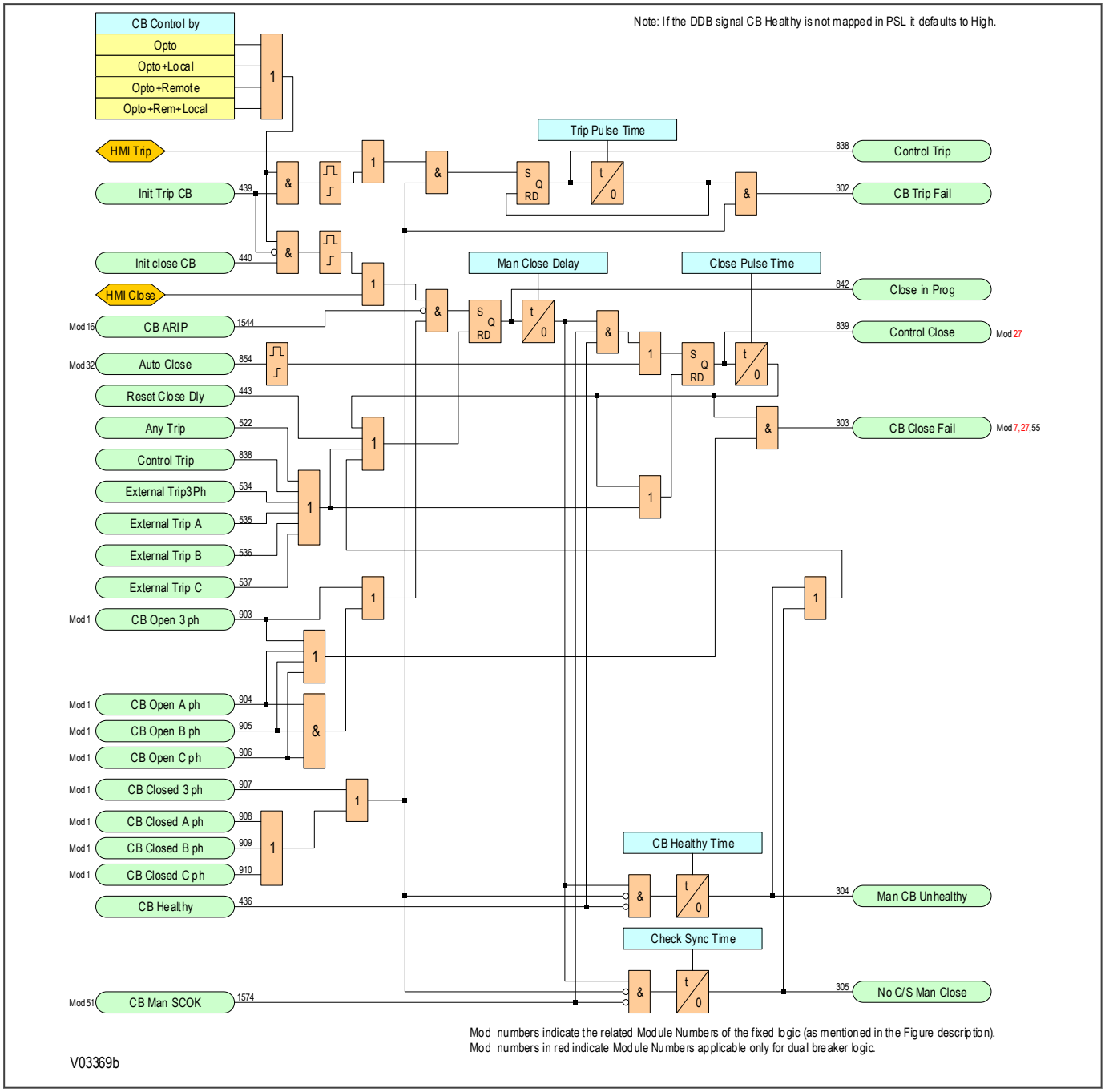



**Figure 244: CB Control logic diagram (Module 43)**

# 17.8 POLE DEAD FUNCTION

The Pole Dead Logic is used to determine and indicate that one or more phases of the line are not energised. A Pole Dead condition is determined either by measuring:

- the line currents and/or voltages, or
- by monitoring the status of the circuit breaker auxiliary contacts, as shown by dedicated DDB signals.

It can also be used to block operation of underfrequency and undervoltage elements where applicable.

## 17.8.1 POLE DEAD LOGIC

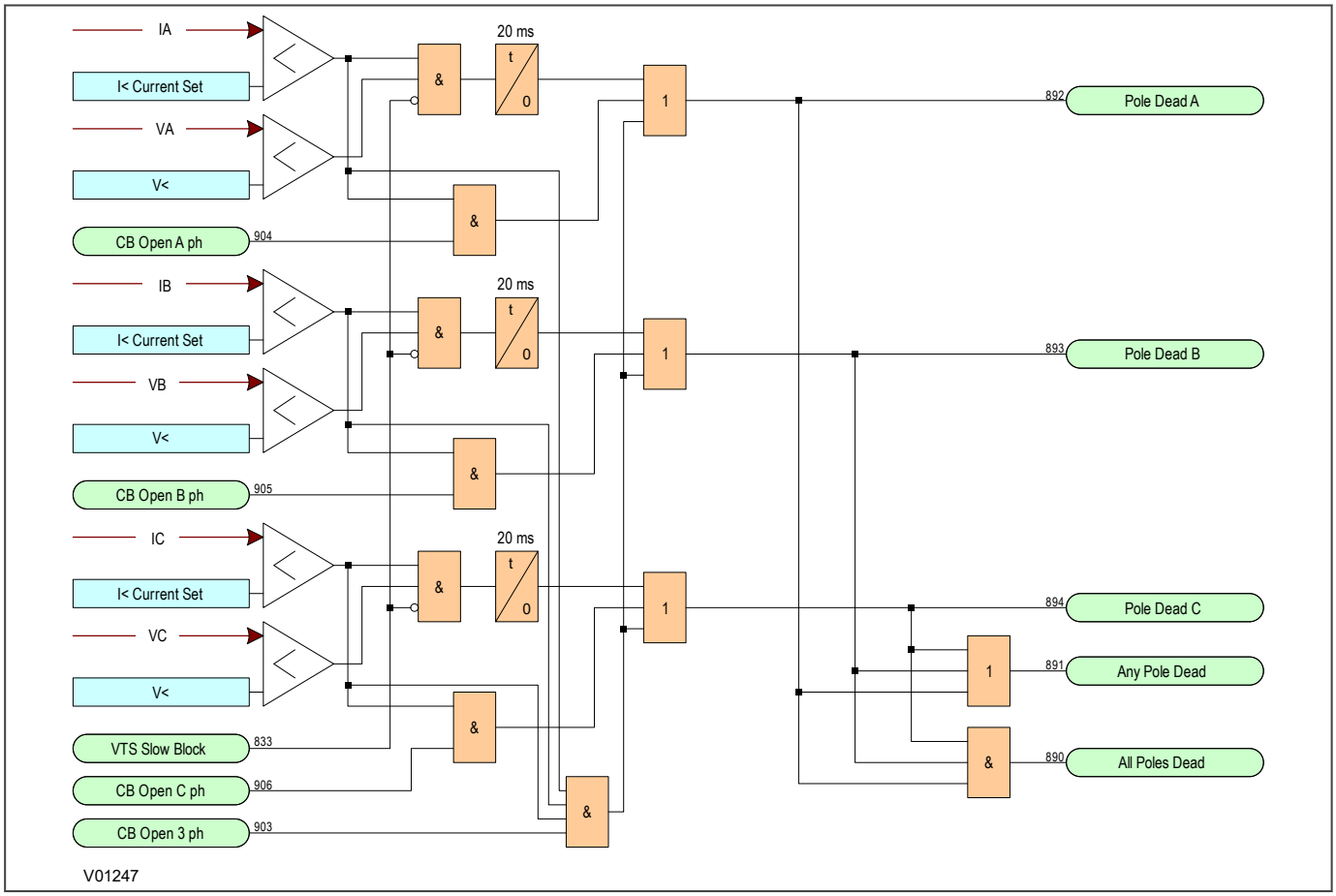



**Figure 245: Pole Dead logic**

If both the line current and voltage values fall below a certain threshold, or a CB Open condition is asserted from the state control logic, the device initiates a Pole Dead condition. The current and voltage thresholds can be set with the ***I< Current Set*** and the ***V< settings*** respectively, in the *CBFAIL&P.DEAD* column.

If one or more poles are dead, the device indicates which phase is dead and asserts the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal is accompanied by the ***All Poles Dead*** signal.

If the VT fails, a ***VTS Slow Block*** signal is taken from the VTS logic to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds.

*Note:*
*If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the IED for a correct pole dead indication.*

## 17.9 SYSTEM CHECKS

In some situations it is possible for both "bus" and "line" sides of a circuit breaker to be live when a circuit breaker is open - for example at the ends of a feeder that has a power source at each end. Therefore, it is normally necessary to check that the network conditions on both sides are suitable, before closing the circuit breaker. This applies to both manual circuit breaker closing and autoreclosing. If a circuit breaker is closed when the line and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to connected machines.

The System Checks functionality involves monitoring the voltages on both sides of a circuit breaker, and if both sides are live, performing a synchronisation check to determine whether any differences in voltage magnitude, phase angle or frequency are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration, and for autoreclosing, on the selected autoreclose program. For example, on a feeder with delayed autoreclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing. The second line end circuit breaker now sees a live bus and a live line.

If there is a parallel connection between the ends of the tripped feeder the frequencies will be the same, but any increased impedance could cause the phase angle between the two voltages to increase. Therefore just before closing the second circuit breaker, it may be necessary to perform a synchronisation check, to ensure that the phase angle between the two voltages has not increased to a level that would cause unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism altogether and the frequency at one end could "slip" relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line-end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

### 17.9.1 SYSTEM CHECKS IMPLEMENTATION

The System Checks function provides *Live/Dead Voltage Monitoring*, two stages of *Check Synchronisation* and *System Split* indication.

The System Checks function is enabled or disabled by the ***System Checks*** setting in the *CONFIGURATION* column. If ***System Checks*** is disabled, the *SYSTEM CHECKS* menu becomes invisible, and a ***SysChks Inactive*** DDB signal is set.

The System Checks functionality can also be enabled or disabled by the ***System Checks*** setting in the *SYSTEM CHECKS* column. For the Systems Checks functionality to be enabled, both the ***System Checks*** setting in the *CONFIGURATION* column AND the ***System Checks*** setting in the *SYSTEM CHECKS* column must be enabled. For the System Checks functionality to be disabled, either the ***System Checks*** setting in the *CONFIGURATION* column OR the ***System Checks*** setting in the *SYSTEM CHECKS* column must be be enabled. In the latter case, the ***SysChks Inactive*** DDB signal is set.

#### 17.9.1.1 VT CONNECTIONS

The device provides inputs for a three-phase "Main VT" and at least one single-phase VT for check synchronisation. Depending on the primary system arrangement, the Main VT may be located on either the line-side of the busbar-side of the circuit breaker, with the Check Sync VT on the other. Normally, the Main VT is located on the line-side (as per the default setting), but this is not always the case. For this reason, a setting is provided where you can define this. This is the ***Main VT Location*** setting, which is found in the *CT AND VT RATIOS* column.

The Check Sync VT may be connected to one of the phase-to-phase voltages or phase-to-neutral voltages. This needs to be defined using the ***CS Input*** setting in the *CT AND VT RATIOS* column. Options are, A-B, B-C, C-A, A-N, B-N, or C-N.

### 17.9.1.2 VOLTAGE MONITORING

The settings in the *VOLTAGE MONITORS* sub-heading in the *SYSTEM CHECKS* column allow you to define the threshold at which a voltage is considered live, and a threshold at which the voltage is considered dead. These thresholds apply to both line and bus sides. If the measured voltage falls below the ***Dead Voltage*** setting, a DDB signal is generated (***Dead Bus***, or ***Dead Line***, depending on which side is being measured). If the measured voltage exceeds the ***Live Voltage*** setting, a DDB signal is generated (***Live Bus***, or ***Live Line***, depending on which side is being measured).

### 17.9.1.3 CHECK SYNCHRONISATION

The device provides two stages of Check Synchronisation. The first stage (CS1) is intended for use in synchronous systems. This means, where the frequencies and phase angles of both sides are compared and if the difference is within set limits, the circuit breaker is allowed to close. The second stage (CS2) is similar to stage, but has an additional adaptive setting. The second stage CS2 is intended for use in asynchronous systems, i.e. where the two sides are out of synchronism and one frequency is slipping continuously with respect to another. If the closing time of the circuit breaker is known, the CB Close command can be issued at a definite point in the cycle such that the CB closes at the point when both sides are in phase.

In situations where it is possible for the voltages on either side of a circuit breaker to be either synchronous or asynchronous, both CS1 and CS2 can be enabled to provide a CB Close signal if either set of permitted closing conditions is satisfied.

Each stage can also be set to inhibit circuit breaker closing if selected blocking conditions such as overvoltage, undervoltage or excessive voltage magnitude difference are detected. CS2 requires the phase angle difference to be decreasing in magnitude before permitting the circuit breaker to close. CS2 has an optional “Adaptive” closing feature, which issues the permissive close signal when the predicted phase angle difference immediately prior to the instant of circuit breaker main contacts closing (i.e. after CB Close time) is as close as practicable to zero.

Slip frequency is the rate of change of phase between each side of the circuit breaker, which is measured by the difference between the voltage signals on either side of the circuit breaker.

Having two system synchronism check stages available allows the circuit breaker closing to be enabled under different system conditions (for example, low slip / moderate phase angle, or moderate slip / small phase angle).

The settings specific to Check Synchronisation are found under the sub-heading *CHECK SYNC* in the *SYSTEM CHECKS* column. The only difference between the CS1 settings and the CS2 settings is that CS2 has a ***CS2 Adaptive*** setting for predictive closure of CB.

### 17.9.1.4 CHECK SYNCRONISATION VECTOR DIAGRAM

The following vector diagram represents the conditions for the System Check functionality. The Dead Volts setting is represented as a circle around the origin whose radius is equal to the maximum voltage magnitude, whereby the voltage can be considered dead. The nominal line voltage magnitude is represented by a circle around the origin whose radius is equal to the nominal line voltage magnitude. The minimum voltage magnitude at which the system can be considered as Live, is the magnitude difference between the bus and line voltages.

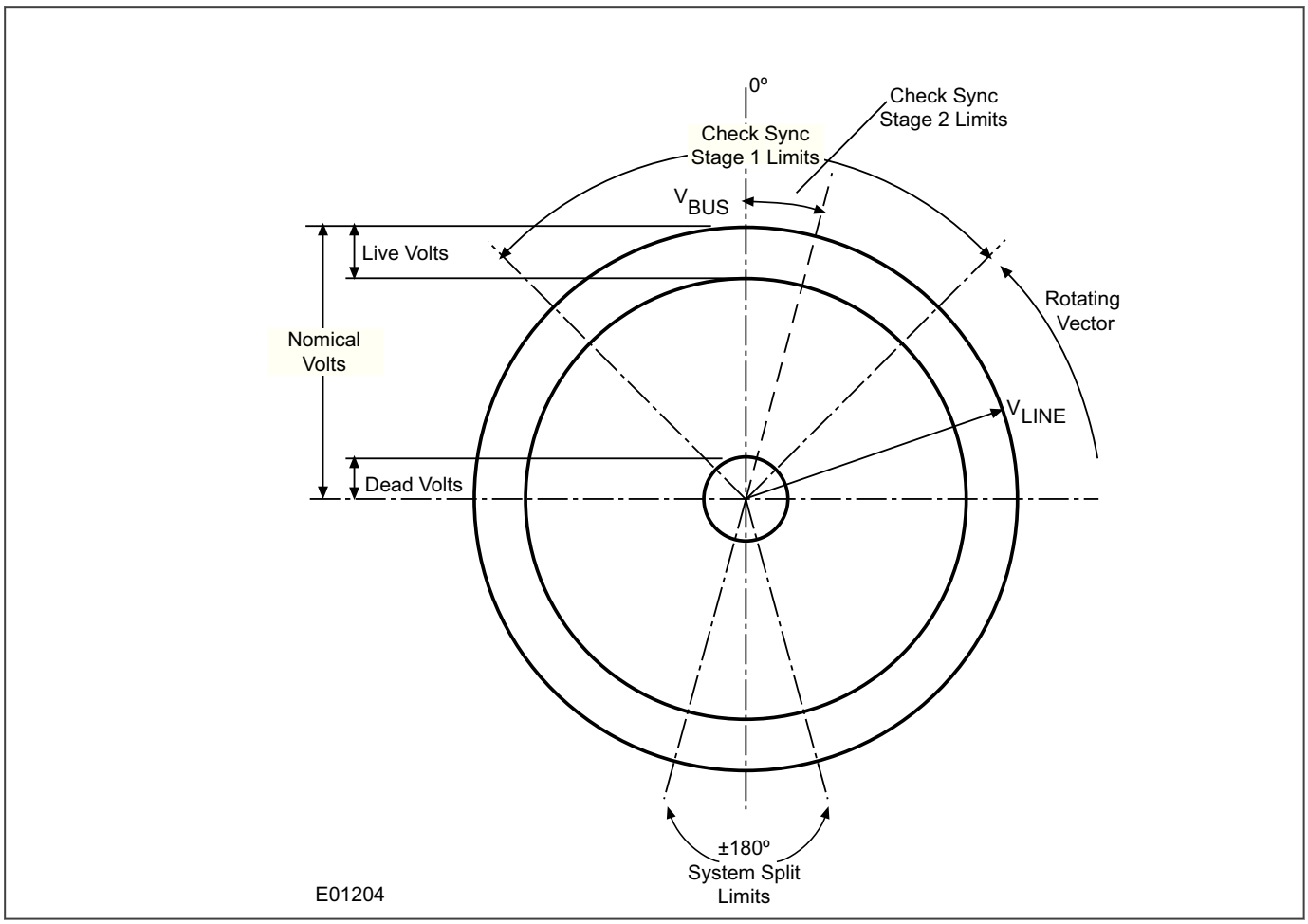



**Figure 246: Check Synchronisation vector diagram**

## 17.9.2 VOLTAGE MONITOR FOR CB CLOSURE

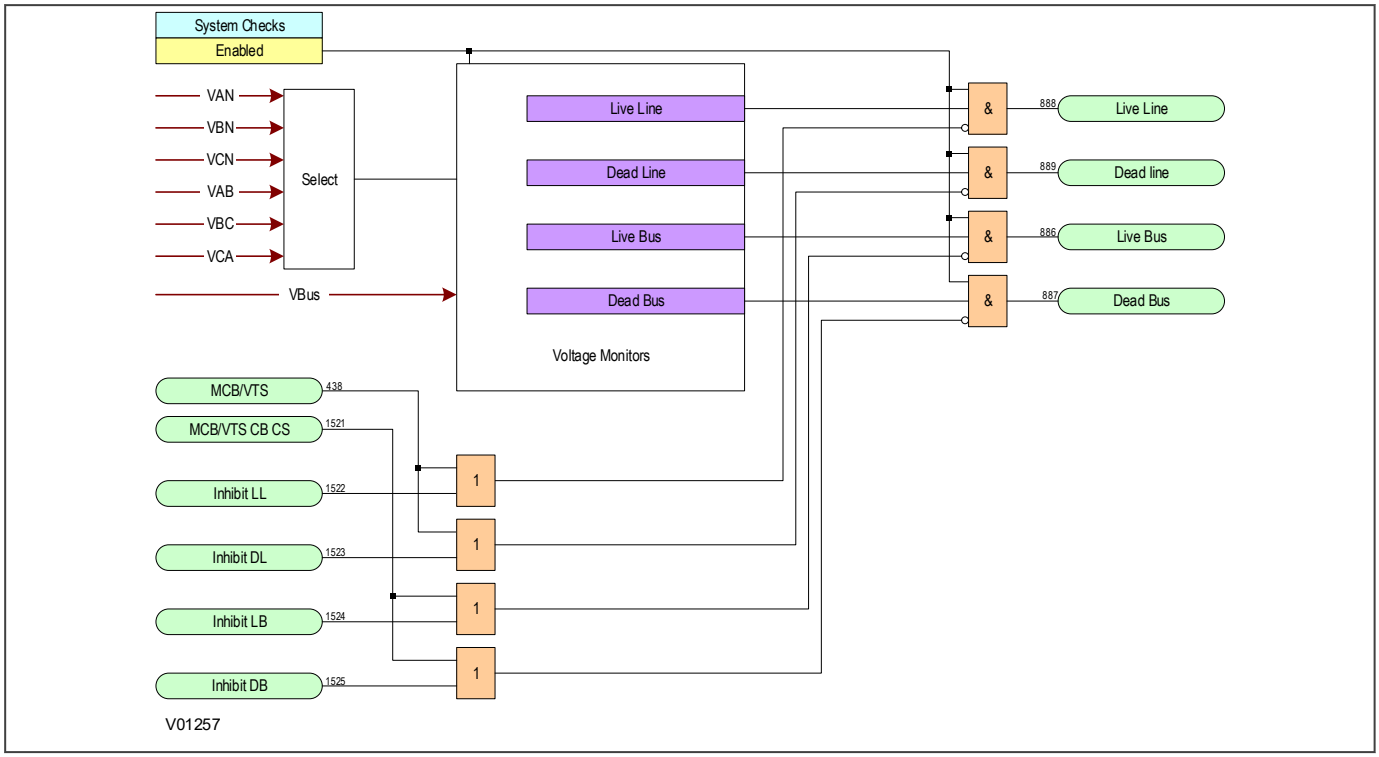



**Figure 247: Voltage Monitor for CB Closure (Module 59)**

## 17.9.3 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

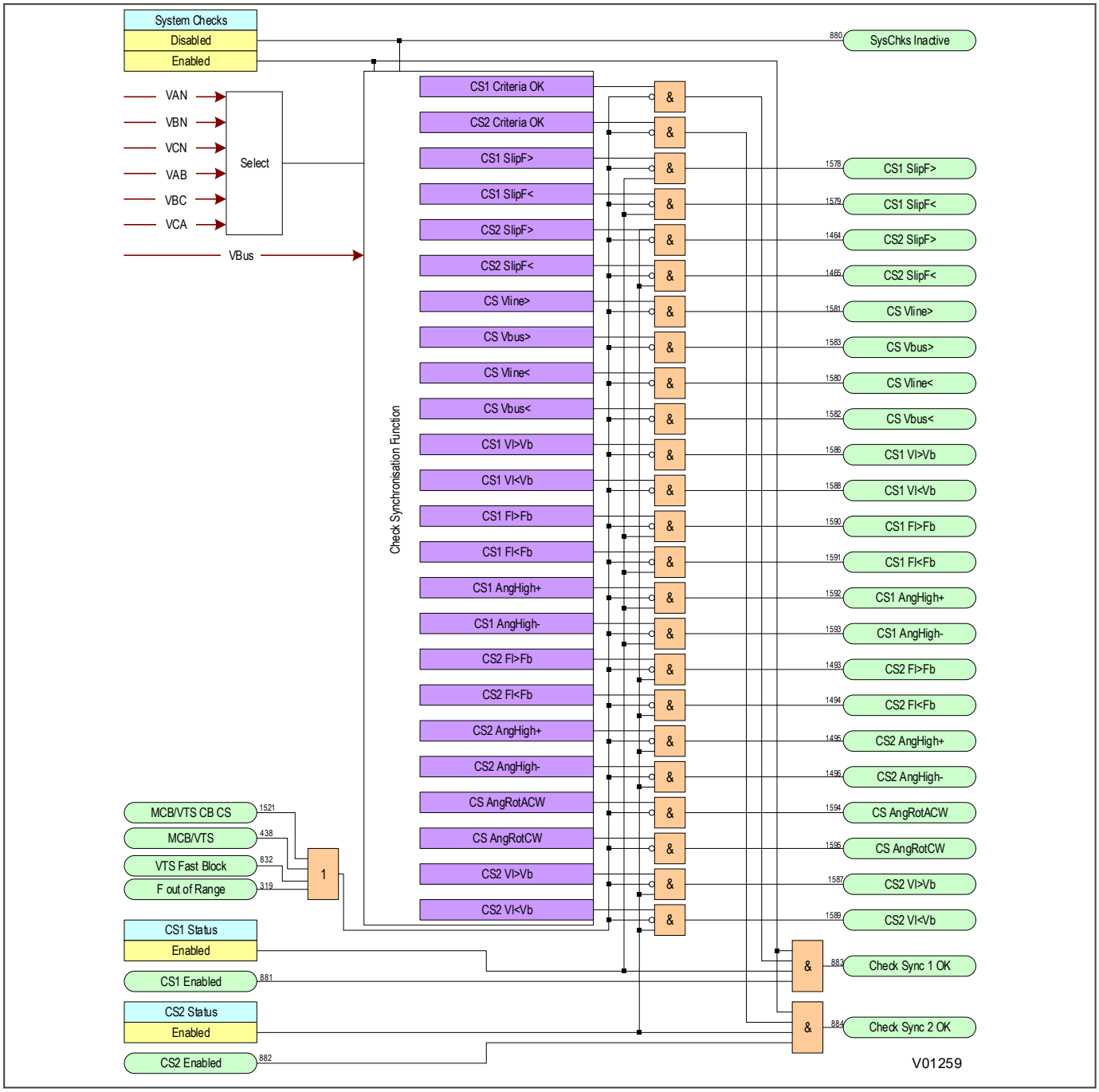



**Figure 248: Check Synchronisation Monitor for CB closure (Module 60)**

## 17.9.4 SYSTEM CHECK PSL

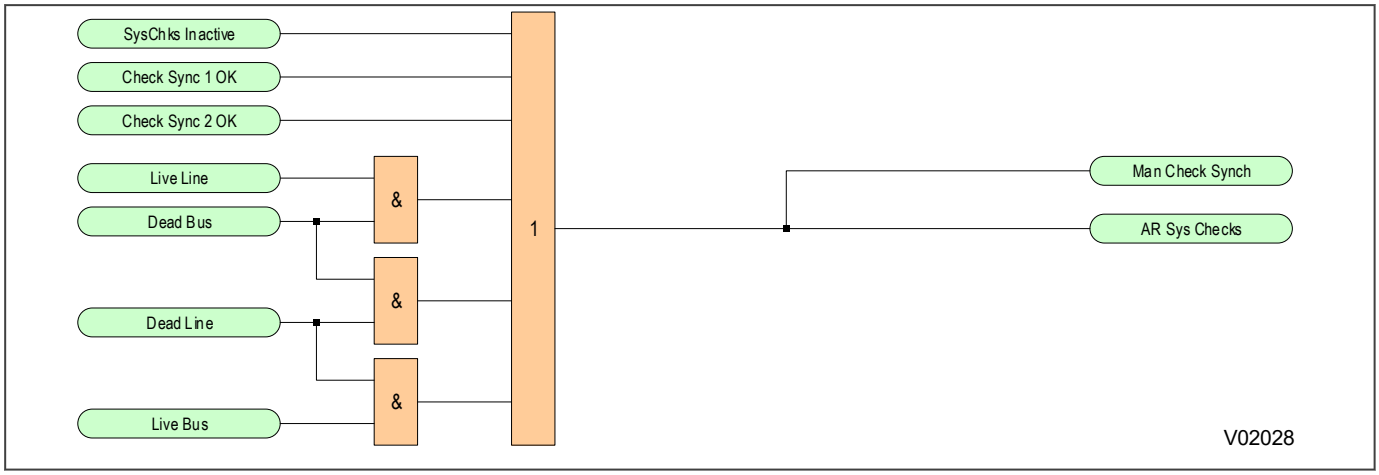



**Figure 249: System Check PSL**

## 17.9.5 APPLICATION NOTES

### 17.9.5.1 PREDICTIVE CLOSURE OF CIRCUIT BREAKER

The ***CS2 Adaptive*** setting compensates for the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 65 Hz.

### 17.9.5.2 VOLTAGE AND PHASE ANGLE CORRECTION

For the Check Synchronisation function, the device needs to convert measured secondary voltages into primary voltages. In some applications, VTs either side of the circuit breaker may have different VT Ratios. In such cases, a magnitude correction factor is required.

There are some applications where the main VT is on the HV side of a transformer and the Check Sync VT is on the LV side, or vice-versa. If the vector group of the transformer is not "0", the voltages are not in phase, so phase correction is also necessary.

The correction factors are as follows and are located in the *CT AND VT RATIOS* column:

- C/S V kSM, where kSM is the voltage correction factor.
- C/S Phase kSA, where kSA is the angle correction factor.

Assuming C/S input setting is A-N, then:

The line and bus voltage magnitudes are matched if $V_{a\ sec} = V_{cs\ sec}$ x C/S V kSA

The line and bus voltage angles are matched if $\angle V_{a\ sec} = \angle V_{cs\ sec}$ + C/S Phase kSA

The following application scenarios show where the voltage and angular correction factors are applied to match different VT ratios:

| Scenario | Physical Ratios (ph-N Values) | | | | Setting Ratios | | | | CS Correction Factors | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Main VT Ratio | | CS VT Ratio | | Main VT Ratio (ph-ph) Always | | CS VT Ratio | | kSM | kSA |
| | Pri (kV) | Sec (V) | Pri (kV) | Sec (V) | Pri (kV) | Sec (V) | Pri (kV) | Sec (V) | | |
| 1 | 220/√3 | 110/√3 | 132/√3 | 100/√3 | 220 | 110 | 132 | 100 | 1.1 | 30º |

| Scenario | Physical Ratios (ph-N Values) | | | | Setting Ratios | | | | CS Correction Factors | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Main VT Ratio | | CS VT Ratio | | Main VT Ratio (ph-ph) Always | | CS VT Ratio | | kSM | kSA |
| | Pri (kV) | Sec (V) | Pri (kV) | Sec (V) | Pri (kV) | Sec (V) | Pri (kV) | Sec (V) | | |
| 2 | 220/√3 | 110/√3 | 220/√3 | 110 | 220 | 110 | 127 | 110 | 0.577 | 0º |
| 3 | 220/√3 | 110/√3 | 220/√3 | 110/3 | 220 | 110 | 381 | 110 | 1.732 | 0º |

# CHAPTER 18

# SUPERVISION

# 18.1 CHAPTER OVERVIEW

This chapter describes the supervison functions.

This chapter contains the following sections:

Chapter Overview 407
Voltage Transformer Supervision 408
Current Transformer Supervision 412
Trip Circuit Supervision 414

## 18.2 VOLTAGE TRANSFORMER SUPERVISION

The Voltage Transformer Supervision (VTS) function is used to detect failure of the AC voltage inputs to the protection. This may be caused by voltage transformer faults, overloading, or faults on the wiring, which usually results in one or more of the voltage transformer fuses blowing.

If there is a failure of the AC voltage input, the IED could misinterpret this as a failure of the actual phase voltages on the power system, which could result in unnecessary tripping of a circuit breaker.

The VTS logic is designed to prevent such a situation by detecting voltage input failures, which are NOT caused by power system phase voltage failure, and automatically blocking associated voltage dependent protection elements. A time-delayed alarm output is available to warn of a VTS condition.

The following scenarios are possible with respect to the failure of the VT inputs.

- Loss of one or two-phase voltages
- Loss of all three-phase voltages under load conditions
- Absence of three-phase voltages upon line energisation

### 18.2.1 LOSS OF ONE OR TWO PHASE VOLTAGES

If the power system voltages are healthy, no Negative Phase Sequence (NPS) current will be present. If however, one or two of the AC voltage inputs are missing, there will be Negative Phase Sequence voltage present, even if the actual power system phase voltages are healthy. VTS works by detecting Negative Phase Sequence (NPS) voltage without the presence of Negative Phase Sequence current. So if there is NPS voltage present, but no NPS current, it is certain that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

The Negative Sequence VTS Element is blocked by the ***Any Pole Dead*** DDB signal during ***SP AR Dead Time***. The resetting of the blocking signal is delayed by 240 ms after an ***Any Pole Dead*** condition disappears.

### 18.2.2 LOSS OF ALL THREE PHASE VOLTAGES

If all three voltage inputs are lost, there will be no Negative Phase Sequence quantities present, but the device will see that there is no voltage input. If this is caused by a power system failure, there will be a step change in the phase currents. However, if this is not caused by a power system failure, there will be no change in any of the phase currents. So if there is no measured voltage on any of the three phases and there is no change in any of the phase currents, this indicates that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation.

To avoid blocking VTS due to changing load condition, the superimposed current signal can only prevent operation of the VTS during the time window of 40 ms following the voltage collapse.

### 18.2.3 ABSENCE OF ALL THREE PHASE VOLTAGES ON LINE ENERGISATION

On line energisation there should be a change in the phase currents as a result of loading or line charging current. Under this condition we need an alternative method of detecting three-phase VT failure.

If there is no measured voltage on all three phases during line energisation, two conditions might apply:

- A three-phase VT failure
- A three-phase fault.

The first condition would require VTS to block the voltage-dependent functions.

In the second condition, voltage dependent functions should not be blocked, as tripping is required.

To differentiate between these two conditions an overcurrent level detector is used (***VTS I> Inhibit***). This prevents a VTS block from being issued in case of a genuine fault. This overcurrent level detector is only enabled for 240 ms following line energization (based on an ***All Poles Dead*** signal drop off). It must still be set below any three-phase fault along the line.

If the line is closed where a three-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

## 18.2.4 VTS IMPLEMENTATION

VTS is implemented in the *SUPERVISION* column of the relevant settings group.

The following settings are relevant for VT Supervision:

- ***VTS Mode***: determines the mode of operation (Measured + MCB, Measured Only, MCB Only)
- ***VTS Status***: determines whether the VTS Operate output will be a blocking output or an alarm indication only
- ***VTS Reset Mode***: determines whether the Reset is to be manual or automatic
- ***VTS Time Delay***: determines the operating time delay
- ***VTS I> Inhibit***: inhibits VTS operation in the case of a phase overcurrent fault
- ***VTS I2> Inhibit***: inhibits VTS operation in the case of a negative sequence overcurrent fault

For faults with I2 less than the setting ***VTS I2 Inhibit***, VTS will be active and block the associated functions if sufficient V2 is measured. VTS is only enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions.

### Thresholds

The negative sequence thresholds used by the element are:

- V2 = 10 V (fixed)
- I2 = 0.05 to 0.5 In settable (default 0.05 In).

The phase voltage level detectors are:

- Drop off = 10 V (fixed)
- Pickup = 30 V (fixed)

The sensitivity of the superimposed current elements is fixed at 0.1 In.

### Fuse Fail

The device includes a setting (***VT Connected*** ) in the *CT AND VT RATIOS* column, which determines whether there are voltage transformers connected to it. If set to `No`, this setting has no effect.

If set to `No` it causes the VTS logic to set the ***VTS Slow Block*** and ***VTS Fast Block*** DDBs, but not raise any alarms. It also disables the VTS function. This prevents the pole dead logic working incorrectly if there is no voltage or current. It also blocks the distance, under voltage and other voltage-dependant functions. However, it does not affect the CB open part of the logic.

A VTS condition can be raised by a mini circuit breaker (MCB) status input, by internal logic using IED measurement, or both. The setting ***VTS Mode*** is used to select the method of indicating VT failure.

## 18.2.5 VTS LOGIC

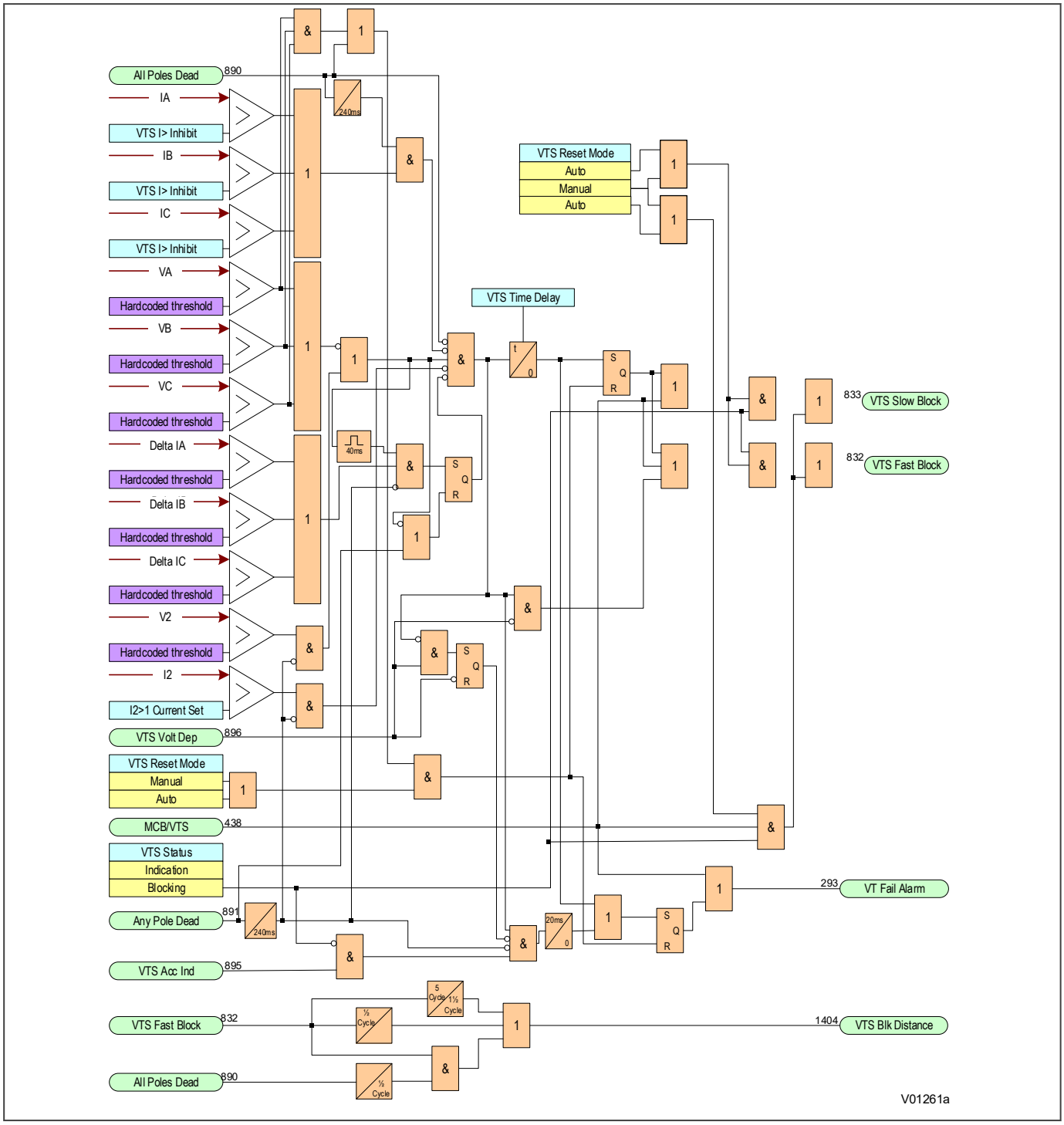



**Figure 250: VTS logic**

The IED may respond as follows, on operation of any VTS element:

- VTS set to provide alarm indication only
- Optional blocking of voltage-dependent protection elements
- Optional conversion of directional overcurrent elements to non-directional protection (by setting the relevant current protection status cells to *Enabled VTS*. In this case, the directional setting cells are automatically set to *non-directional*.)

The ***VTS I> Inhibit*** or ***VTS I2> Inhibit*** elements are used to override a VTS block if a fault occurs that could trigger the VTS logic. However, once the VTS block is set, subsequent system faults must not override the block. Therefore the VTS block is latched after a settable time delay (***VTS Time Delay***). Once the signal has latched, there are two methods of resetting. The first is manually using the front panel HMI, or remote communications (if the VTS condition has been removed). The second is in Auto mode, by restoring the 3 phase voltages above the phase level detector settings mentioned previously.

***VTS Status*** can be set to *Disabled*, *Blocking* or *Indication*. If ***VTS Status*** is set to *Blocking*, a VTS condition will block operation of the relevant protection elements. In this case, a VTS indication is given after the ***VTS Time Delay*** has expired. If it is set to *Indication*, their is a risk of maloperation because protection elements are not blocked. In this case the VTS indication is given before the ***VTS Time Delay*** expires, if a trip signal is given (in this case a signal from the VTS acceleration logic is used as an input).

This scheme also operates correctly under very low load or even no load conditions. To achieve this, it uses a combination of time delayed signals derived from the DDB signals ***VTS Fast Block*** and ***All Poles Dead***, to generate the distance blocking DDB signal called ***VTS Blk Distance.***

*Note:*
*All non-distance voltage-dependent elements are blocked by the **VTS Fast Block** DDB.*

If a miniature circuit breaker (MCB) is used to protect the voltage transformer output circuits, MCB auxiliary contacts can be used to indicate a three-phase output disconnection. It is possible for the VTS logic to operate correctly without this input, but this facility has been provided to maintain compatibility with some practises. Energising an opto-isolated input assigned to the ***MCB/VTS*** provides the necessary block.

The VTS function is inhibited if:

- An ***All Poles Dead*** DDB signal is present
- Any phase overcurrent condition exists
- A Negative Phase Sequence current exists
- If the phase current changes over the period of 1 cycle

# 18.3 CURRENT TRANSFORMER SUPERVISION

The Current Transformer Supervision function (CTS) is used to detect failure of the AC current inputs to the protection. This may be caused by internal current transformer faults, overloading, or faults on the wiring. If there is a failure of the AC current input, the protection could misinterpret this as a failure of the actual phase currents on the power system, which could result in maloperation. Also, an open circuit in the AC current circuits can cause dangerous CT secondary voltages to be generated.

## 18.3.1 CTS IMPLEMENTATION

If the power system currents are healthy, no zero sequence voltage are derived. However, if one or more of the AC current inputs are missing, a zero sequence current would be derived, even if the actual power system phase currents are healthy. Standard CTS works by detecting a derived zero sequence current where there is no corresponding derived zero sequence voltage.

The voltage transformer connection used must be able to refer zero sequence voltages from the primary to the secondary side. Therefore, this element should only be enabled where the VT is of a five-limb construction, or comprises three single-phase units with the primary star point earthed.

The CTS function is implemented in the *SUPERVISION* column of the relevant settings group, under the sub-heading *CT SUPERVISION*.

The following settings are relevant for CT Supervision:

- ***CTS Status***: to disable or enable CTS
- ***CTS VN< Inhibit***: inhibits CTS if the zero sequence voltage exceeds this setting
- ***CTS IN> Set***: determines the level of zero sequence current
- ***CTS Time Delay***: determines the operating time delay

## 18.3.2 STANDARD CTS LOGIC

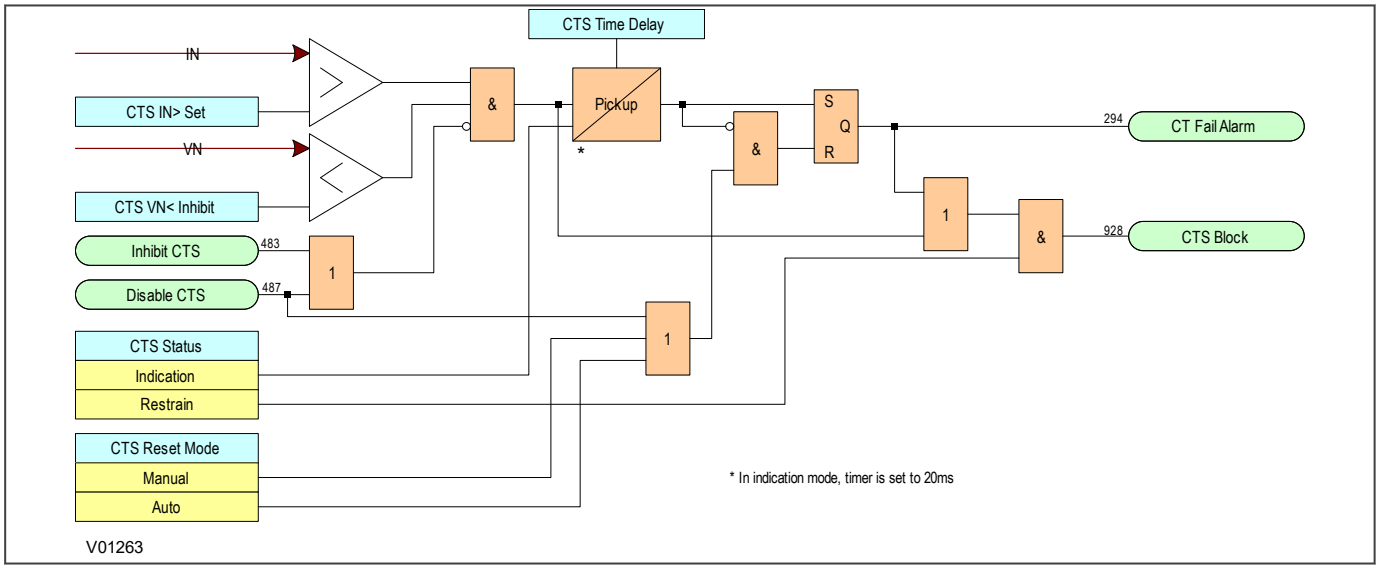



**Figure 251: Standard CTS**

## 18.3.3 CTS BLOCKING

Both the standard and differential CTS methods block protection elements operating from derived quantities, such as Broken conductor, derived earth fault and negative sequence overcurrent. Measured quantities such as DEF can be selectively blocked by designing an appropriate PSL scheme.

Differential CTS can be used to restrain the differential protection if required.

## 18.3.4 APPLICATION NOTES

### 18.3.4.1 SETTING GUIDELINES

The residual voltage setting, ***CTS VN< Inhibit*** and the residual current setting, ***CTS IN> Set***, should be set to avoid unwanted operation during healthy system conditions. For example:

- ***CTS VN< Inhibit*** should be set to 120% of the maximum steady state residual voltage.
- ***CTS IN> Set*** will typically be set below minimum load current.
- ***CTS Time Delay*** is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent protection elements being blocked during fault conditions.

## 18.4 TRIP CIRCUIT SUPERVISION

In most protection schemes, the trip circuit extends beyond the IED enclosure and passes through components such as links, relay contacts, auxiliary switches and other terminal boards. Such complex arrangements may require dedicated schemes for their supervision.

There are two distinctly separate parts to the trip circuit; the trip path, and the trip coil. The trip path is the path between the IED enclosure and the CB cubicle. This path contains ancillary components such as cables, fuses and connectors. A break in this path is possible, so it is desirable to supervise this trip path and to raise an alarm if a break should appear in this path.

The trip coil itself is also part of the overall trip circuit, and it is also possible for the trip coil to develop an open-circuit fault.

This product supports a number of trip circuit supervision (TCS) schemes.

### 18.4.1 TRIP CIRCUIT SUPERVISION SCHEME 1

This scheme provides supervision of the trip coil with the CB open or closed, however, it does not provide supervision of the trip path whilst the breaker is open. The CB status can be monitored when a self-reset trip contact is used. However, this scheme is incompatible with latched trip contacts, as a latched contact will short out the opto-input for a time exceeding the recommended Delayed Drop-off (DDO) timer setting of 400 ms, and therefore does not support CB status monitoring. If you require CB status monitoring, further opto-inputs must be used.

*Note:*
*A 52a CB auxiliary contact follows the CB position. A 52b auxiliary contact is the opposite.*

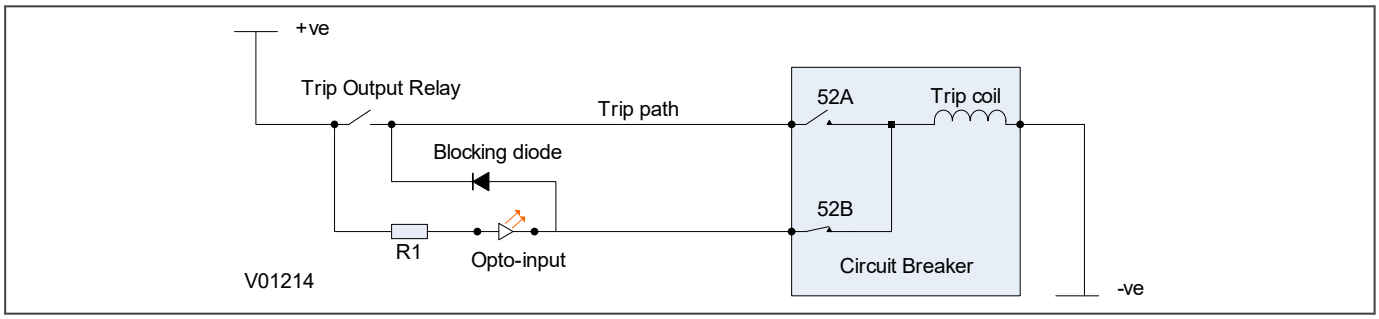



**Figure 252: TCS Scheme 1**

When the CB is closed, supervision current passes through the opto-input, blocking diode and trip coil. When the CB is open, supervision current flows through the opto-input and into the trip coil via the 52b auxiliary contact. This means that *Trip Coil* supervision is provided when the CB is either closed or open, however *Trip Path* supervision is only provided when the CB is closed. No supervision of the trip path is provided whilst the CB is open (pre-closing supervision). Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

#### 18.4.1.1 RESISTOR VALUES

The supervision current is a lot less than the current required by the trip coil to trip a CB. The opto-input limits this supervision current to less than 10 mA. If the opto-input were to be short-circuited however, it could be possible for the supervision current to reach a level that could trip the CB. For this reason, a resistor R1 is often used to limit the current in the event of a short-circuited opto-input. This limits the current to less than 60mA. The table below shows the appropriate resistor value and voltage setting for this scheme.

| Trip Circuit Voltage | Opto Voltage Setting with R1 Fitted | Resistor R1 (ohms) |
|---|---|---|
| 48/54 | 24/27 | 1.2k |
| 110/125 | 48/54 | 2.7k |
| 220/250 | 110/125 | 5.2k |

**Warning:**
**This Scheme is not compatible with Trip Circuit voltages of less than 48 V.**

#### 18.4.1.2 PSL FOR TCS SCHEME 1

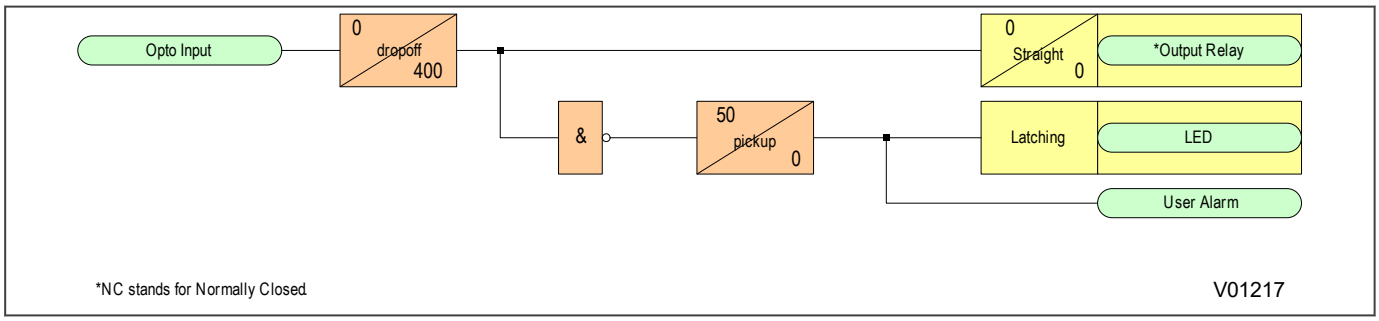



**Figure 253: PSL for TCS Scheme 1**

The opto-input can be used to drive a Normally Closed Output Relay, which in turn can be used to drive alarm equipment. The signal can also be inverted to drive a latching programmable LED and a user alarm DDB signal.

The DDO timer operates as soon as the opto-input is energised, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto-input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the power up time, following a voltage supply interruption.

### 18.4.2 TRIP CIRCUIT SUPERVISION SCHEME 2

This scheme provides supervision of the trip coil with the breaker open or closed but does not provide pre-closing supervision of the trip path. However, using two opto-inputs allows the IED to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning one opto-input to the 52a contact and another opto-input to the 52b contact. Provided the ***CB Status*** setting in the *CB CONTROL* column is set to `Both 52A and 52B`, the IED will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

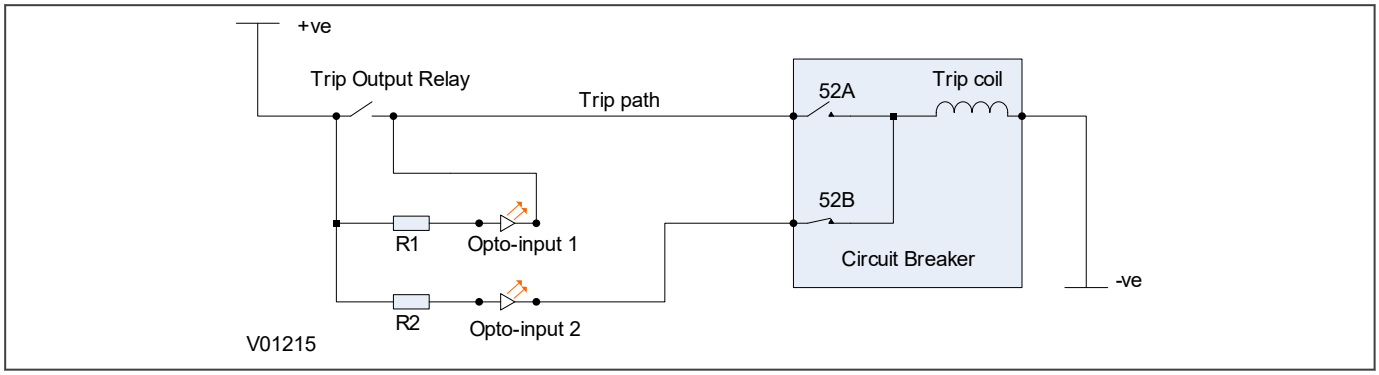



**Figure 254: TCS Scheme 2**

When the breaker is closed, supervision current passes through opto input 1 and the trip coil. When the breaker is open current flows through opto input 2 and the trip coil. No supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

### 18.4.2.1 RESISTOR VALUES

Optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto-input is shorted. The table below shows the appropriate resistor value and voltage setting for this scheme.

| Trip Circuit Voltage | Opto Voltage Setting with R1 Fitted | Resistor R1 and R2 (ohms) |
|---|---|---|
| 48/54 | 24/27 | 1.2k |
| 110/125 | 48/54 | 2.7k |
| 220/250 | 110/125 | 5.2k |

**Warning:**
**This Scheme is not compatible with Trip Circuit voltages of less than 48 V.**

### 18.4.2.2 PSL FOR TCS SCHEME 2

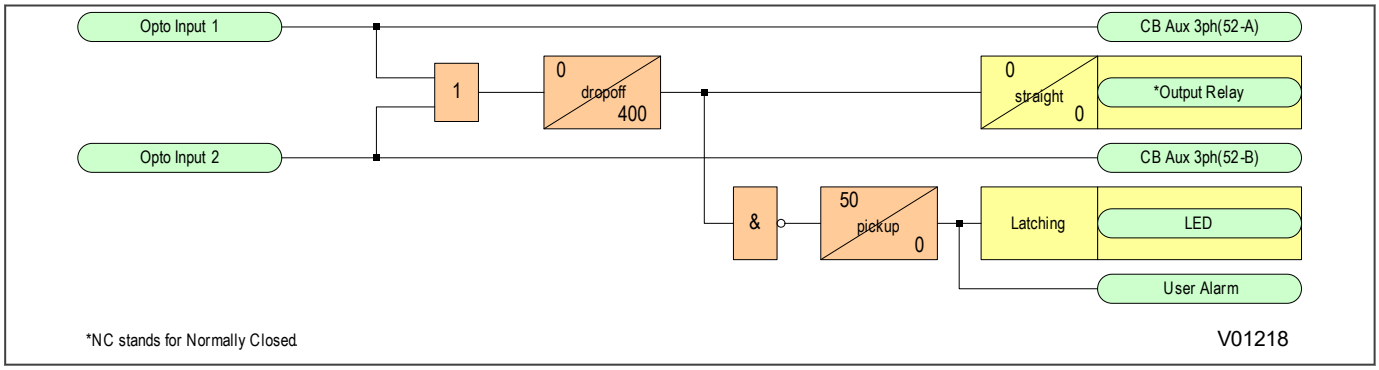



**Figure 255: PSL for TCS Scheme 2**

In TCS scheme 2, both opto-inputs must be low before a trip circuit fail alarm is given.

## 18.4.3 TRIP CIRCUIT SUPERVISION SCHEME 3

TCS Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed. It provides pre-closing supervision of the trip path. Since only one opto-input is used, this scheme is not compatible with latched trip contacts. If you require CB status monitoring, further opto-inputs must be used.

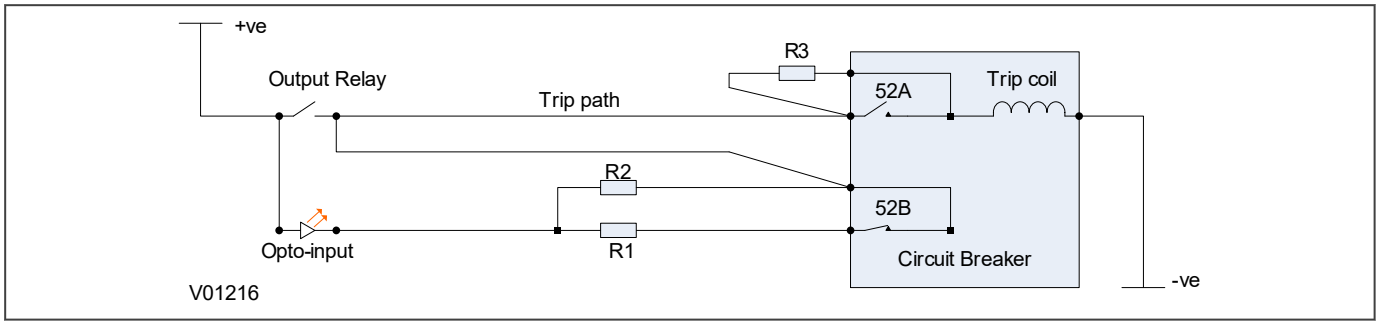



**Figure 256: TCS Scheme 3**

When the CB is closed, supervision current passes through the opto-input, resistor R2 and the trip coil. When the CB is open, current flows through the opto-input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. The supervision current is maintained through the trip path with the breaker in either state, therefore providing pre-closing supervision.

### 18.4.3.1 RESISTOR VALUES

Resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes. This scheme is dependent upon the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

| Trip Circuit Voltage | Opto Voltage Setting with R1 Fitted | Resistor R1 & R2 (ohms) | Resistor R3 (ohms) |
|---|---|---|---|
| 48/54 | 24/27 | 1.2k | 600 |
| 110/250 | 48/54 | 2.7k | 1.2k |
| 220/250 | 110/125 | 5.0k | 2.5k |

**Warning:**
**This Scheme is not compatible with Trip Circuit voltages of less than 48 V.**

### 18.4.3.2 PSL FOR TCS SCHEME 3

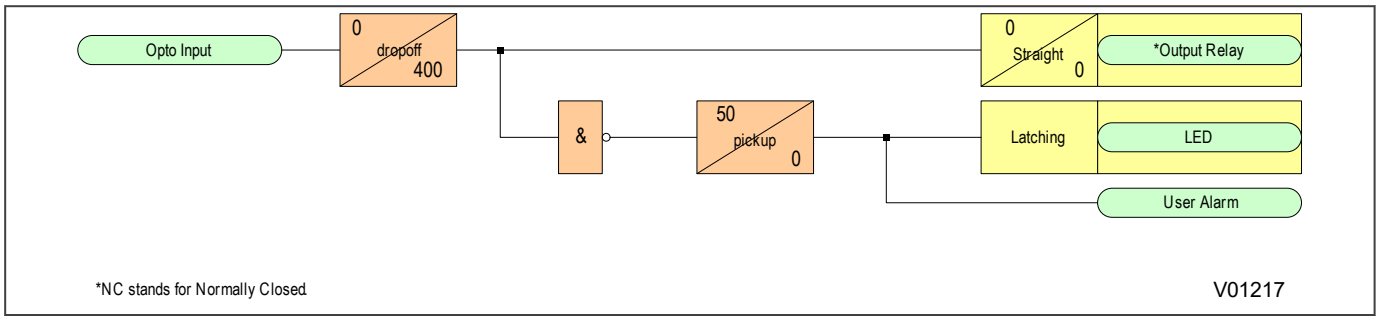



**Figure 257: PSL for TCS Scheme 3**

CHAPTER 19

# DIGITAL I/O AND PSL CONFIGURATION

## 19.1 CHAPTER OVERVIEW

This chapter introduces the PSL (Programmable Scheme Logic) Editor, and describes the configuration of the digital inputs and outputs. It provides an outline of scheme logic concepts and the PSL Editor. This is followed by details about allocation of the digital inputs and outputs, which require the use of the PSL Editor. A separate "Settings Application Software" document is available that gives a comprehensive description of the PSL, but enough information is provided in this chapter to allow you to allocate the principal digital inputs and outputs.

This chapter contains the following sections:

Chapter Overview 419
Configuring Digital Inputs and Outputs 420
Scheme Logic 421
Configuring the Opto-Inputs 423
Assigning the Output Relays 424
Fixed Function LEDs 425
Configuring Programmable LEDs 426
Function Keys 428
Control Inputs 429

## 19.2 CONFIGURING DIGITAL INPUTS AND OUTPUTS

Configuration of the digital inputs and outputs in this product is very flexible. You can use a combination of settings and programmable logic to customise them to your application. You can access some of the settings using the keypad on the front panel, but you will need a computer running the settings application software to fully interrogate and configure the properties of the digital inputs and outputs.

The settings application software includes an application called the PSL Editor (Programmable Scheme Logic Editor). The PSL Editor lets you allocate inputs and outputs according to your specific application. It also allows you to apply attributes to some of the signals such as a drop-off delay for an output contact.

In this product, digital inputs and outputs that are configurable are:

- Optically isolated digital inputs (opto-inputs). These can be used to monitor the status of associated plant.
- Output relays. These can be used for purposes such as initiating the tripping of circuit breakers, providing alarm signals, etc..
- Programmable LEDs. The number and colour of the programmable LEDs varies according to the particular product being applied.
- Function keys and associated LED indications. These are not provided on all products, but where they are, each function key has an associated tri-colour LED.
- IEC 61850 GOOSE inputs and outputs. These are only provided on products that have been specified for connection to an IEC61850 system, and the details of the GOOSE are presented in the documentation on IEC61850.
- InterMiCOM inputs and outputs. These are not used by all products. If your product is equipped with an InterMiCOM feature, you will find details of allocation and configuration in the chapter dedicated to the InterMiCOM function.

## 19.3 SCHEME LOGIC

The product is supplied with pre-loaded Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL).

The Scheme Logic is a functional module within the IED, through which all mapping of inputs to outputs is handled. The scheme logic can be split into two parts; the Fixed Scheme Logic (FSL) and the Programmable Scheme Logic (PSL). It is built around a concept called the digital data bus (DDB). The DDB encompasses all of the digital signals (DDBs) which are used in the FSL and PSL. The DDBs included digital inputs, outputs, and internal signals.

The FSL is logic that has been hard-coded in the product. It is fundamental to correct interaction between various protection and/or control elements. It is fixed and cannot be changed.

The PSL gives you a facility to develop custom schemes to suit your application if the factory-programmed default PSL schemes do not meet your needs. Default PSL schemes are programmed before the product leaves the factory. These default PSL schemes have been designed to suit typical applications and if these schemes suit your requirements, you do not need to take any action. However, if you want to change the input-output mappings, or to implement custom scheme logic, you can change these, or create new PSL schemes using the PSL editor.

The PSL consists of components such as logic gates and timers, which combine and condition DDB signals.

The logic gates can be programmed to perform a range of different logic functions. The number of inputs to a logic gate are not limited. The timers can be used either to create a programmable delay or to condition the logic outputs. Output contacts and programmable LEDs have dedicated conditioners.

The PSL logic is event driven. Only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This minimises the amount of processing time used by the PSL ensuring industry leading performance.

The following diagram shows how the scheme logic interacts with the rest of the IED.

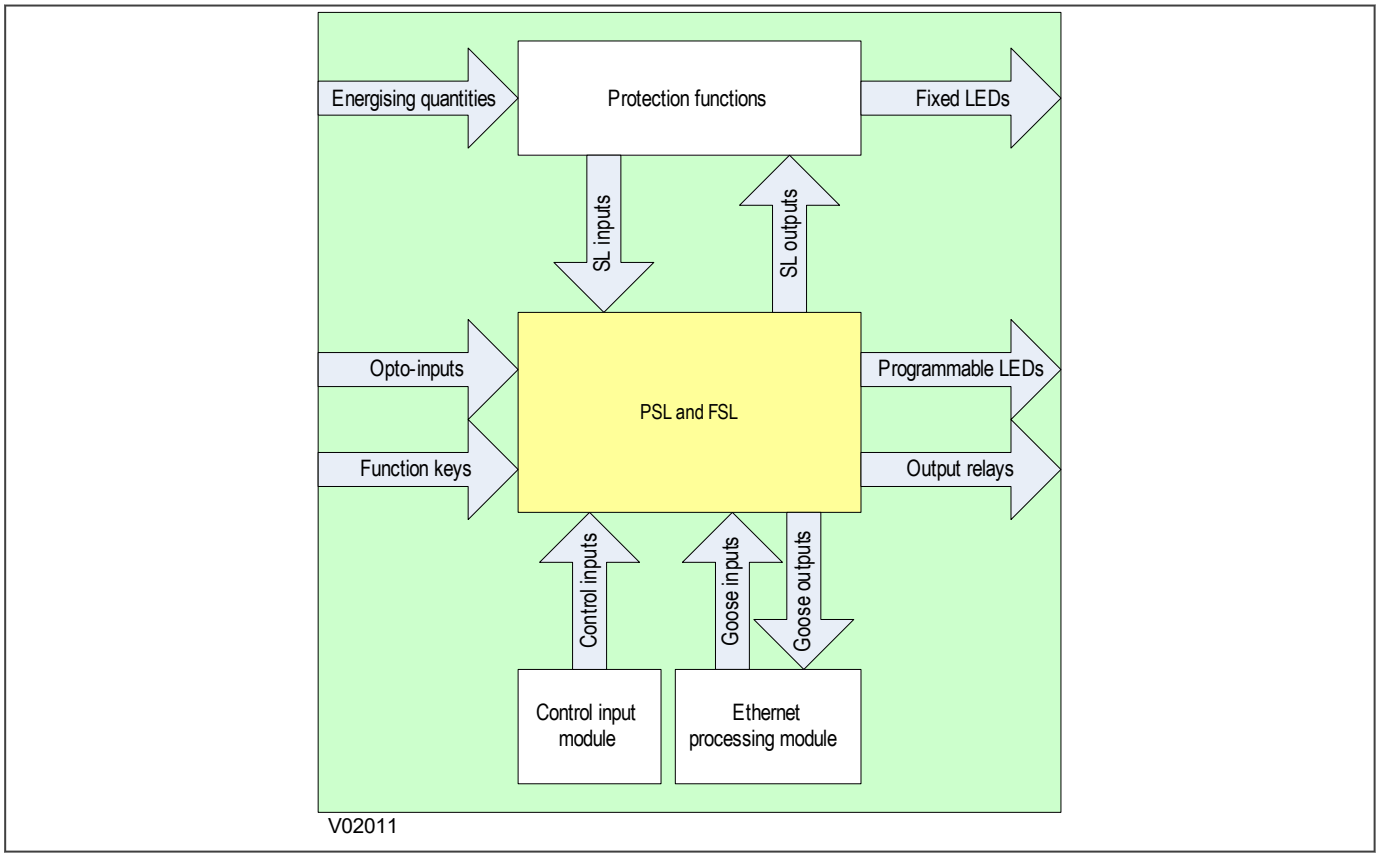



**Figure 258: Scheme Logic Interfaces**

### 19.3.1 PSL EDITOR

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised logic to qualify how the product manages its response to system conditions. The IED's digital inputs are combined with internally generated digital signals using logic gates, timers, and conditioners. The resultant signals are then mapped to digital outputs signals including output relays and LEDs.

The PSL Editor is a tool in the settings application software that allows you to create and edit scheme logic diagrams. You can use the default scheme logic which has been designed to suit most applications, but if it does not suit your application you can change it. If you create a different scheme logic with the software, you need to upload it to the device to apply it.

### 19.3.2 PSL SCHEMES

Your product is shipped with default scheme files. These can be used without modification for most applications, or you can choose to use them as a starting point to design your own scheme. You can also create a new scheme from scratch. To create a new scheme, or to modify an existing scheme, you will need to launch the settings application software. You then need to open an existing PSL file, or create a new one, for the particular product that you are using, and then open a PSL file. If you want to create a new PSL file, you should select **File** then **New** then **Blank scheme...** This action opens a default file appropriate for the device in question, but deletes the diagram components from the default file to leave an empty diagram with configuration information loaded. To open an existing file, or a default file, simply double-click on it.

### 19.3.3 PSL SCHEME VERSION CONTROL

To help you keep track of the PSL loaded into products, a version control feature is included. The user interface contains a *PSL DATA* column, which can be used to track PSL modifications. A total of 12 cells are contained in the *PSL DATA* column; 3 for each setting group.

***Grp(n) PSL Ref***: When downloading a PSL scheme to an IED, you will be prompted to enter the relevant group number and a reference identifier. The first 32 characters of the reference identifier are displayed in this cell. The horizontal cursor keys can scroll through the 32 characters as the LCD display only displays 16 characters.

**Example:**

```
Grp(n) PSL Ref
```

***Date/time***: This cell displays the date and time when the PSL scheme was downloaded to the IED.

**Example:**

```
18 Nov 2002
08:59:32.047
```

***Grp(n) PSL ID***: This cell displays a unique ID number for the downloaded PSL scheme.

**Example:**

```
Grp(n) PSL ID
ID - 2062813232
```

## 19.4 CONFIGURING THE OPTO-INPUTS

The number of optically isolated status inputs (opto-inputs) depends on the specific model supplied. The use of the inputs will depend on the application, and their allocation is defined in the programmable scheme logic (PSL). In addition to the PSL assignment, you also need to specify the expected input voltage. Generally, all opto-inputs will share the same input voltage range, but if different voltage ranges are being used, this device can accommodate them.

In the *OPTO CONFIG* column there is a global nominal voltage setting. If all opto-inputs are going to be energised from the same voltage range, you select the appropriate value in the setting. If you select `Custom` in the setting, then the cells ***Opto Input 1***, ***Opto Input 2***, etc. become visible. You use these cells to set the voltage ranges for each individual opto-input.

Within the *OPTO CONFIG* column there are also settings to control the filtering applied to the inputs, as well as the pick-up/drop-off characteristic.

The filter control setting provides a bit string with a bit associated with all opto-inputs. Setting the bit to '1' means that a half-cycle filter is applied to the inputs. This helps to prevent incorrect operation in the event of power system frequency interference on the wiring. Setting the field to '0' removes the filter and provides for faster operation.

The ***Characteristic*** setting is a single setting that applies to all the opto-inputs. It is used to set the pick-up/drop-off ratios of the input signals. As standard it is set to 80% pick-up and 60% drop-off, but you can change it to other available thresholds if that suits your operational requirements.

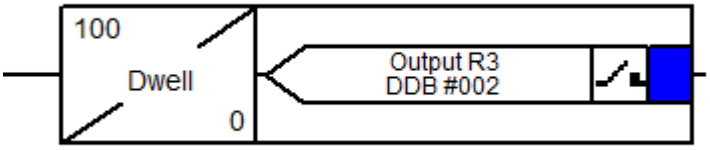
## 19.5 ASSIGNING THE OUTPUT RELAYS

Relay contact action is controlled using the PSL. DDB signals are mapped in the PSL and drive the output relays. The driving of an output relay is controlled by means of a relay output conditioner. Several choices are available for how output relay contacts are conditioned. For example, you can choose whether operation of an output relay contact is latched, has delay on pick-up, or has a delay on drop-off. You make this choice in the **Contact Properties** window associated with the output relay conditioner.

To map an output relay in the PSL you should use the Contact Conditioner button in the toolbar to import it. You then condition it according to your needs. The output of the conditioner respects the attributes you have assigned.

The toolbar button for a Contact Conditioner looks like this:

The PSL contribution that it delivers looks like this:




*Note:*
*Contact Conditioners are only available if they have not all been used. In some default PSL schemes, all Contact Conditioners might have been used. If that is the case, and you want to use them for something else, you will need to re-assign them.*

On the toolbar there is another button associated with the relay outputs. The button looks like this:

This is the "Contact Signal" button. It allows you to put replica instances of a conditioned output relay into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

# 19.6 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

## 19.6.1 TRIP LED LOGIC

When a trip occurs, the trip LED is illuminated. It is possible to reset this with a number of ways:

- Directly with a reset command (by pressing the Clear Key)
- With a reset logic input
- With self-resetting logic

You enable the automatic self-resetting with the ***Sys Fn Links*** cell in the *SYSTEM DATA* column. A '0' disables self resetting and a '1' enables self resetting.

The reset occurs when the circuit is reclosed and the ***Any Pole Dead*** signal has been reset for three seconds providing the ***Any Start*** signal is inactive. The reset is prevented if the ***Any Start*** signal is active after the breaker closes.

The Trip LED logic is as follows:

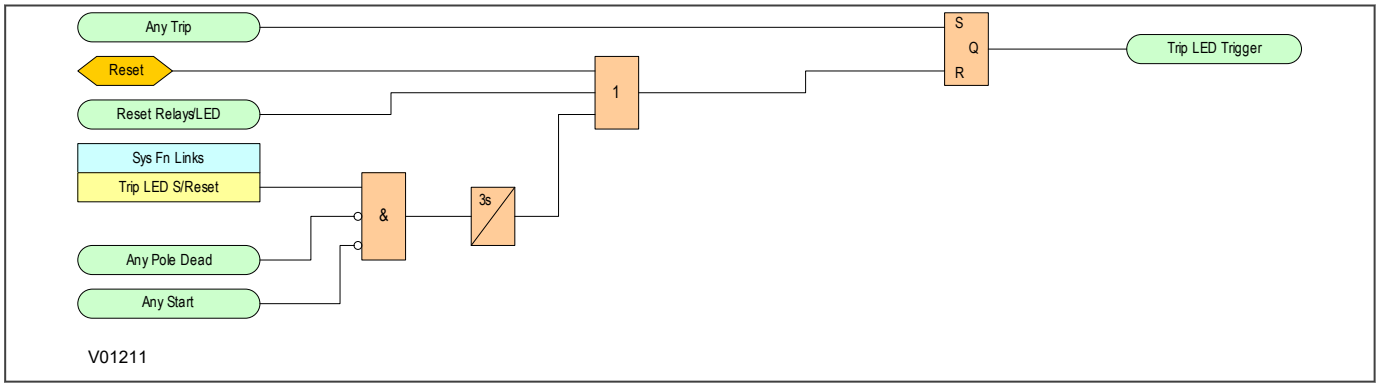



**Figure 259: Trip LED logic**

## 19.7 CONFIGURING PROGRAMMABLE LEDS

There are three types of programmable LED signals which vary according to the model being used. These are:

- Single-colour programmable LED. These are red when illuminated.
- Tri-colour programmable LED. These can be illuminated red, green, or amber.
- Tri-colour programmable LED associated with a Function Key. These can be illuminated red, green, or amber.

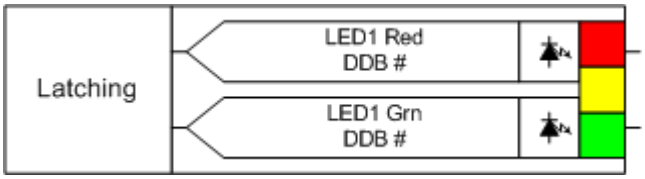
DDB signals are mapped in the PSL and used to illuminate the LEDs. For single-coloured programmable LEDs there is one DDB signal per LED. For tri-coloured LEDs there are two DDB signals associated with the LED. Asserting ***LED # Grn*** will illuminate the LED green. Asserting ***LED # Red*** will illuminate the LED red. Asserting both DDB signals will illuminate the LED amber.

The illumination of an LED is controlled by means of a conditioner. Using the conditioner, you can decide whether the LEDs reflect the real-time state of the DDB signals, or whether illumination is latched pending user intervention.

To map an LED in the PSL you should use the LED Conditioner button in the toolbar to import it. You then condition it according to your needs. The output(s) of the conditioner respect the attribute you have assigned.

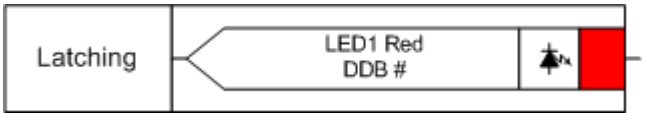
The toolbar button for a tri-colour LED looks like this:

The PSL contribution that it delivers looks like this:




The toolbar button for a single-colour LED looks like this:

The PSL contribution that it delivers looks like this.




*Note:*
*LED Conditioners are only available if they have not all been used up, and in some default PSL schemes they might be. If that is the case and you want to use them for something else, you will need to re-assign them.*

On the toolbar there is another button associated with the LEDs. For a tri-coloured LED the button looks like this:

For a single-colour LED it looks like this:

It is the "LED Signal" button. It allows you to put replica instances of a conditioned LED into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

*Note:*
*All LED DDB signals are always shown in the PSL Editor. However, the actual number of LEDs depends on the device hardware. For example, if a small 20TE device has only 4 programmable LEDs, LEDs 5-8 will not take effect even if they are mapped in the PSL.*

## 19.8 FUNCTION KEYS

For most models, a number of programmable function keys are available. This allows you to assign function keys to control functionality via the programmable scheme logic (PSL). Each function key is associated with a programmable tri-colour LED, which you can program to give the desired indication on activation of the function key.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are found in the *FUNCTION KEYS* column.

Each function key is associated with a DDB signal as shown in the DDB table. You can map these DDB signals to any function available in the PSL.

The ***Fn Key Status*** cell displays the status (energised or de-energised) of the function keys by means of a binary string, where each bit represents a function key starting with bit 0 for function key 1.

Each function key has three settings associated with it, as shown:

- ***Fn Key (n)***, which enables or disables the function key
- ***Fn Key (n) Mode***, which allows you to configure the key as toggled or normal
- ***Fn Key (n) label***, which allows you to define the function key text that is displayed

The ***Fn Key (n)*** cell is used to enable (unlock) or disable (unlock) the function key signals in PSL. The Lock setting has been provided to prevent further activation on subsequent key presses. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

When the ***Fn Key (n) Mode*** cell is set to `Toggle`, the function key DDB signal output will remain in the set state until a reset command is given. In the `Normal` mode, the function key DDB signal will remain energised for as long as the function key is pressed and will then reset automatically. In this mode, a minimum pulse duration can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The ***Fn Key Label*** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of all function keys are recorded in non-volatile memory. In case of auxiliary supply interruption their status will be maintained.

*Note:*
*All function key DDB signals are always shown in the PSL Editor. However, the actual number of function keys depends on the device hardware. For example, if a small 20TE device has no function keys, the function key DDBs mapped in the PSL will not take effect.*

## 19.9 CONTROL INPUTS

The control inputs are software switches, which can be set or reset locally or remotely. These inputs can be used to trigger any PSL function to which they are connected. There are three setting columns associated with the control inputs: *CONTROL INPUTS*, *CTRL I/P CONFIG* and *CTRL I/P LABELS*. These are listed in the Settings and Records appendix at the end of this manual.

# CHAPTER 20

# FIBRE TELEPROTECTION

## 20.1 CHAPTER OVERVIEW

This chapter provides information about the fibre-optic communication mechanism,which is used to provide unit schemes and general-purpose teleprotection signalling for protection of transmission lines and distribution feeders. The feature is called Fibre Teleprotection.

This chapter contains the following sections:

Chapter Overview 431

Protection Signalling Introduction 432

Fibre Teleprotection Implementation 434

IM64 Logic 443

Application Notes 445

## 20.2 PROTECTION SIGNALLING INTRODUCTION

Unit protection schemes can be formed by several IEDs located remotely from each other and some distance protection schemes. Such unit protection schemes need communication between each location to achieve a unit protection function. This communication is known as protection signalling or teleprotection. Communications facilities are also needed when remote circuit breakers need to be operated due to a local event. This communication is known as intertripping.

The communication messages involved may be quite simple, involving instructions for the receiving device to take some defined action (trip, block, etc.), or it may be the passing of measured data in some form from one device to another (as in a unit protection scheme).

Various types of communication links are available for protection signalling, for example:

- Private pilot wires installed by the utility
- Pilot wires or channels rented from a communications company
- Carrier channels at high frequencies over the power lines
- Radio channels at very high or ultra high frequencies
- Optical fibres

Whether or not a particular link is used depends on factors such as the availability of an appropriate communication network, the distance between protection relaying points, the terrain over which the power network is constructed, as well as cost.

Protection signalling is used to implement unit protection schemes, provide teleprotection commands, or implement intertripping between circuit breakers.

### 20.2.1 UNIT PROTECTION SCHEMES

Phase comparison and current differential schemes use signalling to convey information concerning the relaying quantity - phase angle of current and phase and magnitude of current respectively - between local and remote relaying points. Comparison of local and remote signals provides the basis for both fault detection and discrimination of the schemes.

### 20.2.2 TELEPROTECTION COMMANDS

Some Protection schemes use signalling to convey commands between local and remote relaying points. Receipt of the information is used to aid or speed up clearance of faults within a protected zone or to prevent tripping from faults outside a protected zone.

Teleprotection systems are often referred to by their mode of operation, or the role of the teleprotection command in the system.

Three types of teleprotection command are commonly encountered, direct tripping, permissive tripping and blocking schemes.

#### Direct Tripping

In direct tripping applications (also known as intertripping), signals are sent directly to the master trip relay. Receipt of the command causes circuit breaker operation. The method of communication must be reliable and secure because any signal detected at the receiving end causes a trip of the circuit at that end. The communications system must be designed so that interference on the communication circuit does not cause spurious trips. If a spurious trip occurs, the primary system might be unnecessarily isolated.

#### Permissive Tripping

Permissive trip commands are always monitored by a protection relay. The circuit breaker is tripped when receipt of the command coincides with a ‘start’ condition being detected by the protection relay at the receiving end responding to a system fault. Requirements for the communications channel are less onerous than for direct

tripping schemes, since receipt of an incorrect signal must coincide with a ‘start’ of the receiving end protection for a trip operation to take place. The intention of these schemes is to speed up tripping for faults occurring within the protected zone.

#### Blocking Scheme

Blocking commands are initiated by a protection element that detects faults external to the protected zone. Detection of an external fault at the local end of a protected circuit results in a blocking signal being transmitted to the remote end. At the remote end, receipt of the blocking signal prevents the remote end protection operating if it had detected the external fault. Loss of the communications channel is less serious for this scheme than in others as loss of the channel does not result in a failure to trip when required. However, the risk of a spurious trip is higher.

### 20.2.3 TRANSMISSION MEDIA AND INTERFERENCE

The transmission media that provide the communication links involved in protection signalling can be:

- Private pilots
- Rented pilots or channels
- Power line carrier
- Radio
- Optical fibres

Historically, pilot wires and channels (discontinuous pilot wires with isolation transformers or repeaters along the route between signalling points) have been the most widely used due to their availability, followed by Power Line Carrier Communications (PLCC) techniques and radio. In recent years, fibre-optic systems have become the usual choice for new installations, primarily due to their complete immunity from electrical interference. The use of fibre-optic cables also greatly increases the number of communication channels available for each physical fibre connection and thus enables more comprehensive monitoring of the power system to be achieved by the provision of a large number of communication channels.

## 20.3 FIBRE TELEPROTECTION IMPLEMENTATION

The Fibre Teleprotection interface is an optional feature in this product. It provides fibre-optic communications to implement intertripping command signalling which can be freely allocated to realise protection schemes such as Permissive and Blocking schemes. To use the feature you must enable the ***InterMiCOM 64*** setting in the *CONFIGURATION* column.

Each product can have up to 2 fibre-optic communications channels for teleprotection signalling. A range of different fibre-optic interfaces are available to provide:

- Direct fibre connections between devices with a number of options available to suit different requirements
- Indirect connections using the industry standard IEEE C37.94. Fibre-optic connections are made between the product and telecommunications equipment that supports industry standard fibre-optic interfaces (IEEE C37.94). The telecommunications equipment provides the end-to-end service.
- Fibre-optic connection in conjunction with proprietary auxiliary interface units to provide connection to standard electrical telecommunications interfaces (G.703, V.35, X.21). With this indirect connection method, the telecommunications equipment provides the end-to-end service.

Signals to be communicated between devices are constructed into packets (sometimes called telegrams). These packets include addressing, timing, and error checking information as well as teleprotection commands and data, and are transmitted between terminals at frequent regular intervals. Upon reception, they are checked for integrity before the contents are used.

Allocation of teleprotection commands is realised with mappings between InterMiCOM 64 signals and internal DDB logic signals using the product's the Programmable Scheme Logic (PSL).

### 20.3.1 SETTING UP THE IM64 SCHEME

To use the fibre teleprotection features in this product, you will need to configure the protection signalling scheme. The protection signalling scheme is defined by the number of connected terminals, together with the communications links between them.

Products can have either 1 physical fibre teleprotection channel, or two. Products with 1 physical fibre teleprotection channel can be used to connect two products together into a scheme. Products with 2 physical fibre teleprotection channels can be used to connect three products together into a scheme, or they can be used to connect two products together into a scheme with dual communications channels to provide communications redundancy (hot standby) in the event of a single communications channel failure.

For products with 2 physical fibre teleprotection channels use the ***Scheme Setup*** setting in the *PROT COMMS/ IM64* column. The choices are `3 Terminal`, `2 Terminal` (only physical Ch1 is used), and `Dual Redundant` (two terminals with two interconnecting channels).

The physical connections are labelled as Ch1 and Ch2.

In a two-terminal scheme, channel 1 of one device should always connect to channel 1 of the other device. For a two-terminal scheme with dual redundant communications, it follows that channel 2 of one device should connect to channel 2 of the other.

In a three terminal scheme, channel 1 of one device should always connect to channel 2 of another device as shown in the figure below.

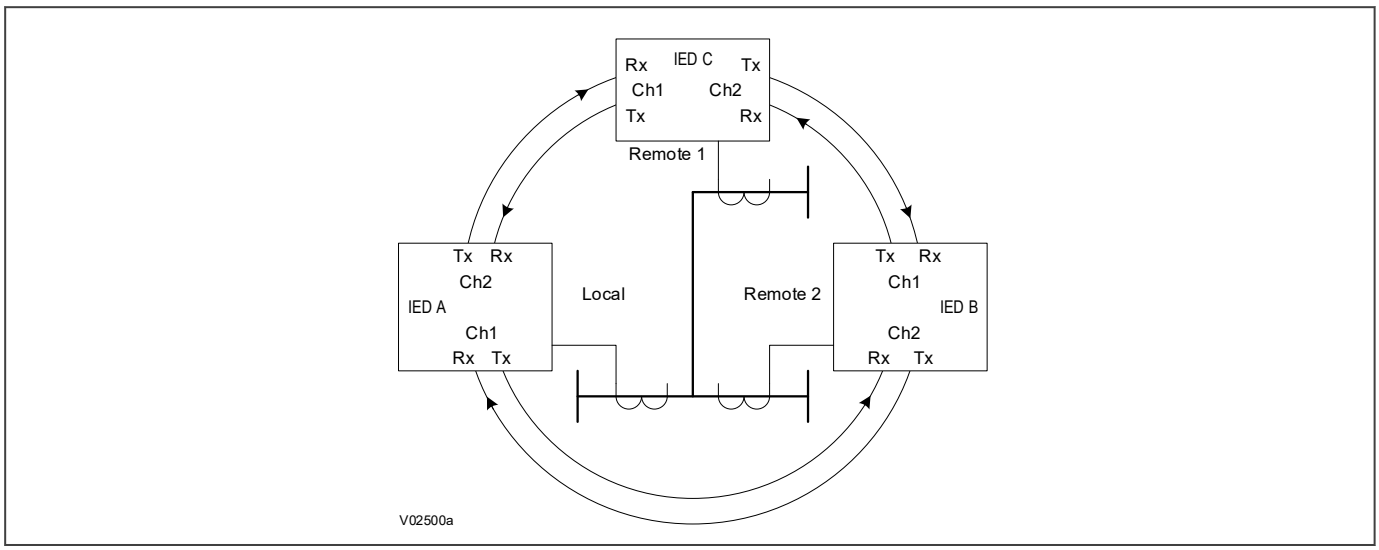



**Figure 260: Fibre Teleprotection connections for a three-terminal Scheme**

### 20.3.1.1 FIBRE TELEPROTECTION SCHEME TERMINAL ADDRESSING

In Fibre Teleprotection schemes, commands are packaged together with other important data for transmission over communications channels to the other devices. The packages of information are generally called ‘messages’. These messages are created for a specific destination where they will be acted upon to realise the overall scheme protection. It is critical that they are only used by the intended device. Making the correct channel connections may not always ensure that the messages get to the correct destination; there may be a possibility that communication paths may become cross-connected or looped back during telecommunications network switching operations. To avoid incorrect scheme operation, extra security is needed to ensure that messages are acted upon only by their intended recipient. This is achieved by means of an address field in the messages. The address field is used to individually match connected devices. A transmitting device includes the address of the intended recipient in the message. If the receiving device matches the address, the message will be used. If it does not match, it is discarded.

The address field is an 8-bit (or 24-bit*) field in the message . It can carry any 8-bit (or 24-bit*) value, but certain values have been chosen for maximum security. For convenience they have been arranged into 32 groups. All devices in a scheme must share the same group. For addressing, the different devices are referenced as ‘A’, ‘B’, and ‘C’ for three-terminal schemes. Their addresses should recognise the referencing.

So for a two-terminal scheme, if one device has the address set to ‘5-A’ the other should have the address to ‘5-B’.

Similarly, in a three-terminal scheme if one device has address ‘1-A’, the other devices would have addresses ‘1-B’ and ‘1-C’. The address is set using the address setting in the *PROT COMMS/IM64* column.

*If the ***Extended IM64*** mode is `Enabled`.

*Note:*
*In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

*Note:*
*A universal address (0-0) is used as default. If this is used all products use the same address ‘0-0’. This is primarily intended to help test the product before it goes into service. We strongly recommend not to use 0-0 in service since any communications switching or loopback condition will not be detected and may cause false tripping.*

*Note:*
*For a three-terminal scheme, the A, B, and C parts of the address group should match the figure shown earlier for a triangulated scheme where device A has address A, device B has address B, and device C has address C.*

### 20.3.1.2 SETTING UP IM64

In this product, the feature that manages the fibre teleprotection command signals is called InterMiCOM 64 (or IM64). IM64 is suitable for the exchange of all teleprotection command types.

Up to 2 banks of teleprotection command signals (IM64 signals) are provided. Each bank provides 8 (or 24*) duplex command signals. That means that each bank assigns 8 bits (or 24 bits*) for IM64 input signals and 8 bits (or 24 bits*) for IM64 output signals. Each bank is associated with a logical channel (referred to as Ch1 or Ch2 in the internal logic). Each logical channel associates with a physical communications channel (labelled Ch1 or Ch2 at the physical connection point). The association of logical channels to physical channels varies according to specific scheme configurations.

*If the ***Extended IM64*** mode is `Enabled`.

*Note:*
*In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

Action of each IM64 input signal is managed by attributes defined by three settings associated with it. These are set in the *PROT COMMS/IM64* column and are of the form:

- ***IM 1 Cmd Type*** (command type)
- ***IM 1 FallBackMode*** (fallback modes)
- ***IM 1 DefaultValue*** (default values)

The settings shown above are for bit 1 only

The IM64 command type settings set the teleprotection type. `Permissive` satisfies the security requirements of a permissive application, as well as the speed needed for a blocking scheme. For direct tripping applications, set it to `Direct`.

The IM64fallback settings determine the behaviour of an input under communications failure conditions. You can choose either to latch the state of the last good command received, or to revert to a default state. If you set the fallback mode to `Default` you will need to set the default state to your requirement (either 1 or 0).

The attributes assigned to bit n of an IM64 input apply to that bit in both logical channels. For example, if ***IM4 DefaultValue*** is chosen as `1` then the default value for bit 4 in logical channel 1 (IM64 Ch1 Input 4) will be the same for bit 4 in logical channel 2 (IM64 Ch2 Input 4), and will take the value 1.

### 20.3.1.3 TWO-TERMINAL IM64 OPERATION

The protection signalling connection requirement for products operating as a Two Terminal scheme is that the Physical Channels labelled as Ch1 should be connected together. That means that the local Ch1 Tx connects to the remote Ch1 Rx, and the local Ch1 Rx connects to the remote Ch1 Tx. Physical Channel 2 (Ch2) connectors may be fitted, but they are not used.

The 8-bits (or 24-bits*) of both Logical Channels (Ch1 and Ch2) are used. The bits of both Logical Channels are all assigned to Physical Channel 1, so 16 (or 64) duplex commands (IM64 Ch1 bits 1-8 (1-24*) and IM64 Ch2 bits 1-8 (1-24*) can be communicated between terminals in IM64 messages using Ch1 Physical Channels.

*If the ***Extended IM64*** mode is `Enabled`.

*Note:*
*In the PROT COMMS/ IM64 column,* ***Extended IM64*** *mode is only available when the* ***Comms Mode*** *is set to either,* `128 kbits/s` *or* `IEEE C37.94`*. When the* ***Comms Mode*** *is set to* `IEEE C37.94`*,* ***Ch1 N*64 kbits/s*** *and* ***Ch2 N*64 kbits/s*** *settings are available and should be set to a minimum of* `2`*.*

### 20.3.1.4 DUAL REDUNDANT TWO-TERMINAL IM64 OPERATION

The protection signalling connection requirement for products operating as a Dual Redundant (Hot Standby) scheme is that the Physical Channels labelled as Ch1 should be connected together and the Physical Channels labelled as Ch2 should be connected together. That means that the local Ch1 Tx connects to the remote Ch1 Rx, the local Ch1 Rx connects to the remote Ch1 Tx, the local Ch2 Tx connects to the remote Ch2 Rx, and the local Ch2 Rx connects to the remote Ch2 Tx.

The 8 bits (or 24 bits*) of both Logical Channels (Ch1 and Ch2) are used. The bits of both Logical Channels are all assigned both to Physical Channel 1 and to Physical Channel 2, so that 16 duplex commands (IM64 Ch1 bits 1-8 and IM64 Ch2 bits 1-8) can be communicated between terminals in IM64 messages with full redundancy of both Logical Channels in the event of failure of either Physical Channel.

*If the ***Extended IM64*** mode is `Enabled`.

*Note:*
*In the PROT COMMS/ IM64 column,* ***Extended IM64*** *mode is only available when the* ***Comms Mode*** *is set to either,* `128 kbits/s` *or* `IEEE C37.94`*. When the* ***Comms Mode*** *is set to* `IEEE C37.94`*,* ***Ch1 N*64 kbits/s*** *and* ***Ch2 N*64 kbits/s*** *settings are available and should be set to a minimum of* `2`*.*

### 20.3.1.5 THREE-TERMINAL IM64 OPERATION

The protection signalling connection requirement for products operating as a Three Terminal scheme is that Physical Channels labelled as Ch1 should be connected to Physical Channels labelled as Ch2 . That means that a local Ch1 Tx connects to a remote Ch2 Rx, and the corresponding Ch1 Rx and Ch2 Tx are connected together as shown in the earlier figure (Fibre Teleprotection Connections for a Three Terminal Scheme).

This Three Terminal scheme uses a triangulation approach and is designed to function if a communications link between two terminals is not present or is degraded. 8 duplex teleprotection commands are available between any pair of terminals even if one communication channel fails.

Logical Channel 1 is associated with Physical Channel 1, and Logical Channel 2 is associated with Physical Channel 2.

Consider a Three terminal scheme where the terminals are referenced as Local, Remote1, and Remote2. Remote 1 correlates to Ch1, and Remote 2 correlates to Ch2. The Local terminal will send the commands that it wants Remote 1 to act on to both Remote 1 and Remote 2. Upon receipt, Remote 1 acts upon the commands that the Local terminal wants it to use. Remote 1 also packages the commands that it wants Remote 2 to use, together with a copy of the commands that Local wants Remote 2 to use, and also the commands it wants Local to use. Remote 1 sends the message to Remote2. Remote 2 acts similarly. The same process occurs in the opposite direction around the ring, so in the event of a single channel failure, and if all terminals have the same mappings for the 8 (or 24*) IM64 bits integrity will be maintained for all 8 (or 24*) duplex commands between connected terminals.

In a triangulated scheme, at each terminal, Logical Channel 1 commands are assigned to Physical Channel 1, and Logical Channel 2 commands are assigned to Physical Channel 2. At each terminal, the eight IM64 commands transmitted on Physical Channel 1 are intended for the device connected as its Remote 1, and the eight IM64 commands transmitted on Channel 2 are intended for the device connected as its Remote 2. So, 8 (or 24*) full-duplex commands are available between any two terminals. Each device transmits both channels of eight IM64 commands to the connected devices. At the Remote 1 device, the eight Channel 1 IM64 commands are used directly by the receiving device which passes through the 8 (or 24*) Channel 2 IM64 commands to the remote 2 device. All three devices in the scheme perform similarly, ensuring that, so long as one device is able to communicate with the other two, scheme integrity is maintained.

*If the ***Extended IM64*** mode is `Enabled`.

> *Note:*
> *In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

This Chain topology (normally invoked when a communication link fails) can be used to save cost in a three-terminal scheme. This is because two legs are cheaper to install than full triangulation implementation. Also if a suitable communication link is not available between two of the line ends, it may be the only option. If a Chain topology is used, or one link in a fully triangulated scheme is lost, the operating delay of the teleprotection commands increases by approximately 7 ms, plus the communications channel signalling delay, due to the extended path length and additional processing.

### 20.3.1.6 PHYSICAL CONNECTION

The protection communications into and out of the products are fibre-optic. Connections are made using BFOC/2.5 connectors (BFOC/2.5 connectors are commonly referred to as “ST” connectors where “ST” is a registered trademark of AT&T).

According to application, different fibre-optic interfaces are available described in the following table:

| Wavelength of Light (nm) | Fibre Type | Maximum Transmission Distance (km) |
|---|---|---|
| 850 | Multi-mode | 1 |
| 1300 | Multi-mode | 50 |
| 1300 | Single-mode | 100 |
| 1550 | Single-mode | 130 |

Connections are made using appropriate fibre-optic cables terminated with BFOC/2.5 connectors. The transmitter of one device (for example Tx1) is connected to the receiver of another (Rx1 or Rx2 according to the scheme set-up)

Products can be supplied with the following fibre-optic channel arrangements:

| Ch 1 | Ch2 |
|---|---|
| 850 nm | 850 nm |
| 1300 nm multi-mode | Not fitted |
| 1300 nm multi-mode | 1300 nm multi-mode |
| 1300 nm single-mode | Not fitted |
| 1300 nm single-mode | 1300 nm single-mode |
| 1550 nm single-mode | Not fitted |
| 1550 nm single-mode | 1550 nm single-mode |
| 850 nm | 1300 nm multi-mode |
| 850 nm | 1300 nm single-mode |
| 850 nm | 1550 nm single-mode |
| 1300 nm multi-mode | 850 nm |
| 1300 nm single-mode | 850 nm |
| 1550 nm single-mode | 850 nm |

#### 20.3.1.6.1 DIRECT CONNECTION

If you are using direct fibre connections you need to set the ***Scheme Setup*** settings and you are advised to change the ***Address*** setting from the default. You find these settings in the PROT *COMMS/IM64* columns. You should not need to use any of the other settings that would be applicable if using shared links and/or interfacing units.

#### 20.3.1.6.2 INDIRECT CONNECTION

For 850nm communications links where the connection is not direct fibre, a number of options are available to interface with standard telecommunications equipment. These are:

- Fibre connection to telecommunications equipment supporting the IEEE C37.94 interface
- Connection to G.703, V.35 or X.21 electrical circuits using auxiliary P59x interface units

P59x interface unit options are:

- P591 - Fiber optic to electrical signal G.703 (co-directional) 64 Kbit/s, 2Mbit/s otr IEEE C39.94, depending on ordering option
- P592 - Fiber optic to electrical signal V.35
- P593 - Fiber optic to electrical signal X.21 (64 Kbit/s or IEEE C37.94, depending on ordering option)

*Note:*
*When the relay is set to 24bit InterMiCOM64 application mode (**Extended IM64** setting `Enabled`), the relay is not compatible with P592. Please contact General Electric for G.703, V.35 or X.21 electrical circuit converter.*

P59x interface units are housed in 10TE wide, 4U high cases. They provide optical-electrical conversion. The optical characteristics match those of the 850nm interface on the protection device. When used, you need one unit for each transmitter/receiver pair. That means one unit at each end of each communications channel as demonstrated in the figure below.

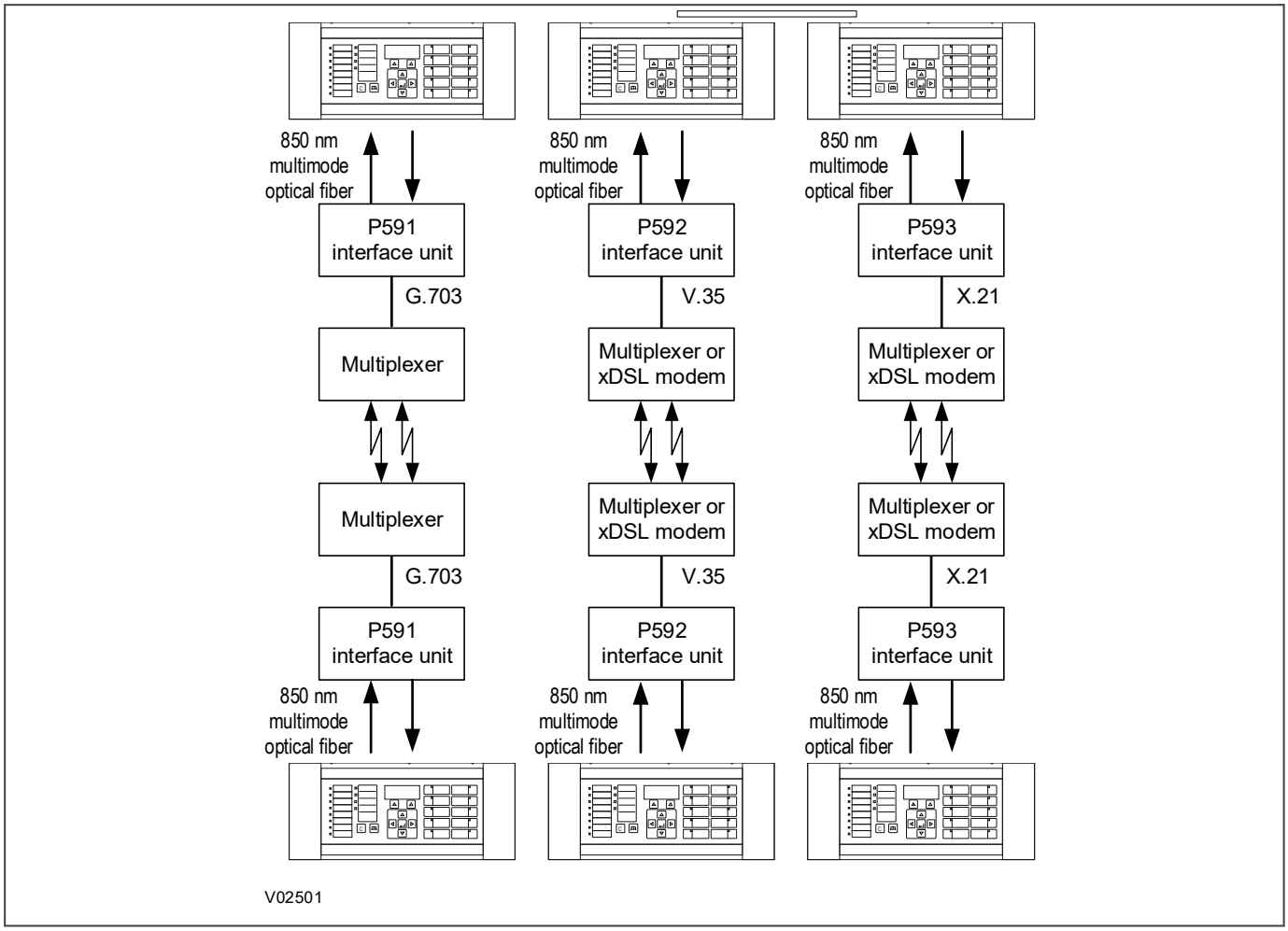



**Figure 261: Interfacing to PCM multiplexers**

*Note:*
*P59x interface units should be mounted as close as possible to the telecommunications equipment to minimise interference on the electrical connections.*

### 20.3.1.6.2.1 INDIRECT CONNECTION - FIBRE (IEEE C37.94)

An 850 nm fibre-optic interface can connect directly to a multiplexer supporting the IEEE C37.94 standard. 850 nm multi-mode optical fibres, either 50/125 μm or 62.5/125 μm are suitable. BFOC/2.5 type fibre optic connectors are used.

*Note:*
*To use this configuration, you need to set* ***Comms Mode*** *to 'IEEE C37.94'. You then need to remove the power supply from the product and then re-apply the power. The setting is now effective. If 'IEEE C37.94' is used, it applies to both communication channels.*

The IEEE C37.94 standard defines an N*64 kbits/s selection, where N is a number between 1 and 12 and selects the channel used in the multiplexer. The value of N is set on a per channel basis by setting ***Ch1 N*64kbits/s*** (and ***Ch2 N*64kbits/s*** where applicable) to N (1 to 12). For convenience an auto-detect setting is provided, if using the ***Extended IM64*** mode, and therefore 128Kb/s, then a minimum of 2 slots will need to be configured. Setting to `Auto` means that the device will automatically determine which multiplexer channel to use.

#### 20.3.1.6.2.2 INDIRECT CONNECTION - ELECTRICAL CIRCUITS

P591, P592, P593 interface units are housed in 10TE wide, 4U high cases. They provide optical-electrical conversion allowing the protection to be used with telecommunications equipment providing interfaces to the ITU-T recommendations G,703, V.35 and X.21 respectively. The optical characteristics of the P59x devices match those of the 850 nm interface on the protection device. When used, you need one unit for each transmitter/receiver pair. That means one unit at each end of each communications channel. The P59x devices should be mounted as close as possible to the telecommunications equipment to minimise interference on the electrical connections.

A detailed description of the devices can be found in the P59x Technical Manual.

The P59x range supports the following electrical connections:

- X.21: Connection at 64 kbps or C37.94 is supported.
- V.35: Connection at 64 kbps or 56 kbps is supported.
- G.703: The data rate (baud rate) is 64 kbps or C37.94 up to 12 x 64 kbps, but connection can be made at either 64 kbps or 2 Mbps.

When P59x units are used in the communications channel of the protection scheme, the following must be set:

- Comms Mode
- Baud Rate Chn (n = 1 or 2)
- Clock Source Chn (n = 1 or 2)

You should set the Comms Mode setting to S*tandard* or *C37.94*, and you should match the Baud Rate to the channel data rate.

For V.35, you should set the Clock Source to *External* for a multiplexer network which is supplying a master clock signal, or to *Internal* for a multiplexer network recovering signal timing from the equipment (clock recovery). For G.703 and X.21, you always set the clock source to E*xternal*.

> *Note:*
> *When you are using C37.94 between the IED and the P591, you must set one of the converters as a master and the other as a slave.*

## 20.3.2 IM64 SELECT 8 OR 32 BITS PER CHANNEL

To enable IM64 24 bits per channel, the devices's data rate must be increased from 64/56Kbps to 128Kbps. To maintain backward compatibility with revious software versions, the data rate will be selectable via the *PROT COMMS/IM64* column ***Comms Mode*** setting, which includes *128Kbits/s* in addition to *Standard* and *IEEE C37.94* options.

If the ***Comms Mode*** setting is set to *128Kbits/s* or *IEEE C37.94* then the option to set IM64 to 8 or 24 bits per channel (via the ***Extended IM64*** setting in the *PROT COMMS/IM64* column) will be available.

If IM64 is configured to 24 bits (***Extended IM64*** set to *Enabled*) and the ***Comms Mode*** set to *IEEE C37.94*, then the minimum number of comms channels used will be 2.

***Extended IM64*** input and output signal names (from ***IM64 Ch1Input 9****/***IM64 Ch2Input 9**** and ***IM64 Ch1Output 9****/***IM64 Ch2Output 9**** onward) are denoted by a trailing asterisk.

If the ***Comms mode*** is set to *Standard* or *IEEE C37.94* and IM64 is configured to 8 bits (***Extended IM64*** set to *Disabled*), the previous software version behaviour will be unchanged.

If only one slot is configured and the ***Comms Mode*** is set to *IEEE C37.94*, then IM64 cannot be set to 24 bits (***Extended IM64*** cannot be set to *Enabled*).

When the ***Comms Mode*** is set to *IEEE C37.94*, ***Ch 1 N*64kbits/s*** or ***Ch 2 N*64kbits/s*** set to *AUTO* and IM64 is set to 24 bits (***Extended IM64*** set to *Enabled*), then a request from the multiplexer for the use of a slot will trigger a ***Ch1 Mismatch RxN*** or ***Ch2 Mismatch RxN*** flag and the request will be ignored.

*Note:*
*The comms message format is not backwards compatible if the **Comms Mode** is 128Kbps or IEEE C37.94 and IM64 is configured to 24 bits (**Extended IM64** set to Enabled).*

*Note:*
*All devices in a scheme must be capable of **Extended IM64** operation.*

The ***Invalid Mesg Fmt*** alarm and the ***IM64 SchemeFail*** alarm will activate if the received comms message is not of the correct format and data rate.

Once the new comms configuration has been set, an alarm ***Comms Changed*** will be active to prompt the user to reboot the relay. Once rebooted, the changed comms configuration will be active.

## 20.4 IM64 LOGIC

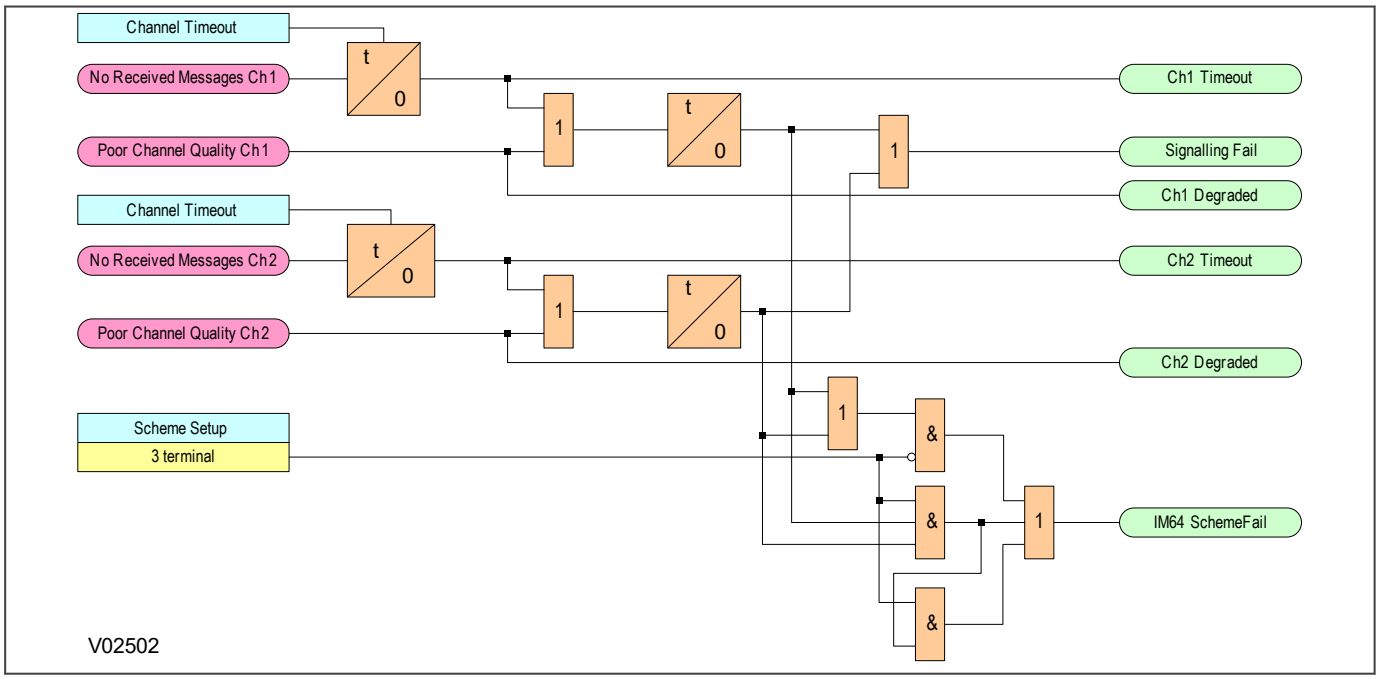



**Figure 262: IM64 channel fail and scheme fail logic**

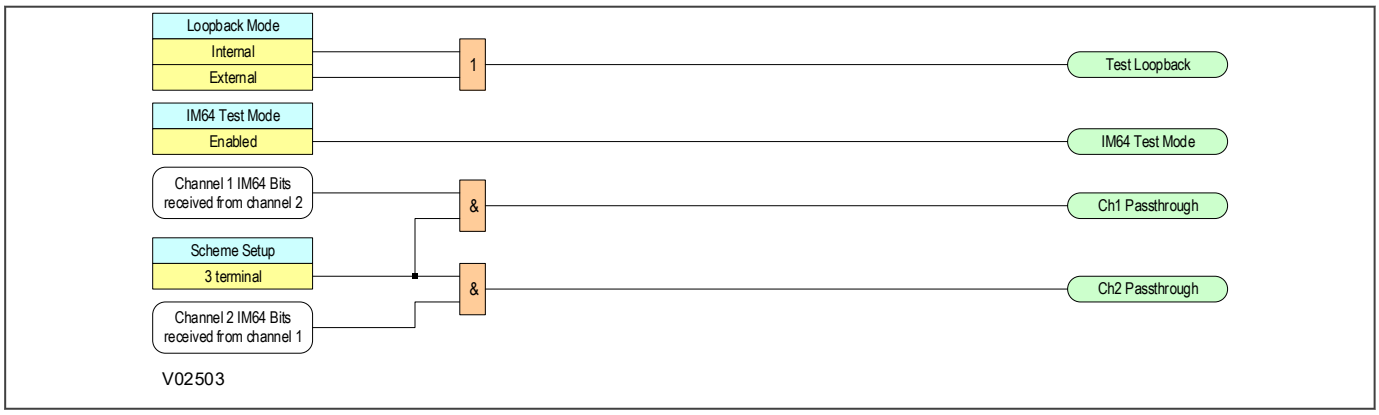



**Figure 263: IM64 general alarm signals logic**

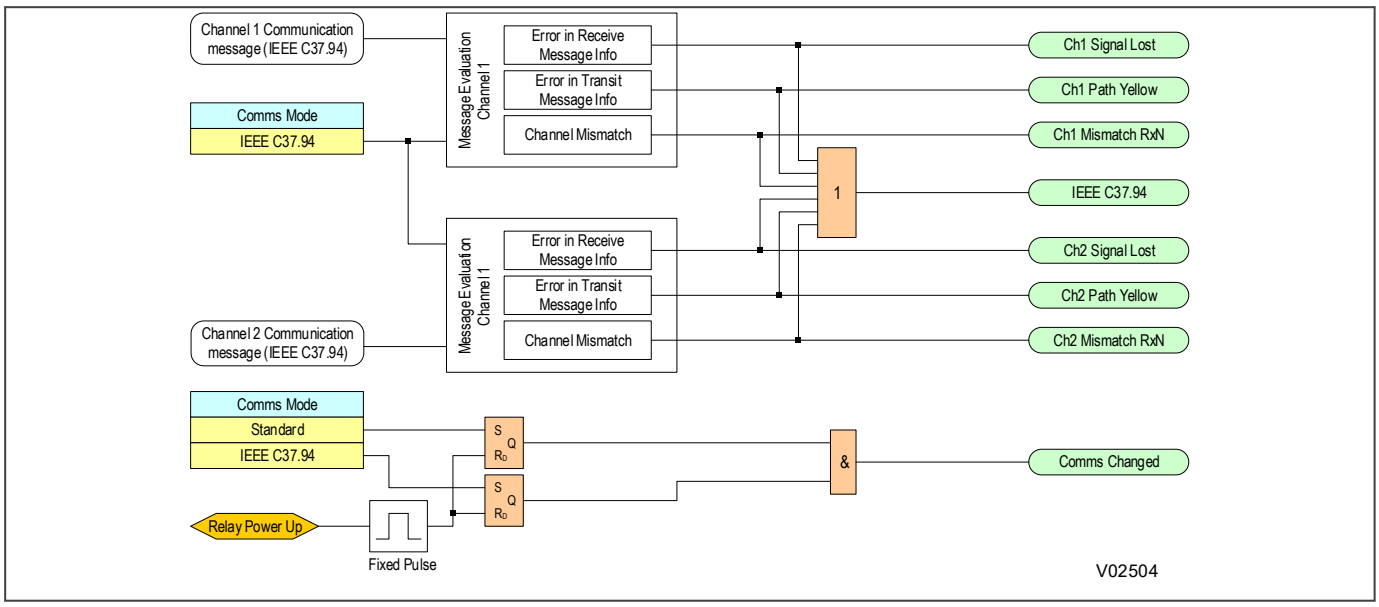



**Figure 264: IM64 communications mode and IEEE C37.94 alarm signals**

## 20.5 APPLICATION NOTES

Effective communications are essential for the performance of teleprotection schemes. Disturbances on the communications links need to be detected and reported so that appropriate actions can be taken to ensure that the power system does not go unprotected.

### 20.5.1 ALARM MANAGEMENT

Due to the criticality of IM64 communications for correct scheme performance, there is an extensive regime to monitor signal quality and integrity, generate and report alarms. For most applications, the alarm management provided as standard will satisfy the needs of the scheme.

For some applications, it may be necessary customise the alarm management. You can do this with the programmable scheme logic. This section provides a detailed explanation the communications alarm signals integrated in this product.

### 20.5.2 ALARM LOGIC

The figures in the logic diagram section show the main alarm DDB signals associated with IM64. Some of the signals are setting or hardware dependent. For example, Channel 2 alarms are not available on a simple two-terminal single communications link application. This section explains the logic, allowing you to understand how you might customise the alarm logic for your application.

The messages received on each channel are individually assessed for quality to ensure the IM64 signalling scheme is available for use. If no messages are received for a period equal to the ***Channel Timeout*** setting or the signal quality falls below a defined value, DDB signals are activated as shown in the IM64 channel fail and scheme fail logic diagram.

Poor quality is indicated if the percentage of incomplete messages exceeds the ***IM Msg Alarm Lvl*** setting in a 100 ms period (rolling window), or if the communications propagation time of the IM64 message exceeds the ***Max Ch PropDelay*** (assuming the ***Prop Delay Stats*** setting is `Enabled`), or if (in IEEE C37.94 configuration only, and not shown on the diagram) the ***Ch Mux Clk*** flag has been raised to indicate an incorrect baud rate.

If either the ***Ch Timeout*** or the ***Ch Degraded*** signal persists in the alarmed state for more than the duration of the ***Comm Fail Timer*** setting, according to the conditions set in the Comm Fail Mode setting, the ***Signalling Fail*** signal is raised.

For two-ended schemes (including dual redundant schemes), the ***IM64 SchemeFail*** signal is generated at the same time as the ***Signalling Fail*** signal. However, for three-terminal applications, the ***IM64 SchemeFail*** signal indicates that the full set of signalling bits cannot be processed by the scheme. Due to the self-healing nature of the three-terminal application, this occurs when both channels at any one terminal are not receiving valid signals. This condition generates a flag in the IM64 message structure which is passed to both remote ends, as well as generating the local ***IM64 SchemeFail*** signal. Using this method, in three-terminal applications the scheme fail indication is raised at all three ends.

The scheme fail signalling is generated by the inability of a device to receive messages through communication failure. The transmitting device only knows that communication to a remote device has failed if it receives notification from the remote device. If a device in the scheme is put into test mode, the communication failure information is not passed on to the remote ends. If the communications failure is bidirectional, there will be no indication at the remote device. If this causes operational issues, it may be necessary to include other signals to enable more precise indication of scheme failure.

In addition to the main IM64 channel fail and scheme fail conceptual logic, there are number of additional alarm DDB signals associated with test modes, reconfiguration for 3-terminal schemes, and the communication mode (‘Standard’ or ‘IEEE C37.94’) shown in the logic diagrams.

The majority of signals are associated with the ‘IEEE C37.94’ communications mode and are not activated if the `Standard` communication mode is selected. The ***Comms Changed*** DDB logic is to show that switching between the different communication modes requires a power cycle to be performed before the change is activated.

### 20.5.3 TWO-ENDED SCHEME EXTENDED SUPERVISION

For two-terminal applications, the ***Signalling Fail*** and ***IM64 SchemeFail*** signals operate together. As such, the basic indications available on each device should be considered as local-terminal indications only. If remote indication is needed to assure scheme functionality, it is necessary to use additional signals to communicate the status to the remote end. One method of performing this is shown below:

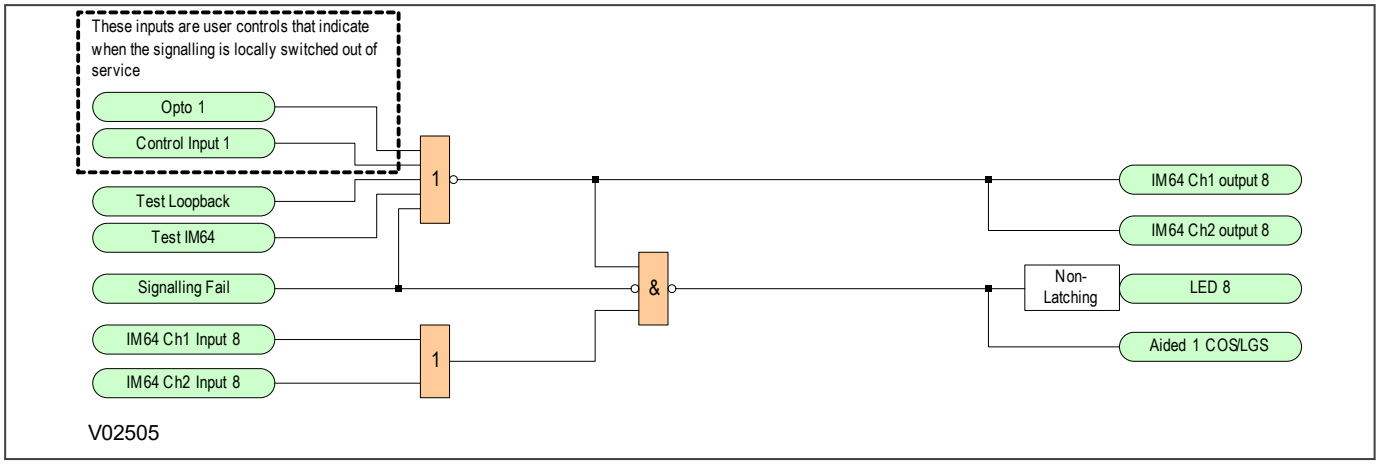



**Figure 265: IM64 two-terminal scheme extended supervision**

In this example scheme, several signals are used to permanently pass an IM64 signal to the remote terminal. These signals take account of the local ability to receive IM64 messages, local test/loopback modes and any other external methods of switching the signalling scheme out of service. If any of these driving signals are energised, the IM64 message is reset (a “0” sent on IM64 bit 8--or bit 24 if ***Extended IM64*** mode is `Enabled`). This causes both ends to raise an alarm (LED 8 in the example) or switch the aided scheme out of service due to loss of channel.

This is intended only as an example. You may need to customise it for your application requirements.

### 20.5.4 THREE-ENDED SCHEME EXTENDED SUPERVISION

The example for an IM64 two-terminal scheme above can be used for three-terminal applications. However for three-terminal applications, the ***IM64 SchemeFail*** signal that is automatically communicated to all ends of the scheme is used rather than the ***Signalling Fail*** signal.

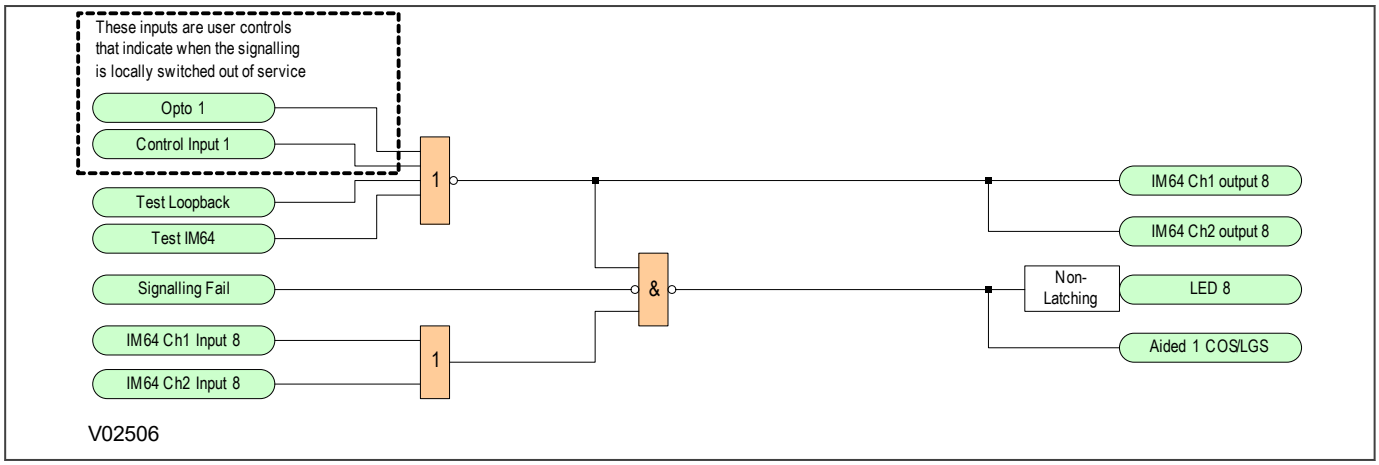



**Figure 266: IM64 three-terminal scheme extended supervision**

In this example if both channels at any one terminal fail to receive information, this is communicated to the other terminals. An alarm is raised and the aided scheme is switched out of service. The example given above, also takes

into account the test modes and local switching, so the scheme is signalled out of service at all terminals if one terminal is locally disabled.

The logic presented above is intended only as an example. You may need to customise it for your application requirements.

CHAPTER 21

# ELECTRICAL TELEPROTECTION

## 21.1 CHAPTER OVERVIEW

This chapter contains the following sections:

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Teleprotection Scheme Principles 451
Implementation 452
Configuration 453
Connecting to Electrical InterMiCOM 455
Application Notes 456

## 21.2 INTRODUCTION

Electrical Teleprotection is an optional feature that uses communications links to create protection schemes. It can be used to replace hard wiring between dedicated relay output contacts and digital input circuits. Two products equipped with electrical teleprotection can connect and exchange commands using a communication link. It is typically used to implement teleprotection schemes.

Using full duplex communications, eight binary command signals can be sent in each direction between connected products. The communication connection complies with the EIA(RS)232 standard. Ports may be connected directly, or using modems. Alternatively EIA(RS)232 converters can be used for connecting to other media such as optical fibres.

Communications statistics and diagnostics enable you to monitor the integrity of the communications link, and a loopback feature is available to help with testing.

## 21.3 TELEPROTECTION SCHEME PRINCIPLES

Teleprotection schemes use signalling to convey a trip command to remote circuit breakers to isolate circuits. Three types of teleprotection commands are commonly encountered:

- Direct Tripping
- Permissive Tripping
- Blocking Scheme

### 21.3.1 DIRECT TRIPPING

In direct tripping applications (often described by the generic term: “intertripping”), teleprotection signals are sent directly to a master trip device. Receipt of a command causes circuit breaker operation without any further qualification. Communication must be reliable and secure because any signal detected at the receiving end causes a trip of the circuit at that end. The communications system must be designed so that interference on the communication circuit does not cause spurious trips. If a spurious trip occurs, the primary system might be unnecessarily isolated.

### 21.3.2 PERMISSIVE TRIPPING

Permissive trip commands are monitored by a protection device. The circuit breaker is tripped when receipt of the command coincides with a ‘start’ condition being detected by the protection at the receiving. Requirements for the communications channel are less onerous than for direct tripping schemes, since receipt of an incorrect signal must coincide with a ‘start’ of the receiving end protection for a trip operation to take place. Permissive tripping is used to speed up tripping for faults occurring within a protected zone.

## 21.4 IMPLEMENTATION

Electrical InterMiCOM is configured using a combination of settings in the *INTERMICOM COMMS* column, settings in the *INTERMICOM CONF* column, and the programmable scheme logic (PSL).

The eight command signals are mapped to DDB signals within the product using the PSL.

Signals being sent to a remote terminal are referenced in the PSL as ***IM Output 1*** - ***IM Output 8***. Signals received from the remote terminal are referenced as ***IM Input 1*** - ***IM Input 8***.

*Note:*
*As well as the optional Modem InterMiCOM, some products are available with a feature called InterMiCOM64 (IM64). The functionality and assignment of commands in InterMiCOM and InterMiCOM64 are similar, but they act independently and are configured independently.*

## 21.5 CONFIGURATION

Electrical Teleprotection is compliant with IEC 60834-1:1999. For your application, you can customise individual command signals to the differing requirements of security, speed, and dependability as defined in this standard.

You customise the command signals using the ***IM# Cmd Type*** cell in the *INTERMICOM CONF* column.

Any command signal can be configured for:

- Direct intertripping by selecting 'Direct'. (this is the most secure signalling but incurs a time delay to deliver the security).
- Blocking applications by selecting 'Blocking'. (this is the fastest signalling)
- Permissive intertripping applications by selecting 'Permissive. (this is dependable signalling that balances speed and security)

You can also select to 'Disable' the command.

*Note:*
*When used in the context of a setting, '#' specifies which command signal (1-8) bit is being configured.*

To ensure that command signals are processed only by their intended recipient, the command signals are packaged into a message (sometimes referred to as a telegram) which contains an address field. A sending device sets a pattern in this field. A receiving device must be set to match this pattern in the address field before the commands will be acted upon. 10 patterns have been carefully chosen for maximum security. You need to choose which ones to use, and set them using the ***Source Address*** and ***Receive Address*** cells in the *INTERMICOM COMMS* column.

The value set in the ***Source Address*** of the transmitting device should match that set in the ***Receive Address*** of the receiving device. For example set ***Source Address*** to `1` at a local terminal and set ***Receive Address*** to `1` at the remote terminal.

The Source Address and Receive Address settings in the device should be set to different values to avoid false operation under inadvertent loopback conditions.

Where more than one pair of devices is likely to share a communication link, you should set each pair to use a different pair of address values.

Electrical InterMiCOM has been designed to be resilient to noise on communications links, but during severe noise conditions, the communication may fail. If this is the case, an alarm is raised and you can choose how the input signals are managed using the ***IM# FallBackMode*** cell in the *INTERMICOM CONF* column:

• If you choose `Latched`, the last valid command to be received can be maintained until a new valid message is received.

• If you choose `Default`, the signal will revert to a default value after the period defined in the ***IM# FrameSyncTim*** setting has expired. You choose the default value using the ***IM# DefaultValue*** setting.

Subsequent receipt of a full valid message will reset the alarm, and the new command signals will be used.

As well as the settings described above, you will need to assign input and output signals in the Programmable Scheme Logic (PSL). Use the 'Integral Tripping' buttons to create the logic you want to apply. A typical example is shown below.

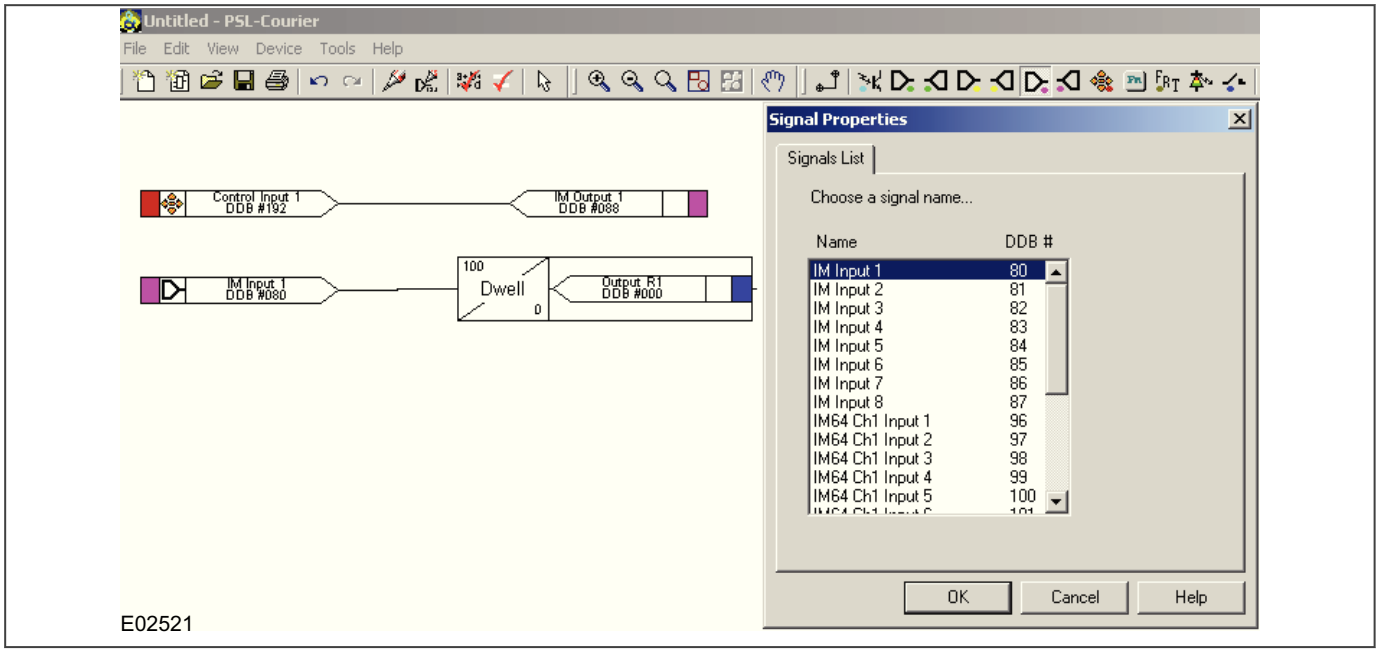


**Figure 267: Example assignment of InterMiCOM signals within the PSL**

*Note:*
*When an Electrical InterMiCOM signal is sent from a local terminal, only the remote terminal will react to the command. The local terminal will only react to commands initiated at the remote terminal.*

## 21.6 CONNECTING TO ELECTRICAL INTERMICOM

Electrical InterMiCOM uses EIA(RS)232 communication presented on a 9-pin 'D' type connector. The connector is labelled SK5 and is located at the bottom of the 2nd Rear communication board. The port is configured as standard DTE (Data Terminating Equipment).

### 21.6.1 SHORT DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is not a problem, direct connection between devices is possible. For this case, inter-device connections should be made as shown below the figure below.

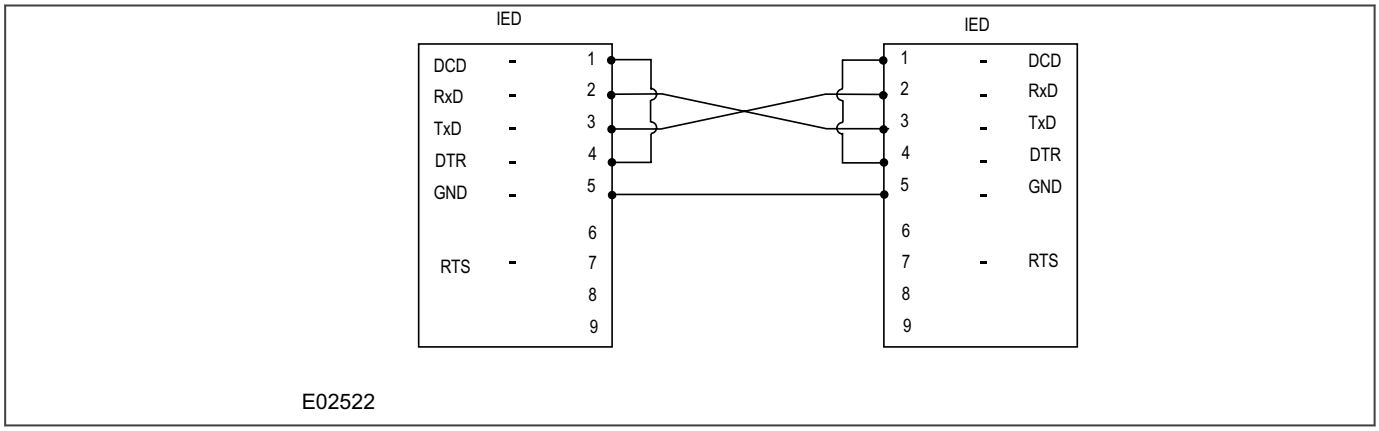


**Figure 268: Direct connection**

For direct connection, the maximum baud rate can generally be used.

### 21.6.2 LONG DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is a problem, direct connection between devices is not possible. For this case, inter-device connections should be made as shown below the figure below.

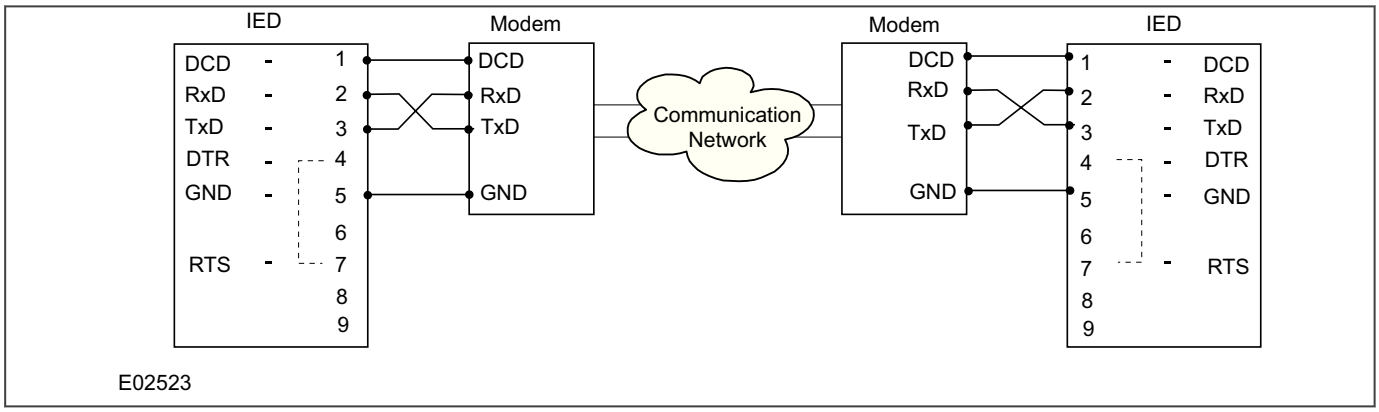


**Figure 269: Indirect connection using modems**

This type of connection should be used when connecting to devices that have the ability to control the DCD line. The baud rate should be chosen to be suitable for the communications network. If the Modem does not support the DCD function, the DCD terminal on the IED should be connected to the DTR terminal.

## 21.7 APPLICATION NOTES

Electrical InterMiCOM settings are contained within two columns; *INTERMICOM COMMS* and *INTERMICOM CONF*. The *INTERMICOM COMMS* column contains all the settings needed to configure the communications, as well as the channel statistics and diagnostic facilities. The *INTERMICOM CONF* column sets the mode of each command signal and defines how they operate in case of signalling failure.

Short metallic direct connections and connections using fire-optic converters will generally be set to have the highest signalling speed of 19200b/s. Due to this high signalling rate, the difference in operating time between the direct, permissive, and blocking type signals is small. This means you can select the most secure signalling command type ('Direct' intertrip) for all commands. You do this with the ***IM# Cmd Type*** settings. For these applications you should set the ***IM# Fallback Mode*** to `Default`. You should also set a minimal intentional delay by setting ***IM# FrameSyncTim*** to 10 msecs. This ensures that whenever two consecutive corrupt messages are received, the command will immediately revert to the default value until a new valid message is received.

For applications that use Modem and/or multiplexed connections, the trade-off between speed, security, and dependability is more critical. Choosing the fastest baud rate (data rate) to achieve maximum speed may appear attractive, but this is likely to increase the cost of the telecommunications equipment. Also, telecommunication services operating at high data rates are more prone to interference and suffer from longer re-synchronisation times following periods of disruption. Taking into account these factors we recommend a maximum baud rate setting of 9600 bps. As baud rates decrease, communications become more robust with fewer interruptions, but overall signalling times increase.

At slower baud rates, the choice of signalling mode becomes significant. You should also consider what happens during periods of noise when message structure and content can be lost.

- In 'Blocking' mode, the likelihood of receiving a command in a noisy environment is high. In this case, we recommend you set ***IM# Fallback Mode*** to `Default`, with a reasonably long ***IM# FrameSyncTim*** setting. Set ***IM# DefaultValue*** to '1'. This provides a substitute for a received blocking signal, applying a failsafe for blocking schemes.
- In 'Direct' mode, the likelihood of receiving commands in a noisy environment is small. In this case, we recommend you set ***IM# Fallback Mode*** to `Default` with a short ***IM# FrameSyncTim*** setting. Set ***IM# DefaultValue*** to '0'. This means that if a corrupt message is received, InterMiCOM will use the default value. This provides a substitute for the intertrip signal not being received, applying a failsafe for direct intertripping schemes.
- In 'Permissive' mode, the likelihood of receiving a valid command under noisy communications conditions is somwhere between that of the 'Blocking' mode and the 'Direct' intertrip mode. In this case, we recommended you set ***IM# Fallback Mode*** to `Latched`.

The table below presents recommended ***IM# FrameSyncTim*** settings for the different signalling modes and baud rates:

| | Minimum Recommended "IM# FrameSyncTim" Setting | | | |
|---|---|---|---|---|
| **Baud Rate** | **Direct Intertrip Mode** | **Blocking Mode** | **Minimum Setting (ms)** | **Maximum Setting (ms)** |
| 600 | 100 | 250 | 100 | 1500 |
| 1200 | 50 | 130 | 50 | 1500 |
| 2400 | 30 | 70 | 30 | 1500 |
| 4800 | 20 | 40 | 20 | 1500 |
| 9600 | 10 | 20 | 10 | 1500 |
| 19200 | 10 | 10 | 10 | 1500 |

*Note:*
*As we have recommended Latched operation, the table does not contain recommendations for 'Permissive' mode. However, if you do select 'Default' mode, you should set* ***IM# FrameSyncTim*** *greater than those listed above. If you set* ***IM# FrameSyncTim*** *lower than the minimum setting listed above, the device could interpret a valid change in a message as a corrupted message.*

We recommend a setting of 25% for the communications failure alarm.

# CHAPTER 22

# COMMUNICATIONS

## 22.1 CHAPTER OVERVIEW

This product supports Substation Automation System (SAS), and Supervisory Control and Data Acquisition (SCADA) communication. It embraces the evolution of communications technologies, since microprocessor technologies were introduced into protection, control, and monitoring devices - now known as Intelligent Electronic Devices for the substation (IEDs).

All products support rugged serial communications for SCADA and SAS applications. Optionally, any product can support Ethernet communications for more advanced SCADA and SAS applications.

This chapter contains the following sections:

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Ethernet Communication 464
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Simple Network Time Protocol (SNTP) 486
Simple Network Management Protocol (SNMP) 487
Data Protocols 494
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Time Synchronisation 526

## 22.2 COMMUNICATION INTERFACES

The products have a number of standard and optional communication interfaces. The standard and optional hardware and protocols are summarised below:

| Port | Availability | Physical Layer | Use | Data Protocols |
|---|---|---|---|---|
| Front | Standard | USB Type B | Local settings | Courier |
| Rear Port 1<br>(RP1 copper) | Standard | RS232/RS485/K-Bus | SCADA<br>Remote settings | Courier, MODBUS, IEC60870-5-103, DNP3.0<br>(order option) |
| Rear Port 1<br>(RP1 fibre) | Optional | Fibre | SCADA<br>Remote settings | Courier, MODBUS, IEC60870-5-103, DNP3.0<br>(order option) |
| Rear Port 2<br>(RP2) | Optional | RS232/RS485/K-Bus | SCADA<br>Remote settings | SK4: Courier only<br>SK5: InterMicom only |
| Ethernet | Optional | Ethernet | IEC 61850<br>Remote settings | IEC 61850, Courier (tunnelled) |

*Note:*
*Optional communications boards are always fitted into slot A.*

*Note:*
*It is only possible to fit one optional communications board, therefore RP2 and Ethernet communications are mutually exclusive.*

## 22.3 SERIAL COMMUNICATION

The physical layer standards that are used for serial communications for SCADA purposes are:

- EIA(RS)485 (often abbreviated to RS485)
- K-Bus (a proprietary customization of RS485)

USB is used for local communication with the IED (for transferring settings and downloading firmware updates).

RS485 is similar to RS232 but for longer distances and it allows daisy-chaining and multi-dropping of IEDs.

K-Bus is a proprietary protocol quite similar to RS485, but it cannot be mixed on the same link as RS485. Unlike RS485, K-Bus signals applied across two terminals are not polarised.

It is important to note that these are not data protocols. They only describe the physical characteristics required for two devices to communicate with each other.

For a description of the K-Bus standard see K-Bus and GE Vernova's K-Bus interface guide reference R6509.

A full description of the RS485 is available in the published standard.

### 22.3.1 USB FRONT PORT

The USB interface uses the proprietary Courier protocol for local communication with the MiCOM S1 Agile settings application software.

This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate of 19200 bps, 11-bit frame (8 data bits, 1 start bit, 1 stop bit, even parity bit), and a fixed device address of '1'.

The USB interface is a Type B connector. Normally a Type A to Type B USB cable will be required to communicate between MiCOM S1 Agile and the IED.

### 22.3.2 EIA(RS)485 BUS

The RS485 two-wire connection provides a half-duplex, fully isolated serial connection to the IED. The connection is polarized but there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

The RS485 bus must be terminated at each end with 120 Ω 0.5 W terminating resistors between the signal wires.

The RS485 standard requires that each device be directly connected to the actual bus. Stubs and tees are forbidden. Loop bus and Star topologies are not part of the RS485 standard and are also forbidden.

Two-core screened twisted pair cable should be used. The final cable specification is dependent on the application, although a multi-strand 0.5 $mm^2$ per core is normally adequate. The total cable length must not exceed 1000 m. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The RS485 signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

It may be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master is waiting in receive mode, in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequently not responding. Symptoms of this are; poor response times (due to retries), increasing message error counts, erratic communications, and in the worst case, complete failure to communicate.

#### 22.3.2.1 EIA(RS)485 BIASING REQUIREMENTS

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean to prevent noise being injected.

*Note:*
*Some devices may be able to provide the bus bias, in which case external components would not be required.*

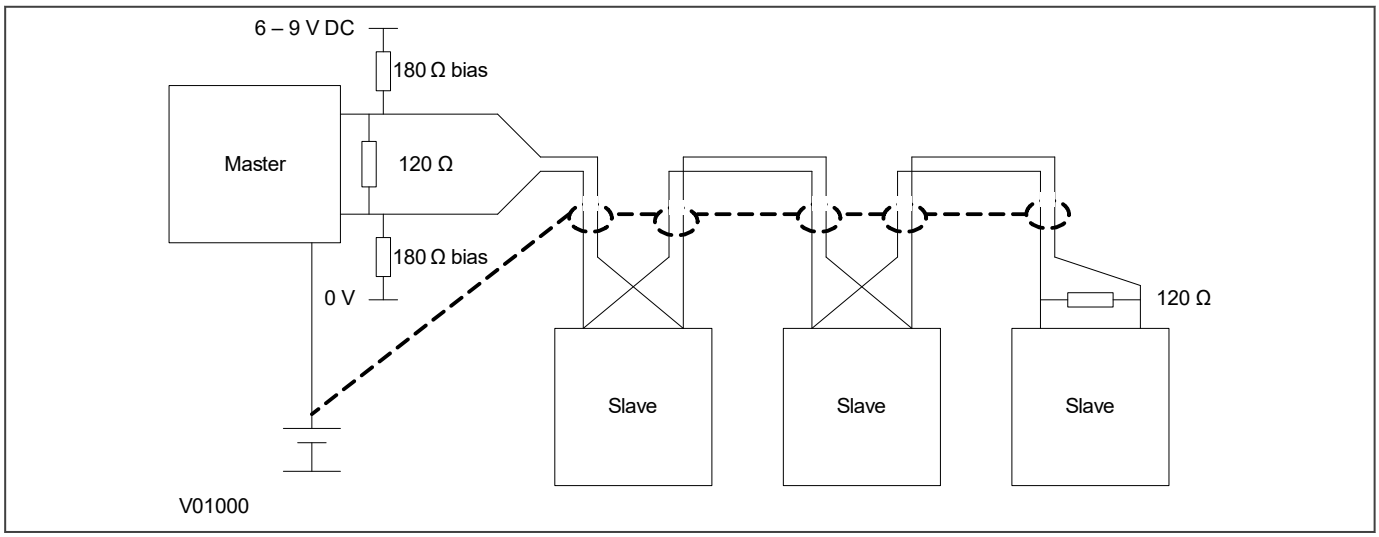


**Figure 270: RS485 biasing circuit**

**Warning:**
**It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.**

### 22.3.3 K-BUS

K-Bus is a robust signalling method based on RS485 voltage levels. K-Bus incorporates message framing, based on a 64 kbps synchronous HDLC protocol with FM0 modulation to increase speed and security.

The rear interface is used to provide a permanent connection for K-Bus, which allows multi-drop connection.

A K-Bus spur consists of up to 32 IEDs connected together in a multi-drop arrangement using twisted pair wiring. The K-Bus twisted pair connection is non-polarised.

It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. A protocol converter, namely the KITZ101 or KITZ102, must be used for this purpose. Please consult GE Vernova for information regarding the specification and supply of KITZ devices. The following figure demonstrates a typical K-Bus connection.

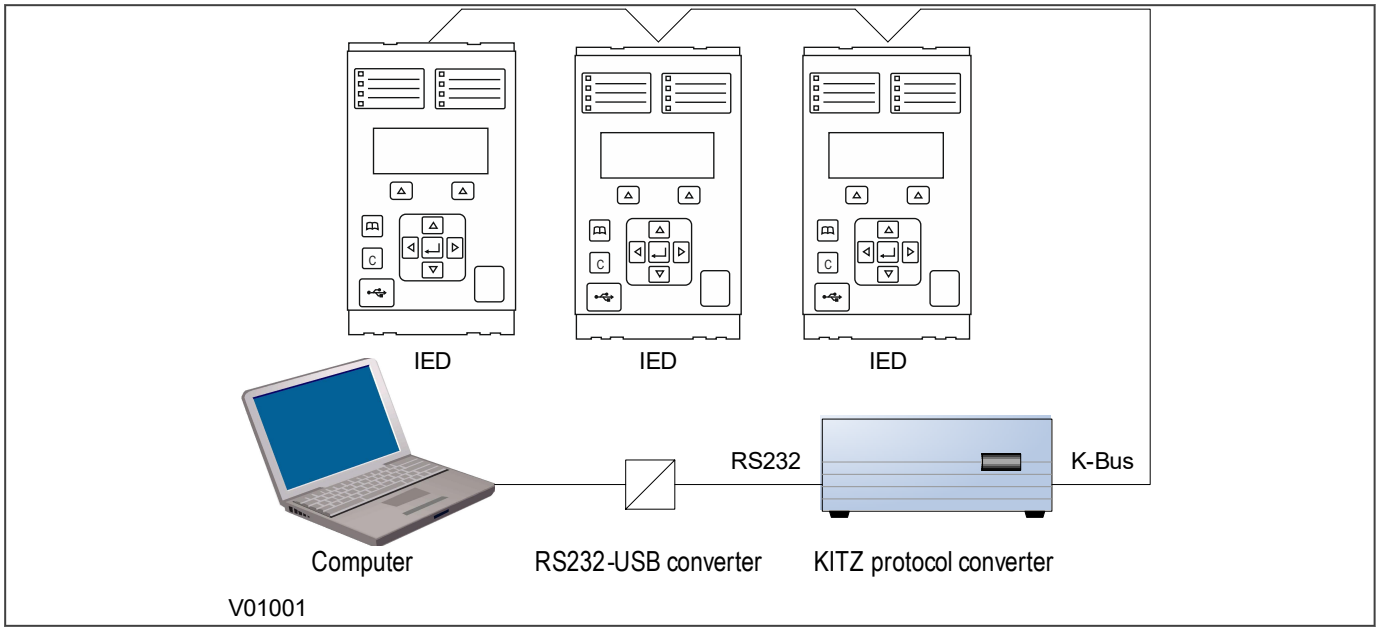


**Figure 271: Remote communication using K-Bus**

*Note:*
*An RS232-USB converter is only needed if the local computer does not provide an RS232 port.*

Further information about K-Bus is available in the publication R6509: K-Bus Interface Guide, which is available on request.

## 22.4 ETHERNET COMMUNICATION

The type of Ethernet board depends on the chosen model. The available boards and their features are described in the Hardware Design chapter of this manual.

The Ethernet interface is required for IEC 61850, and the Ethernet interface also offers communication with the S1 Agile settings application software for remote configuration and record extraction.

Fibre optic connection is recommended for use in permanent connections in a substation environment, as it offers advantages in terms of noise rejection. The fibre optic ports provide 100 Mbps communication and use either ST or LC connectors, depending on the board chosen. Fibres should be suitable for 1300 nm transmission and be multimode 50/125 µm or 62.5/125 µm.

Some Ethernet boards provide "copper" 100Base-TX ports using an RJ45 connector.

## 22.5 ETHERNET BOARD VERSIONS

Each board combines Ethernet communications, with IRIG-B timing functionality. There is a choice of embedded protocols for the Ethernet communications, and two types of IRIG-B.

### Board variants

| Board | Part No. | Compatible With |
|---|---|---|
| Redundant Ethernet PRP/HSR/RSTP/Failover, 2 multi-mode fibre ports + Modulated/Un-Modulated IRIG-B | ZN0087 001 | Any PRP, HSR, RSTP or standard Ethernet network. |
| Redundant Ethernet PRP/HSR/RSTP/Failover, 2 copper ports RJ45 + Modulated/Un-Modulated IRIG-B | ZN0087 002 | Any PRP, HSR, RSTP or standard Ethernet network. |
| Redundant Ethernet PRP/HSR/RSTP/Failover, 1 copper port RJ45 + 1 multi-mode fibre port + Modulated/Un-Modulated IRIG-B | ZN0087 003 | Any PRP, HSR, RSTP or standard Ethernet network. |

When using any of the redundant Ethernet boards on an IED the final product will have two MAC addresses and will require two IP addresses, one for the managed embedded switch that handles the redundancy and one for the IED that handles the communications at protocol level and to S1 Agile. The MAC address of the embedded switch is printed on the board. The MAC address of the IED is printed on the rear panel of the IED. The redundant Ethernet board is fitted into Slot A of the IED, which is the optional communications slot.

All Ethernet connections are made with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST® connector). The boards support IEC 61850 over Ethernet.

## 22.6 BOARD CONNECTIONS

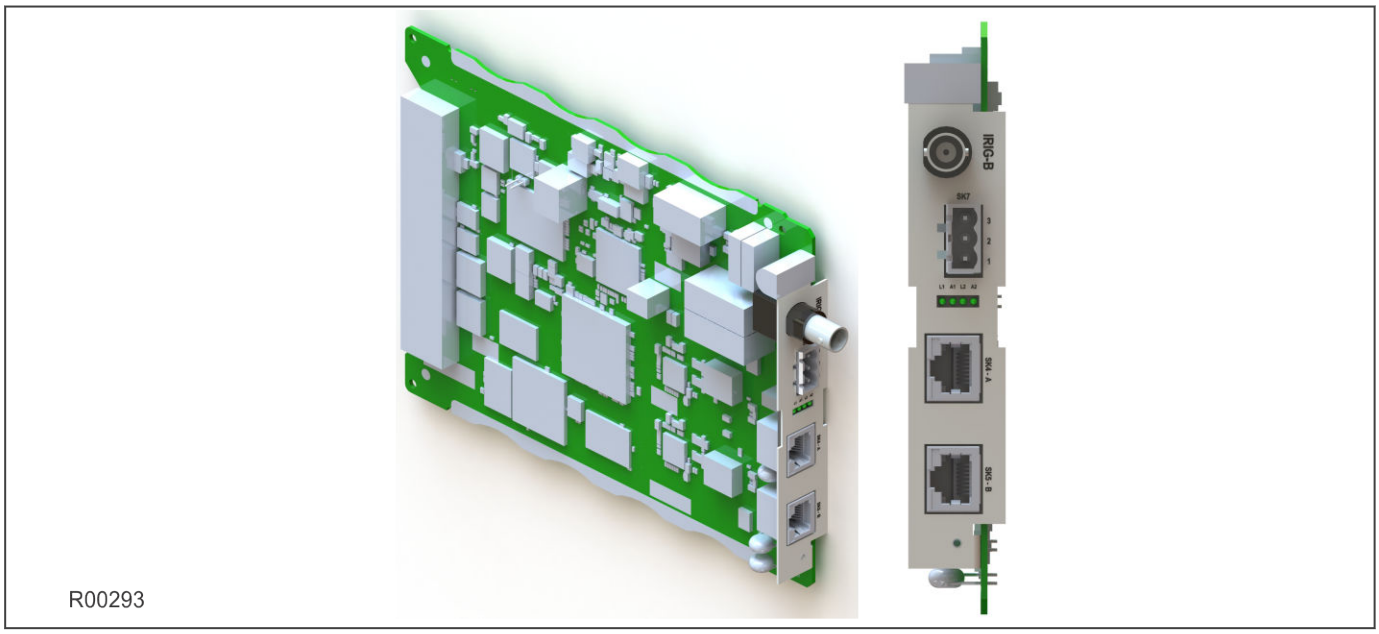


**Figure 272: Board connectors**

### IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

### Link Fail Connector (Ethernet Board Watchdog Relay)

| Pin | Closed | Open |
|---|---|---|
| 1-2 | Link fail Channel 1 (A) | Link ok Channel 1 (A) |
| 2-3 | Link fail Channel 2 (B) | Link ok Channel 2 (B) |

### LEDs

| LED | Function | On | Off | Flashing |
|---|---|---|---|---|
| Green | Link | Link ok | Link broken | |
| Yellow | Activity | Running | | PRP, RSTP traffic |

### Optical Fibre Connectors (ST)

| Connector | RSTP | PRP | HSR |
|---|---|---|---|
| A | RX1 | RXA | RXA |
| B | TX1 | TXA | TXA |
| C | RX2 | RXB | RXB |
| D | TX2 | TXB | TXB |

# 22.7 CONFIGURING IP ADDRESSES

An IP address is a logical address assigned to devices in a computer network that uses the Internet Protocol (IP) for communication between nodes. IP addresses are stored as binary numbers but they are represented using Decimal Dot Notation, where four sets of decimal numbers are separated by dots as follows:

XXX.XXX.XXX.XXX

For example:

10.86.254.85

An IP address in a network is usually associated with a subnet mask. The subnet mask defines which network the device belongs to. A subnet mask has the same form as an IP address.

For example:

255.255.255.0

Both the IED and the REB each have their own IP address. The following diagram shows the IED as IP1 and the REB as IP2.

*Note:*
*IP1 and IP2 are different but use the same subnet mask.*

The REB IP address (IP2) must be configured through the Ethernet network.

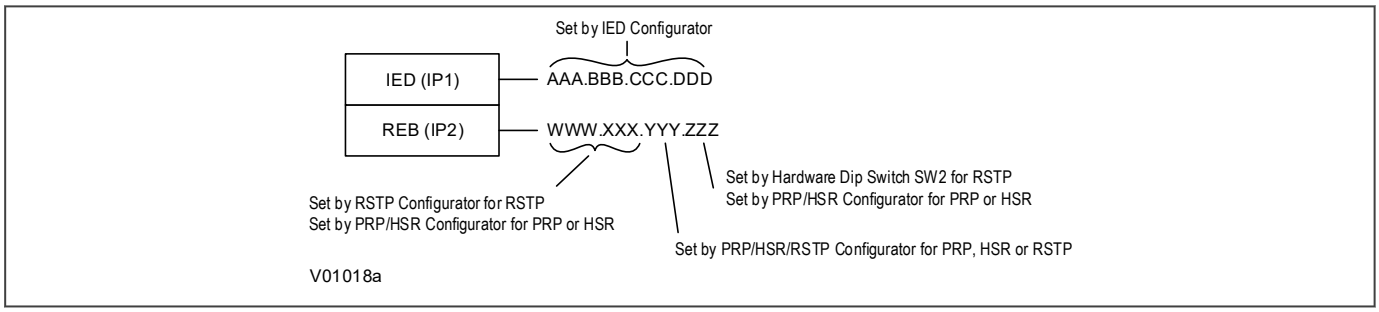


**Figure 273: IED and REB IP address configuration**

## 22.7.1 CONFIGURING THE IED IP ADDRESS

If the relay supports IEC 61850, set the IED IP1 address using the IEC 61850 Configurator software. In the IEC 61850 Configurator, set **Media** to **Single Copper or Redundant Fibre** for all Redundant Ethernet Board variants.

If the relay supports DNP3 over Ethernet, set the IED IP1 address by editing the DNP3 file, using the DNP3 Configurator software. In the DNP3 Configurator, set **Ethernet Media** to **Copper**, even though the redundant Ethernet network uses fibre optic cables.

## 22.7.2 CONFIGURING THE REB IP ADDRESS

The board IP address must be configured before connecting the IED to the network to avoid an IP address conflict. The way you configure the IP address depends on the redundancy protocol you have chosen.

### PRP/HSR/RSTP/Failover

From S1 Agile 2.0.1. onwards cards that support the PRP/HSR/RSTP/Failover protocols in any of the combinations are configured using the Redundant Ethernet Configurator software tool. If you are using a ZN008700X card only this tool supports it. If using S1 Agile 1.4.2 or older you will need to use the PRP/HSR Configurator for PRP and/or HSR, and the RSTP Configurator for RSTP cards.

| Board | Part No. | Compatible With |
|---|---|---|
| Redundant Ethernet PRP/HSR/RSTP/Failover, 2 multi-mode fibre ports + Modulated/Un-Modulated IRIG-B | ZN0087 001 | Redundant Ethernet Configurator (S1 Agile 2.0.1 onwards) |
| Redundant Ethernet PRP/HSR/RSTP/Failover, 2 copper ports RJ45 + Modulated/Un-Modulated IRIG-B | ZN0087 002 | Redundant Ethernet Configurator (S1 Agile 2.0.1 onwards) |
| Redundant Ethernet PRP/HSR/RSTP/Failover, 1 copper port RJ45 + 1 multi-mode fibre port + Modulated/Un-Modulated IRIG-B | ZN0087 003 | Redundant Ethernet Configurator (S1 Agile 2.0.1 onwards) |

# 22.8 REDUNDANT ETHERNET CONFIGURATOR

The Redundant Ethernet Configurator tool is intended for MiCOM Px4x IEDs with redundant Ethernet using PRP (Parallel Redundancy Protocol), HSR (High-availability Seamless Redundancy), RSTP (Rapid Spanning Tree Protocol) or Failover. This tool is used to identify IEDs, switch between PRP, HSR, RSTP and Failover, configure their parameters, configure the redundancy IP address, or configure the SNTP IP address.

## 22.8.1 CONNECTING THE IED TO A PC

Connect the IED to the PC on which the Configurator tool is used. This connection is done through an Ethernet switch or through a media converter.

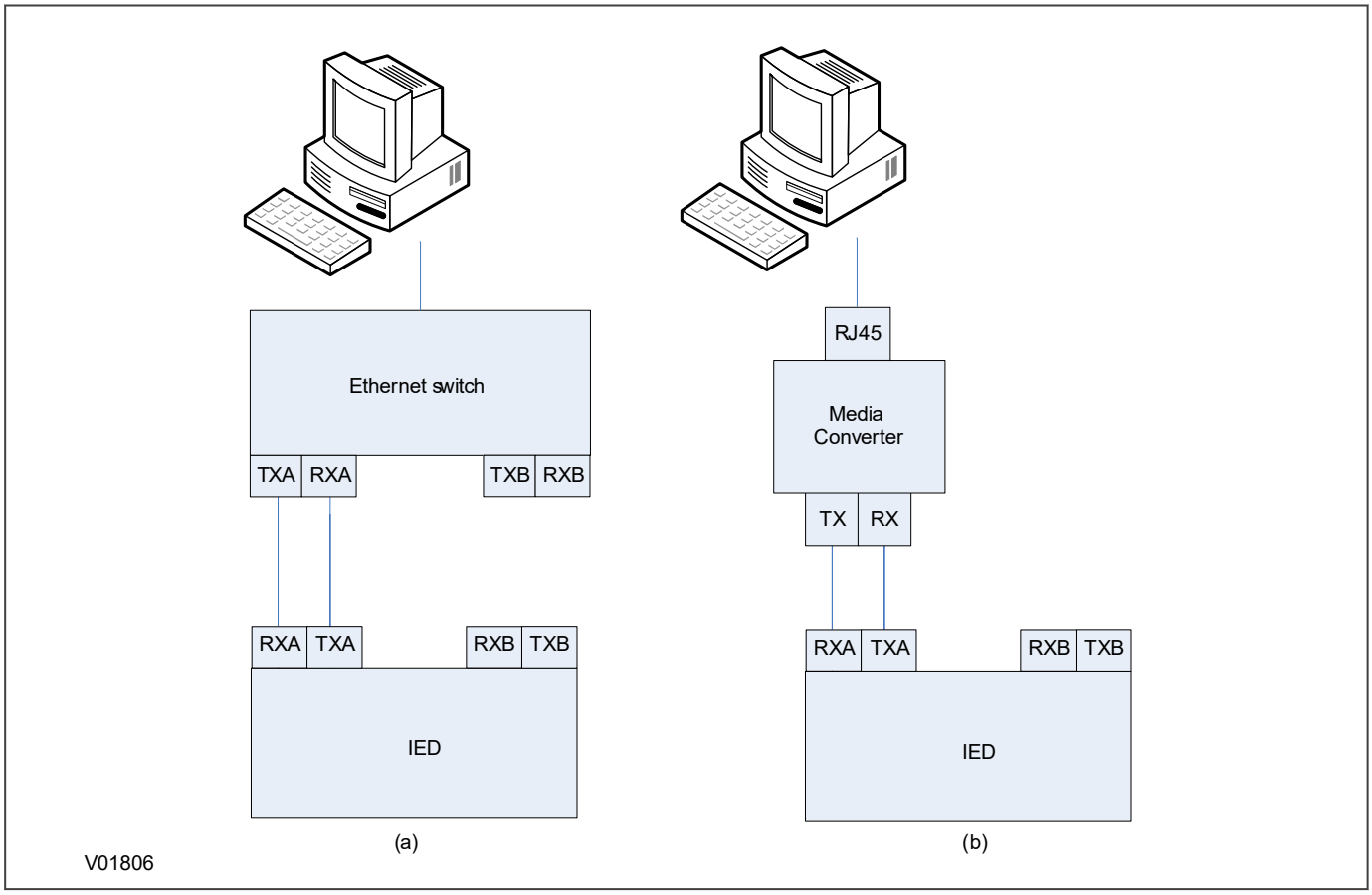


**Figure 274: Connection using (a) an Ethernet switch and (b) a media converter**

## 22.8.2 INSTALLING THE CONFIGURATOR

The Redundant Ethernet Configurator is installed as part of S1 Agile 2.0.1 onwards.

### 22.8.3 STARTING THE CONFIGURATOR

To start the configurator:

1. Go to S1 Agile and select the **Ethernet Configuration** tile, then select the **Redundant Ethernet Configurator** tile.
2. The Login screen appears. For user mode login, enter the **Login name** as **User** and click **OK** with no password. This level allows for IP address changes only. For Admin mode login, enter the **Login name** as **Admin** and password **Admin** and click **OK**. This level allows for network protocol configurations.
3. If the login screen does not appear, check all network connections.
4. From the **Network Board** drop-down list select the Network Board, IP Address and MAC Address of the PC in which the Configurator is running.

### 22.8.4 DEVICE IDENTIFICATION

To configure the redundant Ethernet board, go to the main window and click the **Identify Device** button. A list of devices are shown with the following details:

- Device address
- MAC address
- Version number of the firmware
- SNTP IP address
- Date & time of the real-time clock, from the board.

Select the device you wish to configure. The MAC address of the selected device is highlighted.

### 22.8.5 SELECTING THE DEVICE MODE

You must now select the device mode that you wish to use. This will be either PRP, HSR, RSTP or Failover. To do this, select the appropriate radio button then click the **Update** button. You will be asked to confirm a device reboot. Click **OK** to confirm.

### 22.8.6 FILTER BY BOARD TYPE

Once the list has been populated you can use the filter option to show only Process Bus cards or Station Bus cards by selecting the appropriate checkbox.

### 22.8.7 PASSWORD CONFGURATION

To assign a password the current password needs to be input first, then a new password can be given. The default password is AAAA.

If the password does not follow NERC rules a message will be shown. Click on the **NERC Rules** button to review the rules.

If the password is not known then the password can be recovered by using the **Recover Password** button and following the instructions.

### 22.8.8 IP ADDRESS CONFIGURATION

To change the network address component of the IP address:

1. From the main window click the **IP Config** button. The **Device setup** screen appears.
2. Enter the required board IP address and click **OK**. This is the network address for the redundancy card, not the IED IP address, which is set in the IED Configurator or DNP3.0 over Ethernet section.
3. The board network address is updated and displayed in the main window.

### 22.8.9 SNTP IP ADDRESS CONFIGURATION

If using SNMP to poll information from the REB an SNTP server can be used to synchronise the time of the reported messages. To configure the SNTP server IP address:

1. From the main window click the **SNTP Config** button. The **Device setup** screen appears.
2. Enter the required **MAC SNTP address** and server **IP SNTP Address**. Click **OK**.
3. The updated MAC and IP SNTP addresses appear in the main screen.

### 22.8.10 CHECK MAC TABLE FOR CONNECTED EQUIPMENT

To check what devices are connected to the device being monitored:

1. From the main window, select the device.
2. Click the **MAC Table** button.
3. At the bottom of the main window, a box shows the ports where devices are connected and their MAC addresses.

### 22.8.11 PRP CONFIGURATION

To view or configure the PRP Parameters:

1. Ensure that you have set the device mode to **PRP**.
2. Click the **PRP/HSR Configuration** button. The **PRP Configuration Parameters** screen appears.
3. To view the available parameters, click the **Get PRP Parameters** button.
4. To change the parameters, click the **Set Parameters** button and modify their values.

If you need to restore the default values of the parameters, click the **Restore Defaults** button.

The configurable parameters are as follows:

- **Multicast Address**: Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
- **Node Forget Time**: This is the time after which a node entry is cleared in the nodes table.
- **Life Check Interval**: This defines how often a node sends a PRP_Supervision frame. All DANPs shall be configured with the same Life Check Interval.

### 22.8.12 HSR CONFIGURATION

To view or configure the HSR Parameters:

1. Click the **PRP/HSR Configuration** button. The **HSR Configuration Parameters** screen appears.
2. To view the available parameters in the board that is connected, click the **Get HSR Parameters** button.
3. To change the parameters, click the **Set HSR Parameters** button and modify their values.

If you need to restore the default values of the parameters, click the **Restore Defaults** button.

The configurable parameters are as follows:

- **Multicast Address**: Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
- **Node Forget Time**: This is the time after which a node entry is cleared in the nodes table.
- **Life Check Interval**: This defines how often a node sends a PRP Supervision frame. All DANPs must be configured with the same Life Check Interval.

- **Proxy Node Table Forget Time**: This is the time after which a node entry is cleared in the ProxyTable.
- **Proxy Node Table Max Entries**: This is the maximum number of entries in the ProxyTable.
- **Entry Forget Time**: This is the time after which an entry is removed from the duplicates.
- **Node Reboot Interval**: This is the minimum time during which a node that reboots remains silent.

## 22.8.13 RSTP CONFIGURATION

1. To view or configure the RSTP Bridge Parameters, from the main window, click the device address to select the device. The selected device MAC address appears highlighted.
2. Click the **RSTP Configuration** button. The **RSTP Configuration** screen appears.
3. To view the available parameters in the board that is connected, click the **Get RSTP Parameters** button.
4. To set the configurable parameters such as Bridge Max Age, Bridge Hello Time, Bridge Forward Delay, and Bridge Priority, modify the parameter values according to the following table and click **Set RSTP Parameters**.

| S.No | Parameter | Default Value (second) | Minimum Value (second) | Maximum Value (second) |
|---|---|---|---|---|
| 1 | Bridge Max Age | 20 | 6 | 40 |
| 2 | Bridge Hello Time | 2 | 1 | 10 |
| 3 | Bridge Forward Delay | 15 | 4 | 30 |
| 4 | Bridge Priority | 32768 | 0 | 61440 |

## 22.8.14 BRIDGE PARAMETERS

To read the RSTP bridge parameters from the board,

1. From the main window click the device address to select the device. The **RSTP Configuration** window appears and the default tab is **Bridge Parameters**.
2. Click the **Get RSTP Parameters** button. This displays all the RSTP bridge parameters from the Ethernet board.
3. To modify the RSTP parameters, enter the values and click **Set RSTP Parameters**.
4. To restore the default values, click **Restore Default** and click **Set RSTP Parameters**.

The grayed parameters are read-only and cannot be modified.

*Note:*
*When assigning the bridge priority, make sure the root of the network is the Ethernet switch, not the IEDs. This reduces the number of hops to reach all devices in the network. Also make sure the priority values for all IEDs are higher than that of the switch.*

## 22.8.15 PORT PARAMETERS

This function is useful if you need to view the parameters of each port.

1. From the main window, click the device address to select the device. The **RSTP Configuration** window appears.
2. Select the **Port Parameters** tab, then click **Get Parameters** to read the port parameters. Alternatively, select the port numbers to read the parameters.

## 22.8.16 PORT STATES

This is used to see which ports of the board are enabled or disabled.

1. From the main window, click the device address to select the device. The **RSTP Configuration** window appears.
2. Select the **Port States** tab then click the **Get Port States** button. This lists the ports of the Ethernet board. A tick shows they are enabled.

## 22.8.17 FAILOVER CONFIGURATION

To view or configure the Failover Parameters:

Click the **Failover Configuration** button. The **Failover Configuration** screen appears.

1. To view the available parameters in the board that is connected, click the **Get Failover Parameters** button.
2. To change the parameters, click the **Set Failover Parameters** button and modify their values.

If you need to restore the default values of the parameters, click the **Restore Defaults** button. The configurable parameters are as follows:

- Port A and Port B select your main port for the Failover (Port A is the port at the top of your REB).
- The Failover time defines how long it takes for the redundancy switch over to trigger. The minimum value is 2s.

## 22.8.18 FILTERING DATABASE

The Filtering Database is used to determine how frames are forwarded or filtered across the Redundant Ethernet Board (REB). Filtering information specifies the set of ports to which frames received from a specific port are forwarded. The REB examines each received frame to see if the frame's destination address matches a source address listed in the Filtering Database. If there is a match, the device uses the filtering/forwarding information for that source address to determine how to forward or filter the frame. Otherwise the frame is forwarded to all the ports in the REB.

### General tab

The Filtering Database contains two types of entry; static and dynamic. The Static Entries are the source addresses entered by an administrator. The Dynamic Entries are the source addresses learnt by the switch process. The Dynamic Entries are removed from the Filtering Database after the Ageing Time. The Database holds a maximum of 1024 entries.

1. To access the forwarding database functions, if required, click the Filtering Database button in the main window
2. To view the Forwarding Database Size, Number of Static Entries and Number of Dynamic Entries, click **Read Database Info**
3. To set the Ageing Time, enter the number of seconds in the text box and click the **Set** button

### Filtering Entries tab

The **Filtering Entries** section allows to set the Static MAC addresses and read dynamic ones. This will likely not be used in any application.

### Goose Filtering tab

The Filtering entries section allows to set the Static MAC addresses and read dynamic ones. This will likely not be used in any application. The GOOSE Filtering allows to filter GOOSE from being received based on Multicast MAC addresses. This can be done either by clicking on the checkboxes or by typing the desired range.

### 22.8.19 END OF SESSION

To finish the session:

1. In the main window, click the **Quit** button, a new screen appears.
2. If a database backup is required, click **Yes**, a new screen appears.
3. Click the **...** button to browse the path. Enter the name in the text box.

# 22.9 REDUNDANT ETHERNET COMMUNICATION

Redundancy is required where a single point of failure cannot be tolerated. It is required in critical applications such as substation automation. Redundancy acts as an insurance policy, providing an alternative route if one route fails.

Ethernet communication redundancy is available for most GE Vernova products, using a Redundant Ethernet Board (REB). The REB is a Network Interface Card (NIC), which incorporates an integrated Ethernet switch. The board provides two Ethernet transmitter/receiver pairs.

In addition to the two Ethernet transmitter/receiver pairs, the REB provides link activity indication in the form of LEDs, link fail indication in the form of watchdog contacts, and a dedicated time synchronisation input.

The dedicated time synchronisation input is designed to connect to an IRIG-B signal. Both modulated and un-modulated IRIG-B formats are supported according to the selected option. Simple Network Time Protocol (SNTP) is supported over the Ethernet communications.

## 22.9.1 SUPPORTED PROTOCOLS

A range of Redundant Ethernet Boards are available to support different protocols for different requirements. One of the key requirements of substation redundant communications is "bumpless" redundancy. This means the ability to transfer from one communication path to another without noticeable consequences. Standard protocols of the time could not meet the demanding requirements of network availability for substation automation solutions. Switch-over times were unacceptably long. For this reason, companies developed proprietary protocols. More recently, however, standard protocols, which support bumpless redundancy (namely PRP and HSR) have been developed and ratified.

As well as supporting standard non-bumpless protocols such as RSTP, the REB was originally designed to support bumpless redundancy, using proprietary protocols (SHP, DHP) before the standard protocols became available. Since then, variants have been produced for the newer standard protocols.

REB variants for each of the following protocols are available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- RSTP (Rapid Spanning Tree Protocol)
- Failover

*Note:*
*The protocol you require must be selected at the time of ordering.*

## 22.9.2 PARALLEL REDUNDANCY PROTOCOL

PRP (Parallel Redundancy Protocol) is defined in IEC 62439-3. PRP provides bumpless redundancy and meets the most demanding needs of substation automation. The PRP implementation of the REB is compatible with any standard PRP device.

PRP uses two independent Ethernet networks operating in parallel. PRP systems are designed so that there should be no common point of failure between the two networks, so the networks have independent power sources and are not connected together directly.

Devices designed for PRP applications have two ports attached to two separate networks and are called Doubly Attached Nodes (DAN). A DAN has two ports, one MAC address and one IP address.

The sending node replicates each frame and transmits them over both networks. The receiving node processes the frame that arrives first and discards the duplicate. Therefore there is no distinction between the working and backup path. The receiving node checks that all frames arrive in sequence and that frames are correctly received on both ports.

Devices such as printers that have a single Ethernet port can be connected to either of the networks but will not directly benefit from the PRP principles. Such devices are called Singly Attached Nodes (SAN). For devices with a single Ethernet port that need to connect to both LANs, this can be achieved by employing Ethernet Redundancy Boxes (sometimes abbreviated to RedBox). Devices with a single Ethernet port that connect to both LANs by means of a RedBox are known as Virtual DAN (VDAN).

The figure below summarises DAN, SAN, VDAN, LAN, and RedBox connectivity.

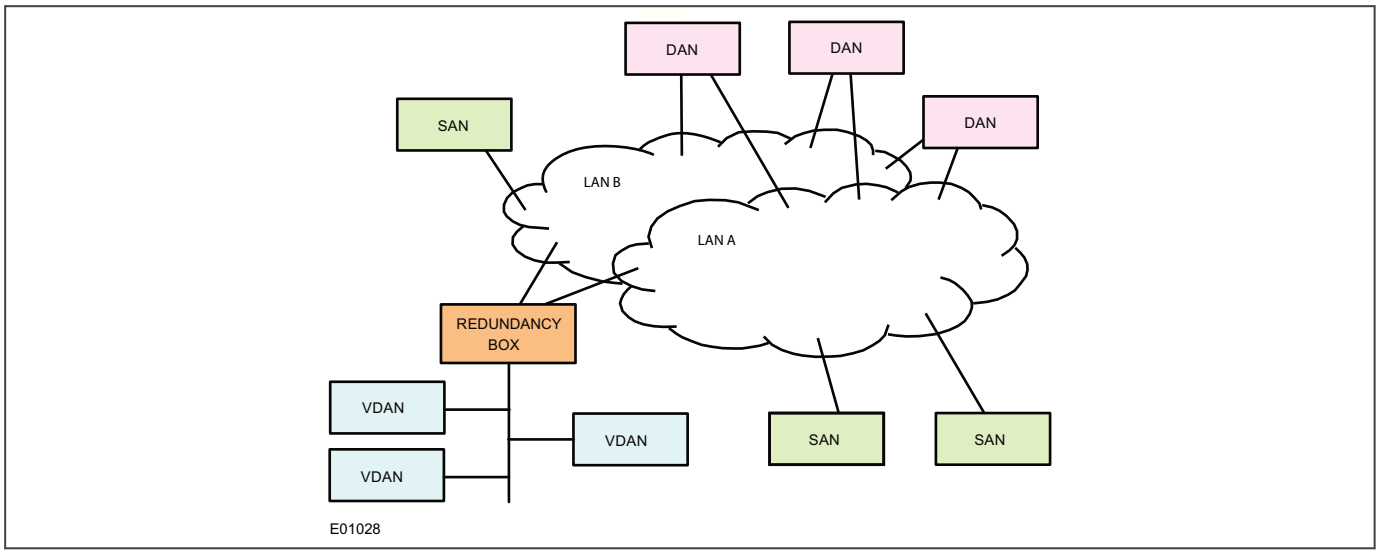


**Figure 275: IED attached to separate LANs**

In a DAN, both ports share the same MAC address so it does not affect the way devices talk to each other in an Ethernet network (Address Resolution Protocol at layer 2). Every data frame is seen by both ports.

When a DAN sends a frame of data, the frame is duplicated on both ports and therefore on both LAN segments. This provides a redundant path for the data frame if one of the segments fails. Under normal conditions, both LAN segments are working and each port receives identical frames.

## 22.9.3 HIGH-AVAILABILITY SEAMLESS REDUNDANCY (HSR)

HSR is standardized in IEC 62439-3 (clause 5) for use in ring topology networks. Similar to PRP, HSR provides bumpless redundancy and meets the most demanding needs of substation automation. HSR has become the reference standard for ring-topology networks in the substation environment. The HSR implementation of the redundancy Ethernet board (REB) is compatible with any standard HSR device.

HSR works on the premise that each device connected in the ring is a doubly attached node running HSR (referred to as DANH). Similar to PRP, singly attached nodes such as printers are connected via Ethernet Redundancy Boxes (RedBox).

### 22.9.3.1 HSR MULTICAST TOPOLOGY

When a DANH is sending a multicast frame, the frame (C frame) is duplicated (A frame and B frame), and each duplicate frame A/B is tagged with the destination MAC address and the sequence number. The frames A and B differ only in their sequence number, which is used to identify one frame from the other. Each frame is sent to the network via a separate port. The destination DANH receives two identical frames, removes the HSR tag of the first frame received and passes this (frame D) on for processing. The other duplicate frame is discarded. The nodes forward frames from one port to the other unless it was the node that injected it into the ring.

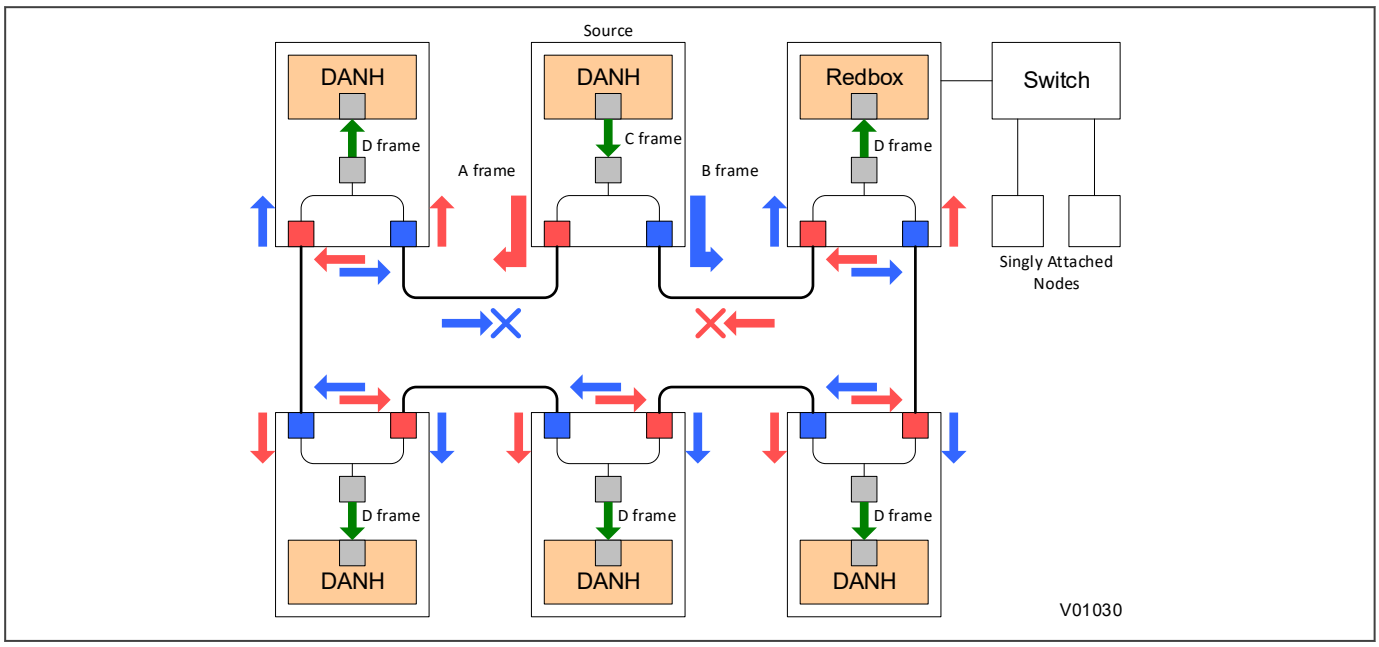


**Figure 276: HSR multicast topology**

Only about half of the network bandwidth is available in HSR for multicast or broadcast frames because both duplicate frames A & B circulate the full ring.

### 22.9.3.2 HSR UNICAST TOPOLOGY

With unicast frames, there is just one destination and the frames are sent to that destination alone. All non-recipient devices simply pass the frames on. They do not process them in any way. In other words, D frames are produced only for the receiving DANH. This is illustrated below.

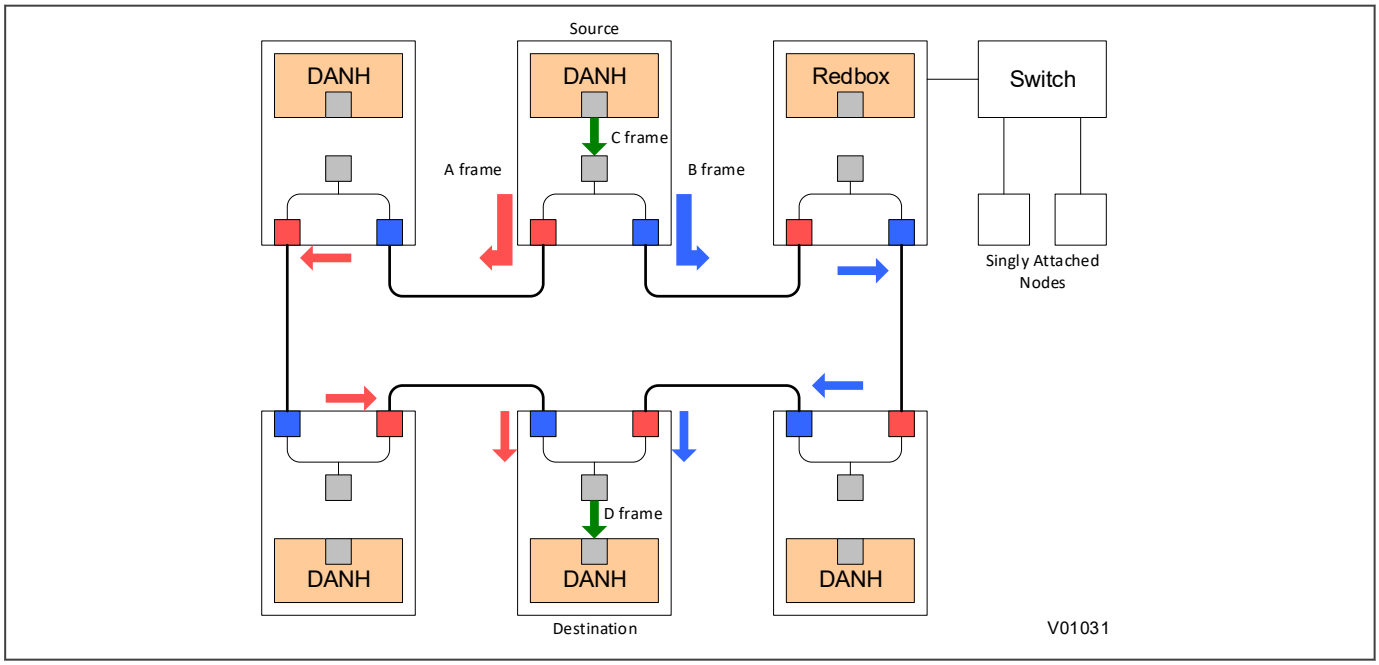


**Figure 277: HSR unicast topology**

For unicast frames, the whole bandwidth is available as both frames A & B stop at the destination node.

### 22.9.3.3 HSR APPLICATION IN THE SUBSTATION

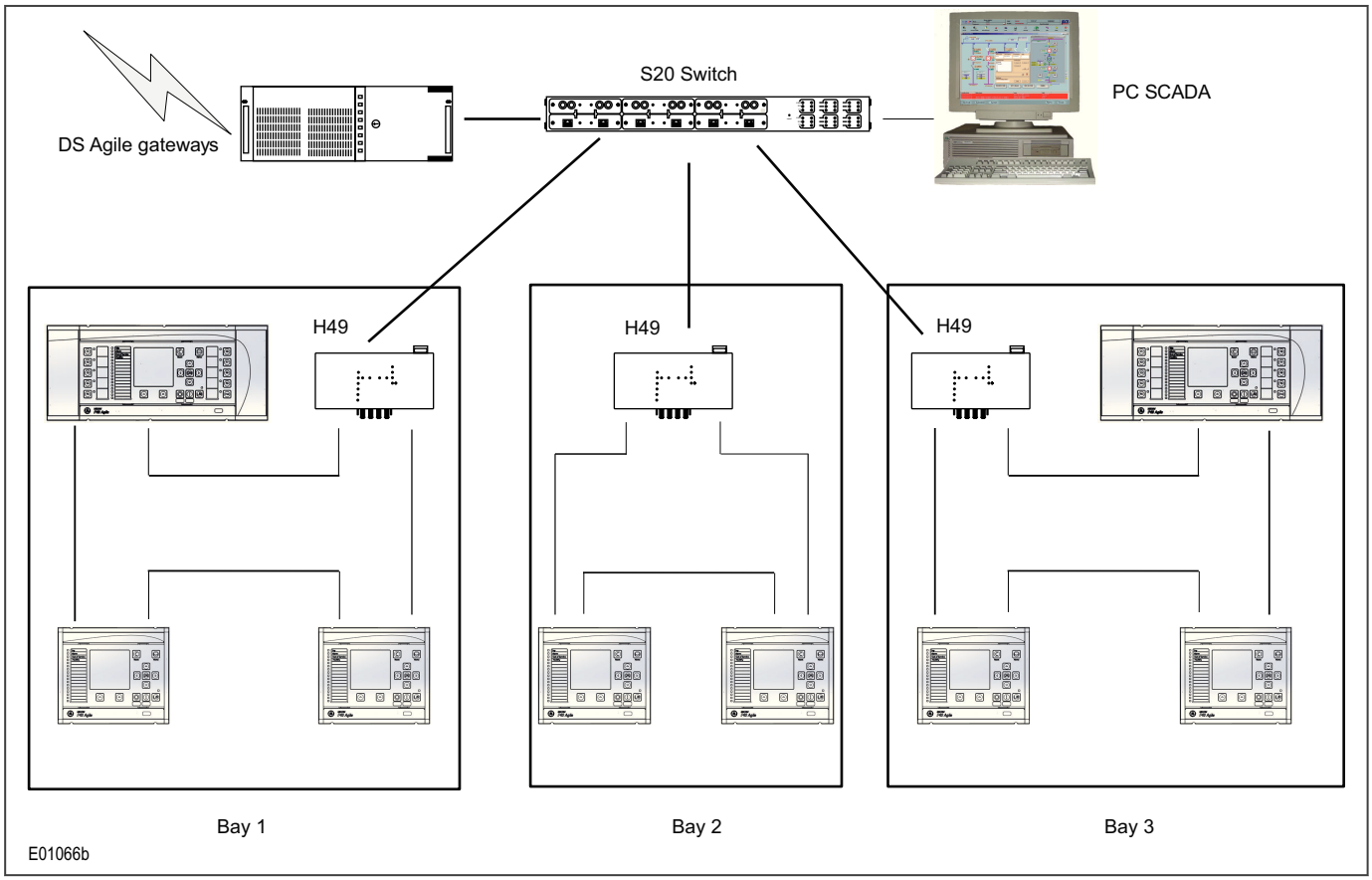


**Figure 278: HSR application in the substation**

## 22.9.4 RAPID SPANNING TREE PROTOCOL

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path. It stops network loops whilst enabling redundancy. It can be used in star or ring connections as shown in the following figure.

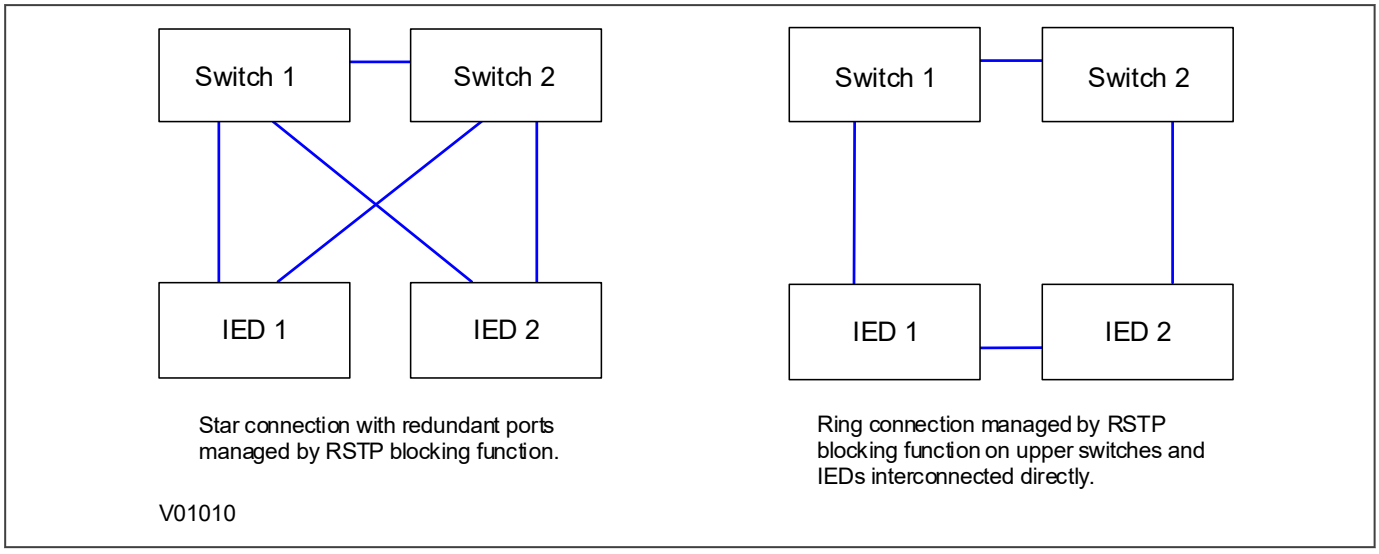


**Figure 279: IED attached to redundant Ethernet star or ring circuit**

The RSTP implementation in this product is compatible with any devices that use RSTP.

RSTP can recover network faults quickly, but the fault recovery time depends on the number of devices on the network and the network topology. A typical figure for the fault recovery time is 300ms. Therefore, RSTP cannot achieve the “bumpless” redundancy that some other protocols can.

Refer to IEEE 802.1D 2004 standard for detailed information about the oepration of the protocol.

### 22.9.5 FAILOVER

Failover is a simple redundancy mechanism that is not tied to any protocol. It works by selecting a main port and a switching time that can be as low as 2 seconds. When the main port link fails, the redundant port becomes physically active. At no point are both ports physically active, which means it can be used on any redundant or non-redundant network.

# 22.10 GENERAL FUNCTIONS FOR REDUNDANT ETHERNET BOARDS

The following functions apply to all redundant Ethernet protocols.

## 22.10.1 FORWARDING

The MiCOM Ethernet switch products support store and forward mode. The switch forwards messages with known addresses to the appropriate port. The messages with unknown addresses, the broadcast messages and the multicast messages are forwarded out to all ports except the source port. MiCOM switches do not forward error packets, 802.3x pause frames, or local packets. 802.1p priority tagging is enabled on all ports.

## 22.10.2 SIMPLE NETWORK MANAGEMENT PROTOCOL (SNMP)

Simple Network Management Protocol (SNMP) is a network protocol designed to manage devices in an IP network. SNMP uses a Management Information Base (MIB) that contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read or set using SNMP with the appropriate software. The information in the MIB is standardized.

Each system in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

The SNMP-related branches of the MIB tree are located in the internet branch, which contains two main types of branches:

- Public branches (mgmt=2), which are defined by the Internet Engineering Task Force (IETF).
- Private branches (private=4), which are assigned by the Internet Assigned Numbers Authority (IANA). These are defined by the companies and organizations to which these branches are assigned.

The following figure shows the structure of the SNMP MIB tree. There are no limits on the width and depth of the MIB tree.

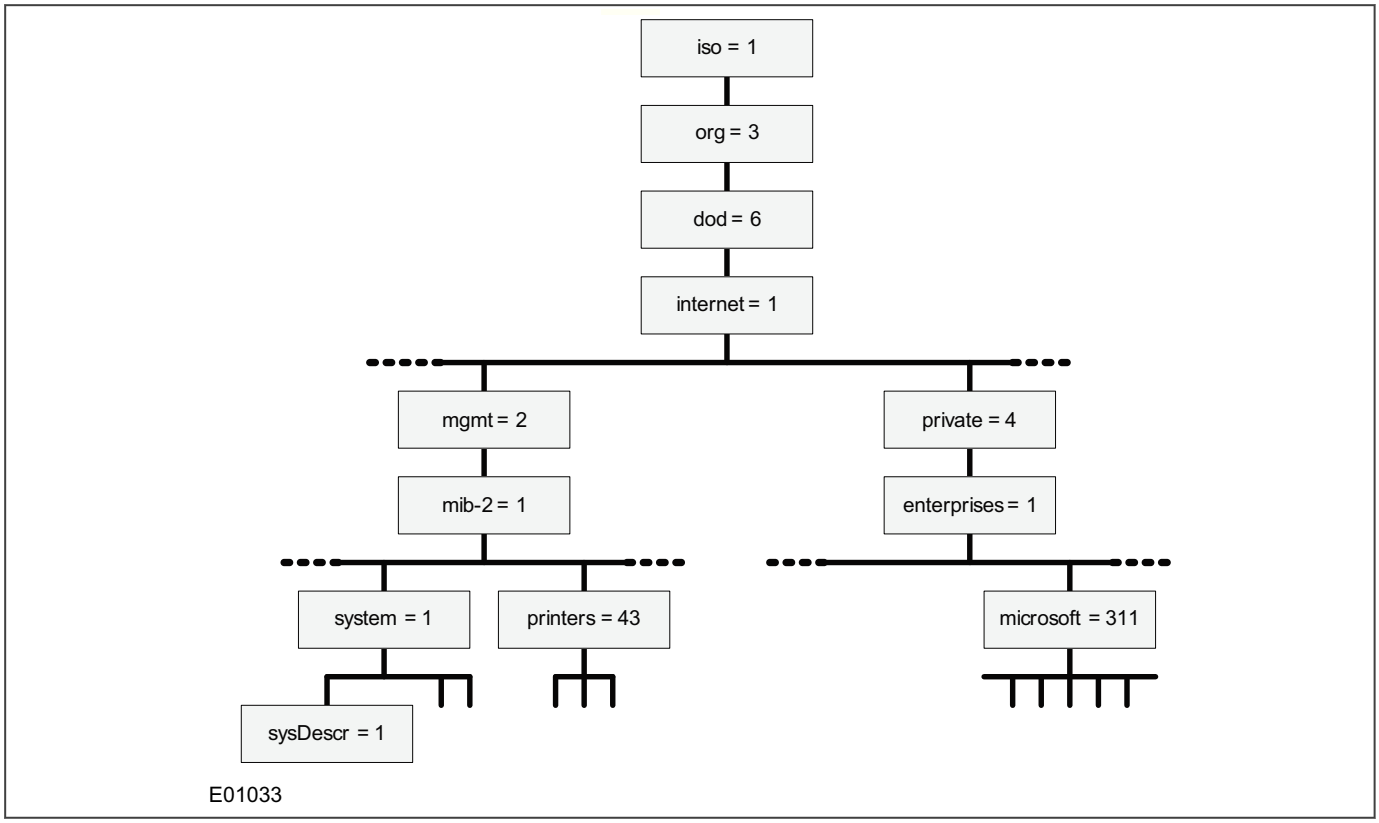


**Figure 280: SNMP MIB tree**

The top four levels of the hierarchy are fixed. These are:

- International Standards Organization (iso)
- Organization (org)
- Department of Defence (dod)
- Internet

Management (mgmt) is the main public branch. It defines network management parameters common to devices from all vendors. Underneath the Management branch is MIB-II (mib-2), and beneath this are branches for common management functions such as system management, printers, host resources, and interfaces.

The private branch of the MIB tree contains branches for large organizations, organized under the enterprises branch. This is not applicable to GE Vernova.

## 22.10.3 SNMP MIB STRUCTURE FOR RSTP

Our MIB uses three types of OID:

- sysDescr
- sysUpTime
- sysName

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | CCITT |
| | 1 | | | | | | | | | | | ISO |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 3 | | | | | | | | | Org |
| | | | | 6 | | | | | | | | DOD |
| | | | | | 1 | | | | | | | Internet |
| | | | | | | 2 | | | | | | mgmt |
| | | | | | | | 1 | | | | | Mib-2 |
| | | | | | | | | 1 | | | | sys |
| | | | | | | | | | 1 | | | sysDescr |
| | | | | | | | | | 3 | | | sysUpTime |
| | | | | | | | | | 4 | | | sysName |
| Remote Monitoring | | | | | | | | | | | | |
| | | | | | | | | 16 | | | | RMON |
| | | | | | | | | | 1 | | | statistics |
| | | | | | | | | | | 1 | | etherstat |
| | | | | | | | | | | | 1 | etherStatsEntry |
| | | | | | | | | | | | 9 | etherStatsUndersizePkts |
| | | | | | | | | | | | 10 | etherStatsOversizePkts |
| | | | | | | | | | | | 12 | etherStatsJabbers |
| | | | | | | | | | | | 13 | etherStatsCollisions |
| | | | | | | | | | | | 14 | etherStatsPkts64Octets |
| | | | | | | | | | | | 15 | etherStatsPkts65to127Octets |
| | | | | | | | | | | | 16 | etherStatsPkts128to255Octets |
| | | | | | | | | | | | 17 | etherStatsPkts256to511Octets |
| | | | | | | | | | | | 18 | etherStatsPkts512to1023Octets |

Various SNMP client software tools can be used. We recommend using an SNMP MIB browser, which can perform the basic SNMP operations such as GET, GETNEXT and RESPONSE.

*Note:*
*When communicating with the Redundant Ethernet Card, there are two IP addresses visible: one for the IED and one for the Ethernet switch on the redundant Ethernet board. To access the network using SNMP, use the IP address of the redundant Ethernet board switch and not that of the IED. See the Configuration chapter for further information.*

## 22.10.4 SNMP MIB STRUCTURE FOR PRP AND HSR

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | ITU |
| | 1 | | | | | | | | | | | ISO |
| | | 0 | | | | | | | | | | Standard |
| | | | 62439 | | | | | | | | | IECHighavailibility |
| | | | | 3 | | | | | | | | PRP |
| | | | | | 1 | | | | | | | linkRedundancyEntityObjects |
| | | | | | | 0 | | | | | | lreConfiguration |
| | | | | | | | 0 | | | | | lreConfigurationGeneralGroup |
| | | | | | | | | 1 | | | | lreManufacturerName |
| | | | | | | | | 2 | | | | lreInterfaceCount |
| | | | | | | | 1 | | | | | lreConfigurationInterfaceGroup |
| | | | | | | | | 0 | | | | lreConfigurationInterfaces |
| | | | | | | | | | 1 | | | lreInterfaceConfigTable |
| | | | | | | | | | | 1 | | lreInterfaceConfigEntry |
| | | | | | | | | | | | 1 | lreInterfaceConfigIndex |
| | | | | | | | | | | | 2 | lreRowStatus |
| | | | | | | | | | | | 3 | lreNodeType |
| | | | | | | | | | | | 4 | lreNodeName |
| | | | | | | | | | | | 5 | lreVersionName |
| | | | | | | | | | | | 6 | lreMacAddressA |
| | | | | | | | | | | | 7 | lreMacAddressB |
| | | | | | | | | | | | 8 | lreAdapterAdminStateA |
| | | | | | | | | | | | 9 | lreAdapterAdminStateB |
| | | | | | | | | | | | 10 | lreLinkStatusA |
| | | | | | | | | | | | 11 | lreLinkStatusB |
| | | | | | | | | | | | 12 | lreDuplicateDiscard |
| | | | | | | | | | | | 13 | lreTransparentReception |
| | | | | | | | | | | | 14 | lreHsrLREMode |
| | | | | | | | | | | | 15 | lreSwitchingEndNode |
| | | | | | | | | | | | 16 | lreRedBoxIdentity |
| | | | | | | | | | | | 17 | lreSanA |
| | | | | | | | | | | | 18 | lreSanB |
| | | | | | | | | | | | 19 | lreEvaluateSupervision |
| | | | | | | | | | | | 20 | lreNodesTableClear |
| | | | | | | | | | | | 21 | lreProxyNodeTableClear |
| | | | | | | 1 | | | | | | lreStatistics |
| | | | | | | | 1 | | | | | lreStatisticsInterfaceGroup |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 0 | | | | IreStatisticsInterfaces |
| | | | | | | | | | 1 | | | IreInterfaceStatsTable |
| | | | | | | | | | | | 1 | IreInterfaceStatsIndex |
| | | | | | | | | | | | 2 | IreCntTotalSentA |
| | | | | | | | | | | | 3 | IreCntTotalSentB |
| | | | | | | | | | | | 4 | IreCntErrWrongLANA |
| | | | | | | | | | | | 5 | IreCntErrWrongLANB |
| | | | | | | | | | | | 6 | IreCntReceivedA |
| | | | | | | | | | | | 7 | IreCntReceivedB |
| | | | | | | | | | | | 8 | IreCntErrorsA |
| | | | | | | | | | | | 9 | IreCntErrorsB |
| | | | | | | | | | | | 10 | IreCntNodes |
| | | | | | | | | | | | 11 | IreOwnRxCntA |
| | | | | | | | | | | | 12 | IreOwnRxCntB |
| | | | | | | | | | 3 | | | IreProxyNodeTable |
| | | | | | | | | | | 1 | | IreProxyNodeEntry |
| | | | | | | | | | | | 1 | reProxyNodeIndex |
| | | | | | | | | | | | 2 | reProxyNodeMacAddress |
| | | 3 | | | | | | | | | | Org |
| | | | 6 | | | | | | | | | Dod |
| | | | | 1 | | | | | | | | Internet |
| | | | | | 2 | | | | | | | mgmt |
| | | | | | | 1 | | | | | | mib-2 |
| | | | | | | | 1 | | | | | System |
| | | | | | | | | 1 | | | | sysDescr |
| | | | | | | | | 3 | | | | sysUpTime |
| | | | | | | | | 5 | | | | sysName |
| | | | | | | | | 7 | | | | sysServices |
| | | | | | | | 2 | | | | | interfaces |
| | | | | | | | | 2 | | | | ifTable |
| | | | | | | | | | 1 | | | ifEntry |
| | | | | | | | | | | 1 | | ifIndex |
| | | | | | | | | | | 2 | | ifDescr |
| | | | | | | | | | | 3 | | ifType |
| | | | | | | | | | | 4 | | ifMtu |
| | | | | | | | | | | 5 | | ifSpeed |
| | | | | | | | | | | 6 | | ifPhysAddress |
| | | | | | | | | | | 7 | | ifAdminStatus |
| | | | | | | | | | | 8 | | ifOpenStatus |
| | | | | | | | | | | 9 | | ifLastChange |
| | | | | | | | | | | 10 | | ifInOctets |
| | | | | | | | | | | 11 | | ifInUcastPkts |
| | | | | | | | | | | 12 | | ifInNUcastPkts |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 13 | | ifInDiscards |
| | | | | | | | | | | 14 | | ifInErrors |
| | | | | | | | | | | 15 | | ifInUnknownProtos |
| | | | | | | | | | | 16 | | ifOutOctets |
| | | | | | | | | | | 17 | | ifOutUcastPkts |
| | | | | | | | | | | 18 | | ifOutNUcastPkts |
| | | | | | | | | | | 19 | | ifOutDiscards |
| | | | | | | | | | | 20 | | ifOutErrors |
| | | | | | | | | | | 21 | | ifOutQLen |
| | | | | | | | | | | 22 | | ifSpecific |
| | | | | | | | 16 | | | | | rmon |
| | | | | | | | | 1 | | | | statistics |
| | | | | | | | | | 1 | | | etherStatsTable |
| | | | | | | | | | | 1 | | etherStatsEntry |
| | | | | | | | | | | | 1 | etherStatsIndex |
| | | | | | | | | | | | 2 | etherStatsDataSource |
| | | | | | | | | | | | 3 | etherStatsDropEvents |
| | | | | | | | | | | | 4 | etherStatsOctets |
| | | | | | | | | | | | 5 | etherStatsPkts |
| | | | | | | | | | | | 6 | etherStatsBroadcastPkts |
| | | | | | | | | | | | 7 | etherStatsMulticastPkts |
| | | | | | | | | | | | 8 | etherStatsCRCAlignErrors |
| | | | | | | | | | | | 9 | etherStatsUndersizePkts |
| | | | | | | | | | | | 10 | etherStatsOversizePkts |
| | | | | | | | | | | | 11 | etherStatsFragments |
| | | | | | | | | | | | 12 | etherStatsJabbers |
| | | | | | | | | | | | 13 | etherStatsCollisions |
| | | | | | | | | | | | 14 | etherStatsPkts64Octets |
| | | | | | | | | | | | 15 | etherStatsPkts65to127Octets |
| | | | | | | | | | | | 16 | etherStatsPkts128to255Octets |
| | | | | | | | | | | | 17 | etherStatsPkts256to511Octets |
| | | | | | | | | | | | 18 | etherStatsPkts512to1023Octets |
| | | | | | | | | | | | 19 | etherStatsPkts1024to1518Octets |
| | | | | | | | | | | | 20 | etherStatsOwner |
| | | | | | | | | | | | 21 | etherStatsStatus |

Various SNMP client software tools can be used. GE Vernova recommends using an SNMP MIB browser, which can perform the basic SNMP operations such as GET, GETNEXT and RESPONSE.

*Note:*
*When communicating with the Redundant Ethernet Card, there are two IP addresses visible: one for the IED and one for the Ethernet switch on the redundant Ethernet board. To access the network using SNMP, use the IP address of the redundant Ethernet board switch and not that of the IED. See the Configuration chapter for further information.*

## 22.11 SIMPLE NETWORK TIME PROTOCOL (SNTP)

Simple Network Time Protocol (SNTP) is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. A jitter buffer is used to reduce the effects of variable latency introduced by queuing, ensuring a continuous data stream over the network.

SNTP is supported by both the IED and the switch in the redundant Ethernet board. Both the IED and the redundant Ethernet board have their own IP address. Using the IP address of each device it can be synchronised to the SNTP server.

For the IED this is done by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software.

For the redundant Ethernet board, this is done using the Redundant Ethernet Configurator.

# 22.12 SIMPLE NETWORK MANAGEMENT PROTOCOL (SNMP)

Simple Network Management Protocol (SNMP) is a network protocol designed to manage devices in an IP network. The MiCOM P40 Modular products can provide up to two SNMP interfaces on Ethernet models; one to the IED's Main Processor for device level status information, and another directly to the redundant Ethernet board (where applicable) for specific Ethernet network level information.

Two versions of SNMP are supported: Version 2c, and a secure implementation of version 3 that includes cyber-security. Only the Main Processor SNMP interface supports Version 3.

## 22.12.1 SNMP MANAGEMENT INFORMATION BASES

SNMP uses a Management Information Base (MIB), which contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read using SNMP with the appropriate software. The information in the MIB is standardized.

Each device in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

## 22.12.2 MAIN PROCESSOR MIBS STRUCTURE

The Main Processor MIB uses a private OID with a specific number assigned by the IANA. Some items in this MIB also support SNMP traps (where indicated). These are items that can automatically notify a host without being read.

| Address | | | | | | | | | | | Name | Trigger Trap? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | ROOT NODE | |
| | 1 | | | | | | | | | | ISO | |
| | | 3 | | | | | | | | | Org | |
| | | | 6 | | | | | | | | DOD | |
| | | | | 1 | | | | | | | Internet | |
| | | | | | 4 | | | | | | Private | |
| | | | | | | 1 | | | | | Enterprise | |
| | | | | | | | 43534 | | | | (IANA No) | |
| | | | | | | | | 1 | | | Px4x | |
| | | | | | | | | | 1 | | System Data | |
| | | | | | | | | | | 1 | Description | YES |
| | | | | | | | | | | 2 | Plant Reference | YES |
| | | | | | | | | | | 3 | Model Number | NO |
| | | | | | | | | | | 4 | Serial Number | NO |
| | | | | | | | | | | 5 | Frequency | NO |
| | | | | | | | | | | 6 | Plant Status | YES |
| | | | | | | | | | | 7 | Active Group | YES |
| | | | | | | | | | | 8 | Software Ref.1 | NO |
| | | | | | | | | | | 9 | Software Ref.2 | NO |
| | | | | | | | | | | 10 | Access Level (UI) | YES |
| | | | | | | | | | 2 | | Date and Time | |

| Address | | | | | | | | | | | Name | Trigger Trap? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 1 | Date Time | NO |
| | | | | | | | | | | 2 | IRIG-B Status | YES |
| | | | | | | | | | | 3 | Battery Status | YES |
| | | | | | | | | | | 4 | Active Sync source | YES |
| | | | | | | | | | | 5 | SNTP Server 1 | NO |
| | | | | | | | | | | 6 | SNTP Server 2 | NO |
| | | | | | | | | | | 7 | SNTP Status | YES |
| | | | | | | | | | | 8 | PTP Status | YES |
| | | | | | | | | | 3 | | System Alarms | |
| | | | | | | | | | | 1 | Invalid Message Format | YES |
| | | | | | | | | | | 2 | Main Protection Fail | YES |
| | | | | | | | | | | 3 | Comms Changed | YES |
| | | | | | | | | | | 4 | Max Prop. Alarm | YES |
| | | | | | | | | | | 5 | 9-2 Sample Alarm | YES |
| | | | | | | | | | | 6 | 9-2LE Cfg Alarm | YES |
| | | | | | | | | | | 7 | Battery Fail | YES |
| | | | | | | | | | | 8 | Rear Communication Fail | YES |
| | | | | | | | | | | 9 | GOOSE IED Missing | YES |
| | | | | | | | | | | 10 | Intermicom loopback | YES |
| | | | | | | | | | | 11 | Intermicom message fail | YES |
| | | | | | | | | | | 12 | Intermicom data CD fail | YES |
| | | | | | | | | | | 13 | Intermicom Channel fail | YES |
| | | | | | | | | | | 14 | Backup setting fail | YES |
| | | | | | | | | | | 15 | User Curve commit to flash failure | YES |
| | | | | | | | | | | 16 | SNTP time Sync fail | YES |
| | | | | | | | | | | 17 | PTP failure alarm | YES |
| | | | | | | | | | 4 | | Device Mode | |
| | | | | | | | | | | 1 | IED Mod/Beh | YES |
| | | | | | | | | | | 2 | Simulation Mode of Subscription | YES |

## 22.12.3 REDUNDANT ETHERNET BOARD MIB STRUCTURE

The Redundant Ethernet board MIB uses three types of OID:

- sysDescr
- sysUpTime
- sysName

### MIB structure for RSTP

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | CCITT |
| | 1 | | | | | | | | | | | ISO |
| | | 3 | | | | | | | | | | Org |
| | | | 6 | | | | | | | | | DOD |
| | | | | 1 | | | | | | | | Internet |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 2 | | | | | | | mgmt |
| | | | | | | 1 | | | | | | Mib-2 |
| | | | | | | | 1 | | | | | sys |
| | | | | | | | | 1 | | | | sysDescr |
| | | | | | | | | 3 | | | | sysUpTime |
| | | | | | | | | 4 | | | | sysName |
| Remote Monitoring | | | | | | | | | | | | |
| | | | | | | | 16 | | | | | RMON |
| | | | | | | | | 1 | | | | statistics |
| | | | | | | | | | 1 | | | etherstat |
| | | | | | | | | | | 1 | | etherStatsEntry |
| | | | | | | | | | | | 9 | etherStatsUndersizePkts |
| | | | | | | | | | | | 10 | etherStatsOversizePkts |
| | | | | | | | | | | | 12 | etherStatsJabbers |
| | | | | | | | | | | | 13 | etherStatsCollisions |
| | | | | | | | | | | | 14 | etherStatsPkts64Octets |
| | | | | | | | | | | | 15 | etherStatsPkts65to127Octets |
| | | | | | | | | | | | 16 | etherStatsPkts128to255Octets |
| | | | | | | | | | | | 17 | etherStatsPkts256to511Octets |
| | | | | | | | | | | | 18 | etherStatsPkts512to1023Octets |

## MIB structure for PRP/HSR

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | ITU |
| | 1 | | | | | | | | | | | ISO |
| | | 0 | | | | | | | | | | Standard |
| | | | 62439 | | | | | | | | | IECHighavailibility |
| | | | | 3 | | | | | | | | PRP |
| | | | | | 1 | | | | | | | linkRedundancyEntityObjects |
| | | | | | | 0 | | | | | | IreConfiguration |
| | | | | | | | 0 | | | | | IreConfigurationGeneralGroup |
| | | | | | | | | 1 | | | | IreManufacturerName |
| | | | | | | | | 2 | | | | IreInterfaceCount |
| | | | | | | | 1 | | | | | IreConfigurationInterfaceGroup |
| | | | | | | | | 0 | | | | IreConfigurationInterfaces |
| | | | | | | | | | 1 | | | IreInterfaceConfigTable |
| | | | | | | | | | | 1 | | IreInterfaceConfigEntry |
| | | | | | | | | | | | 1 | IreInterfaceConfigIndex |
| | | | | | | | | | | | 2 | IreRowStatus |
| | | | | | | | | | | | 3 | IreNodeType |
| | | | | | | | | | | | 4 | IreNodeName |
| | | | | | | | | | | | 5 | IreVersionName |
| | | | | | | | | | | | 6 | IreMacAddressA |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | 7 | IreMacAddressB |
| | | | | | | | | | | | 8 | IreAdapterAdminStateA |
| | | | | | | | | | | | 9 | IreAdapterAdminStateB |
| | | | | | | | | | | | 10 | IreLinkStatusA |
| | | | | | | | | | | | 11 | IreLinkStatusB |
| | | | | | | | | | | | 12 | IreDuplicateDiscard |
| | | | | | | | | | | | 13 | IreTransparentReception |
| | | | | | | | | | | | 14 | IreHsrLREMode |
| | | | | | | | | | | | 15 | IreSwitchingEndNode |
| | | | | | | | | | | | 16 | IreRedBoxIdentity |
| | | | | | | | | | | | 17 | IreSanA |
| | | | | | | | | | | | 18 | IreSanB |
| | | | | | | | | | | | 19 | IreEvaluateSupervision |
| | | | | | | | | | | | 20 | IreNodesTableClear |
| | | | | | | | | | | | 21 | IreProxyNodeTableClear |
| | | | | | | 1 | | | | | | IreStatistics |
| | | | | | | | 1 | | | | | IreStatisticsInterfaceGroup |
| | | | | | | | | 0 | | | | IreStatisticsInterfaces |
| | | | | | | | | | 1 | | | IreInterfaceStatsTable |
| | | | | | | | | | | | 1 | IreInterfaceStatsIndex |
| | | | | | | | | | | | 2 | IreCntTotalSentA |
| | | | | | | | | | | | 3 | IreCntTotalSentB |
| | | | | | | | | | | | 4 | IreCntErrWrongLANA |
| | | | | | | | | | | | 5 | IreCntErrWrongLANB |
| | | | | | | | | | | | 6 | IreCntReceivedA |
| | | | | | | | | | | | 7 | IreCntReceivedB |
| | | | | | | | | | | | 8 | IreCntErrorsA |
| | | | | | | | | | | | 9 | IreCntErrorsB |
| | | | | | | | | | | | 10 | IreCntNodes |
| | | | | | | | | | | | 11 | IreOwnRxCntA |
| | | | | | | | | | | | 12 | IreOwnRxCntB |
| | | | | | | | | | 3 | | | IreProxyNodeTable |
| | | | | | | | | | | 1 | | IreProxyNodeEntry |
| | | | | | | | | | | | 1 | reProxyNodeIndex |
| | | | | | | | | | | | 2 | reProxyNodeMacAddress |
| | | 3 | | | | | | | | | | Org |
| | | | 6 | | | | | | | | | Dod |
| | | | | 1 | | | | | | | | Internet |
| | | | | | 2 | | | | | | | mgmt |
| | | | | | | 1 | | | | | | mib-2 |
| | | | | | | | 1 | | | | | System |
| | | | | | | | | 1 | | | | sysDescr |
| | | | | | | | | 3 | | | | sysUpTime |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 5 | | | | sysName |
| | | | | | | | | 7 | | | | sysServices |
| | | | | | | | 2 | | | | | interfaces |
| | | | | | | | | 2 | | | | ifTable |
| | | | | | | | | | 1 | | | ifEntry |
| | | | | | | | | | | 1 | | ifIndex |
| | | | | | | | | | | 2 | | ifDescr |
| | | | | | | | | | | 3 | | ifType |
| | | | | | | | | | | 4 | | ifMtu |
| | | | | | | | | | | 5 | | ifSpeed |
| | | | | | | | | | | 6 | | ifPhysAddress |
| | | | | | | | | | | 7 | | ifAdminStatus |
| | | | | | | | | | | 8 | | ifOpenStatus |
| | | | | | | | | | | 9 | | ifLastChange |
| | | | | | | | | | | 10 | | ifInOctets |
| | | | | | | | | | | 11 | | ifInUcastPkts |
| | | | | | | | | | | 12 | | ifInNUcastPkts |
| | | | | | | | | | | 13 | | ifInDiscards |
| | | | | | | | | | | 14 | | ifInErrors |
| | | | | | | | | | | 15 | | ifInUnknownProtos |
| | | | | | | | | | | 16 | | ifOutOctets |
| | | | | | | | | | | 17 | | ifOutUcastPkts |
| | | | | | | | | | | 18 | | ifOutNUcastPkts |
| | | | | | | | | | | 19 | | ifOutDiscards |
| | | | | | | | | | | 20 | | ifOutErrors |
| | | | | | | | | | | 21 | | ifOutQLen |
| | | | | | | | | | | 22 | | ifSpecific |
| | | | | | | | 16 | | | | | rmon |
| | | | | | | | | 1 | | | | statistics |
| | | | | | | | | | 1 | | | etherStatsTable |
| | | | | | | | | | | 1 | | etherStatsEntry |
| | | | | | | | | | | | 1 | etherStatsIndex |
| | | | | | | | | | | | 2 | etherStatsDataSource |
| | | | | | | | | | | | 3 | etherStatsDropEvents |
| | | | | | | | | | | | 4 | etherStatsOctets |
| | | | | | | | | | | | 5 | etherStatsPkts |
| | | | | | | | | | | | 6 | etherStatsBroadcastPkts |
| | | | | | | | | | | | 7 | etherStatsMulticastPkts |
| | | | | | | | | | | | 8 | etherStatsCRCAlignErrors |
| | | | | | | | | | | | 9 | etherStatsUndersizePkts |
| | | | | | | | | | | | 10 | etherStatsOversizePkts |
| | | | | | | | | | | | 11 | etherStatsFragments |
| | | | | | | | | | | | 12 | etherStatsJabbers |

| Address | | | | | | | | | | | | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | 13 | etherStatsCollisions |
| | | | | | | | | | | | 14 | etherStatsPkts64Octets |
| | | | | | | | | | | | 15 | etherStatsPkts65to127Octets |
| | | | | | | | | | | | 16 | etherStatsPkts128to255Octets |
| | | | | | | | | | | | 17 | etherStatsPkts256to511Octets |
| | | | | | | | | | | | 18 | etherStatsPkts512to1023Octets |
| | | | | | | | | | | | 19 | etherStatsPkts1024to1518Octets |
| | | | | | | | | | | | 20 | etherStatsOwner |
| | | | | | | | | | | | 21 | etherStatsStatus |

## 22.12.4 ACCESSING THE MIB

Various SNMP client software tools can be used. We recommend using an SNMP MIB browser, which can perform the basic SNMP operations such as GET, GETNEXT and RESPONSE.

*Note:*
*There are two IP addresses visible when communicating with the Redundant Ethernet Card via the fibre optic ports: Use the one for the IED itself to the Main Processor SNMP interface, and use the one for the on-board Ethernet switch to access the Redundant Ethernet Board SNMP interface. See the configuration chapter for more information.*

## 22.12.5 MAIN PROCESSOR SNMP CONFIGURATION

You configure the main processor SNMP interface using the HMI panel. Two different versions are available; SNMPv2c and SNMPv3:

To enable the main processor SNMP interface:

1. Select the COMMUNICATIONS column and scroll to the SNMP PARAMETERS heading
2. You can select either v2C, V3 or both. Selecting None will disable the main processor SNMP interface.

### SNMP Trap Configuration

SNMP traps allow for unsolicited reporting between the IED and up to two SNMP managers with unique IP addresses. The device MIB details what information can be reported using Traps. To configure the SNMP Traps:

1. Move down to the cell ***Trap Dest. IP 1*** and enter the IP address of the first destination SNMP manager. Setting this cell to `0.0.0.0` disables the first Trap interface.
2. Move down to the cell ***Trap Dest. IP 2*** and enter the IP address of the second destination SNMP manager. Setting this cell to `0.0.0.0` disables the Second Trap interface.

### SNMP V3 Security Configuration

SNMPv3 provides a higher level of security via authentication and privacy protocols. The IED adopts a secure SNMPv3 implementation with a user-based security model (USM).

Authentication is used to check the identity of users, privacy allows for encryption of SNMP messages. Both are optional, however you must enable authentication in order to enable privacy. To configure these security options:

1. If SNMPv3 has been enabled, set the ***Security Level*** setting. There are three levels; without authentication and without privacy (*noAuthNoPriv*), with authentication but without privacy (*authNoPriv*), and with authentication and with privacy (*authPriv*).
2. If Authentication is enabled, use the ***Auth Protocol*** setting to select the authentication type. There are two options: *HMAC-MD5-96* or *HMAC-SHA-96*.
3. Using the ***Auth Password*** setting, enter the 8-character password to be used by the IED for authentication.
4. If privacy is enabled, use the ***Encrypt Protocol*** setting to set the 8-character password that will be used by the IED for encryption.

*Note:*
*When setting the SNMP browser for RBAC compatible relays, the Context Name should be 'px4x'.*

### SNMP V2C Security Configuration

SNMPv2c implements authentication between the master and agent using a parameter called the ***Community Name***. This is effectively the password but it is not encrypted during transmission (this makes it inappropriate for some scenarios in which case version 3 should be used instead). To configure the SNMP 2c security:

1. If SNMPv2c has been enabled, use the ***Community Name*** setting to set the password that will be used by the IED and SNMP manager for authentication. This may be between one and 8 characters.

# 22.13 DATA PROTOCOLS

The products supports a wide range of protocols to make them applicable to many industries and applications. The exact data protocols supported by a particular product depend on its chosen application, but the following table gives a list of the data protocols that are typically available.

### DATA PROTOCOLS

| Data Protocol | Layer 1 Protocol | Description |
|---|---|---|
| Courier | USB, K-Bus, RS232, RS485, Ethernet | Standard for SCADA communications developed by GE Vernova. |
| MODBUS | RS485 | Standard for SCADA communications developed by Modicon. |
| IEC 60870-5-103 | RS485 | IEC standard for SCADA communications |
| DNP 3.0 | RS485 | Standard for SCADA communications |
| IEC 61850 | Ethernet | IEC standard for substation automation. Facilitates interoperability. |

The relationship of these protocols to the lower level physical layer protocols are as follows:

| Data Protocols | IEC 60870-5-103<br>MODBUS<br>DNP3.0<br>Courier | IEC 61850<br>Courier | Courier | Courier | Courier |
|---|---|---|---|---|---|
| **Data Link Layer** | EIA(RS)485 | Ethernet | EIA(RS)232 | K-Bus | USB |
| **Physical Layer** | Copper or Optical Fibre | | | | USB Type B |

## 22.13.1 COURIER

This section should provide sufficient detail to enable understanding of the Courier protocol at a level required by most users. For situations where the level of information contained in this manual is insufficient, further publications (R6511 and R6512) containing in-depth details about the protocol and its use, are available on request.

Courier is a GE Vernova proprietary communication protocol. Courier uses a standard set of commands to access a database of settings and data in the IED. This allows a master to communicate with a number of slave devices. The application-specific elements are contained in the database rather than in the commands used to interrogate it, meaning that the master station does not need to be preconfigured. Courier also provides a sequence of event (SOE) and disturbance record extraction mechanism.

### 22.13.1.1 PHYSICAL CONNECTION AND LINK LAYER

Courier can be used with four physical layer protocols: USB, K-Bus, EIA(RS)232 or EIA(RS)485.

Several connection options are available for Courier

- The front USB port (for connection to Settings application software on, for example, a laptop)
- Rear Port 1 (RP1) - for permanent SCADA connection via serial RS485 or K-Bus
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via serial optical fibre
- Optional Rear Port 2 (RP2) - for permanent SCADA connection via serial RS485, K-Bus, or RS232

Optional Ethernet board (NIC) - for remote communication with the S1 Agile settings application software across an Ethernet network.

For either of the serial rear ports, both the IED address and baud rate can be selected using the front panel menu or by the settings application software.

*Note:*
*Changing the **RP2 Port Config** setting (K-Bus, EIA(RS)232) requires the IED to be rebooted, for the change to become effective.*

### 22.13.1.2 COURIER DATABASE

The Courier database is two-dimensional and resembles a table. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255 (0000 to FFFF Hexadecimal. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The product-specific menu databases contain the complete database definition.

### 22.13.1.3 SETTINGS CATEGORIES

There are two main categories of settings in protection IEDs:

- Control and support settings
- Protection settings

With the exception of the Disturbance Recorder settings, changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to the Protection settings and the Disturbance Recorder settings are stored in 'scratchpad' memory and are not immediately implemented. These need to be committed by writing to the ***Save Changes*** cell in the *CONFIGURATION* column.

### 22.13.1.4 SETTING CHANGES

Courier provides two mechanisms for making setting changes. Either method can be used for editing any of the settings in the database.

#### Method 1

This uses a combination of three commands to perform a settings change:

First, enter Setting mode: This checks that the cell is settable and returns the limits.

1. Preload Setting: This places a new value into the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
2. Execute Setting: This confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
3. Abort Setting: This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are extracted before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

#### Method 2

The Set Value command can be used to change a setting directly. The response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method; however the limits are not extracted. This method is therefore most suitable for off-line setting editors such as MiCOM S1 Agile, or for issuing preconfigured control commands.

### 22.13.1.5 EVENT EXTRACTION

You can extract events either automatically (rear serial port only) or manually (either serial port). For automatic extraction, all events are extracted in sequential order using the Courier event mechanism. This includes fault and

maintenance data if appropriate. The manual approach allows you to select events, faults, or maintenance data as desired.

#### 22.13.1.5.1 AUTOMATIC EVENT RECORD EXTRACTION

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the ***Event*** bit is set in the ***Status*** byte. This indicates to the Master device that event information is available. The oldest, non-extracted event can be extracted from the IED using the ***Send Event*** command. The IED responds with the event data.

Once an event has been extracted, the ***Accept Event*** command can be used to confirm that the event has been successfully extracted. When all events have been extracted, the ***Event*** bit is reset. If there are more events still to be extracted, the next event can be accessed using the ***Send Event*** command as before.

#### 22.13.1.5.2 MANUAL EVENT RECORD EXTRACTION

The *VIEW RECORDS* column (location 01) is used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. You can select events by event number and directly select a fault or maintenance record by number.

##### Event Record Selection ('Select Event' cell: 0101)

This cell can be set the number of stored events. For simple event records (Type 0), cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

##### Fault Record Selection ('Select Fault' cell: 0105)

This cell can be used to select a fault record directly, using a value between 0 and 4 to select one of up to five stored fault records. (0 is the most recent fault and 4 is the oldest). The column then contains the details of the fault record selected.

##### Maintenance Record Selection ('Select Maint' cell: 01F0)

This cell can be used to select a maintenance record using a value between 0 and 4. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information, the number associated with a particular record changes when a new event or fault occurs.

##### Event Types

The IED generates events under certain circumstances such as:

- Change of state of output contact
- Change of state of opto-input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

### Event Record Format

The IED returns the following fields when the Send Event command is invoked:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Menu Database contains tables of possible events, and shows how the contents of the above fields are interpreted. Fault and Maintenance records return a Courier Type 3 event, which contains the above fields plus two additional fields:

- Event extraction column
- Event number

These events contain additional information, which is extracted from the IED using column B4. Row 01 contains a ***Select Record*** setting that allows the fault or maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the IED by uploading the text and data from the column.

## 22.13.1.6 DISTURBANCE RECORD EXTRACTION

The stored disturbance records are accessible through the Courier interface. The records are extracted using column (B4).

The ***Select Record*** cell can be used to select the record to be extracted. Record 0 is the oldest non-extracted record. Older records which have already been extracted are assigned positive values, while younger records are assigned negative values. To help automatic extraction through the rear port, the IED sets the ***Disturbance*** bit of the ***Status*** byte, whenever there are non-extracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from the ***Trigger Time*** cell (B402). The disturbance record can be extracted using the block transfer mechanism from cell B40B and saved in the COMTRADE format. The settings application software software automatically does this.

## 22.13.1.7 PROGRAMMABLE SCHEME LOGIC SETTINGS

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the IED using the block transfer mechanism.

The following cells are used to perform the extraction:

- ***Domain*** cell (B204): Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- ***Sub-Domain*** cell (B208): Used to select the Protection Setting Group to be uploaded or downloaded.
- ***Version*** cell (B20C): Used on a download to check the compatibility of the file to be downloaded.
- ***Transfer Mode*** cell (B21C): Used to set up the transfer process.
- ***Data Transfer*** cell (B120): Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the IED using this mechanism. The settings application software must be used to edit the settings. It also performs checks on the validity of the settings before they are transferred to the IED.

## 22.13.1.8 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the Courier protocol. The device will correct for the transmission delay. The time synchronization message may be sent as either a global command or to any individual IED address. If the time synchronization message is sent to an individual address, then the device will respond with a confirm message. If sent as a global command, the (same) command must be sent twice. A time

synchronization Courier event will be generated/produced whether the time-synchronization message is sent as a global command or to any individual IED address.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

### 22.13.1.9 COURIER CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 protocol***). This is a non-settable cell, which shows the chosen communication protocol – in this case `Courier`.

```
COMMUNICATIONS
RP1 Protocol
Courier
```

4. Move down to the next cell (***RP1 Address***). This cell controls the address of the RP1 port on the device. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 1 and 254 for the Relay Address. It is set to 255 by default, which has to be changed. It is important that no two IEDs share the same address.

```
COMMUNICATIONS
RP1 Address
100
```

5. Move down to the next cell (***RP1 InactivTimer***). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before revoking any password access that was enabled and discarding any changes. For the rear port this can be set between 1 and 30 minutes.

```
COMMUNICATIONS
RP1 Inactivtimer
10.00 mins.
```

6. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

```
COMMUNICATIONS
RP1 PhysicalLink
Copper
```

7. Move down to the next cell (***RP1 Card Status***). This cell is not settable. It displays the status of the chosen physical layer protocol for RP1.

```
COMMUNICATIONS
RP1 Card Status
K-Bus OK
```

8. Move down to the next cell (***RP1 Port Config***). This cell controls the type of serial connection. Select between K-Bus or RS485.

```
COMMUNICATIONS
RP1 Port Config
K-Bus
```

9. If using EIA(RS)485, the next cell (***RP1 Comms Mode***) selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity. If using K-Bus this cell will not appear.

```
COMMUNICATIONS
RP1 Comms Mode
IEC 60870 FT1.2
```

10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; 9600, 19200 and 38400. If using K-Bus this cell will not appear as the baud rate is fixed at 64 kbps.

```
COMMUNICATIONS
RP1 Baud rate
19200
```

## 22.13.2 IEC 60870-5-103

The specification IEC 60870-5-103 (Telecontrol Equipment and Systems Part 5 Section 103: Transmission Protocols), defines the use of standards IEC 60870-5-1 to IEC 60870-5-5, which were designed for communication with protection equipment.

This section describes how the IEC 60870-5-103 standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 60870-5-103 standard.

This section should provide sufficient detail to enable understanding of the standard at a level required by most users.

The IEC 60870-5-103 interface is a master/slave interface with the device as the slave device. The device conforms to compatibility level 2, as defined in the IEC 60870-5-103.standard.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (reset)
- Time synchronization
- Event record extraction
- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

### 22.13.2.1 PHYSICAL CONNECTION AND LINK LAYER

Two connection options are available for IEC 60870-5-103:

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

If the optional fibre optic port is fitted, a menu item appears in which the active port can be selected. However, the selection is only effective following the next power up.

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

### 22.13.2.2 INITIALISATION

Whenever the device has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The device will respond to either of the two reset commands; Reset CU or Reset FCB (Communication Unit or Frame Count Bit). The difference between the two commands is that the Reset CU command will clear any unsent messages in the transmit buffer, whereas the Reset FCB command does not delete any messages.

The device will respond to the reset command with an identification message ASDU 5. The Cause of Transmission (COT) of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Menu Database, available from GE Vernova separately if required.

In addition to the above identification message, it will also produce a power up event.

### 22.13.2.3 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The device will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send/confirm message then the device will respond with a confirm message. A time synchronization Class 1 event will be generated/produced whether the time-synchronization message is sent as a send confirm or a broadcast (send/no reply) message.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

### 22.13.2.4 SPONTANEOUS EVENTS

Events are categorized using the following information:

- Function type
- Information Number

The IEC 60870-5-103 profile in the Menu Database contains a complete listing of all events produced by the device.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for spontaneous communication, by settting the ***Config Mode*** cell to `Std+UserConfig`, and configuring the DDB masks as required.

### 22.13.2.5 GENERAL INTERROGATION (GI)

The GI request can be used to read the status of the device, the function numbers, and information numbers that will be returned during the GI cycle. These are shown in the IEC 60870-5-103 profile in the Menu Database.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for GI reporting, by setting the ***Config Mode*** cell to `Std+UserConfig`, and configuring the DDB masks as required.

### 22.13.2.6 CYCLIC MEASUREMENTS

The device will produce measured values using ASDU 9 on a cyclical basis, this can be read from the device using a Class 2 poll (note ADSU 3 is not used). The rate at which the device produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu or using MiCOM S1 Agile. It is active immediately following a change.

The device transmits its measurands with maximum value of 2.4 times the rated value of the measurement.

### 22.13.2.7 COMMANDS

A list of the supported commands is contained in the Menu Database. The device will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating 'negative acknowledgement'.

### 22.13.2.8 TEST MODE

It is possible to disable the device output contacts to allow secondary injection testing to be performed using either the front panel menu or the front serial port. The IEC 60870-5-103 standard interprets this as 'test mode'. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the device is in test mode will have a COT of 'test mode'.

### 22.13.2.9 DISTURBANCE RECORDS

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

*Note:*
*IEC 60870-5-103 only supports up to 8 records.*

### 22.13.2.10 COMMAND/MONITOR BLOCKING

The device supports a facility to block messages in the monitor direction (data from the device) and also in the command direction (data to the device). Messages can be blocked in the monitor and command directions using one of the two following methods

- The menu command ***RP1 CS103Blcking*** in the *COMMUNICATIONS* column
- The DDB signals Monitor Blocked and Command Blocked

### 22.13.2.11 IEC 60870-5-103 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the table cell, which shows the chosen communication protocol – in this case `IEC 60870-5-103`.

```
COMMUNICATIONS
RP1 Protocol
IEC 60870-5-103
```

4. Move down to the next cell (***RP1 Address***). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.

```
COMMUNICATIONS
RP1 address
162
```

5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Two baud rates are supported by the IED, `9600 bits/s` and `19200 bits/s`. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
9600 bits/s
```

6. Move down to the next cell (***RP1 Meas Period***). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

```
COMMUNICATIONS
RP1 Meas Period
30.00 s
```

7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

```
COMMUNICATIONS
RP1 PhysicalLink
Copper
```

8. The next cell down (***RP1 CS103Blcking***) can be used for monitor or command blocking.

```
COMMUNICATIONS
RP1 CS103Blcking
Disabled
```

9. There are three settings associated with this cell; these are:

| Setting: | Description: |
|---|---|
| Disabled | No blocking selected. |
| Monitor Blocking | When the monitor blocking DDB Signal is active high, either by energising an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a "Termination of general interrogation" message to the master station. |
| Command Blocking | When the command blocking DDB signal is active high, either by energising an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a "negative acknowledgement of command" message to the master station. |

## 22.13.3 DNP 3.0

This section describes how the DNP 3.0 standard is applied in the product. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the DNP 3.0 standard.

The descriptions given here are intended to accompany the device profile document that is included in the Menu Database document. The DNP 3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP 3.0 implementation. This is the standard format DNP 3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the device using DNP 3.0. The IED operates as a DNP 3.0 slave and supports subset level 2, as described in the DNP 3.0 standard, plus some of the features from level 3.

The DNP 3.0 protocol is defined and administered by the DNP Users Group. For further information on DNP 3.0 and the protocol specifications, please see the DNP website (www.dnp.org).

### 22.13.3.1 PHYSICAL CONNECTION AND LINK LAYER

DNP 3.0 can be used with EIA(RS)485.

Several connection options are available for DNP 3.0

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

The baud rate can be selected using the front panel menu or by the settings application software.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 stop bit and optional configurable parity bit.

### 22.13.3.2 OBJECT 1 BINARY INPUTS

Object 1, binary inputs, contains information describing the state of signals in the IED, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and opto-inputs, alarm signals, and protection start and trip signals. The 'DDB number' column in the device profile document provides the DDB numbers for the DNP 3.0 point data. These can be used to cross-reference to the DDB definition list. See the relevant Menu Database document. The binary input points can also be read as change events using Object 2 and Object 60 for class 1-3 event data.

*Note:*
*For the DNP Events to be transmitted it is mandatory to have the corresponding DDBs of the Configured Point Index to be included in the Courier Event Record. The RECORD CONTROL Menu lists all the DDBs, and the mask settings control their inclusion/exclusion as a Courier Event.*

### 22.13.3.3 OBJECT 10 BINARY OUTPUTS

Object 10, binary outputs, contains commands that can be operated using DNP 3.0. Therefore the points accept commands of type pulse on (null, trip, close) and latch on/off as detailed in the device profile in the relevant Menu Database document, and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the Control Inputs. Described as Alias Control Inputs, they reflect the state of the Control Input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

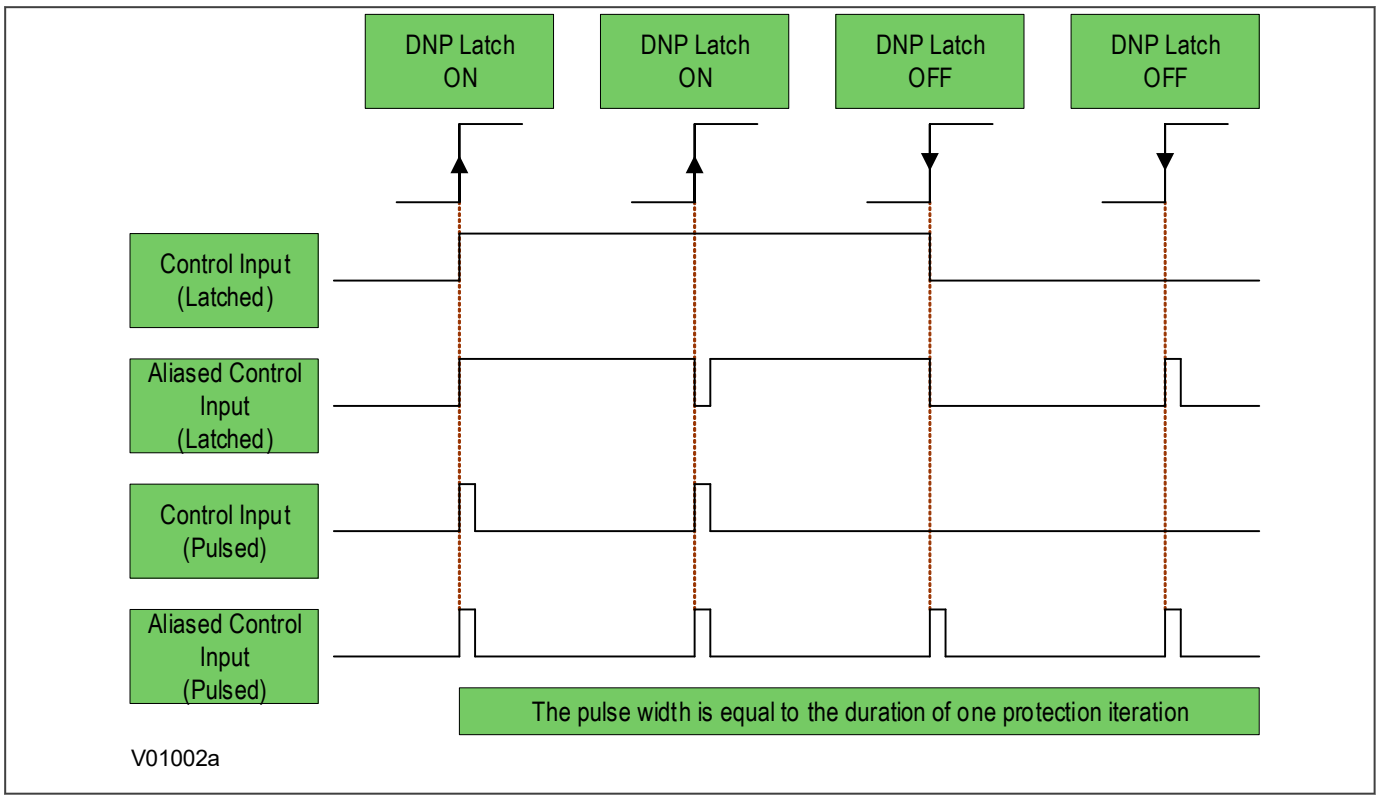


**Figure 281: Control input behaviour**

Many of the IED's functions are configurable so some of the Object 10 commands described in the following sections may not be available. A read from Object 10 reports the point as off-line and an operate command to Object 12 generates an error response.

Examples of Object 10 points that maybe reported as off-line are:

- Activate setting groups: Ensure setting groups are enabled
- CB trip/close: Ensure remote CB control is enabled
- Reset NPS thermal: Ensure NPS thermal protection is enabled
- Reset thermal O/L: Ensure thermal overload protection is enabled
- Reset RTD flags: Ensure RTD Inputs is enabled
- Control inputs: Ensure control inputs are enabled

### 22.13.3.4 OBJECT 20 BINARY COUNTERS

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from Object 20, or as a 'frozen' value from Object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding Object 21 frozen counter. The freeze and clear function resets the Object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from Object 22 and Object 23 respectively. Counter change events (Object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (Object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

#### 22.13.3.5 OBJECT 30 ANALOGUE INPUT

Object 30, analogue inputs, contains information from the IED's measurements columns in the menu. All object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the IED's CT and VT ratios), and this is settable in the *COMMUNICATIONS* column in the IED. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analogue measurement that is unavailable when it is read is reported as offline. For example, the frequency would be offline if the current and voltage frequency is outside the tracking range of the IED. All Object 30 points are reported as secondary values in DNP 3.0 (with respect to CT and VT ratios).

#### 22.13.3.6 OBJECT 40 ANALOGUE OUTPUT

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the IED such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

#### 22.13.3.7 OBJECT 50 TIME SYNCHRONISATION

Function codes 1 (read) and 2 (write) are supported for Object 50 (time and date) variation 1. The DNP Need Time function (the duration of time waited before requesting another time sync from the master) is supported, and is configurable in the range 1 - 30 minutes.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

#### 22.13.3.8 DNP3 DEVICE PROFILE

This section describes the specific implementation of DNP version 3.0 within GE Vernova MiCOM P40 Agile IEDs for both compact and modular ranges.

The devices use the DNP 3.0 Slave Source Code Library version 3 from Triangle MicroWorks Inc.

This document, in conjunction with the DNP 3.0 Basic 4 Document Set, and the DNP Subset Definitions Document, provides complete information on how to communicate with the devices using the DNP 3.0 protocol.

This implementation of DNP 3.0 is fully compliant with DNP 3.0 Subset Definition Level 2. It also contains many Subset Level 3 and above features.

##### 22.13.3.8.1 DNP3 DEVICE PROFILE TABLE

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

| DNP 3.0<br>Device Profile Document | |
|---|---|
| Vendor Name: | GE Vernova |
| Device Name: | MiCOM P40Agile Protection Relays - compact and modular range |
| Models Covered: | All models |
| Highest DNP Level Supported*:<br>* This is the highest DNP level FULLY supported. Parts of level 3 are also supported | For Requests: Level 2<br>For Responses: Level 2 |
| Device Function: | Slave |
| Notable objects, functions, and/or qualifiers supported in addition to the highest DNP levels supported (the complete list is described in the DNP 3.0 Implementation Table):<br>For static (non-change event) object requests, request qualifier codes 00 and 01 (start-stop), 07 and 08 (limited quantity), and 17 and 28 (index) are supported in addition to the request qualifier code 06 (no range (all points))<br>Static object requests sent with qualifiers 00, 01, 06, 07, or 08 will be responded with qualifiers 00 or 01<br>Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28<br>For change-event object requests, qualifiers 17 or 28 are always responded<br>16-bit and 32-bit analogue change events with time may be requested<br>The read function code for Object 50 (time and date) variation 1 is supported<br>Analogue Input Deadbands, Object 34, variations 1 through 3, are supported<br>Floating Point Analogue Output Status and Output Block Objects 40 and 41 are supported<br>Sequential file transfer, Object 70, variations 2 through 7, are supported<br>Device Attribute Object 0 is supported | |
| Maximum Data Link Frame Size (octets): | Transmitted: 292<br>Received: 292 |
| Maximum Application Fragment Size (octets) | Transmitted: Configurable (100 to 2048). Default 2048<br>Received: 249 |
| Maximum Data Link Retries: | Fixed at 2 |
| Maximum Application Layer Retries: | None |
| Requires Data Link Layer Confirmation: | Configurable to Never or Always |
| Requires Application Layer Confirmation: | When reporting event data (Slave devices only)<br>When sending multi-fragment responses (Slave devices only) |
| Timeouts while waiting for: | |
| Data Link Confirm: | Configurable |
| Complete Application Fragment: | None |
| Application Confirm: | Configurable |
| Complete Application Response: | None |
| Others: | |
| Data Link Confirm Timeout: | Configurable from 0 (Disabled) to 120s, default 10s. |
| Application Confirm Timeout: | Configurable from 1 to 120s, default 2s. |
| Select/Operate Arm Timeout: | Configurable from 1 to 10s, default 10s. |
| Need Time Interval (Set IIN1-4): | Configurable from 1 to 30, default 10min. |
| Application File Timeout | 60 s |
| Analog Change Event Scan Period: | Fixed at 0.5s |
| Counter Change Event Scan Period | Fixed at 0.5s |
| Frozen Counter Change Event Scan Period | Fixed at 1s |
| Maximum Delay Measurement Error: | 2.5 ms |
| Time Base Drift Over a 10-minute Interval: | 7 ms |

| DNP 3.0<br>Device Profile Document | |
|---|---|
| Sends/Executes Control Operations: | |
| Write Binary Outputs: | Never |
| Select/Operate: | Always |
| Direct Operate: | Always |
| Direct Operate - No Ack: | Always |
| Count > 1 | Never |
| Pulse On | Always |
| Pulse Off | Sometimes |
| Latch On | Always |
| Latch Off | Always |
| Queue | Never |
| Clear Queue | Never |
| Note: Paired Control points will accept Pulse On/Trip and Pulse On/Close, but only single point will accept the Pulse Off control command. | |
| Reports Binary Input Change Events when no specific variation requested: | Configurable to send one or the other |
| Reports time-tagged Binary Input Change Events when no specific variation requested: | Binary input change with time |
| Sends Unsolicited Responses: | Never |
| Sends Static Data in Unsolicited Responses: | Never<br>No other options are permitted |
| Default Counter Object/Variation: | Configurable, Point-by-point list attached<br>Default object: 20<br>Default variation: 1 |
| Counters Roll Over at: | 32 bits |
| Sends multi-fragment responses: | Yes |
| Sequential File Transfer Support: | |
| Append File Mode | No |
| Custom Status Code Strings | No |
| Permissions Field | Yes |
| File Events Assigned to Class | No |
| File Events Send Immediately | Yes |
| Multiple Blocks in a Fragment | No |
| Max Number of Files Open | 1 |

### 22.13.3.8.2 DNP3 IMPLEMENTATION TABLE

The implementation table provides a list of objects, variations and control codes supported by the device:

| Object | | | Request (Library Will Parse) | | | | Response (Library Will Respond With) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Object Number | Variation Number | Description | Function Codes (dec) | | Qualifier Codes (hex) | | Function Codes (dec) | | Qualifier Codes (hex) | |
| 1 | 0 | Binary Input (Variation 0 is used to request default variation) | 1<br>22 | (read)<br>(assign class) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |

| Object | | | Request (Library Will Parse) | | | | Response (Library Will Respond With) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Object Number | Variation Number | Description | Function Codes (dec) | | Qualifier Codes (hex) | | Function Codes (dec) | | Qualifier Codes (hex) | |
| 1 | 1 (default - see note 1) | Binary Input | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 1 | 2 | Binary Input with Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 2 | 0 | Binary Input Change - Any Variation | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| 2 | 1 | Binary Input Change without Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 2 | 2 | Binary Input Change with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 10 | 0 | Binary Output Status - Any Variation | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |
| 10 | 2 (default - see note 1) | Binary Output Status | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 12 | 1 | Control Relay Output Block | 3<br>4<br>5<br>6 | (select)<br>(operate)<br>(direct op)<br>(dir. op, noack) | 17, 28 | (index) | 129 | response | | echo of request |
| 20 | 0 | Binary Counter - Any Variation | 1<br>22 | (read)<br>(assign class) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |
| | | | 7<br>8<br>9<br>10 | (freeze)<br>(freeze noack)<br>(freeze clear)<br>(frz. cl. Noack) | 00, 01<br>06<br>07, 08 | (start-stop)<br>(no range, or all)<br>(limited qty) | | | | |
| 20 | 1 | 32-Bit Binary Counter with Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 20 | 2 | 16-Bit Binary Counter with Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 20 | 5 (default - see note 1) | 32-Bit Binary Counter without Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 20 | 6 | 16-Bit Binary Counter without Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 21 | 0 | Frozen Counter - Any Variation | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |
| 21 | 1 | 32-Bit Frozen Counter with Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 21 | 2 | 16-Bit Frozen Counter with Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 21 | 5 | 32-Bit Frozen Counter with Time of Freeze | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 1) |

| Object | | | Request (Library Will Parse) | | | | Response (Library Will Respond With) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Object Number | Variation Number | Description | Function Codes (dec) | | Qualifier Codes (hex) | | Function Codes (dec) | | Qualifier Codes (hex) | |
| 21 | 6 | 16-Bit Frozen Counter with Time of Freeze | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>17, 28 (index - see note 1) |
| 21 | 9<br>(default - see note 1) | 32-Bit Frozen Counter without Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 21 | 10 | 16-Bit Frozen Counter without Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| `22 | 0 | Counter Change Event - Any Variation | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| 22 | 1<br>(default - see note 1) | 32-Bit Counter Change Event without Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 22 | 2 | 16-Bit Counter Change Event without Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 22 | 5 | 32-Bit Counter Change Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 22 | 6 | 16-Bit Counter Change Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 23 | 0 | Frozen Counter Event (Variation 0 is used to request default variation) | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| 23 | 1<br>(default - see note 1) | 32-Bit Frozen Counter Event | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 23 | 2 | 16-Bit Frozen Counter Event | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 23 | 5 | 32-Bit Frozen Counter Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 23 | 6 | 16-Bit Frozen Counter Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 30 | 0 | Analog Input - Any Variation | 1<br>22 | (read)<br>(assign class) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |
| 30 | 1 | 32-Bit Analog Input | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 30 | 2 | 16-Bit Analog Input | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 30 | 3<br>(default - see note 1) | 32-Bit Analog Input without Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 30 | 4 | 16-Bit Analog Input without Flag | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 30 | 5 | Short floating point | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 32 | 0 | Analog Change Event - Any Variation | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| 32 | 1<br>(default - see note 1) | 32-Bit Analog Change Event without Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 32 | 2 | 16-Bit Analog Change Event without Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 32 | 3 | 32-Bit Analog Change Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |

| Object | | | Request (Library Will Parse) | | | | Response (Library Will Respond With) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Object Number | Variation Number | Description | Function Codes (dec) | | Qualifier Codes (hex) | | Function Codes (dec) | | Qualifier Codes (hex) | |
| 32 | 4 | 16-Bit Analog Change Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 32 | 5 | Short floating point Analog Change Event without Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 32 | 7 | Short floating point Analog Change Event with Time | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | 129 | response | 17, 28 | (index) |
| 34 | 0 | Analog Input Deadband (Variation 0 is used to request default variation) | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |
| 34 | 1 | 16 Bit Analog Input Deadband | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| | | | 2 | (write) | 00, 01<br>07, 08<br>17, 27, 28 | (start-stop)<br>(limited qty)<br>(index) | | | | |
| 34 | 2<br>(default - see note 1) | 32 Bit Analog Input Deadband | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| | | | 2 | (write) | 00, 01<br>07, 08<br>17, 27, 28 | (start-stop)<br>(limited qty)<br>(index) | | | | |
| 34 | 3 | Short Floating Point Analog Input Deadband | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| | | | 2 | (write) | 00, 01<br>07, 08<br>17, 27, 28 | (start-stop)<br>(limited qty)<br>(index) | | | | |
| 40 | 0 | Analog Output Status (Variation 0 is used to request default variation) | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | | | | |
| 40 | 1<br>(default - see note 1) | 32-Bit Analog Output Status | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 40 | 2 | 16-Bit Analog Output Status | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 40 | 3 | Short Floating Point Analog Output Status | 1 | (read) | 00, 01<br>06<br>07, 08<br>17, 27, 28 | (start-stop)<br>(no range, or all)<br>(limited qty)<br>(index) | 129 | response | 00, 01<br>17, 28 | (start-stop)<br>(index - see note 2) |
| 41 | 1 | 32-Bit Analog Output Block | 3<br>4<br>5<br>6 | (select)<br>(operate)<br>(direct op)<br>(dir. op, noack) | 17, 28<br>27 | (index)<br>(index) | 129 | response | | echo of request |
| 41 | 2 | 16-Bit Analog Output Block | 3<br>4<br>5<br>6 | (select)<br>(operate)<br>(direct op)<br>(dir. op, noack) | 17, 28<br>27 | (index)<br>(index) | 129 | response | | echo of request |
| 41 | 3 | Short Floating Point Analog Output Block | 3<br>4<br>5<br>6 | (select)<br>(operate)<br>(direct op)<br>(dir. op, noack) | 17, 27, 28 | (index) | 129 | response | | echo of request |
| 50 | 1<br>(default - see note 1) | Time and Date | 1 | (read) | 07 | (limited qty = 1) | 129 | response | 07 | (limited qty = 1) |
| | | | 2 | (write) | 07 | (limited qty = 1) | | | | |
| 60 | 0 | Not defined | | | | | | | | |
| 60 | 1 | Class 0 Data | 1 | (read) | 06 | (no range, or all) | | | | |
| 60 | 2 | Class 1 Data | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |

| Object | | | Request (Library Will Parse) | | | | Response (Library Will Respond With) | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Object Number | Variation Number | Description | Function Codes (dec) | | Qualifier Codes (hex) | | Function Codes (dec) | | Qualifier Codes (hex) | |
| | | | 22 | (assign class) | 06 | (no range, or all) | | | | |
| 60 | 3 | Class 2 Data | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| | | | 22 | (assign class) | 06 | (no range, or all) | | | | |
| 60 | 4 | Class 3 Data | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| | | | 22 | (assign class) | 06 | (no range, or all) | | | | |
| 70 | 0 | File Event - Any Variation | 1 | (read) | 06<br>07, 08 | (no range, or all)<br>(limited qty) | | | | |
| | | | 22 | (assign class) | 06 | (no range, or all) | | | | |
| 70 | 2 | File Authentication | 29 | (authenticate) | 5b | (free-format) | 129 | response | | 5B (free-format) |
| 70 | 3 | File Command | 25<br>27 | (open)<br>(delete) | 5b | (free-format) | | | | |
| 70 | 4 | File Command Status | 26<br>30 | (close)<br>(abort) | 5b | (free-format) | 129 | response | | 5B (free-format) |
| 70 | 5 | File Transfer | 1 | (read) | 5b | (free-format) | 129 | response | | 5B (free-format) |
| 70 | 6 | File Transfer Status | | | | | 129 | response | | 5B (free-format) |
| 70 | 7 | File Descriptor | 28 | (get file info) | 5b | (free-format) | 129 | response | | 5B (free-format) |
| 80 | 1 | Internal Indications | 1 | (read) | 00, 01 | (start-stop) | 129 | response | 00, 01 | (start-stop) |
| | | No Object (function code only) | 13 | (cold restart) | | | | | | |
| | | No Object (function code only) | 14 | (warm restart) | | | | | | |
| | | No Object (function code only) | 23 | (delay meas.) | | | | | | |

*Note:*
*A Default variation refers to the variation responded to when variation 0 is requested and/or in class 0, 1, 2, or 3 scans.*

*Note:*
*For static (non-change-event) objects, qualifiers 17 or 28 are only responded to when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded to with qualifiers 00 or 01. For change-event objects, qualifiers 17 or 28 are always responded to.*

### 22.13.3.8.3 DNP3 INTERNAL INDICATIONS

The following table lists the DNP3.0 Internal Indications (IIN) and identifies those that are supported by the device.

The IIN form an information element used to convey the internal states and diagnostic results of a device. This information can be used by a receiving station to perform error recovery or other suitable functions. The IIN is a two-octet field that follows the function code in all responses from the device. When a request cannot be processed due to formatting errors or the requested data is not available, the IIN is always returned with the appropriate bits set.

| Bit | Indication | Description | Supported |
|---|---|---|---|
| Octet 1 | | | |

| Bit | Indication | Description | Supported |
|---|---|---|---|
| 0 | All stations message received | Set when a request is received with the destination address of the all stations address (6553510). It is cleared after the next response (even if a response to a global request is required).<br>This IIN is used to let the master station know that a "broadcast" message was received by the relay. | Yes |
| 1 | Class 1 data available | Set when data that has been configured as Class 1 data is ready to be sent to the master.<br>The master station should request this class data from the relay when this bit is set in a response. | Yes |
| 2 | Class 2 data available | Set when data that has been configured as Class 2 data is ready to be sent to the master.<br>The master station should request this class data from the relay when this bit is set in a response. | Yes |
| 3 | Class 3 data available | Set when data that has been configured as Class 3 data is ready to be sent to the master.<br>The master station should request this class data from the relay when this bit is set in a response. | Yes |
| 4 | Time-synchronisation required | The relay requires time synchronization from the master station (using the Time and Date object).<br>This IIN is cleared once the time has been synchronised. It can also be cleared by explicitly writing a 0 into this bit of the Internal Indication object. | Yes |
| 5 | Local | Set when some or all of the relays digital output points (Object 10/12) are in the Local state. That is, the relays control outputs are NOT accessible through the DNP protocol.<br>This IIN is clear when the relay is in the Remote state. That is, the relays control outputs are fully accessible through the DNP protocol. | No |
| 6 | Device in trouble | Set when an abnormal condition exists in the relay. This IIN is only used when the state cannot be described by a combination of one or more of the other IIN bits. | No |
| 7 | Device restart | Set when the device software application restarts. This IIN is cleared when the master station explicitly writes a 0 into this bit of the Internal Indications object. | Yes |
| **Octet 2** | | | |
| 0 | Function code not implemented | The received function code is not implemented within the relay. | Yes |
| 1 | Requested object(s) unknown | The relay does not have the specified objects or there are no objects assigned to the requested class.<br>This IIN should be used for debugging purposes and usually indicates a mismatch in device profiles or configuration problems. | Yes |
| 2 | Out of range | Parameters in the qualifier, range or data fields are not valid or out of range. This is a 'catch-all' for application request formatting errors. It should only be used for debugging purposes. This IIN usually indicates configuration problems. | Yes |
| 3 | Buffer overflow | Event buffer(s), or other application buffers, have overflowed. The master station should attempt to recover as much data as possible and indicate to the user that there may be lost data. The appropriate error recovery procedures should be initiated by the user. | Yes |
| 4 | Already executing | The received request was understood but the requested operation is already executing. | |
| 5 | Bad configuration | Set to indicate that the current configuration in the relay is corrupt. The master station may download another configuration to the relay. | Yes |
| 6 | Reserved | Always returned as zero. | |

| Bit | Indication | Description | Supported |
|---|---|---|---|
| 7 | Reserved | Always returned as zero. | |

#### 22.13.3.8.4 DNP3 RESPONSE STATUS CODES

When the device processes Control Relay Output Block (Object 12) requests, it returns a set of status codes; one for each point contained within the original request. The complete list of codes appears in the following table:

| Code Number | Identifier Name | Description |
|---|---|---|
| 0 | Success | The received request has been accepted, initiated, or queued. |
| 1 | Timeout | The request has not been accepted because the 'operate' message was received after the arm timer (Select Before Operate) timed out.<br>The arm timer was started when the select operation for the same point was received. |
| 2 | No select | The request has not been accepted because no previous matching 'select' request exists. (An 'operate' message was sent to activate an output that was not previously armed with a matching 'select' message). |
| 3 | Format error | The request has not been accepted because there were formatting errors in the control request ('select', 'operate', or 'direct operate'). |
| 4 | Not supported | The request has not been accepted because a control operation is not supported for this point. |
| 5 | Already active | The request has not been accepted because the control queue is full or the point is already active. |
| 6 | Hardware error | The request has not been accepted because of control hardware problems. |
| 7 | Local | The request has not been accepted because local access is in progress. |
| 8 | Too many operations | The request has not been accepted because too many operations have been requested. |
| 9 | Not authorized | The request has not been accepted because of insufficient authorisation. |
| 127 | Undefined | The request not been accepted because of some other undefined reason. |

*Note:*
*Code numbers 10 through to 126 are reserved for future use.*

### 22.13.3.9 DNP3 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 protocol***). This is a non-settable cell, which shows the chosen communication protocol – in this case `DNP3.0`.

```
COMMUNICATIONS
RP1 Protocol
DNP3.0
```

4. Move down to the next cell (***RP1 Address***). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the Relay Address. It is important that no two IEDs have the same address.

```
COMMUNICATIONS
RP1 Address
1
```

5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps and 38400 bps. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
9600 bits/s
```

6. Move down to the next cell (***RP1 Parity***). This cell controls the parity format used in the data frames. The parity can be set to be one of *None*, *Odd* or *Even*. Make sure that the parity format selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Parity
None
```

7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

```
COMMUNICATIONS
RP1 PhysicalLink
Copper
```

8. Move down to the next cell (***RP1 Time Sync***). This cell affects the time synchronisation request from the master by the IED. It can be set to *enabled* or *disabled*. If enabled it allows the DNP3.0 master to synchronise the time on the IED.

```
COMMUNICATIONS
RP1 Time Sync
Enabled
```

#### 22.13.3.9.1 DNP3 CONFIGURATOR

A PC support package for DNP3.0 is available as part of the supplied settings application software (MiCOM S1 Agile) to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new DNP3.0 configuration takes effect after the download is complete. To restore the default configuration at any time, from the *CONFIGURATION* column, select the ***Restore Defaults*** cell then select *All Settings*.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

If the device supports DNP Over Ethernet, the configuration related settings are done in the folder **DNP Over Ethernet**.

## 22.13.4 IEC 61850

This section describes how the IEC 61850 standard is applied to GE Vernova products. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 61850 standard.

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security that is so essential in substations today.

There are two editions of most parts of the IEC 61850 standard; edition 1 and edition 2. The edition which this product supports depends on the Software Version.

Software Version 70 onwards provides an IEC 61850 Edition 2 compatible implementation.

From Software Version 90 onwards, it supports edition 2.

An additional section detailing the enhancements in edition 2 models is documented later in this chapter, if applicable.

### 22.13.4.1 BENEFITS OF IEC 61850

The standard provides:

- Standardised models for IEDs and other equipment within the substation
- Standardised communication services (the methods used to access and exchange data)
- Standardised formats for configuration files
- Peer-to-peer communication

The standard adheres to the requirements laid out by the ISO OSI model and therefore provides complete vendor interoperability and flexibility on the transmission types and protocols used. This includes mapping of data onto Ethernet, which is becoming more and more widely used in substations, in favour of RS485. Using Ethernet in the substation offers many advantages, most significantly including:

- Ethernet allows high-speed data rates (currently 100 Mbps, rather than tens of kbps or less used by most serial protocols)
- Ethernet provides the possibility to have multiple clients
- Ethernet is an open standard in every-day use
- There is a wide range of Ethernet-compatible products that may be used to supplement the LAN installation (hubs, bridges, switches)

### 22.13.4.2 IEC 61850 INTEROPERABILITY

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs, which allows interoperability between products from multiple vendors.

An IEC 61850-compliant device may be interoperable, but this does not mean it is interchangeable. You cannot simply replace a product from one vendor with that of another without reconfiguration. However, the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able to integrate a new device very quickly without having to map all of the new data. IEC 61850 brings improved substation communications and interoperability to the end user, at a lower cost.

### 22.13.4.3 THE IEC 61850 DATA MODEL

The data model of any IEC 61850 IED can be viewed as a hierarchy of information, whose nomenclature and categorization is defined and standardized in the IEC 61850 specification.

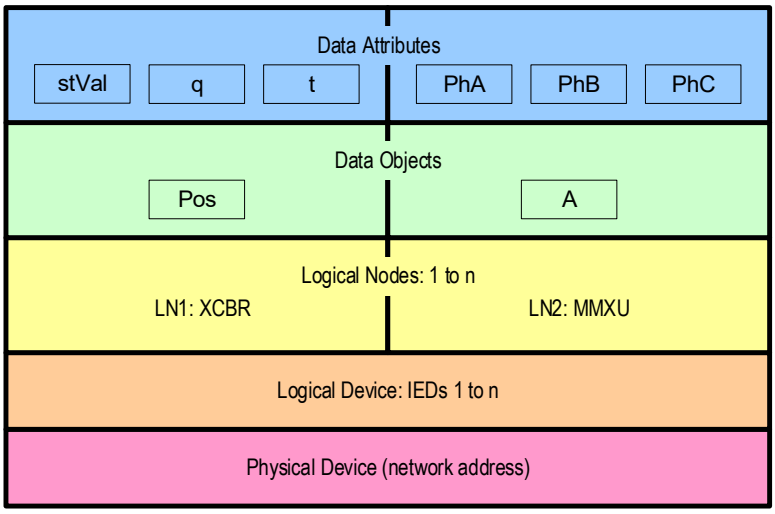


**Figure 282: Data model layers in IEC 61850**

The levels of this hierarchy can be described as follows:

### Data Frame format

| Layer | Description |
|---|---|
| Physical Device | Identifies the actual IED within a system. Typically the device's name or IP address can be used (for example Feeder_1 or 10.0.0.2. |
| Logical Device | Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM IEDs, 5 Logical Devices exist: Control, Measurements, Protection, Records, System. |
| Wrapper/Logical Node Instance | Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number.<br>For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2). |
| Data Object | This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR. |
| Data Attribute | This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR. |

## 22.13.4.4 IEC 61850 IN MICOM IEDS

IEC 61850 is implemented by use of a separate Ethernet card. This Ethernet card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection functions.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a bay computer (MiCOM C264)
- An HMI
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge of the IED

The IEC 61850 compatible interface standard provides capability for the following:

- Read access to measurements
- Refresh of all measurements at a standard rate.

- Generation of non-buffered and buffered reports on change of status or measurement
- SNTP time synchronization over an Ethernet link. (This is used to synchronize the IED's internal real time clock.
- GOOSE peer-to-peer communication
- Disturbance record extraction by IEC 61850 MMS file transfer. The record is extracted as an ASCII format COMTRADE file
- Controls (Direct and Select Before Operate)

*Note:*
*Setting changes are not supported in the current IEC 61850 implementation. Currently these setting changes are carried out using the settings application software.*

### 22.13.4.5 IEC 61850 DATA MODEL IMPLEMENTATION

The data model naming adopted in the IEDs has been standardised for consistency. Therefore the Logical Nodes are allocated to one of the five Logical Devices, as appropriate.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available as a separate document.

### 22.13.4.6 IEC 61850 COMMUNICATION SERVICES IMPLEMENTATION

The IEC 61850 communication services which are implemented in the IEDs are described in the Protocol Implementation Conformance Statement (PICS) document, which is available as a separate document.

### 22.13.4.7 IEC 61850 PEER-TO-PEER (GOOSE) COMMUNICATIONS

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) enables faster communication between IEDs offering the possibility for a fast and reliable system-wide distribution of input and output data values. The GOOSE model uses multicast services to deliver event information. Multicast messaging means that messages are sent to selected devices on the network. The receiving devices can specifically accept frames from certain devices and discard frames from the other devices. It is also known as a publisher-subscriber system. When a device detects a change in one of its monitored status points it publishes a new message. Any device that is interested in the information subscribes to the data it contains.

### 22.13.4.8 GOOSE MESSAGE VALIDATION

Whenever a new GOOSE message is received its validity is checked before the dataset is decoded and used to update the Programmable Scheme Logic. As part of the validation process a check is made for state and sequence number anomalies. If an anomaly is detected, the 'out-of-order' GOOSE message is discarded. When a message is discarded the last valid message remains active until a new valid GOOSE message is received or its validity period (TAL) expires.

Out-of-order GOOSE message indicators and reporting are provided to the subscriber via the IEC61850 LGOS logical node.

### 22.13.4.9 MAPPING GOOSE MESSAGES TO VIRTUAL INPUTS

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

An IED can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

#### 22.13.4.9.1 IEC 61850 GOOSE CONFIGURATION

All GOOSE configuration is performed using the IEC 61850 Configurator tool available in the MiCOM S1 Agile software application.

All GOOSE publishing configuration can be found under the **GOOSE Publishing** tab in the configuration editor window. All GOOSE subscription configuration parameters are under the **External Binding** tab in the configuration editor window.

Settings to enable GOOSE signalling and to apply Test Mode are available using the HMI.

### 22.13.4.10 ETHERNET FUNCTIONALITY

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost, and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association, and terminate any which are no longer active.

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

### 22.13.4.11 IEC 61850 CONFIGURATION

You cannot configure the device for IEC 61850 edition 1 using the HMI panel on the product. For this you must use the IEC 61850 Configurator, which is part of the settings application software. If the device is compatible with edition 2, however, you can configure it with the HMI. To configure IEC61850 edition 2 using the HMI, you must first enable the IP From HMI setting, after which you can set the media (copper or fibre), IP address, subnet mask and gateway address.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IED's system configuration capabilities are determined from an IED Capability Description file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and test (using simulation tools), a substation's entire protection scheme before the products are installed into the substation.

To help with this process, the settings application software provides an IEC 61850 Configurator tool, which allows the pre-configured IEC 61850 configuration file to be imported and transferred to the IED. As well as this, you can manually create configuration files for all products, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

*Note:*
*Some configuration data is available in the IEC61850 CONFIG. column, allowing read-only access to basic configuration data.*

#### 22.13.4.11. IEC 61850 CONFIGURATION BANKS 1

There are two configuration banks:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the IED is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration.

Following an upgrade, the IEC 61850 Configurator tool can be used to transmit a command, which authorises activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the *IEC61850 CONFIG.* column of the HMI.

The SCL Name and Revision attributes of both configuration banks are available in the *IEC61850 CONFIG.* column of the HMI.

#### 22.13.4.11. IEC 61850 NETWORK CONNECTIVITY 2

Configuration of the IP parameters and SNTP (Simple Network Time Protocol) time synchronisation parameters is performed by the IEC 61850 Configurator tool. If these parameters are not available using an SCL (Substation Configuration Language) file, they must be configured manually.

Every IP address on the Local Area Network must be unique. Duplicate IP addresses result in conflict and must be avoided. Most IEDs check for a conflict on every IP configuration change and at power up and they raise an alarm if an IP conflict is detected.

The IED can be configured to accept data from other networks using the ***Gateway*** setting. If multiple networks are used, the IP addresses must be unique across networks.

### 22.13.4.12 SELECTION OF THE IEC 61850 EDITION

From Software Version 90 onwards, it is possible to select between edition 1 and edition 2. Edition 1 and edition 2 implementations have different IEC 61850 data models and different ICD files. Only one can be active at any time in the product, so the selection is a decision related to system engineering.

Selection of edition 1 or edition 2 is done based on the configuration file (MCL) that is sent to the product and activated.

To configure the product for edition 1, start with the edition 1 ICD file. This can be done in one of two ways:

1. Using the system engineering process of an IEC 61850 system. In this case, import either the edition 1 ICD file (for example “P545____91A_ED1.ICD”) or the edition 2 ICD file (for example “P545____91A_ED2.ICD”), as applicable, into the System Configuration Tool. Perform the system configuration, then export the configured file (.SCD or CID). Import this configured file into MiCOM S1 Agile’s IEC 61850 Configurator.
2. Using the IED Configurator tool to manually configure the product. Launch the IED Configurator tool. Select **File**, **New** and then check only the **Edition 1** or **Edition 2** box, as applicable, and then proceed to select the product model and software version. Configure the parameters manually and save the MCL file.

In either case, the edition 1 or edition 2 configuration is activated in the product by sending the configuration file to the product from the IED Configurator and switching it to the Active Bank, after which the Ethernet application will restart with the new configuration.

### 22.13.4.13 IEC 61850 EDITION 2

Many parts of the IEC 61850 standard have now been released as the second edition. This offers some significant enhancements including:

- Improved interoperability
- Many new logical nodes
- Better defined testing; it is now possible to perform off-line testing and simulation of functions

Edition 2 implementation requires use of version 3.8 of the IEC 61850 configurator, which is installed with version 2.0.1 of MiCOM S1 Agile.

### 22.13.4.13. BACKWARD COMPATIBILITY 1

#### IEC61850 System - Backward compatibility

An Edition 1 IED can operate with an Edition 2 IEC 61850 system, provided that the Edition 1 IEDs do not subscribe to GOOSE messages with data objects or data attributes which are only available in Edition 2.

The following figure explains this concept:

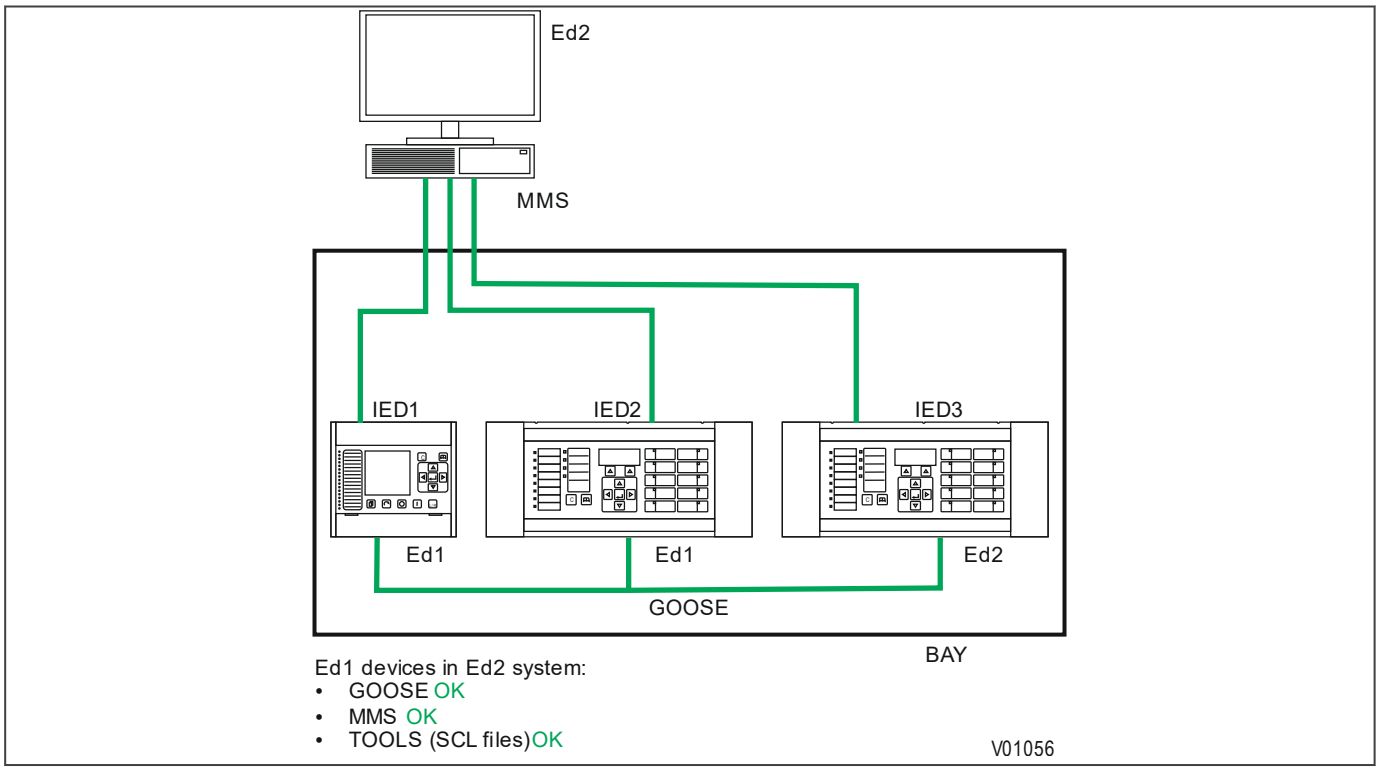


**Figure 283: Edition 2 system - backward compatibility**

An Edition 2 IED cannot normally operate within an Edition 1 IEC 61850 system. An Edition 2 IED can work for GOOSE messaging in a mixed system, providing the client is compatible with Edition 2.

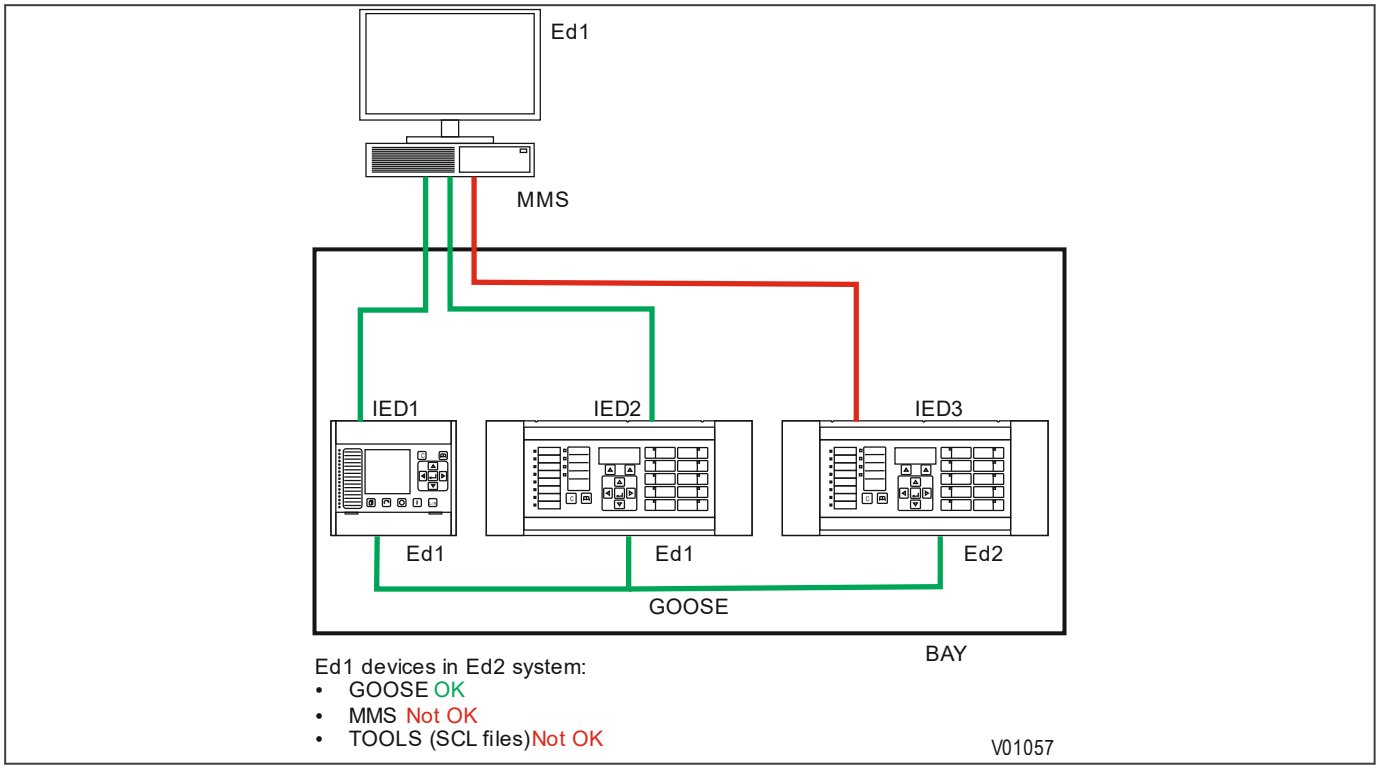


**Figure 284: Edition 1 system - forward compatibility issues**

### 22.13.4.13. EDITION-2 COMMON DATA CLASSES 2

The following common data classes (CDCs) are new to Edition 2 and therefore should not be used in GOOSE control blocks in mixed Edition 1 and Edition 2 systems

- Histogram (HST)
- Visible string status (VSS)
- Object reference setting (ORG)
- Controllable enumerated status (ENC)
- Controllable analogue process value (APC)
- Binary controlled analogue process value (BAC)
- Enumerated status setting (ENG)
- Time setting group (TSG)
- Currency setting group (CUG)
- Visible string setting (VSG)
- Curve shape setting (CSG)

Of these, only ENS and ENC types are available from a MiCOM P40 IED when publishing GOOSE messages, so Data Objects using these Common Data Classes should not be published in mixed Edition 1 and Edition 2 systems.

For compatibility between Edition 1 and Edition 2 IEDs, SCL files using SCL schema version 2.1 must be used. For a purely Edition 2 system, use the schema version 3.1.

### 22.13.4.13. STANDBY PROTECTION REDUNDANCY 3

With digital substation architectures, measurements can be shared freely on the process bus across the substation and between different devices without any additional wiring. This is because there are no longer any electrical connections to instruments transformers that restrict the location of IEDs.

The new IEC 61850 Edition 2 test modes enable the introduction of standby protection IEDs at any location within the substation, which has access to both station and process buses. In the case of failure, these devices can temporarily replace the protection functions inside other IEDs.

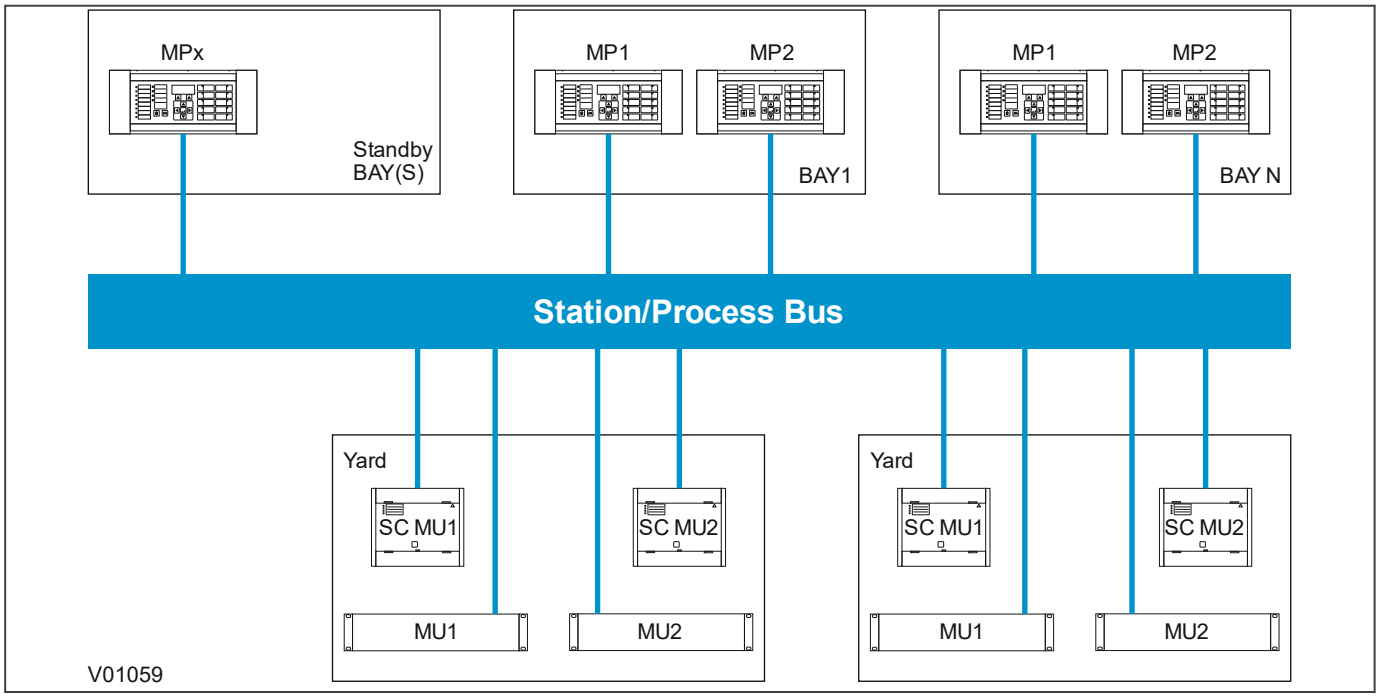


**Figure 285: Example of Standby IED**

See the example below. If a failure occurs in the Bay 1 protection IED (MP2), we could disable this device and activate a standby protection IED to replace its functionality.

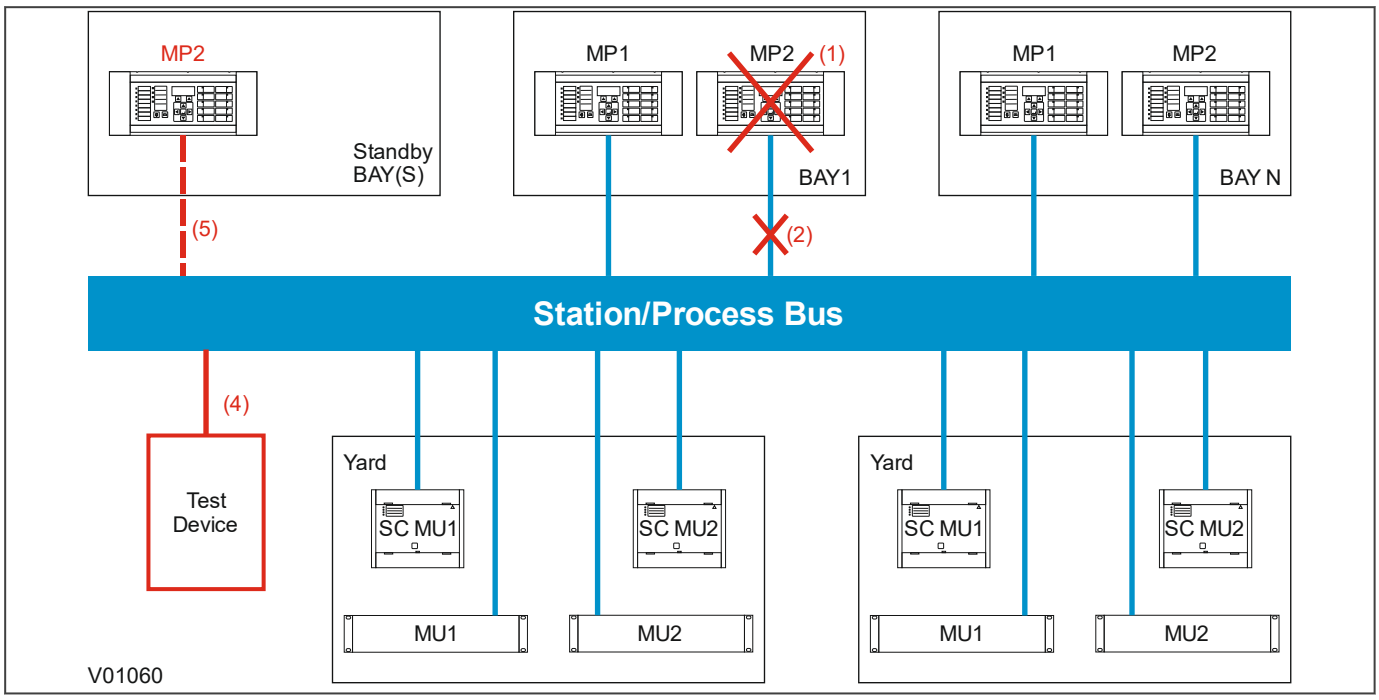


**Figure 286: Standby IED Activation Process**

The following sequence would occur under this scenario:

1. During the installation phase, a spare standby IED is installed in the substation. This can remain inactive, until it is needed to replace functions in one of several bays. The device is connected to the process bus, but does not have any subscriptions enabled.
2. If a failure occurs (in this example, bay 1), first isolate the faulty device by disabling its process bus and station bus interfaces. You do this by turning off the attached network interfaces.
3. Retrieve the configuration that the faulty device normally uses, and load this into the standby redundant IED.
4. Place the IED into the "Test Blocked" mode, as defined in IEC 61850-7-4 Edition Two. This allows test signals to be injected into the network, which will check that the configuration is correct. GOOSE signals issued by the device will be flagged as "test" so that subscribing switchgear controllers know not to trip during this testing. In this way the protection can be tested all the way up to the switchgear control merging units without having to operate primary circuit breakers, or by carrying out any secondary injection.
5. Take the standby IED out of "Test-Blocked" mode and activate it so that it now replaces the protection functions that were disabled from the initial device failure.

The standby IED reduces downtime in the case of device failure, as protection functions can be restored quickly before the faulted device is replaced.

## 22.14 READ ONLY MODE

With IEC 61850 and Ethernet/Internet communication capabilities, security has become an important issue. For this reason, all relevant GE Vernova IEDs have been adapted to comply with the latest cyber-security standards.

In addition to this, a facility is provided which allows you to enable or disable the communication interfaces. This feature is available for products using Courier, IEC 60870-5-103, or IEC 61850.

### 22.14.1 IEC 60870-5-103 PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with IEC 60870-5-103, the following commands are blocked at the interface:

- Write parameters (=change setting) (private ASDUs)
- General Commands (ASDU20), namely:
  - INF16 auto-recloser on/off
  - INF19 LED reset
  - Private INFs (for example: CB open/close, Control Inputs)

The following commands are still allowed:

- Poll Class 1 (Read spontaneous events)
- Poll Class 2 (Read measurands)
- GI sequence (ASDU7 'Start GI', Poll Class 1)
- Transmission of Disturbance Records sequence (ASDU24, ASDU25, Poll Class 1)
- Time Synchronisation (ASDU6)
- General Commands (ASDU20), namely:
  - INF23 activate characteristic 1
  - INF24 activate characteristic 2
  - INF25 activate characteristic 3
  - INF26 activate characteristic 4

*Note:*
*For IEC 60870-5-103, Read Only Mode function is different from the existing Command block feature.*

### 22.14.2 COURIER PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with Courier, the following commands are blocked at the interface:

- Write settings
- All controls, including:
  - Reset Indication (Trip LED)
  - Operate Control Inputs
  - CB operations
  - Auto-reclose operations
  - Reset demands
  - Clear event/fault/maintenance/disturbance records
  - Test LEDs & contacts

The following commands are still allowed:

- Read settings, statuses, measurands
- Read records (event, fault, disturbance)
- Time Synchronisation
- Change active setting group

### 22.14.3 IEC 61850 PROTOCOL BLOCKING

If Read-Only Mode is enabled for the Ethernet interfacing with IEC 61850, the following commands are blocked at the interface:

- All controls, including:
  - Enable/disable protection
  - Operate Control Inputs
  - CB operations (Close/Trip, Lock)
  - Reset LEDs

The following commands are still allowed:

- Read statuses, measurands
- Generate reports
- Extract disturbance records
- Time synchronisation
- Change active setting group

### 22.14.4 READ-ONLY SETTINGS

The following settings are available for enabling or disabling Read Only Mode.

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

### 22.14.5 READ-ONLY DDB SIGNALS

The remote read only mode is also available in the PSL using three dedicated DDB signals:

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

Using the PSL, these signals can be activated by opto-inputs, Control Inputs and function keys if required.

## 22.15 TIME SYNCHRONISATION

In modern protection schemes it is necessary to synchronise the IED's real time clock so that events from different devices can be time stamped and placed in chronological order. This is achieved in various ways depending on the chosen options and communication protocols.

- Using the IRIG-B input (if fitted)
- Using the SNTP time protocol (for Ethernet IEC 61850 versions)
- Using IEEE 1588 Precision Time Protocol (PTP)
- By using the time synchronisation functionality inherent in the data protocols

The time synchronisation sources can be configured in a priority order using the Primary Source and Secondary Source cells in the DATE AND TIME column. If the Primary source becomes unavailable, the Secondary source will be used, if available.

### 22.15.1 IRIG-B

IRIG stands for Inter Range Instrumentation Group, which is a standards body responsible for standardising different time code formats. There are several different formats starting with IRIG-A, followed by IRIG-B and so on. The letter after the "IRIG" specifies the resolution of the time signal in pulses per second (PPS). IRIG-B, the one which we use has a resolution of 100 PPS. IRIG-B is used when accurate time-stamping is required.

The following diagram shows a typical GPS time-synchronised substation application. The satellite RF signal is picked up by a satellite dish and passed on to receiver. The receiver receives the signal and converts it into time signal suitable for the substation network. IEDs in the substation use this signal to govern their internal clocks and event recorders.

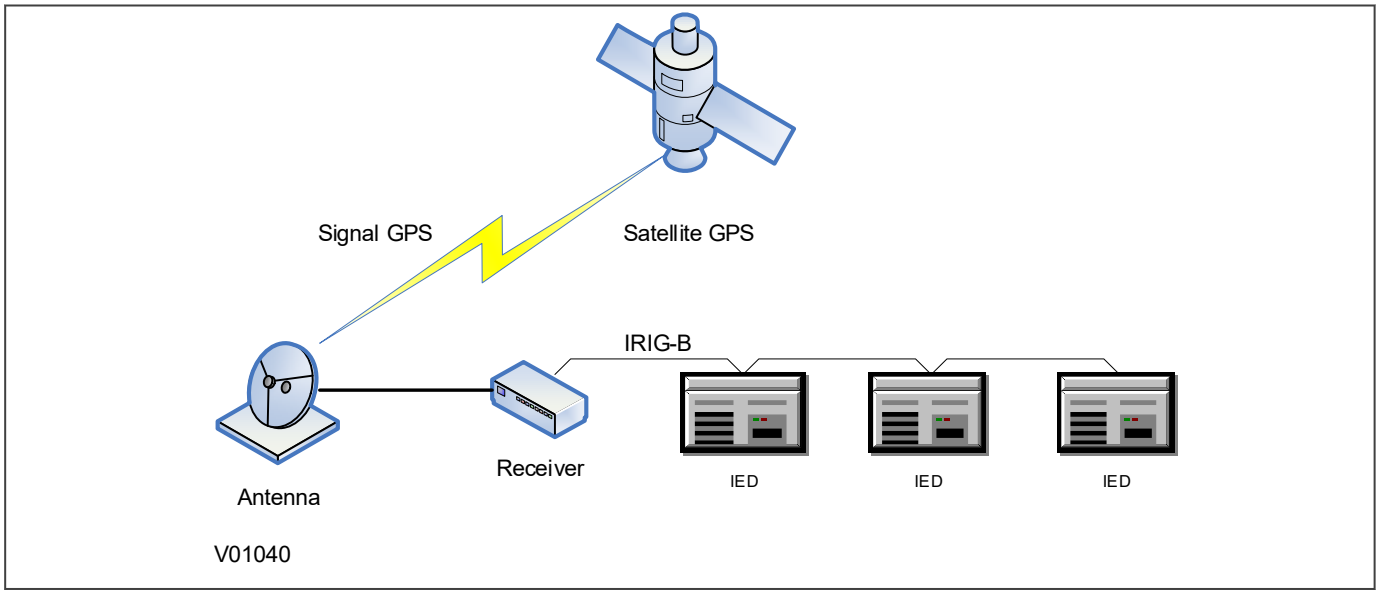


**Figure 287: GPS satellite timing signal**

The IRIG-B time code signal is a sequence of one second time frames. Each frame is split up into ten 100 mS slots as follows:

- Time-slot 1: Seconds
- Time-slot 2: Minutes

- Time-slot 3: Hours
- Time-slot 4: Days
- Time-slot 5 and 6: Control functions
- Time-slots 7 to 10: Straight binary time of day

The first four time-slots define the time in BCD (Binary Coded Decimal). Time-slots 5 and 6 are used for control functions, which control deletion commands and allow different data groupings within the synchronisation strings. Time-slots 7-10 define the time in SBS (Straight Binary Second of day).

#### 22.15.1.1 IRIG-B IMPLEMENTATION

Depending on the chosen hardware options, the product can be equipped with an IRIG-B input for time synchronisation purposes. The IRIG-B interface is implemented either on a dedicated board, or together with other communication functionality such as Ethernet. The IRIG-B connection is presented by a connector is a BNC connector. IRIG-B signals are usually presented as an RF-modulated signal. The boards support universal IRIG-B, which means they accept demodulated or modulated IRIG-B.

To set the device to use IRIG-B, use the setting ***IRIG-B Sync*** cell in the *DATE AND TIME* column.

The IRIG-B status can be viewed in the ***IRIG-B Status*** cell in the *DATE AND TIME* column.

### 22.15.2 SNTP

SNTP is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. SNTP can be used as the time synchronisation method for models using IEC 61850 over Ethernet.

The device is synchronised by the main SNTP server. This is achieved by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software described in the settings application software manual. A second server is also configured with a different IP address for backup purposes.

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. This could be because there is no response or no valid clock signal.

The HMI menu does not contain any configurable settings relating to SNTP, as the only way to configure it is using the IEC 61850 Configurator. However it is possible to view some parameters in the *COMMUNICATIONS* column under the sub-heading SNTP parameters. Here you can view the SNTP server addresses and the SNTP poll rate in the cells ***SNTP Server 1***, ***SNTP Server 2*** and ***SNTP Poll rate*** respectively.

The SNTP time synchronisation status is displayed in the ***SNTP Status*** cell in the *DATE AND TIME* column.

#### 22.15.2.1 LOSS OF SNTP SERVER SIGNAL ALARM

This function issues an alarm when there is a loss of time synchronization on the SNTP server. It is issued when the SNTP sever has not detected a valid time synchronisation response within its 5 second window. This is because there is no response or no valid clock. The alarm is mapped to IEC 61850.

### 22.15.3 IEEE 1588 PRECISION TIME PROTOCOL

The MiCOM P40 modular products support IEEE 1588 Precision Time Protocol (PTP) as a slave-only clock. MiCOM relays are profile unaware, which means that they will accept synchronization from any PTP profile. Power Utility Profile (IEC 61850-9-3) is specifically designed to perform well for substation related applications, with PMU applications needing the most stringent requirements.

#### 22.15.3.1 ACCURACY AND DELAY CALCULATION

A time synchronisation accuracy of within 5 ms is possible. Both peer-to-peer or end-to-end mode delay measurement can be used.

In peer-to-peer mode, delays are measured between each link in the network and are compensated for. This provides greater accuracy, but requires that every device between the Grand Master and Slaves supports the peer-to-peer delay measurement.

In end-to-end mode, delays are only measured between each Grand Master and Slave. The advantage of this mode is that the requirements for the switches on the network are lower; they do not need to independently calculate delays. The main disadvantage is that more inaccuracy is introduced, because the method assumes that forward and reverse delays are always the same, which may not always be correct.

When using end-to-end mode, the IED can be connected in a ring or line topology using RSTP or Self Healing Protocol without any additional Transparent Clocks. But because the IED is a slave-only device, additional inaccuracy is introduced. The additional error will be less than 1ms for a network of eight devices.

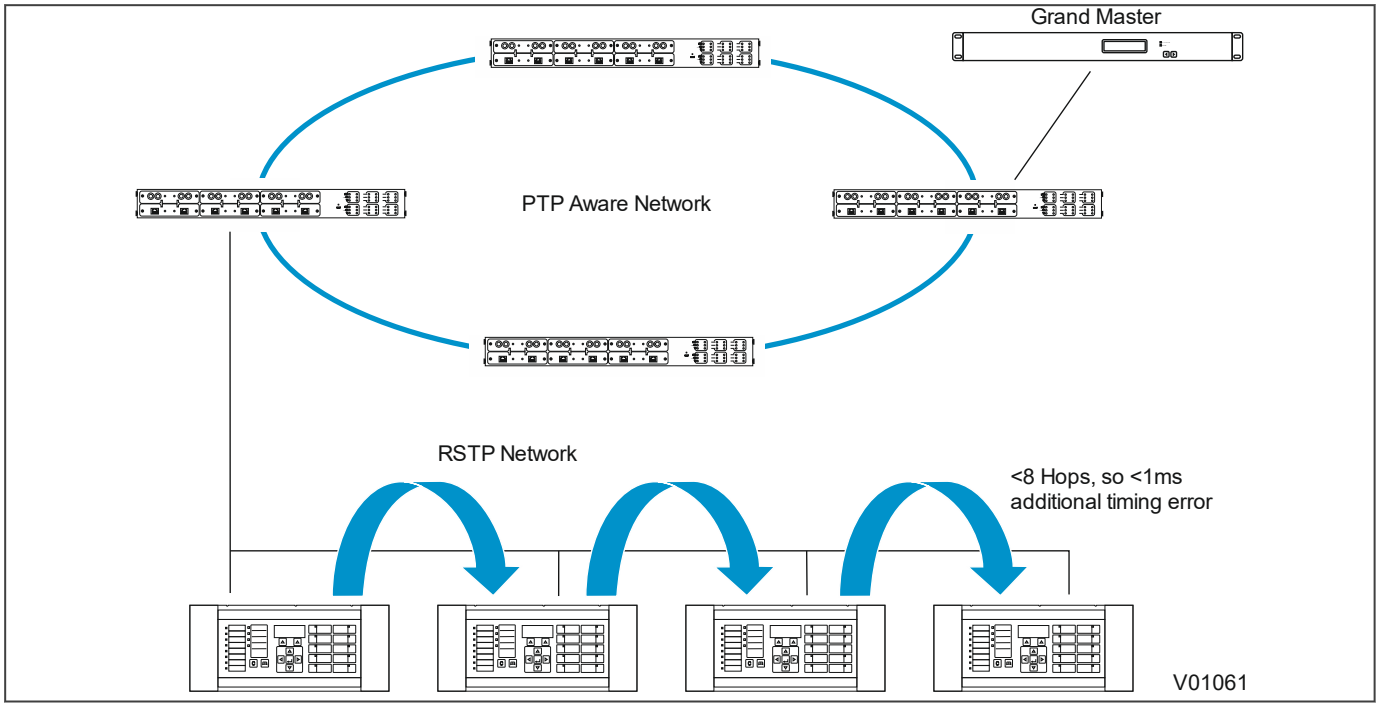


**Figure 288: Timing error using ring or line topology**

### 22.15.3.2 PTP DOMAINS

PTP traffic can be segregated into different domains using Boundary Clocks. These allow different PTP clocks to share the same network while maintaining independent synchronisation within each grouped set.

## 22.15.4 TIME SYNCHRONISATION USING THE COMMUNICATION PROTOCOLS

All communication protocols have in-built time synchronisation mechanisms. If an external time synchronisation mechanism such as IRIG-B, SNTP, or IEEE 1588 PTP is not used to synchronise the devices, the time synchronisation mechanism within the relevant serial protocol is used. The real time is usually defined in the master station and communicated to the relevant IEDs via one of the rear serial ports using the chosen protocol. It is also possible to define the time locally using settings in the *DATE AND TIME* column.

The time synchronisation for each protocol is described in the relevant protocol description section.

# CHAPTER 23

# CYBERSECURITY

## 23.1 DISCLAIMER

GE Vernova Grid Automation products are digital devices designed to be installed and operated in utility substations & industrial plant environments and connected to secure private networks. GE Vernova IEDs should not be connected to the public internet.

GE Vernova strongly recommends that users protect their digital devices using a defense-in-depth strategy which will protect their products, their network, their systems and interfaces against cyber security threats. This includes, but is not limited to, placing digital devices inside the control system network security perimeter, deploying and maintaining access controls, monitoring and intrusion detection, security awareness training, security policies, network segmentation and firewalls installation, strong and active password management, data encryption, antivirus and other mitigating applicable technologies.

GE Vernova IEDs are available with standard features, and in some products additional optional software options, which provide cyber security mechanisms to help users protect against cyber security intrusion. GE Vernova strongly recommends using all available cyber security options.

For additional details and recommendations on how to protect the GE Vernova IEDs, please see Cyber Security sections of the manuals. GE Vernova Grid Automation may also provide additional instructions and recommendations to users from time to time relating to IED and cyber security threats or vulnerabilities.

It is the users' sole responsibility to make sure that all GE Vernova Grid Automation IEDs are installed and operated considering its cyber security capabilities, security context, and the instructions and recommendations provided to the user relating to GE Vernova. Users assume all risks and liability associated with damages or losses incurred in connection with any and all cyber security incidences.

**IT IS THE SOLE RESPONSIBILITY OF THE USER TO SECURE THEIR NETWORK AND ASSOCIATED DEVICES AGAINST CYBER SECURITY INTRUSIONS OR ATTACKS. GE VERNOVA GRID AUTOMATION AND ITS AFFILIATES ARE NOT LIABLE FOR ANY DAMAGES AND/OR LOSSES ARISING FROM OR RELATED TO SUCH SECURITY INTRUSION OR ATTACKS.**

## 23.2 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were often proprietary.

For these reasons, the substation environment was very secure against cyber-attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it cannot be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them).

However, note that these are not recognised defences against attackers.

The increasing sophistication of protection schemes, coupled with the advancement of technology and the desire for vendor interoperability, has resulted in standardisation of networks and data interchange within substations. Today, devices within substations use standardised protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardised protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for our range of Intelligent Electronic Devices (IEDs).

*Note:*
*Cyber-security compatible devices do not enforce NERC compliance, they merely facilitate it. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary.*

This chapter contains the following sections:

Disclaimer 530
Overview 531
The Need for Cybersecurity 532
Standards 533
Cyber-Security Implementation 537
Roles and Permissions 538
Authentication 541
Security Event Management 553

## 23.3 THE NEED FOR CYBERSECURITY

Cybersecurity provides protection against unauthorised disclosure, transfer, modification, or destruction of information or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorised access to information)
- Integrity (preventing unauthorised modification)
- Availability/Authentication (preventing the denial of service and assuring authorised access to information)
- Non-repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyse incidents)

The threats to Cybersecurity may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber-attacks by hackers).

Good Cybersecurity can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (users keep passwords on their computer)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Bypassing of controls (users turn off security measures)
- Inadequate technology (substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate preventing access to equipment

To help tackle these issues, standards organisations have produced various standards. Compliance with these standards significantly reduces the threats associated with lack of Cybersecurity.

## 23.4 STANDARDS

There are several standards, which apply to substation Cybersecurity. The standards currently applicable to GE Vernova's IEDs are NERC and IEEE1686.

| Standard | Country | Description |
|---|---|---|
| NERC CIP (North American Electric Reliability Corporation) | USA | Framework for the protection of the grid critical Cyber Assets |
| BDEW (German Association of Energy and Water Industries) | Germany | Requirements for Secure Control and Telecommunication Systems |
| ANSI ISA 99 | USA | ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management |
| IEEE 1686 | International | International Standard for substation IED Cybersecurity capabilities |
| IEC 62351 | International | Power system data and Comm. protocol |
| ISO/IEC 27002 | International | Framework for the protection of the grid critical Cyber Assets |
| NIST SP800-53 (National Institute of Standards and Technology) | USA | Complete framework for SCADA SP800-82and ICS Cybersecurity |
| CPNI Guidelines (Centre for the Protection of National Infrastructure) | UK | Clear and valuable good practices for Process Control and SCADA security |

### 23.4.1 NERC COMPLIANCE

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of 'Critical Cyber Assets', which control or have an influence on the reliability of North America's electricity generation and distribution systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

#### NERC CIP standards

| CIP Standard | Description |
|---|---|
| CIP-002-1 Critical Cyber Assets | Define and document the Critical Assets and the Critical Cyber Assets |
| CIP-003-1 Security Management Controls | Define and document the Security Management Controls required to protect the Critical Cyber Assets |
| CIP-004-1 Personnel and Training | Define and Document Personnel handling and training required protecting Critical Cyber Assets |
| CIP-005-1 Electronic Security | Define and document logical security perimeters where Critical Cyber Assets reside. Define and document measures to control access points and monitor electronic access |
| CIP-006-1 Physical Security | Define and document Physical Security Perimeters within which Critical Cyber Assets reside |
| CIP-007-1 Systems Security Management | Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets |
| CIP-008-1 Incident Reporting and Response Planning | Define and document procedures necessary when Cybersecurity Incidents relating to Critical Cyber Assets are identified |

| CIP Standard | Description |
|---|---|
| CIP-009-1 Recovery Plans | Define and document Recovery plans for Critical Cyber Assets |

#### 23.4.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| Create the list of the assets | We can help the power utilities to create this asset register automatically.<br>We can provide audits to list the Cyber assets |

#### 23.4.1.2 CIP 003

CIP 003 requires the implementation of a Cybersecurity policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| To create a Cybersecurity policy | We can help the power utilities to have access control to its critical assets by providing centralized Access control.<br>We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software. |

#### 23.4.1.3 CIP 004

CIP 004 requires that personnel with authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| To provide appropriate training of its personnel | We can provide Cybersecurity training |

#### 23.4.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| To monitor access to the ESP<br>To perform the vulnerability assessments<br>To document network changes | To disable all ports not used in the IED<br>To monitor and record all access to the IED |

#### 23.4.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| Provide physical security controls and perimeter monitoring<br>Ensure that people who have access to critical cyber assets don't have criminal records | GE Vernova cannot provide additional help with this aspect |

#### 23.4.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring
- An annual vulnerability assessment should be performed

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| To provide an incident response team and have appropriate processes in place | Test procedures, we can provide advice and help on testing<br>Ports and services, our devices can disable unused ports and services<br>Security patch management, we can provide assistance<br>Antivirus, we can provide advise and assistance<br>Account management, we can provide advice and assistance<br>Monitoring, our equipment monitors and logs access |

#### 23.4.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| To provide an incident response team and have appropriate processes in place. | GE Vernova Vernova cannot provide additional help with this aspect. |

#### 23.4.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

| Power Utility Responsibilities | GE Vernova's Contribution |
|---|---|
| To implement a recovery plan | To provide guidelines on recovery plans and backup/restore documentation |

### 23.4.2 IEEE 1686-2013

IEEE 1686-2013 is an IEEE Standard for substation IEDs' Cybersecurity capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.
- The audit trail is recorded, listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

## 23.5 CYBER-SECURITY IMPLEMENTATION

GE Vernova IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

From Software Version 90 onwards, the MiCOM P40 Agile products provide enhanced security through the following features:

- An Authentication, Authorization, Accounting (AAA) Remote Authentication Dial-In User Service (RADIUS) client that is managed centrally, enables user attribution, provides accounting of all user activities, and uses secure standards based on strong cryptography for authentication and credential protection. In other words, this option uses a RADIUS.
- Server for user authentication. There is provision for both remote (RADIUS) and local (device) authentication.
- A Role-Based Access Control (RBAC) system that provides a permission model that allows access to the device operations and configurations based on specific roles and individual user accounts configured on the AAA server. That is, Administrator, Engineer, Operator, and Viewer roles are used.
- Security event reporting through both proprietary event logs and the Syslog protocol for supporting Security Information Event Management (SIEM) systems for centralised cybersecurity monitoring.
- Encryption of passwords – stored within the IED, in network messages between the MiCOM S1 Agile software and the IED, and in network messages between the RADIUS server and the IED (subject to the RADIUS server configuration).

### 23.5.1 INITIAL SETUP

The requirements for initial setup of the IED for cyber-security and RBAC will depend on:

1. which interfaces, if any, the cyber-security is required,
2. the intended authentication method, as defined in the setting ***Auth. Method*** in *SECURITY CONFIG* column (see the Authentication methods section).

When the authentication method is configured as `Device Only`, there are four pre-defined usernames, **VIEWER**, **OPERATOR, ENGINEER**, and **ADMINISTRATOR** that align with the **VIEWER**, **OPERATOR**, **ENGINEER** and **ADMINISTRATOR** roles (see the Device Users section).

When the authentication method is configured as ‘Server Only’ or ‘Server + Device’, users must be set up on the Radius server (see the RADIUS users section). These users are separate from the pre-defined Device users. RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication (see the RADIUS server settings section). It is recommended that the Radius shared secret be changed from the default (see the RADIUS client-server validation section).

Whatever the authentication method, it is strongly recommended that the password for the Administrator be changed from the default. Changing the passwords for the other roles is optional.

# 23.6 ROLES AND PERMISSIONS

## 23.6.1 ROLES

The P40 Agile products provide 4 specific roles to which individual user accounts can be configured:

- VIEWER (Level 0) Read some, Write minimal
- OPERATOR (Level 1) Read All, Write Few
- ENGINEER (Level 2) Read All, Write Some
- ADMINISTRATOR (Level 3) Read All, Write All

Only one role of one type is allowed to be logged in at a time. For example, one Operator can be logged in but not a second Operator at the same time. This prevents subsets of settings from being changed at the same time.

Roles are mapped to Access Level definitions:

**VIEWER** - No password required - Read access to Security features, Model Number, Serial Number, S/W version, Description, Plant reference, Security code (UI Only), Encryption key (UI Only), User Banner and security related cells. This role will allow maximum concurrent access provided by P40. Viewer is the default role

**OPERATOR -** Operator password required - Read access to all data and settings. Write access to Primary/ Secondary selector, Operator password setting, Password reset cell and log extraction cells (record selector). This role will not allow concurrent access.

**ENGINEER -** Engineer password required - Read access to all data and settings. Write access to Reset demands and counters. This role will not allow concurrent access.

**ADMINISTRATOR -** Administrator password required - Read access to all data and settings. Write access to All settings, PSL, IED Config, Security settings (port disabling etc). This role can enable the bypass mode and forcefully logout any other role. This role will not allow concurrent access.

The IED defines the following roles with reference to the roles defined by IEC 62351-8.

| P40 Roles | IEC 62351- 8 Roles | Access Level |
|---|---|---|
| **VIEWER** | VIEWER | Level 0 |
| **OPERATOR** | OPERATOR | Level 1 |
| **ENGINEER** | ENGINEER | Level 2 |
| **ADMINISTRATOR** | SECADM + SECAUD | Level 3 |

By default, the IED is delivered with default factory roles account and passwords. These default passwords are shown in the below table.

| Role | Default Password |
|---|---|
| **ADMINISTRATOR** | ChangeMe1# |
| **ENGINEER** | ChangeMe1# |
| **OPERATOR** | ChangeMe1# |
| **VIEWER** | NA |

*Note:*
*It is strongly recommended that the password for the Administrator be changed from the default. Changing the passwords for the other roles is optional.*

Administrators have the following rights as well:

- Setting the Bypass mode
- Forcefully logging out any other role
- Setting Authentication Method

'Firmware lock' is not supported by the P40 Agile IED. Firmware upgrade is not managed by the main software. The process involves using a dedicated firmware loading software tool. There is no access or control to this process via the main product firmware.

### 23.6.2 PERMISSIONS

Authentication and authorization are two different processes. An authenticated user cannot perform any action on the IED unless a privilege has been explicitly granted to them. This is the concept of “least privileges” access.

Privileges must be granted to users through roles. A role is a collection of privileges, and roles are granted to users. Each user is associated to only one role. The privilege/role matrix is stored on the IED. This is known as Role-Based-Access Control (RBAC).

On successful user authentication, the IED will load the user’s role list. If the user’s role changes, the user must logout and log back in to exercise his/her privileges.

Existing User level/permission mapping in P40 are:

| Role | Meaning | Read Operation | Write Operation |
|---|---|---|---|
| VIEWER | Read Some<br>Write Minimal | SYSTEM DATA column:<br>Description<br>Plant Reference<br>Model Number<br>Serial Number<br>S/W Ref.<br>Access Level<br>Security Feature<br>SECURITY CONFIG column:<br>User Banner<br>Attempts Remain<br>Blk Time Remain<br>Fallback PW level<br>Security Code (UI only) | Password Entry<br>LCD Contrast (UI only) |
| OPERATOR | Read All<br>Write Few | All data and settings are readable.<br>Poll Measurements | All items writeable at "Viewer".<br>Select Event, Main and Fault (upload)<br>Extract Events (e.g. via MiCOM S1 Agile) |
| ENGINEER | Read All<br>Write Some | All data and settings are readable.<br>Poll Measurements | All items writeable at "Operator".<br>Setting Cells that change visibility (Visible/Invisible).<br>Setting Values (Primary/Secondary) selector<br>Commands:<br>Reset Indication<br>Reset Demand<br>Reset Statistics<br>Reset CB Data / counters |

| Role | Meaning | Read Operation | Write Operation |
|---|---|---|---|
| ADMINISTRATOR | Read All<br>Write All | All data and settings are readable.<br>Poll Measurements | All items writeable at "Engineer".<br>Change all Setting cells<br>Operations:<br>Extract and download Setting file.<br>Extract and download PSL<br>Extract and download MCL (IEC 61850)<br>Extraction of Disturbance Recorder<br>Courier/MODBUS Accept Event (auto event extraction, e.g. via AE2R)<br>Commands:<br>Change Active Group setting<br>Close/Open CB<br>Change Comms device address.<br>Set Date & Time<br>Switch MCL banks/Switch Conf. Bank in UI (IEC 61850)<br>Enable/Disable Device ports (in SECURITY CONFIG column)<br>All password settings<br>Bypass Enable/disable<br>Change Authentication Method |

The table below shows the predefined permissions assignment for the predefined Roles according to IEC 62351-8

| Role | View | Read | Dataset | Report | File Read | File Write | File Mngt | Control | Config. | Setting Group | Security |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **VIEWER** | x | | | x | | | | | | | |
| **OPERATOR** | x | x | | x | | | | x | | | |
| **ENGINEER** | x | x | x | x | | x | x | | x | | |
| **ADMINISTRATOR** | x | x | x | x | x | x | x | x | x | x | x |

The table below shows the predefined permissions description according to IEC 62351-8

| Permission | Description |
|---|---|
| VIEW | Allows the subject/role to discover what objects are present within a Logical Device by presenting the type ID of those objects. |
| READ | Allows the subject/role to obtain all or some of the values in addition to the type and ID of objects that are present within a Logical-Device |
| DATASET | Allows the subject/role to have full management rights for both permanent and non-permanent DataSets |
| REPORTING | Allows a subject/role to use buffered reporting as well as un-buffered reporting |
| FILEREAD | Allows the subject/role to have read rights for file objects |
| FILEWRITE | Allows the subject/role to have write rights for file objects. This right includes the FILEREAD right |
| FILEMNGT | Allows the role to transfer files to the Logical-Device, as well as delete existing files on the Logical-Device |
| CONTROL | Allows a subject to perform control operations |
| CONFIG | Allows a subject to locally or remotely configure certain aspects of the server |
| SETTINGGROUP | Allows a subject to remotely configure Settings Groups |
| SECURITY | Allows a subject/role to perform security functions at both a Server/Service Access Point and Logical-Device basis |

# 23.7 AUTHENTICATION

## 23.7.1 AUTHENTICATION METHODS

The IED supports Bypass (no authentication), Device authentication and Server authentication.

| Authentication Method | Description |
|---|---|
| Bypass Auth. | IED does not provide security, any user (Local/Remote) can login to the IED. IED does not validate user and password. In this case, there is no need to enter user-id and password to login. |
| Device Only | IED allows role access using local authentication. |
| Server Only | IED uses RADIUS server to validate access. |
| Server + Device | IED uses server authentication to validate user first. And it allows fallback to device authentication if the RADIUS server(s) are unavailable. |

If ***Bypass Auth.*** is enabled, the IED ignores the ***Auth. Method*** setting.

The ***Auth. Method*** setting offers the following options for user authentication:

- *Server + Device* (This is the default setting for IEC 61850+Courier; IEC 61850+103; DNP3OE - where applicable)
- *Device Only* (This is the default setting for Courier/IEC 60870-5-103/MODBUS/DNP3)
- *Server Only*

Only an **ADMINISTRATOR** role may change the ***Auth. Method*** setting. If Administrator changes it, the role remains logged in. But only when the user log-out, their access-level is revoked.

If Authentication method is *Server Only* and RADIUS Server IP addresses are configured, no device user has access to the IED (only the RADIUS users will have access). Only the RADIUS Administrator role will be able to switch to "Server and Device auth". When the setting is “Server Only” but RADIUS Server IP are not configured (both Primary & Secondary are 0.0.0.0), the IED will automatically fall back to Device authentication.

When Authentication method is *Server Only*, if the RADIUS server(s) are unavailable, the user should first take actions to recover the RADIUS connection. If both RADIUS servers ultimately failed to recover, the user should follow the password reset procedure to reset the ***Auth. Method*** setting to *Device Only*.

## 23.7.2 BYPASS

In ***Bypass Auth.*** mode, the IED does not provide security - any user can login. IED does not validate user and password. The bypass security feature provides an easier access, with no authentication and encryption for situations when this is considered safe. Only the Administrator can enable Bypass mode.

There are five modes for authentication bypass:

1. *Disabled* – no interfaces in ***Bypass Auth.*** mode (normal authentication is active)
2. *Local & Remote*
    a. Front Panel;
    b. Front Port
    c. Rear Ports
    d. Ethernet

3. *Local* – will bypass authentication for
   a. Front Panel;
   b. Front Port
4. *Remote* – will bypass authentication for
   a. Ethernet
   b. Rear Ports
5. *HMI-Only* – will bypass authentication only for front panel

| Bypass Authentication for Bypass Mode: | Front panel | Front Port | Rear Port | Ethernet |
|---|---|---|---|---|
| *Disabled* | | | | |
| *Local & Remote* | X | X | X | X |
| *Local* | X | X | | |
| *Remote* | | | X | X |
| *HMI-Only* | X | | | |

The DDB signal ***Security Bypass*** is available to indicate that the IED is in ***Bypass Auth.*** mode.

### 23.7.3 LOGIN

A user can only login through the following methods:

- Front Panel User Interface
- Using MiCOM S1 Agile, connected to either the Front Port, Rear Port 1 or 2, or NIC (Ethernet) interface.

The interfaces/protocols implemented in P40 are listed in the following table.

The product supports both RBAC (with *Server + Device* authentication) and original Access Level. The Courier Interfaces/HMI use the RBAC whilst other protocols such as MODBUS, IEC 60870-5-103, DNP3 use the original Access Level to authenticate.

The following table shows different product variants that supports different protocols on Rear ports and Network port.

| Local Access | Front Port | Rear Port (1/2) | NIC (Ethernet) Port | Supported Auth. Mechanism |
|---|---|---|---|---|
| HMI<br>Courier | Courier | Courier | - | Device |
| HMI<br>Courier | Courier | Courier | IEC 61850 + SNMP + Courier tunnel | Server and Device |
| HMI<br>Courier | Courier | MODBUS<br>(no server, device auth only, old access levels) | - | Device<br>Old Access level for MODBUS |
| HMI<br>Courier | Courier | IEC 60870-5-103<br>(no server, device auth only, old access levels) | - | Device<br>Old Access level for 103 |
| HMI<br>Courier | Courier | IEC 60870-5-103<br>(no server, device auth only, old access levels) | IEC 61850 + SNMP + Courier tunnel | Server and Device<br>Old Access level for 103 |

| Local Access | Front Port | Rear Port (1/2) | NIC (Ethernet) Port | Supported Auth. Mechanism |
|---|---|---|---|---|
| HMI<br>Courier | Courier | DNP3<br>(no server, device auth only, old access levels) | - | Device<br>Old Access level for DNP3 |
| HMI<br>Courier | Courier | Courier | DNP3 + SNMP + Courier tunnel | Server and Device<br>Old Access level for DNP3 |

#### 23.7.3.1 FRONT PANEL LOGIN

Front panel User Interface supports both Device authentication and Server authentication. The P40 gives the user the option to enter a username in HMI panel.

The user can type their password in the password cell.

For Device authentication, the user must enter one of the pre-defined usernames **VIEWER**, **OPERATOR**, **ENGINEER**, **ADMINISTRATOR**. The user can scroll through these names using either of the hotkeys. Users must then enter their password.

For Server authentication, the user can enter any valid pre-defined Radius server username. Using the front panel User Interface, the user can change the displayed character type (digit, uppercase letter, lowercase letter, special character) by either of the hotkeys. For ease of typing, it is preferable to do Server authentication login using MiCOM S1 Agile.

After successful log in, a confirmation message is displayed, showing the logged in username. For example:

```
LOGIN SUCCESS
OPERATOR
```

#### 23.7.3.2 MICOM S1 LOGIN

When the user attempts to login, MiCOM S1 Agile will prompt the user with a login dialog box that contains a username text entry field and a password text entry field. The username field is a combo-dropdown style text field that includes the fixed usernames (**Administrator**, **Engineer**, **Operator**, **Viewer**) for Device authentication - the user can pick one of these if they wish, or type any other pre-defined username for Radius authentication in the textbox.

#### 23.7.3.3 WARNING BANNER

After successful authentication and authorisation to access the IED, MiCOM S1 Agile will display a security warning banner to the user.

If **I Agree** is selected, the integrated authentication and authorisation is completed. Selecting **I Disagree** causes the program to close and the login user to logout.

For S1 Agile authentication, this is a pop-up dialog that the user must click to acknowledge.

#### 23.7.3.4 LOGIN FAILED

When Device authentication fails, a failure message is displayed:

```
LOGIN FAILED
```

For front panel authentication, this is shown for 2 seconds on the LCD.

For S1 Agile authentication, this is a pop-up dialog that the user must click to acknowledge.

### 23.7.4 USER SESSIONS

Open sessions will be automatically closed by the IED after a configurable session timeout.

The inactivity timer configuration setting defines the period of time that the IED waits in idleness before a logged in user is automatically logged out.

If there is any data change that does not commit to IED, the data change is discarded when user logged out. If there is any access that does not finish, the access will fail when user logged out. Front panel will display the default page when user reaches the defined inactivity time.

If the keypad is inactive for configured UI inactivity timer, user logout message is displayed. And front panel user interface reverts to the Viewer access level.

Currently in the P40, the inactivity timer for both front port and HMI is fixed to 15 minutes. Already, ***RP1 InactivTimer*** and ***RP2 InactivTimer*** settings control the inactivity timer for RP1 and RP2. There are two new settings to support configurable inactivity timer for front port and front panel user interface:

- ***FP InactvTimer***
- ***UI InactivTimer***

Administrator, Operator and Engineer roles will accept only one session to the device at one time. Only Viewer allows 4 concurrent sessions at one time.

Only one user session is allowed from all the access methods mentioned below:

- Front Panel Push buttons
- Front Port (serial) FP1
- Rear Port 1 (RP1)
- Rear Port 2 (RP2)
- Ethernet Port (NIC)

| Setting Name | Description | Min | Max | Default | Units | Minimum Permissions |
|---|---|---|---|---|---|---|
| Attempts Limit | Number of failed authentications before the device blocks subsequent authentication attempts for the lockout period. A value of 0 means Lockout is disabled. | 0 (lockout disabled) | 99 | 3 | - | Administrator |
| Lockout Period | The period of time in seconds a user is prevented from logging in, after being locked out. | 1 | 5940 | 5 | sec | Administrator |
| FP InactivTimer | FP Inactivity Timer is the time of idleness on Front Port before a logged in user is automatically logged out and revert the access level to the viewer role | 0 (no Inactivity Timeout) | 30 | 10 | min | Administrator |
| UI InactivTimer | UI Inactivity Timer is the time of idleness on Front Panel before a logged in user is automatically logged out and revert the access level to the viewer role | 0 (no Inactivity Timeout) | 30 | 10 | min | Administrator |

The recommended settings for ***Attempts Limit*** is `3` and ***Lockout Period*** is `5 sec` to discourage brute force attacks. If the Lockout period is too large, anybody can lockout Device users.

## 23.7.5 USER LOCKING POLICY

A local user locking policy is implemented for Device access:

- This user locking policy applies to both Device users.
- The account is unlocked at the first successful login after the ***Lockout Period***
- By default, if the user consecutively fails to login 3 times, the user account will be locked for 3 minutes.

Each user account records how long it has been locked if the account is locked.

Each user account records how many times it has consecutively failed to login. User account failed times include all interfaces login attempts. For example, if the ***Attempts Limit*** setting is *3* and the operator failed to login from front panel 2 times, and they changed to login from the Courier interface, but failed again, then the Operator would be locked out.

When the IED is powered on, these ***Attempts Limit*** counter resets to zero.

When the user account exceeds the ***Attempts Limit*** it is locked for ***Lockout period***, at that time ***Attempt limit*** resets to zero.

The locked user account will be unlocked automatically, after the configured “Lockout Period” is expired.

All user accounts need to wait until the lockout period expires. No user can unlock the locked account.

If the locked account attempts to login the IED from the Front Panel, the following text is displayed (example):

```
OPERATOR
IS LOCKED
```

Usernames are specific to each user account, such as **Engineer**, **Operator** and **Administrator** for Device authentication.

When supporting both RBAC enabled interfaces and non-RBAC interfaces (such as MODBUS), the P40 handles features such as user-locking feature as follows

- If an RBAC user exceeds the invalid password limit, that user gets locked for all the interfaces.
- On a non-RBAC interface, if an Access Level exceeds the invalid password limit, P40 only blocks that.

## 23.7.6 LOGOUT

Each user should ***Log out*** after reading or configuring the IED.

Both S1 Agile and the Front Panel provide a one step logout.

The user can only log out from the front panel, if they logged in from the front panel. If the user logged in from S1 Agile, they have to logout from S1 Agile.

### 23.7.6.1 FRONT PANEL LOGOUT

Go up to the top of the menu tree. When you are at the Column Heading level and you press the Up button, you may be prompted to log out with the following display:

```
ENTER TO LOGOUT
CLEAR TO CANCEL
```

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT <ROLE NAME>
LOGGED OUT
ADMINISTRATOR
```

If you decide not to log out (i.e. you cancel), the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
ADMINISTRATOR
```

#### 23.7.6.2 MICOM S1 LOGOUT

Right-click on the device name in the System Explorer panel in MiCOM S1 Agile and select **Log Off**.

In the Log Off confirmation dialog, click **Yes**.

### 23.7.7 DEVICE USERS

For device authentication, the user must enter one of the pre-defined usernames **VIEWER**, **OPERATOR**, **ENGINEER**, or **ADMINISTRATOR**. This means that device users and roles are same in the P40, and therefore there can be only one user for each role.

### 23.7.8 PASSWORD POLICY

Cyber-security requires strong passwords and validation for NERC compliance.

The NERC password complexity policy requires an alpha-numeric password (for all accesses, front panel, and network/local port) that meets the following **mandatory** requirements:

1. Passwords cannot contain the user's account name or parts of the user's full name that exceed two consecutive characters.
2. Passwords must be at least eight characters in length, but not exceed 16 characters in length.
3. Passwords must contain characters from all four categories:
   a. English uppercase characters (A through Z).
   b. English lowercase characters (a through z).
   c. Numeric (digits 0 through 9).
   d. Special non-alphanumeric characters (such as @,!,#,{, but not limited to only those)

For Device authentication, the IED will enforce that configured passwords meet these requirements.

For Server authentication, the password complexity and user locking policy is defined in the external Radius server.

### 23.7.9 CHANGE PASSWORD

In the Device authentication mode, **VIEWER** does not have a password associated with it.

The password can be changed either from the front panel User Interface, or from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

**Caution:**
**It is recommended that user passwords are changed periodically.**

### 23.7.10 RADIUS

When the ***Auth. Method*** setting is configured as *Server Only* or *Server + Device*, a user must log in with a username and password that has been predefined on the Radius server.

This log in can be performed from any interface, as described in the Login section. The IED will authenticate the user to the active RADIUS server, over the Ethernet connection.

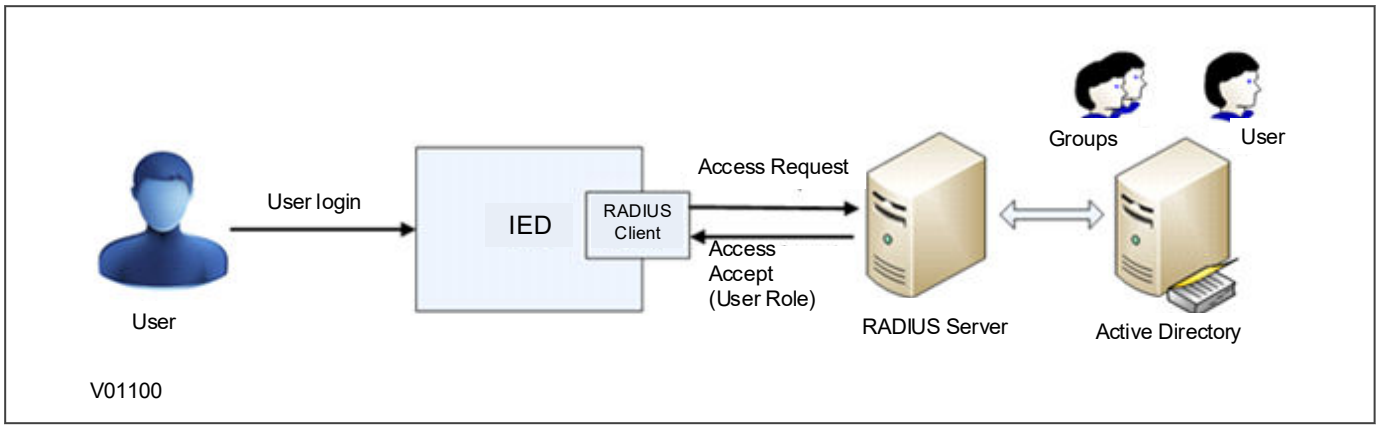


**Figure 289: RADIUS server/client communication**

### 23.7.10.1 RADIUS USERS

For Server authentication, RADIUS users and passwords are created in the RADIUS server (in the Active Directory).

The username must consist of uppercase letters (A to Z) and digits (0 to 9) only. No lowercase letters or special characters are allowed.

Each RADIUS user must have a password that meets the password policy of the Active Directory (not the password policy of the P40) and have one of the four roles assigned in the Active Directory.

The number of RADIUS users is not limited by the IED.

RADIUS password changes are done in the Active Directory (after password expiration).

### 23.7.10.2 RADIUS CLIENT

Two Radius servers are supported by the IED in the configuration for redundancy. The IED will try each in sequence until one responds.

The IED will first try server 1 up to the configured number of retries, leaving a request timeout between each request. If, after this point there is still no valid answer from server 1, the IED will switch to server 2 and repeat for up to the configured number of retries.

If the number of retries for the second server is exceeded, the IED will give up entirely on Server authentication. If Authentication Method is *Server + Device*, the IED will fallback to Device authentication. A **RADIUS Server unavailable** security event is also logged under this condition.

The RADIUS implementation supports the following authentication protocols:

- EAP-TTLS-MSCHAP2
- PAP
- EAP-PEAP-MSCHAP2
- PAP EAP-TTLS-PAP (Default)

The RADIUS implementation queries the Role ID vendor attribute and establish the logged in user security context with that role.

| RADIUS Config. | Value |
|---|---|
| Vendor ID | 2910 |
| Vendor Attribute | 1 |

| RADIUS Config. | Value |
|---|---|
| **P40 Role Values** | |
| Administrator | 3 |
| Engineer | 2 |
| Operator | 1 |
| Viewer | 0 |

### 23.7.10.3 RADIUS SERVER SETTINGS

The following RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication.

| Setting Name | Description | Min | Max | Default | Units | Minimum Permissions |
|---|---|---|---|---|---|---|
| **RADIUS** Pri IP | IP address of Server 1. Default value indicates no Primary Radius server is configured, and so Radius is disabled. | 0.0.0.0 | 255.255.255.255 | 0.0.0.0 | - | Administrator |
| RADIUS Sec IP | IP address of Server 2. Default value indicates no Secondary Radius server is configured | 0.0.0.0 | 255.255.255.255 | 0.0.0.0 | - | Administrator |
| RADIUS Auth Port | Radius authentication port | 1 | 65535 | 1812 | - | Administrator |
| RADIUS Security | Authentication protocol to be used by Radius server | EAP-TTLS-MSCHAP2<br>PAP<br>EAP-PEAP-MSCHAP2<br>PAP EAP-TTLS-PAP | | PAP EAP-TTLS-PAP | - | Administrator |
| RADIUS Timeout | Timeout in seconds between re-transmission requests | 1 | 900 | 2 | sec | Administrator |
| RADIUS Retries | Number of retries before giving up | 1 | 99 | 10 | - | Administrator |
| RADIUS Secret | Shared Secret used in authentication. It is only displayed as asterisks. | 1 character | 16 characters | ChangeMe1# | - | Administrator |

The data cell ***RADIUS Status*** indicates the status of the currently-selected RADIUS server. This will display either *Disabled*, *Server OK*, or *Failed*.

### 23.7.10.4 RADIUS ACCOUNTING

RADIUS accounting is not supported by the IED. The user can achieve accounting through syslog (see the SYSLOG section).

#### 23.7.10.5 RADIUS CLIENT-SERVER VALIDATION

Client-server validation is achieved using a shared secret. The IED must be configured with the ***RADIUS Secret*** setting to match the shared secret configured in the RADIUS server. It is recommended (but not enforced) that this setting meets the P40 password requirements.

> *Note:*
> *It is recommended that the shared secret be changed from the default before using Radius authentication.*

The IED does not support exchange of CA certificates. The RADIUS server may send a certificate but the IED will not verify it.

### 23.7.11 RECOVERY

#### 23.7.11.1 RESTORE TO LOCAL FACTORY DEFAULT

The ***Restore Defaults*** setting is available to facilitate NERC CIP compliance requirements for decommissioning critical cyber devices. Only the **Administrator** role can change this setting.

The ***Restore Defaults*** setting under the *CONFIGURATION* column is used to restore a setting group to factory default settings.

0 = `No Operation`

1 = `All Settings`

2 = `Setting Group 1`

3 = `Setting Group 2`

4 = `Setting Group 3`

5 = `Setting Group 4`

To restore the default values to the settings in any setting group, set the ***Restore Defaults*** setting to the relevant Group number. Alternatively, it is possible to set the ***Restore Defaults*** setting to `All Settings` to restore the default values to all the IEDs settings, not only one setting group.

> *Note:*
> *Restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.*

Data (events, DR, fault records, protection counters etc) is left untouched. When decommissioning critical cyber IEDs, users may want to clear all data and events as well.

#### 23.7.11.2 PASSWORD RESET PROCEDURE

If you mislay a devices password (if Administrator forgets their password), the passwords can be reset to default using a recovery password. To obtain the recovery password you must contact the Contact Centre and supply the Serial Number and the security code. The Contact Centre will use these items to generate a Recovery Password.

> *Note:*
> *The Test ID on the label in the top compartment of the front panel is the serial number of the relay and consists of 6 numeric and 1 alphanumeric characters, for example 123456Z. The serial number is also shown in the System Data menu of the HMI. This serial number can be used to obtain the recovery password from the Contact Centre.*
> *The serial number on the label in the top compartment of the front panel is the SAP manufacturing serial number and consists of 8 numeric characters, for example 37123456.*

The security code is a 16-character string of uppercase characters. It is a read-only parameter. The device generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

This reset procedure can be only accomplished through front panel exclusively and cannot be done over any other interface. As soon as the security code is displayed on the front panel User Interface, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the Contact Centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the Contact Centre over weekends and bank holidays.

The procedure is:

The security code is displayed on confirmation. The validity timer is then started. The security code can only be read from the front panel.

This reset procedure can be only accomplished through front panel exclusively and cannot be done over the Ethernet/serial port, but only when physically present in front of the IED. In the event of losing all passwords (if the Administrator forgets their password) the user could reset the IED to default passwords, following the procedure below:

1. User navigates to ***Security Code*** cell in *SECURITY CONFIG* column
2. To prevent accidental reading of the IED ***Security Code***, the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

3. Press Enter to read the ***Security Code***.
4. User sends an email to the Contact Centre providing the full IED serial number and displayed ***Security Code***, using a recognisable corporate email account
5. Contact Centre emails the user with the Recovery Password. The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.
6. User logs in with the username **ADMINISTRATOR** and the recovery password in to the ***Password*** setting in *SYSTEM DATA* column.
7. Then IED will prompt

```
RESET PASSWORD?
ENTER or CLEAR
```

8. Press Enter to continue the reset procedure
9. If the recovery password successfully validates, the default passwords are restored for each access level for Device authentication.
10. Change ***Auth. Method*** setting to `Server + Device` if applicable.

*Note:*
*Restoring passwords to defaults does not affect any other settings and does not provoke reboot of the IED. The protection and control functions of the IED are always maintained.*

### 23.7.11.3 ACCESS LEVEL DDBS

The current level of access for each interface is available for use in the Programmable Scheme Logic (PSL) as these DDB signals:

- ***HMI Access Lvl 1***
- ***HMI Access Lvl 2***
- ***FPort AccessLvl1***
- ***FPort AccessLvl2***
- ***RPrt1 AccessLvl1***
- ***RPrt1 AccessLvl2***
- ***RPrt2 AccessLvl1***
- ***RPrt2 AccessLvl2***

Each pair of DDB signals indicates the access level as follows:

- Level 1 off, Level 2 off = 0
- Level 1 on, Level 2 off = 1
- Level 1 off, Level 2 on = 2
- Level 1 on, Level 2 on = 3

**KEY:**

HMI = Human Machine Interface

FPort = Front Port

RPrt = Rear Port

Lvl = Level

## 23.7.12 DISABLING PHYSICAL PORTS

It is possible to disable unused physical ports. A level 3 password is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example, if rear port 1 is to be disabled, the following message appears:

```
REAR PORT 1 TO BE
DISABLED.CONFIRM
```

The following ports can be disabled, depending on the model.

- Front port (***Front Port*** setting)
- Rear port 1 (***Rear Port 1*** setting)
- Rear port 2 (***Rear Port 2*** setting)
- Ethernet port (***Ethernet Port*** setting)

*Note:*
*It is not possible to disable a port from which the disabling port command originates.*
*We do not generally advise disabling the physical Ethernet port.*

## 23.7.13 DISABLING LOGICAL PORTS

It is possible to disable unused logical ports. A level 3 password is needed to perform this action.

*Note:*
*The port disabling setting cells are not provided in the settings file. It is only possible to do this using the HMI front panel.*

The following protocols can be disabled:

- IEC 61850 (***IEC 61850*** setting)
- DNP3 Over Ethernet (***DNP3 OE*** setting)--where available
- Courier Tunnelling (***Courier Tunnel*** setting)

*Note:*
*If any of these protocols are enabled or disabled, the Ethernet card will reboot.*

## 23.8 SECURITY EVENT MANAGEMENT

To implement NERC-compliant cyber-security, a range of security events are logged in the Security Event file.

### 23.8.1 SECURITY EVENTS: COURIER

| Event Value | Display |
|---|---|
| PASSWORD LEVEL UNLOCKED | USER LOGGED IN<br>ON {int} LEVEL {n} |
| PASSWORD LEVEL RESET | USER LOGGED OUT<br>ON {int} LEVEL {n} |
| PASSWORD SET BLANK | P/WORD SET BLANK<br>BY {int} LEVEL {p} |
| PASSWORD SET NON-COMPLIANT | P/WORD NOT-NERC<br>BY {int} LEVEL {p} |
| PASSWORD MODIFIED | PASSWORD CHANGED<br>BY {int} LEVEL {p} |
| PASSWORD ENTRY BLOCKED | PASSWORD BLOCKED<br>ON {int} |
| PASSWORD ENTRY UNBLOCKED | P/WORD UNBLOCKED<br>ON {int} |
| INVALID PASSWORD ENTERED | INV P/W ENTERED<br>ON <int} |
| PASSWORD EXPIRED | P/WORD EXPIRED<br>ON {int} |
| PASSWORD ENTERED WHILE BLOCKED | P/W ENT WHEN BLK<br>ON {int} |
| RECOVERY PASSWORD ENTERED | RCVY P/W ENTERED<br>ON {int} |
| IED SECURITY CODE READ | IED SEC CODE RD<br>ON {int} |
| IED SECURITY CODE TIMER EXPIRED | IED SEC CODE EXP<br>- |
| PORT DISABLED | PORT DISABLED<br>BY {int} PORT {prt} |
| PORT ENABLED | PORT ENABLED<br>BY {int} PORT {prt} |
| DEF. DISPLAY NOT NERC COMPLIANT | DEF DSP NOT-NERC |
| PSL SETTINGS DOWNLOADED | PSL STNG D/LOAD<br>BY {int} GROUP {grp} |
| DNP SETTINGS DOWNLOADED | DNP STNG D/LOAD<br>BY {int} |
| TRACE DATA DOWNLOADED | TRACE DAT D/LOAD<br>BY {int} |
| IEC 61850 CONFIG DOWNLOADED | IED CONFG D/LOAD<br>BY {int} |
| USER CURVES DOWNLOADED | USER CRV D/LOAD<br>BY {int} GROUP {crv} |

| Event Value | Display |
|---|---|
| PSL CONFIG DOWNLOADED | PSL CONFG D/LOAD<br>BY {int} GROUP {grp} |
| SETTINGS DOWNLOADED | SETTINGS D/LOAD<br>BY {int} GROUP {grp} |
| PSL SETTINGS UPLOADED | PSL STNG UPLOAD<br>BY {int} GROUP {grp} |
| DNP SETTINGS UPLOADED | DNP STNG UPLOAD<br>BY {int} |
| TRACE DATA UPLOADED | TRACE DAT UPLOAD<br>BY {int} |
| IEC 61850 CONFIG UPLOADED | IED CONFG UPLOAD<br>BY {int} |
| USER CURVES UPLOADED | USER CRV UPLOAD<br>BY {int} GROUP {crv} |
| PSL CONFIG UPLOADED | PSL CONFG UPLOAD<br>BY {int} GROUP {grp} |
| SETTINGS UPLOADED | SETTINGS UPLOAD<br>BY {int} GROUP {grp} |
| EVENTS HAVE BEEN EXTRACTED | EVENTS EXTRACTED<br>BY {int} {nov} EVNTS |
| ACTIVE GROUP CHANGED | ACTIVE GRP CHNGE<br>BY {int} GROUP {grp} |
| CS SETTINGS CHANGED | C & S CHANGED<br>BY {int} |
| DR SETTINGS CHANGED | DR CHANGED<br>BY {int} |
| SETTING GROUP CHANGED | SETTINGS CHANGED<br>BY {int} GROUP {grp} |
| POWER ON | POWER ON<br>- |
| SOFTWARE_DOWNLOADED | S/W DOWNLOADED<br>- |

where:

- int is the interface definition (UI, FP, RP1, RP2, TNL, TCP)
- prt is the port ID (FP, RP1, RP2, TNL, DNP3, IEC, ETHR)
- grp is the group number (1, 2, 3, 4)
- crv is the Curve group number (1, 2, 3, 4)
- n is the new access level (0, 1, 2, 3)
- p is the password level (1, 2, 3)
- nov is the number of events (1 - nnn)

Each new event has an incremented unique number, therefore missing events appear as gap in the sequence. The unique identifier forms part of the event record that is read or uploaded from the IED.

*Note:*
*It is no longer possible to clear Event, Fault, Maintenance, and Disturbance Records.*

### 23.8.2 SYSLOG

Security events are also logged to a remote syslog server.

All login and logout attempts from local and central authentication, whether successful or failed, are logged. The contents of each successful or failed, login and logout security event include a specific username.

The security log cannot be cleaned by any of the available roles.

The contents of each login and/or logout security event include the relevant interface. The following interfaces are supported:

| Interface | Abbr. |
|---|---|
| Front Port | FP |
| Rear Port 1 | RP1 |
| Rear Port 2 | RP2 |
| Ethernet | NET |
| Front Panel | UI |

The following events are available to be logged to the syslog server:

| Event Categorisation | Severity |
|---|---|
| Login - Authentication successful | Informational (6) |
| Login - Authentication Failure | Informational (6) |
| Logout | Informational (6) |
| RADIUS Server Unavailable | Alert (1) |
| Session timeout | Informational (6) |
| Account Locked | Notice (5) |
| User accessed while locked | Notice (5) |
| ByPass Activate | Notice (5) |
| ByPass Deactivate | Notice (5) |
| Password Change | Notice (5) |
| Recovery password is entered to reset the passwords | Notice (5) |
| Settings/Configuration Changed | Notice (5) |
| Settings/Configuration uploaded (to S1 Agile) | Notice (5) |
| Event Records uploaded | Notice (5) |
| Default settings restored | Notice (5) |
| Active Setting Group Changed | Notice (5) |
| | Notice (5) |
| | Notice (5) |
| | Notice (5) |
| Default user curves restored | Notice (5) |
| | Notice (5) |
| | Notice (5) |

### 23.8.3 SYSLOG CLIENT

The IED supports security event reporting through the Syslog protocol for supporting Security Information Event Management (SIEM) systems for centralized cyber security Monitoring over UDP protocol.

The IED is a Syslog client that supports two Syslog servers. The following settings are available in the *COMMUNICATIONS* column.

| Setting Name | Description | Min | Max | Default | Units | Min. Permission |
|---|---|---|---|---|---|---|
| SysLog Pri IP | The IP address of the target Syslog server (Primary) | 0.0.0.0 | 223.255.255.254 | 0.0.0.0 | - | Administrator |
| SysLog Sec IP | The IP address of the target Syslog server (Secondary) | 0.0.0.0 | 223.255.255.254 | 0.0.0.0 | - | Administrator |
| SysLog Port | The UDP port number of the target Syslog server | 1 | 65535 | 514 | - | Administrator |

### 23.8.4 SYSLOG FUNCTIONALITY

The P40 supports the RFC 5424 UDP protocol.

The table below shows the format of a Syslog event.

| | | |
|---|---|---|
| Header | <PRIVAL>1 YYYY-MM-DDTHH:mm:ss.fffZ IEDName userlog - MSGID | |
| | PRIVAL | 32 + [event severity]<br>32 is derived from the facility number 4 (meaning security/authorization messages)<br>Event severity is derived from the received message. |
| | YYYY | 4 Digit year; i.e. 2018<br>Derived from the received message timestamp. |
| | MM | 2 Digit month; 01 to 12 (for January to December).<br>Derived from the received message timestamp. |
| | DD | 2 Digit day of month; 01 to 31 (depending upon the month)<br>Derived from the received message timestamp. |
| | HH | 2 Digit hour of day; 00 to 23<br>Derived from the received message timestamp. |
| | mm | 2 Digit count of minutes elapsed in the current hour; 00 to 59<br>Derived from the received message timestamp. |
| | ss | 2 Digit count of seconds elapsed in the current minute; 00 to 59<br>Derived from the received message timestamp. |
| | fff | 3 Digit fraction of seconds (millisecond resolution); 0 to 999<br>Derived from the received message timestamp. |
| | IP Addr | IP Address assigned to the Ethernet Board. |
| | MSGID | Unique message type identity<br>Derived from the received message event type. |
| Data (common) | [timeQuality tzKnown=X] | |
| | X | Timezone quality attribute for event timestamp (in header)<br>0; indicating Local Time offset and DST settings are not enabled (i.e. timestamp is UTC) |

| | | |
|---|---|---|
| Data (Platform event) | [gePlatformEvt channel=IFACE accessLevel=AL evtid=UUID extra=EDATA] DETAIL | |
| | IFACE | Channel access type<br>Copied from the received message interface name. |
| | AL | Access Level<br>Copied from the received message access level. |
| | UUID | Unique event identification<br>Copied from the received message unique id. |
| | EDATA | Extra event data – meaning of which is specific to the event type (see MSGID in header)<br>Copied from the received message extra info. |
| | DETAIL | Event details.<br>Derived from the received message event text and value. |
| Data (Enhanced event) | [geUserInfo channel=IFACE loginId=USER] DETAIL | |
| | IFACE | Channel access type<br>Copied from the received message interface name. |
| | USER | Logged in username who generated the event<br>Copied from the received message user id. |
| | DETAIL | Event details.<br>Copied from the received message event text. |
| Formatted Examples: | <38>1 2018-02-06T11:46:32.074Z Feeder1 userlog - 5120 [timeQuality tzKnown=0][gePlatformEvt channel=UI accessLevel=3 evtid=4 extra=0] User Logged In on UI Level 3User Logged In on UI Level 3 <38>1 2018-02-06T11:46:32.074Z Feeder1 userlog - 9999 [timeQuality tzKnown=0][geUserInfo channel=UI loginId=user1] Login - Authentication successful | |

Sample Syslog messages are shown below:

| Event | Access Method | Syslog Message (As from Syslog Server) |
|---|---|---|
| Authentication Successful | UI | 04-17-2019 14:43:32 Auth.Info 192.168.1.30 1 1994-01-23T21:34:06.102Z 192.168.1.30 userlog - 9999 [timeQuality tzKnown=0][geUserInfo channel=FP loginid=ADMINISTRATOR] Login - Authentication successful |
| Authentication Failure | Serial | 04-19-201913:36:08Auth.Info192.168.1.301 1994-01-25T20:26:42.872Z 192.168.1.30 userlog - 9999 [timeQuality tzKnown=0][geUserInfo channel=RP1 loginid=ENGINEER] Login - Authentication fail |
| Network Login Success | Courier Tunnel (device authentication) | 04-17-201915:29:20Auth.Info192.168.1.301 1994-01-23T22:19:58.168Z 192.168.1.30 userlog - 9999 [timeQuality tzKnown=0][geUserInfo channel=NET loginid=ENGINEER] Login - Authentication successful |
| Logout | Serial | 04-19-201913:52:08Auth.Info192.168.1.301 1994-01-25T20:42:42.782Z 192.168.1.30 userlog - 9999 [timeQuality tzKnown=0][geUserInfo channel=RP1 loginid=ADMINISTRATOR] Logout |
| RADIUS Unavailable | FP | 04-18-201912:40:14Auth.Alert192.168.1.301 1994-01-24T19:30:55.839Z 192.168.1.30 userlog - 5163 [timeQuality tzKnown=0][gePlatformEvt channel=FP accessLevel=0 evtid=3715 extra=0] RADIUS UnAvailbl |
| Bypass Activated | FP | 04-18-201912:39:19Auth.Warning192.168.1.301 1994-01-24T19:30:00.573Z 192.168.1.30 userlog - 9998 [timeQuality tzKnown=0][geUserInfo channel=FP loginid=ADMINISTRATOR] ByPass Activated |
| Settings modified | Courier Tunnel | 04-18-201911:52:35Auth.Notice192.168.1.301 1994-01-24T18:43:16.537Z 192.168.1.30 userlog - 5149 [timeQuality tzKnown=0][gePlatformEvt channel=NET accessLevel=3 evtid=3677 extra=0] Settings Upload By TNL |

CHAPTER 24

# INSTALLATION

## 24.1 CHAPTER OVERVIEW

This chapter provides information about installing the product.

This chapter contains the following sections:

Chapter Overview 559
Handling the Goods 560
Mounting the Device 561
Cables and Connectors 563
Case Dimensions 568

## 24.2 HANDLING THE GOODS

Our products are of robust construction but require careful treatment before installation on site. This section discusses the requirements for receiving and unpacking the goods, as well as associated considerations regarding product care and personal safety.

**Caution:**
**Before lifting or moving the equipment you should be familiar with the Safety Information chapter of this manual.**

### 24.2.1 RECEIPT OF THE GOODS

On receipt, ensure the correct product has been delivered. Unpack the product immediately to ensure there has been no external damage in transit. If the product has been damaged, make a claim to the transport contractor and notify us promptly.

For products not intended for immediate installation, repack them in their original delivery packaging.

### 24.2.2 UNPACKING THE GOODS

When unpacking and installing the product, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any CDROMs or technical documentation (where included). These should accompany the unit to its destination substation and put in a dedicated place.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies where installation is being carried out at the same time as construction work.

### 24.2.3 STORING THE GOODS

If the unit is not installed immediately, store it in a place free from dust and moisture in its original packaging. Keep any dehumidifier bags included in the packing. The dehumidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals before replacing it in the carton. Ideally regeneration should be carried out in a ventilating, circulating oven at about 115°C. Bags should be placed on flat racks and spaced to allow circulation around them. The time taken for regeneration will depend on the size of the bag. If a ventilating, circulating oven is not available, when using an ordinary oven, open the door on a regular basis to let out the steam given off by the regenerating silica gel.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. Avoid storing in locations of high humidity. In locations of high humidity the packaging may become impregnated with moisture and the dehumidifier crystals will lose their efficiency.

The device can be stored between –25º to +70ºC for unlimited periods or between -40°C to + 85°C for up to 96 hours (see technical specifications).

To avoid deterioration of electrolytic capacitors, power up units that are stored in a de-energised state once a year, for one hour continuously.

### 24.2.4 DISMANTLING THE GOODS

If you need to dismantle the device, always observe standard ESD (Electrostatic Discharge) precautions. The minimum precautions to be followed are as follows:

- Use an antistatic wrist band earthed to a suitable earthing point.
- Avoid touching the electronic components and PCBs.

## 24.3 MOUNTING THE DEVICE

The products are dispatched either individually or as part of a panel or rack assembly.

Individual products are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres.

The products are designed so the fixing holes in the mounting flanges are only accessible when the access covers are open.

If you use a P991 or MMLG test block with the product, when viewed from the front, position the test block on the right-hand side of the associated product. This minimises the wiring between the product and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

### 24.3.1 FLUSH PANEL MOUNTING

Panel-mounted devices are flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

**Caution:**
**Do not use conventional self-tapping screws, because they have larger heads and could damage the faceplate.**

Alternatively, you can use tapped holes if the panel has a minimum thickness of 2.5 mm.

For applications where the product needs to be semi-projection or projection mounted, a range of collars are available.

If several products are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.

**Caution:**
**Do not fasten products with pop rivets because this makes them difficult to remove if repair becomes necessary.**

### 24.3.2 RACK MOUNTING

Panel-mounted variants can also be rack mounted using single-tier rack frames (our part number FX0021 001), as shown in the figure below. These frames are designed with dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm (19 inch) rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the products by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

**Caution:**
**Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS products because they have slightly larger heads.**

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

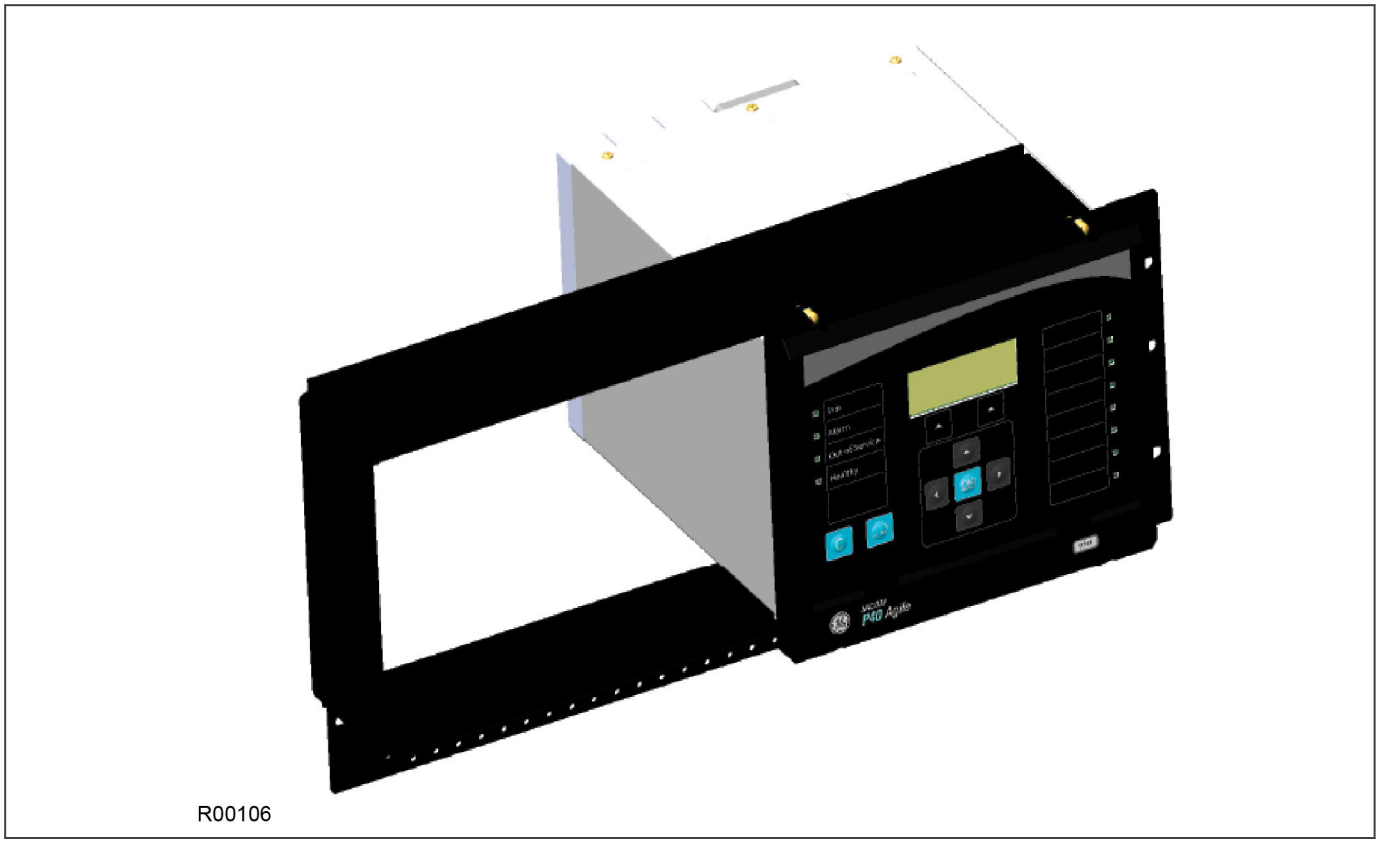


**Figure 290: Rack mounting of products**

Products can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from different product ranges to be pre-wired together before mounting.

Use blanking plates to fill any empty spaces. The spaces may be used for installing future products or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The part numbers are as follows:

| Case size summation | Blanking plate part number |
|---|---|
| 5TE | GJ2028 001 |
| 10TE | GJ2028 002 |
| 15TE | GJ2028 003 |
| 20TE | GJ2028 004 |
| 25TE | GJ2028 005 |
| 30TE | GJ2028 006 |
| 35TE | GJ2028 007 |
| 40TE | GJ2028 008 |
| 60TE | GJ2028 012 |
| 80TE | GJ2028 016 |

## 24.4 CABLES AND CONNECTORS

This section describes the type of wiring and connections that should be used when installing the device. For pin-out details please refer to the Hardware Design chapter or the wiring diagrams.

**Caution:**
**Before carrying out any work on the equipment you should be familiar with the Safety Section and the ratings on the equipment's rating label.**

### 24.4.1 TERMINAL BLOCKS

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

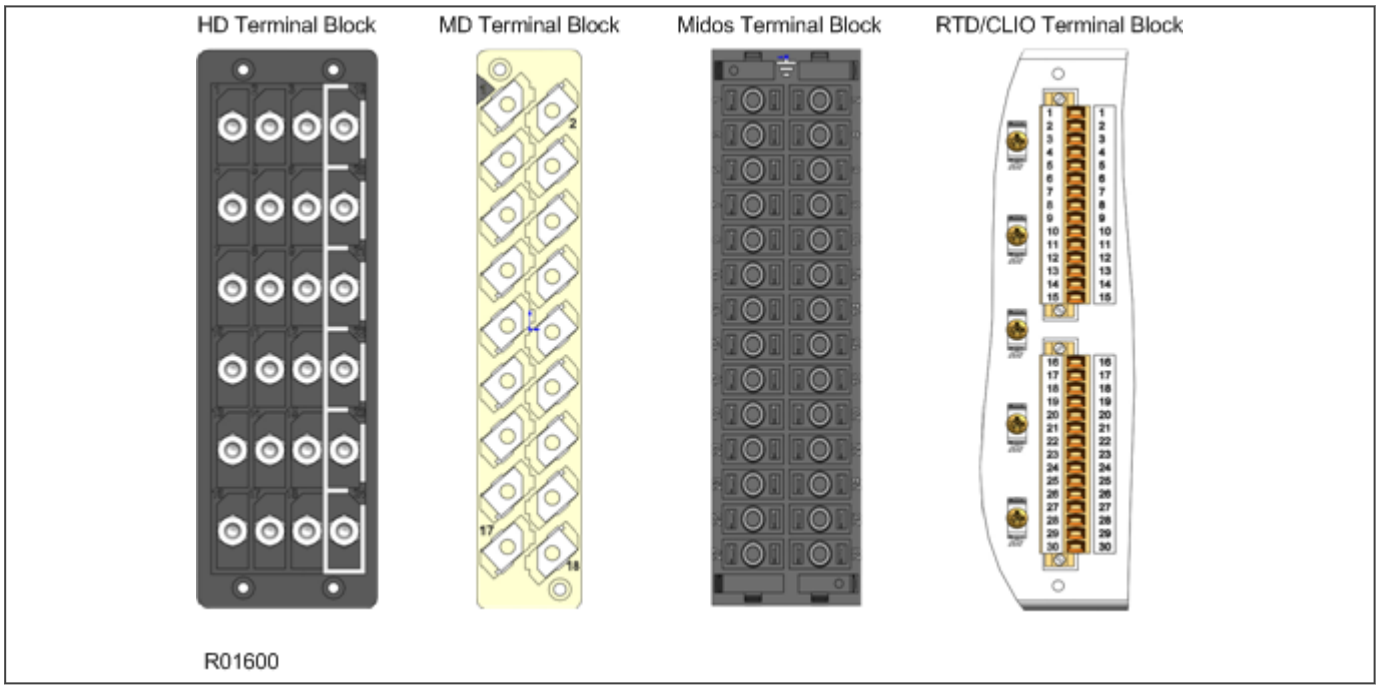


**Figure 291: Terminal block types**

MiCOM products are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per terminal.

If required, M4 90° crimp ring terminals can be supplied in three different sizes depending on wire size. Each type is available in bags of 100.

| Part number | Wire size | Insulation color |
|---|---|---|
| ZB9124 901 | 0.25 - 1.65 $mm^2$ (22 – 16 AWG) | Red |
| ZB9124 900 | 1.04 - 2.63 $mm^2$ (16 – 14 AWG) | Blue |

*Note:*
*IP2x shields and side cover panels may be fitted to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers can be attached during installation or retrofitted to upgrade existing installations. The shields are supplied with four language fitting instructions, publication number: IP2x-TM-4L-n (where n is the current issue number). For more information, contact your local sales office or our worldwide Contact Centre.*

## 24.4.2 POWER SUPPLY CONNECTIONS

These should be wired with 1.5 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

**Caution:**
**Protect the auxiliary power supply wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.**

## 24.4.3 EARTH CONNNECTION

Every device must be connected to the cubicle earthing bar using the M4 earth terminal.

Use a wire size of at least 2.5 $mm^2$ terminated with a ring terminal.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 $mm^2$ using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 $mm^2$ per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

*Note:*
*To prevent any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the product, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the product case, or using tinned ring terminals.*

## 24.4.4 CURRENT TRANSFORMERS

Current transformers would generally be wired with 2.5 $mm^2$ PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 $mm^2$ using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 $mm^2$ per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

**Caution:**
**Current transformer circuits must never be fused.**

*Note:*
*If there are CTs present, spring-loaded shorting contacts ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken.*

*Note:*
*For 5A CT secondaries, we recommend using 2 x 2.5 $mm^2$ PVC insulated multi-stranded copper wire.*

### 24.4.5 VOLTAGE TRANSFORMER CONNECTIONS

Voltage transformers should be wired with 2.5 $mm^2$ PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

### 24.4.6 WATCHDOG CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

### 24.4.7 EIA(RS)485 AND K-BUS CONNECTIONS

For connecting the EIA(RS485) / K-Bus ports, use 2-core screened cable with a maximum total length of 1000 m or 200 nF total cable capacitance.

To guarantee the performance specifications, you must ensure continuity of the screen, when daisy chaining the connections.

Two-core screened twisted pair cable should be used. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The K-Bus signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

A typical cable specification would be:

- Each core: 16/0.2 $mm^2$ copper conductors, PVC insulated
- Nominal conductor area: 0.5 $mm^2$ per core
- Screen: Overall braid, PVC sheathed

### 24.4.8 IRIG-B CONNECTION

The IRIG-B input and BNC connector have a characteristic impedance of 50 ohms. We recommend that connections between the IRIG-B equipment and the product are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

### 24.4.9 OPTO-INPUT CONNECTIONS

These should be wired with 1 $mm^2$ PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Each opto-input has a selectable preset ½ cycle filter. This makes the input immune to noise induced on the wiring. This can, however slow down the response. If you need to switch off the ½ cycle filter, either use double pole switching on the input, or screened twisted cable on the input circuit.

**Caution:**
**Protect the opto-inputs and their wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.**

## 24.4.10 OUTPUT RELAY CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

## 24.4.11 ETHERNET METALLIC CONNECTIONS

If the device has a metallic Ethernet connection, it can be connected to a 100Base-TX Ethernet hub. Due to noise sensitivity, we recommend this type of connection only for short distance connections, ideally where the products and hubs are in the same cubicle. For increased noise immunity, CAT 6 (category 6) STP (shielded twisted pair) cable and connectors can be used.

The connector for the Ethernet port is a shielded RJ-45. The pin-out is as follows:

| Pin | Signal name | Signal definition |
|---|---|---|
| 1 | TXP | Transmit (positive) |
| 2 | TXN | Transmit (negative) |
| 3 | RXP | Receive (positive) |
| 4 | - | Not used |
| 5 | - | Not used |
| 6 | RXN | Receive (negative) |
| 7 | - | Not used |
| 8 | - | Not used |

## 24.4.12 ETHERNET FIBRE CONNECTIONS

We recommend the use of fibre-optic connections for permanent connections in a substation environment. The 100 Mbps fibre optic port uses type ST or LC connectors depending on the order option (one for Tx and one for Rx), compatible with 50/125 µm or 62.5/125 µm multimode fibres at 1300 nm wavelength.

*Note:*
*For models equipped with redundant Ethernet connections the product must be partially dismantled to set the fourth octet of the second IP address. This ideally, should be done before installation.*

## 24.4.13 USB CONNECTION

The IED has a type B USB socket inside the bottom compartment. A standard USB printer cable (type A one end, type B the other end) can be used to connect a local PC to the IED. This cable is the same as that used for connecting a printer to a PC.

## 24.4.14 GPS FIBRE CONNECTION

Some products use a GPS 1 PPS timing signal. If applicable, this is connected to a fibre-optic port on the coprocessor board in slot B. The fibre-optic port uses an ST type connector, compatible with fibre multimode 50/125 µm or 62.5/125 µm – 850 nm.

### 24.4.15 FIBRE COMMUNICATION CONNECTIONS

The fibre optic port consists of one or two channels using ST type connectors (one for Tx and one for Rx). The type of fibre used depends on the option selected.

850 nm and 1300 nm multimode systems use 50/125 µm or 62.5/125 µm multimode fibres. 1300 nm and 1550 nm single mode systems use 9/125 µm single mode fibres.

## 24.5 CASE DIMENSIONS

Not all products are available in all case sizes.

### 24.5.1 CASE DIMENSIONS 40TE

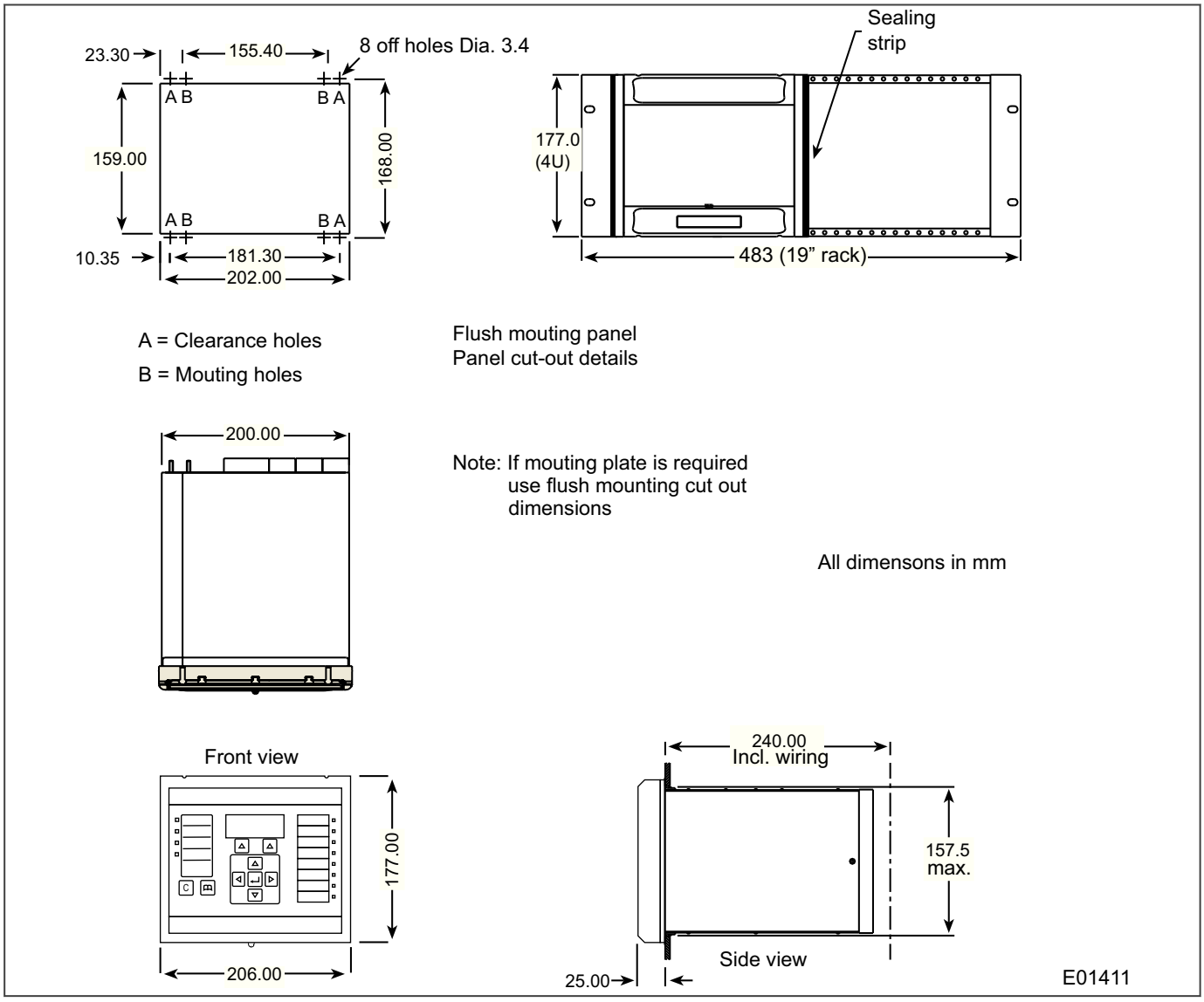


**Figure 292: 40TE case dimensions**

## 24.5.2 CASE DIMENSIONS 60TE

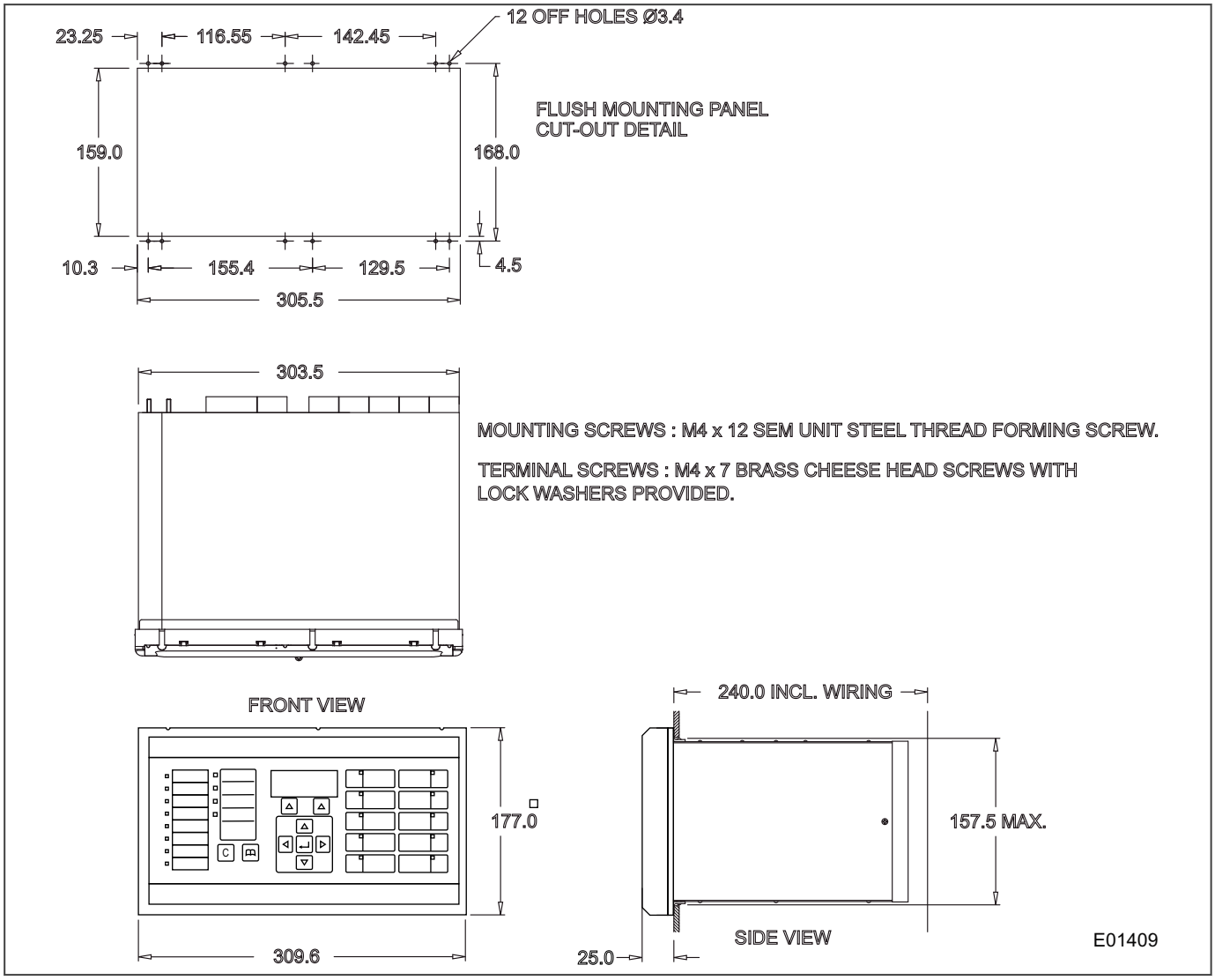


**Figure 293: 60TE case dimensions**

## 24.5.3 CASE DIMENSIONS 80TE

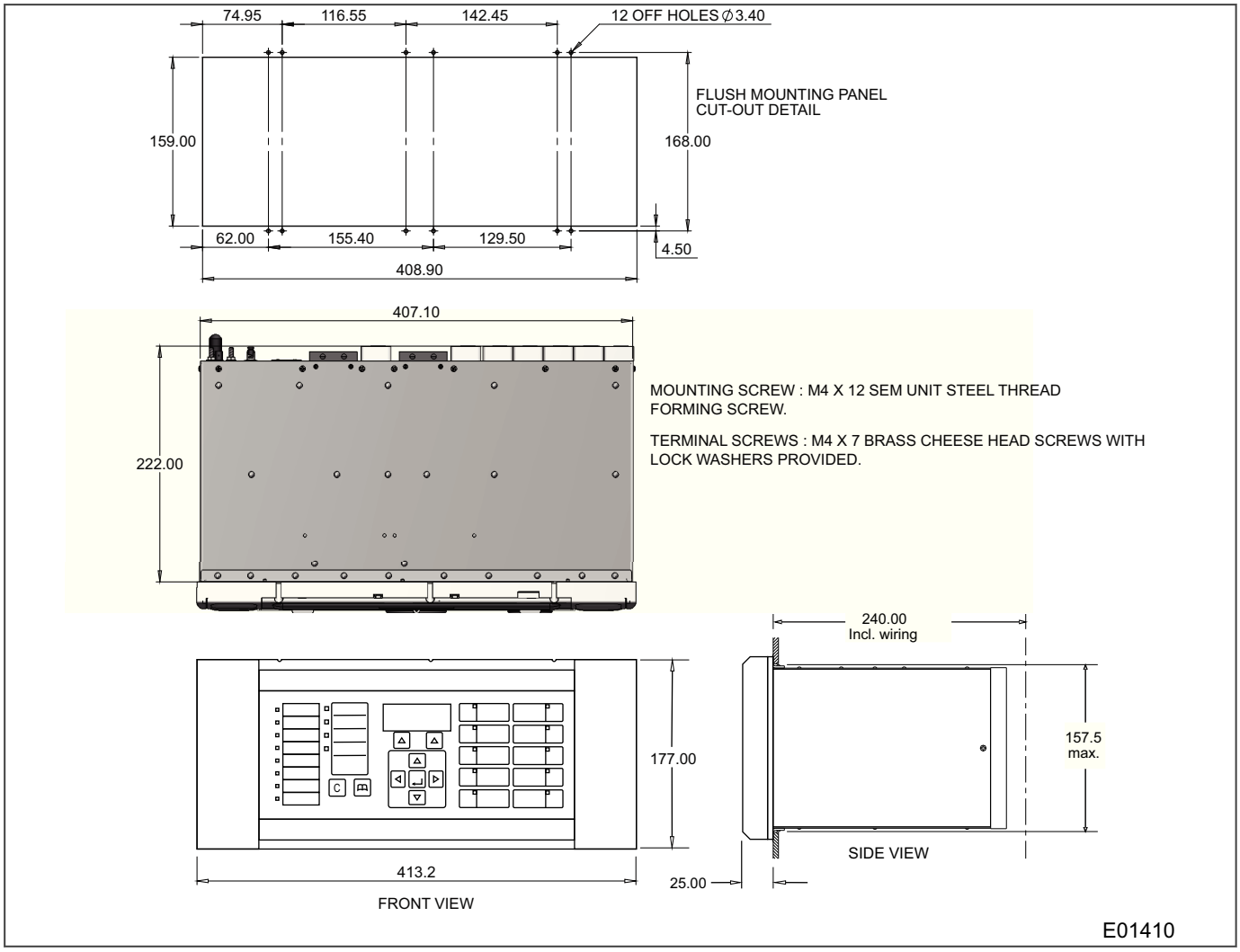


**Figure 294: 80TE case dimensions**

## CHAPTER 25

# COMMISSIONING INSTRUCTIONS

## 25.1 CHAPTER OVERVIEW

This chapter contains the following sections:

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General Guidelines 573
Commissioning Test Menu 574
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Product Checks 580
Electrical Intermicom Communication Loopback 589
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End-to-End Communication Tests 617
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## 25.2 GENERAL GUIDELINES

GE Vernova IEDs are self-checking devices and will raise an alarm in the unlikely event of a failure. This is why the commissioning tests are less extensive than those for non-numeric electronic devices or electro-mechanical relays.

To commission the devices, you (the commissioning engineer) do not need to test every function. You need only verify that the hardware is functioning correctly and that the application-specific software settings have been applied. You can check the settings by extracting them using the settings application software, or by means of the front panel interface (HMI panel).

The menu language is user-selectable, so you can change it for commissioning purposes if required.

*Note:*
*Remember to restore the language setting to the customer's preferred language on completion.*

**Caution:**
**Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM as well as the ratings on the equipment's rating label.**

**Warning:**
**With the exception of the CT shorting contacts check, do not disassemble the device during commissioning.**

## 25.3 COMMISSIONING TEST MENU

The IED provides several test facilities under the *COMMISSION TESTS* menu heading. There are menu cells that allow you to monitor the status of the opto-inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs. This section describes these commissioning test facilities.

### 25.3.1 OPTO I/P STATUS CELL (OPTO-INPUT STATUS)

This cell can be used to monitor the status of the opto-inputs while they are sequentially energised with a suitable DC voltage. The cell is a binary string that displays the status of the opto-inputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each logic input.

### 25.3.2 RELAY O/P STATUS CELL (RELAY OUTPUT STATUS)

This cell can be used to monitor the status of the relay outputs. The cell is a binary string that displays the status of the relay outputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each relay output.

The cell indicates the status of the output relays when the IED is in service. You can check for relay damage by comparing the status of the output contacts with their associated bits.

*Note:*
*When the **Test Mode** cell is set to `Contacts Blocked`, the relay output status indicates which contacts would operate if the IED was in-service. It does not show the actual status of the output relays, as they are blocked.*

### 25.3.3 TEST PORT STATUS CELL

This cell displays the status of the DDB signals that have been allocated in the ***Monitor Bit*** cells. If you move the cursor along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the IED. This allows you to test the Programmable Scheme Logic (PSL).

### 25.3.4 MONITOR BIT 1 TO 8 CELLS

The eight Monitor Bit cells allows you to select eight DDB signals that can be observed in the Test Port Status cell or downloaded via the front port.

Each Monitor Bit cell can be assigned to a particular DDB signal. You set it by entering the required DDB signal number from the list of available DDB signals.

The pins of the monitor/download port used for monitor bits are as follows:

| Monitor Bit | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| Monitor/Download Port Pin | 11 | 12 | 15 | 13 | 20 | 21 | 23 | 24 |

The signal ground is available on pins 18, 19, 22 and 25.

**Caution:**
**The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.**

### 25.3.5 TEST MODE CELL

This cell allows you to perform secondary injection testing. It also lets you test the output contacts directly by applying menu-controlled test signals.

To go into test mode, select the `Test Mode` option in the ***Test Mode*** cell. This takes the IED out of service causing an alarm condition to be recorded and the ***Out of Service*** LED to illuminate. This also freezes any information stored in the *CB CONDITION* column. In IEC 60870-5-103 versions, it changes the Cause of Transmission (COT) to Test Mode.

In Test Mode, the output contacts are still active. To disable the output contacts you must select the `Contacts Blocked` option.

Once testing is complete, return the device back into service by setting the ***Test Mode*** Cell back to `Disabled`.

**Caution:**
**When the cell is in Test Mode, the Scheme Logic still drives the output relays, which could result in tripping of circuit breakers. To avoid this, set the *Test Mode* cell to `Contacts Blocked`.**

*Note:*
`Test mode` *and* `Contacts Blocked` *mode can also be selected by energising an opto-input mapped to the Test Mode signal, and the Contact Block signal respectively.*

### 25.3.6 TEST PATTERN CELL

The ***Test Pattern*** cell is used to select the output relay contacts to be tested when the ***Contact Test*** cell is set to `Apply Test`. The cell has a binary string with one bit for each user-configurable output contact, which can be set to '1' to operate the output and '0' to not operate it.

### 25.3.7 CONTACT TEST CELL

When the `Apply Test` command in this cell is issued, the contacts set for operation change state. Once the test has been applied, the command text on the LCD will change to ***No Operation*** and the contacts will remain in the Test state until reset by issuing the `Remove Test` command. The command text on the LCD will show ***No Operation*** after the `Remove Test` command has been issued.

*Note:*
*When the **Test Mode** cell is set to* `Contacts Blocked` *the **Relay O/P Status** cell does not show the current status of the output relays and therefore cannot be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.*

### 25.3.8 TEST LEDS CELL

When the `Apply Test` command in this cell is issued, the user-programmable LEDs illuminate for approximately 2 seconds before switching off, and the command text on the LCD reverts to ***No Operation***.

### 25.3.9 TEST AUTORECLOSE CELL

Where the IED provides an auto-reclose function, this cell will be available for testing the sequence of circuit breaker trip and auto-reclose cycles.

The `Trip 3 Pole` option in the ***Test Autoreclose*** cell causes the device to perform the first three phase trip/ reclose cycle so that associated output contacts can be checked for operation at the correct times during the cycle.

Once the trip output has operated the command text will revert to *No Operation* whilst the rest of the auto-reclose cycle is performed. To test subsequent three-phase autoreclose cycles, you repeat the *Trip 3 Pole* command. You can also test the single phases with *Trip Pole A*, *Trip Pole B* and *Trip Pole C*.

*Note:*
*The default settings for the programmable scheme logic has the AR Trip Test signals mapped to the Trip Input signals. If the programmable scheme logic has been changed, it is essential that these signals retain this mapping for the Test Autoreclose facility to work.*

### 25.3.10 STATIC TEST MODE

Static Test Mode can be set to *Enabled* or *Disabled*. When the Static Test mode is enabled it allows injection test that don't support dynamic switching to be used to commission and test the device.

Dynamic secondary injection test sets are able to accurately mimic real power system faults. The test sets mimic an instantaneous fault “shot”, with the real rate of rise of current, and the decaying DC exponential component. Dynamic injection test sets are available, which cater for all three phases, providing a six signal set of analogue inputs: Va, Vb, Vc, Ia, Ib, Ic. Such injection test sets can be used with the device, with no special testing limitations.

Static test sets, also known as Static Simulators, may not properly provide or simulate:

- A healthy pre-fault voltage
- A real fault shot (instead a gradually varying current or voltage would be used)
- The rate of rise of current and DC components
- A complete set of three-phase analogue inputs
- Real dynamic step changes in current and voltage.

Some of the protection in this product is based on delta techniques which recognise step changes in actual power system quantities. Because these may not be produced by static test sets,, certain functions are can be disabled or bypassed to allow injection testing with static test sets. Enabling the ***Static Test Mode*** option does this..

For the tests, the delta directional line is replaced by a conventional distance directional line. Extra filtering of distance comparators is used so the filtering slows to use a fixed one cycle window. Memory polarising is replaced by cross-polarising from unfaulted phases.

*Note:*
*Trip times may be up to ½ cycle longer when tested in the static mode, due to the nature of the test voltage and current, and the slower filtering. This is normal, and perfectly acceptable.*

### 25.3.11 LOOPBACK MODE

Loopback Mode can be used to test InterMiCOM$^{64}$ signalling.

*Note:*
*If the cell is set to Internal, only the IED software is checked. If the cell is set to External, both the software and hardware are checked.*

When the device is switched into Loopback Mode, it automatically uses generic addresses 0-0. It responds as if it is connected to a remote device. The sent and received IM$^{64}$ signals continue to be routed to and from the signals defined in the programmable logic.

*Note:*
*Loopback mode can also be selected by energising an opto-input mapped to the Loopback signal.*

### 25.3.12 IM64 TEST PATTERN

This cell is used with the ***IM64 Test Mode*** cell to set a 16-bit pattern (8 bits per channel), which is transmitted whenever the ***IM64 Test Mode*** cell is set to `Enabled`. The ***IM64 TestPattern*** cell has a binary string with one bit for each user-defined Inter-MiCOM command. These can be set to '1' to operate the IM64 output under test conditions and '0' for no operation.

### 25.3.13 IM64 TEST PATTERN CH1 & CH2

***IM64 TestPattern CH1*** and ***IM64 TestPattern CH2*** are used with the ***IM64 Test Mode*** cell to set a 48-bit pattern (24 bits per channel), which is transmitted whenever the ***IM64 Test Mode*** cell is `Enabled` and the ***Extended IM64*** mode is also `Enabled`. The ***IM64 TestPattern CH1*** and ***IM64 TestPattern CH2*** cells have a binary string with one bit for each user-defined Inter-MiCOM command. These can be set to '1' to operate the IM64 output under test conditions and '0' for no operation.

### 25.3.14 IM64 TEST MODE

When the `Enable` command in this cell is issued, the InterMiCOM$^{64}$ commands change to reflect the state of the values set in the ***IM64 TestPattern*** cell. If the cell is set to Disabled, the InterMiCOM$^{64}$ commands reflect the state of the signals generated by the protection and control functions.

When the ***Extended IM64*** mode is `Enabled`, two test pattern cells are used, ***IM64 TestPattern CH1*** and ***IM64 TestPattern CH2***.

### 25.3.15 RED AND GREEN LED STATUS CELLS

These cells contain binary strings that indicate which of the user-programmable red and green LEDs are illuminated when accessing from a remote location. A '1' indicates that a particular LED is illuminated.

> *Note:*
> *When the status in both **Red LED Status** and **Green LED Status** cells is '1', this indicates the LEDs illumination is yellow.*

## 25.4 COMMISSIONING EQUIPMENT

Specialist test equipment is required to commission this product. We recognise three classes of equipment for commissioning :

- Recommended
- Essential
- Advisory

Recommended equipment constitutes equipment that is both necessary, and sufficient, to verify correct performance of the principal protection functions.

Essential equipment represents the minimum necessary to check that the product includes the basic expected protection functions and that they operate within limits.

Advisory equipment represents equipment that is needed to verify satisfactory operation of features that may be unused, or supplementary, or which may, for example, be integral to a distributed control/automation scheme. Operation of such features may, perhaps, be more appropriately verified as part of a customer defined commissioning requirement, or as part of a system-level commissioning regime.

### 25.4.1 RECOMMENDED COMMISSIONING EQUIPMENT

The minimum recommended equipment is a multifunctional three-phase AC current and voltage injection test set featuring :

- Controlled three-phase AC current and voltage sources,
- Transient (dynamic) switching between pre-fault and post-fault conditions (to generate delta conditions),
- Dynamic impedance state sequencer (capable of sequencing through 4 impedance states),
- Integrated or separate variable DC supply (0 - 250 V)
- Integrated or separate AC and DC measurement capabilities (0-440V AC, 0-250V DC)
- Integrated and/or separate timer,
- Integrated and/or separate test switches.

In addition, you will need :

- A portable computer, installed with appropriate software to liaise with the equipment under test (EUT). Typically this software will be proprietary to the product's manufacturer (for example MiCOM S1 Agile).
- Suitable electrical test leads.
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- Continuity tester
- Verified application-specific settings files

For products that use fibre-optic communications to implement unit protection schemes :

- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm, OR single mode (according to the model variant) terminated with connectors as required by the product.
- Fibre-optic power meter
- P59x commissioning instructions

### 25.4.2 ESSENTIAL COMMISSIONING EQUIPMENT

As an absolute minimum, the following equipment is required:

- AC current source coupled with AC voltage source
- Variable DC supply (0 - 250V)

- Multimeter capable of measuring AC and DC current and voltage (0-440V AC, 0-250V DC)
- Timer
- Test switches
- Suitable electrical test leads
- Continuity tester

For products that use fibre-optic communications to implement unit protection schemes :

- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm, OR single mode (according to the model variant) terminated with connectors as required by the product.
- Fibre-optic power meter

*Note:*
*If the AC test source that you are using is not capable of dynamic fault simulation (cannot dynamically switch from load to fault conditions) you must use the product's static test mode feature*

*Note:*
*To do this, in COMMISSION TESTS, set* ***Static Test Mode*** *to* `Enabled`.

### 25.4.3 ADVISORY TEST EQUIPMENT

Advisory test equipment may be required for extended commissioning procedures:

- Current clamp meter
- Multi-finger test plug:
  - P992 for test block type P991
  - MMLB for test block type MMLG blocks
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- KITZ K-Bus - EIA(RS)232 protocol converter for testing EIA(RS)485 K-Bus port
- EIA(RS)485 to EIA(RS)232 converter for testing EIA(RS)485 Courier/MODBUS/IEC60870-5-103/DNP3 port
- A portable printer (for printing a setting record from the portable PC) and or writeable, detachable memory device
- Phase angle meter
- Phase rotation meter
- Fibre-optic power meter
- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm terminated with BFOC (ST) 2.5 or BFOC (LC) connectors depending on the Ethernet board ordered for testing the fibre-optic RP1 port.

## 25.5 PRODUCT CHECKS

These product checks are designed to ensure that the device has not been physically damaged prior to commissioning, is functioning correctly and that all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the IED prior to commissioning, you should make a copy of the settings. This will allow you to restore them at a later date if necessary. This can be done by:

- Obtaining a setting file from the customer.
- Extracting the settings from the IED itself, using a portable PC with appropriate setting software.

If the customer has changed the password that prevents unauthorised changes to some of the settings, either the revised password should be provided, or the original password restored before testing.

*Note:*
*If the password has been lost, a recovery password can be obtained from GE Vernova.*

### 25.5.1 PRODUCT CHECKS WITH THE IED DE-ENERGISED

**Warning:**
**The following group of tests should be carried out without the auxiliary supply being applied to the IED and, if applicable, with the trip circuit isolated.**

The current and voltage transformer connections must be isolated from the IED for these checks. If a P991 test block is provided, the required isolation can be achieved by inserting test plug type P992. This open circuits all wiring routed through the test block.

Before inserting the test plug, you should check the scheme diagram to ensure that this will not cause damage or a safety hazard (the test block may, for example, be associated with protection current transformer circuits). The sockets in the test plug, which correspond to the current transformer secondary windings, must be linked before the test plug is inserted into the test block.

**Warning:**
**Never open-circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.**

If a test block is not provided, the voltage transformer supply to the IED should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the IED terminals. Where means of isolating the auxiliary supply and trip circuit (for example isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

#### 25.5.1.1 VISUAL INSPECTION

**Warning:**
**Check the rating information under the top access cover on the front of the IED.**

**Warning:**
**Check that the IED being tested is correct for the line or circuit.**

**Warning:**
**Record the circuit reference and system details.**

**Warning:**
**Check the CT secondary current rating and record the CT tap which is in use.**

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

#### 25.5.1.2 CURRENT TRANSFORMER SHORTING CONTACTS

Check the current transformer shorting contacts to ensure that they close when the heavy-duty terminal block is disconnected from the current input board.

The heavy-duty terminal blocks are fastened to the rear panel using four crosshead screws. These are located two at the top and two at the bottom.

*Note:*
*Use a magnetic bladed screwdriver to minimise the risk of the screws being left in the terminal block or lost.*

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed.

#### 25.5.1.3 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

#### 25.5.1.4 EXTERNAL WIRING

**Caution:**
**Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.**

#### 25.5.1.5 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

| Terminals | Contact State with Product De-energised |
|---|---|
| 11 - 12 on power supply board | Closed |
| 13 - 14 on power supply board | Open |

#### 25.5.1.6 POWER SUPPLY

Depending on its nominal supply rating, the IED can be operated from either a DC only or an AC/DC auxiliary supply. The incoming voltage must be within the operating range specified below.

Without energising the IED measure the auxiliary supply to ensure it is within the operating range.

| Nominal supply rating DC | Nominal Supply Rating AC RMS | DC Operating Range | AC Operating Range |
|---|---|---|---|
| 24 - 54 V | N/A | 19 to 65 V | N/A |
| 48 - 125 V | 30 - 100 V | 37 to 150 V | 24 - 110 V |
| 110 - 250 V | 100 - 240 V | 87 to 300 V | 80 to 265 V |

*Note:*
*The IED can withstand an AC ripple of up to 15% of the upper rated voltage on the DC auxiliary supply.*

**Warning:**
**Do not energise the IED or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.**

**Caution:**
**Energise the IED only if the auxiliary supply is within the specified operating ranges. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the IED.**

### 25.5.2 PXXX_CI_PRODUCTCHECKSENERGISED

**Warning:**
**The current and voltage transformer connections must remain isolated from the IED for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.**

The following group of tests verifies that the IED hardware and software is functioning correctly and should be carried out with the supply applied to the IED.

#### 25.5.2.1 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states when energised and healthy.

| Terminals | Contact State with Product Energised |
|---|---|
| 11 - 12 on power supply board | Open |
| 13 - 14 on power supply board | Closed |

### 25.5.2.2 TEST LCD

The Liquid Crystal Display (LCD) is designed to operate in a wide range of substation ambient temperatures. For this purpose, the IEDs have an ***LCD Contrast*** setting. The contrast is factory pre-set, but it may be necessary to adjust the contrast to give the best in-service display.

To change the contrast, you can increment or decrement the ***LCD Contrast*** cell in the *CONFIGURATION* column.

**Caution:**
**Before applying a contrast setting, make sure that it will not make the display so light or dark such that menu text becomes unreadable. It is possible to restore the visibility of a display by downloading a setting file, with the LCD Contrast set within the typical range of 7 - 11.**

### 25.5.2.3 DATE AND TIME

The date and time is stored in memory, which is backed up by a supercapacitor.

The method for setting the date and time depends on whether an IRIG-B signal is being used or not. The IRIG-B signal will override the time, day and month settings, but not the initial year setting. For this reason, you must ensure you set the correct year, even if the device is using IRIG-B to maintain the internal clock.

You set the Date and Time by one of the following methods:

- Using the front panel to set the ***Date and Time*** cells respectively
- By sending a courier command to the ***Date/Time*** cell (Courier reference 0801)

*Note:*
*If the auxiliary supply fails, the time and date will be maintained by the supercapacitor. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energised for approximately 30 seconds. On re energisation, the time should be correct.*

When using IRIG-B to maintain the clock, the IED must first be connected to the satellite clock equipment (usually an RT430), which should be energised and functioning.

1. Set the IRIG-B Sync cell in the *DATE AND TIME* column to `Enabled`.
2. Ensure the IED is receiving the IRIG-B signal by checking that cell IRIG-B Status reads `Active`.
3. Once the IRIG-B signal is active, adjust the time offset of the universal co coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.
4. Check that the time, date and month are correct in the Date/Time cell. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.
5. Reconnect the IRIG-B signal.

If the time and date is not being maintained by an IRIG-B signal, ensure that the IRIG-B Sync cell in the *DATE AND TIME* column is set to `Disabled`.

1. Set the date and time to the correct local time and date using Date/Time cell or using the serial protocol.

### 25.5.2.4 TEST LEDS

On power-up, all LEDs should first flash yellow. Following this, the green "Healthy" LED should illuminate indicating that the device is healthy.

The IED's non-volatile memory stores the states of the alarm, the trip, and the user-programmable LED indicators (if configured to latch). These indicators may also illuminate when the auxiliary supply is applied.

If any of these LEDs are ON then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes off), no testing is needed for that LED because it is obviously operational.

*Note:*
*In most cases, alarms related to the communications channels will not reset at this stage.*

### 25.5.2.5 TEST ALARM AND OUT-OF-SERVICE LEDS

The alarm and out of service LEDs can be tested using the *COMMISSION TESTS* menu column.

1. Set the ***Test Mode*** cell to `Contacts Blocked`.
2. Check that the out of service LED illuminates continuously and the alarm LED flashes.

It is not necessary to return the ***Test Mode*** cell to `Disabled` at this stage because the test mode will be required for later tests.

### 25.5.2.6 TEST TRIP LED

The trip LED can be tested by initiating a manual circuit breaker trip. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

### 25.5.2.7 TEST USER-PROGRAMMABLE LEDS

To test these LEDs, set the Test LEDs cell to `Apply Test`. Check that all user-programmable LEDs illuminate.

### 25.5.2.8 TEST OPTO-INPUTS

This test checks that all the opto-inputs on the IED are functioning correctly.

The opto-inputs should be energised one at a time. For terminal numbers, please see the external connection diagrams in the "Wiring Diagrams" chapter. Ensuring correct polarity, connect the supply voltage to the appropriate terminals for the input being tested.

The status of each opto-input can be viewed using either the ***Opto I/P Status*** cell in the *SYSTEM DATA* column, or the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column.

A '1' indicates an energised input and a '0' indicates a de-energised input. When each opto-input is energised, one of the characters on the bottom line of the display changes to indicate the new state of the input.

### 25.5.2.9 TEST OUTPUT RELAYS

This test checks that all the output relays are functioning correctly.

1. Ensure that the IED is still in test mode by viewing the ***Test Mode*** cell in the *COMMISSION TESTS* column. Ensure that it is set to `Contacts Blocked`.
2. The output relays should be energised one at a time. To select output relay 1 for testing, set the Test Pattern cell as appropriate.
3. Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagram.
4. To operate the output relay set the Contact Test cell to `Apply Test`.
5. Check the operation with the continuity tester.
6. Measure the resistance of the contacts in the closed state.
7. Reset the output relay by setting the Contact Test cell to `Remove Test`.
8. Repeat the test for the remaining output relays.
9. Return the IED to service by setting the Test Mode cell in the *COMMISSION TESTS* menu to `Disabled`.

### 25.5.2.10 TEST SERIAL COMMUNICATION PORT RP1

You need only perform this test if the IED is to be accessed from a remote location with a permanent serial connection to the communications port. The scope of this test does not extend to verifying operation with connected equipment beyond any supplied protocol converter. It verifies operation of the rear communication port (and if applicable the protocol converter) and varies according to the protocol fitted.

#### 25.5.2.10.1 CHECK PHYSICAL CONNECTIVITY

The rear communication port RP1 is presented on terminals 16, 17 and 18 of the power supply terminal block. Screened twisted pair cable is used to make a connection to the port. The cable screen should be connected to pin 16 and pins 17 and 18 are for the communication signal:

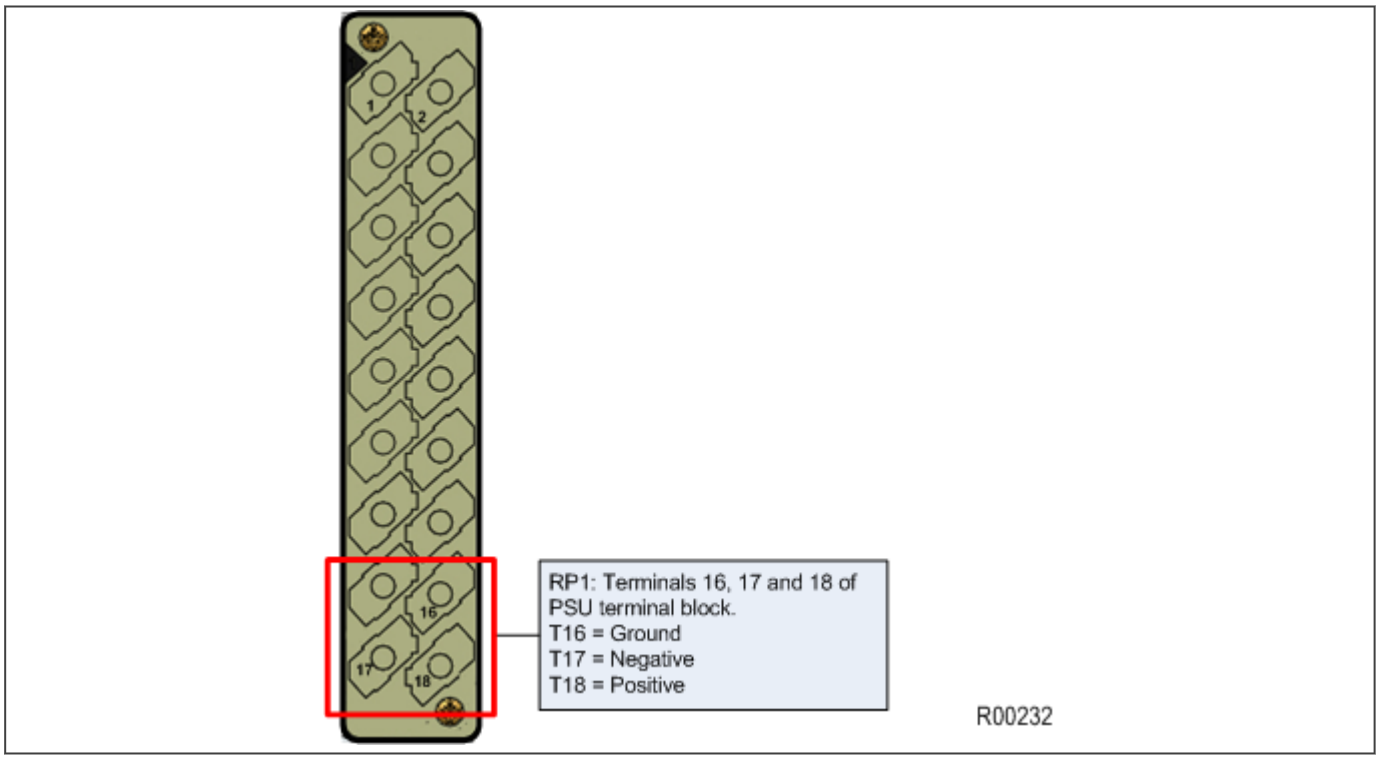



**Figure 295: RP1 physical connection**

For K-Bus applications, pins 17 and 18 are not polarity sensitive and it does not matter which way round the wires are connected. EIA(RS)485 is polarity sensitive, so you must ensure the wires are connected the correct way round (pin 18 is positive, pin 17 is negative).

If K-Bus is being used, a Kitz protocol converter (KITZ101, KITZ102 OR KITZ201) will have been installed to convert the K-Bus signals into RS232. Likewise, if RS485 is being used, an RS485-RS232 converter will have been installed. In the case where a protocol converter is being used, a laptop PC running appropriate software (such as MiCOM S1 Agile) can be connected to the incoming side of the protocol converter. An example for K-bus to RS232 conversion is shown below. RS485 to RS232 would follow the same principle, only using a RS485-RS232 converter. Most modern laptops have USB ports, so it is likely you will also require a RS232 to USB converter too.

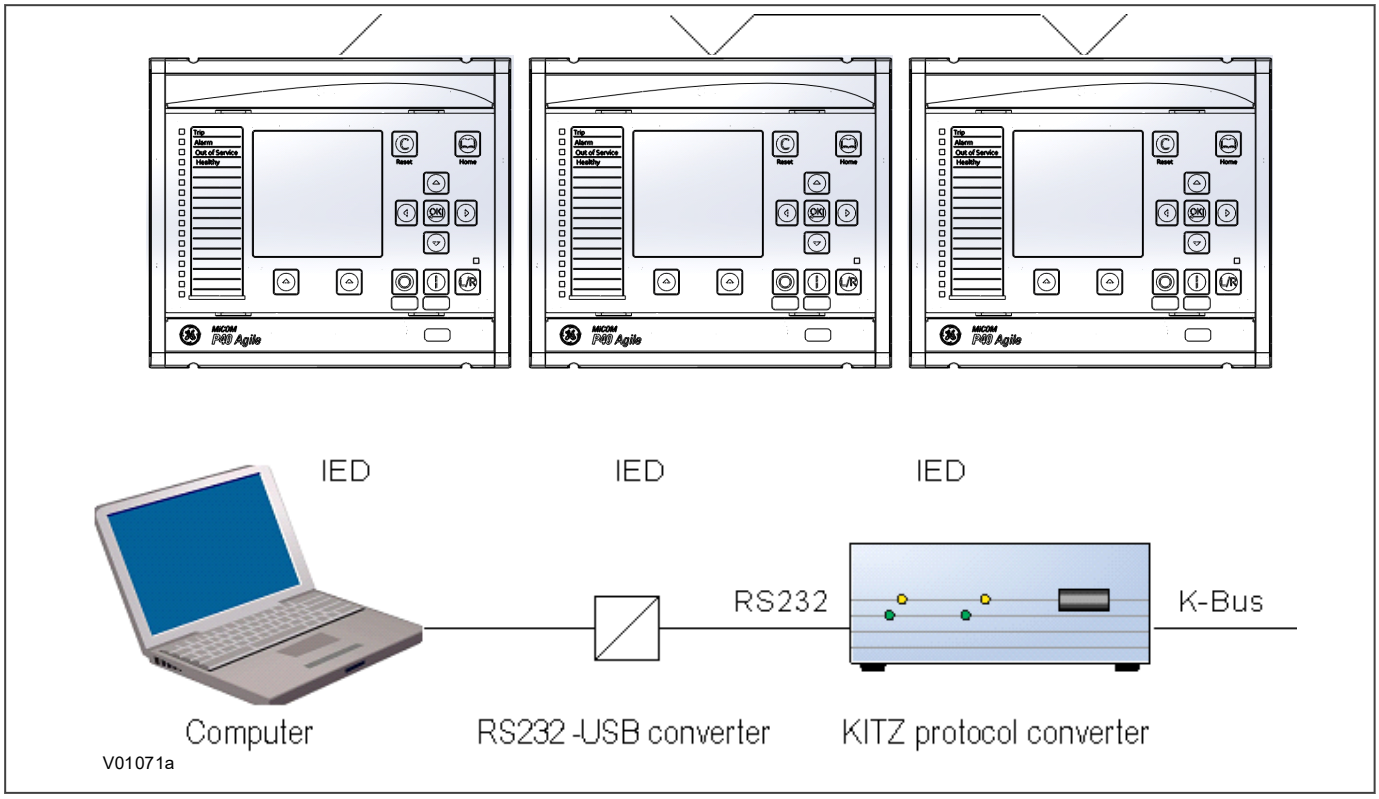



**Figure 296: Remote communication using K-bus**

### Fibre Connection

Some models have an optional fibre optic communications port fitted (on a separate communications board). The communications port to be used is selected by setting the Physical Link cell in the *COMMUNICATIONS* column, the values being `Copper` or `K-Bus` for the RS485/K-bus port and `Fibre Optic` for the fibre optic port.

#### 25.5.2.10.2 CHECK LOGICAL CONNECTIVITY

The logical connectivity depends on the chosen data protocol, but the principles of testing remain the same for all protocol variants:

1. Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter.
2. For Courier models, ensure that you have set the correct RP1 address
3. Check that communications can be established with this IED using the portable PC/Master Station.

### 25.5.2.11 TEST SERIAL COMMUNICATION PORT RP2

RP2 is an optional second serial port board providing additional serial connectivity. It provides two 9-pin D-type serial port connectors SK4 and SK5. Both ports are configured as DTE (Date Terminal Equipment) ports. That means they can be connected to communications equipment such as a modem with a straight-through cable.

SK4 can be configured as an EIA(RS232), EIA(RS485), or K-Bus connection for Courier protocol only, whilst SK5 is fixed to EIA(RS)232 for InterMiCOM signalling only.

It is not the intention of this test to verify the operation of the complete communication link between the IED and the remote location, just the IED's rear communication port and, if applicable, the protocol converter.

The only checks that need to be made are as follows:

1. Set the ***RP2 Port Config*** cell in the *COMMUNICATIONS* column to the required physical protocol; (K-Bus, EIA(RS)485, or EIA(RS)232.
2. Set the IED's Courier address to the correct value (it must be between 1 and 254).

#### 25.5.2.12 TEST ETHERNET COMMUNICATION

For products that employ Ethernet communications, we recommend that testing be limited to a visual check that the correct ports are fitted and that there is no sign of physical damage.

If there is no board fitted or the board is faulty, a NIC link alarm will be raised (providing this option has been set in the ***NIC Link Report*** cell in the *COMMUNICATIONS* column).

### 25.5.3 SECONDARY INJECTION TESTS

Secondary injection testing is carried out to verify the integrity of the VT and CT readings. All devices leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, you must set this in the Frequency cell in the *SYSTEM DATA* column.

The PMU must be installed and connected to a 1pps fibre optic synchronising signal and a demodulated IRIG-B signal, provided by a device such as a REASON RT430.

Connect the current and voltage outputs of the test set to the appropriate terminals of the first voltage and current channel and apply nominal voltage and current with the current lagging the voltage by 90 degrees.

#### 25.5.3.1 TEST CURRENT INPUTS

This test verifies that the current measurement inputs are configured correctly.

1. Using secondary injection test equipment such as an Omicron, apply and measure nominal rated current to each CT in turn.
2. Check its magnitude using a multi-meter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the displayed value. The measured current values will either be in primary or secondary Amperes. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied current.

> *Note:*
> *If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

### 25.5.3.2 TEST VOLTAGE INPUTS

This test verifies that the voltage measurement inputs are configured correctly.

1. Using secondary injection test equipment, apply and measure the rated voltage to each voltage transformer input in turn.
2. Check its magnitude using a multimeter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the value displayed. The measured voltage values will either be in primary or secondary Volts. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied voltage.

*Note:*
*If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

## 25.6 ELECTRICAL INTERMICOM COMMUNICATION LOOPBACK

If the IED is used in a scheme with standard InterMiCOM communication (Electrical Teleprotection), you need to configure a loopback for testing purposes.

### 25.6.1 SETTING UP THE LOOPBACK

The communication path may include various connectors and signal converters before leaving the substation. We therefore advise making the loopback as close as possible to where the communication link leaves the substation. This way, as much of the wiring as possible and all associated communication signal converters are included in the test.

1. Set *CONFIGURATION* > ***InterMiCOM*** to `Enabled`.
2. Set *INTERMICOM COMMS* > ***Ch Statistics*** and ***Ch Diagnostics*** to `Visible`.
3. Check that *INTERMICOM COMMS* > ***IM H/W Status*** displays OK. This means the InterMiCOM hardware is fitted and initialised.

### 25.6.2 LOOPBACK TEST

*INTERMICOM COMMS* > ***Loopback Mode*** allows you to test the InterMiCOM channel. In normal service it must be disabled. *INTERMICOM COMMS* > ***Loopback Status*** shows the status of the InterMiCOM loopback mode.

*Note:*
*If INTERMICOM COMMS* > ***Loopback Mode*** *is set to* `Internal`*, only the internal software of the device is checked. This is useful for testing functionality if no communications connections are made. Use the 'External' setting during commissioning because it checks both the software and hardware. When the IED is switched into either Internal or External Loopback Mode it automatically inhibits InterMiCOM messages to the PSL by setting all eight InterMiCOM message command states to zero.*

Set *INTERMICOM COMMS* > ***Loopback Mode*** to `External` and form a communications loopback by connecting the transmit signal (pin 2) to the receive signal (pin 3).

*Note:*
*The DCD signal must be held high (by connecting pin 1 to pin 4) if the connected equipment does not support DCD.*

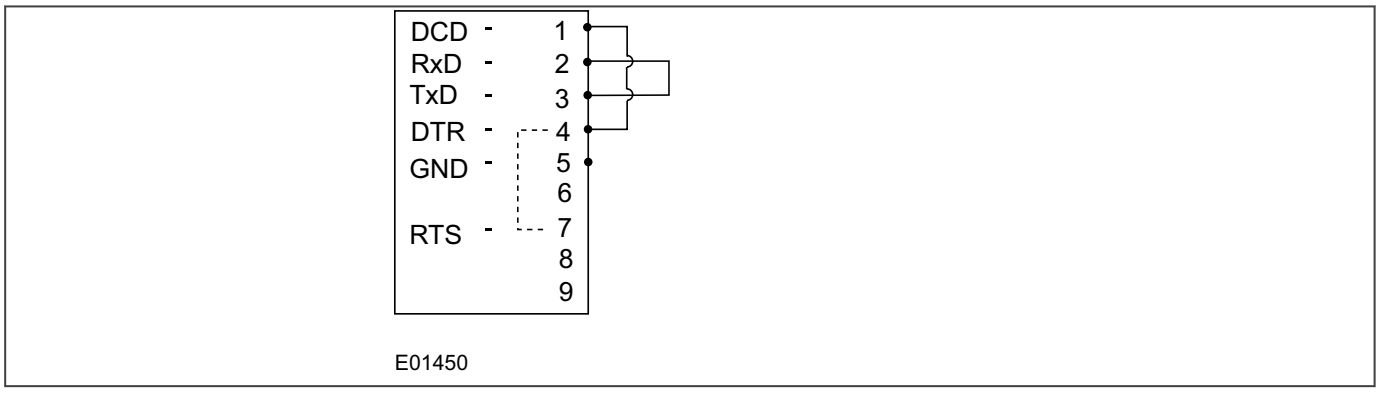



**Figure 297: InterMicom loopback testing**

The loopback mode is shown on the front panel by an Alarm LED and the message IM Loopback on the LCD.

Check that all connections are correct and the software is working correctly.

Check that *INTERMICOM COMMS* > ***Loopback Status*** shows OK.

#### 25.6.2.1 INTERMICOM COMMAND BITS

To test the InterMiCOM command bits, go to the *INTERMICOM COMMS* column and do the following:

1. Enter any test pattern in the ***Test Pattern*** cell in the by scrolling through and changing selected bits between 1 and 0. The entered pattern is transmitted through the loopback.
2. Check that the ***IM Output Status*** cell matches the applied Test Pattern.
3. Check that all 8 bits in the ***IM Input Status*** cell are zero.

#### 25.6.2.2 INTERMICOM CHANNEL DIAGNOSTICS

Check that the following cells in the *INTERMICOM COMMS* column all read **OK**.

- ***Data CD Status***
- ***FrameSync Status***
- ***Message Status***
- ***Channel Status***

#### 25.6.2.3 SIMULATING A CHANNEL FAILURE

1. Simulate a failure of the communications link by breaking a connection and checking that some of these cells show **Fail**.
2. Restore the communications loopback and ensure that the four diagnostic cells display **OK.**

*Note:*
*Some or all of these cells show **Fail** depending on the communications configuration and the way the link has failed.*

## 25.7 INTERMICOM 64 COMMUNICATION

If the IED is used in a scheme with InterMiCOM$^{64}$ communication, you need to configure a loopback for testing purposes.

IM64 is fibre-based. Several different fibre-optic interfaces are available. In general, 1300 nm fibres are used for direct connection (these may be single mode or multimode). 850 nm multimode fibres are generally used with multiplexing telecommunications equipment.

*Note:*
*It is important that fibres used for testing are correct for the specified interface(s).*

Optical fibres should be terminated with BFOC2.5 (ST2.5) connectors. For multimode applications use 50/125 µm core fibre. Make sure fibre test leads used for measurements are long enough for mode stripping (a method of reducing loss within the core). We recommend a minimum length of 10 m (30ft) for this.

If IEDs communicate using IEEE C37.94 compliant multiplexed electrical communication channels, a P590 is used. This is a bidirectional optical-to-electrical signal converter. It is situated near the multiplexer, between the fibre from the IED and the electrical interface of the multiplexer. Apply the loopback either at the P590 or the multiplexer to ensure as much of the circuit as possible is tested. If the IED is connected to a multiplexer, the loopback testing is exactly the same whether connected directly or via a multiplexer. The P590 interface units require additional tests (see P590 documentation).

To enable IM64, set the ***InterMiCOM64*** cell in the *CONFIGURATION* column to `Enable`.

**Warning:**
**NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.**

### 25.7.1 CHECKING THE INTERFACE

Before carrying out the loopback test, you need to check that the interface is transmitting a suitable signal. To check this ...

1. Set *COMMISSION TESTS*> ***Loopback Mode*** to `External`.
2. Using an appropriate fibre-optic cable, connect the Channel 1 transmitter (TX1) to an optical power meter. Check that the average power transmitted is within the range given in the following table.
3. Record the transmit power level.
4. Repeat for Channel 2 if applicable.
5. Measure the received power strength at remote ends.

| Power | 850 nm Multi-Mode | 1300 nm Multi-Mode | 1300/1550 nm Single-Mode |
|---|---|---|---|
| Minimum transmitter power (average value) | -19.8 dBm | -6 dBm | -6 dBm |
| Receiver sensitivity (average power) | -25.4 dBm | -49 dBm | -49 dBm |

*Note:*
*If CONFIGURATION >* ***InterMiCOM64*** *is set to* `Enable`*, the signals normally sent and received by and from the communications interface are routed to and from the signals defined in the Programmable Scheme Logic. If, however, COMMISSION TESTS >* ***IM64 Test Mode*** *is set to* `Enabled`*, an IM64 test pattern is transmitted instead.*

### 25.7.2 SETTING UP THE LOOPBACK

Set up a communications loopback for each of the two channels.

Where direct fibre connections are used (or where multiplexer channels conforming to the IEEE C37.94 standard are used), connect an appropriate fibre-optic cable from the channel transmitter to the channel receiver port on the rear of the device.

If the communications use P59x interface devices, connect the appropriate optical fibre(s) between the channel transmitter(s) on the IED used to make connection to the P59x optical receiver(s). Then commission the relevant P59x devices.

### 25.7.3 LOOPBACK TEST

1. Set *COMMISSION TESTS* > ***IM64 Test Mode*** to `Enabled`, and use *COMMISSION TESTS* > ***Test Pattern*** to set a bit pattern sent using the InterMiCOM$^{64}$ loopback.
2. Check that *MEASUREMENTS 4* > ***IM64 Rx Status*** matches the test pattern set. The communication statistics show the number of valid and erroneous messages received.

*Note:*
*The propagation delay measurement is not valid in this mode of operation. The IED responds as if it is connected to a remote IED. It indicates a loopback alarm which can only be cleared by setting COMMISSION TESTS >* ***Loopback Mode*** *to* `Disabled`*.*

*Note:*
*In loopback mode the signals sent and received through the protection communications interface continue to be routed to and from the signals defined in the programmable logic.*

*Note:*
*A test pattern can also be sent to the remote end to test the whole InterMiCOM communication path. To do this, set COMMISSION TESTS >****IM64 Test Mode*** *to* `Enable` *and connect two ends. Take special care because the test pattern is executed using PSL at the remote end.*

## 25.8 SETTING CHECKS

The setting checks ensure that all of the application-specific settings (both the IED's function and Programmable Scheme Logic settings) have been correctly applied.

> *Note:*
> *If applicable, the trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.*

### 25.8.1 APPLY APPLICATION-SPECIFIC SETTINGS

There are two different methods of applying the settings to the IED

- Transferring settings to the IED from a pre-prepared setting file using MiCOM S1 Agile
- Enter the settings manually using the IED's front panel HMI

#### 25.8.1.1 TRANSFERRING SETTINGS FROM A SETTINGS FILE

This is the preferred method for transferring function settings. It is much faster and there is a lower margin for error.

1. Connect a PC running the Settings Application Software to the IED's front port, or a rear Ethernet port. Alternatively connect to the rear Courier communications port, using a KITZ protocol converter if necessary.
2. Power on the IED
3. Enter the IP address of the device if it is Ethernet enabled
4. Right-click the appropriate device name in the System Explorer pane and select **Send**
5. In the **Send to** dialog select the setting files and click **Send**

> *Note:*
> *The device name may not already exist in the system shown in **System Explorer**. In this case, perform a **Quick Connect** to the IED, then manually add the settings file to the device name in the system. Refer to the Settings Application Software help for details of how to do this.*

#### 25.8.1.2 ENTERING SETTINGS USING THE HMI

1. Starting at the default display, press the Down cursor key to show the first column heading.
2. Use the horizontal cursor keys to select the required column heading.
3. Use the vertical cursor keys to view the setting data in the column.
4. To return to the column header, either press the Up cursor key for a second or so, or press the **Cancel** key once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the Up cursor key or the Cancel key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
7. To change the setting value, press the vertical cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the left and right cursor keys.

8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the down cursor key. Before returning to the default display, the following prompt appears.

```
Update settings?
ENTER or CLEAR
```

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

*Note:*
*If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.*
*Control and support settings are updated immediately after they are entered, without the Update settings prompt.*
*It is not possible to change the PSL using the IED's front panel HMI.*

**Caution:**
**Where the installation needs application-specific PSL, the relevant .psl files, must be transferred to the IED, for each and every setting group that will be used. If you do not do this, the factory default PSL will still be resident. This may have severe operational and safety consequences.**

# 25.9 IEC 61850 EDITION 2 TESTING

## 25.9.1 USING IEC 61850 EDITION 2 TEST MODES

In a conventional substation, functionality typically resides in a single device. It is usually easy to physically isolate these functions, as the hardwired connects can simply be removed. Within a digital substation architecture however, functions may be distributed across many devices. This makes isolation of these functions difficult, because there are no physical wires that can be disconnected on a Ethernet network. Logical isolation of the various functions is therefore necessary.

With devices that support IEC 61850 Edition 2, it is possible to use a test mode to conduct online testing, which helps with the situation. The advantages of this are as follows:

- The device can be placed into a test mode, which can disable the relay outputs when testing the device with test input signals.
- Specific protection and control functions can be logically isolated.
- GOOSE messages can be tagged so that receiving devices can recognise they are test signals.
- An IED receiving simulated GOOSE or Sampled Value messages from test devices can differentiate these from normal process messages, and be configured to respond appropriately.

### 25.9.1.1 IED TEST MODE BEHAVIOUR

Test modes define how the device responds to test messages, and whether the relay outputs are activated or not. You can select the mode of operation by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column.
- Using an IEC 61850 control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the IED behaviour under the different modes:

| IED Test Mode Setting | Result |
|---|---|
| *Disabled* | • Normal IED behaviour |
| *Test* | • Protection remains enabled<br>• Output from the device is still active<br>• IEC 61850 message output has the 'quality' parameter set to 'test'<br>• The device only responds to IEC61850 MMS messages from the client with the 'test' flag set |
| *Contacts Blocked* | • Protection remains enabled<br>• Output from the device is disabled<br>• IEC 61850 message output has quality set to ‘test’<br>• The device only responds to IEC 61850 MMS messages from the client with the 'test' flag set |

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

### 25.9.1.2 SAMPLED VALUE TEST MODE BEHAVIOUR

The SV Test Mode defines how the device responds to test sampled value messages. You can select the mode of operation by using the front panel HMI, with the setting ***SV Test Mode*** under the *IEC 61850-9.2LE* column.

The following table summarises the behaviour for sampled values under the different modes:

| SV Test Mode Setting | Result |
|---|---|
| *Disabled* | • Normal IED behaviour<br>• All sampled value data frames received with an IEC 61850 Test quality bit set are treated as invalid<br>• The IED will display the measurement values for sampled values with the Simulated flag set but the protection elements within the IED will be blocked |
| *Enabled* | • All sampled value data frames received are treated as good, no matter if they have an IEC 61850-9-2 Simulated flag set or not |

## 25.9.2 SIMULATED INPUT BEHAVIOUR

Simulated GOOSE messages and sampled value streams can be used during testing.

The ***Subscriber Sim*** setting in the *COMMISSION TESTS* column controls whether a device listens to simulated signals or to real ones. An IEC 61850 control service to System/LPHD.Sim can also be used to change this value.

The device may be presented with both real signals and test signals. An internal state machine is used to control how the device switches between signals:

- The IED will continue subscribing to the 'real' GOOSE1 (in green) until it receives the first simulated GOOSE 1 (in red). This will initiate subscription changeover.
- After changeover to this new state, the IED will continue to subscribe to the simulated GOOSE 1 message (in red). Even if this simulated GOOSE 1 message disappears, the real GOOSE 1 message (in green) will still not be processed. This means all Virtual Inputs derived from the GOOSE 1 message will go to their default state.
- The only way to bring the IED out of this state is to set the ***Subscriber Sim*** setting back to False. The IED will then immediately stop processing the simulated messages and start processing real messages again.
- During above steps, IED1 will continuously process the real GOOSE 2 and GOOSE 3 messages as normal because it has not received any simulated messages for these that would initiate a changeover.

The process is represented in the following figure:

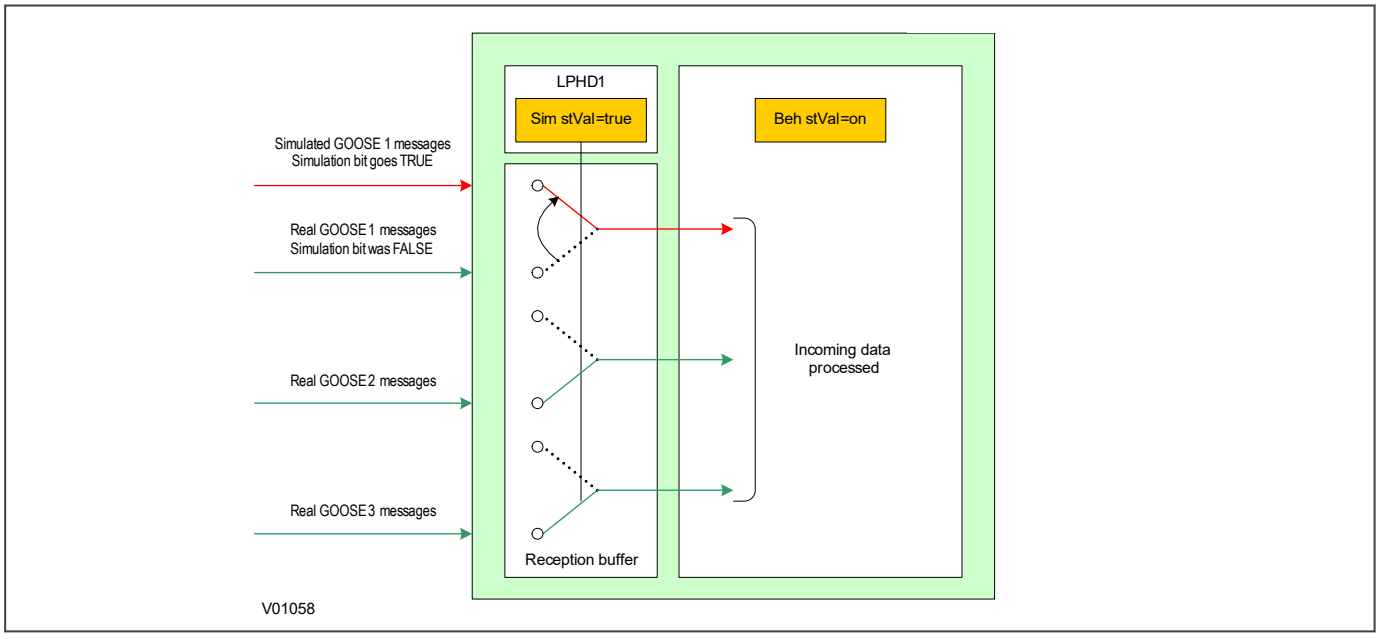



**Figure 298: Simulated input behaviour**

## 25.9.3 TESTING EXAMPLES

These examples show how you test the IED with and without simulated values. Depending on the IED Test Mode, it may respond by operating plant (for example by tripping the circuit breaker) or it may not operate plant.

### 25.9.3.1 TEST PROCEDURE FOR REAL VALUES

This procedure is for testing with real values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Disabled`
4. If using sampled values set the sampled values test mode
   Select *IEC 61850-9.2LE* → ***SV Test Mode*** → `Disabled`
5. Inject real signals using a test device connected to the merging units. The device will continue to listen to 'real' GOOSE messages and ignore simulated messages received.
6. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

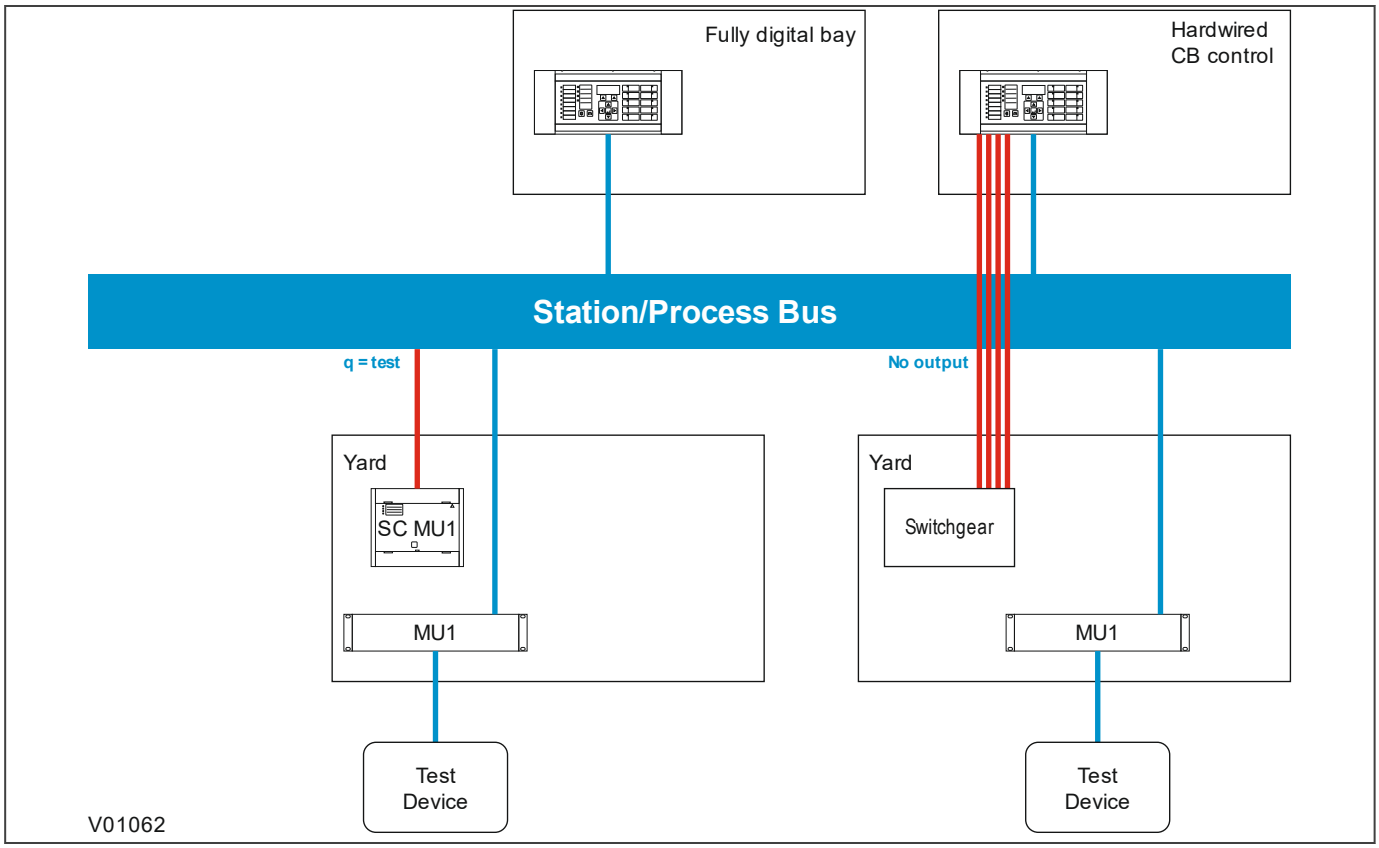



**Figure 299: Test example 1**

### 25.9.3.2 TEST PROCEDURE FOR SIMULATED VALUES - NO PLANT

This procedure is for testing with simulated values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`
4. If using sampled values set the sampled values test mode
   Select *IEC 61850-9.2LE* → ***SV Test Mode*** → `Enabled`
5. Inject simulated signals using a test device connected to the Ethernet network. The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of test mode. Each message is treated separately, but sampled values are considered as a single message.
6. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

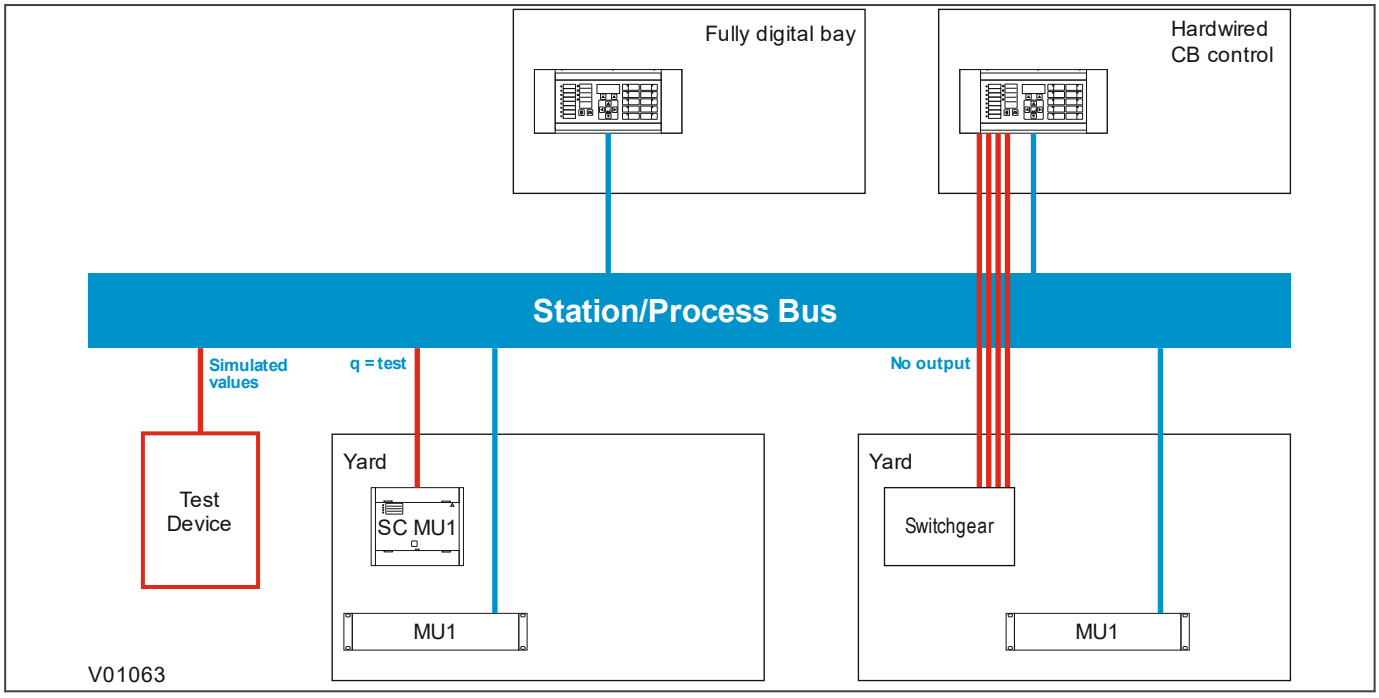



**Figure 300: Test example 2**

### 25.9.3.3 TEST PROCEDURE FOR SIMULATED VALUES - WITH PLANT

This procedure is for testing with simulated values with operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Test`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test`
3. Set device into Simulation Listening Mode

Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`

4. If using sampled values set the sampled values test mode

   Select *IEC 61850-9.2LE* → ***SV Test Mode*** → `Enabled`

5. Inject simulated signals using a test device connected to the Ethernet network.

   The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of IED test mode. Each message is treated separately, but sampled values are considered as a single message.

6. Verify function based on test signal outputs.

   Binary outputs (e.g. CB trips) will operate as normal. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram:

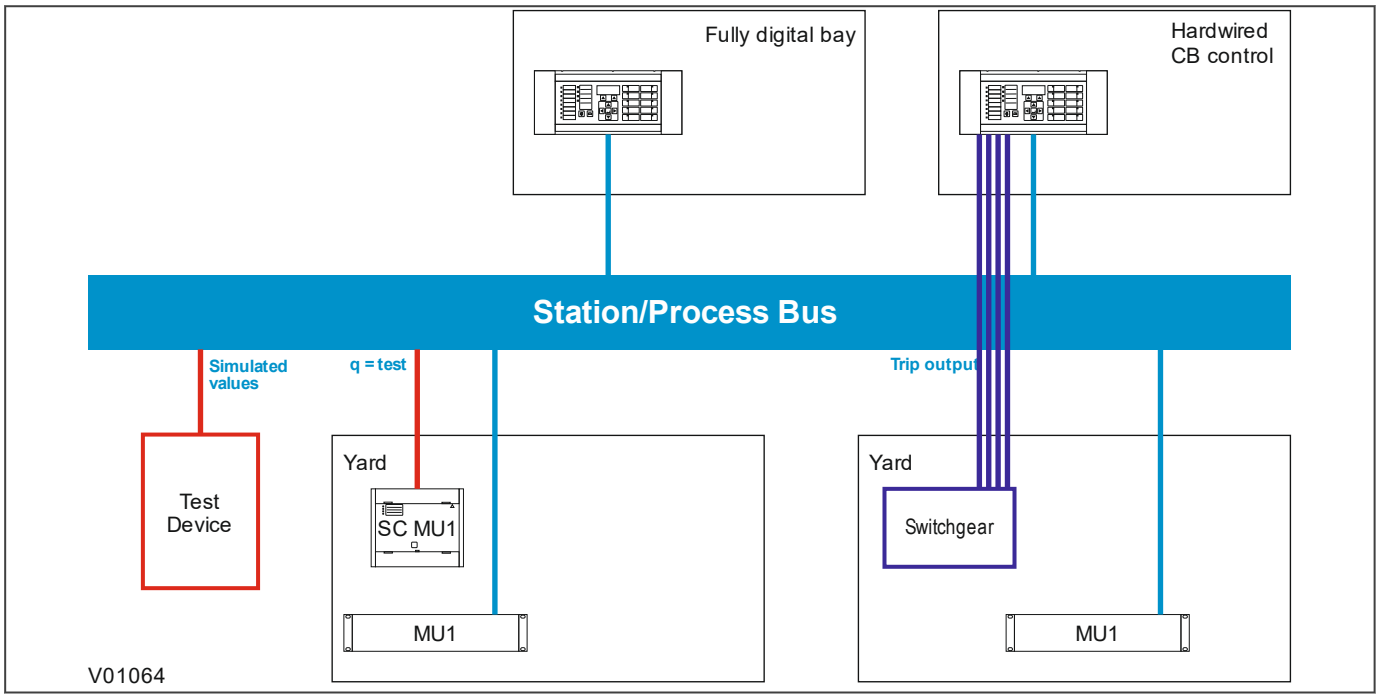



**Figure 301: Test example 3**

### 25.9.3.4 CONTACT TEST

The ***Apply Test*** command in this cell is used to change the state of the contacts set for operation.

If the device has been put into 'Contact Blocked' mode using an input signal (via the ***Block Contacts*** DDB signal) then the ***Apply Test*** command will not execute. This is to prevent a device that has been blocked by an external process having its contacts operated by a local operator using the HMI.

If the ***Block Contacts*** DDB is not set and the ***Apply Test*** command in this cell is issued, contacts change state and the command text on the LCD changes to `No Operation`. The contacts remain in the Test state until reset by issuing the ***Remove Test*** command. The command text on the LCD shows `No Operation` after the ***Remove Test*** command has been issued.

*Note:*
*When the **IED Test Mode** cell is set to Contacts Blocked, the **Relay O/P Status** cell does not show the current status of the output relays so cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.*

# 25.10 DISTANCE PROTECTION

## 25.10.1 SINGLE-ENDED TESTING

If the distance protection function is being used, test the reaches and time delays.

1. Check for any possible dependency conditions and simulate as appropriate
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested
3. Make a note of which elements need to be re-enabled after testing

### 25.10.1.1 PRELIMINARIES

You should now connect the IED to equipment able to supply phase-phase and phase-neutral volts with current in the correct phase relation for a particular type of fault on the selected characteristic angle. The facility for altering the loop impedance (phase-to-ground fault or phase-phase) presented to the IED is essential.

Use a three-phase digital/electronic injection test set to make the commissioning procedure easier.

1. If testing the distance elements using using test sets that do not provide a dynamic model to generate true fault delta conditions, set *COMMISSION TESTS* > ***Static Test Mode*** to `Enabled`. When set, this disables phase selector control and forces the device to use a conventional (non-delta) directional line.
2. For lower specification test equipment that cannot apply a full three phase set of healthy simulated pre-fault voltages, the VT supervision may need to be disabled to avoid spurious pickup. Set *CONFIGURATION* > ***Supervision*** to `Disabled`.
3. Connect the test equipment to the device using the test block(s), taking care not to open-circuit any CT secondary windings. If using MMLG type test blocks, the live side of the test plug must be provided with shorting links before it is inserted into the test block.
4. When the test is complete, make sure *COMMISSION TESTS* > ***Static Test Mode*** is set back to `Disabled`.

### 25.10.1.2 ZONE 1 REACH CHECK

The zone 1 element is set to be directional forward.

1. Apply a dynamic A-phase-to-neutral fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ1 timer setting, but less than tZ2. These settings are in the *DISTANCE* column. No trip should occur, and the red Trip LED should remain OFF.
2. Reduce the impedance and reapply the simulated fault.
3. Repeat this procedure until a trip occurs. When this happens, the display shows **Alarms/Faults present** and the Alarm and Trip LEDs switch ON.
4. To view the alarm message, keep pressing the read key until the yellow alarm LED changes from flashing to being steadily on.
5. At the prompt Press clear to reset alarms, press the C key. This clears the fault record from the display.
6. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
7. Read and reset the alarms

Modern injection test sets usually calculate the expected fault loop impedance from the device settings. For those that do not, check the reach for phase-phase and confirm the operation of the contacts. The appropriate loop impedance is given by the vector sum:

Z1 + Z1 residual = Z1 + (Z1.kZN Res Comp ∠kZN Angle) Ω

### 25.10.1.3 ZONE 2 REACH CHECK

The zone 2 element is set to be directional forward.

1. Apply a dynamic B-C fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ2 timer setting, but less than tZ3. These settings are in the *DISTANCE* column. No trip should occur, and the red Trip LED should remain OFF.
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
4. Read and reset the alarms.

Modern injection test sets usually calculate the expected fault loop impedance from the device settings. For those that do not, check the reach for phase-phase and confirm the operation of the appropriate contacts. The appropriate loop impedance is now given by:

2 x Z2 Ω

### 25.10.1.4 ZONE 3 REACH CHECK

1. The zone 3 element is set to forward, reverse or offset. The current injected must be in the appropriate direction to match the setting in the *DISTANCE SETUP* column.
2. Apply a dynamic C-A fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ3 timer setting (typically tZ3 + 100 ms).
3. Repeat the test described above to find the zone reach.
4. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
5. Read and reset the alarms.
6. Check that the correct reverse offset (Z3') has been applied. The setting is in the ***Z3' Ph Rev Reach*** and ***Z3' Gnd Rev Reach*** cells.

### 25.10.1.5 ZONE 4 REACH CHECK

The zone 4 element is set to be directional reverse.

1. Apply a dynamic B-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ4 timer setting (typically tZ4 + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
4. Read and reset the alarms.

### 25.10.1.6 ZONE P REACH CHECK

The zone P element can be set to forward or reverse directional or offset. The current injected must be in the correct direction to match the setting in the *DISTANCE SETUP* column.

1. Apply a dynamic C-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZP timer setting (typically tZP + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the relay trips. The measured impedance should be within +/-10% of the expected reach.
4. Read and reset the alarms.

#### 25.10.1.7 RESISTIVE REACH

This is for quadrilateral characteristics only.

Check that the correct settings for phase and ground element resistive reaches have been applied. The relevant settings are:

- R1Ph, R2Ph, R3Ph, R3Ph reverse, R4Ph and RP Ph for phase fault zones.
- R1Gnd, R2Gnd, R3Gnd, R3Gnd reverse, R4Gnd and RP Gnd for ground fault zones.

*Note:*
*Zone 3 has an independent setting for the forward resistance reach (right-hand resistive reach line), and the reverse resistance reach (left-hand resistive reach line).*

#### 25.10.1.8 LOAD BLINDER

1. Check that the correct settings for the load blinder have been applied. The settings are at the end of the *DISTANCE SETUP* column.
2. Verify that the ***Load B/Angle*** cell is set at least 10 degrees less than the ***Line Angle*** setting in the *LINE PARAMETERS* column.

### 25.10.2 OPERATION AND CONTACT ASSIGNMENT

You should inject a fault at half Z1 reach with the intention of causing a distance protection trip.

#### 25.10.2.1 PHASE A

1. Prepare a dynamic A-phase-to-neutral fault, as detailed above.
2. Set a timer to start when the fault injection is applied and to stop when the trip occurs.
3. To verify correct output contact mapping use the trip contacts that would be expected to trip the circuit breaker(s) (Any Trip for 3-pole tripping, Trip A for single pole tripping).
4. For two breaker applications, stop the timer when CB1 and CB2 trip contacts have both closed. Monitor by connecting the contacts in series to stop the timer if necessary.
5. Record the phase A trip time.
6. Switch OFF the AC supply and reset the alarms.

#### 25.10.2.2 PHASE B

1. Reconfigure to test a B phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to B phase operation close correctly.
3. Record the phase B trip time.
4. Switch OFF the AC supply and reset the alarms.

#### 25.10.2.3 PHASE C

1. Reconfigure to test a C phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to C phase operation close correctly.
3. Record the phase C trip time.
4. Switch OFF the AC supply and reset the alarms.

The average of the recorded operating times for the three phases should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.

*Note:*
*Where a non-zero time delay is set in the DISTANCE menu column, the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" delay.*

### 25.10.2.4 TIME DELAY SETTINGS

Check that the correct time delay settings have been applied. The relevant settings are in the *SCHEME LOGIC* column and are as follows:

- tZ1 Ph Time Delay and tZ1 Gnd Time Delay
- tZ2 Ph Time Delay and tZ2 Gnd Time Delay
- tZ3 Ph Time Delay and tZ3 Gnd Time Delay
- tZP Ph Time Delay and tZP Gnd Time Delay
- tZ4 Ph Time Delay and tZ4 Gnd Time Delay
- tZQ Ph Time Delay and tZQ Gnd Time Delay
- tZR Ph Time Delay and tZR Gnd Time Delay
- tZS Ph Time Delay and tZS Gnd Time Delay

*Note:*
*The device allows separate time delay settings for phase ("Ph") and ground ("Gnd") fault elements. BOTH must be checked to ensure that they have been set correctly.*

## 25.10.3 SCHEME TESTING

The device is tested for its response to internal and external fault simulations but the response depends on the aided channel (pilot) scheme selected. The response to the 'Reset Z1 Extension' opto-input is shown in the case of a Zone 1 Extension scheme.

We assume a conventional signalling scheme implementation.

If an InterMiCOM$^{64}$ scheme is used to provide the signalling, the scheme logic may not use opto-inputs for the aided scheme implementation. In this case, internal DDB signals need to be set or reset to test the operation of the protection scheme.

Use the IM64 Test Mode with the IM64 Test Pattern to assert or monitor the relevant signals.

Ensure that the injection test set timer is still connected to measure the time taken for the device to trip. A series of fault injections are applied, with a Zone 1, end-of-line, or Zone 4 fault simulated. At this stage, note the method in which each fault is applied, but do not inject yet:

- **Zone 1 fault**: A dynamic forward A-B fault at half the Zone 1 reach is simulated.
- **End of line fault**: A dynamic forward A-B fault at the remote end of the line is simulated. The fault impedance simulated should match the *LINE PARAMETERS* > ***Line Impedance*** setting.
- **Zone 4 fault**: A dynamic reverse A-B fault at half the Zone 4 reach is simulated.

The following table indicates the expected response for various test situations for a conventional signalling scheme.

| Fault Type Simulated | IED RESPONSE | | | | | |
|---|---|---|---|---|---|---|
| | Forward Fault in Zone 1 | | Forward Fault at End of Line (Within Z1X/Z2) | | Reverse Fault in Zone 4 | |
| Signal receive opto | ON | OFF | ON | OFF | ON | OFF |
| Zone 1 extension | Trip | Trip | No Trip | Trip | No Trip | No Trip |

| Fault Type Simulated | IED RESPONSE | | | | | |
|---|---|---|---|---|---|---|
| | Forward Fault in Zone 1 | | Forward Fault at End of Line (Within Z1X/Z2) | | Reverse Fault in Zone 4 | |
| Blocking scheme | Trip, No Signal Send | Trip, No Signal Send | No Trip, No Signal Send | Trip, No Signal Send | No Trip, Signal Send | No Trip, Signal Send |
| Permissive Scheme (PUR/PUTT) | Trip, Signal Send | Trip, Signal Send | Trip, No Signal Send | No Trip, No Signal Send | No Trip, No Signal Send | No Trip, No Signal Send |
| Permissive Scheme (POR/POTT) | Trip, Signal Send | Trip, Signal Send | Trip, Signal Send | No Trip, Signal Send | No Trip, No Signal Send | No Trip, No Signal Send |

### 25.10.3.1 SCHEME TRIP TEST FOR ZONE 1 EXTENSION

1. Energise the ***Reset Z1X*** (Reset Zone 1 Extension) opto-input. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, or station battery.
2. Inject an end of line fault. The duration of injection should be set to 100 ms. No trip should occur.
3. De-energise the ***Reset Z1X*** opto-input
4. Repeat the test injection and record the operating time. This should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.
5. Switch OFF the AC supply and reset the alarms.

*Note:*
*Here a non-zero tZ1 Ph or tZ1 Gnd time delay is set in the DISTANCE column, the expected operating time is typically within +/- 5% of the tZ1 setting plus the "instantaneous" delay quoted above.*

### 25.10.3.2 SCHEME TRIP TESTS FOR PERMISSIVE SCHEMES

This test applies to both Permissive Underreach, and Permissive Overreach aided scheme applications.

1. Energise the ***Signal Receive*** opto-input. This is done by applying a continuous DC voltage onto the required opto-input from the test set, or station battery.
2. Inject an end of line fault, and record the operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.
3. Switch OFF the AC supply and reset the alarms.
4. De-energise the ***Signal Receive*** opto-input (remove the temporary energisation link, to turn it OFF).

*Note:*
*Where a non-zero Aided Distance Dly time delay is set in the DISTANCE menu column, the expected operating time is typically within +/- 5% of the tZ1 setting plus the "instantaneous" delay quoted above.*

### 25.10.3.3 SCHEME TRIP TESTS FOR BLOCKING SCHEME

1. Energise the ***Signal Receive*** opto-input. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, or station battery.
2. Inject an end of line fault. The duration of injection should be set to 100 ms. No trip should occur.
3. De-energise the ***channel received*** opto-input.
4. Repeat the test injection, and record the operating time.
5. Switch OFF the AC supply and reset the alarms.

*Note:*
*For blocking schemes, a non-zero Aided Distance Dly time delay is set, so the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" operating delay. The trip time should thus be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz, plus 1.05 x Delay setting.*

### 25.10.3.4 SIGNAL SEND TEST FOR PERMISSIVE SCHEMES

This test applies to both Permissive Underreach, and Permissive Overreach scheme applications.

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the ***Signal Send*** contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Inject a Zone 1 fault, and record the ***Signal Send*** contact operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
3. Switch OFF the AC supply and reset the alarms.

### 25.10.3.5 SIGNAL SEND TEST FOR BLOCKING SCHEME

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the Signal Send contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Inject a Zone 4 fault, and record the signal send contact operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
3. Switch OFF the ACsupply and reset the alarms.

### 25.10.3.6 SCHEME TIMER SETTINGS

1. Check that the correct time delay settings have been applied. The relevant settings in the *AIDED SCHEMES* column are:
   a. ***tRev. Guard*** (if applicable/visible)
   b. ***Unblocking Delay*** (if applicable/visible)
   c. ***Wl Trip Delay*** (if applicable/visible)
2. When the tests are completed, restore all settings that were disabled for testing purposes.
3. Set the ***Static Test Mode*** to `Disabled`.
4. Remove any wires or leads temporarily fitted to energise the channel receive opto-input

# 25.11 DELTA DIRECTIONAL COMPARISON

## 25.11.1 SINGLE-ENDED TESTING

If the delta directional comparison aided scheme is being used, test the operation

1. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
2. Make a note of which elements need to be re-enabled after testing

### 25.11.1.1 PRELIMINARIES

Use a three-phase digital/electronic injection test set to make the commissioning procedure easier.

Connect the test equipment to the device using the test block(s) taking care not to open-circuit any CT secondary. If MMLG type test blocks are used, the live side of the test plug must be provided with shorting links before it is inserted into the test block.

### 25.11.1.2 SINGLE-ENDED INJECTION TEST

This set of injection tests aims to determine correct operation of a single IED at one end of the scheme. The device is tested in isolation, with the communications channel to the remote line terminal disconnected.

First verify that the device cannot send or receive channel scheme signals to or from the remote line end.

The device is tested for its response to forward and reverse fault injections, but the response depends on the aided channel (pilot) scheme that is selected. The table below shows the expected response for various test situations for a conventional signalling scheme.

We assume a conventional signalling scheme implementation.

If an InterMiCOM$^{64}$ scheme is used to provide the signalling, the scheme logic may not use opto-inputs for the aided scheme implementation. In this case, internal DDB signals need to be set or reset to test the operation of the protection scheme.

Use the IM64 Test Mode with the IM64 Test Pattern to assert or monitor the relevant signals.

| Direction of Fault Test Injection | IED RESPONSE | | | |
|---|---|---|---|---|
| | Forward Fault | | Reverse Fault | |
| Signal receive opto | ON | OFF | ON | OFF |
| Blocking scheme | No Trip,<br>No Signal Send | Trip,<br>No Signal Send | No Trip,<br>Signal Send | No Trip,<br>Signal Send |
| Permissive scheme (POR/POTT) | Trip,<br>Signal Send | No Trip,<br>Signal Send | No Trip,<br>No Signal Send | No Trip,<br>No Signal Send |

### 25.11.1.3 FORWARD FAULT PREPARATION

Configure the test set to inject a dynamic sequence of injection, as follows:

1. Simulate a healthy three-phase set of balanced voltages, each of magnitude Vn. No load current should be simulated. The duration of injection should be set to 1 second. Step 1 therefore mimics a healthy unloaded line before the onset of a fault.
2. Simulate a forward fault on the A-phase. The A-phase voltage must be simulated to drop by 3 times the ***Dir. V Fwd*** setting,

Va = Vn – 3 (***Dir. V Fwd***)

The fault current on the A-phase should be set to 3 times the Dir. I Fwd setting, lagging Va by a phase angle equal to the line angle,

Ia = 3 (Dir. I Fwd)∠-θ Line

Phases B and C should retain their healthy pre-fault voltage, and no current. The duration of injection should be set to 100 ms longer than the ***Aid. 1 Delta Dly***, ***Aid. 2 Delta Dly*** time setting.

## 25.11.2 OPERATION AND CONTACT ASSIGNMENT

You should inject a forward fault with the intention of causing a scheme trip. For a Permissive scheme, the Signal Receive opto-input needs to be energized. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, or station battery.

For a Blocking scheme, the opto-input should remain de-energised.

### 25.11.2.1 PHASE A

1. Prepare a dynamic A-phase-to-neutral fault, as detailed above.
2. Set a timer to start when the fault injection is applied and to stop when the trip occurs.
3. To verify correct output contact mapping use the trip contacts that would be expected to trip the circuit breaker(s) (Any Trip for 3-pole tripping, Trip A for single pole tripping).
4. For two breaker applications, stop the timer when CB1 and CB2 trip contacts have both closed. Monitor by connecting the contacts in series to stop the timer if necessary.
5. Record the phase A trip time.
6. Switch OFF the AC supply and reset the alarms.

### 25.11.2.2 PHASE B

1. Reconfigure to test a B phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to B phase operation close correctly.
3. Record the phase B trip time.
4. Switch OFF the AC supply and reset the alarms.

### 25.11.2.3 PHASE C

1. Reconfigure to test a C phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to C phase operation close correctly.
3. Record the phase C trip time.
4. Switch OFF the AC supply and reset the alarms.

The average of the recorded operating times for the three phases should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.

*Note:*
*Where a non-zero time delay is set in the DISTANCE menu column, the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" delay.*

## 25.11.3 DELTA PROTECTION SCHEME TESTING

### 25.11.3.1 SIGNAL SEND TEST FOR PERMISSIVE SCHEMES

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the ***Signal Send*** contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Repeat the forward fault injection, and record the ***Signal Send*** contact operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
3. Switch OFF the AC supply and reset the alarms.

### 25.11.3.2 SIGNAL SEND TEST FOR BLOCKING SCHEMES

Configure the test set to inject a dynamic sequence of injection, as follows:

1. Simulate a healthy three-phase set of balanced voltages, each of magnitude Vn. No load current should be simulated. The duration of injection should be set to 1 second. Step 1 therefore mimics a healthy unloaded line, prior to the onset of a fault.
2. Simulate a reverse fault on the A-phase. The A-phase voltage must be simulated to drop by 3 times the Dir. V Rev setting; Va = Vn – 3(Dir. V Rev)
3. The fault current on the A-phase should be set to 3 times the DI Rev setting, and in antiphase to the forward injections; Ia = 3 (Dir. I Rev) ∠180°-θ Line
4. Prepare the dynamic A phase reverse fault, as detailed above. Ensure that the test set is simulating Steps 1 and 2 as one continuous transition.
5. Set a timer to start when the fault injection is applied, and to stop when the Delta scheme Signal Send contact closes.
6. Apply the test, and record the signal send contact response time. The recorded operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
7. Switch OFF the AC supply and reset the alarms.

**Caution:**
**When the tests are completed, restore all settings that were disabled for testing purposes.**

**Caution:**
**Remove any wires or leads temporarily fitted to energise the channel receive opto-input.**

# 25.12 DEF AIDED SCHEMES

## 25.12.1 EARTH CURRENT PILOT SCHEME

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Make a note of which elements need to be re-enabled after testing.

We assume a conventional signalling scheme implementation.

If an InterMiCOM$^{64}$ scheme is used to provide the signalling, the scheme logic may not use opto-inputs for the aided scheme implementation. In this case, internal logic signals (DDBs) need to be set or reset to test the operation of the protection scheme.

The IM64 Test Mode in conjunction with the IM64 Test Pattern should be used to assert or monitor the relevant signals.

This set of injection tests aims to determine that a single device, at one end of the scheme is performing correctly.

*Note:*
*The device must be tested in isolation, with the communications channel to the remote line terminal disconnected.*

### 25.12.1.1 PRELIMINARIES

1. Determine which output relays have been selected to operate when a DEF trip occurs, by viewing the programmable scheme logic. If the trip outputs are phase segregated (a different output relay allocated for each phase), the output relay assigned for tripping on 'A' phase faults should be used.
2. Connect the output relay so that its operation will trip the test set and stop the timer.
3. Connect the current output of the test set to the 'A' phase current transformer input
4. Connect, all three phase voltages Va, Vb, and Vc.
5. Depending on the test equipment used, make sure the timer is set to start when the current is applied.

### 25.12.1.2 PERFORM THE TEST

1. Ensure that the timer is reset and prepare the following test shot.
2. Simulate a forward fault on the A-phase. The A-phase voltage must be simulated to drop by 4 times the ***DEF VNpol Set*** setting; Va = Vn - 4 (DEF Vpol)
3. Set the fault current on the A-phase should to 2 times the DEF Threshold setting, and in the forward direction. For a forward fault, the current Ia should lag the voltage Va by the DEF Char Angle setting; Ia = 2 (IN DEF Threshold $\angle\theta$ DEF)
4. Phases B and C should retain their healthy pref-ault voltage, and no current. The duration of the injection should be in excess of the DEF Delay setting (typically ***Aid. 1 DEF Dly.*** and ***Aid. 2 DEF Dly.*** + 100 ms).

| Direction of Fault Test Injection | IED RESPONSE | | | |
|---|---|---|---|---|
| | Forward Fault | | Reverse Fault | |
| Signal Receive Opto | ON | OFF | ON | OFF |
| Blocking Scheme | No Trip,<br>No Signal Send | Trip,<br>No Signal Send | No Trip,<br>Signal Send | No Trip,<br>Signal Send |
| Permissive Scheme (POR/POTT) | Trip,<br>Signal Send | No Trip,<br>Signal Send | No Trip,<br>No Signal Send | No Trip,<br>No Signal Send |

#### 25.12.1.3 FORWARD FAULT TRIP TEST

A forward fault is now injected as described, with the intention to cause a scheme trip.

For a permissive scheme, the ***Signal Receive*** opto-input should be energised. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, station battery, or IED field voltage. The commissioning engineer decides on the best method.

For a blocking scheme, the opto-input should remain de-energised (“OFF”).

1. Apply the fault and record the (phase A) trip time.
2. Switch OFF the AC supply and reset the alarms.

The aided earth fault (DEF) scheme trip time for POR schemes (permissive overreach) POR schemes should be less than 40 ms.

For blocking schemes, where a non-zero ***DEF Dly*** time delay is set, the expected operating time is typically within +/- 5% of the delay setting plus the “instantaneous” (40 ms) delay quoted above.

There is no need to repeat the test for phases B and C, as these trip assignments have already been proven by the distance/delta trip tests.

### 25.12.2 SCHEME TESTING

#### 25.12.2.1 SIGNAL SEND TEST FOR PERMISSIVE SCHEMES

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the ***Signal Send*** contact (the contact that would normally be connected to the pilot/signalling channel).
2. Repeat the forward fault injection, and record the ***Signal Send*** contact operating time. The measured operating time should typically be less than 40 ms.
3. Switch OFF the AC supply and reset the alarms.

#### 25.12.2.2 SIGNAL SEND TEST FOR BLOCKING SCHEMES

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the Signal Send contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Reverse the current flow direction on the A phase to simulate a reverse fault.
3. Perform the reverse fault injection and record the signal send contact operating time. The measured operating time should typically be less than 40 ms.
4. Switch OFF the AC supply and reset the alarms.

**Caution:**
**When the tests are completed, restore all settings that were disabled for testing purposes.**

**Caution:**
**Remove any wires or leads temporarily fitted to energise the channel receive opto-input.**

## 25.13 OUT OF STEP PROTECTION

For this test, an injection set with a state sequencer function is required, as dynamic impedance conditions are going to be tested. The four states impedances that applied during the Out of Step commissioning process are shown below:

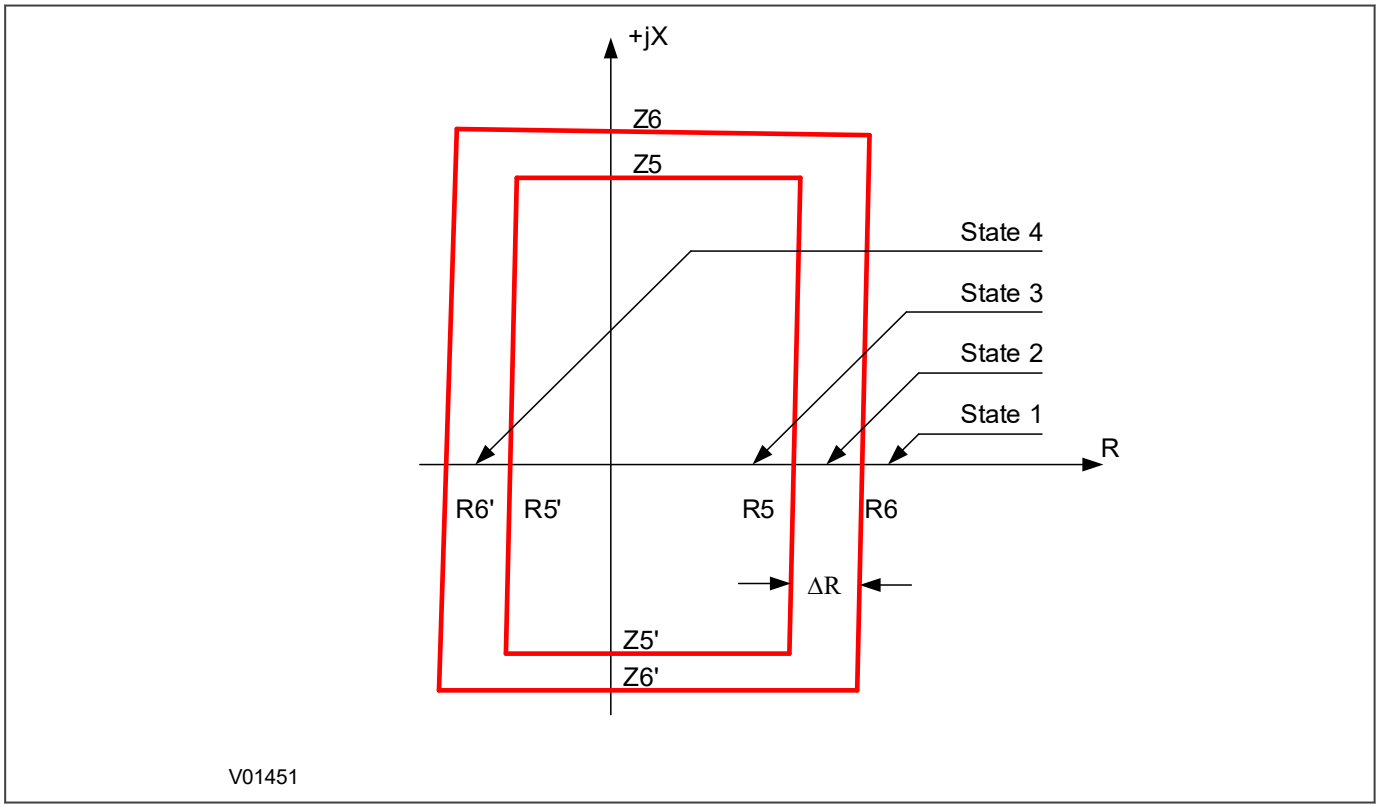



**Figure 302: State impedances**

Depending on the Out of Step (OST) settings, use one of the following setting options.

- OST setting
- Predictive OST setting
- Predictive and OST setting

### 25.13.1 OST SETTING

1. Clear all alarms.
2. Set the OST timer to zero.
3. To test OST, a 4-state test sequence is required. Based on healthy voltages (VA = VB = VC = 57.8 V) calculate the currents to generate the impedances as below.

| | State 1 | State 2 | State 3 | State 4 |
|---|---|---|---|---|
| Applied current (all 3 phases) | 57.8/(1.1R6) | 57.8/(R5+0.5(R6-R5)) | 57.8/(0.95R5) | 57.8/(1.1R5') |
| Angle | 0° | 0° | 0° | 180° |
| Duration | 500 ms | Longer than 'Delta t' set time | 100 ms | 500 ms |

Now apply the 4-state sequence, check that all 3-phases have tripped and that an OST alarm is displayed on the local LCD.

*Note:*
*The angle in the table above is the angle between voltages and their respective currents. In state 4 the currents are displaced 180° from their respective voltages.*

## 25.13.2 PREDICTIVE OST SETTING

1. Clear all alarms.
2. Set the OST timer to zero.
3. To test OST, a 3-state test sequence is required. Based on healthy voltages (VA = VB = VC = 57.8 V) calculate the currents to generate the impedances as below.

| | State 1 | State 2 | State 3 |
|---|---|---|---|
| Applied current (all 3 phases) | 57.8/(1.1R6) | 57.8/(R5+0.5(R6-R5)) | 57.8/(0.95R5) |
| Angle | 0° | 0° | 0° |
| Duration | 500 ms | Longer than 25 ms but shorter than 'Delta t' set time | 500 ms |

Now apply the 3-state sequence, check that all 3-phases have tripped and that an OST alarm is displayed on the local LCD.

## 25.13.3 PREDICTIVE AND OST SETTING

As per Predictive OST

## 25.13.4 OST TIMER TEST

1. Repeat the test as for 'predictive OST' and observe that the 3-phase tripping comes up after the 'Tost' set delay.
2. Record the operating time in the commissioning record sheet.

## 25.14 PROTECTION TIMING CHECKS

There is no need to check every protection function. Only one protection function needs to be checked as the purpose is to verify the timing on the processor is functioning correctly.

### 25.14.1 DEPENDENCY CONDITIONS

Some protection elements can be set to have dependencies on the availability of the protection communication channel(s) and on the status of the voltage transformer supervision function (VTS).

If you are testing a distance model, the distance protection can be permanently enabled, or it can be set so that it is only enabled in the event of a failure of the protection communications channel(s).

The overcurrent and earth faults elements can be permanently enabled, or can be set so that they are only enabled:

- in the event of a failure of the protection communications channel(s)
- in the event of a VTS alarm
- according to a logical combination of both conditions.

If these elements are enabled with a dependency upon the above conditions, it is necessary to simulate the condition to test the correct operation of the protection function.

A communications failure can be simulated by setting the Test Loopback cell to Disabled and checking that the IED raises a Comms Fail alarm.

At the end of the test, clear the communications alarms and reset the statistics.

A VTS alarm can be raised by applying a 3-phase voltage to the VT inputs and then removing one phase voltage for a duration exceeding the VTS Time Delay setting.

At the end of the tests, clear the VTS alarm.

### 25.14.2 OVERCURRENT CHECK

If the overcurrent protection function is being used, test the overcurrent protection for stage 1.

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Make a note of which elements need to be re-enabled after testing.
4. Connect the test circuit.
5. Perform the test.
6. Check the operating time.

### 25.14.3 CONNECTING THE TEST CIRCUIT

1. Use the PSL to determine which output relay will operate when an overcurrent trip occurs.
2. Use the output relay assigned to ***Trip Output A***.
3. Use the PSL to map the protection stage under test directly to an output relay.

> *Note:*
> *If using the default PSL, use output relay 3 as this is already mapped to the DDB signal* ***Trip Command Out****.*

4. Connect the output relay so that its operation will trip the test set and stop the timer.
5. Connect the current output of the test set to the A-phase current transformer input.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column is set to `Directional Fwd`, the current should flow out of terminal 2. If set to `Directional Rev`, it should flow into terminal 2.

If the ***I>1 Directional*** cell in the *OVERCURRENT* column has been set to `Directional Fwd` or `Directional Rev`, the rated voltage should be applied to terminals 20 and 21.

6. Ensure that the timer starts when the current is applied.

*Note:*
*If the timer does not stop when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the direction of operation set. Try again with the current connections reversed.*

## 25.14.4 PERFORMING THE TEST

1. Ensure that the timer is reset.
2. Apply a current of twice the setting shown in the ***I>1 Current Set*** cell in the *OVERCURRENT* column.
3. Note the time displayed when the timer stops.
4. Check that the red trip LED has illuminated.

## 25.14.5 CHECK THE OPERATING TIME

Check that the operating time recorded by the timer is within the range shown below.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

| Characteristic | Operating Time at Twice Current Setting and Time Multiplier/Time Dial Setting of 1.0 | |
|---|---|---|
| | Nominal (seconds) | Range (seconds) |
| DT | I>1 Time Delay setting | Setting ±2% |
| IEC S Inverse | 10.03 | 9.53 - 10.53 |
| IEC V Inverse | 13.50 | 12.83 - 14.18 |
| IEC E Inverse | 26.67 | 24.67 - 28.67 |
| UK LT Inverse | 120.00 | 114.00 - 126.00 |
| IEEE M Inverse | 3.8 | 3.61 - 4.0 |
| IEEE V Inverse | 7.03 | 6.68 - 7.38 |
| IEEE E Inverse | 9.50 | 9.02 - 9.97 |
| US Inverse | 2.16 | 2.05 - 2.27 |
| US ST Inverse | 12.12 | 11.51 - 12.73 |

*Note:*
*With the exception of the definite time characteristic, the operating times given are for a Time Multiplier Setting (TMS) or Time Dial Setting (TDS) of 1. For other values of TMS or TDS, the values need to be modified accordingly.*
*For definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively. You may need to add this the IED's acceptable range of operating times.*

**Caution:**
**On completion of the tests, you must restore all settings to customer specifications.**

## 25.15 SYSTEM CHECK AND CHECK SYNCHRONISM

This function performs a comparison between the line voltage and the bus voltage.

There are two voltage inputs to compare:

- one from the voltage transformer input from the line side of the circuit breaker (Main VT)
- one from the VT on the bus side of the circuit breaker (CS VT).

In most cases the line VT input is three phase, whereas the bus VTs are single phase.

The bus VT inputs are normally single phase so the system voltage checks are made on single phases and the VT may be connected to either a phase-to-phase or phase to neutral voltage.

For these reasons, the IED has to be programmed with the appropriate connection. The ***CS Input*** setting in the *CT AND VT RATIOS* column can be set to A-N, B-N, C-N, A-B, B-C or C-A according to the application.

The single-phase bus VT inputs each have associated phase shift and voltage magnitude compensation settings to compensate for healthy voltage angle and magnitude differences between the check sync VT input and the selected main VT reference phase. These are:

- ***CS VT Ph Shift*** and ***CS VT Mag***

Any voltage measurements or comparisons using bus VT inputs are made using the compensated values.

Each circuit breaker controlled can have two stages of check synchronism enabled according to the settings:

- ***System Checks***, ***CS1 Status*** and ***CS2 Status***

When the system voltage check conditions are satisfied, the relevant DDB signals are asserted high as follows:

- DDB (883): Check Sync 1 OK
- DDB (884): Check Sync 2 OK

These DDB signals should be mapped to the monitor/download port and used to indicate that the system check synchronism condition has been satisfied.

### 25.15.1 CHECK SYNCHRONISM PASS

1. Taking note of the check synchronism settings, identify the appropriate VT input terminals and inject voltage signals that should satisfy the system voltage check synchronism criteria.
2. Check that the DDB signals are asserted high.

### 25.15.2 CHECK SYNCHRONISM FAIL

1. Change the voltage signals so that the criteria are not satisfied
2. Check that the appropriate DDB signals are driven low

## 25.16 CHECK TRIP AND AUTORECLOSE CYCLE

If the auto-reclose function is being used, the circuit breaker trip and auto reclose cycle can be tested automatically by using the application-specific settings.

To test the trip and close operation without operating the breaker, the following conditions must be satisfied:

- The ***CB Healthy*** DDB signal should either not be mapped, or if it is mapped it must be asserted high.
- The CB status inputs (52A, etc.) should either not be mapped, or if they are mapped they should be activated to mimic the circuit breaker operation.
- Some models can be configured for single-pole tripping. If configured for single pole tripping, either set *CT/VT RATIO* > ***VT Connected*** to `No`, or apply appropriate voltage signals to prevent the pole dead logic from converting to 3-pole tripping.

1. To test the first three-phase auto-reclose cycle, set *COMMISSION TESTS* > ***Test Autoreclose*** to `Trip 3 Pole`. The IED performs a trip/reclose cycle.
2. Repeat this operation to test the subsequent three-phase auto-reclose cycles.
3. Check all output relays (used for such as circuit breaker tripping and closing, or blocking other devices) operate at the correct times during the trip/close cycle.

Check the auto-reclose cycles for single phase trip conditions one at a time by sequentially setting *COMMISSION TESTS* > ***Test Autoreclose*** to `Trip Pole A`, `Trip Pole B` and `Trip Pole C`.

## 25.17 END-TO-END COMMUNICATION TESTS

If the IED is being used in a scheme with InterMiCOM$^{64}$ communications you must perform end-to-end testing of the protection communications channels.

In this section all loopbacks are removed and satisfactory communications between line ends of the IEDs in the scheme are confirmed.

*Note:*
*End-to-end communication requires a working telecommunication channel between line ends (which may be a multiplexed link or may be a direct connection). If the telecommunication channel is not available, it is not possible to establish end-to end communication. Unless otherwise directed by local operational practise, follow the instructions in this section so the scheme is ready for full operation when the telecommunications channels become available.*

*Note:*
*The trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.*

### 25.17.1 REMOVE LOCAL LOOPBACKS

As well as removing the loopback, this section checks that all wiring and optical fibre are reconnected. If P591, P592 or P593 interface units are installed the application-specific settings are also applied.

1. Check the alarm records to ensure that no communications failure alarms have occurred while the loopback test was in progress. If it was necessary to 'fail' the communications while testing the non-current differential elements, observe the communications behaviour for a few minutes before removing the loopbacks.
2. After you are satisfied with the communications behaviour in loopback, set *COMMISSION TESTS* > ***Test Mode*** and ***Test Loopback*** to `Disabled`.

*Note:*
*Most of the required optical signal power levels have already been measured and recorded. If all signalling uses P59x interface units, no further measurements are required. If, however, 56/64 kb/s or C37.94 direct fibre communications are used, further measurements are needed.*

#### 25.17.1.1 RESTORING DIRECT FIBRE CONNECTIONS

When restoring direct fibre connections, check the optical power level received from the remote IED(s).

1. Remove the loopback test fibres and at both ends of each channel used, reconnect the fibre optic cables for communications between IEDs.
2. For each channel fitted, remove the fibre connecting to the optical receiver (RX).
3. Using an optical power meter measure the strength of the signal received from the remote IED. The measurements should be within -25.4 dBm and -16.8 dBm for 850 nm fibre connections and between -37 dBm and -7 dBm for 1300 nm fibre connections
4. Record the received power level(s).
5. Reconnect the fibre(s) to the IED receiver(s).

**Warning:**
**NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.**

#### 25.17.1.2 RESTORING C37.94 FIBRE CONNECTIONS

When restoring C37.94 fibre connections, check the optical power level received from both the IED and the C37.94 multiplexer.

1. Remove the loopback test fibres and at both ends of each channel used.
2. Reconnect the fibre optic cables for communications between IEDs and the C37.94 compatible multiplexer.
3. Check that the value received from the IED at the C37.94 multiplexer, as well as that received by the IED from the C37.94 multiplexer are between -25.4 dBm (min) and -16.8 dBm (max).
4. Record the received power level(s).
5. Reconnect the fibre(s) to the IED receiver(s).

**Warning:**
**NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.**

#### 25.17.1.3 COMMUNICATIONS USING P59X INTERFACE UNITS

If external wiring has been removed to facilitate testing, ensure that it is replaced in accordance with the relevant connection diagram or scheme diagram.

**For the P591:**

1. Check that all the cabling is correct.
2. Verify that the Healthy LED is on.
3. If you are using the C37.94 protocol, please confirm one P591 is set to Master and the other P591 is set to Slave.

**For the P592:**

1. Set the V.35 LOOPBACK switch to the 0 position.
2. Set the CLOCK SWITCH, DSR, CTS and DATA RATE switches on each unit to the positions required for the specific application.
3. Ensure the OPTO LOOPBACK switch is in the 0 position.
4. If applicable, replace the secondary front cover.

**For the P593:**

1. Set the X.21 LOOPBACK switch to the OFF position.
2. Ensure the OPTO LOOPBACK switch is also in the OFF position.
3. If applicable, replace the secondary front cover.

### 25.17.2 REMOVE REMOTE LOOPBACKS

Remove loopbacks at remote terminal connected to channel 1 and channel 2 by repeating the instructions for local loopback removal.

### 25.17.3 VERIFY COMMUNICATION BETWEEN IEDS

Reset any alarm indications and check that no further communications failure alarms are raised.

1. Check channel status and propagation delays in *MEASUREMENTS 4* column for channel 1 (and channel 2 where fitted).
2. Check that the first two bits in ‘Channel Status’ (Rx and Tx) are displaying ‘1’ (11********** where * indicates a ‘don’t care’ state).

3. Clear the statistics and record the number of valid messages and the number of errored messages after a minimum period of 1 hour.
4. Check that the ratio of errored/good messages is better than 10-4.
5. Record the measured message propagation delays for channel 1, and channel 2 (if fitted).

# 25.18 END-TO-END SCHEME TESTS

This section aims to check that the signalling channel is able to transmit the ON/OFF signals used in aided schemes between the remote line ends.

Before testing, check that the channel is healthy. For example, if a power line carrier link is being used, it may not be possible to perform the tests until the protected circuit is in service.

## 25.18.1 AIDED SCHEME 1

Aided Scheme 1 can be tested by operating output contacts to mimic the transmission of an aided channel signal.

For these tests, an engineer needs to be present at both ends of the line - at the local end to send aided signals, and at the remote end to observe that the signals are received. A telephone link between the two commissioning engineers is also necessary, to allow conversation.

1. Put the IED in test mode by setting *COMMISSION TESTS* > ***Test Mode*** to `Blocked`.
2. Record which contact is assigned as the ***Signal Send 1*** output
3. Select this output contact as the one to test and advise the engineer at the remote end that the contact is about to be tested.

### 25.18.1.1 PREPARATION AT REMOTE END

At the remote end, the engineer must confirm the assignment of the ***Monitor Bits*** in the *COMMISSION TESTS* column in the menu, to be able to see the aided channel on arrival.

Scroll down and ensure that the ***Monitor Bit 1*** cell is set to `DDB493` and that the ***Monitor Bit 5*** cell is set to `DDB507`. The Test Port Status cell appropriately sets or resets the bits that now represent Aided 1 Scheme Receive (DDB493), and Aided 2 Scheme Receive (DDB507), with the rightmost bit representing Aided Channel 1. From now on the engineer at the remote end should monitor the indication of the ***Test Port Status*** cell.

### 25.18.1.2 PERFORMING THE TEST

1. At the local end, set the *COMMISSION TESTS* > ***Contact Test*** to `Apply Test`.
2. Reset the output relay by setting *COMMISSION TESTS* > ***Contact Test*** to `Remove Test`.
3. Check with the engineer at the remote end that the Aided Channel 1 signal did change state as expected. The ***Test Port Status*** cell should have responded as in the table below.

| DDB No. | | | | 507 | | | | 493 |
|---|---|---|---|---|---|---|---|---|
| Monitor Bit | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| Contact Test OFF | X | X | X | X | X | X | X | 0 |
| Contact Test Applied (ON) | X | X | X | X | X | X | X | 1 |
| Test OFF | X | X | X | X | X | X | X | 0 |

X = Don't Care

Now return the IED to service by setting *COMMISSION TESTS* > ***Test Mode*** to `Disabled`.

### 25.18.1.3 CHANNEL CHECK IN THE OPPOSITE DIRECTION

Repeat the aided scheme 1 test procedure, but this time to check that the channel responds correctly when keyed from the remote end. The remote end commissioning engineer should perform the contact test, with the Monitor Option observed at the local end.

### 25.18.2 AIDED SCHEME 2

1. If applicable, repeat the test for Aided Channel 2.
2. Return the device to service by setting *COMMISSION TESTS* > ***Test Mode*** to `Disabled`.

## 25.19 ONLOAD CHECKS

**Warning:**
**Onload checks are potentially very dangerous and may only be carried out by qualified and authorised personnel.**

Onload checks can only be carried out if there are no restrictions preventing the energisation of the plant, and the other devices in the group have already been commissioned.

Remove all test leads and temporary shorting links, then replace any external wiring that has been removed to allow testing.

**Warning:**
**If any external wiring has been disconnected for the commissioning process, replace it in accordance with the relevant external connection or scheme diagram.**

### 25.19.1 CONFIRM VOLTAGE CONNECTIONS

1. Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated.
2. Check that the system phase rotation is correct using a phase rotation meter.
3. Compare the values of the secondary phase voltages with the measured voltage magnitude values, which can be found in the *MEASUREMENTS 1* menu column.

| Cell in MEASUREMENTS 1 Column | Corresponding VT Ratio in CT/VT RATIOS Column |
|---|---|
| *VAB MAGNITUDE*<br>*VBC MAGNITUDE*<br>*VCA MAGNITUDE*<br>*VAN MAGNITUDE*<br>*VBN MAGNITUDE*<br>*VCN MAGNITUDE* | Main VT Primary / Main VT Sec'y |
| C/S Voltage Mag | CS VT Primary / CS VT Secondary |

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

### 25.19.2 CONFIRM CURRENT CONNECTIONS

1. Measure the current transformer secondary values for each input either by:
   a. reading from the device's HMI panel (providing it has first been verified by a secondary injection test)
   b. using a current clamp meter
2. Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control centre.
3. Ensure the current flowing in the neutral circuit of the current transformers is negligible.

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

### 25.19.3 ON-LOAD DIRECTIONAL TEST

This test ensures that directional overcurrent and fault locator functions have the correct forward/reverse response to fault and load conditions. For this test you must first know the actual direction of power flow on the system. If you do not already know this you must determine it using adjacent instrumentation or protection already in-service.

- For load current flowing in the Forward direction (power export to the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show positive power signing.
- For load current flowing in the Reverse direction (power import from the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show negative power signing.

*Note:*
*This check applies only for Measurement Modes 0 (default), and 2. This should be checked in the MEASURE'T SETUP column (**Measurement Mode** = 0 or 2). If measurement modes 1 or 3 are used, the expected power flow signing would be opposite to that shown above.*

In the event of any uncertainty, check the phase angle of the phase currents with respect to their phase voltage.

## 25.20 FINAL CHECKS

1. Remove all test leads and temporary shorting leads.
2. If you have had to disconnect any of the external wiring in order to perform the wiring verification tests, replace all wiring, fuses and links in accordance with the relevant external connection or scheme diagram.
3. The settings applied should be carefully checked against the required application-specific settings to ensure that they are correct, and have not been mistakenly altered during testing.
4. Ensure that all protection elements required have been set to `Enabled` in the *CONFIGURATION* column.
5. Ensure that the IED has been restored to service by checking that the ***Test Mode*** cell in the *COMMISSION TESTS* column is set to `Disabled`.
6. If the IED is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using the ***Reset All Values*** cell. If the required access level is not active, the device will prompt for a password to be entered so that the setting change can be made.
7. If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.
8. If a P991/MMLG test block is installed, remove the P992/MMLB test plug and replace the cover so that the protection is put into service.
9. Ensure that all event records, fault records, disturbance records, alarms and LEDs and communications statistics have been reset.

*Note:*
*Remember to restore the language setting to the customer's preferred language on completion.*

# 25.21 COMMMISSIONING THE P59X

If you are setting up a scheme, which involves a P59x device, you will need to commission the P59x too. The following instructions describe the commissioning procedure for a P59x.

## 25.21.1 VISUAL INSPECTION

**Warning:**
**Check the rating information under the top access cover on the front of the IED.**

**Warning:**
**Check that the IED being tested is correct for the line or circuit.**

**Warning:**
**Record the circuit reference and system details.**

**Warning:**
**Check the CT secondary current rating and record the CT tap which is in use.**

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

## 25.21.2 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

*Note:*
*The V.35 circuits and the X.21 circuits of the P592 and P593 respectively are isolated from all other circuits but are electrically connected to the outer case. The circuits must therefore not be insulation or impulse tested to the case.*

## 25.21.3 EXTERNAL WIRING

**Caution:**
**Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.**

### 25.21.4 P59X AUXILIARY SUPPLY

P591 devices operate from a DC auxiliary supply within the range of 19 V to 65 V for a 24 - 48 V version and 87.5 V to 300 V for a 110 - 250 V version.

P592 and P593 units operate from a DC auxiliary supply within the range of 19 V to 300 V.

Without energizing the device, measure the auxiliary supply to ensure it is within the operating range.

The devices are designed to withstand an AC ripple component of up to 15% of the normal DC auxiliary supply. However, in all cases the peak value of the DC supply must not exceed the maximum specified operating limit.

**Warning:**
**Do not energise the device or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.**

### 25.21.5 P59X LEDS

On power up the green ‘SUPPLY HEALTHY’ LED should be permanently illuminated, indicating that the device is healthy.

#### P592 only

The four red LEDs can be tested by appropriate setting of the DIL switches on the front plate. Set the data rate switch according to the communication channel bandwidth available. Set all other switches to 0. To illuminate the ‘DSR OFF’ and ‘CTS OFF’ LED’s, disconnect the V.35 connector from the rear of the P592 and set the ‘DSR’ and ‘CTS’ switches to ‘0’. The ‘OPTO LOOPBACK’ and ‘V.35 LOOPBACK’ LEDs can be illuminated by setting their corresponding switches to ‘1’.

Once operation of the LEDs has been established set all DIL switches, except for the ‘OPTO LOOPBACK’ switch, to ‘0’ and reconnect the V.35 connector.

#### P593 only

Set the ‘X.21 LOOPBACK’ switch to ‘ON’. The green ‘CLOCK’ and red ‘X.21 LOOPBACK’ LED’s should illuminate. Reset the ‘X.21 LOOPBACK’ switch to the ‘OFF’ position.

Set the ‘OPTO LOOPBACK’ switch to ‘ON’. The red ‘OPTO LOOPBACK’ LED should illuminate. Do not reset the “OPTO LOOPBACK’ switch as it is required in this position for the next test.

### 25.21.6 RECEIVED OPTICAL SIGNAL LEVEL

1. With an optical cable connected to the P54x optical transmitter, disconnect the other end of the cable from the P59x receiver (Rx) and use an optical power meter to measure the received signal strength. The value should be in the range -16.8 dBm to -25.4 dBm.
2. Record the measured value and replace the connector to the P59x receiver.

**Warning:**
**NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.**

### 25.21.7 OPTICAL TRANSMITTER LEVEL

1. Using an appropriate fibre-optic cable, connect the optical transmitter (Tx) to an optical power meter.
2. Check that the average power transmitted is within the range -16.8 dBm to -22.8 dBm.

3. Record the transmit power level.
4. Connect the appropriate optical fibre to connect the P591 transmitter to the IED's optical receiver
5. Return to the IED

## 25.21.8 LOOPBACK TEST

### P591

It is necessary to loop the transmitted electrical G.703 signal presented on terminals 3 and 4 of the P591 to the received signal presented on terminals 7 and 8.

If test links have been designed into the scheme to facilitate this they should be used. Alternatively, remove any external wiring from terminals 3, 4, 7 and 8 at the rear of each P591 unit. Loopback the G.703 signals on each device by connecting a wire link between terminals 3 and 7, and a second wire between terminals 4 and 8.

### P592

With the ‘OPTO LOOPBACK’ switch in the ‘1’ position, the receive and transmit optical ports are connected together. This allows the optical fibre communications between the IED and the P592 to be tested, but not the internal circuitry of the P592 itself.

### P593

Set the ‘OPTO LOOPBACK’ switch to ‘OFF’ and ‘X.21 LOOPBACK’ switch to ‘ON’ respectively. With the ‘X.21 LOOPBACK’ switch in this position the ‘Receive Data’ and ‘Transmit Data’ lines of the X.21 communication interface are connected together. This allows the optical fibre communications between the IED and the P593, and the internal circuitry of the P593 itself to be tested.

CHAPTER 26

# MAINTENANCE AND TROUBLESHOOTING

## 26.1 CHAPTER OVERVIEW

The Maintenance and Troubleshooting chapter provides details of how to maintain and troubleshoot products based on the Px4x and P40Agile platforms. Always follow the warning signs in this chapter. Failure to do so may result injury or defective equipment.

**Caution:**
**Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.**

The troubleshooting part of the chapter allows an error condition on the IED to be identified so that appropriate corrective action can be taken.

If the device develops a fault, it is usually possible to identify which module needs replacing. It is not possible to perform an on-site repair to a faulty module.

If you return a faulty unit or module to the manufacturer or one of their approved service centres, you should include a completed copy of the Repair or Modification Return Authorization (RMA) form.

This chapter contains the following sections:

Chapter Overview 629
Maintenance 630
Troubleshooting 638

# 26.2 MAINTENANCE

## 26.2.1 MAINTENANCE CHECKS

In view of the critical nature of the application, GE Vernova products should be checked at regular intervals to confirm they are operating correctly. GE Vernova products are designed for a life in excess of 20 years.

The devices are self-supervising and so require less maintenance than earlier designs of protection devices. Most problems will result in an alarm, indicating that remedial action should be taken. However, some periodic tests should be carried out to ensure that they are functioning correctly and that the external wiring is intact. It is the responsibility of the customer to define the interval between maintenance periods. If your organisation has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

Although some functionality checks can be performed from a remote location, these are predominantly restricted to checking that the unit is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. For this reason, maintenance checks should also be performed locally at the substation.

**Caution:**
**Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.**

### 26.2.1.1 ALARMS

First check the alarm status LED to see if any alarm conditions exist. If so, press the Read key repeatedly to step through the alarms.

After dealing with any problems, clear the alarms. This will clear the relevant LEDs.

### 26.2.1.2 OPTO-ISOLATORS

Check the opto-inputs by repeating the commissioning test detailed in the Commissioning chapter.

### 26.2.1.3 OUTPUT RELAYS

Check the output relays by repeating the commissioning test detailed in the Commissioning chapter.

### 26.2.1.4 MEASUREMENT ACCURACY

If the power system is energised, the measured values can be compared with known system values to check that they are in the expected range. If they are within a set range, this indicates that the A/D conversion and the calculations are being performed correctly. Suitable test methods can be found in Commissioning chapter.

Alternatively, the measured values can be checked against known values injected into the device using the test block, (if fitted) or injected directly into the device's terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

## 26.2.2 REPLACING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, you can replace either the complete device or just the faulty PCB, identified by the in-built diagnostic software.

If possible you should replace the complete device, as this reduces the chance of damage due to electrostatic discharge and also eliminates the risk of fitting an incompatible replacement PCB. However, we understand it may be difficult to remove an installed product and you may be forced to replace the faulty PCB on-site. The case and rear terminal blocks are designed to allow removal of the complete device, without disconnecting the scheme wiring.

**Caution:**
**Replacing PCBs requires the correct on-site environment (clean and dry) as well as suitably trained personnel.**

**Caution:**
**If the repair is not performed by an approved service centre, the warranty will be invalidated.**

**Caution:**
**Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.**

**Warning:**
**Before working at the rear of the device, isolate all voltage and current supplying it.**

*Note:*
*The current transformer inputs are equipped with integral shorting switches which will close for safety reasons, when the terminal block is removed.*

To replace the complete device:

1. Carefully disconnect the cables not connected to the terminal blocks (e.g. IRIG-B, fibre optic cables, earth), as appropriate, from the rear of the device.
2. Remove the terminal block screws using a magnetic screwdriver to minimise the risk of losing the screws or leaving them in the terminal block.
3. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
4. Remove the terminal block screws that fasten the device to the panel and rack. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.
5. Withdraw the device from the panel and rack. Take care, as the device will be heavy due to the internal transformers.
6. To reinstall the device, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the chassis ground, IRIG-B and fibre optic connections are replaced. The terminal blocks are labelled alphabetically with 'A' on the left hand side when viewed from the rear.

Once the device has been reinstalled, it should be re-commissioned as set out in the Commissioning chapter.

**Caution:**
**If the top and bottom access covers have been removed, some more screws with smaller diameter heads are made accessible. Do NOT remove these screws, as they secure the front panel to the device.**

*Note:*
*There are four possible types of terminal block: RTD/CLIO input, heavy duty, medium duty, and MiDOS. The terminal blocks are fastened to the rear panel with slotted or cross-head screws depending on the type of terminal block. Not all terminal block types are present on all products.*

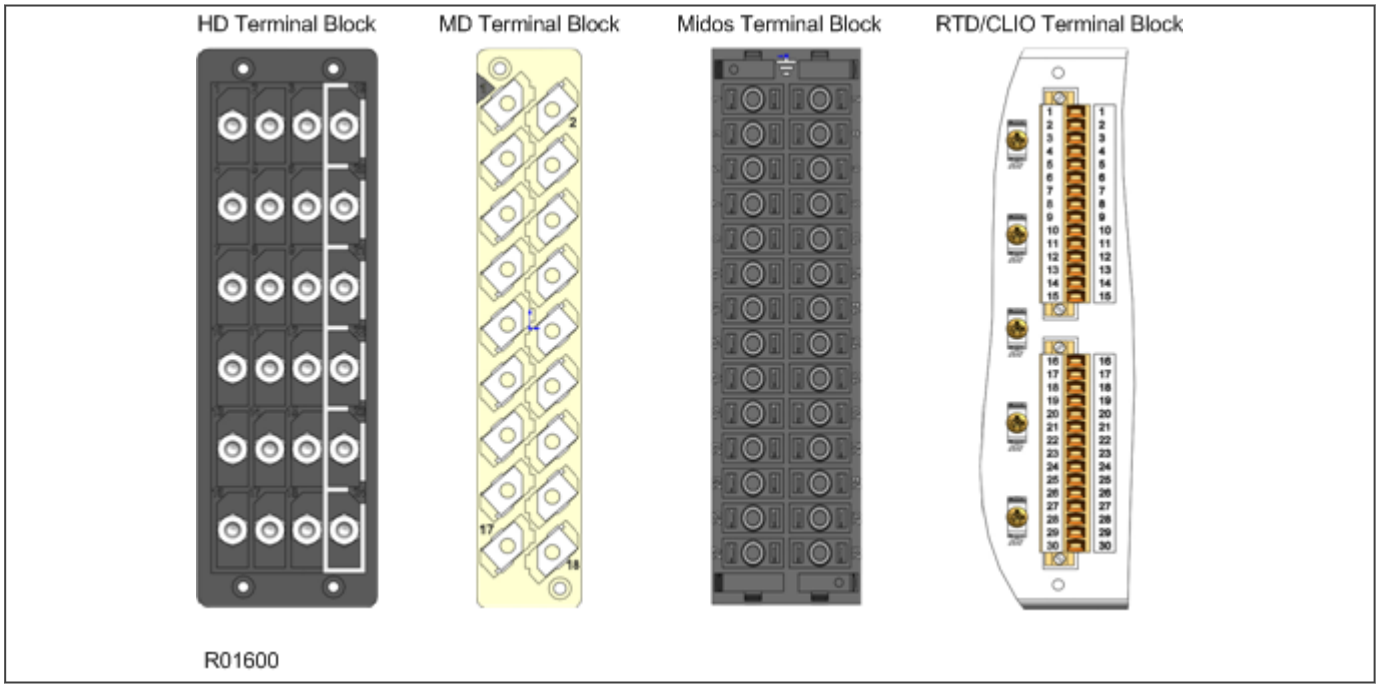



**Figure 303: Possible terminal block types**

## 26.2.3 REPAIRING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, either the complete unit or just the faulty PCB, identified by the in-built diagnostic software, should be replaced.

Replacement of printed circuit boards and other internal components must be undertaken by approved Service Centres. Failure to obtain the authorization of after-sales engineers prior to commencing work may invalidate the product warranty.

We recommend that you entrust any repairs to Automation Support teams, which are available world-wide.

## 26.2.4 REMOVING THE FRONT PANEL

**Warning:**
**Before removing the front panel to replace a PCB, you must first remove the auxiliary power supply and wait 5 seconds for the internal capacitors to discharge. You should also isolate voltage and current transformer connections and trip circuit.**

**Caution:**
**Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.**

To remove the front panel:

1. Open the top and bottom access covers. You must open the hinged access covers by more than 90° before they can be removed.
2. If fitted, remove the transparent secondary front cover.
3. Apply outward pressure to the middle of the access covers to bow them and disengage the hinge lug, so the access cover can be removed. The screws that fasten the front panel to the case are now accessible.
4. Undo and remove the screws. The 40TE case has four cross-head screws fastening the front panel to the case, one in each corner, in recessed holes. The 60TE/80TE cases have an additional two screws, one midway along each of the top and bottom edges of the front plate.
5. When the screws have been removed, pull the complete front panel forward to separate it from the metal case. The front panel is connected to the rest of the circuitry by a 64-way ribbon cable.
6. The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable and a plug with locking latches on the front panel. Gently push the two locking latches outwards which eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.

**Caution:**
**Do not remove the screws with the larger diameter heads which are accessible when the access covers are fitted and open. These screws hold the relay in its mounting (panel or cubicle).**

**Caution:**
**The internal circuitry is now exposed and is not protected against electrostatic discharge and dust ingress. Therefore ESD precautions and clean working conditions must be maintained at all times.**

## 26.2.5 REPLACING PCBS

1. To replace any of the PCBs, first remove the front panel.
2. Once the front panel has been removed, the PCBs are accessible. The numbers above the case outline identify the guide slot reference for each printed circuit board. Each printed circuit board has a label stating the corresponding guide slot number to ensure correct relocation after removal. To serve as a reminder of the slot numbering there is a label on the rear of the front panel metallic screen.
3. Remove the 64-way ribbon cable from the PCB that needs replacing
4. Remove the PCB in accordance with the board-specific instructions detailed later in this section.

*Note:*
*To ensure compatibility, always replace a faulty PCB with one of an identical part number.*

### 26.2.5.1 REPLACING THE MAIN PROCESSOR BOARD

The main processor board is situated in the front panel. This board contains application-specific settings in its non-volatile memory. You may wish to take a backup copy of these settings. This could save time in the re-commissioning process.

To replace the main processor board:

1. Remove front panel.
2. Place the front panel with the user interface face down and remove the six screws from the metallic screen, as shown in the figure below. Remove the metal plate.
3. Remove the screws that hold the main processor board in position.
4. Carefully disconnect the ribbon cable. Take care as this could easily be damaged by excessive twisting.
5. Replace the main processor board
6. Reassemble the front panel using the reverse procedure. Make sure the ribbon cable is reconnected to the main processor board and that all eight screws are refitted.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, carry out the standard commissioning procedure as defined in the Commissioning chapter.

*Note:*
*After replacing the main processor board, all the settings required for the application need to be re-entered. This may be done either manually or by downloading a settings file.*

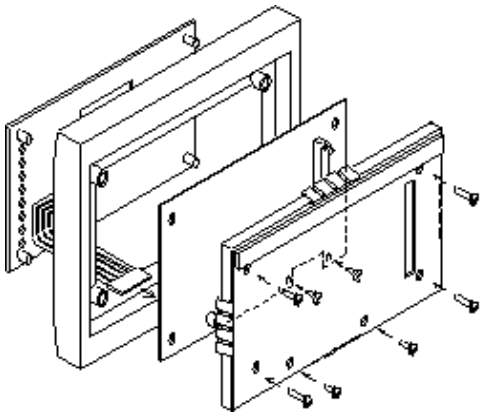



**Figure 304: Front panel assembly**

### 26.2.5.2 REPLACEMENT OF COMMUNICATIONS BOARDS

Most products will have at least one communications board of some sort fitted. There are several different boards available offering various functionality, depending on the application. Some products may even be fitted with two boards of different types.

To replace a faulty communications board:

1. Remove front panel.
2. Disconnect all connections at the rear.
3. The board is secured in the relay case by two screws, one at the top and another at the bottom. Remove these screws carefully as they are not captive in the rear panel.
4. Gently pull the communications board forward and out of the case.

5. Before fitting the replacement PCB check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
6. Fit the replacement PCB carefully into the correct slot. Make sure it is pushed fully back and that the securing screws are refitted.
7. Reconnect all connections at the rear.
8. Refit the front panel.
9. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
10. Once the unit has been reassembled, commission it according to the Commissioning chapter.

### 26.2.5.3 REPLACEMENT OF THE INPUT MODULE

Depending on the product, the input module consists of two or three boards fastened together and is contained within a metal housing. One board contains the transformers and one contains the analogue to digital conversion and processing electronics. Some devices have an additional auxiliary transformer contained on a third board.

To replace an input module:

1. Remove front panel.
2. The module is secured in the case by two screws on its right-hand side, accessible from the front, as shown below. Move these screws carefully as they are not captive in the front plate of the module.
3. On the right-hand side of the module there is a small metal tab which brings out a handle (on some modules there is also a tab on the left). Grasp the handle(s) and pull the module firmly forward, away from the rear terminal blocks. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
4. Remove the module from the case. The module may be heavy, because it contains the input voltage and current transformers.
5. Slot in the replacement module and push it fully back onto the rear terminal blocks. To check that the module is fully inserted, make sure the v-shaped cut-out in the bottom plate of the case is fully visible.
6. Refit the securing screws.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

**Caution:**
**With non-mounted IEDs, the case needs to be held firmly while the module is withdrawn. Withdraw the input module with care as it suddenly comes loose once the friction of the terminal blocks is overcome.**

*Note:*
*If individual boards within the input module are replaced, recalibration will be necessary. We therefore recommend replacement of the complete module to avoid on-site recalibration.*

### 26.2.5.4 REPLACEMENT OF THE POWER SUPPLY BOARD

**Caution:**
**Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.**

The power supply board is fastened to an output relay board with push fit nylon pillars. This doubled-up board is secured on the extreme left hand side, looking from the front of the unit.

1. Remove front panel.
2. Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
3. Separate the boards by pulling them apart carefully. The power supply board is the one with two large electrolytic capacitors.
4. Before reassembling the module, check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label
5. Reassemble the module with a replacement PCB. Push the inter-board connectors firmly together. Fit the four push fit nylon pillars securely in their respective holes in each PCB.
6. Slot the power supply module back into the housing. Push it fully back onto the rear terminal blocks.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

#### 26.2.5.5 REPLACEMENT OF THE I/O BOARDS

There are several different types of I/O boards, which can be used, depending on the product and application. Some boards have opto-inputs, some have relay outputs and others have a mixture of both.

1. Remove front panel.
2. Gently pull the board forward and out of the case
3. If replacing the I/O board, make sure the setting of the link above IDC connector on the replacement board is the same as the one being replaced.
4. Before fitting the replacement board check the number on the round label next to the front edge of the board matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
5. Carefully slide the replacement board into the appropriate slot, ensuring that it is pushed fully back onto the rear terminal blocks.
6. Refit the front panel.
7. Refit and close the access covers then press at the hinge assistance T-pieces so they click back into the front panel moulding.
8. Once the unit has been reassembled, commission it according to the Commissioning chapter.

### 26.2.6 RECALIBRATION

Recalibration is not needed when a PCB is replaced, unless it is one of the boards in the input module. If any of the boards in the input module is replaced, the unit must be recalibrated.

Although recalibration is needed when a board inside the input module is replaced, it is not needed if the input module is replaced in its entirety.

Although it is possible to carry out recalibration on site, this requires special test equipment and software. We therefore recommend that the work be carried out by the manufacturer, or entrusted to an approved service centre.

### 26.2.7 SUPERCAPACITOR DISCHARGED

The supercapacitor maintains charge for two weeks with the IED de-energised. When first energising the IED after this time there may be a Battery Alarm due to the supercapacitor voltage dropping below a pre-defined threshold.

The battery alarm will clear after approximately 30 minutes of IED being energised, and once cleared there will be enough charge in the supercapacitor to backup status data.

*Note:*
*Events, disturbance and maintenance records will be lost if the supercapacitor is fully discharged.*

### 26.2.8 CLEANING

**Warning:**
**Before cleaning the device, ensure that all AC and DC supplies and transformer connections are isolated, to prevent any chance of an electric shock while cleaning.**

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the product's surfaces and leave a conductive residue.

# 26.3 TROUBLESHOOTING

## 26.3.1 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

## 26.3.2 POWER-UP ERRORS

If the IED does not appear to power up, use the following to determine whether the fault is in the external wiring, auxiliary fuse, IED power supply module or IED front panel.

| Test | Check | Action |
|---|---|---|
| 1 | Measure the auxiliary voltage on terminals 1 and 2. Verify the voltage level and polarity against the rating label on the front.<br>Terminal 1 is –dc, 2 is +dc | If the auxiliary voltage is correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply. |
| 2 | Check the LEDs and LCD backlight switch on at power-up. Also check the N/O (normally open) watchdog contact for closing. | If the LEDs and LCD backlight switch on, or the contact closes and no error code is displayed, the error is probably on the main processor board in the front panel.<br>If the LEDs and LCD backlight do not switch on and the contact does not close, go to test 3. |
| 3 | Check the output (nominally 48 V DC). | If there is no field voltage, the fault is probably in the IED power supply module. |

## 26.3.3 ERROR MESSAGE OR CODE ON POWER-UP

The IED performs a self-test during power-up. If it detects an error, a message appears on the LCD and the power-up sequence stops. If the error occurs when the IED application software is running, a maintenance record is created and the device reboots.

| Test | Check | Action |
|---|---|---|
| 1 | Is an error message or code permanently displayed during power up? | If the IED locks up and displays an error code permanently, go to test 2.<br>If the IED prompts for user input, go to test 4.<br>If the IED reboots automatically, go to test 5. |
| 2 | Record displayed error, and then remove and re-apply IED auxiliary supply. | Record whether the same error code is displayed when the IED is rebooted. If no error code is displayed, contact the local service centre stating the error code and IED information. If the same code is displayed, go to test 3. |

| Test | Check | Action |
|---|---|---|
| 3 | Error Code Identification<br>The following text messages (in English) are displayed if a fundamental problem is detected, preventing the system from booting:<br>Bus Fail – address lines<br>SRAM Fail – data lines<br>FLASH Fail format error<br>FLASH Fail checksum<br>Code Verify Fail<br>The following hex error codes relate to errors detected in specific IED modules: | These messages indicate that a problem has been detected on the IED's main processor board in the front panel. |
| 3.1 | 0c140005/0c0d0000 | Input Module (including opto-isolated inputs) |
| 3.2 | 0c140006/0c0e0000 | Output IED boards |
| 3.3 | The last four digits provide details on the actual error. | Other error codes relate to hardware or software problems on the main processor board. Contact GE Vernova with details of the problem for a full analysis. |
| 4 | The IED displays a message for corrupt settings and prompts for the default values to be restored for the affected settings. | The power-up tests have detected corrupted IED settings. Restore the default settings to allow the power-up to complete, and then reapply the application-specific settings. |
| 5 | The IED resets when the power-up is complete. A record error code is displayed | Error 0x0E080000, programmable scheme logic error due to excessive execution time. If the IED powers up successfully, check the programmable logic for feedback paths.<br>Other error codes relate to software errors on the main processor board. |

## 26.3.4 OUT OF SERVICE LED ON AT POWER-UP

| Test | Check | Action | |
|---|---|---|---|
| 1 | Using the IED menu, confirm the Commission Test or Test Mode setting is Enabled. If it is not Enabled, go to test 2. | If the setting is Enabled, disable the test mode and make sure the Out of Service LED is OFF. | |
| 2 | Select the *VIEW RECORDS* column then view the last maintenance record from the menu. | Check for the H/W Verify Fail maintenance record. This indicates a discrepancy between the IED model number and the hardware. Examine the ***Maint Data***; cell. This indicates the causes of the failure using bit fields:<br>Bit Meaning | |
| | | 0 | The application type field in the model number does not match the software ID |
| | | 1 | The application field in the model number does not match the software ID |
| | | 2 | The variant 1 field in the model number does not match the software ID |
| | | 3 | The variant 2 field in the model number does not match the software ID |
| | | 4 | The protocol field in the model number does not match the software ID |

| Test | Check | Action | |
|---|---|---|---|
| | | 5 | The language field in the model number does not match the software ID |
| | | 6 | The VT type field in the model number is incorrect (110 V VTs fitted) |
| | | 7 | The VT type field in the model number is incorrect (440 V VTs fitted) |
| | | 8 | The VT type field in the model number is incorrect (no VTs fitted) |

## 26.3.5 ERROR CODE DURING OPERATION

The IED performs continuous self-checking. If the IED detects an error it displays an error message, logs a maintenance record and after a short delay resets itself. A permanent problem (for example due to a hardware fault) is usually detected in the power-up sequence. In this case the IED displays an error code and halts. If the problem was transient, the IED reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

## 26.3.6 MAL-OPERATION DURING TESTING

### 26.3.6.1 FAILURE OF OUTPUT CONTACTS

An apparent failure of the relay output contacts can be caused by the configuration. Perform the following tests to identify the real cause of the failure. The self-tests verify that the coils of the output relay contacts have been energized. An error is displayed if there is a fault in the output relay board.

| Test | Check | Action |
|---|---|---|
| 1 | Is the Out of Service LED ON? | If this LED is ON, the relay may be in test mode or the protection has been disabled due to a hardware verify error. |
| 2 | Examine the Contact status in the Commissioning section of the menu. | If the relevant bits of the contact status are operated, go to test 4; if not, go to test 3. |
| 3 | Examine the fault record or use the test port to check the protection element is operating correctly. | If the protection element does not operate, check the test is correctly applied.<br>If the protection element operates, check the programmable logic to make sure the protection element is correctly mapped to the contacts. |
| 4 | Using the Commissioning or Test mode function, apply a test pattern to the relevant relay output contacts. Consult the correct external connection diagram and use a continuity tester at the rear of the relay to check the relay output contacts operate. | If the output relay operates, the problem must be in the external wiring to the relay. If the output relay does not operate the output relay contacts may have failed (the self-tests verify that the relay coil is being energized). Ensure the closed resistance is not too high for the continuity tester to detect. |

### 26.3.6.2 FAILURE OF OPTO-INPUTS

The opto-isolated inputs are mapped onto the IED's internal DDB signals using the programmable scheme logic. If an input is not recognised by the scheme logic, use the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column to check whether the problem is in the opto-input itself, or the mapping of its signal to the scheme logic functions.

If the device does not correctly read the opto-input state, test the applied signal. Verify the connections to the opto-input using the wiring diagram and the nominal voltage settings in the *OPTO CONFIG* column. To do this:

1. Select the nominal voltage for all opto-inputs by selecting one of the five standard ratings in the ***Global Nominal V*** cell.
2. Select `Custom` to set each opto-input individually to a nominal voltage.
3. Using a voltmeter, check that the voltage on its input terminals is greater than the minimum pick-up level (See the Technical Specifications chapter for opto pick-up levels).

If the signal is correctly applied, this indicates failure of an opto-input, which may be situated on standalone opto-input board, or on an opto-input board that is part of the input module. Separate opto-input boards can simply be replaced. If, however, the faulty opto-input board is part of the input module, the complete input module should be replaced. This is because the analogue input module cannot be individually replaced without dismantling the module and recalibration of the IED.

#### 26.3.6.3 INCORRECT ANALOGUE SIGNALS

If the measured analogue quantities do not seem correct, use the measurement function to determine the type of problem. The measurements can be configured in primary or secondary terms.

1. Compare the displayed measured values with the actual magnitudes at the terminals.
2. Check the correct terminals are used.
3. Check the CT and VT ratios set are correct.
4. Check the phase displacement to confirm the inputs are correctly connected.

### 26.3.7 COPROCESSOR BOARD FAILURES

If a coprocessor board is used, this may cause the IED to report one or more of the following alarms:

- Signalling failure alarm (on its own)
- C diff failure (on its own)
- Signalling failure and C diff failure together
- Incompatible IED
- Comms changed
- IEEE C37.94 fail

#### 26.3.7.1 SIGNALLING FAILURE ALARM (ON ITS OWN)

This indicates that there is a problem with one of the fibre-optic signalling channels. This alarm can occur in dual redundant or three terminal schemes. The fibre may have been disconnected, the device may have been incorrectly configured at one of the ends, or there is a problem with the communications equipment. Further information about the status of the signalling channels can be found in *MEASUREMENTS 4* column.

#### 26.3.7.2 C DIFF FAILURE ALARM (ON ITS OWN)

This indicates there is a problem with the Coprocessor board. As a result the current differential/distance protection is not available and backup protection will operate, if configured to do so. Further information can be found in the maintenance records.

#### 26.3.7.3 SIGNALLING FAILURE AND C DIFF FAILURE ALARMS TOGETHER

This indicates that there is a problem with one or both fibre-optic signalling channels. The fibre may have been disconnected, the device may have been incorrectly configured at one of the ends, or there is a problem with the communications equipment. As a result the current differential protection is not available and backup protection will operate, if configured to do so. Further information about the status of the signalling channels can be found in *MEASUREMENTS 4* column.

#### 26.3.7.4 INCOMPATIBLE IED

This occurs if the IEDs trying to communicate with each other are of incompatible types.

#### 26.3.7.5 COMMS CHANGED

This indicates that the ***Comms Mode*** setting has been changed without a subsequent power off and on.

#### 26.3.7.6 IEEE C37.94 FAIL

This indicates a Signal Lost, a Path Yellow (indicating a fault on the communications channel) or a mismatch in the number of N*64 channels used on either channel 1 or channel 2. Further information can be found in the *MEASUREMENTS 4* column.

### 26.3.8 PSL EDITOR TROUBLESHOOTING

A failure to open a connection could be due to one or more of the following:

- The IED address is not valid (this address is always 1 for the front port)
- Password in not valid
- Communication set-up (COM port, Baud rate, or Framing) is not correct
- Transaction values are not suitable for the IED or the type of connection
- The connection cable is not wired correctly or broken
- The option switches on any protocol converter used may be incorrectly set

#### 26.3.8.1 DIAGRAM RECONSTRUCTION

Although a scheme can be extracted from an IED, a facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals are drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B. Any annotation added to the original diagram such as titles and notes are lost.

Sometimes a gate type does not appear as expected. For example, a single-input AND gate in the original scheme appears as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 also appear as OR gates

#### 26.3.8.2 PSL VERSION CHECK

The PSL is saved with a version reference, time stamp and CRC check (Cyclic Redundancy Check). This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

### 26.3.9 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Return Authorization (RMA) form
   An electronic version of the RMA form is available from the following:
   GA.support@gevernova.com
2. Fill in the RMA form
   Fill in only the white part of the form.
   Please ensure that all fields marked **(M)** are completed such as:
   - Equipment model
   - Model No. and Serial No.

- Description of failure or modification required (please be specific)
- Value for customs (in case the product requires export)
- Delivery and invoice addresses
- Contact details

3. Send the RMA form to your local contact
   For a list of local service contacts worldwide, email us at:
   GA.support@gevernova.com
4. The local service contact provides the shipping information
   Your local service contact provides you with all the information needed to ship the product:
   - Pricing details
   - RMA number
   - Repair centre address

   If required, an acceptance of the quote must be delivered before going to the next stage.
5. Send the product to the repair centre
   - Address the shipment to the repair centre specified by your local contact
   - Make sure all items are packaged in an anti-static bag and foam protection
   - Make sure a copy of the import invoice is attached with the returned unit
   - Make sure a copy of the RMA form is attached with the returned unit
   - E-mail or fax a copy of the import invoice and airway bill document to your local contact.

CHAPTER 27

# TECHNICAL SPECIFICATIONS

## 27.1 CHAPTER OVERVIEW

This chapter describes the technical specifications of the product.

This chapter contains the following sections:

Chapter Overview 645
Interfaces 646
Protection Functions 651
Monitoring, Control and Supervision 657
Measurements and Recording 659
Ratings 660
Input/Output Connections 663
Mechanical Specifications 665
Type Tests 666
Environmental Conditions 667
Electromagnetic Compatibility 668
Regulatory Compliance 671

# 27.2 INTERFACES

## 27.2.1 FRONT USB PORT

| Front USB port | |
|---|---|
| Use | For local connection to laptop for configuration purposes and firmware downloads |
| Connector | USB type B |
| Isolation | Isolation to ELV level |
| Constraints | Maximum cable length 5 m |

## 27.2.2 REAR SERIAL PORT 1

| Rear serial port 1 (RP1) | |
|---|---|
| Use | For SCADA communications (multi-drop) |
| Standard | EIA(RS)485, K-bus |
| Connector | General purpose block, M4 screws (2 wire) |
| Cable | Screened twisted pair (STP) |
| Supported Protocols * | Courier, IEC-60870-5-103, DNP3.0, MODBUS |
| Isolation | Isolation to SELV level |
| Constraints | Maximum cable length 1000 m |

* Not all models support all protocols - see ordering options

## 27.2.3 FIBRE REAR SERIAL PORT 1

| Optional fibre rear serial port (RP1) | |
|---|---|
| Main Use | Serial SCADA communications over fibre |
| Connector | IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx) |
| Fibre type | Multimode 50/125 µm or 62.5/125 µm |
| Supported Protocols | Courier, IEC870-5-103, DNP 3.0, MODBUS |
| Wavelength | 850 nm |

## 27.2.4 REAR SERIAL PORT 2

| Optional rear serial port (RP2) | |
|---|---|
| Use | For SCADA communications (multi-drop) |
| Standard | EIA(RS)485, K-bus, EIA(RS)232 |
| Designation | SK4 |
| Connector | 9 pin D-type female connector |
| Cable | Screened twisted pair (STP) |
| Supported Protocols | Courier |
| Isolation | Isolation to SELV level |
| Constraints | Maximum cable length 1000 m for RS485 and K-bus, 15 m for RS232 |

### 27.2.5 OPTIONAL REAR SERIAL PORT (SK5)

| Optional rear serial port for teleprotection | |
|---|---|
| Use | For teleprotection in distance products |
| Standard | EIA(RS)232 |
| Designation | SK5 |
| Connector | 9 pin D-type female connector |
| Cable | Screened twisted pair (STP) |
| Supported Protocols | InterMiCOM (IM) |
| Isolation | Isolation to SELV level |
| Constraints | Maximum cable length 15 m |

### 27.2.6 IRIG-B (DEMODULATED)

| IRIG-B Interface (Demodulated) | |
|---|---|
| Use | External clock synchronisation signal |
| Standard | IRIG 200-98 format B00X |
| Connector | BNC |
| Cable type | 50 ohm coaxial |
| Isolation | Isolation to SELV level |
| Input signal | TTL level |
| Input impedance | 10 k ohm at dc |
| Accuracy | +/- 1 ms |

### 27.2.7 IRIG-B (MODULATED)

| IRIG-B Interface (Modulated) | |
|---|---|
| Use | External clock synchronisation signal |
| Standard | IRIG 200-98 format B12X |
| Connector | BNC |
| Cable type | 50 ohm coaxial |
| Isolation | Isolation to SELV level |
| Input signal | Peak to peak, 200 mV to 20 mV |
| Input impedance | 6 k ohm at 1000 Hz |
| Accuracy | +/- 1 ms |

### 27.2.8 REAR ETHERNET PORT COPPER

| Rear Ethernet Port Using CAT 5/6/7 Wiring | |
|---|---|
| Main Use | Substation Ethernet communications |
| Standard | IEEE 802.3 100BaseTX |
| Connector | RJ45 |
| Cable type | Screened twisted pair (STP) |
| Isolation | 1.5 kV |

| Rear Ethernet Port Using CAT 5/6/7 Wiring | |
|---|---|
| Supported Protocols | IEC 61850 |
| Constraints | Maximum cable length 100 m |

## 27.2.9 REAR ETHERNET PORT FIBRE (HARDWARE OPTION (R/S/T)

| Rear Ethernet Port Using Fibre-optic Cabling | |
|---|---|
| Main Use | Substation Ethernet communications |
| Connector | IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx) |
| Standard | IEEE 802.3 100 BaseFX |
| Fibre type | Multimode 50/125 µm or 62.5/125 µm |
| Supported Protocols | IEC 61850 |
| Optional Redundancy Protocols Supported | PRP (Parallel Redundancy Protocol)<br>HSR (High-availability Seamless Redundancy)<br>RSTP (Rapid Spanning Tree Protocol)<br>Failover |
| Wavelength | 1300 nm |

### 27.2.9.1 100 BASE FX RECEIVER CHARACTERISTICS

| Parameter | Sym | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Optical Power Minimum at Window Edge | PIN Min. (W) | | -33.5 | –31 | dBm avg. |
| Input Optical Power Minimum at Eye Center | PIN Min. (C) | | -34.5 | -31.8 | Bm avg. |
| Input Optical Power Maximum | PIN Max. | -14 | -11.8 | | dBm avg. |

Conditions: TA = 0°C to 70°C

### 27.2.9.2 100 BASE FX TRANSMITTER CHARACTERISTICS

| Parameter | Sym | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Output Optical Power BOL 62.5/125 µm NA = 0.275 Fibre EOL | PO | -19<br>-20 | -16.8 | -14 | dBm avg. |
| Output Optical Power BOL 50/125 µm NA = 0.20 Fibre EOL | PO | -22.5<br>-23.5 | -20.3 | -14 | dBm avg. |
| Optical Extinction Ratio | | | | 10<br>-10 | %<br>dB |
| Output Optical Power at Logic "0" State | PO | | | -45 | dBm avg. |

Conditions: TA = 0°C to 70°C

## 27.2.10 REAR ETHERNET PORT FIBRE (HARDWARE OPTION U/W/Y)

| Rear Ethernet Port Using Fibre-optic Cabling | |
|---|---|
| Main Use | Substation Ethernet communications |
| Connector | IEC 874-10 BFOC 2.5 - (LC®) (1 each for Tx and Rx) |
| Standard | IEEE 802.3 100 BaseFX |

| Rear Ethernet Port Using Fibre-optic Cabling | |
|---|---|
| Fibre type | Multimode 50/125 µm (OM2 or OM3) or 62.5/125 µm (OM1) |
| Supported Protocols | Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog |
| Redundancy Protocols Supported | PRP (Parallel Redundancy Protocol)<br>HSR (High-availability Seamless Redundancy)<br>RSTP (Rapid Spanning Tree Protocol)<br>Failover |
| Wavelength | 1310 nm |

#### 27.2.10.1 100 BASE FX RECEIVER CHARACTERISTICS

| Parameter | Sym | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Optical Power Minimum at Window Edge | PIN Min. (W) | -31.0 | | -12.0 | dBm avg. |
| Input Optical Power Minimum at Eye Center | PIN Min. (C) | | -34.5 | -31.8 | Bm avg. |
| Input Optical Power Maximum | PIN Max. | -14 | -11.8 | | dBm avg. |

Conditions: TA = 0°C to 70°C

#### 27.2.10.2 100 BASE FX TRANSMITTER CHARACTERISTICS

| Parameter | Sym | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Output Optical Power BOL 62.5/125 µm NA = 0.275 Fibre EOL | PO | -20 | -17.0 | -14.0 | dBm avg. |
| Output Optical Power BOL 50/125 µm NA = 0.20 Fibre EOL | PO | -24.0 | -21.0 | -17.0 | dBm avg. |
| Optical Extinction Ratio | ER | 10 | | | dB |
| Output Optical Power at Logic "0" State | $P_{O(off)}$ | | | -45 | dBm avg. |

Conditions: TA = 0°C to 70°C

### 27.2.11 1 PPS PORT

| 1 PPS port (fibre) | |
|---|---|
| Main Use | GPS accuracy clock reference |
| Connector | BFOC 2.5 –(ST®) |
| Standard | IEC 874-10 |
| Fibre type | Multimode 50/125 µm or 62.5/125 µm |
| Wavelength | 850 nm |
| Minimum reception level | -28 dBm |
| Accuracy | Better than +/- 50 ns for maximum absolute error between actual GPS time and rising edge of 1 PPS signal. |

### 27.2.12 FIBRE TELEPROTECTION INTERFACE

| ibre Teleprotection Interface | |
|---|---|
| Main Use | Teleprotection communications |

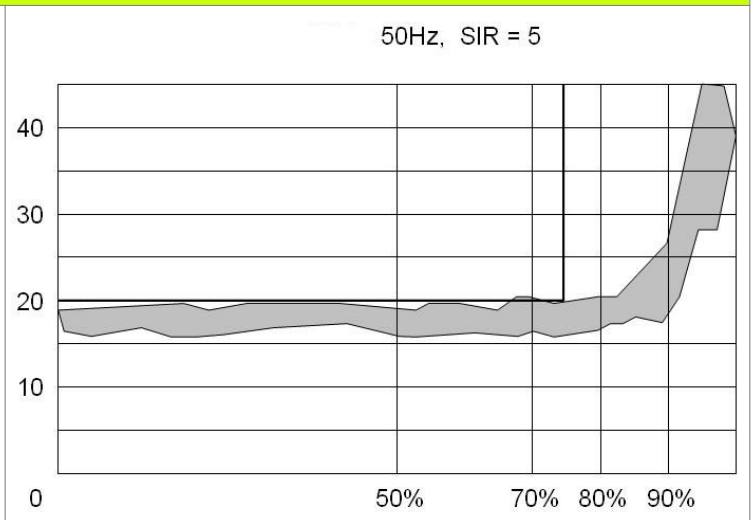
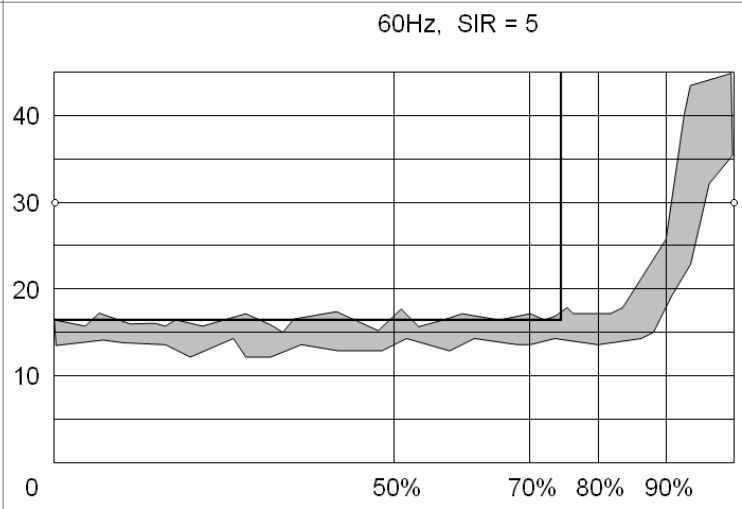
| ibre Teleprotection Interface | |
|---|---|
| Connectors (2) | BFOC 2.5 –(ST®) |
| Standard | IEC 874-10 |
| Protocol | InterMicom 64 |
| Fibre type | Multimode 50/125 µm or 62.5/125 µm or single-mode 9/125 µm |
| Wavelength | 850 nm or 1300 nm (multimode), 1300 nm or 1500 nm (single mode) |
| Minimum reception level | -28 dBm |
| Accuracy | Better than +/- 50 ns for maximum absolute error between actual GPS time and rising edge of 1 PPS signal. |

## Optical budget

| | 850nm MM | 1300 nm MM | 1300 nm SM | 1550 nm SM |
|---|---|---|---|---|
| Minimum transmit output level (average power) | -19.8 dBm | -6 dBm | -6 dBm | -6 dBm |
| Receiver sensitivity (average power) | -25.4 dBm | -49 dBm | -49 dBm | -49 dBm |
| Optical budget | 5.6 dB | 43 dB | 43 dB | 43 dB |
| Less safety margin (3 dB) | 2.6 dB | 40 dB | 40 dB | 40 dB |
| Typical cable loss | 2.6 dB/km | 0.8 dB/km | 0.4 dB/km | 0.3 dB/km |
| Maximum transmission distance | 1 km | 50 km | 100 km | 130 km |

# 27.3 PROTECTION FUNCTIONS

## 27.3.1 DISTANCE PROTECTION

| Tripping characteristics P44xxxxxxxAxxxQ Subcycle Transmission Distance | |
|---|---|
| Operating time versus reach percentage, for faults close to line angle.<br><br>50 Hz, SIR = 5<br><br>All quoted operating times include closure of the trip output contact |  |
| Operating time versus reach percentage, for faults close to line angle.<br><br>60 Hz, SIR = 5<br><br>All quoted operating times include closure of the trip output contact |  |
| Operating time for resistive faults > 20% inside the characteristic | 50 Hz, up to SIR = 30 < 30 ms<br>60 Hz, up to SIR = 30 < 25 ms |

| Accuracy | |
|---|---|
| Characteristic shape, up to SIR = 30 | +/- 5% for on-angle fault (on the set line angle)<br>+/- 10% for off-angle fault<br>Example: For a 70 degree set line angle, injection testing at 40 degrees would be referred to as "off-angle". |
| Zone time delay deviations | +/- 20 ms or 2%, whichever is greater |

### 27.3.2 POWER SWING BLOCKING

| Accuracy | |
|---|---|
| Accuracy of zones and timers | As per Distance |

### 27.3.3 OUT OF STEP PROTECTION

| Accuracy | |
|---|---|
| Accuracy of zones and timers | As per Distance |
| Operating range | Up to 7 Hz |

### 27.3.4 FIBRE TELEPROTECTION TRANSFER TIMES

The table below shows the minimum and maximum transfer time for InterMiCOM64 (IM64). The times are measured from opto initialization (with no opto filtering) to relay standard output and include a small propagation delay for back-back test.

IDiff IM64 indicates InterMiCOM64 signals working in conjunction with the differential protection fibre optic communications channel. IM64 indicates InterMiCOM64 signals working as a standalone feature.

| Configuration | Signals | Permissive Op Times (ms) | Direct Op Times (ms) | MaxCh1 Prop Delay Measured |
|---|---|---|---|---|
| IM64 at 56kbps | 8 | 18-21 | 21-24 | 1.6ms |
| IM64 at 64kbps | 8 | 18-21 | 21-24 | 1.3ms |
| IM64 at 128kbps | 24 | 17-20 | 20-23 | 1.4ms |
| IDiff IM64 at 56kbps | 8 | 24-26 | 29-31 | 3.3ms |
| IDiff IM64 at 64kbps | 8 | 24-26 | 29-31 | 2.9ms |
| IDiff IM64 at 128kbps | 32 | 20-26 | 24-31 | 1.9ms |

### 27.3.5 AUTORECLOSE AND CHECK SYNYCHRONISM

| Accuracy | |
|---|---|
| Timers | +/- 20 ms or 2%, whichever is greater |

### 27.3.6 PHASE OVERCURRENT PROTECTION

| Accuracy | |
|---|---|
| IDMT pick-up | 1.05 x Setting +/-5% |
| DT pick-up | Setting +/-5% |
| Drop-off (IDMT and DT) | 0.95 x setting +/-5% |
| IDMT operate | +/-5% of expected operating time or 40 ms, whichever is greater* |
| IEEE reset | +/-5% or 40 ms, whichever is greater** |
| DT operate time | +/-2% of setting or 60 ms, whichever is greater (Non Directional)**<br>+/-2% of setting or 60 ms, whichever is greater (Directional) |
| DT reset | Setting +/-5% |
| Repeatability | <5% |
| Characteristic UK | IEC 60255-151: 2009 |

| Accuracy | |
|---|---|
| Characteristic US | IEEE C37.112 1996 |

*Note:*
**Reference conditions: TMS = 1, TD = 7, I> = 1A, operating range = 2-20In*
***Reference conditions: Injected value is 2 x pick-up value.*

#### 27.3.6.1 TRANSIENT OVERREACH AND OVERSHOOT

| | |
|---|---|
| Additional tolerance due to increasing X/R ratios | +/-5% over the X/R ratio of 1 to 90 |
| Overshoot of overcurrent elements | < 30 ms |

#### 27.3.6.2 PHASE OVERCURRENT DIRECTIONAL PARAMETERS

| Accuracy | |
|---|---|
| Directional boundary pickup (RCA +/-90%) | +/-2° |
| Directional boundary hysteresis | < 2° |
| Directional boundary repeatability | <2% |

### 27.3.7 EARTH FAULT PROTECTION

| Accuracy | |
|---|---|
| IDMT pick-up | 1.05 x Setting +/-5% |
| DT pick-up | Setting +/-5%, or 20 mA, whichever is greater |
| Drop-off (IDMT and DT) | 0.9 x setting +/-5% |
| IDMT Operate | +/-5% or 40 ms, whichever is greater* |
| IEEE reset | +/-10% or 40 ms, whichever is greater |
| Repeatability | < 5% |
| DT operate | +/-2% or 50 ms, whichever is greater |
| DT reset | +/- 5% or 50 ms, whichever is greater |

*Note:*
*Reference conditions: TMS = 1, TD = 1, IN> = 1A, operating range = 2-20In.*

#### 27.3.7.1 EARTH FAULT DIRECTIONAL PARAMETERS

| Zero Sequence Polarising accuracy | |
|---|---|
| Directional boundary pick-up (RCA +/- 90°) | +/-2° |
| Hysteresis | <3° |
| VN> pick-up | Setting+/-10% |
| VN> drop-off | 0.9 x Setting +/-10% |

| Negative Sequence Polarising accuracy | |
|---|---|
| Directional boundary pick-up (RCA +/- 90°) | +/-2° |

| Negative Sequence Polarising accuracy | |
|---|---|
| Hysteresis | <3° |
| VN2> pick-up | Setting+/-10% |
| VN2> drop-off | 0.9 x Setting +/-10% |
| IN2> pick-up | Setting+/-10% |
| IN2> drop-off | 0.9 x Setting +/-10% |

## 27.3.8 SENSITIVE EARTH FAULT PROTECTION

| | |
|---|---|
| IDMT pick-up | 1.05 x Setting +/-5% |
| DT Pick-up | Setting +/- 5% |
| Drop-off (IDMT + DT) | 0.95 x Setting +/-5% |
| IDMT operate | +/- 5% or 70 ms, whichever is greater (1.05 - 2) Is<br>+/- 5% or 40 ms, whichever is greater (2 - 20) Is |
| DT operate | +/- 2% or 70 ms, whichever is greater (1.05 - 2) Is<br>+/- 2% or 50 ms, whichever is greater (2 - 20) Is |
| DT reset | Setting +/- 5% or 50 ms, whichever is greater |
| Repeatability | < 5% |

*Note:*
*SEF claims apply to SEF input currents of no more than 2 x In. For input ranges above 2 x In, the claim is not supported.*

### 27.3.8.1 SENSITIVE EARTH FAULT PROTECTION DIRECTIONAL ELEMENT

| Wattmetric SEF | |
|---|---|
| Pick-up P = 0 W | ISEF > +/-5% or 5 mA |
| Pick-up P > 0 W | P > +/-5% |
| Drop-off P = 0 W | 0.95 x ISEF> +/- 5% or 5 mA |
| Drop-off P > 0 W | 0.9 x P> +/- 5% or 5 mA |
| Boundary accuracy | +/-5% with hysteresis < 1° |
| Repeatability | < 1% |

## 27.3.9 RESTRICTED EARTH FAULT PROTECTION

| Low Impedance REF | |
|---|---|
| Pick-up | Setting formula +/- 5% |
| Drop-off | 0.8 x Setting formula +/-5% |
| Operating time | < 60 ms |
| Repeatability | < 5% |

| High Impedance REF | |
|---|---|
| High set pick-up | Setting +/- 10% |
| High set operating time | < 30 ms |
| Repeatability | < 5% |

## 27.3.10 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

| | |
|---|---|
| IDMT pick-up | 1.05 x Setting +/-5% |
| DT pick-up | Setting +/- 5% |
| Drop-off (IDMT and DT) | 0.95 x Setting +/-5% |
| IDMT operate | +/- 5% or 40 ms, whichever is greater |
| DT operate | +/- 2% or 60 ms, whichever is greater |
| DT Reset | Setting +/- 5% |

### 27.3.10.1 NPSOC DIRECTIONAL PARAMETERS

| | |
|---|---|
| Directional boundary pick-up (RCA +/-90%) | +/-2° |
| Directional boundary hysteresis | < 1° |
| Directional boundary repeatability | < 1% |

## 27.3.11 CIRCUIT BREAKER FAIL AND UNDERCURRENT PROTECTION

| | |
|---|---|
| I< Pick-up | Setting +/- 10% or 0.025 In, whichever is greater |
| I< Drop-off | Setting +/- 5% or 20 mA, whichever is greater |
| Operate time | < 12 ms |
| Timers | +/- 2% or 20 ms, whichever is greater |
| Reset time | < 15 ms |

## 27.3.12 BROKEN CONDUCTOR PROTECTION

| | |
|---|---|
| Pick-up | Setting +/- 2.5% |
| Drop-off | 0.95 x Setting +/- 2.5% |
| DT operate | +/- 2% or 40 ms, whichever is greater |
| Reset time | <25 ms |

## 27.3.13 THERMAL OVERLOAD PROTECTION

| | |
|---|---|
| Thermal alarm pick-up | Calculated trip time +/- 10% |
| Thermal overload pick-up | Calculated trip time +/- 10% |
| Cooling time accuracy | +/- 15% of theoretical |
| Repeatability | <5% |

*Note:*
*Operating time measured with applied current of 20% above thermal setting.*

# 27.4 MONITORING, CONTROL AND SUPERVISION

## 27.4.1 VOLTAGE TRANSFORMER SUPERVISION

| | |
|---|---|
| Fast block operation | < 1 cycle |
| Fast block reset | < 1.5 cycles |
| Time delay | +/- 2% or 20 ms, whichever is greater |

## 27.4.2 STANDARD CURRENT TRANSFORMER SUPERVISION

| | |
|---|---|
| IN> Pick-up | Setting +/- 5% |
| VN< Pick-up | Setting +/- 5% |
| IN> Drop-off | 0.9 x setting +/- 5% |
| VN< Drop-off | 1.05 x setting +/-5% or 1 V, whichever is greater |
| Time delay operation | Setting +/-2% or 30 ms, whichever is greater |
| CTS block operation | < 1 cycle |
| CTS reset | < 35 ms |

## 27.4.3 DIFFERENTIAL CURRENT TRANSFORMER SUPERVISION

| Accuracy | |
|---|---|
| I1> Pick-up | Setting +/- 5% |
| I1> Drop-off | 0.9 x setting +/- 5% |
| I2/I1> Pick-up | Setting +/- 5% |
| I2/I1> Drop-off | 0.9 x setting +/-5% |
| I2/I1>> Pick-up | Setting +/- 5% |
| I2/I1 >> Drop-off | 0.9 x setting +/-5% |
| Time delay operation | Setting +/-2% or 20 ms, whichever is greater |
| CTS block diff operation | < 1 cycle |
| CTS reset | < 35 ms |

## 27.4.4 CB STATE AND CONDITION MONITORING

| Accuracy | |
|---|---|
| Timers | +/- 40 ms or 2%, whichever is greater |
| Broken current accuracy | +/- 5% |
| Reset time | < 30 ms |

### 27.4.5 PSL TIMERS

| | |
|---|---|
| Output conditioner timer | Setting ±2% or 50 ms, whichever is greater |
| Dwell conditioner timer | Setting ±2% or 50 ms, whichever is greater |
| Pulse conditioner timer | Setting ±2% or 50 ms, whichever is greater |

# 27.5 MEASUREMENTS AND RECORDING

## 27.5.1 GENERAL

| General Measurement Accuracy | |
|---|---|
| General measurement accuracy | Typically +/- 1%, but +/- 0.5% between 0.2 - 2 In/Vn |
| Phase | 0° to 360° +/- 0.5% |
| Current (0.05 to 3 In) | +/- 1.0% of reading, or 4mA (1A input), or 20mA (5A input) |
| Voltage (0.05 to 2 Vn) | +/- 1.0% of reading |
| Frequency (45 to 65 Hz) | +/- 0.025 Hz |
| Power (W) (0.2 to 2 Vn and 0.05 to 3 In) | +/- 5.0% of reading at unity power factor |
| Reactive power (Vars) (0.2 to 2 Vn and 0.05 to 3 In) | +/- 5.0% of reading at zero power factor |
| Apparent power (VA) (0.2 to 2 Vn and 0.05 to 3 In) | +/- 5.0% of reading |
| Energy (Wh) (0.2 to 2 Vn and 0.2 to 3 In) | +/- 5.0% of reading at unity power factor |
| Energy (Varh) (0.2 to 2 Vn and 0.2 to 3In) | +/- 5.0% of reading at zero power factor |

## 27.5.2 DISTURBANCE RECORDS

| Disturbance Records Measurement Accuracy | |
|---|---|
| Minimum record duration | 0.1 s |
| Maximum record duration | 10.5 s |
| Minimum number of records at 10.5 seconds | 100 |
| Magnitude and relative phases accuracy | +/- 5% of applied quantities |
| Duration accuracy | +/- 2% |
| Trigger position accuracy | +/- 2% (minimum Trigger 100 ms) |

## 27.5.3 EVENT, FAULT AND MAINTENANCE RECORDS

| Event, Fault & Maintenance Records | |
|---|---|
| Record location | Supercapacitor backed memory |
| Viewing method | Front panel display or Settings Application Software |
| Extraction method | Extracted via the USB port |
| Number of Event records | Up to 1024 time tagged event records (newest overwrites oldest) |
| Number of Fault Records | Up to 15 |
| Number of Maintenance Records | Up to 10 |
| Event time stamp resolution | 1 ms |

## 27.5.4 FAULT LOCATOR

| Accuracy | |
|---|---|
| Fault Location | +/- 2% of line length<br>Reference conditions: solid fault applied on line |

# 27.6 RATINGS

## 27.6.1 AC MEASURING INPUTS

| AC Measuring Inputs | |
|---|---|
| Nominal frequency | 50 Hz or 60 Hz (settable) |
| Operating range | 45 to 65 Hz |
| Phase rotation | ABC or CBA |

## 27.6.2 CURRENT TRANSFORMER INPUTS

| AC Current Inputs | |
|---|---|
| Nominal current (In) | 1A or 5A |
| Nominal burden per phase | < 0.2 VA at In |
| AC current thermal withstand (5A input) | 20 A (continuous operation)<br>150 A (for 10 s)<br>500 A (for 1 s) |
| AC current thermal withstand (1A input) | 4 A (continuous operation)<br>30 A (for 10 s)<br>100 A (for 1 s) |
| Linearity | Standard: Linear up to 64 × In (non-offset AC current)<br>Sensitive: Linear up to 2 × In (non-offset AC current) |

## 27.6.3 VOLTAGE TRANSFORMER INPUTS

| AC Voltage Inputs | | |
|---|---|---|
| Version | 100 V to 120 V (ph-ph) | 380 V to 480 V (ph-ph) |
| Nominal burden per VT input *1 | < 0.003 VA @ Vn (ph-n); Vn < 120/√3 V (ph-n)<br>< 0.01 VA @ Vn (ph-n); Vn < 240/√3 V (ph-n) | < 0.02 VA @ Vn (ph-n); Vn < 440/3√ V (ph-n)<br>< 0.07 VA @ Vn (ph-n); Vn < 880/3√ V (ph-n) |
| Linearity for each VT input | Linear up to 200 Vac rms | Linear up to 800 Vac rms |
| Continuous rating for each VT input | 240 Vac rms | 880 Vac rms |
| 10 seconds rating for each VT input | 312 Vac rms | 1144 Vac rms |

*Note:*
*Reference Conditions: *1 = Overfrequency operating range 50/60 Hz and over temperature range 20° +/- 5° C.*

## 27.6.4 AUXILIARY SUPPLY VOLTAGE

| | |
|---|---|
| Nominal operating range | CORTEC option (DC only)<br>24 to 48 V DC<br>CORTEC option (rated for AC or DC operation)<br>48 to 110 V DC<br>40 to 100 V AC rms<br>CORTEC option (rated for AC or DC operation)<br>110 to 250 V DC<br>100 to 240 V AC rms |
| Maximum operating range | CORTEC option (DC only)<br>19 to 65 V DC<br>CORTEC option (rated for AC or DC operation)<br>37 to 150 V DC<br>32 to 110 V AC rms<br>CORTEC option (rated for AC or DC operation)<br>87 to 300 V DC<br>80 to 265 V AC rms |
| Frequency range for AC supply | 45 to 65 Hz |
| Ripple | <15% for a DC supply (compliant with IEC 60255-26:2013) |
| Power up time | < 11 seconds |

## 27.6.5 NOMINAL BURDEN

| | |
|---|---|
| Quiescent burden | 11 W or 22 VA |
| 2nd rear communications port | 1.25 W or 2.5 VA |
| Each relay output burden | 0.13 W or 0.25 VA per output relay |
| Each opto-input burden (24 – 27 V) | 0.065 W or 0.13 VA max |
| Each opto-input burden (30 – 34 V) | 0.065 W or 0.13 VA max |
| Each opto-input burden (48 – 54 V) | 0.125 W or 0.25 VA max |
| Each opto-input burden (110 – 125 V) | 0.36 W or 0.72 VA max |
| Each opto-input burden (220 – 250 V) | 0.9 W or 1.8 VA max |

## 27.6.6 POWER SUPPLY INTERRUPTION

| | |
|---|---|
| Standard | IEC 60255-26:2013 (DC and AC) |
| 24-48V DC SUPPLY<br>100% interruption without de-energising | 20 ms at 24 V (half and full load)<br>50 ms at 36 V (half and full load)<br>100 ms at 48 V (half and full load) |
| 48-110V DC SUPPLY<br>100% interruption without de-energising | 20 ms at 37V (half and full load)<br>50 ms at 60 V (half and full load)<br>100 ms at 72 V (half load)<br>100 ms at 85 V (full load)<br>200 ms at 110 V (half and full load) |

| | |
|---|---|
| 110-250V DC SUPPLY<br>100% interruption without de-energising | 20 ms at 87 V (half load)<br>50 ms at 110 V (half load)<br>50 ms at 98 V (full load)<br>100 ms at 160 V (half load)<br>100 ms at 135 V (full load)<br>200 ms at 210 V (half load)<br>200 ms at 174 V (full load) |
| 40-100V AC SUPPLY<br>100% voltage dip without de-energising | 50 ms at 32 V (half load)<br>10 ms at 32 V (full load) |
| 100-240V AC SUPPLY<br>100% voltage dip without de-energising | 50 ms at 80 V (full and half load) |

*Note:*
*Maximum loading = all inputs/outputs energised.*

*Note:*
*Quiescent or 1/2 loading = 1/2 of all inputs/outputs energised.*

### 27.6.7 SUPERCAPACITOR

| | |
|---|---|
| Discharge time | >14 days |

# 27.7 INPUT/OUTPUT CONNECTIONS

## 27.7.1 ISOLATED DIGITAL INPUTS

| Opto-isolated digital inputs (opto-inputs) | |
|---|---|
| Compliance | ESI 48-4 |
| Rated nominal voltage | 24 to 250 V dc |
| Operating range | 19 to 265 V dc |
| Withstand | 300 V dc |
| Recognition time with half-cycle ac immunity filter removed | < 2 ms |
| Recognition time with filter on | < 12 ms |

### 27.7.1.1 NOMINAL PICKUP AND RESET THRESHOLDS

| Nominal battery voltage | Logic levels: 60-80% DO/PU | Logic Levels: 50-70% DO/PU |
|---|---|---|
| 24/27 V | Logic 0 < 16.2V, Logic 1 > 19.2V | Logic 0 <12V, Logic 1 > 16.8V |
| 30/34 | Logic 0 < 20.4V, Logic 1 > 24V | Logic 0 < 15V, Logic 1 > 21V |
| 48/54 | Logic 0 < 32.4V, Logic 1 > 38.4V | Logic 0 < 24V, Logic 1 > 33.6V |
| 110/125 | Logic 0 < 75V, Logic 1 > 88V | Logic 0 < 55.V, Logic 1 > 77V |
| 220/250 | Logic 0 < 150V, Logic 1 > 176V | Logic 0 < 110V, Logic 1 > 154V |

*Note:*
*Filter is required to make the opto-inputs immune to induced AC voltages.*

In addition to the above thresholds, some models of this product provide the following threshold levels for FSK applications:

- For 220/250 voltage inputs: Logic 0 < 145V, Logic 1 > 165V

## 27.7.2 STANDARD OUTPUT CONTACTS

| | |
|---|---|
| Compliance | In accordance with IEC 60255-1:2009 |
| Use | General purpose relay outputs for signalling, tripping and alarming |
| Rated voltage | 300 V |
| Maximum continuous current | 10 A |
| Short duration withstand carry | 30 A for 3 s<br>250 A for 30 ms |
| Make and break, dc resistive | 50 W |
| Make and break, dc inductive | 62.5 W (L/R = 50 ms) |
| Make and break, ac resistive | 2500 VA resistive (cos phi = unity) |
| Make and break, ac inductive | 2500 VA inductive (cos phi = 0.7) |
| Make and carry, dc resistive | 30 A for 3 s, 10000 operations (subject to a maximum load of 7500W)) |

| | |
|---|---|
| Make, carry and break, dc resistive | 4 A for 1.5 s, 10000 operations (subject to the above limit for make and break, dc resistive load) |
| Make, carry and break, dc inductive | 0.5 A for 1 s, 10000 operations (subject to the above limit for make and break, dc inductive load) |
| Make, carry and break ac resistive | 30 A for 200 ms, 2000 operations (subject to the above limits) |
| Make, carry and break ac inductive | 10 A for 1.5 s, 10000 operations (subject to the above limits) |
| Loaded contact | 10000 operations min. |
| Unloaded contact | 100000 operations min. |
| Operate time | < 5 ms |
| Reset time | < 10 ms |

### 27.7.3 HIGH BREAK OUTPUT CONTACTS

| | |
|---|---|
| Compliance | In accordance with IEC 60255-1:2009 |
| Use | For applications requiring high rupture capacity |
| Rated voltage | 300 V |
| Maximum continuous current | 10 A DC |
| Short duration withstand carry | 30 A DC for 3 s<br>250 A for 30 ms |
| Make and break, dc resistive | 7500 W |
| Make and break, dc inductive | 2500 W (L/R = 50 ms) |
| Make and carry, dc resistive | 30 A for 3 s, 10000 operations (subject to the above limits) |
| Make, carry and break, dc resistive | 30 A for 3 s, 5000 operations (subject to the above limit for make and break, dc resistive load)<br>30 A for 200 ms, 10000 operations (subject to the above limit for make and break, dc resistive load) |
| Make, carry and break, dc inductive | 10 A for 40 ms, 10000 operations (subject to the above limit for make and break, dc inductive load)<br>10 A for 20 ms (250V, 4 shots per second, subject to the above limit for make and break, dc inductive load) |
| Loaded contact | 10,000 operations minimum. |
| Unloaded contact | 100,000 operations minimum. |
| Operate time | < 0.2 ms |
| Reset time | < 8 ms |
| MOV Protection | Maximum voltage 330 V DC |

### 27.7.4 WATCHDOG CONTACTS

| | |
|---|---|
| Use | Non-programmable contacts for relay healthy/relay fail indication |
| Breaking capacity, dc resistive | 30 W |
| Breaking capacity, dc inductive | 15 W (L/R = 40 ms) |
| Breaking capacity, ac inductive | 375 VA inductive (cos phi = 0.7) |

# 27.8 MECHANICAL SPECIFICATIONS

## 27.8.1 PHYSICAL PARAMETERS

| | |
|---|---|
| Case Types* | 40TE<br>60TE<br>80TE |
| Weight (40TE case) | 7 kg - 8 kg (depending on chosen options) |
| Weight (60TE case) | 9 kg - 12 kg (depending on chosen options) |
| Weight (80TE case) | 13 kg - 16 kg (depending on chosen options) |
| Dimensions in mm (w x h x l) (40TE case) | W: 206.0 mm H: 177.0 mm D: 243.1 mm |
| Dimensions in mm (w x h x l) (60TE case) | W: 309.6 mm H: 177.0 mm D: 243.1 mm |
| Dimensions in mm (w x h x l) (80TE case) | W 413.2 mm H 177.0 mm D 243.1 mm |
| Mounting | Panel, rack, or retrofit |

*Note:*
**Case size is product dependent.*

## 27.8.2 ENCLOSURE PROTECTION

| | |
|---|---|
| Against dust and dripping water (front face) | IP52 as per IEC 60529:1989/A2:2013 |
| Protection against dust (whole case) | IP50 as per IEC 60529:1989/A2:2013 |
| Protection for sides of the case (safety) | IP30 as per IEC 60529:1989/A2:2013 |
| Protection for rear of the case (safety) | IP10 as per IEC 60529:1989/A2:2013 |

## 27.8.3 MECHANICAL ROBUSTNESS

| | |
|---|---|
| Vibration test per EN 60255-21-1:1998 | Response: class 2, Endurance: class 2 |
| Shock and bump immunity per EN 60255-21-2:1988 | Shock response: class 2, Shock withstand: class 1, Bump withstand: class 1 |
| Seismic test per EN 60255-21-3: 1993 | Class 2 |

## 27.8.4 TRANSIT PACKAGING PERFORMANCE

| | |
|---|---|
| Primary packaging carton protection | ISTA 1C |
| Vibration tests | 3 orientations, 7 Hz, amplitude 5.3 mm, acceleration 1.05g |
| Drop tests | 10 drops from 610 mm height on multiple carton faces, edges and corners |

# 27.9 TYPE TESTS

## 27.9.1 INSULATION

| | |
|---|---|
| Compliance | IEC 60255-27: 2013 |
| Insulation resistance | > 100 M ohm at 500 V DC (Using only electronic/brushless insulation tester) |

## 27.9.2 CREEPAGE DISTANCES AND CLEARANCES

| | |
|---|---|
| Compliance | IEC 60255-27: 2013 |
| Pollution degree | 3 |
| Overvoltage category | III |
| Impulse test voltage (not RJ45) | 5 kV |
| Impulse test voltage (RJ45) | 1 kV |

## 27.9.3 HIGH VOLTAGE (DIELECTRIC) WITHSTAND

| | |
|---|---|
| IEC Compliance | IEC 60255-27: 2013 |
| Between all independent circuits | 2 kV ac rms for 1 minute |
| Between independent circuits and protective earth conductor terminal | 2 kV ac rms for 1 minute |
| Between all case terminals and the case earth | 2 kV ac rms for 1 minute |
| Across open watchdog contacts | 1 kV ac rms for 1 minute |
| Across open contacts of changeover output relays | 1 kV ac rms for 1 minute |
| Between all RJ45 contacts and protective earth | 1 kV ac rms for 1 minute |
| Between all screw-type EIA(RS)485 contacts and protective earth | 1 kV ac rms for 1 minute |
| ANSI/IEEE Compliance | ANSI/IEEE C37.90-2005 |
| Across open contacts of normally open output relays | 1.5 kV ac rms for 1 minute |
| Across open contacts of normally open changeover output relays | 1 kV ac rms for 1 minute |
| Across open watchdog contacts | 1 kV ac rms for 1 minute |

## 27.9.4 IMPULSE VOLTAGE WITHSTAND TEST

| | |
|---|---|
| Compliance | IEC 60255-27: 2013 |
| Between all independent circuits | Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J |
| Between terminals of all independent circuits | Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J |
| Between all independent circuits and protective earth conductor terminal | Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J |

*Note:*
*Exceptions are communications ports and normally-open output contacts, where applicable.*

# 27.10 ENVIRONMENTAL CONDITIONS

## 27.10.1 AMBIENT TEMPERATURE RANGE

| | |
|---|---|
| Compliance | IEC 60255-27: 2013 |
| Test Method | IEC 60068-2-1:2007 and IEC 60068-2-2 2007 |
| Operating temperature range | -25°C to +55°C (continuous) |
| Storage and transit temperature range | -25°C to +70°C (continuous) |

## 27.10.2 TEMPERATURE ENDURANCE TEST

| Temperature Endurance Test | |
|---|---|
| Test Method | IEC 60068-2-1: 2007 and 60068-2-2: 2007 |
| Operating temperature range | -40°C (96 hours)<br>+70°C (96 hours) |
| Storage and transit temperature range | -40°C (96 hours)<br>+70°C (96 hours) |

## 27.10.3 AMBIENT HUMIDITY RANGE

| | |
|---|---|
| Compliance | IEC 60068-2-78: 2012 and IEC 60068-2-30: 2005 |
| Durability | 56 days at 93% relative humidity and +40°C |
| Damp heat cyclic | six (12 + 12) hour cycles, 93% RH, +25 to +55°C |

## 27.10.4 CORROSIVE ENVIRONMENTS

| | |
|---|---|
| Compliance, Industrial corrosive environment/poor environmental control | IEC 60068-2-42: 2003, IEC 60068-2-43: 2003, IEC 60068-2-52: 1996 |
| Sulphur Dioxide, IEC 60068-2-42: 2003 | 21 days exposure to elevated concentrations (25ppm) of $SO_2$ at 75% relative humidity and +25°C |
| Hydrogen Sulphide, IEC 60068-2-43: 2003 | 21 days exposure to elevated concentrations (10ppm) of $H_2S$ at 75% relative humidity and +25°C |
| Salt mist, IEC 60068-2-52: 1996 | 7 days, KB severity 3 |

# 27.11 ELECTROMAGNETIC COMPATIBILITY

## 27.11.1 1 MHZ BURST HIGH FREQUENCY DISTURBANCE TEST

| | |
|---|---|
| Compliance | IEC 60255-26:2013 |
| Common-mode test voltage (level 3) | 2.5 kV |
| Differential test voltage (level 3) | 1.0 kV |

## 27.11.2 DAMPED OSCILLATORY TEST

| | |
|---|---|
| Compliance | EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz. Level 4: 3 MHz, 10 MHz and 30 MHz, IEC 60255-26:2013 |
| Common-mode test voltage (level 3) | 2.5 kV |
| Common-mode test voltage (level 4) | 4.0 kV |
| Differential mode test voltage | 1.0 kV |

## 27.11.3 IMMUNITY TO ELECTROSTATIC DISCHARGE

| | |
|---|---|
| Compliance | IEC 60255-26:2013, IEC 61000-4-2:2009 |
| Class 4 Condition | 15 kV discharge in air to user interface, display, and exposed metalwork |
| Class 3 Condition | 8 kV discharge in air to all communication ports |

## 27.11.4 ELECTRICAL FAST TRANSIENT OR BURST REQUIREMENTS

| | |
|---|---|
| Compliance | IEC 60255-26:2013, IEC 61000-4-4:2012 |
| Applied to communication inputs | Amplitude: 2 kV, burst frequency 5 kHz and 100 KHz (level 4) |
| Applied to power supply and all other inputs except for communication inputs | Amplitude: 4 kV, burst frequency 5 kHz and 100 KHz (level 4) |

## 27.11.5 SURGE WITHSTAND CAPABILITY

| | |
|---|---|
| Compliance | IEEE/ANSI C37.90.1: 2012 |
| Condition 1 | 4 kV fast transient and 2.5 kV oscillatory applied common mode and differential mode to opto inputs, output relays, CTs, VTs, power supply |
| Condition 2 | 4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B |

### 27.11.6 SURGE IMMUNITY TEST

| | |
|---|---|
| Compliance | IEC 60255-26:2013, IEC 61000-4-5:2014+AMD1:2017 |
| Pulse duration | Time to half-value: 1.2/50 µs |
| Between all groups and protective earth conductor terminal | Amplitude 4 kV |
| Between terminals of each group (excluding communications ports, where applicable) | Amplitude 2 kV |

### 27.11.7 IMMUNITY TO RADIATED ELECTROMAGNETIC ENERGY

| | |
|---|---|
| Compliance | IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010 |
| Frequency band | 80 MHz to 3.0 GHz |
| Spot tests at | 80, 160, 380, 450, 900, 1850, 2150 MHz |
| Test field strength | 10 V/m |
| Test using AM | 1 kHz @ 80% |
| Compliance | IEEE/ANSI C37.90.2: 2004 |
| Frequency band | 80 MHz to 1 GHz |
| Spot tests at | 80, 160, 380, 450 MHz |
| Waveform | 1 kHz @ 80% am and pulse modulated |
| Field strength | 35 V/m |

### 27.11.8 RADIATED IMMUNITY FROM DIGITAL COMMUNICATIONS

| | |
|---|---|
| Compliance | IEC 61000-4-3:2006 + A2:2010 |
| Frequency bands | 800 to 960 MHz, 1.4 to 2.0 GHz |
| Test field strength | 30 V/m |
| Test using AM | 1 kHz / 80% |

### 27.11.9 RADIATED IMMUNITY FROM DIGITAL RADIO TELEPHONES

| | |
|---|---|
| Compliance | IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010 |
| Frequency bands | 900 MHz and 1.89 GHz |
| Test field strength | 10 V/m |

### 27.11.10 IMMUNITY TO CONDUCTED DISTURBANCES INDUCED BY RADIO FREQUENCY FIELDS

| | |
|---|---|
| Compliance | IEC 60255-26:2013, IEC 61000-4-6:2013 Level 3 |
| Frequency bands | 150 kHz to 80 MHz |

| | |
|---|---|
| Test disturbance voltage | 10 V rms |
| Test using AM | 1 kHz @ 80% |
| Spot tests | 27 MHz and 68 MHz |

## 27.11.11 MAGNETIC FIELD IMMUNITY

| | |
|---|---|
| Compliance | IEC 61000-4-8:2009 Level 5<br>IEC 61000-4-9:2016 Level 5<br>IEC 61000-4-10:2016 Level 5 |
| IEC 61000-4-8 test | 100 A/m applied continuously, 1000 A/m applied for 3 s |
| IEC 61000-4-9 test | 1000 A/m applied in all planes |
| IEC 61000-4-10 test | 100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 seconds |

## 27.11.12 CONDUCTED EMISSIONS

| | |
|---|---|
| Compliance | IEC 60255-26:2013, EN 55032: 2015+A1:2020 |
| Power supply test 1 | 0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average) |
| Power supply test 2 | 0.5 – 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average) |
| RJ45 test 1 (where applicable) | 0.15 - 0.5 MHz, 97 dBµV (quasi peak) 84 dBµV (average) |
| RJ45 test 2 (where applicable) | 0.5 – 30 MHz, 87 dBµV (quasi peak) 74 dBµV (average) |

## 27.11.13 RADIATED EMISSIONS

| | |
|---|---|
| Compliance | IEC 60255-26:2013 |
| Test 1 | 30 – 230 MHz, 40 dBµV/m at 10 m measurement distance |
| Test 2 | 230 – 1 GHz, 47 dBµV/m at 10 m measurement distance |
| Test 3 | 1 – 2 GHz, 76 dBµV/m at 10 m measurement distance |

## 27.11.14 POWER FREQUENCY

| | |
|---|---|
| Compliance | IEC 60255-26:2013 |
| Opto-inputs (Compliance is achieved using the opto-input filter) | 300 V common-mode (Class A)<br>150 V differential mode (Class A) |

*Note:*
*Compliance is achieved using the opto-input filter.*

## 27.12 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

### 27.12.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

### 27.12.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

### 27.12.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

### 27.12.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL us

## APPENDIX A

# ORDERING OPTIONS

**Ordering information**

| Variants Order No. | | Order No. | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Distance Protection P443** | | **P443** | | | | | | | | | | | ** | |
| **1 & 3 Pole Tripping/Reclosing MHO/Quad Distance with Product Options** | | | | | | | | | | | | | | |
| **Nominal Aauxiliary Voltage** | | | | | | | | | | | | | | |
| 24 - 54Vdc | | | 7 | | | | | | | | | | | |
| 48 - 125Vdc (40 - 100Vac) | | | 8 | | | | | | | | | | | |
| 110 - 250 Vdc (100 - 240 Vac) | | | 9 | | | | | | | | | | | |
| **In/Vn Rating** | | | | | | | | | | | | | | |
| Dual rated CT (1 & 5A : 100 - 120V) | | | | 1 | | | | | | | | | | |
| Non-conventional input transformers NCIT (IEC 61850-9-2 LE) (**NOT yet available**) | | | | A | | | | | | | | | | |
| **Hardware Options** | **Protocol** | | | | | | | | | | | | | |
| Standard - None | 1, 3 & 4 | | | | 1 | | | | | | | | | |
| IRIG-B Only (Modulated) | 1, 3 & 4 | | | | 2 | | | | | | | | | |
| IRIG-B (Modulated) & Fibre Optic Converter | 1, 3 & 4 | | | | 4 | | | | | | | | | |
| Ethernet (100Mbit/s) | 6, 7 & 8 | | | | 6 | | | | | | | | | |
| Second Rear Comms + InterMiCOM | 1, 3 & 4 | | | | 7 | | | | | | | | | |
| IRIG-B (Modulated) + Second Rear Comms + InterMiCOM | 1, 3 & 4 | | | | 8 | | | | | | | | | |
| Ethernet (100Mbit/s) plus IRIG-B (Modulated) * | 6, 7 & 8 | | | | A | | | | | | | | | |
| Ethernet (100Mbit/s) plus IRIG-B (Un-modulated) * | 6, 7 & 8 | | | | B | | | | | | | | | |
| InterMiCOM + Courier Rear Port + IRIG-B modulated *** | 1, 3 & 4 | | | | F | | | | | | | | | |
| Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B ** | 6, 7 & 8 | | | | J | | | | | | | | | |
| Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B ** | 6, 7 & 8 | | | | K | | | | | | | | | |
| Redundant Ethernet PRP/HSR****, 2 fibre ports + Modulated IRIG-B **** | 6, 7 & 8 | | | | N | | | | | | | | | |
| Redundant Ethernet PRP/HSR****, 2 fibre ports + Unmodulated IRIG-B **** | 6, 7 & 8 | | | | P | | | | | | | | | |
| Single Ethernet 1 LC Duplex port + Universal IRIG-B + 1588 | 6 & 7 | | | | U | | | | | | | | | |
| Redundant Ethernet PRP/HSR/RSTP/Failover 2 RJ45 + Universal IRIG-B + 1588 Redundant | 6 & 7 | | | | W | | | | | | | | | |
| Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex ports + Universal IRIG-B + 1588 | 6 & 7 | | | | Y | | | | | | | | | |
| * Only On K/M Suffix & later Relays) | | | | | | | | | | | | | | |
| ** Only on Suffix K/M relays with 55 Software & later | | | | | | | | | | | | | | |
| *** Only on Suffix K/M relays with 57 Software & later, replaces hardware options '7' & '8' | | | | | | | | | | | | | | |
| **** Only on Suffix K relays with 55 Software & later | | | | | | | | | | | | | | |
| ***** For HSR - contact GE Vernova for details | | | | | | | | | | | | | | |
| **Product Options** | | | | | | | | | | | | | | |
| 16 inputs and 24-standard outputs | | | | | | A | | | | | | | | |
| 24 inputs and 32-standard outputs | | | | | | B | | | | | | | | |
| 16 inputs and 16-standard plus 4-high break outputs | | | | | | C | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs | | | | | | D | | | | | | | | |
| 16 inputs and 24-standard outputs + 850nm dual channel | | | | | | E | | | | | | | | |
| 24 inputs and 32-standard outputs + 850nm dual channel | | | | | | F | | | | | | | | |
| 16 inputs and 16-standard plus 4-high break outputs + 850nm dual channel | | | | | | G | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 850nm dual channel | | | | | | H | | | | | | | | |
| 16 inputs and 24-standard outputs + 1300nm SM single channel | | | | | | I | | | | | | | | |
| 24 inputs and 32-standard outputs + 1300nm SM single channel | | | | | | J | | | | | | | | |
| 16 inputs and 16-standard plus 4-high break outputs + 1300nm SM single channel | | | | | | K | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 1300nm SM single channel | | | | | | L | | | | | | | | |
| 16 inputs and 24-standard outputs + 1300nm SM dual channel | | | | | | M | | | | | | | | |
| 24 inputs and 32-standard outputs + 1300nm SM dual channel | | | | | | N | | | | | | | | |
| 16 inputs and 16-standard plus 4-high break outputs + 1300nm SM dual channel | | | | | | O | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 1300nm SM dual channel | | | | | | P | | | | | | | | |
| 16 inputs and 24-standard outputs + 1300nm MM single channel | | | | | | Q | | | | | | | | |
| 24 inputs and 32-standard outputs + 1300nm MM single channel | | | | | | R | | | | | | | | |
| 16 inputs and 16-standard plus 4-high break outputs + 1300nm MM single channel | | | | | | S | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 1300nm MM single channel | | | | | | T | | | | | | | | |
| 16 inputs and 24-standard outputs + 1300nm MM dual channel | | | | | | U | | | | | | | | |
| 24 inputs and 32-standard outputs + 1300nm MM dual channel | | | | | | V | | | | | | | | |
| 16 inputs and 16-standard plus 4-high break outputs + 1300nm MM dual channel | | | | | | W | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 1300nm MM dual channel | | | | | | X | | | | | | | | |
| 32 inputs and 32-standard outputs (only available on Design Suffix K/M devices with version "54" software and later) | | | | | | Y | | | | | | | | |
| 24 inputs and 32-standard outputs + 850nm MM + 1300nm SM dual channel | | | | | | Z | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 850nm MM + 1300nm SM dual channel | | | | | | 1 | | | | | | | | |
| 24 inputs and 32-standard outputs + 1300nm SM + 850nm MM dual channel | | | | | | 2 | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 1300nm SM + 850nm MM dual channel | | | | | | 3 | | | | | | | | |
| 24 inputs and 32-standard outputs + 850nm MM + 1300nm MM dual channel | | | | | | 4 | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 850nm MM + 1300nm MM dual channel | | | | | | 5 | | | | | | | | |
| 24 inputs and 32-standard outputs + 1300nm MM + 850nm MM dual channel | | | | | | 6 | | | | | | | | |
| 24 inputs and 16-standard plus 8-high break outputs + 1300nm MM + 850nm MM dual channel | | | | | | 7 | | | | | | | | |
| **Protocol Options** | **Hardware Compatibilty** | | | | | | | | | | | | | |
| K-Bus | 1, 2, 3, 4, C, E & F | | | | | | 1 | | | | | | | |
| IEC870 | 1, 2, 3, 4, C, E & F | | | | | | 3 | | | | | | | |
| DNP3.0 | 1, 2, 3, 4, C, E & F | | | | | | 4 | | | | | | | |
| IEC61850 + Courier via rear RS485 port | 6, A, B, G, H, J, K, L, M, N, P | | | | | | 6 | | | | | | | |
| IEC61850+IEC60870-5-103 via rear RS485 port | 6, A, B, G, H, J, K, L, M, N, P | | | | | | 7 | | | | | | | |
| DNP3.0 Over Ethernet * | 6, A, B, G, H, J, K, L, M, N, P | | | | | | 8 | | | | | | | |
| * Available on Design Suffix K/M devices with version "54" software and later | | | | | | | | | | | | | | |
| **Mounting** | | | | | | | | | | | | | | |
| Flush/Panel Mounting with Harsh Env. Coating, with USB Port, Black and Silver Front Panel | | | | | | | | S | | | | | | |
| 19" Rack Mounting with Harsh Env. Coating, with USB Port, Black and Silver Front Panel | | | | | | | | T | | | | | | |
| Flush/panel mounting with harsh environment coating | | | | | | | | P | | | | | | |
| 19" Rack mounting with harsh environmental coating | | | | | | | | Q | | | | | | |

| Variants Order No. | Order No. |
|---|---|
| **Distance Protection P443** | **P443** ** |
| **Language** | |
| English, French, German, Spanish | 0 |
| English, French, German, Russian (only available on Design Suffix K/M and later devices) | 5 |
| English, Italian, Polish and Portuguese (software '75' and later) | 7 |
| **Software Version** | |
| Date and application dependant | ** |
| **Customer Specific Options** | |
| Standard version | 0 |
| Customer version | A |
| **Hardware Version** | |
| Enhanced Main Processor (CPU2) with hotkeys, dual characteristic optos | J |
| Extended main processor (XCPU2) With Function Keys & Tri-colour LEDs | K |
| As K plus increased main processor memory (XCPU3), Cyber Security | M |

## APPENDIX B

# SETTINGS AND SIGNALS

Tables containing a full list of settings for each model are provided in a separate Excel file, attached as an embedded resource. If using Adobe Acrobat Reader, click on the button below to open the spreadsheet.

This manual must be opened with a PDF viewer capable of opening attachments, such as Adobe Acrobat Reader or Nitro PDF. If using Nitro PDF, attachments are shown in the attachment pane. To show or hide the attachments pane, look in the sidebar and click the attachments tab.

*Note:*
*An Open File dialogue box may open with a warning message about potential harm from programs, macros or viruses. The file supplied does not contain any harmful content, and may be safely opened.*

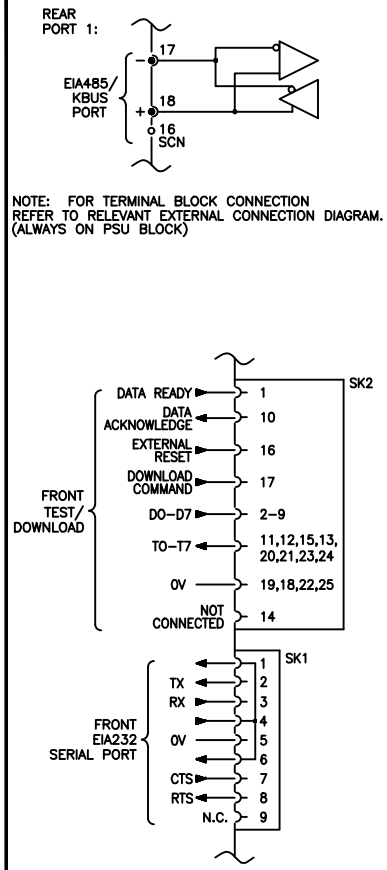
Settings and Signals

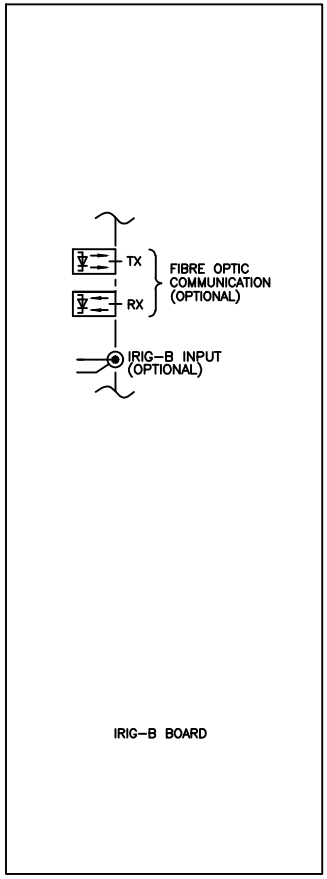
## APPENDIX C

# WIRING DIAGRAMS

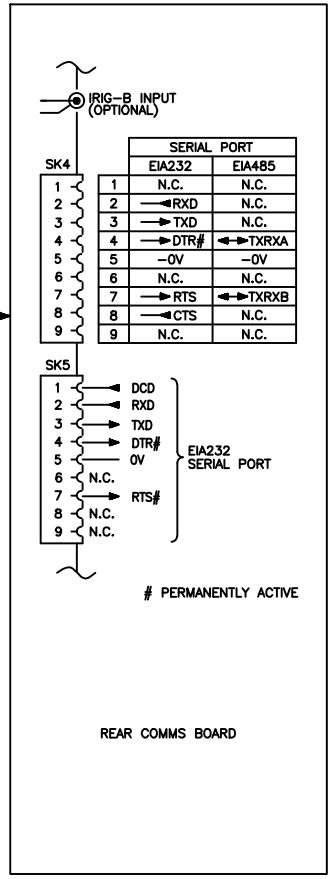
| Model | CORTEC Option* | Input/Output Options and Case Size Compatibility | | Drawing-Sheet | Issue |
|---|---|---|---|---|---|
| All | - | Comms Options MiCOM Px40 Platform | | 10Px4001-1<br>10Px4001-2 | N<br>B |
| P443 | I/O Options:<br>A, E, I, M, Q, U | (16 I/P & 24 O/P) | (80TE) | 10P44304-1<br>10P44304-3 | F<br>E |
| | I/O Options:<br>B, F, J, N, R, Z, 2, 4, 6 | (24 I/P & 32 O/P) | (80TE) | 10P44303-1<br>10P44303-3 | F<br>E |
| | I/O Options:<br>C, G, K, O, S, W | (16 I/P & 16 O/P) plus 4 High Break Relays | (80TE) | 10P44306-1<br>10P44306-3 | G<br>E |
| | I/O Options:<br>D, H, L, P, T, X | (24 I/P & 16 O/P) plus 8 High Break Relays | (80TE) | 10P44305-1<br>10P44305-3 | F<br>E |
| | I/O Option Y | (32 I/P & 32 O/P) | (80TE) | 10P44307-1<br>10P44307-3 | F<br>E |
| | I/O Option V | (24 I/P & 32 O/P) | (80TE) | 10P44343-1 | C |

* When selecting the applicable wiring diagram(s), refer to the appropriate model CORTEC.

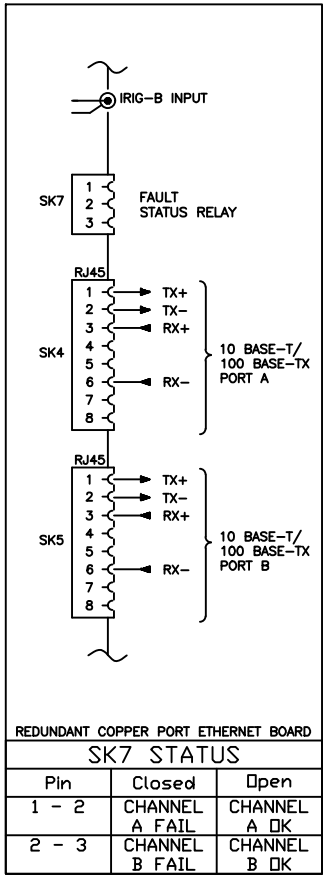



OR

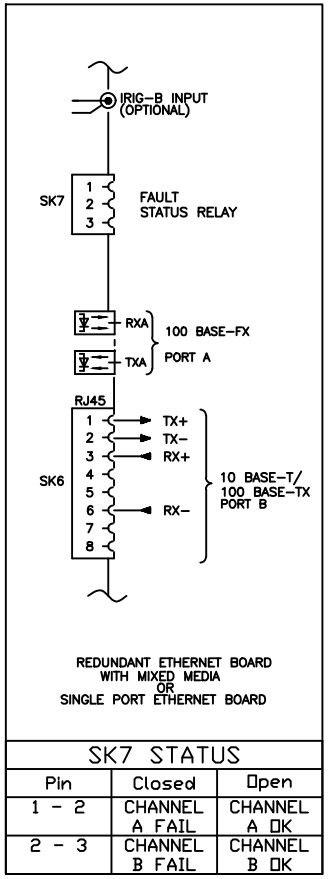



OR



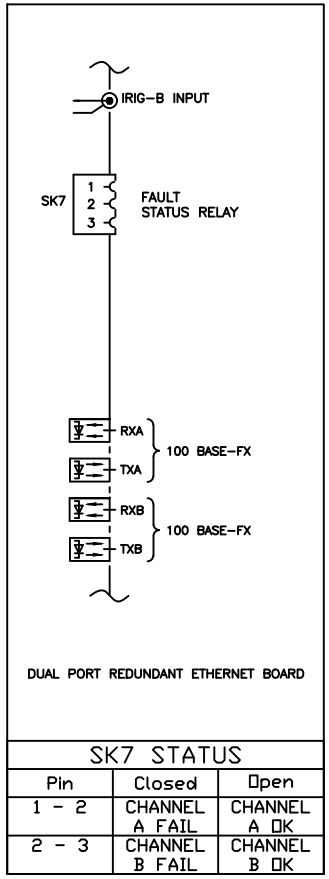

| SK7 STATUS | | |
|---|---|---|
| Pin | Closed | Open |
| 1 - 2 | CHANNEL A FAIL | CHANNEL A OK |
| 2 - 3 | CHANNEL B FAIL | CHANNEL B OK |

OR




| SK7 STATUS | | |
|---|---|---|
| Pin | Closed | Open |
| 1 - 2 | CHANNEL A FAIL | CHANNEL A OK |
| 2 - 3 | CHANNEL B FAIL | CHANNEL B OK |

OR




| SK7 STATUS | | |
|---|---|---|
| Pin | Closed | Open |
| 1 - 2 | CHANNEL A FAIL | CHANNEL A OK |
| 2 - 3 | CHANNEL B FAIL | CHANNEL B OK |

| | | | | | |
|---|---|---|---|---|---|
| Issue: N | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAGRAM: COMMS OPTIONS MICOM Px40 PLATFORM | | |
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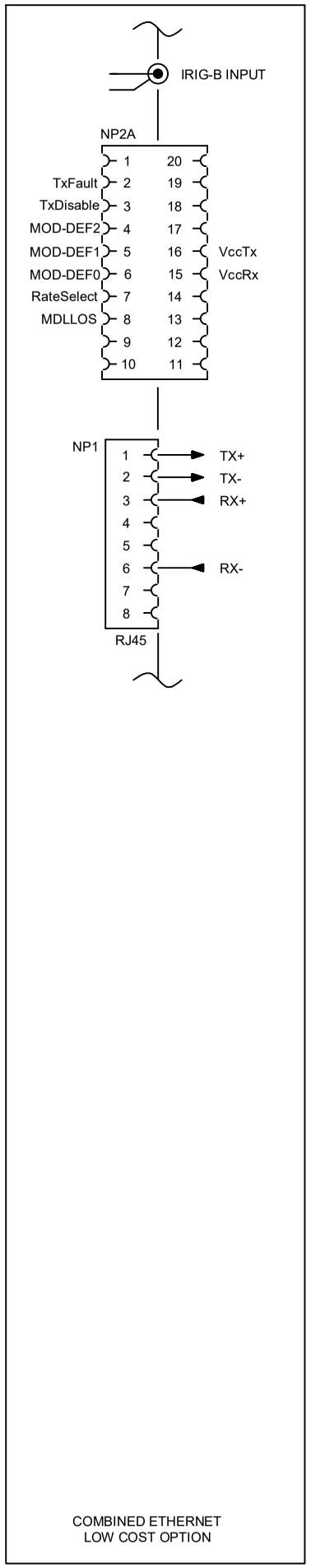
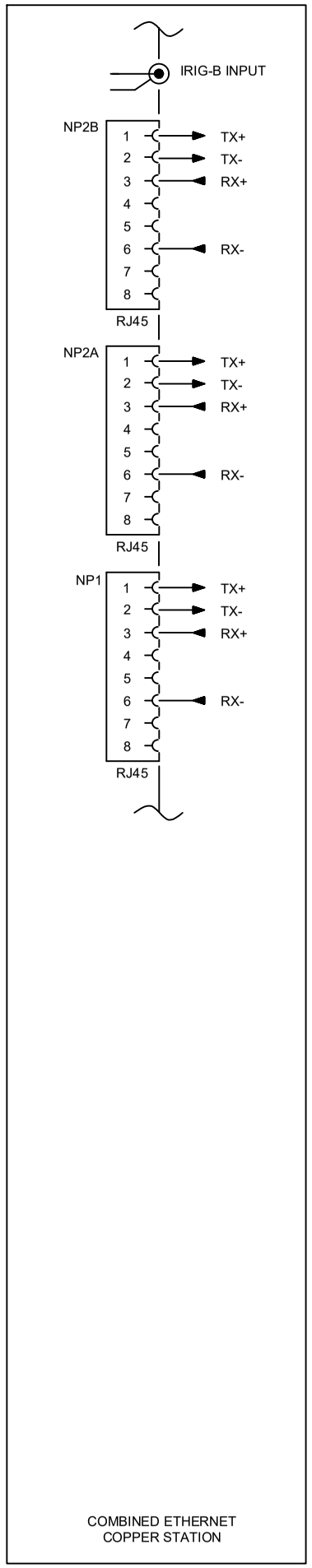
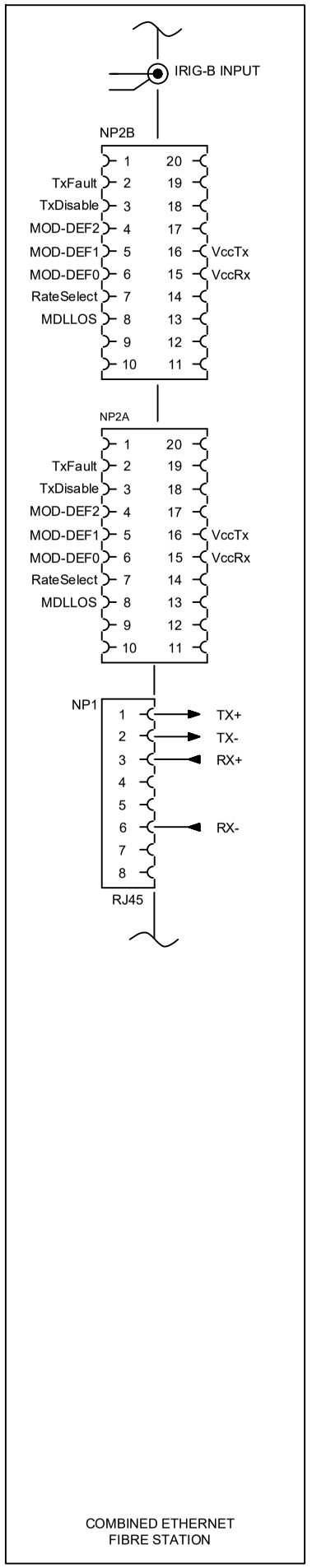
| Date: | Chkd: | | | | GE VERNOVA |



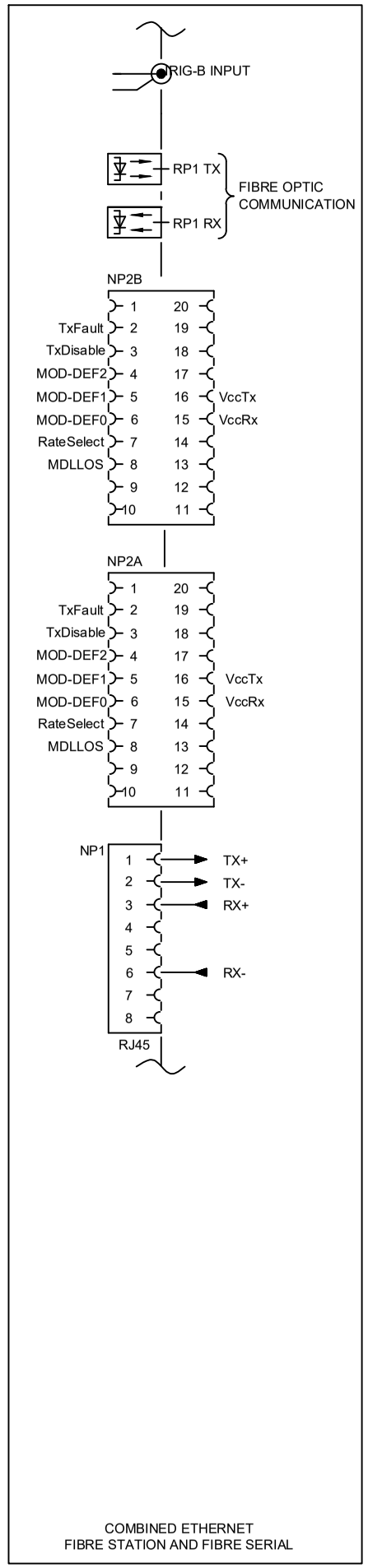

COMBINED ETHERNET
LOW COST OPTION




COMBINED ETHERNET
COPPER STATION




COMBINED ETHERNET
FIBRE STATION




COMBINED ETHERNET
FIBRE STATION AND FIBRE SERIAL

| | | | | | | |
|---|---|---|---|---|---|---|
| Issue: B | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAGRAM COMMS OPTIONS MICOM Px40 | | | |
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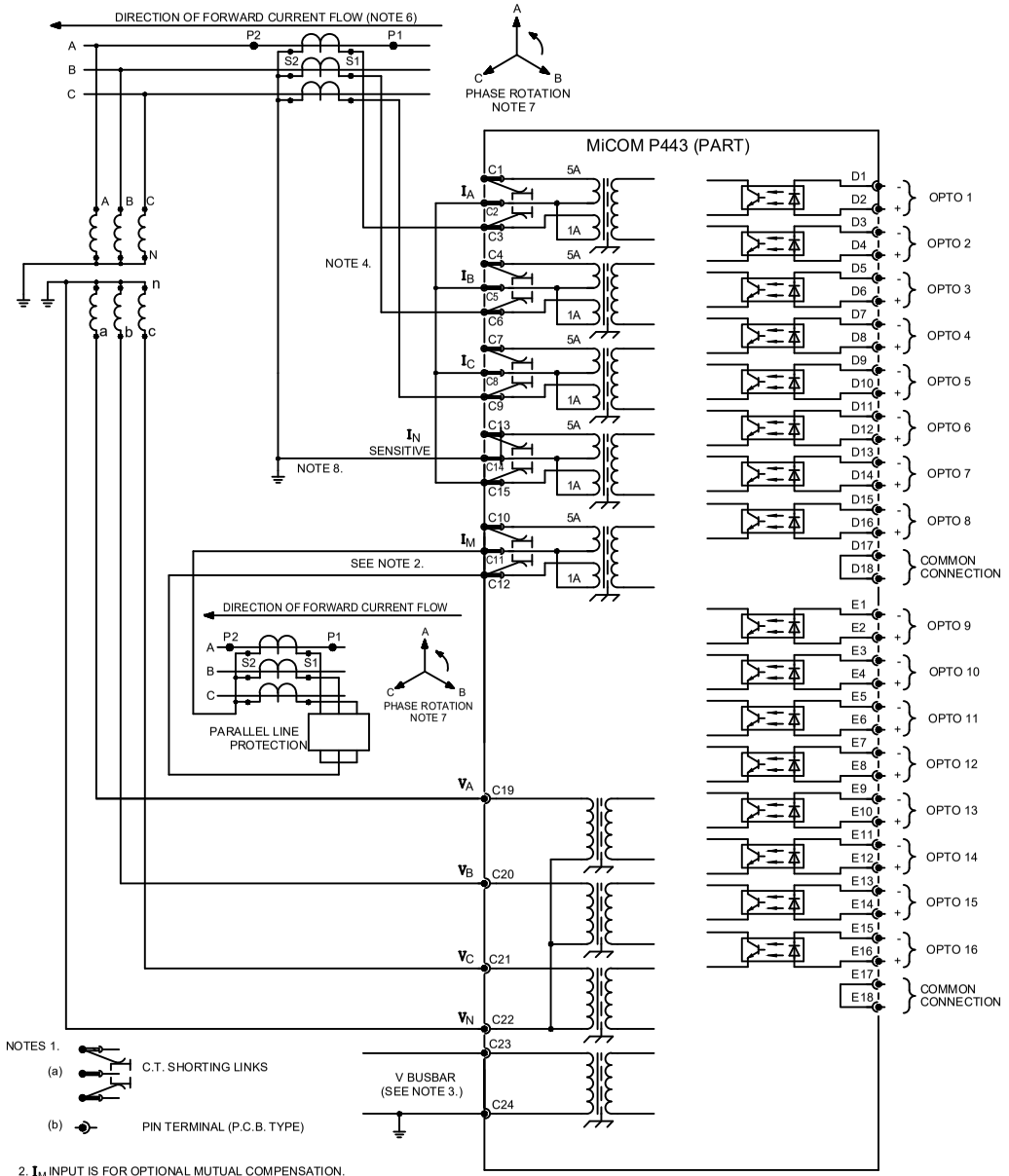
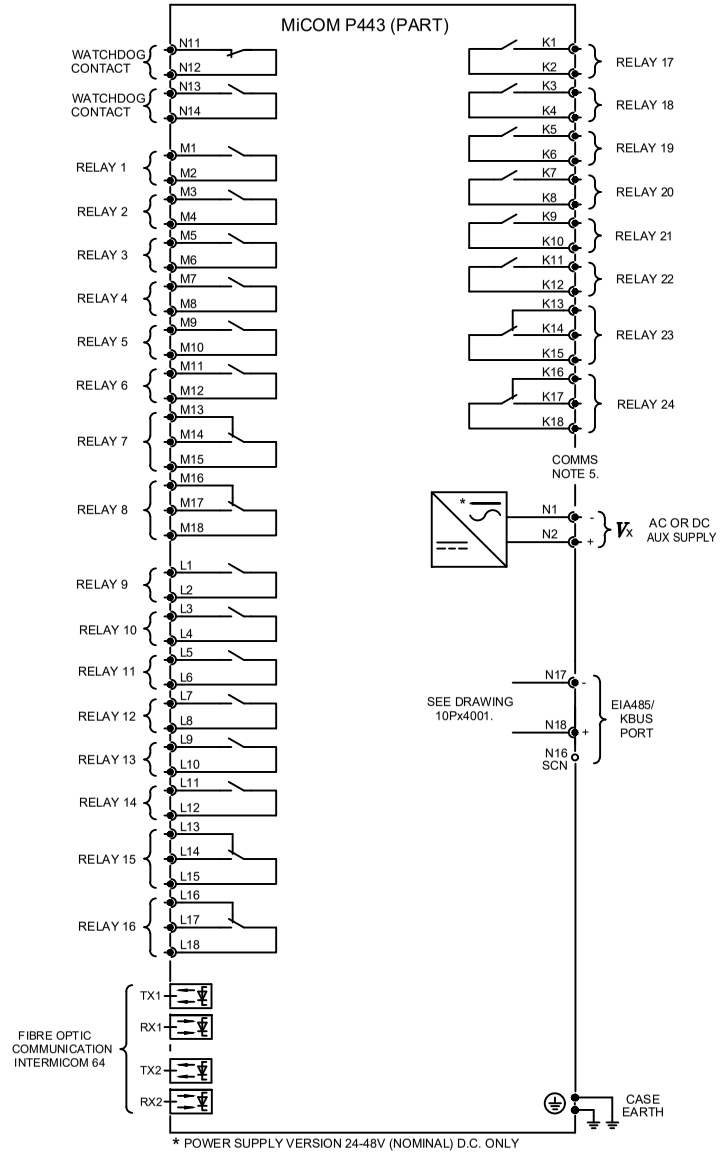
| Date: | Chkd: | | | | | |




2. $I_M$ INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
5. FOR COMMS OPTIONS SEE DRAWING 10PX4001
6. WITH C.T. POLARITY SETTING 'STANDARD'.
7. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
8. USED FOR SEF PROTECTION. $I_N$ SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

SHT.1 & SHT.2 DIAGRAMS ARE IDENTICAL APART FROM :-
- PICTORIAL REPRESENTATION OF RELAY CONTACTS.
- CTs SHOWN CONNECTED (1A SHT.1 & 5A SHT.2).

IEC SYMBOLS

| | | | | | |
|---|---|---|---|---|---|
| Issue: F | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (16 I/P & 24 O/P) | | |
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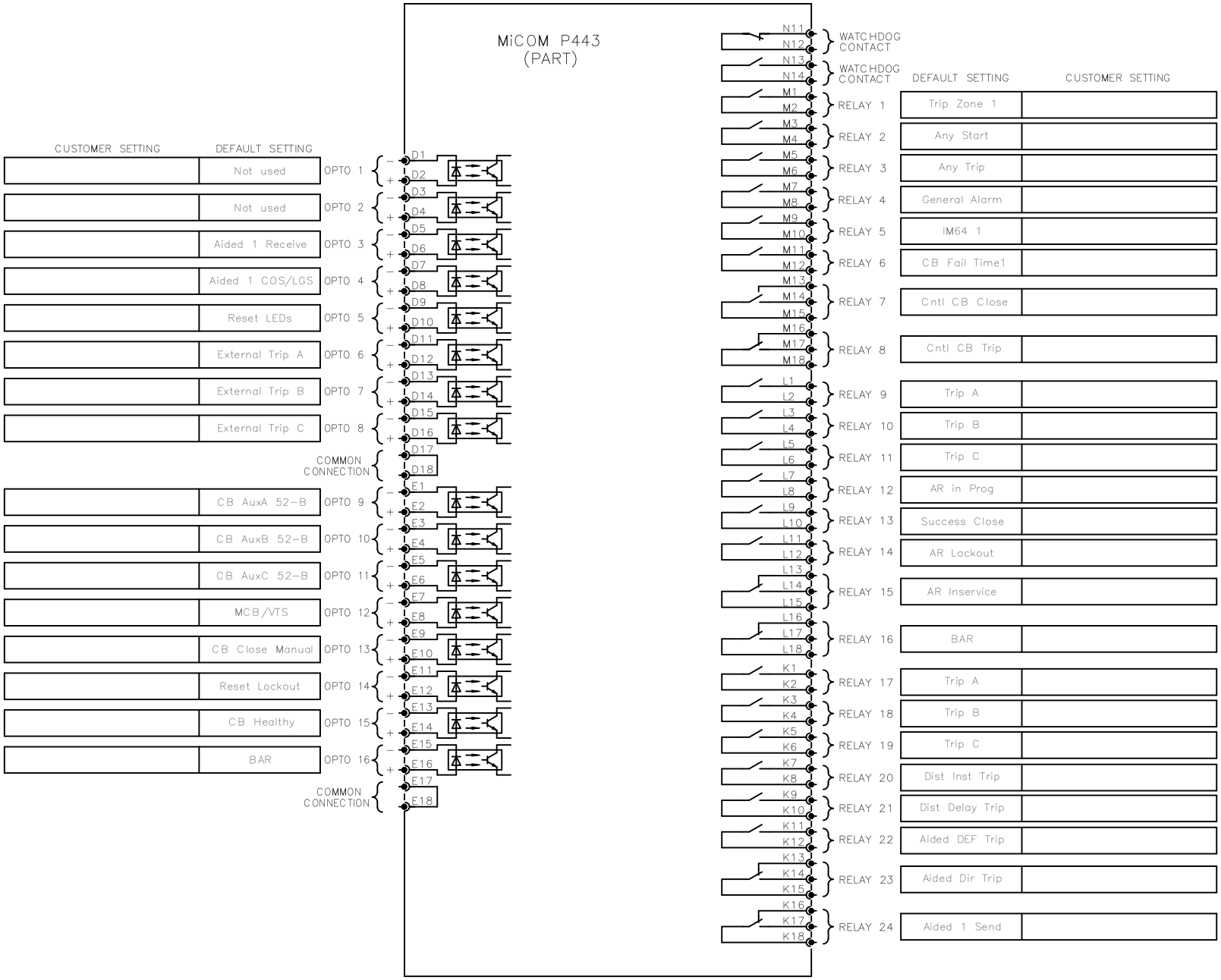


| | | | | | | |
|---|---|---|---|---|---|---|
| Issue: E | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (16 I/P & 24 O/P) | | | |
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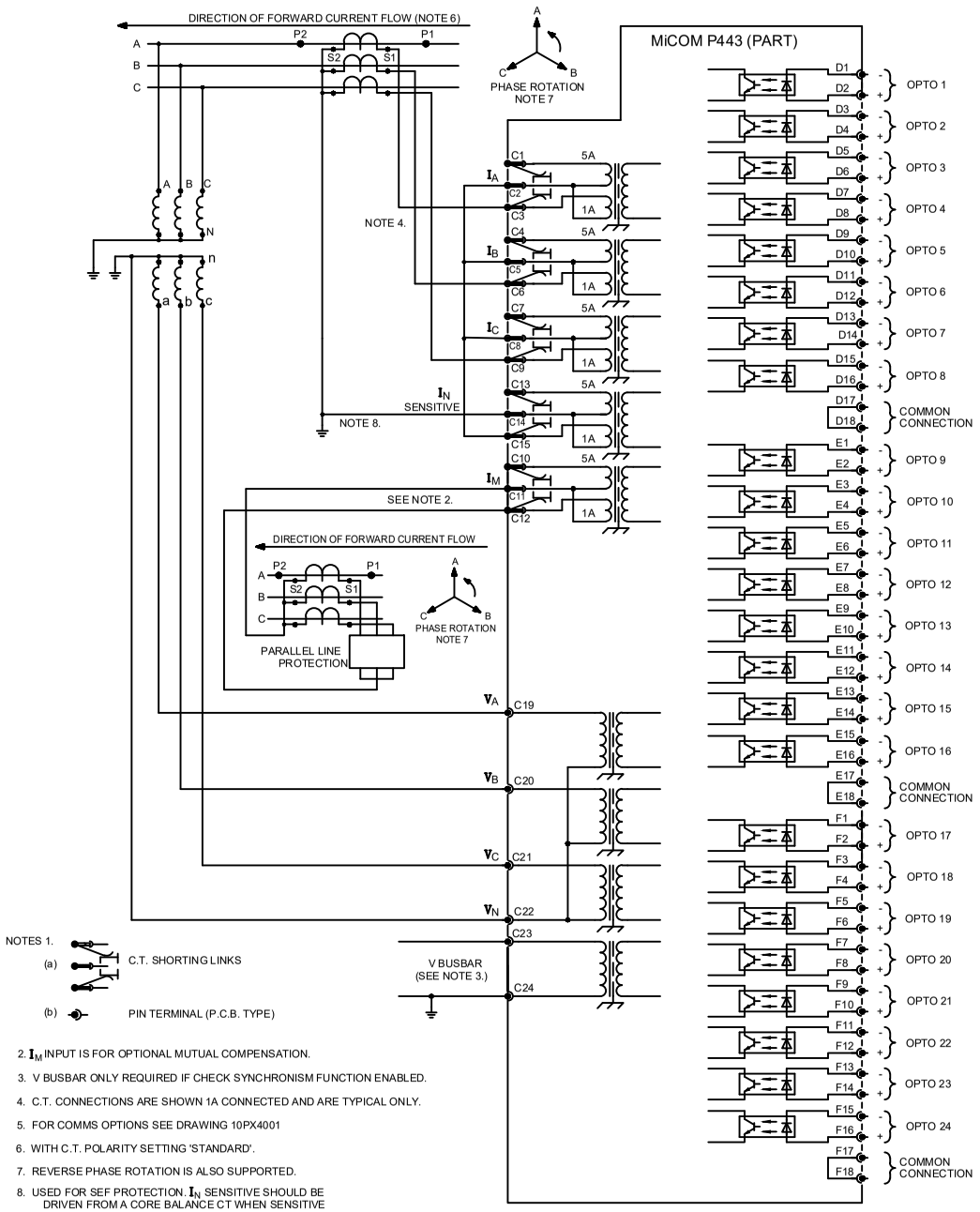
| Date: | Chkd: | | | | Next Sht: - | |

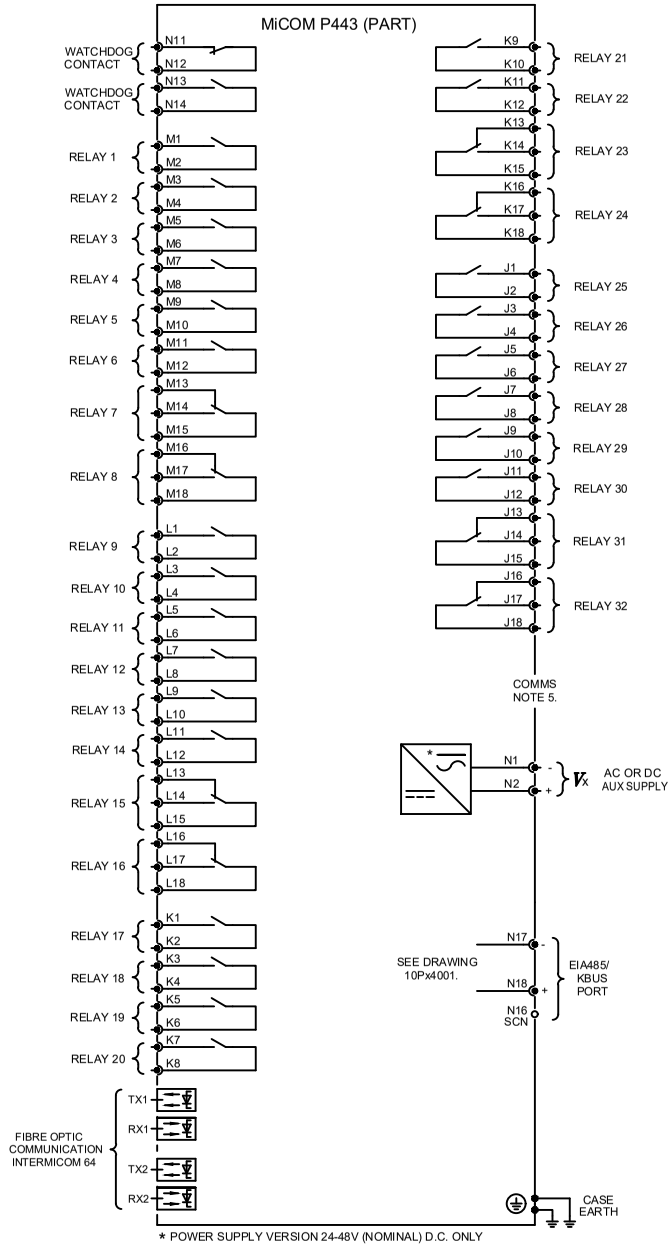



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. $I_M$ INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
5. FOR COMMS OPTIONS SEE DRAWING 10PX4001
6. WITH C.T. POLARITY SETTING 'STANDARD'.
7. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
8. USED FOR SEF PROTECTION. $I_N$ SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.




* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

SHT.1 & SHT.2 DIAGRAMS ARE IDENTICAL APART FROM :-
- PICTORIAL REPRESENTATION OF RELAY CONTACTS.
- CTs SHOWN CONNECTED (1A SHT.1 & 5A SHT.2).

IEC SYMBOLS

| | | | | | |
|---|---|---|---|---|---|
| Issue: F | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (24 I/P &32 O/P) | | |
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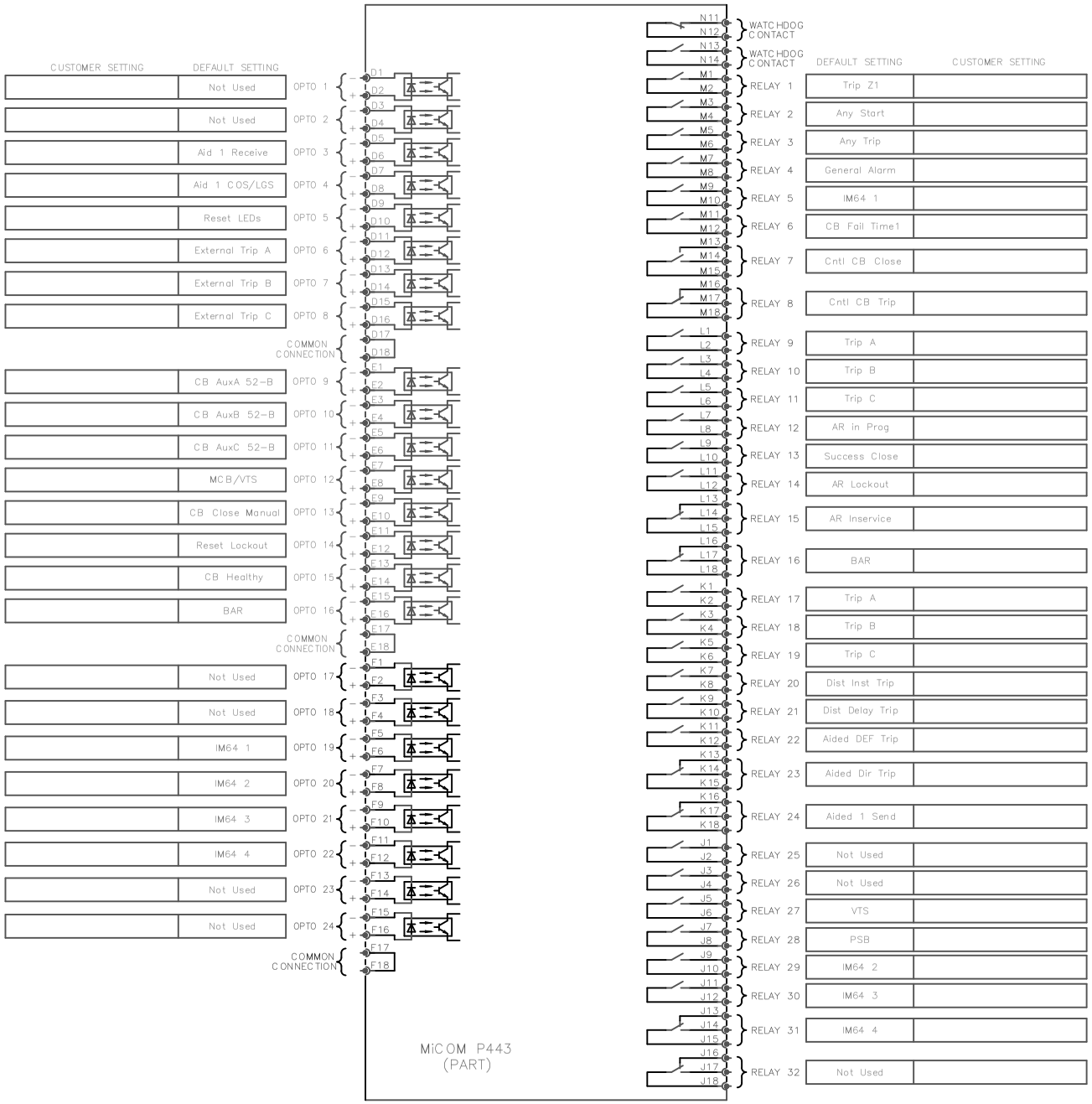


| | | | | | | |
|---|---|---|---|---|---|---|
| Issue: E | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (24 I/P & 32 O/P) | | | |
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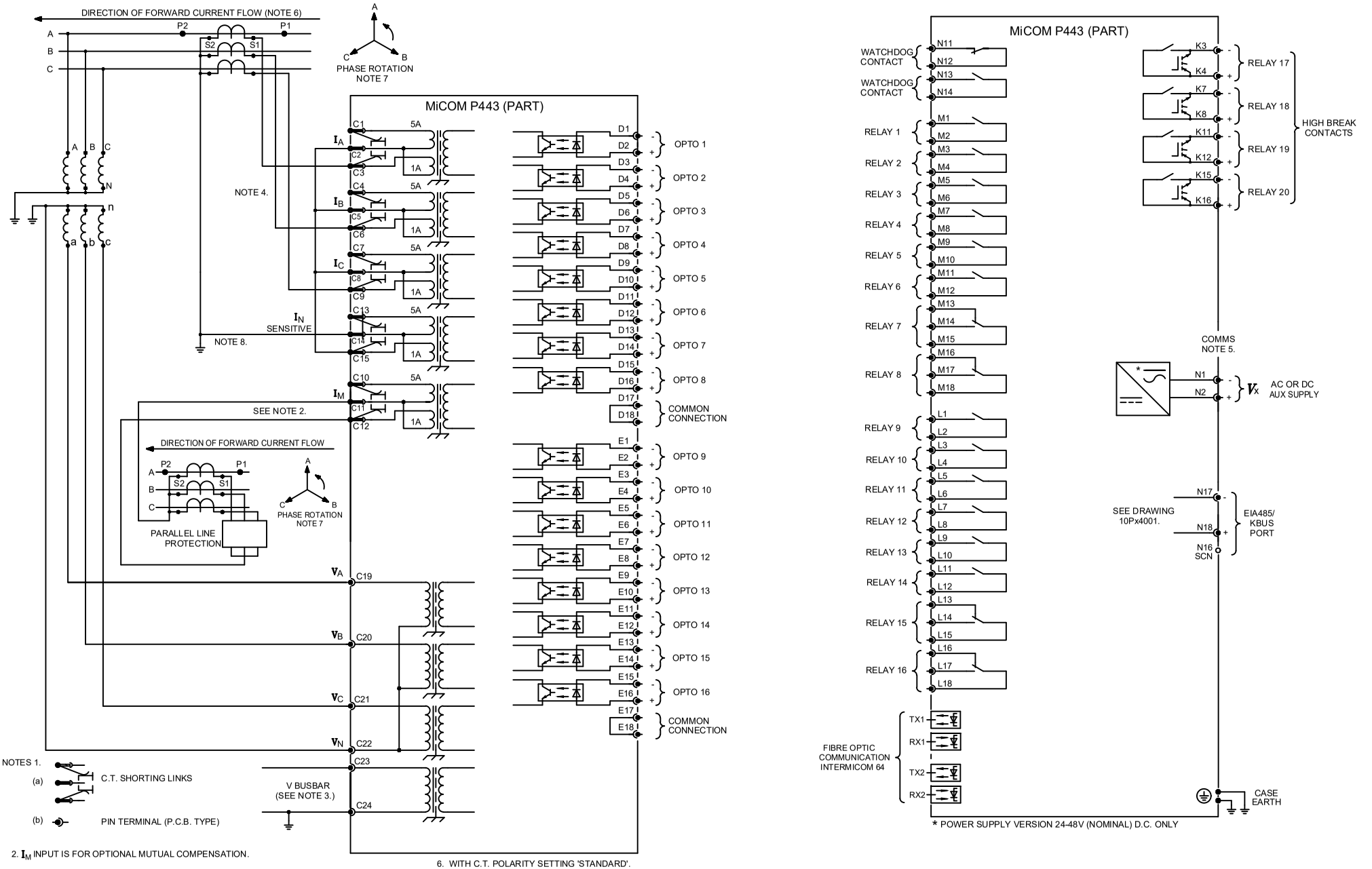
| Date: | Chkd: | | | | Next Sht: - | |




NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. $I_M$ INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
5. FOR COMMS OPTIONS SEE DRAWING 10PX4001
6. WITH C.T. POLARITY SETTING 'STANDARD'.
7. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
8. USED FOR SEF PROTECTION. $I_N$ SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

SHT.1 & SHT.2 DIAGRAMS ARE IDENTICAL APART FROM :-
- PICTORIAL REPRESENTATION OF RELAY CONTACTS.
- CTs SHOWN CONNECTED (1A SHT.1 & 5A SHT.2).

IEC SYMBOLS

| | | | | | |
|---|---|---|---|---|---|
| Issue: G | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (16 I/P & 20 O/P) HIGH BREAK RELAYS | | |
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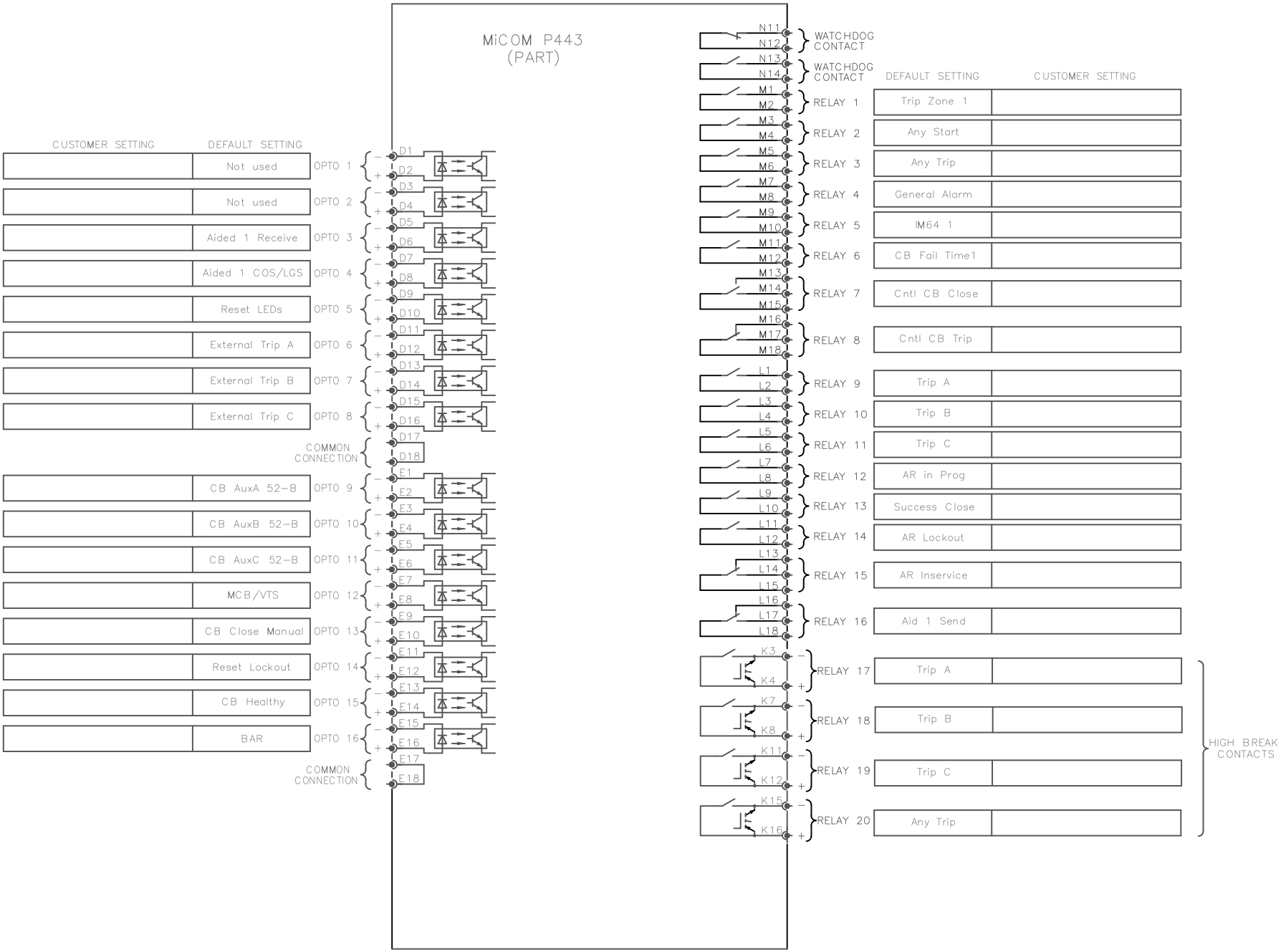
| Date: | Chkd: | | | | GE VERNOVA |

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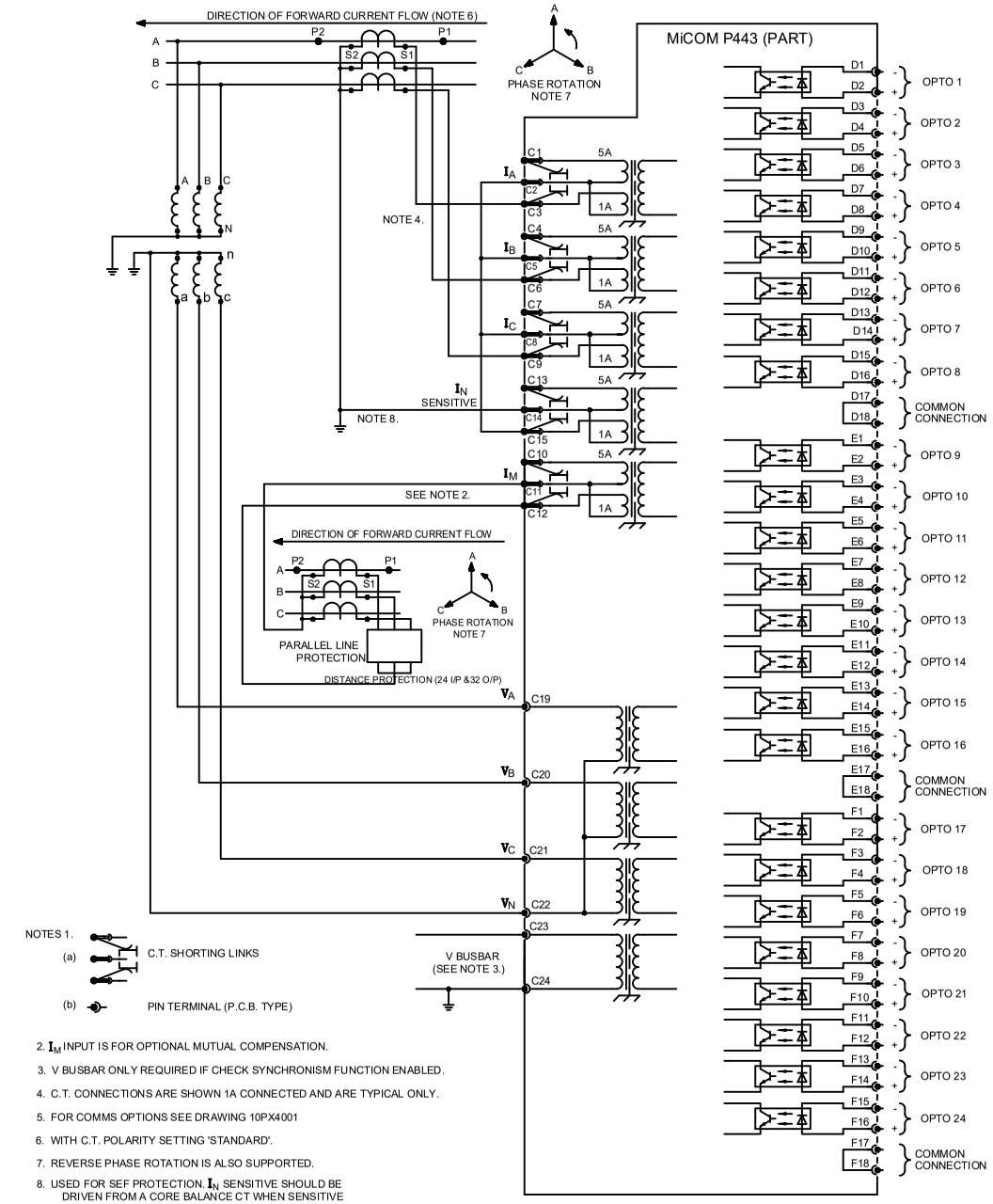
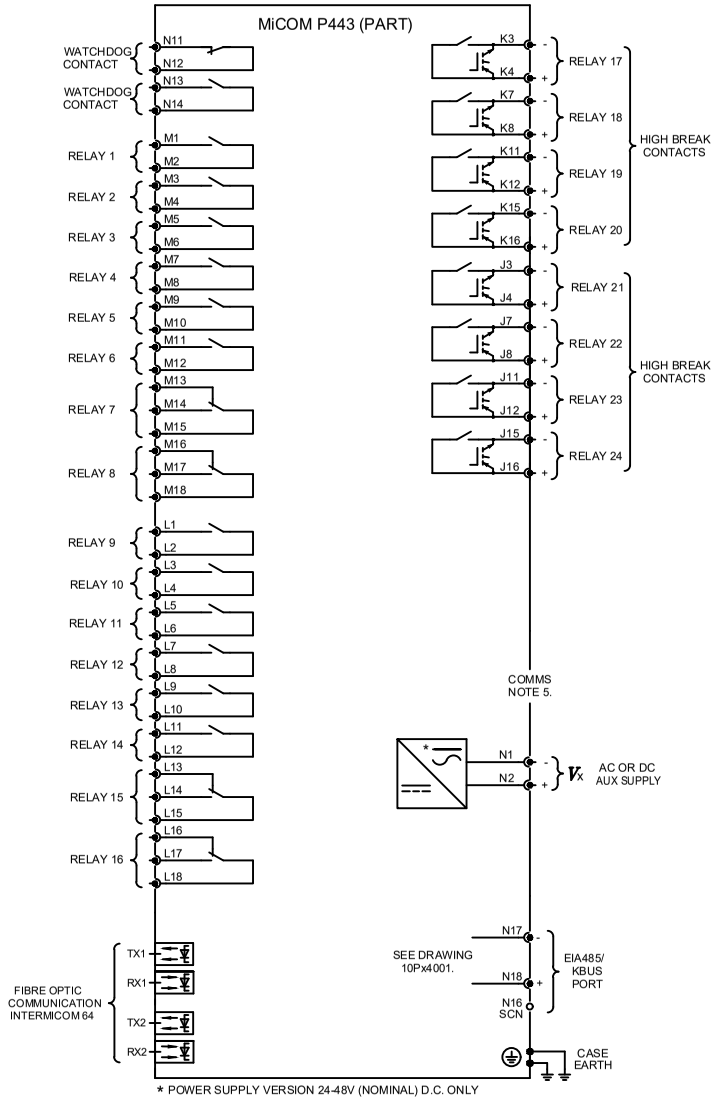
|---|---|---|---|---|---|---|
| Issue: E | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (16 I/P & 20 O/P) WITH HIGH BREAK RELAYS | | | |
| Date: 10/10/2024 | Name: S Burton | PROPRIETARY AND CONFIDENTIAL INFORMATION<br>This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK. | Drg No: **10P44306** | PLM No: A20058051 | Sht: 3 | GE VERNOVA |
| Date: | Chkd: | | | | Next Sht: - | |




NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. $I_M$ INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
5. FOR COMMS OPTIONS SEE DRAWING 10PX4001
6. WITH C.T. POLARITY SETTING 'STANDARD'.
7. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
8. USED FOR SEF PROTECTION. $I_N$ SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

SHT.1 & SHT.2 DIAGRAMS ARE IDENTICAL APART FROM :-
- PICTORIAL REPRESENTATION OF RELAY CONTACTS.
- CTs SHOWN CONNECTED (1A SHT.1 & 5A SHT.2).

IEC SYMBOLS

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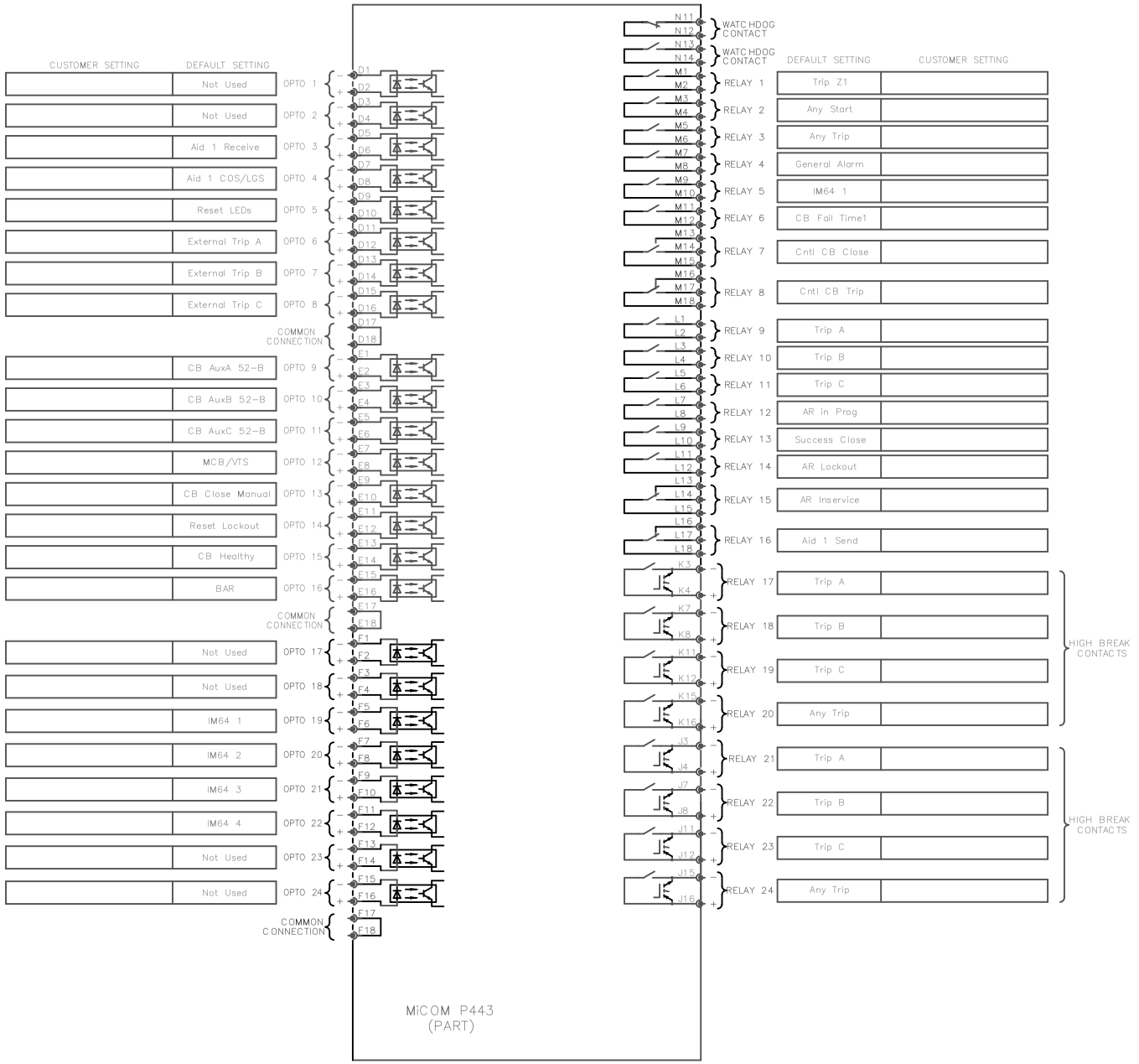
|---|---|---|---|---|---|
| Issue: F | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (24 I/P & 24 O/P) HIGH BREAK RELAYS | | |
| Date: 10/10/2024 | Name: S Burton | PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK. | Drg No: **10P44305** | PLM No: A20058307 | Sht: 1 / Next Sht: 3 |
| Date: | Chkd: | | | | GE VERNOVA |

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| Issue: E | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG: (80TE) DISTANCE PROTECTION (24 I/P & 24 O/P) HIGH BREAK RELAYS | | |
| Date: 10/10/2024 | Name: S Burton | PROPRIETARY AND CONFIDENTIAL INFORMATION<br>This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK. | Drg No: **10P44305** | PLM No: A20058122 | Sht: 3 |
| Date: | Chkd: | | | | Next Sht: - |

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| PART | DESCRIPTION | MATERIAL |
|---|---|---|
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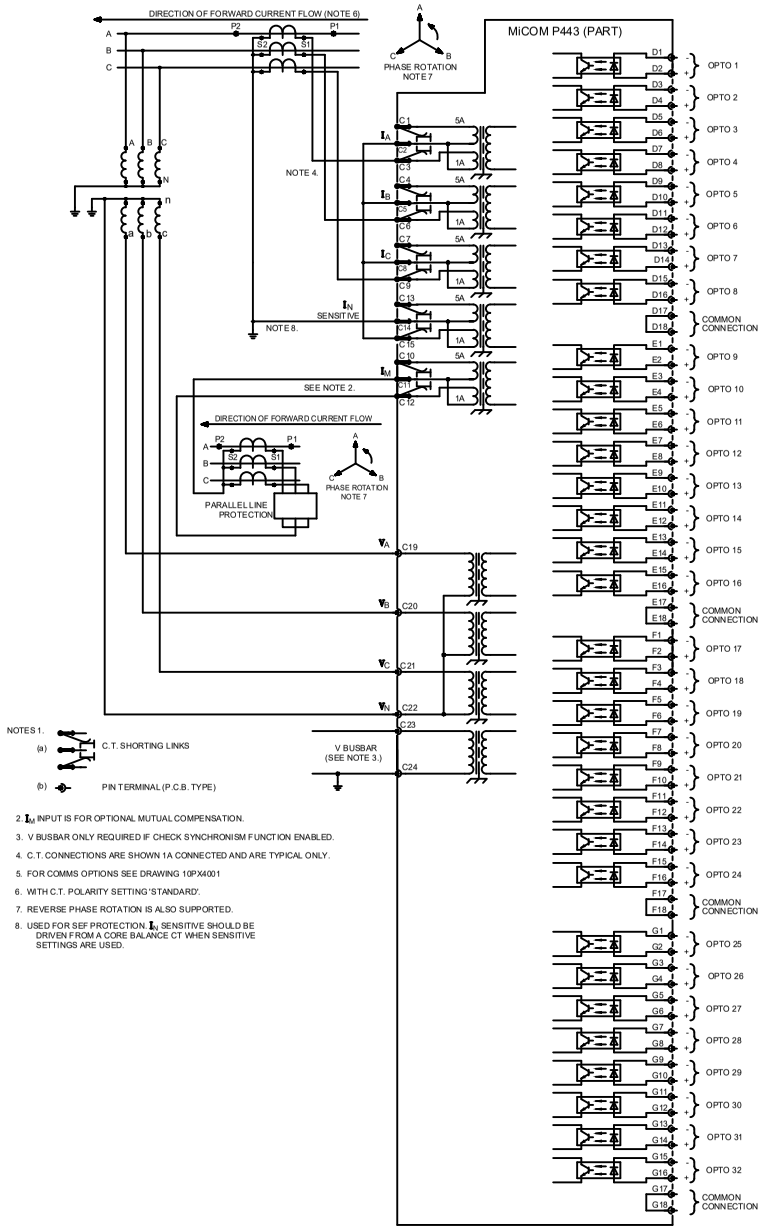
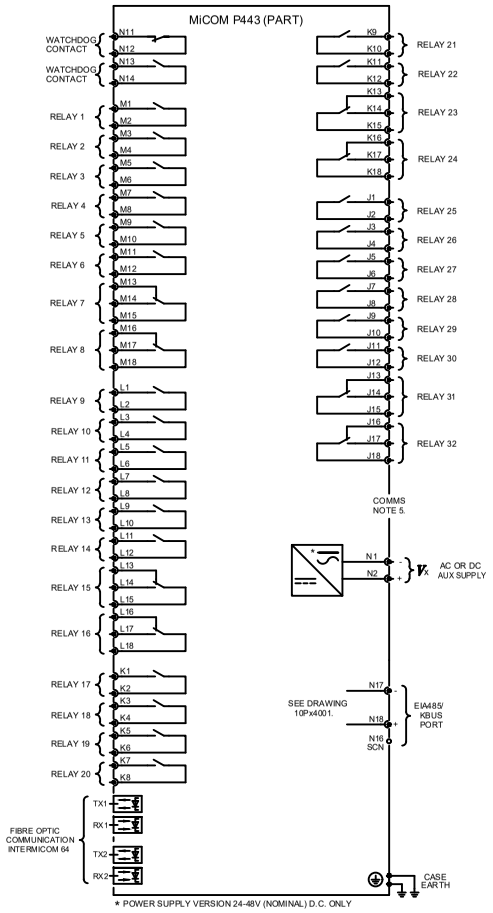



NOTES 1.
(a) C.T. SHORTING LINKS
(b) PIN TERMINAL (P.C.B. TYPE)

2. $I_M$ INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
5. FOR COMMS OPTIONS SEE DRAWING 10PX4001
6. WITH C.T. POLARITY SETTING 'STANDARD'.
7. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
8. USED FOR SEF PROTECTION. $I_N$ SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

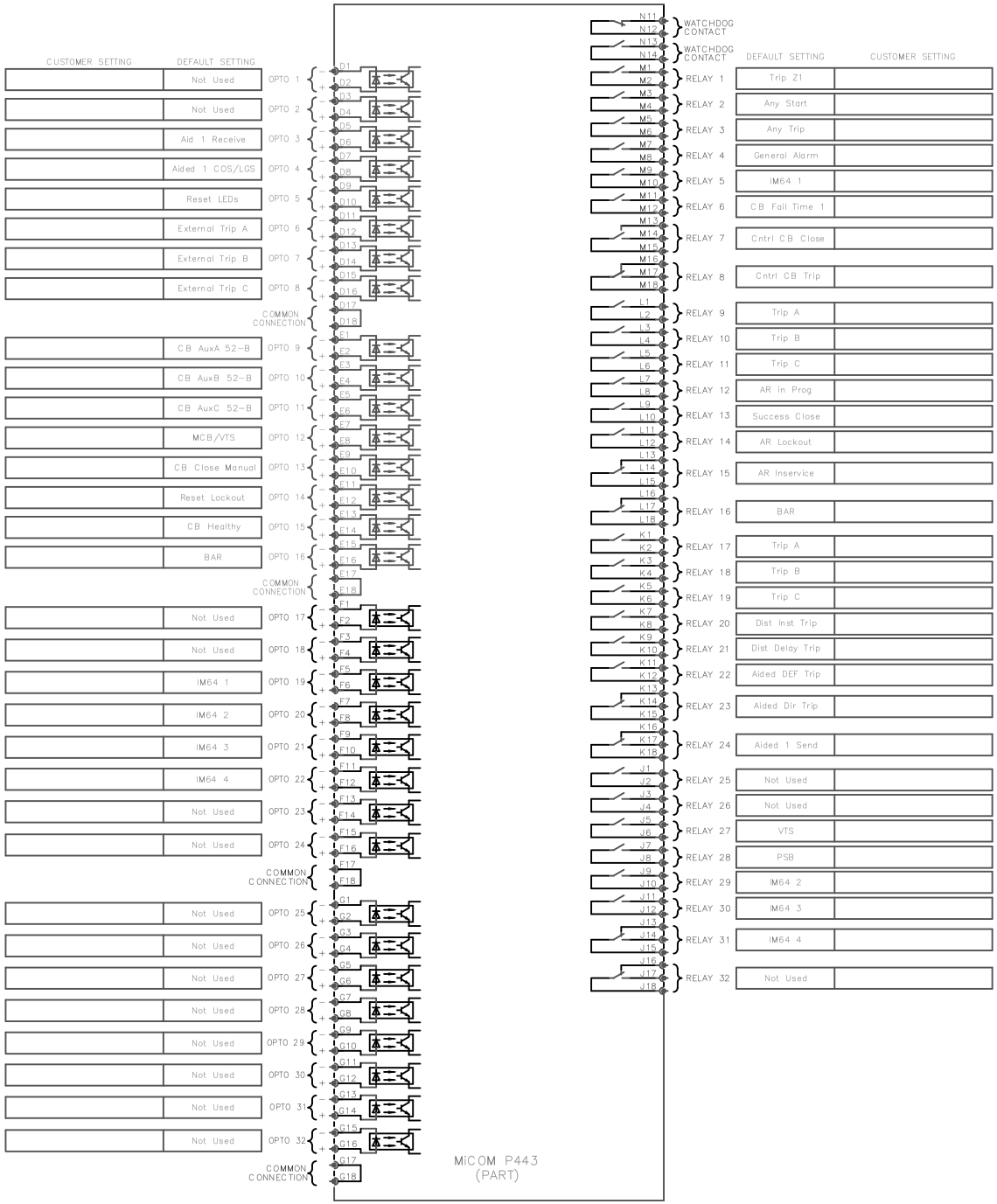



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

SHT.1 & SHT.2 DIAGRAMS ARE IDENTICAL APART FROM :-
- PICTORIAL REPRESENTATION OF RELAY CONTACTS.
- CTs SHOWN CONNECTED (1A SHT.1 & 5A SHT.2).

IEC SYMBOLS

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Next Stage: | | | | | Drg No: 10P44307 | ECN No: CID008567 Outline update only | Revision F | |
| Date: 10/10/2024 | Name: S Burton | Sub-Contractor reference: | Drg Title: EXTERNAL CONNECTION DIAG (80TE) DISTANCE PROTECTION (32 I/P & 32 O/P) | CAD DATA 1:1 DIMENSIONS: mm DO NOT SCALE | Linear Tol mm: Angular Tol deg: | GE VERNOVA | PLM No: A20064626 | Sht: 1 Next Sht: 3 Status: Approved |
| Date: | Chkd: | Finish: | | | | | | |

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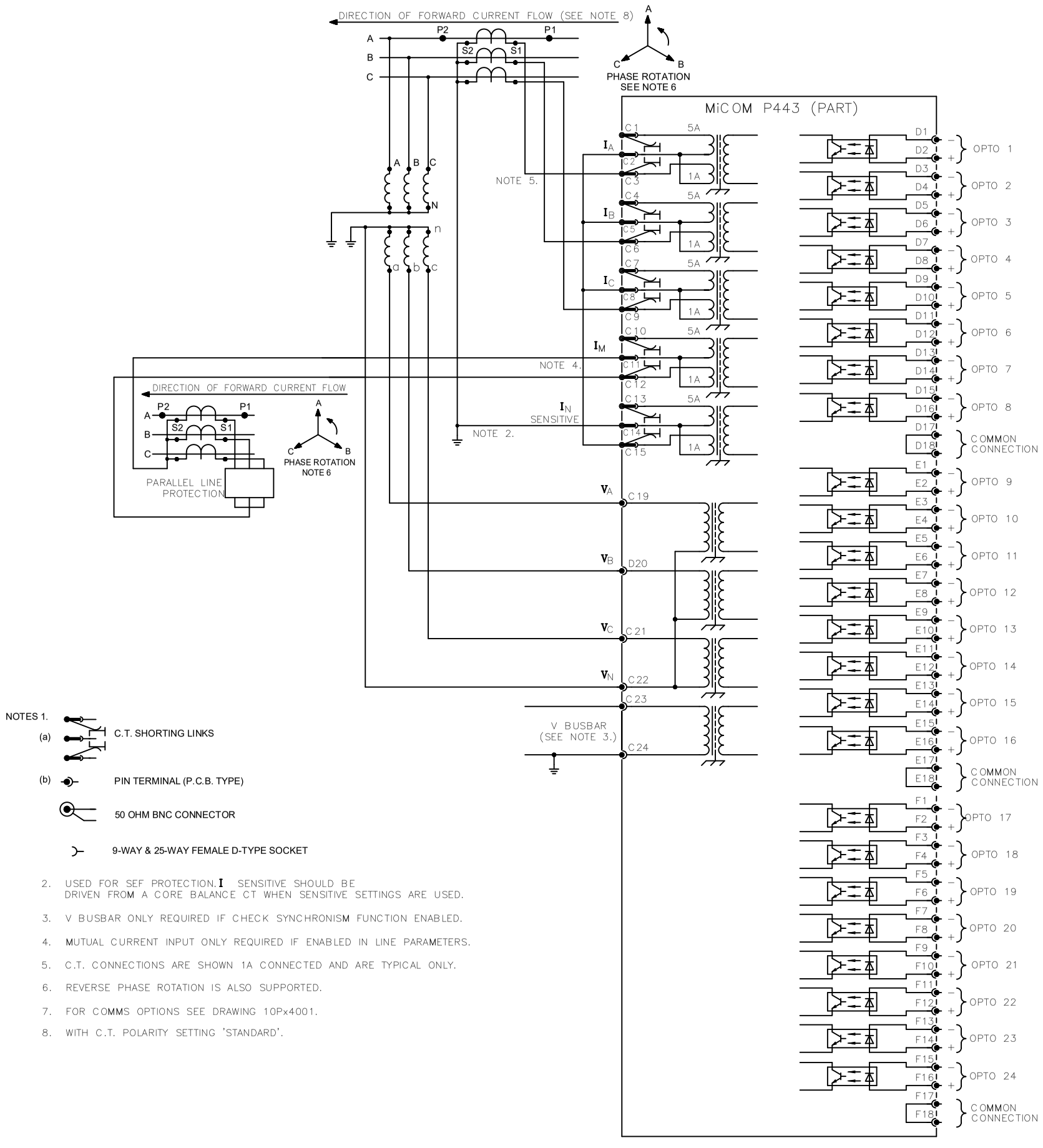
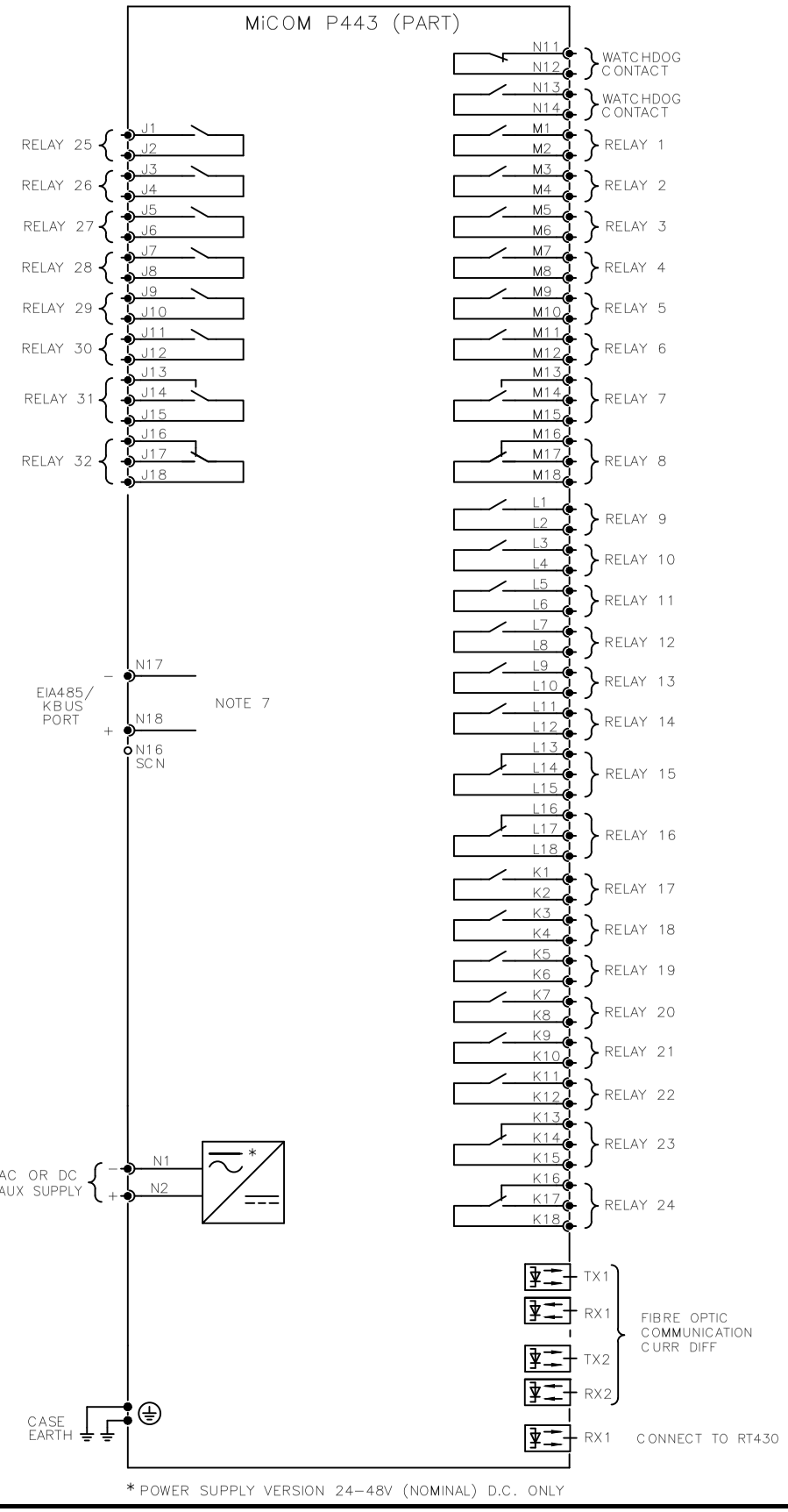
|---|---|---|---|---|---|---|
| Issue: E | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAG (80TE) DISTANCE PROTECTION (32 I/P & 32 O/P) | | | |
| Date: 10/10/2024 | Name: S Burton | PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK. | Drg No: **10P44307** | PLM No: A20064692 | Sht: 3 | GE VERNOVA |
| Date: | Chkd: | | | | Next Sht: - | |




NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

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|---|---|---|---|---|---|---|
| Issue: C | Status: **Approved** | Revision Notes: CID008567 - Outline update only | Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I/32O | | | |
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| Date: | Chkd: | | | | Next Sht: - | |

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