GE VERNOVA

MiCOM P40 Agile

P442, P444

Technical Manual
Numerical Distance Protection IED

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It is the responsibility of the user to verify and validate the suitability of all GE Vernova Grid Automation products. This equipment must be used within its design limits. The proper application including the configuration and setting of this product to suit the power system assets is the responsibility of the user, who is also required to ensure that all local or regional safety guidelines are adhered to. Incorrect application of this product could risk damage to property/the environment, personal injuries or fatalities and shall be the sole responsibility of the person/entity applying and qualifying the product for use.

The content of this document has been developed to provide guidance to properly install, configure and maintain this product for its intended applications. This guidance is not intended to cover every possible contingency that may arise during commissioning, operation, service, or maintenance activities. Should you encounter any circumstances not clearly addressed in this document, contact your local GE Vernova service site.

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1. OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

2. HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however, cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorization. Please contact your local sales office and request the necessary information.

3. SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.



Refer to equipment documentation. Failure to do so could result in damage to the equipment



Risk of electric shock



Risk of damage to eyesight



Earth terminal. Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.



Protective conductor (earth) terminal



Instructions on disposal requirements



The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

4. INSTALLING, COMMISSIONING AND SERVICING

4.1 Lifting Hazards

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

4.2 Electrical Hazards



All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.



Consult the equipment documentation before installing, commissioning, or servicing the equipment.



Always use the equipment as specified. Failure to do so will jeopardize the protection provided by the equipment.



Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.



Isolate the equipment before working on the terminal strips.



Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.



Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.



NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.



Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.



Operate the equipment within the specified electrical and environmental limits.



Before cleaning the equipment, ensure that no connections are energized. Use a lint free cloth dampened with clean water.



Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

4.3 UL/CSA/CUL Requirements

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.



Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).



To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognized parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

4.4 Fusing Requirements



Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).



Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).
For P50 models, use a 1A maximum T-type fuse.
For P60 models, use a 4A maximum T-type fuse.



Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.



CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

4.5 Equipment Connections



Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.



Tighten M4 clamping screws of heavy-duty terminal block connectors to a nominal torque of 1.3 Nm.
Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.



Always use insulated crimp terminations for voltage and current connections.



Always use the correct crimp terminal and tool according to the wire size.



Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

4.6 Protection Class 1 Equipment Requirements



Earth the equipment with the supplied PCT (Protective Conductor Terminal).



Do not remove the PCT.



The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.



Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.



The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations.
For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.



The PCT connection must have low-inductance and be as short as possible.



All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

4.7 Pre-energisation Checklist



Check voltage rating/polarity (rating label/equipment documentation).



Check CT circuit rating (rating label) and integrity of connections.



Check protective fuse or miniature circuit breaker (MCB) rating.



Check integrity of the PCT connection.



Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

4.8 Peripheral Circuitry



Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.



For most GE Vernova equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore, external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.



Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.



Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.

Data communication cables with accessible screens and/or screen conductors, (including optical fibre cables with metallic elements), may create an electric shock hazard in a sub-station environment if both ends of the cable screen are not connected to the same equipotential bonded earthing system.

To reduce the risk of electric shock due to transferred potential hazards:

i. The installation shall include all necessary protection measures to ensure that no fault currents can flow in the connected cable screen conductor.

ii. The connected cable shall have its screen conductor connected to the protective conductor terminal (PCT) of the connected equipment at both ends. This connection may be inherent in the connectors provided on the equipment but, if there is any doubt, this must be confirmed by a continuity test.



iii. The protective conductor terminal (PCT) of each piece of connected equipment shall be connected directly to the same equipotential bonded earthing system.

iv. If, for any reason, both ends of the cable screen are not connected to the same equipotential bonded earth system, precautions must be taken to ensure that such screen connections are made safe before work is done to, or in proximity to, any such cables.

v. No equipment shall be connected to any download or maintenance circuits or connectors of this product except temporarily and for maintenance purposes only.

vi. Equipment temporarily connected to this product for maintenance purposes shall be protectively earthed (if the temporary equipment is required to be protectively earthed), directly to the same equipotential bonded earthing system as the product.



Small Form-factor Pluggable (SFP) modules which provide copper Ethernet connections typically do not provide any additional safety isolation. Copper Ethernet SFP modules must only be used in connector positions intended for this type of connection.

4.9 Upgrading/Servicing



Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energized, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.



Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

INTRODUCTION

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1 INTRODUCTION TO MiCOM GUIDES

This manual provides a functional and technical description of the MiCOM protection relay and a comprehensive set of instructions for the relay's use and application.

The section contents are summarized below:

Safety Guide

P44x-EN IT Introduction

A guide to the MiCOM range of relays and the documentation structure. General safety aspects of handling Electronic Equipment is discussed with particular reference to relay safety symbols. Also a general functional overview of the relay and brief application summary is given.

P44x-EN TD Technical Data

Technical data including setting ranges, accuracy limits, recommended operating conditions, ratings and performance data. Compliance with norms and international standards is quoted where appropriate.

P44x-EN GS Getting Started

A guide to the different user interfaces of the protection relay describing how to start using it. This section provides detailed information regarding the communication interfaces of the relay, including a detailed description of how to access the settings database stored within the relay.

P44x-EN ST Settings

List of all the relay settings, including ranges, step sizes and defaults, together with a brief explanation of each setting.

P44x-EN AP Application Notes

This section includes a description of common power system applications of the relay, calculation of suitable settings, some typical worked examples, and how to apply the settings to the relay.

P44x-EN PL Programmable Logic

Overview of the programmable scheme logic and a description of each logical node. This section includes the factory default (PSL) and an explanation of typical applications.

P44x-EN MR Measurements and Recording

Detailed description of the relays recording and measurements functions including the configuration of the event and disturbance recorder and measurement functions.

P44x-EN FD Firmware Design

Overview of the operation of the relay's hardware and software. This section includes information on the self-checking features and diagnostics of the relay.

P44x-EN CM Commissioning

Instructions on how to commission the relay, comprising checks on the calibration and functionality of the relay.

P44x-EN MT Maintenance

A general maintenance policy for the relay is outlined.

P44x-EN TS Troubleshooting

Advice on how to recognize failure modes and the recommended course of action. Includes guidance on who to contact for advice.

P44x-EN SC SCADA Communications

This section provides an overview regarding the SCADA communication interfaces of the relay. Detailed protocol mappings, semantics, profiles and interoperability tables are not provided within this manual. Separate documents are available per protocol, available for download from our website.

P44x-EN SG Symbols and Glossary

List of common technical abbreviations found within the product documentation.

P44x-EN IN Installation

Recommendations on unpacking, handling, inspection and storage of the relay. A guide to the mechanical and electrical installation of the relay is provided, incorporating earthing recommendations. All external wiring connections to the relay are indicated.

P44x-EN CS Cyber Security (Software Version C7.x only, hardware suffix K)

This section provides an overview about cyber security protection (to secure communication and equipment within substations environment). Cyber security standards and implementation are described.

P44x-EN VH Firmware and Service Manual Version History

History of all hardware and software releases for the product.

2 INTRODUCTION TO MiCOM

MiCOM is a comprehensive solution capable of meeting all electricity supply requirements. It comprises a range of components, systems and services from GE Vernova.

Central to the MiCOM concept is flexibility.

MiCOM provides the ability to define an application solution and, through extensive communication capabilities, to integrate it with your power supply control system.

The components in MiCOM are:

- P range protection relays;
- C range control products;
- M range measurement products for accurate metering and monitoring;
- S range versatile PC support and substation control packages.

MiCOM products include extensive facilities for recording information on the state and behaviour of the power system using disturbance and fault records. They can also provide measurements of the system at regular intervals to a control centre enabling remote monitoring and control to take place.

For up-to-date information on any MiCOM product, visit our website:

GA.support@gevernova.com

3 PRODUCT SCOPE

The MiCOM P442 and P444 Numerical Full Scheme Distance Relays provide comprehensive distance protection for different applications like: lines, cables, tapped lines, lines with multiple zero sequence sources, non-homogeneous lines, series compensated lines and parallel lines.

The independently settable resistive reach for each zone allows easy application to short lines and cable protection. Using well-proven, patented techniques to directionalise, and making full use of digital memory, the relays can be applied in situations that can cause classic distance implementations to maloperate (crosscountry faults and close-up faults).

The MiCOM P442 and P444 are in-built with a library of channel aided scheme logic, supplementary and back-up protection. It provides complete protection (4 alternative setting groups) to solidly earthed systems from distribution to transmission voltage levels.

Three phase tripping with faulted phase indication is provided for all protection functions. In addition models P442 and P444 allow single-phase tripping for the distance protection and the channel aided DEF protection (67N).

The P442 and P444 distance relays equipped with 150 MHz CPU and coprocessor board have been enhanced as described in the following table:

Protection Functions Overview				
ANSI	**IEC 61850**	**Features**	**P442**	**P444**
21P	PDIS	Quadrilateral full scheme phase distance (6 zones)	●	●
21G	PDIS	Quadrilateral full scheme ground distance (6 zones)	●	●
		Load Blinder	●	●
50/51/67	OcpPTOC / RDIR	Directional / non-directional phase overcurrent (2 stages)	●	●
50N / 51N / 67N	EfdPTOC / RDIR	Directional / non-directional stand by earth fault (2 stages)	●	●
67N	EfaPSCH	Channel aided directional earth fault protection (DEF)	●	●
32N		Directional zero sequence power protection	●	●
67/46	NgcPTOC / RDIR	Directional / non-directional negative sequence overcurrent	●	●
27	PTUV	Undervoltage (4 stages, 1st stage DT and IDMT)	●	●
59	PTOV	Overvoltage (4 stages, 1st stage DT and IDMT)	●	●
37		3-phase undercurrent (2 stages)	●	●
81U		Underfrequency (4 stages)	●	●
81O		Overfrequency (2 stages)	●	●
49	PTTR	Thermal overload protection	●	●
50 / 27	PSOF	Switch on to fault / trip on reclose (SOTF/TOR)	●	●
78 / 68	RPSB	Power swing blocking & Out of step tripping (using PSL)	●	●
85	PSCH	Channel aided schemes (PUP, POP, Blocking)	●	●
		Weak Infeed (WI) Echo logic	●	●
		Accelerated trip feature: Loss of Load - Zx extension	●	●
46BC		Broken conductor (open jumper)	●	●
50ST	OcpPTOC	Stub bus protection	●	●
50BF	RBRF	Circuit breaker failure	●	●

Protection Functions Overview				
ANSI	**IEC 61850**	**Features**	**P442**	**P444**
	PTRC	Tripping	1/3p	1/3p
79	RREC	Autoreclose (4 shots)	1/3p	1/3p
25	RSYN	Check synchronism	●	●
VTS		Voltage Transformer Supervision (1, 2 & 3 phase fuse failure detection)	●	●
CTS		Current Transformer Supervision	●	●
CVTS		Capacitive Voltage Transformer Supervision	●	●
51FF	PTOC	Emergency Overcurrent on VT failure	●	●
	OptGGIO	Digital inputs	16	24
	RlyGGIO	Output relays (fast output optional)	21	32 or 46
	SV	IEC 61850-9-2 sampled values	●	●
		Front communication port (RS232/K-bus)	●	●
		Rear communication port (RS485/Optic/Ethernet) *	●	●
		Second rear communication port (RS232/RS485/K-Bus)*	option	option
		Time synchronisation port (IRIG-B) *	option	option
		IEC 61850-9-2-LE Sampled Analogue values Ethernet board	option	option

*It may be possible to get all in one particular model.
NA: Not applicable

To complement the wide range of protection functions listed in the table, the P442 and P444 relays are provided with the following **measurement, control, monitoring, post fault analysis** and **self-diagnostic** functions.

- Fault locator
- Display of instantaneous measured and derived values
- Circuit breaker control, status & condition monitoring.
- Trip circuit and coil supervision
- 4 alternative setting groups
- Programmable scheme logic
- Sequence of event recording
- Comprehensive disturbance recording (waveform capture)
- User configurable LEDs
- Local and remote communication ports
- Multiple communication protocol and interface options
- Time synchronisation
- Fully customisable menu texts
- Multi level password protection
- Test facilities
- Power-up diagnostics and continuous self monitoring of the relay
- User friendly setting and analysis software (MiCOM S1 Agile)

Application overview

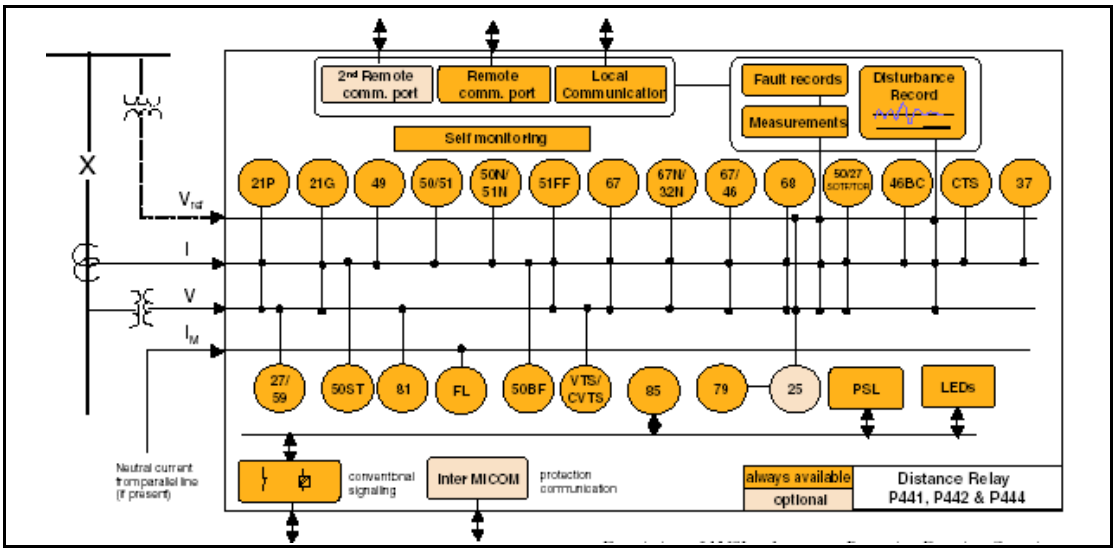


Figure 1: Functional diagram

Rating options

Auxiliary Voltage Rating options		
Features	**P442**	**P444**
24 – 48 Vdc only	●	●
48 – 110 Vdc (30 – 100 Vac)	●	●
110 – 250 Vdc (100 – 240 Vac)	●	●

In/Vn Rating boards options		
Features	**P442**	**P444**
Dual rated CT (1&5A: 100-120 V)	●	●
Module Sum (Σ1A / PXDB)	●	●
IEC 61850-9-2-LE Sampled Analogue values Ethernet board	●	

Communication protocol options

Communication protocol options		
Features	**P442**	**P444**
K-Bus / Courier	●	●
MODBUS	●	●
VDEW (IEC 60870-5-103) (RS485 or Fibre Optic)	●	●
DNP3.0	●	●
IEC 61850 + Courier via rear RS485 port	●	●
IEC 61850 + IEC 60870-5-103 via rear RS485 port	●	●
DNP3.0 over Ethernet and Courier via rear K-Bus/RS485	●	●
IEC 61850-9-2-LE	●	●

3.1 Ordering options

	Variants Order No.
Distance Protection **P442**	P44 2 **
Nominal auxiliary voltage	
24-54 Vdc	7
48-125 Vdc (40-100 Vac)	8
110-250 Vdc (100-240 Vac)	9
In/Vn rating	
Dual rated CT (1 & 5A : 100 - 120V)	1
Module Sum (∑1A / PXDB)	5
Non-conventional input transformers NCIT (IEC 61850-9-2 LE)	C
Hardware options	
Standard version	1
IRIG-B Only (Modulated)	2
Fibre optic converter (Courier, Modbus,IEC60870-5-103 or DNP3) (Note: converts RS485 port to fibre optic; NOT extra port)	3
IRIG-B input and Fibre optic converter (Courier, Modbus,IEC60870-5-103 or DNP3) (Note: converts RS485 port to fibre optic; NOT extra port)	4
Single Ethernet 100Mbit/s	6
Second Rear Comms + InterMiCOM	7
IRIG-B (Modulated) + Second Rear Comms + InterMiCOM	8
Single Ethernet (100Mbit/s) plus IRIG-B (Modulated) Software version '31' and later (Suffix J)	A
Single Ethernet (100Mbit/s) plus IRIG-B (Un-modulated) Software version '31' and later (Suffix J)	B
IRIG-B (Un-modulated) Software version '31' and later (Suffix J)	C
InterMiCOM + Courier Rear Port *	E
InterMiCOM + Courier Rear Port + IRIG-B modulated *	F
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B	H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	J
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B	K
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B	L
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B	M
Redundant Ethernet PRP/HSR**, 2 fibre ports + Modulated IRIG-B	N
Redundant Ethernet PRP/HSR**, 2 fibre ports + Unmodulated IRIG-B	P
* NB: Options available with Software version 45 & later (Design Suffix K)	
** For HSR – contact Alstom for details	
Software options	
16 Logic Inputs & 21 Relay Outputs	B
16 Logic Inputs & 21 Relay Outputs (3 Fast trip)	D
16 Logic Inputs & 21 Relay Outputs (6 Fast trip)	E
16 Logic Inputs & 18 Relay Outputs (4 High Break) *	C
* NB: Option C is only available with Design Suffix K & Software version 40 or later	
Protocol options	
K-Bus	1
Modbus	2
VDEW (IEC 60870-5-103)	3
DNP3.0	4
UCA2 + Courier via rear RS485 port (Ethernet hardware options [i.e. 6] only)	5
IEC61850 + Courier via rear RS485 port *	6
IEC61850 + IEC60870-5-103 via rear RS485 port *	7
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol	8
* NB: IEC61850 Edition 2 available with '82' Software	
Mounting	
Flush Panel Mounting, with Harsh Environment Coating	M
Language	
English, French, German, Spanish	0
English, French, German, Italian	4
Chinese, English or French via HMI, with English or French only via Communications port	C
Software version	
Date and application dependant	**
Customer specific options	
Standard version	0
Customer engineered version: ENEL	1
Customer engineered version: TERNA	2
Customer engineered version: RTE	4
Customer engineered version: general	A
Hardware version	
Model and hardware version dependant	*

		Variants					Order No.		
Distance Protection **P444**	P444						**		
Nominal auxiliary voltage									
24-54 Vdc	7								
48-125 Vdc (40-100 Vac)	8								
110-250 Vdc (100-240 Vac)	9								
In/Vn rating									
Dual rated CT (1 & 5A : 100 - 120V)		1							
Module Sum (∑1A / PXDB)		5							
Non-conventional input transformers NCIT (IEC 61850-9-2 LE) NEW BOARD		C							
Hardware options									
Standard version			1						
IRIG-B input			2						
Fibre optic converter (IEC60870-5-103)			3						
IRIG-B input and Fibre optic converter (IEC60870-5-103)			4						
Single Ethernet 100Mbit/s			6						
Rear Comms + InterMiCOM			7						
Rear Comms + IRIB-B + InterMiCOM			8						
Single Ethernet (100Mbit/s) plus IRIG-B (Modulated) Software version '31' and later (Suffix J)			A						
Single Ethernet (100Mbit/s) plus IRIG-B (Un-modulated) Software version '31' and later (Suffix J)			B						
IRIG-B (Un-modulated) (Software version '31' and later)			C						
InterMiCOM + Courier Rear Port *			E						
InterMiCOM + Courier Rear Port + IRIG-B modulated *			F						
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B			G						
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B			H						
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B			J						
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B			K						
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B			L						
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B			M						
Redundant Ethernet PRP/HSR, 2 fibre ports + Modulated IRIG-B			N						
Redundant Ethernet PRP/HSR, 2 fibre ports + Unmodulated IRIG-B			P						
* NB: Options available with Software version 45 & later (Design Suffix K)									
Models									
1 & 3 Pole tripping/reclosing with 24 inputs & 32 outputs				B					
1 & 3 Pole tripping/reclosing with 24 inputs & 34 ouputs (12 high break)				C					
1 & 3 Pole tripping/reclosing with 24 inputs & 32 outputs (4 fast output contacts)				D					
1 & 3 Pole tripping/reclosing with 24 inputs & 32 outputs (8 fast output contacts)				E					
1 & 3 Pole tripping/reclosing with 24 inputs & 46 outputs				J					
1 & 3 Pole tripping/reclosing with 24 inputs & 46 outputs (4 fast output contacts)				K					
1 & 3 Pole tripping/reclosing with 24 inputs & 46 outputs (8 fast output contacts)				L					
Protocol options					1				
K-Bus					1				
Modbus					2				
VDEW (IEC 60870-5-103) (RS485 or Fibre Optic)					3				
DNP3.0					4				
UCA2					5				
IEC61850 + Courier via rear RS485 port *					6				
IEC61850 + IEC60870-5-103 via rear RS485 port *					7				
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol					8				
* NB: IEC61850 Edition 2 available with '82' Software									
Mounting						M			
Flush/Panel Mounting with Harsh Environment Coating						M			
19" Rack Mounting with Harsh Environmental Coating						N			
Language							0		
English, French, German, Spanish							0		
English, French, German, Italian							4		
Chinese, English or French via HMI, with English or French only via Communications port							C		
Software version									
Date and application dependant									
Customer specific options								0	
Standard version								0	
Customer engineered version: ENEL								1	
Customer engineered version: TERNA								2	
Customer engineered version: RTE								4	
Customer engineered version: General								A	
Hardware version									
Model and hardware version dependant									*

TECHNICAL DATA

Technical Data

P442 & P444 Numerical Distance Protection:
* 1 & 3 Pole tripping/reclosing (P442 & P444)

In/Vn rating (ordering option):
* Dual rated CT (1&5A: 100-120 V)
* Module sum (Σ1A / PXDB)
* IEC 61850-9-2LE Sampled Analogue Values Ethernet board.

Input / Output (I/O)
P442 (with or without Check Synchronism):
* 16I/21O,
* 18I/18O (4 high break)
* 16I/21O (3 or 6 Fast Trip)

P444 (with or without Check Synchronism):
* 24I/32O,
* 24I/46O,
* 24I/34O (12 high break).

Protocol options:
* K-Bus
* Modbus,
* VDEW (IEC 60870-5-103)
* DNP3.0

+ (P442 and P444 only):
* IEC 61850 + Courier via rear RS485 port
* IEC 61850 + IEC 60870-5-103 via rear RS485 port
* DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol

Hardware options (P442 & P444):
* IRIG-B input
* Fibre optic converter (IEC 60870-5-103)
* IRIG-B input and Fibre optic converter (IEC 60870-5-103)
* Single Ethernet 100 Mbit/s
* Rear Comms + InterMiCOM
* Rear Comms + IRIB-B + InterMiCOM
* Single Ethernet (100 Mbit/s) plus IRIG-B (Modulated)
* Single Ethernet (100 Mbit/s) plus IRIG-B (De-modulated)
* IRIG-B (De-modulated)
* InterMiCOM + Courier Rear Port *
* InterMiCOM + Courier Rear Port + IRIG-B modulated *
* Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B
* Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B
* Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B
* Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B
* Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B
* Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B

Mechanical Specification

Design
Modular MiCOM Px40 platform relay available in three different case sizes:
* P442 60TE (12”),
* P444 80TE (16”).

Mounting:
* front of panel flush mounting,
* rack mounted (19” ordering option).

Enclosure Protection

Per IEC 60529: 1989
IP 52 Protection (front panel) against dust and dripping water,
IP 50 Protection for the rear and sides of the case against dust,
IP 10 Product safety protection for the rear due to live connections on the terminal block.

Weight

40TE: approx. 7.3kg
60TE: approx. 9.2kg
80TE: approx. 11.0kg

Terminals

AC Current and Voltage Measuring Inputs
Located on heavy duty (black) terminal block: Threaded M4 terminals, for ring lug connection.
CT inputs have integral safety shorting, upon removal of the terminal block.

General Input/Output Terminals
For power supply, opto inputs, output contacts and COM1 & optional COM2 rear communications.
Located on general purpose (grey) blocks: Threaded M4 terminals, for ring lug connection.

Case Protective Earth Connection
Rear stud connection, threaded M4.
Must be earthed (grounded) using the protective (earth) conductor for safety, minimum earth wire size 2.5 mm^2.

Front Port Serial PC Interface
EIA RS232 DTE, 9 pin D-type female connector.
Courier protocol for interface to MiCOM S1 Agile software.
PEB* rated Maximum cable length 15 m.

Front Download/Monitor Port
EIA RS232, 25 pin D-type female connector.
For firmware downloads. PEB* rated circuit.
Isolation to ELV level.

Rear Communications Port
K-Bus/EIA(RS485) signal levels, two wire
Connections located on general purpose block, M4 screw.
For screened twisted pair cable, multidrop, 1000 m max.

SELV* rated circuit.
Ethernet (copper & fibre)

Optional Rear IRIG-B Interface modulated or un-modulated
BNC socket
SELV* rated circuit.
50 ohms coaxial cable.

Optional Rear Fiber Connection for SCADA/DCS
BFOC 2.5-(ST®)-interface for multi-mode glass fibre type 62.5, as per IEC874-10, 850 nm short-haul fibers, one Tx and one Rx.
Optical budget: 5.6 dB
Data rate: 2.5 Mbits
Max Length: 1000 m

Optional Rear Ethernet Connection for IEC 61850

10 Base T / 100 Base TX Communications
Interface in accordance with IEEE802.3 and IEC 61850
Isolation: 1.5 kV.
Connector type: RJ45
Cable type: Screened Twisted Pair (STP)
Max. cable length: 100 m

100 Base FX Interface
Interface in accordance with IEEE802.3 and IEC 61850
Wavelength: 1300 nm
Fiber: multi-mode 50/125 µm or 62.5/125 µm
Connector style: BFOC 2.5 - (ST®)

Optional Second Rear Communication Port EIA(RS)

232, 9 pin D-type female connector, socket SK4. Courier protocol: K-Bus, or EIA(RS)485 or EIA(RS)232. Maximum cable length: 15 m.

*: PEB = Protective equipotential bonded
*: SELV = Safety/Separated extra low voltage
Both PEB and SELV circuits are safe to touch after a single fault condition.

Optional Rear redundant Ethernet connection for IEC 61850

100 Base FX Interface
Interface in accordance with IEEE802.3 and IEC 61850
Wavelength: 1300 nm
Fiber: multi-mode 50/125 µm or 62.5/125 µm
Connector style: BFOC 2.5 - (ST®)

Fiber defect connector (watchdog relay)
Redundant Ethernet board

Connector (3 terminals):	2NC contacts
Rated voltage:	250 V
Continuous current:	5 A
Short duration current:	30 A for 3 s

Breaking capacity
DC: 50 W resistive
DC: 25 W resistive
AC: 1500 VA resistive (cos ϕ = unity)
AC: 1500 VA inductive (cos ϕ = unity)
Subject to maxima of 5 A and 250 V

Ratings

AC Measuring Inputs
Nominal frequency:
* 50 and 60 Hz (settable)
Operating range:
* 45 to 65 Hz

AC Current
Nominal current (In):
* 1 and 5 A dual rated (separate terminals are provided for the 1A and 5A windings, with the neutral input of each winding sharing one terminal)

Nominal burden per phase 1 A:
* <0.04 VA at rated current

Impedance per phase 1 A:
* <40 mΩ over 0 – 30 In

Nominal burden per phase 5 A:
* <0.15 VA at rated current

Impedance per phase 5 A:
* <8 mΩ over 0 – 30 In

Thermal withstand:
* continuous 4 In
* for 10 s: 30 In
* for 1 s; 100 In

Linear to 64 In (non-offset AC current).

AC Voltage
Nominal voltage (Vn):
* 100 to 120 V phase-phase

Nominal burden per phase:
* < 0.02 VA at 110/√3 V

Thermal withstand:
* continuous 2 Vn
* for 10 s: 2.6 Vn

Power supply

Auxiliary Voltage (Vx)
Three ordering options:
(i) Vx: 24 to 48 Vdc
(ii) Vx: 48 to 110 Vdc, and 40 to 100Vac (rms)
(iii) Vx: 110 to 250 Vdc, and 100 to 240 Vac (rms).

Operating Range
(i) 19 to 65 V (dc only for this variant)
(ii) 37 to 150 V (dc), 32 to 110 V (ac)
(iii) 87 to 300 V (dc), 80 to 265 V (ac).
With a tolerable ac ripple of up to 12% for a dc supply, per IEC 60255-11: 1979.

Nominal Burden
Quiescent burden: 12 W
Additions for energized binary inputs/outputs:
Per opto input:
* 0.09 W…(24 to 54 V),
* 0.12 W...(110/125 V),
* 0.19 W...(220/250 V).

Per energized output relay: 0.13 W
Per energized high break output relay: 0.73 W

Power-up Time
Time to power up < 11 s.

Power Supply Interruption
Per IEC 60255-11: 1979
The relay will withstand a 20 ms interruption in the DC auxiliary supply, without de-energizing.
Per IEC 61000-4-11: 1994
The relay will withstand a 20 ms interruption in an AC auxiliary supply, without de-energizing.

Battery Backup
Front panel mounted Type ½ AA, 3.6 V

Field Voltage Output
Regulated 48 Vdc
Current limited at 112 mA maximum output
The operating range shall be 40 V to 60 V with an alarm raised at <35 V

Digital (“Opto”) Inputs
Universal opto inputs with programmable voltage thresholds. May be energized from the 48 V field voltage, or the external battery supply.
Rated nominal voltage: 24 to 250 Vdc
Operating range: 19 to 265 Vdc
Withstand: 300 Vdc.
Nominal pick-up and reset thresholds:
* Pick-up: approx. 70% of battery nominal set,
* Reset: approx. 64% of battery nominal set.

Recognition time:
* <2 ms with long filter removed,
* <10 ms with half-cycle ac immunity filter on.

Output Contacts

Standard Contacts
General purpose relay outputs for signalling, tripping and alarming:
Rated voltage: 300 V
Continuous current: 10 A
Short-duration current:
* 30 A for 3 s
Making capacity:
* 250 A for 30 ms
* 10 A continuous.
Breaking capacity:
* DC: 50 W resistive
* DC: 62.5 W inductive (L/R = 50 ms)
* AC: 2500 VA resistive (cos ϕ = unity)
* AC: 2500VA inductive (cos ϕ = 0.7)

Response to command: < 5 ms
Durability:
* Loaded contact: 10000 operations minimum,
* Unloaded contact: 100000 operations minimum.

Fast operation and High Break Contacts
Dedicated purpose relay outputs for tripping:
* Uses IGBT technology

Make and Carry:
* 30 Amps for 3 sec, 30 A @ 250 V resistive

Carry:
* 250 Amps dc for 30 ms

Continuous Carry:
* 10 Amps dc

Break Capacity:
* 10 Amps @ 250 V resistive (10,000 operations) 10 Amps @ 250 V L/R=40 ms

Operating time:
* <200 µs & Reset time: 7.5 ms

Watchdog Contacts
Non-programmable contacts for relay healthy/relay fail indication:
Breaking capacity:
* DC: 30 W resistive
* DC: 15 W inductive (L/R = 40 ms)
* AC: 375 VA inductive (cos ϕ = 0.7)

IRIG-B 12X Interface (Modulated)
External clock synchronization per IRIG standard 200-98, format B12X.
Input impedance 6 kΩ at 1000 Hz
Modulation ratio:
* 3:1 to 6:1

Input signal, peak-peak:
* 200 mV to 20 V

IRIG-B 00X Interface (Un-modulated)
External clock synchronization per IRIG standard 200-98, format B00X.
Input signal TTL level
Input impedance at dc 10 kΩ

Environmental Conditions

Ambient Temperature Range
Ambient temperature range
Operating temperature range:
* –25°C to +55°C (or –13°F to +131°F)

Storage and transit:
* –25°C to +70°C (or –13°F to +158°F)

Tested as per IEC 60068-2-1: 2007:
* –25°C (–13°F) storage (96 hours)
* –40°C (–40°F) operation (96 hours)

IEC 60068-2-2: 2007:
* +70°C (+158°F) (storage (96 hours)
* +85°C (+185°F) operation (96 hours)

Ambient Humidity Range
Per IEC 60068-2-3: 1969:
* 56 days at 93% relative humidity and +40 °C

Per IEC 60068-2-30: 1980:
* Damp heat cyclic, six (12 + 12) hour cycles, 93% RH, +25 to +55 °C

Pollution degree
Per IEC 61010-1:1990/A2:1995:
* Normally only non conductive pollution occurs. Occasionally a temporary conductivity caused by condensation must be expected.

Corrosive Environments
Per IEC 60068-2-60: 1995, Part 2, Test Ke, Method (class) 3
Industrial corrosive environment/poor environmental control, mixed gas flow test.
21 days at 75% relative humidity and +30°C
Exposure to elevated concentrations of H_2S, NO_2, Cl_2 and SO_2.

Type Tests

Insulation
Per IEC 60255-27: 2005,
* Insulation resistance > 100 MΩ at 500 Vdc (Using only electronic/brushless insulation tester).

Creepage Distances and Clearances
Per IEC 60255-27: 2005
* Pollution degree 3,
* overvoltage category III,
* impulse test voltage 5 kV.

High Voltage (Dielectric) Withstand
(EIA RS232 ports excepted).
(i) Per IEC 60255-27: 2005, 2 kV rms, AC, 1 minute:
Between all case terminals connected together and the case earth.
Also, between all terminals of independent circuits.
* 1 kV rms AC for 1 minute, across open watchdog contacts and across open contacts of changeover output relays.

(ii) Per ANSI/IEEE C37.90-1989 (reaffirmed 1994):
* 1.5 kV rms AC for 1 minute, across open contacts of changeover output relays.

Impulse Voltage Withstand Test
Per IEC 60255-27: 2005
Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 5 kV, 0.5J
Between all terminals, and all terminals and case earth.

Electromagnetic Compatibility (EMC)

1 MHz Burst High Frequency Disturbance Test
Per IEC 60255-22-1: 2008, Class III,
Common-mode test voltage: 2.5 kV,
Differential test voltage: 1.0 kV,
Test duration: 2 s, Source impedance: 200 Ω
(EIA RS232 ports excepted).

100 kHz Damped oscillatory Test
Per EN 61000-4-18: 2007, Level 3,
Common-mode test voltage: 2.5 kV,
Differential test voltage: 1.0 kV,

Immunity to Electrostatic Discharge
Per IEC 60255-22-2: 1997, Class 4,
* 15 kV discharge in air to user interface, display, and exposed metalwork.

Per IEC 60255-22-2: 1997, Class 3,
* 8 kV discharge in air to all communication ports.
* 6 kV point contact discharge to any part of the front of the product.

Electrical Fast Transient or Burst Requirements
Per IEC 60255-22-4: 2002 and EN 61000-4-4: 2004.
Test severity:
* Class III and IV:

Amplitude:
* 2 kV, burst frequency 5 kHz (Class III),

Amplitude:
* 4 kV, burst frequency 2.5 kHz (Class IV).

Applied directly to auxiliary supply, and applied to all other inputs. (EIA RS232 ports excepted).
Amplitude:
* 4 kV, burst frequency 5 kHz (Class IV).

Applied directly to auxiliary supply.

Fast transient disturbances on power supply (common mode only): 4 kV, 5 ns rise time, 50 ns decay time, 5 kHz repetition frequency, 15 ms burst, repeated every 300 ms for 1 min in each polarity, with a 50 Ω source impedance

Fast transient disturbances on I/O signal, data and control lines (common mode only): 4 kV, 5 ns rise time, 50 ns decay time, 5 kHz repetition frequency, 15 ms burst, repeated every 300 ms for 1 min in each polarity, with a 50 Ω source impedance.

Surge Withstand Capability
Per IEEE/ANSI C37.90.1: 2002:
4 kV fast transient and 2.5 kV oscillatory applied directly across each output contact, optically isolated input, and power supply circuit.

Surge Immunity Test
(EIA RS232 ports excepted).
Per IEC 61000-4-5: 2006 Level 4,
Time to half-value: 1.2 / 50 µs,
* Amplitude: 4 kV between all groups and case earth,
* Amplitude: 2 kV between terminals of each group.

Immunity to Radiated Electromagnetic Energy
Per IEC 60255-22-3: 2000, Class III:
Test field strength, frequency band 80 to 1000 MHz:
* 10 V/m,
* Test using AM: 1 kHz / 80%,
* Spot tests at 80, 160, 450, 900 MHz

Per IEEE/ANSI C37.90.2: 2004:
25 MHz to 1000 MHz, zero and 100% square wave modulated.
Field strength of 35 V/m.

Radiated Immunity from Digital Communications
Per EN61000-4-3: 2002, Level 4:
Test field strength, frequency band 800 to 960 MHz, and 1.4 to 2.0 GHz:
* 30 V/m,

Test using AM:
* 1 kHz / 80%.

Radiated Immunity from Digital Radio Telephones
Per EN 61000-4-3: 2002
* 10 V/m, 900 MHz and 1.89 GHz.

Immunity to Conducted Disturbances Induced by Radio Frequency Fields
Per IEC 61000-4-6: 1996, Level 3,
Disturbing test voltage: 10 Vrms at 1 kHz 80% am., 0.15 to 80 MHz

Power Frequency Magnetic Field Immunity
Per IEC 61000-4-8: 2001, Level 5,
* 100 A/m applied continuously,
* 1000 A/m applied for 3 s.

Per IEC 61000-4-9: 2001, Level 5,
* 1000 A/m applied in all planes.

Per IEC 61000-4-10: 2001, Level 5,
* 100 A/m applied in all planes at 100 kHz/1MHz with a burst duration of 2 s.

Conducted Emissions
Per EN 55022: 1998:
* 0.15 – 0.5 MHz, 79 dBμV (quasi peak) 66 dBμV (average)
* 0.5 – 30 MHz, 73 dBμV (quasi peak) 60 dBμV (average).

Radiated Emissions
Per EN 55022: 1998:
* 30 – 230 MHz, 40 dBμV/m at 10 m measurement distance
* 230 – 1 GHz, 47 dBμV/m at 10 m measurement distance.

EU Directives

EMC Compliance
Per 2004/108/EC:
Compliance to the European Commission Directive on EMC is claimed via the Technical Construction File route. Product Specific Standards were used to establish conformity:
* EN50263: 2000

Product Safety
Per 2006/95/EC:
Compliance with European Commission Low Voltage Directive. Compliance is demonstrated by reference to generic safety standards:
* IEC 60255-27:2005

CE

R&TTE compliance
Radio and telecommunication terminal equipment (R&TTE) directive 99/5/EC. Compliance demonstrated by compliance to both the EMC directives on low voltage directive down to 0 V.
Applicable to rear communication ports.

Mechanical Robustness

Vibration Test
Per IEC 60255-21-1: 1996
Response Class 2
Endurance Class 2

Shock and Bump
Per IEC 60255-21-2: 1995
Shock response Class 2
Shock withstand Class 1
Bump Class 1

Seismic Test
Per IEC 60255-21-3: 1995
Class 2

Cyber Security
(where applicable)

Implementation
Following measures have been implemented:
* Four level access,
* Password strengthening,
* Disabling of unused application and physical ports,
* Inactivity timer,
* Storage of security events,
* NERC-compliant default display.

Standards
* NERC CIP (North American Electric Reliability Corporation – Critical Infrastructure Protection, USA): CIP-002-1, CIP-003-1, CIP-004-1, CIP-005-1, CIP-006-1, CIP-007-1, CIP-008-1 and CIP-009-1
* BDEW (Germany),
* ANSI ISA 99 (USA), IEEE 1686,
* IEC 62351, ISO/IEC 27002,
* NIST SP800-53 (National Institute of Standards and Technology, USA),
* CPNI Guidelines (Centre for the Protection of National Infrastructure, UK).

IEC 61850-9-2 Ethernet board
(option)
* connexion RJ45 or optical fibre
* Antialiasing filter
* Number of logical nodes: up to 6
* Time-delay at message reception: 0 to 3 ms
* Safety control:
  - presence test alarm,
  - synchronization alarm,
  - quality alarm,
  independent per logical node

Timing and Accuracy

PERFORMANCE DATA

For all accuracies specified, the repeatability is ±5%, unless otherwise specified

DISTANCE PROTECTION

All quoted operating times include the closure of the trip output contact.

50 Hz Operation

Minimum tripping time:	13 ms	(SIR = 5)
	14 ms	(SIR = 30)
Maximum tripping time:	18 ms	(SIR = 5)
	21 ms	(SIR = 30)
Typical tripping time:	17 ms	(SIR = 5)
	17.5 ms	(SIR = 30)

100% of faults up to 75% of Zone 1 reach setting trip subcycle at SIR=5.
99% of faults up to 75% of Zone 1 reach setting trip subcycle at SIR=30.

60 Hz Operation

Minimum tripping time:	13 ms	(SIR = 5)
	13 ms	(SIR = 30)
Maximum tripping time:	16.5 ms	(SIR = 5)
	18 ms	(SIR = 30)
Typical tripping time:	14 ms	(SIR = 5)
	16 ms	(SIR = 30)

100% of faults up to 75% of Zone 1 reach setting trip subcycle at SIR=5.
88% of faults up to 75% of Zone 1 reach setting trip subcycle at SIR=30.

Accuracy

Characteristic shape, up to SIR = 30:
±5% for on-angle fault (the set line angle)
±10% for off-angle
(Example: For a 70 degree set line angle, injection testing at 40 degrees would be referred to as "off-angle").
Zone time delay deviations:
±20 ms or 2%, whichever is greater

Sensitivity

Settings < 5/In Ω: (0.05 In*5/(setting*In)) ±5%
Settings > 5/In Ω: 0.05 In ±5%

Distance elements

Pick-up: Setting ±5%
Zone timer deviation:
20 ms or ±2%, whichever is greater
Timer accuracy: ±2 ms
Minimum trip level for IDMT elements:
1.05 × Setting ± 5%
Inverse time stages:
±40 ms or 5%, whichever is greater
Definite time stages:
±40 ms or 2%, whichever is greater
Repeatability: 5%

Sensitivity

Settings < 5/In Ω: (0.05 In*5/(setting*In)) ±5%
Settings > 5/In Ω: 0.05 In ±5%

Transient Overreach: Additional tolerance due to increasing X/R ratios:
±5% over the X/R ratio from 1 to 90

Breaker fail timers accuracy:
20 ms or ±2%, whichever is greater

DIRECTIONAL AND NON-DIRECTIONAL OVERCURRENT

(I>1, I>2, I>3 or I>4)

Accuracy

DT Pick-up:	Setting ±5%
IDMT Pick-up	1.05 × Setting ±5%
DT reset:	0.95 × Setting ±2%
IDMT reset:	0.95 × Setting ±5%

Definite time stages:
±20 ms or ±2%, whichever is greater
Inverse time stages:
±40 ms or ±5%, whichever is greater

NEGATIVE SEQUENCE OVERCURRENT

(I2>1, I2>2, I2>3 or I2>4)

Accuracy

Zone 1:

Pick-up:	Setting ±5%
Reset:	0.95 × Setting ±5%

Definite time stages:
±40 ms or ±5%, whichever is greater

BROKEN CONDUCTOR DETECTION

Accuracy

(I2/I1)

Pick-up:	Setting ±2.5%
Reset:	0.95 × Setting ±2.5%

Definite time stages:
±20 ms or 2%, whichever is greater

DIRECTIONAL AND NON-DIRECTIONAL EARTH FAULT PROTECTION

(IN>1, IN>2, IN>3 or IN>4)

Accuracy

DT Pick-up: Setting ±5%
IDMT Pick-up 1.05 ×Setting ±5%
Drop-off: 0.95 × setting ±5%
Definite time stages:
±20 ms or ±2%, whichever is greater
DT reset: 0.95 × Setting ±2%
Inverse time stages:
40 ms or ±5%, whichever is greater
IDMT reset: 0.95 × Setting ±5%

AIDED DIRECTIONAL EARTH FAULT (D.E.F.) PROTECTION

Accuracy

Zero Sequence Polarisation
pick-up: Setting ±10%
with relay characterist angle = ±90°
Negative Sequence Polarisation
pick-up: Setting ±5%

THERMAL OVERLOAD

Accuracy

Thermal alarm pick-up:
Calculated trip time ±10% ∗
Thermal overload pick-up:
Calculated trip time ±10% ∗
Cooling time accuracy
±15% of theoretical
Repeatability: <5%

∗ *Operating time measured with applied current of 20% above thermal setting*.

NEUTRAL DISPLACEMENT/ RESIDUAL OVERVOLTAGE

(VN>1, VN>2)

Accuracy

DT Pick-up: Setting ±5%
IDMT Pick-up: 1.05 x setting ±5%
Definite time operation:
±20 ms or 2%, whichever is greater
Instantaneous operation: <50 ms
IDMT characteristic shape:
±40 ms or 2%, whichever is greater
Reset: 0.95 × Setting ±5%

UNDERCURRENT PROTECTION

(I<1,I<2)

Accuracy

Pick-up:
±10% or 0.025 In, whichever is greater
Drop-off: ±5%
Timer accuracy:
±40 ms or 2%, whichever is greater
Reset: <15 ms

UNDERVOLTAGE

(V<1, V<2, V<3 or V<4)

Accuracy

DT Pick-up: Setting ±2%
IDMT Pick-up: 0.95 × Setting ±2%
Definite time operation:
±20 ms or 2%, whichever is greater
IDMT characteristic shape:
±40 ms or 2%, whichever is greater
Reset: 1.05 × Setting ±5%

OVERVOLTAGE

(V>1, V>2, V>3 or V>4)

Accuracy

DT Pick-up: Setting ±1%
IDMT Pick-up: 1.05 x Setting ±2%
Definite time operation:
±20 ms or 2%, whichever is greater
IDMT characteristic shape:
±40 ms or 2%, whichever is greater
Reset: 0.98 to 0.995 × Setting ±5%

CIRCUIT BREAKER FAIL AND UNDERCURRENT

Accuracy

Pick-up:
±10% or 0.025 In, whichever is greater
Operating time: <12 ms
Definite time operation:
±20 ms or 2%, whichever is greater

VOLTAGE TRANSFORMER SUPERVISION

Accuracy

Fast block operation: <1 cycle
Fast block reset: <1.5 cycles
Definite time operation:
±20 ms or 2%, whichever is greater

CURRENT TRANSFORMER SUPERVISION

Accuracy

IN> Pick-up: Setting ±5%
VN< Pick-up: Setting ±5%
IN> Drop-off: 0.9 × setting ±5%
VN< Drop-off: (1.05 × setting) ±5% or 1 V whichever is greater
Time delay operation: Setting ±2% or 20 ms whichever is greater
CTS block operation: <1 cycle
CTS reset: <35 ms

CB STATE MONITORING AND CONDITION MONITORING

Accuracy

Timers:
±20 ms or 2%, whichever is greater
Broken current accuracy: ±5%

PROGRAMMABLE SCHEME LOGIC

Accuracy

Output conditioner timer:
Setting ±20 ms or 2%, whichever is greater
Dwell conditioner timer:
Setting ±20 ms or 2%, whichever is greater
Pulse conditioner timer:
Setting ±20 ms or 2%, whichever is greater

AUTORECLOSE AND CHECK SYNCHRONISM

Accuracy

Timers:
Setting ±20 ms or 2%, whichever is greater

MEASUREMENTS AND RECORDING FACILITIES

Accuracy

Typically ±1%, but ±0.5% between 0.2 - 2In/Vn
Current:
Range: 0.05 to 3 In
Accuracy: ±1.0% of reading
Voltage:
Range: 0.05 to 2 Vn
Accuracy: ±1.0% of reading
Power (W):
Range: 0.2 to 2 Vn and 0.05 to 3 In
Accuracy: ±5.0% of reading at unity power factor
Reactive power (Vars):
Range: 0.2 to 2 Vn and 0.05 to 3 In
Accuracy: ±5.0% of reading at zero power factor
Apparent power (VA):
Range: 0.2 to 2 Vn and 0.05 to 3 In
Accuracy: ±5.0% of reading
Energy (Wh):
Range: 0.2 to 2 Vn and 0.2 to 3 In
Accuracy: ±5.0% of reading at zero power factor
Energy (Varh):
Range: 0.2 to 2 Vn and 0.2 to 3 In
Accuracy: ±5.0% of reading at zero power factor
Phase accuracy:
Range: 0° to 360°
Accuracy: ±0.5%

Frequency:
Range: 45 to 65 Hz
Accuracy: ±0.025 Hz

IRIG-B AND REAL TIME CLOCK

Performance

Real time clock accuracy:
< ±2 seconds/day
Modulation ratio: 1/3 or 1/6
Input signal peak-peak amplitude:
200 mV to 20 V
Input impedance at 1000 Hz: 6000 Ω External clock synchronization:
Conforms to IRIG standard 200-98, format B

FAULT AND DISTURBANCE RECORDS

Accuracy
Time and date stamping:
±2 ms of applied fault/event
Fault clearance time: ±2%
CB operating time: ±5ms
Protection operating time: ±2%
Waveshape:
Comparable with applied quantities, ±5% of applied quantities
Trigger positions: ±2%
Record length: 8 records each of 1.8 s duration (1.5 s at 60 Hz)

FAULT LOCATOR

Accuracy
Fault location: ±2% of line length (under reference conditions)*
** Reference conditions solid fault applied on line.*

REFERENCE CONDITIONS

Ambient temperature: 20°C

FREQUENCY TRACKING RANGE

45 to 65 Hz

BREAKER FAILURE

Accuracy
Reset time < 40 ms ±2%
Thresholds: settings ±5%

Ethernet data

(where applicable)

10 Base T /100 Base TX Communications
Interface in accordance with IEEE802.3 and IEC 61850
Isolation 1.5 kV
Cable type: Screened twisted pair STP
Max length: 100 m

100 Base FX Interface
Interface in accordance with IEEE802.3 and IEC 61850
Wavelength: 1300 nm
Fibre: multi-mode 50/125 µm or 62.5/12 5 µm
Connector style: ST

Transmitter Optical Characteristics
(TA = 0°C to 70°C, VCC = 4.75 V to 5.25 V)
BOL= Beginning of Life, EOL= End of Life

Parameter	Sym	Min.	Typ.	Max	Unit
Output Optical Power BOL 62.5/125 µm, NA = 0.275 Fiber EOL	PO	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm, NA = 0.20 Fiber EOL	PO	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic "0" State	PO ("0")			-45	dBm avg.

BOL – Beginning of life
EOL – End of life

Receive Optical Characteristics
(TA = 0°C to 70°C, VCC = 4.75 V to 5.25 V)

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	–31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

InterMiCOM^{64} fiber optic teleprotection

(where applicable)
End-end operation: Table below shows bit transfer time (for multiplexed links, 'MUX' denotes the multiplexer delay).

IM64 Cmd	Applic.	Typical Delay (ms)	Max (ms)	Note
Permissive	Direct fiber	3 to 7	9	No Noise
	Via MUX	5 to 8 + MUX	12 + MUX	BER ≤10-3
Dir. Intertrip	Direct fiber	4 to 8	10	No Noise
	Via MUX	6 to 8 + MUX	13 + MUX	BER ≤10-3

BER – Bit Error Rate for Channel

SETTINGS, MEASUREMENTS AND RECORDS LIST

SETTINGS LIST

GLOBAL SETTINGS (SYSTEM DATA):

Language:
English/French/German/Spanish/Italian/
Chinese (ordering option)
Frequency: 50/60 Hz

CONFIGURATION

Setting Group:	
Select via Menu	
Select via Opto	
Active Settings:	Group 1/2/3/4
Setting Group 1:	Disabled/Enabled
Setting Group 2:	Disabled/Enabled
Setting Group 3:	Disabled/Enabled
Setting Group 4:	Disabled/Enabled
Distance Protection:	Disabled/Enabled
Power Swing:	Disabled/Enabled
Back-Up I>:	Disabled/Enabled
Negative Sequence overcurrent:	Disabled/Enabled
Broken Conductor:	Disabled/Enabled
Earth Fault overcurrent protection:	Disabled/ Zero sequence power/ Earth fault overcurrent
Aided Directional Earth Fault (DEF):	Disabled/Enabled
Voltage Protection:	Disabled/Enabled
Circuit Breaker Fail & I<:	Disabled/Enabled
Supervision (Voltage, Current or Capacitive Voltage Transformer):	Disabled/Enabled
System Checks:	Disabled/Enabled
Thermal Overload:	Disabled/Enabled
I< Protection:	Disabled/Enabled
Residual Overvoltage protection:	Disabled/Enabled
Frequency Protection:	Disabled/Enabled
Internal Autoreclose:	Disabled/Enabled
Input Labels:	Invisible/Visible
Output Labels:	Invisible/Visible
CT & VT Ratios:	Invisible/Visible
Record Control:	Invisible/Visible
Disturbance Recorder:	Invisible/Visible
Measure't Setup:	Invisible/Visible
Communication Settings:	Invisible/Visible
Commission Tests:	Invisible/Visible
Setting Values:	Primary/Secondary
Control Input:	Invisible/Visible
Control Input Config:	Invisible/Visible
Control Input Labels:	Invisible/Visible
Direct Acces:	Disabled/Enabled
InterMiCOM:	Disabled/Enabled
Ethernet NCIT:	Invisible/Visible
Function key:	Invisible/Visible
RP1 / RP2 Read only	Disabled/Enabled
NIC Read only	Disabled/Enabled
PSL Timers:	Invisible/Visible
RearPortt1ReadOnly	Disabled/Enabled
RearPort2ReadOnly	Disabled/Enabled
RearNICReadOnly	Disabled/Enabled
LCD Contrast:	*(Factory pre-set)*

DISTANCE PROTECTION

Line setting

Line Length (Ln): 0.3 to 1000 km (step 0.010)
or 0.2 to 625 miles (step 0.005)
Line Impedance:
0.001×I1 to 500×I1 (step 0.001×I1)
Positive sequence angle (Line Angle, ϑ_1):
–90.0° to +90° (step 0.1°)

Zone setting

Zone Status:	
* Z1X	Enabled/Disabled
* Z2	Enabled/Disabled
* ZP	Enabled/Disabled
* ZQ	Enabled/Disabled
* Z3	Enabled/Disabled
* Z4	Enabled/Disabled
Z1 (Impedance reach:)	0.001/In to 500/In Ω (step 0.001/In Ω)
Z1X	0.001/In to 500/In Ω (step 0.001/In Ω)
kZ1 residual compensation factor:	0 to 7 (step 0.001)
KZ1 residual compensation angle:	0 to +360° (step 0.1°)
R1G (Resistive reach for phase-earth fault):	0 Ω to 400/In Ω (step 0.01/In Ω)
R1Ph (Resistive reach for phase-phasefault):	0 Ω to 400/In Ω (step 0.01/In Ω)
tZ1 (time-delay for Zone 1):	0 to 10 s (step 0.002 s)

Z2:	0.001/In to 500/In Ω (step 0.001/In/Ω)
kZ2 res comp:	0 to 7 (step 0.001)
kZ2 Angle:	0 to 360° (step 0.1°)
R2G:	0 Ω to 400/In Ω (step 0.01/In Ω)
R2Ph:	0 Ω to 400/In Ω (step 0.01/In Ω)
tZ2:	0 to 10 s (step 0.002 s)

Z3:	0.001/In to 500/In Ω (step 0.001/In/Ω)
kZ3/4 res comp:	0 to 7 (step 0.001)
kZ3/4 Angle:	0 to 360° (step 0.1°)
R3G-R4G:	0 Ω to 400/In Ω (step 0.01/In Ω)
R3Ph-R4Ph:	0 Ω to 400/In Ω (step 0.01/In Ω)
tZ3:	0 to 10 s (step 0.002 s)

Z4:	0.001/In to 500/In Ω (step 0.01/In Ω)
tZ4:	0 to 10 s (step 0.01 s)

Zone P – Directionality	Forward/Reverse
Zp:	0.001/In to 500/In Ω (step 0.001/In/Ω)
kZp res comp:	0 to 7 (step 0.001)
kZp Angle:	0 to 360° (step 0.1°)
RpG:	0 Ω to 400/In Ω (step 0.01/In Ω)
RpPh:	0 Ω to 400/In Ω (step 0.01/In Ω)
tZp:	0 to 10 s (step 0.002 s)

Zone Q – Directionality	Forward/Reverse
Zq:	0.001/In to 500/In Ω (step 0.001/In/Ω)
kZq res comp:	0 to 7 (step 0.001)
kZq Angle:	0 to 360° (step 0.1°)
RqG:	0 Ω to 400/In Ω (step 0.01/In Ω)
RqPh:	0 Ω to 400/In Ω (step 0.01/In Ω)
tZq:	0 to 10 s (step 0.002 s)

Zone Setting other parameters

Serial Compensated Line: Enabled/Disabled
Overlap Z mode: Enabled/Disabled
Z1m Tilt Angle: –45° to +45° (step 1°)
Z1p Tilt Angle: –45° to +45° (step 1°)
Z2/Zp/Zq Tilt Angle –45° to +45° (step 1°)
Fwd Z Chgt Delay: 0 to 100ms (step 1ms)
Volt. Memory Validity: 0 to 10 s (step 10 ms)
Earth Current detection: 0 to 0.1×I1 (step 0.01×I1)
Fault locator:

* KZm mutual Comp: 0 to 7 (step1)
* KZm Angle: 0 to 360° (step 1°)

Load Blinder:

* R< Blinder Lim: 0.001/In to 500/In Ω (step 0.001/In/Ω)
* Load/B Angle: 15° to 65° (step 1°)
* Load Blinder V: 1 V to 70 V (step 0.5 V)

Distance Scheme setting

Program mode Standard or open scheme
Standard Modes:

* Basic + Z1X,
* POP Z1,
* POP Z2,
* PUP Z2,
* PUP Forward,
* BOP Z1,
* BOP Z2.

POP = Permissive Overreach Protection
PUP = Permissive Underreach Protection
BOP = Blocking Overreach Protection

Fault type:

* Phase to Ground,
* Phase to Phase,
* Both enabled.

Trip Mode:

* Force 3 Pole,
* 1 Pole Z1 and Carrier Received (CR),
* POP Z1 Z2 and CR.

Signal sent from a zone to the relays setting (open scheme):

* CsZ1 (Carrier sent by Z1),
* CsZ2,
* CsZ4.

Aided scheme on Carrier receipt “Dist CR” (open scheme):

* None,
* PermZ1: Permissive Z1 (Z1 can trip without waiting the end of tZ1 timout),
* PermZ2,
* PermFwd (forward),
* Blocking Z1 (BlkZ1) (Z1 can only trip if a Carrier is not received),
* BlkZ2.

Additional time-delay for PUP Z2, PUP FWD, POP Z1 and POP Z2 schemes: 0 to 1 s (stem 2 ms)
tReversal Guard: 0 to 0.15 s (step 2 ms)
Unblocking schemes (with permissive schemes):

* None,
* Loss of Guard mode,
* Loss of Carrier mode.

TOR (Trip On Reclose)–SOTF (Switch On To Fault) modes enabled or disabled for:
- TOR logic in case of fault in Z1, Z2, Z3 or All Zones,
- SOTF logic in case of fault in Z1, Z2, Z3 or All Zones,
- TOR or SOTF in Distance scheme,
- SOTF logic in case of fault Z1+Rev, Z2+Rev or I>3 Enabled,
- SOTF initiated by level detectors,

SOTF Delay: 10 to 3600 s (step 1 s)
Z1X extension on channel fail: Enabled/Disabled

Weak Infeed

Mode Status: Disabled/Echo/WI Trip & Echo/PAP
Single Pole: Disabled/Enabled
V< Threshold: 10 to 70 V (step 5 V)
Trip time delay: 0 to 1 s (step 2 ms)

Loss of Load (LoL)

Mode Status: Enabled/Disabled
LoL on Channel failed: Enabled/Disabled
I<: 0.05×In to 1×In (step 0.05×In)
LoL Window: 0.01 s to 0.1 s (step 0.01 s)

POWER SWING DETECTION AND BLOCKING

Power Swing detection boundaries:
- Delta R: 0 to 400/ In Ω (step 0.01/In Ω)
- Delta X: 0 to 400/ In Ω (step 0.01/In Ω)

IN Status: Enabled/Disabled
- IN> (%max) 10% to 100% (step 1%)

I2> Status: Enabled/Disabled
- I2> (%max) 10% to 100% (step 1%)

Imax line Status: Enabled/Disabled
- Imax line> (%max): 1×In to 20×In (step 0.01×In)

Delta I Status: Enabled/Disabled
Unblocking time-delay: 0 to 30 s (step 0.1 s)
Blocking zones:
- Z1/Z1X Block: Yes/No
- Z2 Block: Yes/No
- Zp Block: yes/No
- Zq Block: Yes/No
- Z3 Block: Yes/No
- Z4 Block Yes/No

Out of Step (OOS): 1 to 255 (step 1)
Stable swing: 1 to 255 (step 1)

DIRECTIONAL AND NON DIRECTIONAL OVERCURRENT PROTECTION (Back-up I>)

Directional and non directional I> protections: I>1, I>2 (range 0.08–10×In)
Non directional I> protections: I>3, I>4 (range 0.08–32×In)

I>1 Function / I>2 Function:
- Disabled,
- Definite Time (DT),
- IEC Standard inverse
- IEC Very inverse
- IEC Extremely inverse
- UK Long Time Inverse,
- IEEE Moderately Inverse,
- IEEE Very Inverse
- IEEE Extremely Inverse
- US Inverse
- US Short Time Inverse
- IN> (%max) 10% to 100% (step 1%)

I>1 / I>2 Directional:
- Non-directional,
- Directional forward
- Directional reverse

I>1 / I>2 VTS Block: Block/Non-directional
I>1 / I>2 current set: 0.08×In to 10.00×In (step 0.01×In)
I>1 / I>2 Time-delay: 0 to 100 s (step 0.01 s)
I>1 / I>2 Time-delay VTS: 0 to 100 s (step 0.01 s)
I>1 / I>2 Time Multiplier Setting (TMS): 0.025 to 1.2 (step 0.005)
I>1 / I>2 Time Dial: 0.5 to 15 (step 0.1)
I>1 / I>2 Reset characteristics: DT or Inverse
I>1 / I>2 tReset 0 to 100 s (step 0.01 s)

I>3 Status / I>4 Status: Enabled/Disabled
I>3 / I>4 current set: 0.08×In to 32.00×In (step 0.01×In)
I>3 / I>4 Time-delay: 0 to 100 s (step 0.01 s)

NEGATIVE SEQUENCE OVERCURRENT PROTECTION

Directional and non directional I2> protections: I2>1, I2>2 (range 0.08–4×In)
Non directional I2> protections: I2>3, I2>4 (range 0.08–4×In)

I2>1 Function / I2>2 Function:
- Disabled,
- Definite Time (DT),
- IEC Standard inverse
- IEC Very inverse
- IEC Extremely inverse
- UK Long Time Inverse,
- IEEE Moderately Inverse,
- IEEE Very Inverse
- IEEE Extremely Inverse

* US Inverse
* US Short Time Inverse
* IN> (%max) 10% to 100% (step 1%)

I2>1 / I2>2 Directional:
* Non-directional,
* Directional forward
* Directional reverse

I2>1 / I2>2 VTS Block: Block/Non-directional
I2>1 / I2>2 current set: 0.08×In to 4.00×In (step 0.01×In)
I2>1 / I2>2 Time-delay:0 to 100 s (step 0.01 s)
I2>1 / I2>2 Time VTS:0 to 100 s (step 0.01 s)
I2>1 / I2>2 TMS: 0.025 to 1.2 (step 0.005)
I2>1 / I2>2 Time Dial: 0.01 to 100 (step 0.01)
I2>1 / I2>2 Reset characteristics: DT or Inverse
I2>1 / I2>2 tReset 0 to 100 s (step 0.01 s)

I2>3 Status / I2>4 Status: Enabled/Disabled
I2>3 / I2>4 Directional:
* Non-directional,
* Directional forward
* Directional reverse

I2>3 / I2>4 VTS Block: Block/Non-directional
I2>3 / I2>4 current set: 0.08×In to 32.00×In (step 0.01×In)
I2>3 / I2>4 Time-delay:0 to 100 s (step 0.01 s)
I2>3 / I2>4 Time VTS:0 to 100 s (step 0.01 s)

I>2 Char angle –95° to +95° (step 1°)

MAXIMUM OF RESIDUAL POWER – ZERO SEQUENCE POWER

Zero Sequence Power Status: Activated/Disabled
K Time delay factor: 0 to 2 (step 0.2)
Basis Time Delay: 0 to 10 s (step 0.01 s)
Residual current: 0.05×In to 1×In (step 0.01×In)
P0 threshold: 0.3 to 6.0 VA (step 30 mVA)

BROKEN CONDUCTOR DETECTION

Broken conductor: Enabled/Disabled
I2/I1 setting: 0.2 to 1 (step 0.01)
I2/I1Time Delay: 0 to 100 s (step 1 s)
I2/I1 Trip: Enabled/Disabled

DIRECTIONAL AND NON-DIRECTIONAL EARTH FAULT OVERCURRENT PROTECTION

Earth Fault O/C

Directional and non directional IN> protections:
IN>1, IN>2 (range 0.08–10×In)
Non directional IN> protections:
IN>3, IN>4 (range 0.08–32×In)

IN>1 Function / IN>2 Function:
* Disabled,
* Definite Time (DT),
* IEC Standard inverse
* IEC Very inverse
* IEC Extremely inverse
* UK Long Time Inverse,
* IEEE Moderately Inverse,
* IEEE Very Inverse
* IEEE Extremely Inverse
* US Inverse
* US Short Time Inverse
* IN> (%max) 10% to 100% (step 1%)

IN>1 / IN>2 Directional:
* Non-directional,
* Directional forward
* Directional reverse

IN>1 / IN>2 VTS Block: Block/Non-directional
IN>1 / IN>2 current set: 0.08×In to 10.00×In (step 0.01×In)
IN>1 / IN>2 Time-delay:0 to 200 s (step 0.01 s)
IN>1 / IN>2 Time VTS:0 to 200 s (step 0.01 s)
IN>1 / IN>2 TMS: 0.025 to 1.2 (step 0.005)
IN>1 / IN>2 Time Dial: 0.5 to 15 (step 0.01)
IN>1 / IN>2 Reset characteristics: DT or Inverse
IN>1 / IN>2 tReset 0 to 100 s (step 0.01 s)

IN>3 Status / IN>4 Status: Enabled/Disabled
IN>3 / IN>4 Directional:
* Non-directional,
* Directional forward
* Directional reverse

IN>3 / IN>4 VTS Block: Block/Non-directional
IN>3 / IN>4 current set: 0.08×In to 32.00×In (step 0.01×In)
IN>3 / IN>4 Time-delay:0 to 200 s (step 0.01 s)
IN>3 / IN>4 Time VTS:0 to 200 s (step 0.01 s)

IN> Directional

IN2 Char angle –95° to +95° (step 1°)
Polarisation:
* Zero Sequence,
* Negative Sequence.

AIDED DIRECTIONAL EARTH FAULT (DEF) OVERVOLTAGE PROTECTION

Aided DEF Status: Enabled/Disabled
Polarisation:
* Zero Sequence,
* Negative Sequence.

V> Voltage set: 0.5 V to 20 V (step 0.01 V)
IN Forward: 0.05×In to 4×In (step0.01×In)
Time delay: 0s to 10 s (step 0.1 s)
Scheme logic: Shared/Blocking/Permissive
Tripping: Three Phase/Single Phase
Tp: 0 to 1000 ms (step 2 ms)
IN Rev Factor: 0 to 1 (step 0.1)

THERMAL OVERLOAD

Thermal characteristics: Disabled/Single/Dual
Thermal trip: 0.08×In to 3.2×In (step 0.01×In)
Thermal alarm: 50% to 100% (step 1%)
Time constant 1: 1 mn to 200 mn (step 1 mn)
Time constant 2: 1 mn to 200 mn (step 1 mn)

RESIDUAL OVERVOLTAGE

VN Type: Residual/Homopolar*
VN>1 function: Disabled/DT/IDMT
VN>1 voltage set: 1 V to 180 V (step 1 V)
homopolar: 0.5 V to 60 V (step 0.5 V)*
VN>1 Time delay: 0 s to 100 s (step 0.01 s)
VN>1 TMS: 0.5 to 100 (step 0.5)
VN>1 tReset: 0 to 100 s (step 0.5 s)
VN>2 Status: Enabled/Disabled
VN>2 voltage set: 1 V to 180 V (step 1 V)
homopolar: 0.5 V to 60 V (step 0.5 V)*
VN>2 Time delay: 0 s to 100 s (step 0.01 s)

* (software version C7.x only)

UNDERCURRENT PROTECTION

I< mode (threshold activation):
* I<1 status: activated/deactivated
* I<2 status: activated/deactivated

I<1 status: Enabled/Disabled
I<1 current set 0.08×I1 to 4×I1 (step 0.01×I1)
I<1 Time Delay: 0 to 100 s (step 0.01 s)
I<2 status: Enabled/Disabled
I<2 current set 0.08×I1 to 4×I1 (step 0.01×I1)
I<2 Time Delay: 0 to 100 s (step 0.01 s)

VOLTAGE PROTECTION

V< & V> modes (threshold activation):
* V<1 function: activated/deactivated
* V<2 status: activated/deactivated
* V<3 status: activated/deactivated
* V<4 status: activated/deactivated
* V>1 function: activated/deactivated
* V>2 status: activated/deactivated
* V>3 status: activated/deactivated
* V>4 status: activated/deactivated

Undervoltage

V< Measurement mode:
* Phase–Neutrel,
* Phase–Phase

V<1 function: Disabled/DT/IDMT
V<1 voltage set 10 to 120 V (step 1 V)
V<1 Time Delay: 0 to 100 s (step 0.01 s)
V<1 TMS: 0.5 to 100 (step 0.5)

V<2, V<3 or V<4 status: Enabled/Disabled
V<2, V<3, V<4 voltage set: 10 to 120 V (step 1 V)
V<2, V<3 or V<4 Time Delay: 0s to 100 s (step 0.01 s)

Overvoltage

V> Measurement mode:
* Phase–Neutral,
* Phase–Phase,
* Independent

V> % Hysteresis 0.1 to 2 % (step 1 %)
V>1 function: Disabled/DT/IDMT
V>1 voltage set 10 to 120 V (step 1 V)
V>1 Time Delay: 0 to 100 s (step 0.01 s)
V>1 TMS: 0.5 to 100 (step 0.5)

V>2, V>3 or V>4 status: Enabled/Disabled
V>2, V>3, V>4 voltage set: 10 to 120 V (step 1 V)
V>2, V>3 or V>4 Time Delay: 0 s to 100 s (step 0.01 s)

FREQUENCY PROTECTION

Underfrequency

F<1 Status: Disabled/Enabled
F<1 Setting: 45 Hz to 65 Hz (step 0.01 Hz°
F<1 Time Delay: 0 to 100 s (step 0.01 s)

F<2, F<3 or F<4 Status: Disabled/Enabled
F<2, F<3 or F<4 Setting: 45 Hz to 65 Hz (step 0.01 Hz°
F<2, F<3 or F<4 Time Delay: 0 to 100 s (step 0.01 s)

Overfrequency

F>1 Status: Disabled/Enabled
F>1 Setting: 45 Hz to 65 Hz (step 0.01 Hz°
F>1 Time Delay: 0 to 100 s (step 0.01 s)

F>2 Status: Disabled/Enabled
F>2 Setting: 45 Hz to 65 Hz (step 0.01 Hz°
F>2 Time Delay: 0 to 100 s (step 0.01 s)

CIRCUIT BREAKER FAIL AND I< PROTECTION (CB FAIL & I<)

Circuit Breaker Fail

CB Fail 1 Status: Disabled/Enabled
CB Fail 1 timer: 0 to 10 s (step 0.01 s)
CB Fail 2 Status: Disabled/Enabled
CB Fail 2 timer: 0 to 10 s (step 0.01 s)
CB Fail Non I reset:
* I< only,
* CB Open & I<,
* Prot reset & I<,
* Prot reset or I<,
* Disable

CBF Ext reset:
* I< only,
* CB Open & I<,
* Prot reset & I<,
* Prot reset or I<,
* Disable

Undercurrent I<:

I< current set:
0.05×In to 3.2×In (step 0.01×In)

NON-PROTECTION FUNCTIONS SETTINGS

CB CONDITION

CB Operations (number): 0 to 10000 (step 1)
CBA Operations: 0 to 10000 (step 1)
CBB Operations: 0 to 10000 (step 1)
CBC Operations: 0 to 10000 (step 1)
Total IA Broken: 0 to 25000 In^ (step 1 In^)
Total IB Broken: 0 to 25000 In^ (step 1 In^)
Total IC Broken: 0 to 25000 In^ (step 1 In^)
CB Operate time: 0 to 0.5 s (step 0.001)
Reset CB Data: Yes/No
Total 1P Reclosures: 0 to 0.85 s (0.001)
Total 3P Reclosures: 0 to 0.85 s (0.001)
Reset Total A/R: Yes/No

CB MONITOR SETUP

Broken I^: 0 to 2 (step 0.1)
I^Maintenance:
* Alarm Enabled/Alarm Disabled
* 1In^ to 25000In^ (step 1In^)

I^ Lockout:
* Alarm Enabled/Alarm Disabled
* 1In^ to 25000In^ (step 1In^)

Number CB Operations Maintenance:
* Alarm Enabled/Alarm Disabled
* 1 to 10000 (step 1)

CB Operating time Maintenance:
* Alarm Enabled/Alarm Disabled
* 0.005 s to 0.5 s (step 0.001 s)

CB Operating time Lockout Maintenance:
* Alarm Enabled/Alarm Disabled
* 0.005 s to 0.5 s (step 0.001 s)

CB Fault frequency:
* Lock: Alarm Enabled/Alarm Disabled
* Count: 0 to 9999 (step 1)

Fault frequency time: 0 to 9999 s (step 1 s)
Lockout reset: Yes/No
Reset Lockout by: CB Close/User interface
Man Close reset delay: 0.01 to 600 (step 1)

CB CONTROL

CB Control by:
* Disabled,
* Local,
* Remote,
* Local + Remote,
* Opto-input,
* Opto input + Local,
* Opto input + Remote,
* Opto input + Local + Remote.

Close Pulse Time: 0.1 s to 10 s (step 0.01 s)
Trip Pulse Time: 0.1 s to 5 s (step 0.01 s)
Man Close Delay:0.01 s to 600 s (step 0.01 s)
Healthy Window:0.01 s to 9999 s (step 0.01 s)
Check Synchronizing (C/S) Window:
0.01 s to 9999 s (step 0.01 s)
A/R Single Pole: Enabled/Disabled
A/R Three Pole: Enabled/Disabled

CT AND VT RATIOS

Main VT ratios: 100 V to 1M V (step 1 V)
Main VT's Secondary:
80 V to 140 V (step 1 V)
4th VT:
* Primary: 100 V to 1M V (step 1 V)
* Secondary 80 V to 140 V (step 1 V)

Phase CT:
* Primary: 1A to 30 kA (step 1A)
* Secondary 1A/5A

Mutual Compensation CT: (can also be used for Residual Current measurement)
* Primary: 1A to 30 kA (step 1A)
* Secondary 1A/5A

Check Synchronizing (C/S) input:
A (phase A)–N (Neutral)/
B–B/C–N/A–B/B–C/C–A
Main VT Location: Line/Bus
CT polarity: Standard/Inverted
Measured VN Disabled
Measured IN Disabled

SEQUENCE OF EVENT RECORDER (RECORD CONTROL)

Clear Events: Enabled/Disabled
Clear Faults: Enabled/Disabled
Clear Maint: Enabled/Disabled
Alarm Event: Enabled/Disabled
Relay O/P Event: Enabled/Disabled
Opto Input Event: Enabled/Disabled
System Event: Enabled/Disabled
Fault Rec Event: Enabled/Disabled
Maint Rec Event: Enabled/Disabled
Protection Event: Enabled/Disabled
DDB 31 – 0: *(up to):*
DDB 2047 – 2016:
Binary function link strings, selecting which DDB signals will be stored as events, and which will be filtered out

MEASURED OPERATING DATA (MEASURE'T SETUP)

Default Display:
- Description
- Plant reference,
- U – I – Freq,
- P – Q,
- Date and Time.

Local Values: Primary/Secondary
Remote Values: Primary/Secondary
Measurement Ref: VA/VB/VC/IA/IB/IC
Measurement Mode: 0/1/2/3
Demand Interval: 1…99mn (step 1mn)
Distance Unit: Miles/Kilometres
Fault Location:
Distance
Ohms
% of Line

COMMUNICATIONS COLUMN

Courier protocol:
Protocol indicated
RP1 Address: 7 to 34 (step 1)
RP1 Inactiv timer: 1mn to 30 mn (step 1mn)
Physical link: RS485, Fibre optic
RP1 Status
RP1 Port configuration: Kbus/EIA(RS)485
RP1 comms mode:
- IEC 60870 FT1.2
- 10-Bit no parity

RP1 Baud Rate: 9600/19200/38400 bits/s

IEC 60870-5-103 protocol:
Protocol indicated
RP1 Address: 7 to 34 (step 1)
RP1 Inactiv timer: 1mn to 30 mn (step 1 mn)
Baud Rate: 9600/19200/38400 bits/s
Measurement period: 1 to 60 s (step 1 s)
CS103 blocking:
- Disabled,
- Monitor blocking,
- Command blocking.

RP1 Status
RP1 Port configuration: Kbus/EIA(RS)485
RP1 comms mode:
- IEC 60870 FT1.2
- 10-Bit no parity

RP1 Baud Rate: 9600/19200/38400 bits/s

Modbus protocol:
Protocol indicated
RP1 Address: 7 to 34 (step 1)
RP1 Inactiv timer: 1mn to 30 mn (step 1 mn)
Baud Rate: 9600/19200/38400 bits/s
Parity: Odd/Even/None
Physical link: RS485/Fibre optic
Date/Time Format: Enabled/Disabled
RP1 Status
RP1 Port configuration: Kbus/EIA(RS)485
RP1 comms mode:
- IEC60870 FT1.2
- 10-Bit no parity

RP1 Baud Rate: 9600/19200/38400 bits/s

DNP3.0 protocol:
Protocol indicated
RP1 Address: 7 to 34 (step 1)
RP1 Inactiv timer: 1 mn to 30 mn (step 1 mn)
Baud Rate: 9600/19200/38400 bits/s
Parity: Odd/Even/None
Measurement period: 1 to 60 s (step 1 s)
Physical link: RS485/Fibre optic
Time Synhronization: Enabled/Disabled
Date/Time Format: Enabled/Disabled
RP1 Status
RP1 Port configuration: Kbus/EIA(RS)485
RP1 comms mode:
IEC 60870 FT1.2/10-Bit no parity
RP1 Baud Rate: 9600/19200/38400 bits/s
Scale Value indicated
Message Gap: 0 to 50 ms (step 1 ms)
DNP Need Time: 1 to 30 (step 1)
DNP Application fragment size:
100 to 2048 (step 1)
DNP Application fragment timeout:
1 s to 120 s (step 1 s)
DNB SBO timeout: 1 s to 10 s (step 1 s)
DNP link timeout: 0 to 120 s (step 1 s)

Ethernet port, IEC 61850 protocol:
Protocol indicated
Protocol & Scale value indicated,
Network Interface Card (NIC) protocol:
Courier/IEC 60870-5-103/Modbus/DNP3.0
NIC MAC Adress indicated,
NIC tunnel timeout: 1 to 30 mn (step 1 mn)
NIC Link Report: Alarm/Even/None

Ethernet port, DNP3.0 protocol:
Protocol, IP address, subnet mask, NIC MAC address and Gateway address indicated,
DNP time synchro: Enabled/Disabled
DNP Meas scaling:
Primary/Secondary/Normalized
RP1 Address: 7 to 34 (step 1)
RP1 Inactiv timer: 1 mn to 30 mn (step 1 mn)
Baud Rate: 9600/19200/38400 bits/s
Parity: Odd/Even/None
NIC tunnel timeout: 1 to 30 mn (step 1 mn)
NIC Link Report: Alarm/Even/None
SNTP parameters:
Primary and Secondary SNTP addresses displayed
SNTP poll rate: 64 to 1024 s (step 1 s)
SNTP need time: 1 to 30 mn (step 1 mn)
SNTP Application
Fragment size: 100 to 2048 (step 1)
SNTP Application
fragment timeout: 1 s to 120 s (step 1 s)
SNTP SBO timeout: 1 s to 10 s (step 1 s)

Second rear port connection setting:
Protocol and Status indicated
RP2 Port configuration:
Kbus/EIA(RS)485/EIA RS232
RP2 comms mode:
IEC60870 FT1.2/10-Bit no parity
RP2 Address: 0 to 255 (step 1)
RP2 Inactivity timer: 1 to 30 mn (step 1 mn)
RP2 Baud Rate: 9600/19200/38400 bits/s

COMMISSIONING TESTS

Status of opto-isolated inputs indication,
Status of output relays indication,
Status of test port indication,
Status of LEDs indication,
Monitor Bit 1*(up to 8):*
Binary function link strings, selecting which DDB signals have their status visible in the Commissioning menu, for test purposes
Test Mode: Enabled or Disabled
87BB and 50BF trip blocked per zone
Test Pattern:
Configuration of which output contacts are to be energized when the contact test is applied.
Contact test:
No operation/Apply test/Remove test
LEDs test,
Autoreclose test:
No operation/ 3-pole test/
Pole A, B or C test
Red or Green LED status visible,
DDB31-0 to DDB 2047-2016 status visible.

OPTO CONFIGURATION

Opto input voltage range:
* 24-27 V
* 30-34 V
* 48-54 V
* 110-125 V
* 220-250 V

Custom
Opto Input 1
(up to # = max. opto no. fitted)

Custom options allow independent thresholds to be set per opto, from the same range as above

HOTKEYS AND CONTROL INPUTS

Control Inputs operation (CTRL inputs menu) menu:
Status of control inputs indication,
Control inputs operation:
Set/Reset/No operation

Control Inputs configuration (CTRL I/P config. Menu):
The control inputs can be individually assigned to the hotkeys by stetting,
Control input configuration: Latched/Pulsed
Following text displayed in the hotkey menu can be set: Set/Reset / In/Out / Enabled/Disabled / On/Off

Opto Input Labels (Opto I/P Labels menu)
User defined text string to describe the function of the particular opto input.

Teleprotection (InterMiCOM comms)

Source Address: 0 to 10 (step 1)
Received Address: 0 to 10 (step 1)
Baud rate:
* 600 Baud
* 1200 Baud
* 2400 Baud
* 4800 Baud
* 9600 Baud
* 19200 Baud

Channels statistics: Visible/Invisible
* Nbr of tripping messages received
* Nbr blocking messages received,
* Number of messages received: tripping, blocking, total and incorrect,
* Lost messages,
* Elapsed time,
* Reset statistics: Yes/No

Channel diagnostics: Visible/Invisible
* “Data carrier detect” status,
* Frame synchronization status,
* Message status,
* Channel status,
* InterMiCOM hardware status.

Loopback Mode: Internal/External/Disabled
Configuration of which InterMiCOM signals are to be energized when the loopback test is applied.
* User defined test pattern,
* Loopback status

InterMiCOM configuration

IM Msg Alarm Level: 0 to 100.0% (step 1%)
InterMiCOM command Types:
* IM1, IM2, IM3 and IM4 Command types: Disabled/Direct/Blocking
* IM5 Cmd Type: Disabled/Permissive/Direct
* IM6, IM7 and IM8 Command types: Disabled/Permissive/Direct

Fallback mode:
Default/Latched
Default value: 0/1
Frame Synchronization Time:
10 ms to 1.50 s (step 10 ms)

Function keys

10 function keys:
* Status: Disabled/Locked/Unlocked
* Mode: toggled/Normal
* Label: User defined

Ethernet NCIT

(MiCOM P444 relays with IEC 61850-9-2 board only)
Physical Link: Copper/Fibre optic
AntiAlaising Filter: Enabled/Disabled
Merge Unit Delay: 0 to 3 ms (step 250 µs)
Logical Nodes (LN) Arrangement:
VL,IL,IN / VL,IL,IN2 / VL,IL,IN,VB/
VL,IL,IN2,VB / VL,IL,IN2,IN,VB
VL,Sum(2xIL) / VL,IL,IN,2xVB
VL,IL,IN2,2xVB’
Logical Nodes: 4

IED configurator (IEC61850)

MiCOM P442 & P444 only

Switch between active or inactive configuration banks,

MiCOM Configuration Language (MCL) files restoration.

IEC 61850 configuration data displayed:

- Active / inactive Memory banks,
- Configuration revision number of Active or inactive Memory bank,
- IP address, mask and Gateway conneced,
- SNTP: IP address of the primary and secondary servers,
- IED name,
-

IEC61850 GOOSE

- GOENA setting,
- test mode,
- Ignore test flag option

Supervision

VT Supervision

- Time-delay: 1 to 20 s (step 1 s)
- I2&I0 inhibition: 0 to 1A (step1 mA)
- 3P voltage detection: Enabled/Disabled
- Threshold 3P 10 to 70 V (step 1 V)

CT Supervision

- Status: Enabled/Disabled
- VN< Inhibition: 0.5 to 22 V (step 0.5 V) or 2 V to 88 V (step 2 V)
- IN> setting 0.08×In to 4×In (step 0.01×In)
- Time-delay: 0 to 10 s (step 1 s)

CVT Supervision

- Status: Enabled/Disabled
- VN>: 0.5 to 22 V (step 0.5 V)
- Time-delay: 0 to 300 s (step 0.01 s)
- V2 Status: Enabled/Disabled
- V2>: 0.5 to 22 V (step 0.5 V)

Check Synchronization ("system check" menu

Check Synchronism for autoreclosure or Manual CB closure:

- Live bus/dead line: Yes/No
- Dead bus /Live line: Yes/No
- Live bus / Live line: Yes/No

V< Dead line: 5 to 30 V (step 1 V)
V> Live line: 30 to 120 V (step 1 V)
V< Dead bus: 5 to 30 V (step 1 V)
V> live bus: 30 to 120 V (step 1 V)
Differential voltage: 0.5V to 40 V (step 0.1 V)
Diff. frequency: 0.02 Hz to 1 Hz (step 0.01 Hz)
Diff phase 5° to 90° (step 2.5°)
Bus-Line time-delay: 0.1 s to 2 s (step 0.1 s)

Autorecloser

Autoreclose mode:

Number of shots:

- 1P trip mode: 1, 1/3, 1/3/3 or 1/3/3/3
- 3P trip mode: 3, 3/3, 3/3/3 or 3/3/3/3

1P – Dead time 1 0.1 s to 5 s (step 0.01 s)
1P – Dead time 1 0.1 s to 60 s (step 0.01 s)
Dead time 2 1 s to 3600 s (step 1 s)
Dead time 3 1 s to 3600 s (step 1 s)
Dead time 4 1 s to 3600 s (step 1 s)
Reclaim time: 1 to 600 s (step 1 s)
Reclose time-delay: 0.1 s to 10 s (step 0.1 s)
Discrimination time: 0.1 s to 5 s (step 0.01 s)
A/R Inhibit window: 1 s to 3600 s (step 1 s)
C/S on 3P reclosure during Dead time 1: Enabled/Disabled

Autoreclose lockout

Autoreclose is blocked when user defined fault occurs:

- at T2, t2, Tzp or Tzq
- for Loss of Load Trip
- for I>1 or I>2 Trip
- for V<1, V<2, V<3 or V<4 Trip
- for V>1, V>2, V>3 or V>4 Trip
- for IN>1, IN>2, IN>3 or IN>4 Trip
- for Aided D.E.F Trip
- for Zero Sequence Power Trip
- for PAP Trip (specific customer engineered function)
- for Thermal Trip
- for I2>1, I2>2, I2>3 or I2>4 Trip
- for VN>1 or VN>2 Trip
- for I<1 or I<2 Trip
- for F<1, F<2, F<3 or F<4 Trip
- for F>1 or F>2 Trip

Security config

When Option installed

The security configuration features allows password attempts setting and port access enabling:

- Attemps to enter a valid password setting: 0 to 3*
- Attemps time-delay:1 to 3 mn (step 1 mn)*
- Blocking time-delay (incorrect password): 1 to 30 mn (step 1 mn)*
- Front port access: Enabled/Disabled
- Rear Port 1 access: Enabled/Disabled
- Rear Port 2 access: Enabled/Disabled
- Ethernet port access: Enabled/Disabled
- Courier tunneling logical port access: Enabled/Disabled
- IEC 61850 logical port access: Enabled/Disabled
- DNP3 logical port access: Enabled/Disabled

*: displayed on HMI

PSL Timers

Software version C7.x

PSL timers setting from HMI

- Timer 1 to 32:1 ms to 14400 s (step 1 ms)

Outputs Labels

User defined text string to describe the function of the particular relay output contact.

GETTING STARTED

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1 GETTING STARTED

Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4L-2 or later issue, the Technical Data chapter and the ratings on the equipment rating label.

1.1 User interfaces and menu structure

The settings and functions of the MiCOM protection relay can be accessed both from the front panel keypad and LCD, and via the front and rear communication ports. Information on each of these methods is given in this section to describe how to get started using the relay.

1.2 Introduction to the relay

1.2.1 Front panel

The front panel of the relay is shown in the following figures, with the hinged covers at the top and bottom of the relay shown open. Extra physical protection for the front panel can be provided by an optional transparent front cover. With the cover in place read only access to the user interface is possible. Removal of the cover does not compromise the environmental withstand capability of the product but allows access to the relay settings. When full access to the relay keypad is required, to edit the settings, the transparent cover can be unclipped and removed when the top and bottom covers are open. If the lower cover is secured with a wire seal, this will need to be removed. Using the side flanges of the transparent cover, pull the bottom edge away from the relay front panel until it is clear of the seal tab.

The cover can then be moved vertically down to release the two fixing lugs from their recesses in the front panel.

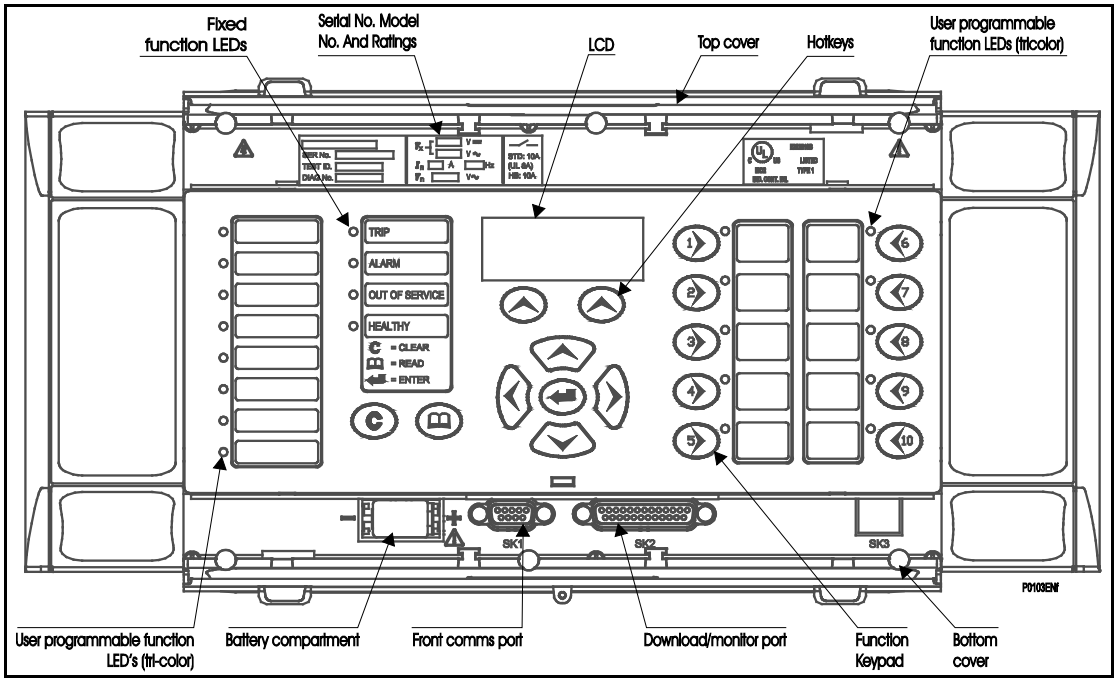


Figure 1: MiCOM P442 & P444 Relay front view (HARDWARE M)

The front panel of the relay includes the following:

- a 16-character by 2- or 3-line (alphanumeric liquid crystal display (LCD).
- a keypad comprising 4 arrow keys (4, 6, 8 and 2), an enter key (5), a clear key (0), and a read key (1) and two additive hotkeys.
- 12 LEDs; 4 fixed function LEDs on the left-hand side of the front panel and 8 programmable function LEDs on the right hand side.
- 10 additional function keys plus 10 additional LEDs.

Hotkey functionality (Figure 1):

- SCROLL: Starts scrolling through the various default displays.
- STOP: Stops scrolling the default display

  for control of setting groups, control inputs and circuit breaker operation.

Function key functionality (Figure 1):

- The relay front panel features control pushbutton switches with programmable LEDs that facilitate local control. Factory default settings associate specific relay functions with these 10 direct-action pushbuttons and LEDs e.g. Enable/Disable the auto-recloser function. Using programmable scheme logic, the user can readily change the default direct-action pushbutton functions and LED indications to fit specific control and operational needs.

Under the top hinged cover:

- the relay serial number, and the relay's current and voltage rating information*.

Under the bottom hinged cover:

- battery compartment to hold the ½ AA size battery which is used for memory back-up for the real time clock, event, fault and disturbance records.
- a 9-pin female D-type front port for communication with a PC locally to the relay (distance of up to 15m) via an EIA(RS)232 serial data connection.
- a 25-pin female D-type port providing internal signal monitoring and high-speed local downloading of software and language text via a parallel data connection.

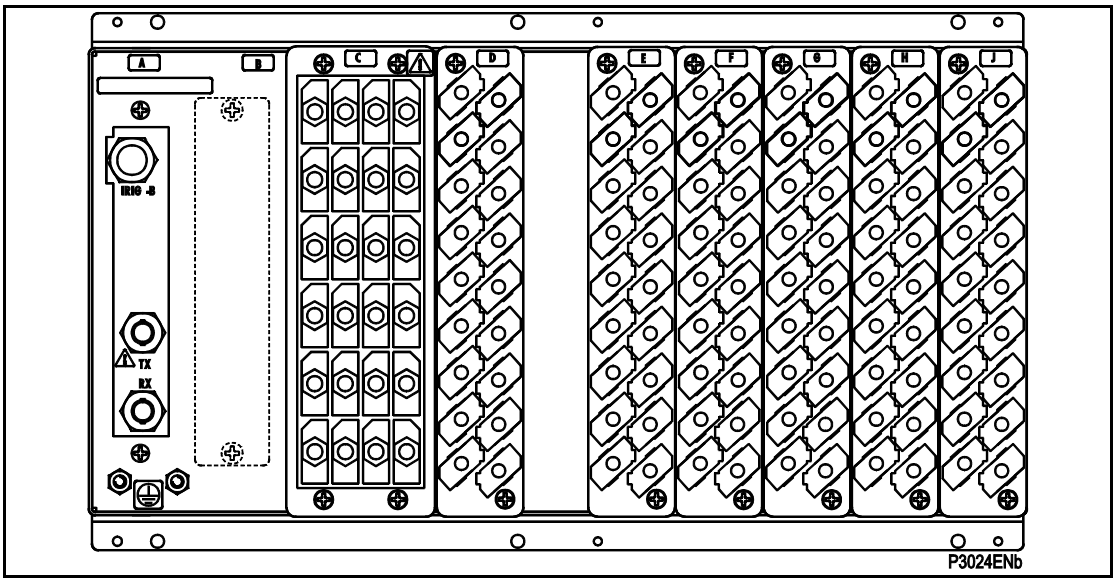
The fixed function LEDs on the left-hand side of the front panel are used to indicate the following conditions:

- Trip (Red) indicates that the relay has issued a trip signal. It is reset when the associated fault record is cleared from the front display. (Alternatively the trip LED can be configured to be self-resetting) *.
- Alarm (Yellow) flashes to indicate that the relay has registered an alarm. This may be triggered by a fault, event or maintenance record. The LED will flash until the alarms have been accepted (read), after which the LED will change to constant illumination, and will extinguish when the alarms have been cleared.
- Out of service (Yellow) indicates that the relay's protection is unavailable.
- Healthy (Green) indicates that the relay is in correct working order and should be on at all times. It will be extinguished if the relay's self-test facilities indicate that there is an error in the relay's hardware or software. The state of the healthy LED is reflected by the watchdog contact at the back of the relay.

To improve the visibility of the settings via the front panel, the LCD contrast can be adjusted using the "LCD Contrast" setting with the last cell in the CONFIGURATION column.

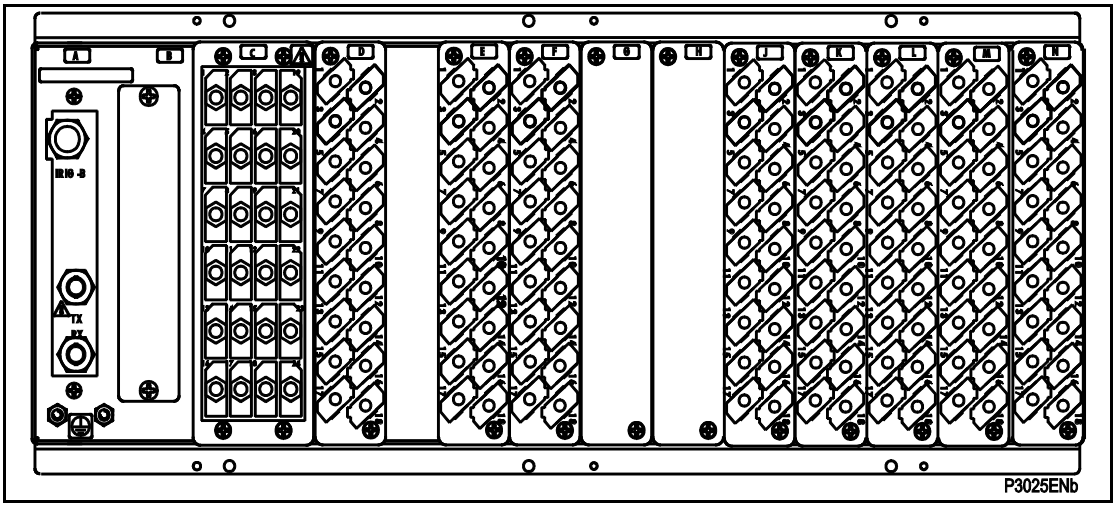
1.2.2 Relay rear panel

The rear panel of the relay is shown in Figure 2 (refer to section P44x/EN IN 'Installation' for terminals connections layout). All current and voltage signals, digital logic input signals and output contacts are connected at the rear of the relay. Also connected at the rear is the twisted pair wiring for the rear EIA(RS)485 communication port, the IRIG-B time synchronising input and the optical fibre rear communication port which are both optional. A second rear port (Courier) and an interMiCOM port are also available.



A –	Optional board *	F –	Output relay/High Break board *
B –	Optional board *	G –	Output relay board
C –	Current and voltage input board	F –	Power supply board
D –	Opto-input board		
E –	Opto-input board	* =	option depending on the model

Figure 2a: P442 Relay rear view (60 TE case)



A –	Optional board *	H –	Relay board
B –	Optional board *	J –	Output relay/High Break board *
C –	Current and voltage input board	K –	Output relay/High Break board *
D –	Opto-input board	L –	Output relay/High Break board *
E –	Opto-input board	M –	Relay board
F –	Opto Input board	N –	Power supply board
G –	Relay board *	* = option depending on the model	

Figure 2b: P444 Relay rear view (80 TE case)

Refer to the wiring diagram in section P44x/EN IN for complete connection details.

1.3 Relay connection and power-up

Before powering-up the relay, confirm that the relay power supply voltage and nominal ac signal magnitudes are appropriate for your application. The relay serial number, and the relay's current and voltage rating, power rating information can be viewed under the top hinged cover. The relay is available in the following auxiliary voltage versions, and these are specified in the table below:

Nominal Ranges	Operative dc Range	Operative ac Range
24 – 48 V dc	19 to 65 V	-
48 – 110 V dc (30 – 100 V ac rms) **	37 to 150 V	24 to 110 V
110 – 250 V dc (100 – 240 V ac rms) **	87 to 300 V	80 to 265 V

** rated for ac or dc operation

Please note that the label does not specify the logic input ratings. The P44x relays are fitted with universal opto isolated logic inputs that can be programmed for the nominal battery voltage of the circuit of which they are a part. See 'Universal Opto input' in the Firmware section for more information on logic input specifications. Please note that the opto inputs have a maximum input voltage rating of 300 V dc at any setting.

Once the ratings have been verified for the application, connect external power capable of delivering the power requirements specified on the label to perform the relay familiarization procedures. Figure 1 and 2 indicates the location of the power supply terminals but please refer to the wiring diagrams in the Installation section for complete installation details ensuring that the correct polarities are observed in the case of dc supply.

1.4 Introduction to the user interfaces and settings options

The relay has thre following interfaces:

- the front panel user interface via the LCD and keypad.
- the front port which supports Courier communication.
- the rear port which supports one protocol of either Courier, Modbus, IEC 60870-5-103 or DNP3.0. The protocol for the rear port must be specified when the relay is ordered.
- the optional Ethernet, dual Ethernet or 9-2 Ethernet port(s),
- The optional second rear port supports Courier protocol.

The measurement information and relay settings which can be accessed from the three interfaces are summarised in Table 1.

	Keypad/ LCD	Courier	Modbus	IEC 870-5-103	DNP3.0	IEC 61850(3)
Display & modification of all settings	•	•	•	•		
Digital I/O signal status	•	•	•	•	•	•
Display/extraction of measurements	•	•	•	•	•	•
Display/extraction of fault records	•	•	•	•	•	•
Extraction of disturbance records		•	•	•	• (Floc in %) (1)	•
Programmable scheme logic settings		•				

	Keypad/ LCD	Courier	Modbus	IEC 870-5-103	DNP3.0	IEC 61850(3)
Reset of fault & alarm records	•	•	•	•	•	
Clear event & fault records	•	•	•	•	•	
Time synchronisation		•	•	•	•	•
Control commands	•	•	•	•	•	

Table 1

1.5 Menu structure

The relay's menu is arranged in a tabular structure. Each setting in the menu is referred to as a cell, and each cell in the menu may be accessed by reference to a row and column address. The settings are arranged so that each column contains related settings, for example all of the disturbance recorder settings are contained within the same column. As shown in Figure 3, the top row of each column contains the heading which describes the settings contained within that column. Movement between the columns of the menu is only possible at the column heading level. A complete list of all the menu settings is given in the manual.

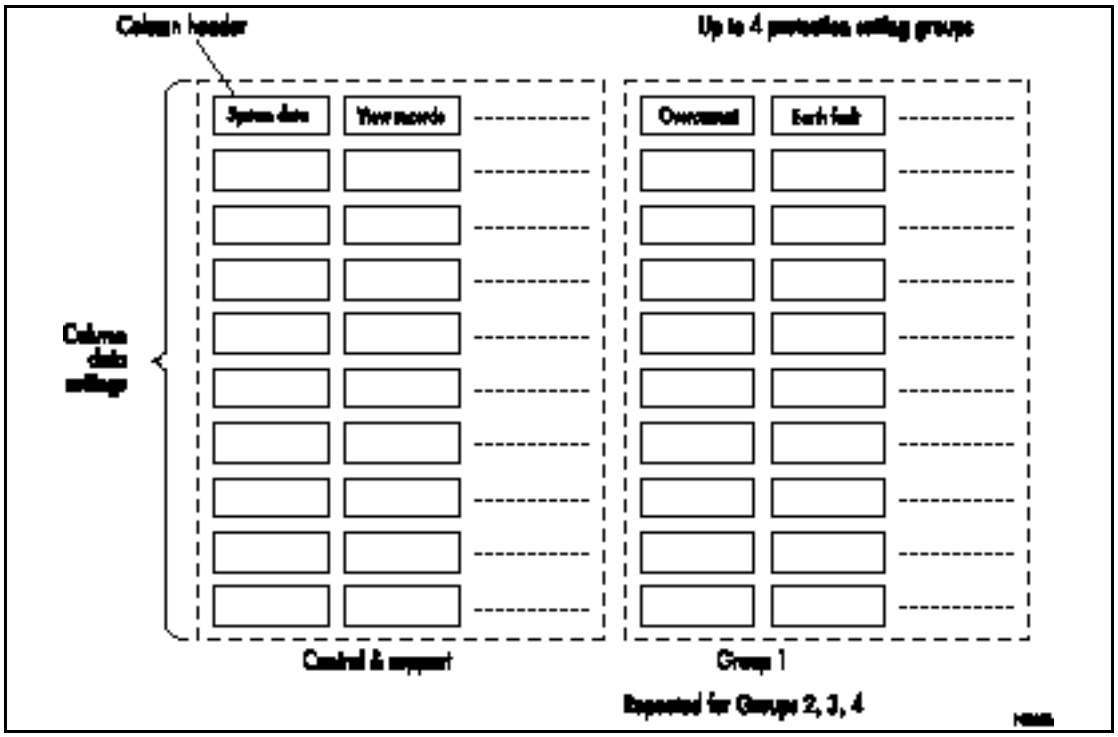


Figure 3: Menu structure

All the settings in the menu fall into one of three categories: protection settings, disturbance recorder settings, or control and support (C&S) settings. One of two different methods is used to change a setting depending on which category the setting falls into. Control and support settings are stored and used by the relay immediately after they are entered. For either protection settings or disturbance recorder settings, the relay stores the new setting values in a temporary 'scratchpad'. It activates all the new settings together, but only after it has been confirmed that the new settings are to be adopted. This technique is employed to provide extra security, and so that several setting changes that are made within a group of protection settings will all take effect at the same time.

1.5.1 Protection settings

The protection settings include the following items:

- protection element settings
- scheme logic settings
- auto-reclose and check synchronisation settings (where appropriate)**
- fault locator settings (where appropriate)*

There are four groups of protection settings, with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements.

1.5.2 Disturbance recorder settings

The disturbance recorder settings include the record duration and trigger position, selection of analogue and digital signals to record, and the signal sources that trigger the recording.

1.5.3 Control and support settings

The control and support settings include:

- relay configuration settings
- open/close circuit breaker*
- CT & VT ratio settings*
- reset LEDs
- active protection setting group
- password & language settings
- circuit breaker control & monitoring settings*
- communications settings
- measurement settings
- event & fault record settings
- user interface settings
- commissioning settings

1.6 Password protection

The menu structure contains three (general) or four (models with Cyber security features) levels of access. The level of access that is enabled determines which of the relay's settings can be changed and is controlled by entry of two different passwords. The levels of access are summarised in Tables 2 or 3.

Access level	Operations enabled
Level 0 No password required	Read access to all settings, alarms, event records and fault records
Level 1 Password 1 or 2	As level 0 plus: Control commands, e.g. circuit breaker open/close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records.
Level 2 As level 1 plus:	Password 2 required All other settings.

Table 2 – Level of access: general case

* may vary according to relay type/model

Level	Meaning	Read Operation	Write Operation
0	Read Some Write Minimal	**SYSTEM DATA** column: Description Plant Reference Model Number Serial Number S/W Ref. Access Level Security Feature **SECURITY CONFIG** column: User Banner Attempts Remain Blk Time Remain Fallback PW level Security Code (user interface only)	Password Entry LCD Contrast (user interface only)
1	Read All Write Few	All data and settings are readable. Poll Measurements	All items writeable at level 0. Level 1 Password setting Select Event, Main and Fault (upload) Extract Events (e.g. via MiCOM S1 Agile)
2	Read All Write Some	All data and settings are readable. Poll Measurements	All items writeable at level 1. Setting Cells that change visibility (Visible/Invisible). Setting Values (Primary/Secondary) selector Commands: - Reset Indication - Reset Demand - Reset Statistics - Reset CB Data / counters - Level 2 Password setting

Level	Meaning	Read Operation	Write Operation
3	Read All Write All	All data and settings are readable. Poll Measurements	All items writeable at level 2. Change all Setting cells Operations: - Extract and download Setting file. - Extract and download PSL - Extract and download MCL61850 (IED Config – IEC 61850) - Extraction of Disturbance Recorder - Courier/Modbus Accept Event (auto event extraction, e.g. via A2R) Commands: - Change Active Group setting - Close / Open CB - Change Comms device address. - Set Date & Time - Switch MCL banks / Switch Conf. Bank in user interface (IED Config – IEC 61850) - Enable / Disable Device ports (in SECURITY CONFIG column) - Level 3 password setting

Table 3 – Level of access: Relays with Cyber Security features

Level management, including password description, management and recovery, is fully described in section P746/EN CS (relays with Cyber Security features).

Each of the passwords is 4 (or 8) characters of upper case text. The factory default for both passwords is AAAA (General case). For models with Cyber Security features: default passwords are blank for Level 1, BBBB for level 2 and AAAA for Level 3. Each password is user-changeable once it has been correctly entered. Entry of the password is achieved either by a prompt when a setting change is attempted, or by moving to the ‘Password’ cell in the ‘System data’ column of the menu. The level of access is independently enabled for each interface, that is to say if level 2 access is enabled for the rear communication port, the front panel access will remain at level 0 unless the relevant password is entered at the front panel. The access level enabled by the password entry will time-out independently for each interface after a period of inactivity and revert to the default level. If the passwords are lost an emergency password can be supplied by contacting GE Vernova with the relay’s serial number and security code (relays with Cyber Security features). The current level of access enabled for an interface can be determined by examining the 'Access level' cell in the 'System data' column, the access level for the front panel User Interface (UI), can also be found as one of the default display options.

The relay is supplied with a default access level of 2 or 3, such that no password is required to change any of the relay settings. It is also possible to set the default menu access level to either level 0 or level 1, preventing write access to the relay settings without the correct password. The default menu access level is set in the ‘Password control’ cell that is found in the ‘System data’ column of the menu (note that this setting can only be changed when level 2 access is enabled).

1.7 Relay configuration

The relay is a multi-function device that supports numerous different protection, control and communication features. In order to simplify the setting of the relay, there is a configuration settings column that can be used to enable or disable many of the functions of the relay. The settings associated with any function that is disabled are made invisible, i.e. they are not shown in the menu. To disable a function change the relevant cell in the ‘Configuration’ column from ‘Enabled’ to ‘Disabled’.

The configuration column controls which of the four protection settings groups is selected as active through the ‘Active settings’ cell. A protection setting group can also be disabled in the

configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

The column also allows all of the setting values in one group of protection settings to be copied to another group.

To do this firstly set the 'Copy from' cell to the protection setting group to be copied, then set the 'Copy to' cell to the protection group where the copy is to be placed. The copied settings are initially placed in the temporary scratchpad, and will only be used by the relay following confirmation.

To restore the default values to the settings in any protection settings group, set the 'Restore defaults' cell to the relevant group number. Alternatively it is possible to set the 'Restore defaults' cell to 'All settings' to restore the default values to all of the relay's settings, not just the protection groups' settings. The default settings will initially be placed in the scratchpad and will only be used by the relay after they have been confirmed. Note that restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.

1.8 Front panel user interface (keypad and LCD)

When the keypad is exposed it provides full access to the menu options of the relay, with the information displayed on the LCD.

The 4, 6, 8 and 2 keys which are used for menu navigation and setting value changes include an auto-repeat function that comes into operation if any of these keys are held continually pressed. This can be used to speed up both setting value changes and menu navigation; the longer the key is held depressed, the faster the rate of change or movement becomes.

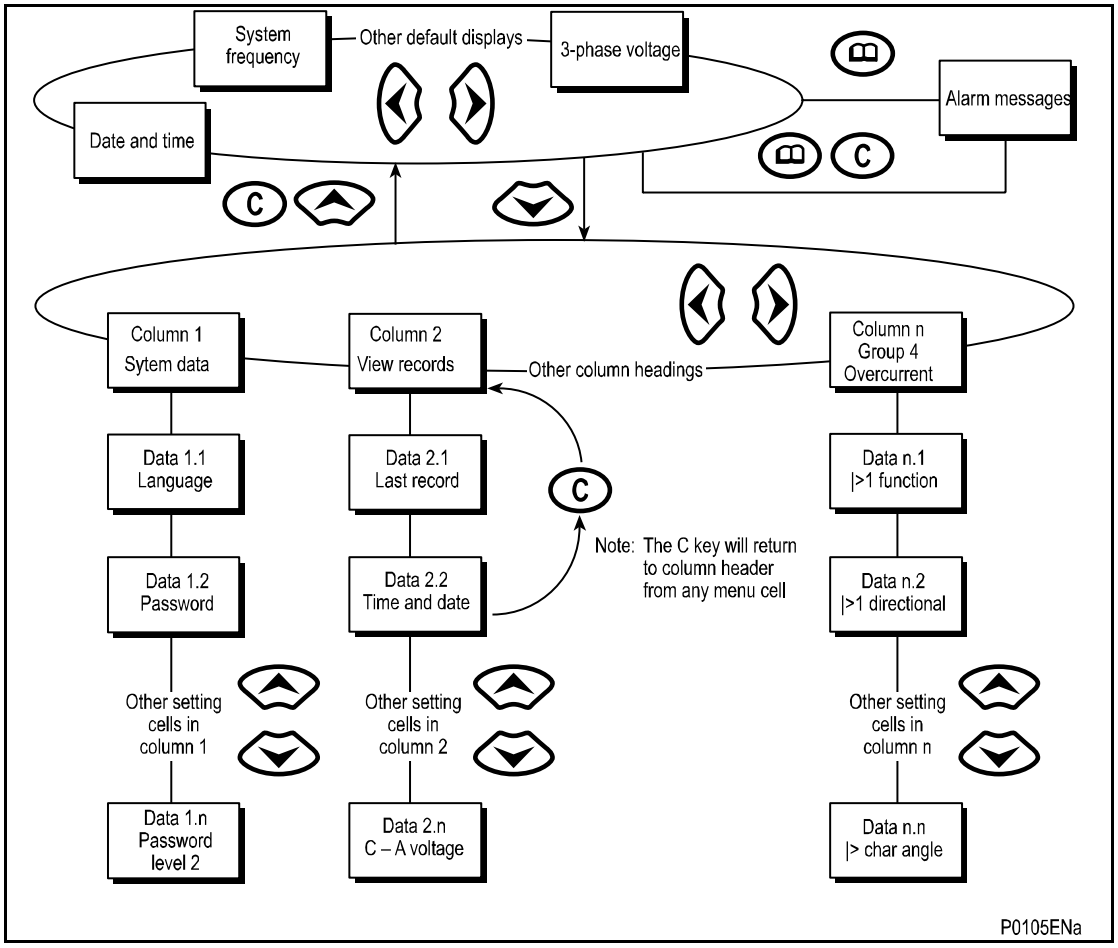
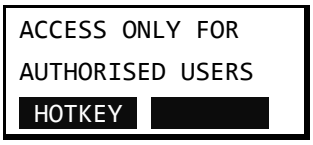


Figure 4: Front panel user interface

1.8.1 Default display and menu time-out

The front panel menu has a selectable default display. The relay will time-out and return to the default display and turn the LCD backlight off after 15 minutes of keypad inactivity. If this happens any setting changes which have not been confirmed will be lost and the original setting values maintained.

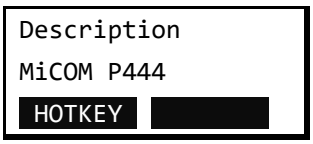
NERC Compliant banner (relays with cyber security features)



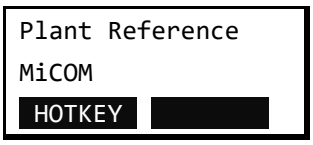
Date and time
For example:



Relay description (user defined)
For example:



Plant reference (user defined)
For example:



Access Level
For example:



The contents of the default display can be selected from the following options: 3-phase and neutral current, 3-phase voltage, power, system frequency, date and time, relay description, or a user-defined plant reference*. The default display is selected with the 'Default display' cell of the 'Measure't setup' column. Also, from the default display the different default display options can be scrolled through using the 4 and 6 keys. However, the menu selected default display will be restored following the menu time-out elapsing. Whenever there is an uncleared alarm present in the relay (e.g. fault record, protection alarm, control alarm etc.) the default display will be replaced by:



Entry to the menu structure of the relay is made from the default display and is not affected if the display is showing the 'Alarms/Faults present' message.

1.8.1.1 Cyber Security

Figure 5 depicts the navigation between default displays.

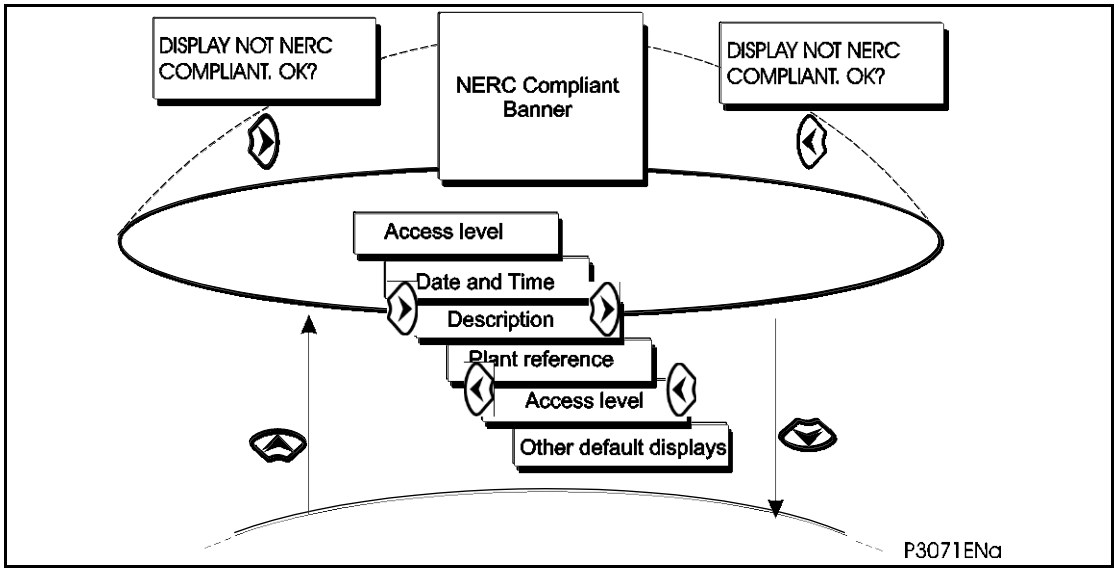


Figure 5: Default display navigation

The right cursor key takes you to the next menu option in a clockwise direction, whereas the left cursor key takes you to the next menu option in an anti-clockwise direction.

If the device is not yet configured for NERC compliance (see cyber Security chapter) a warning will appear when moving from the "NERC compliant" banner. The warning message is as follows:

```
DISPLAY NOT NERC
COMPLIANT. OK?
```

You will have to confirm with the ENTER button before you can go any further.

Note: The unit is delivered with the NERC-compliant default display. Please see the Cyber Security chapter for further details

*Note: Whenever the unit has an uncleared alarm the default display is replaced by the text **Alarms/ Faults present**. You cannot override this default display. However, you can enter the menu structure from the default display, even if the display shows the **Alarms/Faults present** message.*

1.8.2 Menu navigation and setting browsing

The menu can be browsed using the four arrow keys, following the structure shown in Figure 4. Therefore, starting at the default display the 8 key will display the first column heading. To select the required column heading use the 4 and 6 keys. The setting data contained in the column can then be viewed by using the 2 and 8 keys. It is possible to return to the column header either by holding the 8 key down or by a single press of the clear key 0. It is only possible to move across columns at the column heading level. To return to the default display press the 8 key or the clear key 0 from any of the column headings. It is not possible to go straight to the default display from within one of the column cells using the auto-repeat facility of the 8 key, as the auto-repeat will stop at the column heading. To move to the default display, the 8 key must be released and pressed again.

1.8.3 Hotkey menu navigation

The hotkey menu can be browsed using the two keys directly below the LCD. These are known as direct access keys. The direct access keys perform the function that is displayed directly above them on the LCD. Therefore, to access the hotkey menu from the default display the direct access key below the “HOTKEY” text must be pressed. Once in the hotkey menu the 4 and 6 keys can be used to scroll between the available options and the direct access keys can be used to control the function currently displayed. If neither the 4 or 6 keys are pressed with 20 seconds of entering a hotkey sub menu, the relay will revert to the default display. The clear key 0 will also act to return to the default menu from any page of the hotkey menu. The layout of a typical page of the hotkey menu is described below:

- The top line shows the contents of the previous and next cells for easy menu navigation.
- The centre line shows the function.
- The bottom line shows the options assigned to the direct access keys.

The functions available in the hotkey menu are listed below:

1.8.3.1 Setting group selection

The user can either scroll using <<NXT GRP>> through the available setting groups or <<SELECT>> the setting group that is currently displayed.

When the SELECT button is pressed a screen confirming the current setting group is displayed for 2 seconds before the user is prompted with the <<NXT GRP>> or <<SELECT>> options again. The user can exit the sub menu by using the left and right arrow keys.

For more information on setting group selection refer to “Changing setting group” section in the Setting section (P44x/EN ST).

1.8.3.2 Control inputs – user assignable functions

The number of control inputs (user assignable functions – USR ASS) represented in the hotkey menu is user configurable in the “CTRL I/P CONFIG” column. The chosen inputs can be SET/RESET using the hotkey menu.

For more information refer to the “Control Inputs” section in the Setting section (P44x/EN ST).

1.8.3.3 CB control

The CB control functionality varies from one Px40 relay to another. For a detailed description of the CB control via the hotkey menu refer to the “Circuit breaker control” section of the Setting section (P44x/EN ST).

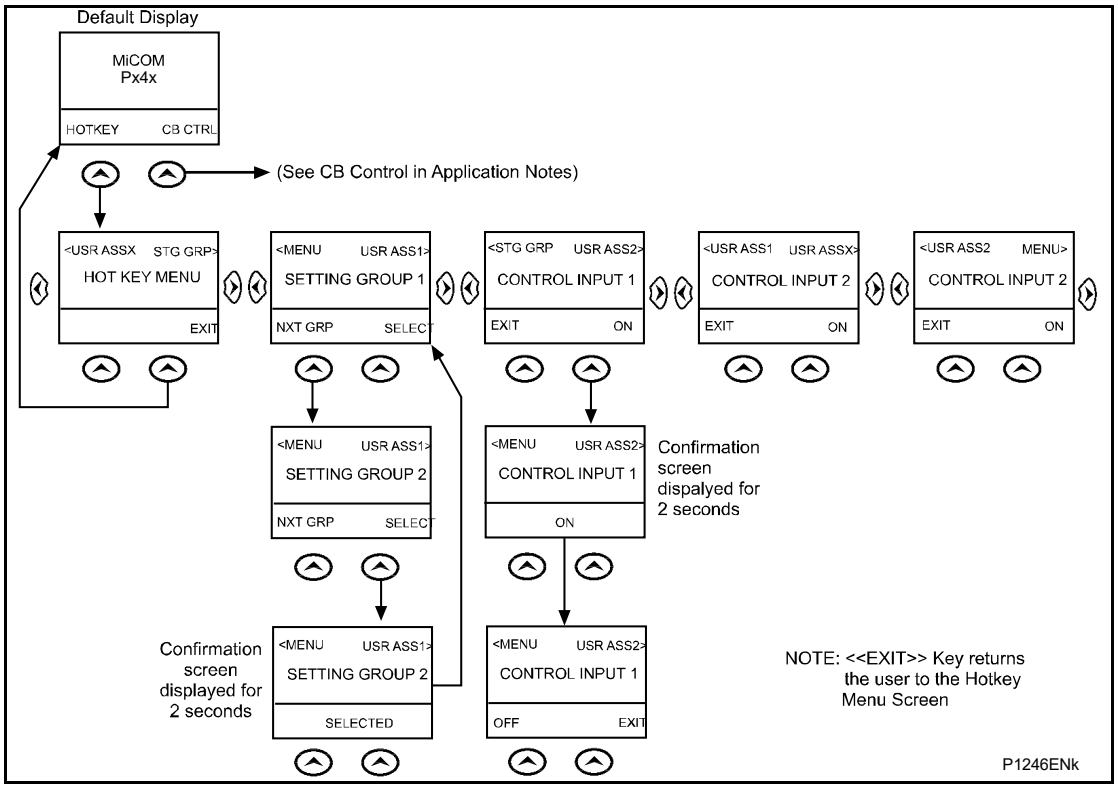


Figure 6: Hotkey menu navigation

1.8.4 Password entry

1.8.4.1 Standard relays

When entry of a password is required the following prompt will appear:

Enter password
****** Level 1**

Note: The password required to edit the setting is the prompt as shown above.

A flashing cursor will indicate which character field of the password may be changed. Press the 8 and 2 keys to vary each character between A and Z. To move between the character fields of the password, use the 4 and 6 keys. The password is confirmed by pressing the enter key 5. The display will revert to 'Enter Password' if an incorrect password is entered. At this point a message will be displayed indicating whether a correct password has been entered and if so what level of access has been unlocked. If this level is sufficient to edit the selected setting then the display will return to the setting page to allow the edit to continue. If the correct level of password has not been entered then the password prompt page will be returned to. To escape from this prompt press the clear key 0. Alternatively, the password can be entered using the 'Password' cell of the 'System data' column.

For the front panel user interface the password protected access will revert to the default access level after a keypad inactivity time-out of 15 minutes. It is possible to manually reset the password protection to the default level by moving to the 'Password' menu cell in the 'System data' column and pressing the clear key 0 instead of entering a password.

1.8.4.2 Relays with Cyber Security

Configuring the default display (in addition to modification of other settings) requires level 3 access. You will be prompted for a password before you can make any changes, as follows. The default level 3 password is AAAA.



1. A flashing cursor shows which character field of the password can be changed. Press the up or down cursor keys to change each character (tip: pressing the up arrow once will return an upper case "A" as required by the default level 3 password).
2. Use the left and right cursor keys to move between the character fields of the password.
3. Press the **Enter** key to confirm the password. If you enter an incorrect password, an invalid password message is displayed then the display reverts to **Enter password**. Upon entering a valid password a message appears indicating that the password is correct and if so what level of access has been unlocked. If this level is sufficient to edit the selected setting, the display returns to the setting page to allow the edit to continue. If the correct level of password has not been entered, the password prompt page appears again.
4. To escape from this prompt press the Clear key. Alternatively, enter the password using System data > Password. If the keypad is inactive for 15 minutes, the password protection of the front panel user interface reverts to the default access level.
5. To manually reset the password protection to the default level, select **System data > Password**, then press the clear key instead of entering a password.

1.8.5 Reading and clearing of alarm messages and fault records

The presence of one or more alarm messages will be indicated by the default display and by the yellow alarm LED flashing. The alarm messages can either be self-resetting or latched, in which case they must be cleared manually. To view the alarm messages press the read key 1. When all alarms have been viewed, but not cleared, the alarm LED will change from flashing to constant illumination and the latest fault record will be displayed (if there is one). To scroll through the pages of this use the 1 key. When all pages of the fault record have been viewed, the following prompt will appear:

Press clear to
reset alarms

To clear all alarm messages press 0; to return to the alarms/faults present display and leave the alarms uncleared, press 1. Depending on the password configuration settings, it may be necessary to enter a password before the alarm messages can be cleared (see section on password entry). When the alarms have been cleared the yellow alarm LED will extinguish, as will the red trip LED if it was illuminated following a trip.

Alternatively it is possible to accelerate the procedure, once the alarm viewer has been entered using the 1 key, the 0 key can be pressed and this will move the display straight to the fault record. Pressing 0 again will move straight to the alarm reset prompt where pressing 0 once more will clear all alarms.

1.8.6 Setting changes

To change the value of a setting, first navigate the menu to display the relevant cell. To change the cell value press the enter key 5 which will bring up a flashing cursor on the LCD to indicate that the value can be changed. This will only happen if the appropriate password has been entered, otherwise the prompt to enter a password will appear. The setting value can then be changed by pressing the 4 or 6 keys. If the setting to be changed is a binary value or a text string, the required bit or character to be changed must first be selected using the 4 and 6 keys. When the desired new value has been reached it is confirmed as the new setting value by pressing 5. Alternatively, the new value will be discarded either if the clear button 0 is pressed or if the menu time-out occurs.

For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used by the relay. To do this, when all required changes have been entered, return to the column heading level and press the key. Prior to returning to the default display the following prompt will be given:

Update settings?
Enter or clear

Pressing 5 will result in the new settings being adopted, pressing 0 will cause the relay to discard the newly entered values. It should be noted that, the setting values will also be discarded if the menu time out occurs before the setting changes have been confirmed. Control and support settings will be updated immediately after they are entered, without 'Update settings?' prompt.

1.9 Front communication port user interface

The front communication port is provided by a 9-pin female D-type connector located under the bottom hinged cover. It provides EIA(RS)232 serial data communication and is intended for use with a PC locally to the relay (up to 15m distance) as shown in Figure 7. This port supports the Courier communication protocol only. Courier is the communication language developed by Alstom Grid to allow communication with its range of protection relays. The front port is particularly designed for use with the relay settings program MiCOM S1 a Windows 95/NT based software package.

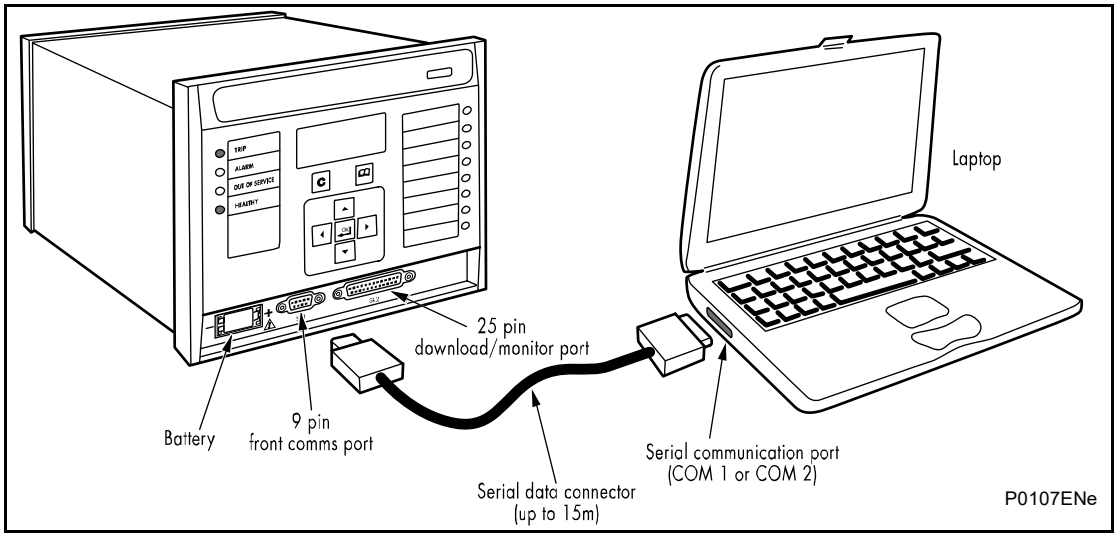


Figure 7: Front port connection

The relay is a Data Communication Equipment (DCE) device. Therefore the pin connections of the relay's 9-pin front port are as follows:

Pin no. 2	Tx Transmit data
Pin no. 3	Rx Receive data
Pin no. 5	0V Zero volts common

None of the other pins are connected in the relay. The relay should be connected to the serial port of a PC, usually called COM1 or COM2. PCs are normally Data Terminal Equipment (DTE) devices that have a serial port pin connection as below (if in doubt check your PC manual):

	25 Way	9 Way	
Pin no.	3	2	Rx Receive data
Pin no.	2	3	Tx Transmit data
Pin no.	7	5	0V Zero volts common

For successful data communication, the Tx pin on the relay must be connected to the Rx pin on the PC, and the Rx pin on the relay must be connected to the Tx pin on the PC, as shown in Figure 8. Therefore, providing that the PC is a DTE with pin connections as given above, a 'straight through' serial connector is required, i.e. one that connects pin 2 to pin 2, pin 3 to pin 3, and pin 5 to pin 5. Note that a common cause of difficulty with serial data

communication is connecting Tx to Tx and Rx to Rx. This could happen if a 'cross-over' serial connector is used, i.e. one that connects pin 2 to pin 3, and pin 3 to pin 2, or if the PC has the same pin configuration as the relay.

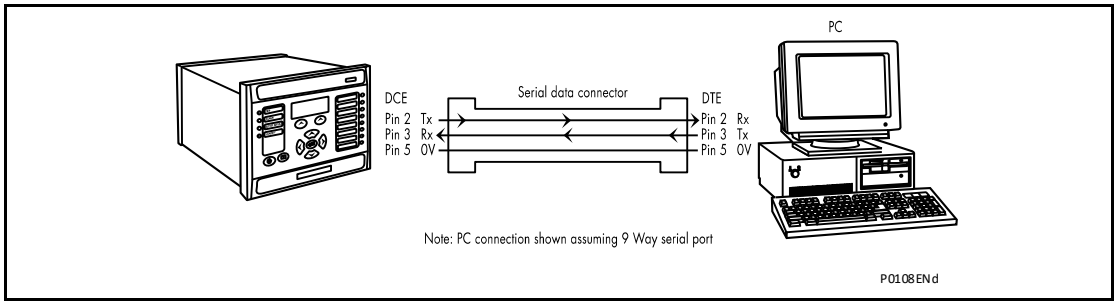


Figure 8: PC – relay signal connection

Having made the physical connection from the relay to the PC, the PC's communication settings must be configured to match those of the relay. The relay's communication settings for the front port are fixed as shown in the table below:

Protocol	Courier
Baud rate	19,200 bits/s
Courier address	1
Message format	11 bit - 1 start bit, 8 data bits, 1 parity bit (even parity), 1 stop bit

The inactivity timer for the front port is set at 15 minutes. This controls how long the relay will maintain its level of password access on the front port. If no messages are received on the front port for 15 minutes then any password access level that has been enabled will be revoked.

1.10 Introduction to the Settings Application Software

The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for managing all aspects of the IEDs. This chapter provides a brief summary of each software tool. Further information is available in the Help system and in the Settings Application Software Guide P40-M&CR-UG-EN-n, where n is the latest version of the settings application software.

The software allows you to edit device settings and commands for GE Vernova's range of IEDs. It is compatible with Windows XP, Windows Vista and Windows 7 operating systems.

It also enables you to manage the MiCOM devices in your system. You can build a list of devices and organize them in the same way as they physically exist in a system. Parameters can be created and uploaded for each device, and devices can be supervised directly.

It also includes a Product Selector tool. This is an interactive product catalogue, which makes it easier to choose the right device for each application.

1.10.1 Getting Started

S1 Agile allows you to create a model of a protection system which simulates a real-world protection system. You can add substations, bays, voltage levels and devices to the system. First you need to download the data models for the devices in the system. Then you can either create a new system or open an existing system. You can connect to an IED either directly through the front port or to an IED in the system model. You can then send or extract settings. You can also extract PSL, DNP3, Events or Disturbance Record files.

If there is no default system, use **Quick Connect** to automatically create one. If a system is no longer needed, right-click it and select Delete to permanently delete it. Systems are not opened automatically. To change this, select **Options** then **Preferences** then check the checkbox **Reopen last System at start-up**.

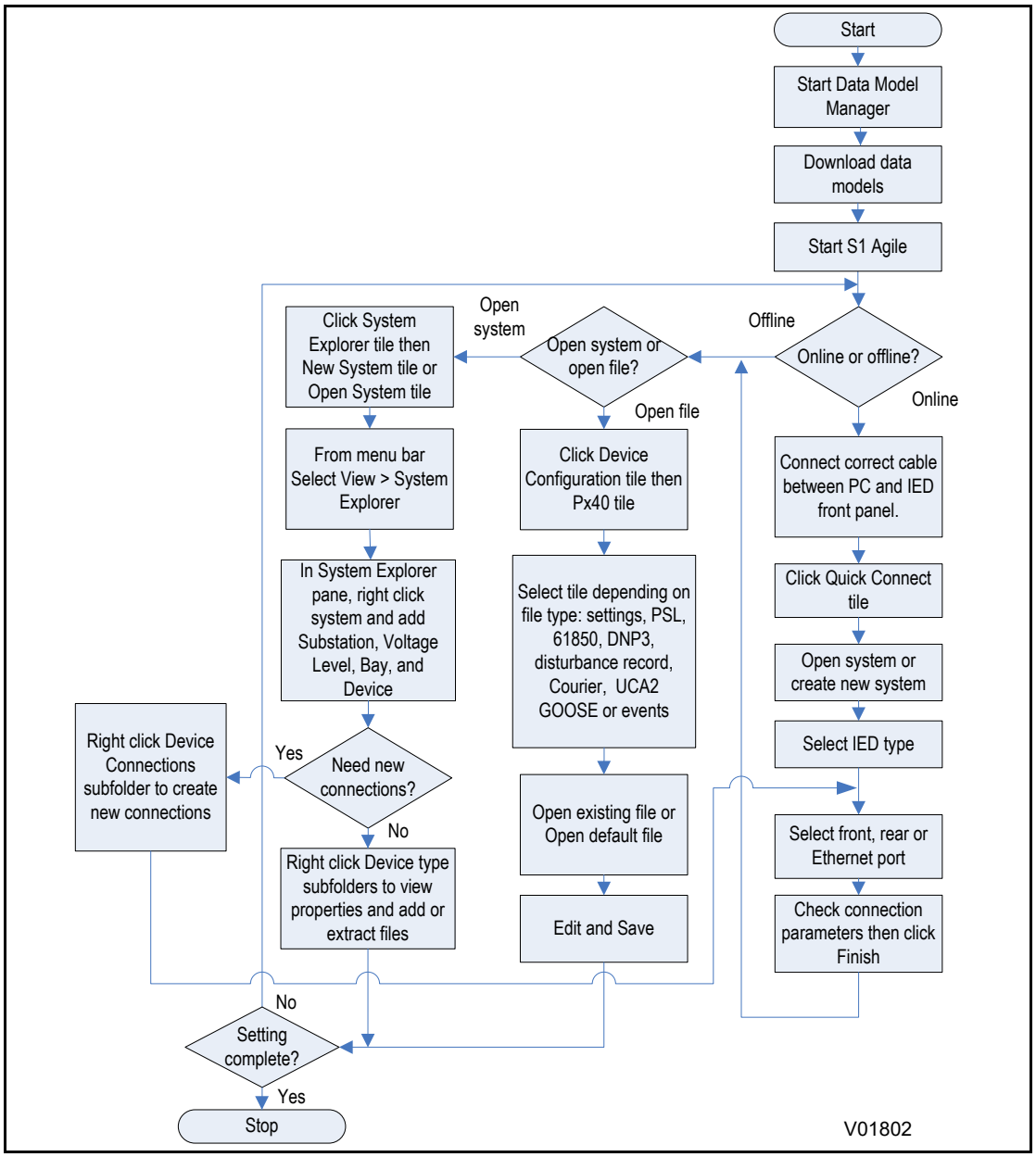


Figure 9: Flowchart showing how S1 Agile can be used to set up and save a protection system offline or online.

1.10.1.1 Quick System Guide

S1 Agile allows you to create a model of a protection system which simulates a real-world protection system. You can add substations, bays, voltage levels and devices to the system. First you need to download the data models for the devices in the system. Then you can either create a new system or open an existing system.

You can connect to an IED either directly through the front port or to an IED in the system model. You canthen send or extract settings. You can also extract a PSL, DNP3, Events or Disturbance Record file.

If there is no default system, use **Quick Connect** to automatically create one. If a system is no longer needed, right-click it and select **Delete** to permanently delete it.

Systems are not opened automatically. To change this, select **Options** then **Preferences** then check the checkbox **Reopen last System at start-up**.

1.10.1.2 Download Data Models

1. Close S1 Agile and run the Data Model Manager.

2. Follow the on-screen instructions.

1.10.1.3 Set up a System

1. Click the System **Explorer** tile then the **New System** tile or **Open System** tile.
2. From the menu bar select **View** then **System Explorer**.
3. In the System Explorer pane, right click System and select **New Substation, New Voltage Level, New Bay**, and **New Device.**
4. Right-click the **Device** subfolders to view properties and add or extract files.

1.10.1.4 Connect to an IED Front Port

1. Connect the cable between the PC and IED.
2. From the main screen, click **Quick Connect**.
3. Select the product range.
4. Select connection to the **Front Port**.
5. Set the connection parameters and click **Finish**.

1.10.1.5 Connect to an IED in a System

1. Make sure that the correct serial rear port or Ethernet cables are in place.
2. From the main screen, click **Quick Connect**.
3. Select the product range.
4. Select connection to the **Rear Port** or **Ethernet Port**.
5. Set the connection parameters and click **Finish**.

1.10.1.6 Send settings to a device

To send settings to a device there must be at least one setting file in a settings folder for a device.

1. Right-click the device name in System Explorer and select **Send**.
2. In the **Send To** dialog select the setting files and click **Send**.
3. Click **Close** to close the **Send To** dialog.

1.10.1.7 Extract settings from a device

1. Using System Explorer, find the device.
2. Right-click the device's Settings folder and select **Extract Settings** or **Extract Full Settings.**
3. Once the settings file is retrieved, click **Close**.

1.10.1.8 Extract a psl file from a device

1. Using System Explorer, find the Px4x device.
2. Right-click the device's **PSL** folder and select **Extrac**t.
3. Once the file is retrieved, click **Close**.

Note:	*If you extract a PSL file from a device that does not store the position information of the PSL scheme elements, the layout of the scheme may not be the same as originally drawn. Also the Original and Logic Only CRC values may not match the original scheme. However, the scheme will be logically correct.*

1.10.1.9 Extract a dnp3 file from a device

1. Using System Explorer, find the device.
2. Right-click the device's **DNP3** folder and select **Extract**.

3. Once the file is retrieved, click **Close**.

1.10.1.10 Extract an event file from a device

1. Using System Explorer, find the device.
2. Right-click the device's Events folder and select Extract Events.
3. Once the file is retrieved, click Close.

1.10.1.11 Extract a disturbance record from a device

1. Using System Explorer, find the device.
2. Right-click the device's **Disturbance Records** folder and select **Extract Disturbances**.
3. Select a disturbance record to extract.
4. Choose a COMTRADE format, 1991 or 2001.
5. Click **Extract** or **Save**. Save leaves the record in the device, Extract deletes it.
6. Once the disturbance records file is retrieved, click Close.

1.10.2 PSL editor

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised internal logic. This is done by combining the IED's digital inputs with internally generated digital signals using logic gates and timers, then mapping the resultant signals to the IED's digital outputs and LEDs.

The Programmable Scheme Logic (PSL) Editor allows you to create and edit scheme logic diagrams to suit your own particular application.

1.10.3 IEC 61850 Configurator

IEC 61850 is a substation communications standard. It standardizes the way data is transferred to and from IEC 61850 compliant IEDs, making the communication independent of the manufacturer. This makes it easier to connect different manufacturers' products together and simplifies wiring and network changes.

The IEC 61850 Configurator tool is used to configure the IEC 61850 settings of MiCOM IEDs, not the protection settings. It also allows you to extract a configuration file so you can view, check and modify the IEC 61850 settings during precommissioning.

1.10.4 DNP3 configurator

DNP3 (Distributed Network Protocol) is a master/slave protocol developed for reliable communications

between various types of data acquisition and control equipment. It allows interoperability between various SCADA components in substations. It was designed to function with adverse electrical conditions such as electromagnetic distortion, aging components and poor transmission media.

The DNP3 Configurator allows you to retrieve and edit its settings and send the modified file back to a MiCOM IED.

1.10.5 S&R courier

Settings and Records - Courier enables you to connect to any Courier device, retrieve and edit its settings and send the modified settings back to a Courier device, including DNP 3.0 configuration if supported by the device.

Although each device has different settings, each cell is presented in a uniform style, showing the permissible range and step size allowed.

Settings and Records - Courier also enables you to:

- extract events from a device

- extract disturbance records from a device
- control breakers and isolators
- set the date and time on a device
- set the active group on a device
- change the address of a device
- save settings, DNP 3.0 configuration, events and disturbance files to disk

1.10.6 AEDR2

AutoExtract Disturbance Records 2 (AEDR2) automatically reads COMTRADE disturbance records from the rear communication ports of both K-Series and MiCOM Px40 devices with the Courier protocol, and from Px40 devices with the IEC 60870-5-103 protocol.

AEDR2 is configured with an initialisation file. This file contains all settings, file names and file directories needed for configuration. This file can be created and edited using a standard text editor. Log files are also defined in the initialisation file which are used by AEDR2 to record a history of events and errors.

Once configured, disturbance records are automatically extracted according to a schedule from devices connected in a defined range of addresses. This is done using the Windows® Scheduled Task facility which can be used to execute one or several schedules. All new disturbance records are saved to a user-defined drive and filename.

AEDR2 also has a test function to ensure the initialisation file has been properly configured. The command line is used to execute the test function and validate the initialisation file. The command line can also be used to manually execute the AEDR2 application on demand.

WinAEDR2 is a management facility for AEDR2. It shows the history of all previous extractions and has shortcut buttons to launch WaveWin, Windows Explorer and the Scheduled Task facility. It can also be used to view log files, and edit and test the initialisation file.

1.10.7 WinAEDR2

WinAEDR2 is a management facility for AEDR2. It shows the history of all previous extractions and has shortcut buttons to launch WaveWin, Windows Explorer and the Scheduled Task facility. It can also be used to view log files, and edit and test the initialisation file.

1.10.8 Wavewin

Wavewin is used for viewing and analysing waveforms from disturbance records. It can be used to determine the sequence of events that led to a fault.

Wavewin provides the following functions:

- File management
- Query management
- Log management
- Report generation
- Sequence of Events(SOE)
- Conversion of COMTRADE files
- Waveform summary

1.10.9 Device (Menu) Text Editor

The Menu Text Editor enables you to modify and replace the menu texts held in MiCOM Px4x IEDs. For example, you may want to customise an IED so that menus appear in a language other than one of the standard languages.

By loading a copy of the current menu text file in one of the standard languages into the reference column, you can type the appropriate translation of each menu entry into the target column.

This can then be sent from the PC to the IED, replacing one of the current standard languages. New menu text files created this way can also be saved to disk for later use or further editing.

1.10.10 Event viewer

IEDs record all events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused.

When available space is exhausted, the oldest event is overwritten by the new one. The IED's internal clock provides a time tag for each event.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

SETTING

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1 SETTINGS

The MiCOM P44x protection must be configured to the system and application by means of appropriate settings. The sequence of the settings is listed and described in this section. They are protection setting, control and configuration settings and the disturbance recorder settings. The relay is supplied with a factory-set configuration of default settings.

1.1 Relay setting configuration ("System Data" column)

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
SYSTEM DATA				
Language	English			
The default language used by the device. Selectable as English, French, German, Spanish, Italian or Chinese (see options in section P44x/EN IT)				
Password	"****" or "_____"			
Device default password (8 characters for models with Cyber Security features)				
Description	"MiCOM"			
16 character relay description. Can be edited.				
Plant Reference	MiCOM			
Associated plant description and can be edited.				
Model Number	P44?????????????			
Relay model number. This display cannot be altered.				
Serial Number	6 digits + 1 letter			
Relay model number. This display cannot be altered.				
Frequency	50Hz	50Hz	60Hz	10Hz
Relay set frequency. Settable between 50 and 60Hz.				
Comms. Level	2			
Displays the conformance of the relay to the Courier Level 2 comms.				
Relay Address	255	7	34	1
Sets the front and first rear port relay address from 7.				
Plant Status	0000000000000000			
The two last digits display the circuit breaker status: "00" = CB not fitted, "01" = CB ompen and healthy, "10" = CB closed and "11" = CB failure or state unknown. Refer to section P44x/EN AP for Circuit breaker state monitoring features.				
Control Status	0000000000000000			
Not used.				
Active Group	1			
Displays the active settings group.				
CB Trip/Close	No Operation	No Operation/ Trip/ Close		
Supports trip and close commands if enabled in the Circuit Breaker Control menu.				
Software Ref. 1				
Displays the relay software version including protocol and relay model.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
SYSTEM DATA				
Software Ref. 2				
Software Ref. 2 is displayed for a relay with IEC 61850 protocol only and displays the software version of the Ethernet card.				
Opto I/P Status	00000000000000000000000			
Duplicate. Displays the status of opto-isolated inputs.				
Relay Status 1	00000000000000000000000000000000			
Duplicate. Displays the status of first 32 output relays.				
Alarm Status 1	00000000000000000000000000000000			
32 bits field give status of first 32 alarms.				
Relay Status 1	00000000000000000000000000000000			
Duplicate. Displays the status of the next output relays.				
Alarm Status 1	00000000000000000000000000000000			
32 bits field give status of the next alarms.				
Alarm Status 2	00000000000000000000000000000000			
Next 32 alarm status defined.				
Alarm Status 3	00000000000000000000000000000000			
Next 32 alarm status defined. Assigned specifically for platform alarms.				
Access Level	2			
Displays the current access level (see section P44x/EN GS for level description and access): – Standard models: Level 0 (No password required) = Read access to all settings, alarms, event records and fault records Level 1(Password 1 or 2 required) = As level 0 plus: Control commands, e.g. circuit breaker open/close + Reset of fault and alarm conditions + Reset LEDs, Clearing of event and fault records Level 2 (Password 2 required) = as level 1 plus all other settings – Models with Cyber Security features: Level 0 = read access to some cells (system data and security config columns). Write access to password entry and LCD contrast Level 1 = level 0 + read access to all data and settings, poll measurements. Write access to some cells (level 1 pasword setting, select event, main and fault, extract events Level 2 = level 1 + write access to setting cells that change visibility, setting values selector, reset indication, demand, statistics and CB data counters and level 2 password setting, Level 3 = All other settings.				
Password Control	2	0	2	1
Sets the menu access level for the relay. This setting can only be changed when level 2 access is enabled.				
Password Level 1	****			
Allows user to change password level 1. Password in relays with Cyber Security deatures may be any length between 0 and 8 characters long (see section P44x/EN CS for password strengthening and validation and blank password management).				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
SYSTEM DATA				
Password Level 2	****			
Allows user to change password level 2. Password in relays with Cyber Security features may be any length between 0 and 8 characters long (see section P44x/EN CS for password strengthening and validation and blank password management).				
Password Level 3	****			
Relays with Cyber Security features only. Allows user to change password level 3 (password may be any length between 0 and 8 characters long). See section P44x/EN CS for password strengthening and validation and blank password management.				

1.2 Configuration column (“Configuration” menu)

The relay is a multi-function device that supports numerous different protection, control and communication features. To simplify the setting of the relay, there is a configuration settings column which can be used to enable or disable many of the functions of the relay. The settings associated with any function that is disabled are made invisible; i.e. they are not shown in the menu. To disable a function change the relevant cell in the **Configuration** column from **Enabled** to **Disabled**.

The configuration column controls which of the four protection settings groups are selected as active through the ‘Active settings’ cell. A protection setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

The column also allows all of the setting values in one group of protection settings to be copied to another group.

Set the **Copy from** cell to the protection setting group to be copied, then set the **Copy to** cell to the protection group where the copy is to be placed. The copied settings are placed in the temporary scratchpad and are only used following confirmation.

Menu text	Default setting	Available settings
CONFIGURATION		
Restore Defaults	No Operation	No Operation All Settings Setting Group 1 Setting Group 2 Setting Group 3 Setting Group 4
Setting to restore a setting group to factory default settings.		
Setting Group	Select via Menu	Select via Menu Select via Optos
Allows setting group changes to be initiated via opto-isolated Input or via Menu. When **Select via Optos** is selected, the two opto-isolated inputs 1 and 2 are used (see section 1.2.1). In this case, The Opto inputs 1 and 2 must not be connected to any output signal (PSL).		
Active Settings	Group 1	Group1 / Group 2 / Group 3 / Group 4
Activate a setting group via the menu when “Select via Menu” is set (‘Setting Group’ cell).		
Save Changes	No Operation	No Operation / Save / Abort
Save all relay settings.		

Menu text	Default setting	Available settings
CONFIGURATION		
Copy From	Group 1	Group1,2,3 or 4
Allows displayed settings to be copied from a selected setting group.		
Copy To	No Operation	No Operation / Group1, 2, 3 or 4
Allows displayed settings to be copied to a selected setting group (ready to paste).		
Setting Group 1	Enabled	Enabled or Disabled
If the setting group is disabled from the configuration, then all associated settings and signals are hidden, with the exception of this setting (paste).		
Setting Group 2	Disabled	Enabled or Disabled
Setting Group 3	Disabled	Enabled or Disabled
Setting Group 4	Disabled	Enabled or Disabled
Distance Protection	Enabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Distance Protection.		
Power Swing	Enabled	Enabled or Disabled
To enable (activate) or disable (turn off) the power swing blocking / out of step.		
Back-up I>	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the directional or non-directional overcurrent protection.		
Neg Sequence O/C	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Negative sequence overcurrent protection.		
Broken Conductor	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Broken Conductor detection.		
Earth Fault O/C Prot	Disabled	Enabled or ‘Zero Seq. power’ or ‘Earth Fault O/C’
To enable (activate) or disable (turn off) the earth fault overcurrent protection. Two earth fault overcurrent protections are available: – Directional and non-directional earth fault overcurrent protection (‘Earth Fault O/C’), – Maximum of Residual – Zero Sequence power protection (‘Zero Seq. power’).		
Earth fault prot (ZSP)	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the earth fault protection function (IN>stages)		
Aided DEF	Enabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Aided directional earth fault protection.		
Volt Protection	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the voltage protection (under / overvoltage) function.		
CB Fail & I<	Enabled	Enabled or Disabled
To enable (activate) or disable (turn off) the circuit breaker fail protection function.		
Supervision	Enabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Supervision (VTS, CTS and CVT) functions.		
System Checks	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the check synchronisation (System check) menu.		

Menu text	Default setting	Available settings
CONFIGURATION		
Thermal Overload	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the thermal overload protection function.		
I< Protection	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Undercurrent protection function.		
Residual O/V NVD	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Residual overvoltage protection function.		
Freq protection	Disabled	Enabled or Disabled
To enable (activate) or disable (turn off) the Frequency protection (under / overfrequency) function.		
Internal A/R	Disabled	Enabled or Disabled
Internal Autoreclose: Should autoreclosure not be required, the function may be Disabled. Disabling the autorecloser does not prevent the use of the internal check synchronism element to supervise manual circuit breaker closing. If the autoreclose function is Enabled, the setting guidelines (autoreclose section) should be read.		
Input Labels	Visible	Invisible or Visible
To the Input Labels menu visible or invisible in the relay menu settings menu.		
Output Labels	Visible	Invisible or Visible
To the output Labels menu visible or invisible in the relay menu settings menu.		
CT & VT Ratios	Visible	Invisible or Visible
Sets the Current and Voltage Transformer ratios menu visible.		
Record Control	Invisible	Invisible or Visible
Sets the record control menu visible or invisible.		
Disturb Recorder	Invisible	Invisible or Visible
Sets the disturbance recorder menu visible or invisible.		
Measure't Setup	Invisible	Invisible or Visible
Sets the measurement setup menu visible or invisible.		
Comms Settings	Visible	Invisible or Visible
Sets the communications settings menu visible or invisible.		
Commission Tests	Visible	Invisible or Visible
Sets the commission tests menu visible or invisible.		
Setting Values	Primary	Primary or Secondary
This affects all protection settings that are dependent on CT and VT ratios. All subsequent settings input must be based in terms of this reference.		
Control Inputs	Visible	Invisible or Visible
Activates the Control Input status and operation menu further on in the relay setting menu.		
Ctrl I/P Config	Visible	Invisible or Visible
Sets the Control Input Configuration menu visible further on in the relay setting menu.		
Ctrl I/P Labels	Visible	Invisible or Visible
Sets the Control Input labels menu visible further on in the relay setting menu.		

Menu text	Default setting	Available settings
CONFIGURATION		
Direct Access	Enabled	Enabled or Disabled
Defines what CB control direct access is allowed. Enabled implies control via menu, hotkeys etc.		
Inter MiCOM	Enabled	Enabled or Disabled
To enable (activate) or disable (turn off) EIA (RS) 232 InterMiCOM (integrated teleprotection).		
Ethernet NCIT	Visible	Visible / Invisible
Sets the Ethernet Non-Conventional Instrument Transformer menu visible or invisible further on in the relay setting menu.		
Function key	Visible	Visible / Invisible
Sets the Function key menu visible or invisible further on in the relay setting menu		
PSL Timers	Visible	Visible / Invisible
Sets the the PSL Timers menu visible or invisible further on in the relay setting menu.		
RearPort1ReadOnly	Disabled	Enabled or Disabled
If this Read Only mode is enabled, then all setting changes and most command/control actions are blocked (not accepted by the relay) for Rear Port 1.		
RearPort2ReadOnly	Disabled	Enabled or Disabled
If this Read Only mode is enabled, then all setting changes and most command/control actions are blocked (not accepted by the relay) for Rear Port 2 (when option available).		
RearNICReadOnly	Disabled	Enabled or Disabled
If this Read Only mode is enabled, then all setting changes and most command/control actions are blocked (not accepted by the relay) for the Ethernet port (when option available).		
LCD Control	11	1 – 31
Sets the LCD contrast.		

1.2.1 Alternative setting groups

The P442 and P444 relays can store up to four independent groups of settings. The active group is selected either locally using the menu or remotely using the serial communications. The ability to quickly reconfigure the relay to a new setting group may be desirable if changes to the system configuration demand new protection settings. Typical examples where this feature can be used include:

Single-bus installations with a transfer bus;

Double bus installations, with or without a separate transfer bus, where the transfer circuit breaker or bus coupler might be used to take up the duties of any feeder circuit breaker when both the feeder circuit breaker and the current transformers are by-passed.

For a double bus installation, it is usual for bus 1 to be referred to as the main bus and bus 2 as the reserve bus, and for any bypass circuit isolator to be connected to bus 2 as shown in Figure 1. This arrangement avoids the need for a current polarity reversing switch that would be required if both buses were to be used for by-pass purposes. The standby relay, associated with the transfer circuit breaker or the bus coupler, can be programmed with the individual setting required for each of the outgoing feeders. For bypass operation the

appropriate setting group can be selected as required. This facility is extremely useful in the case of unattended substations where all of the switching can be controlled remotely.

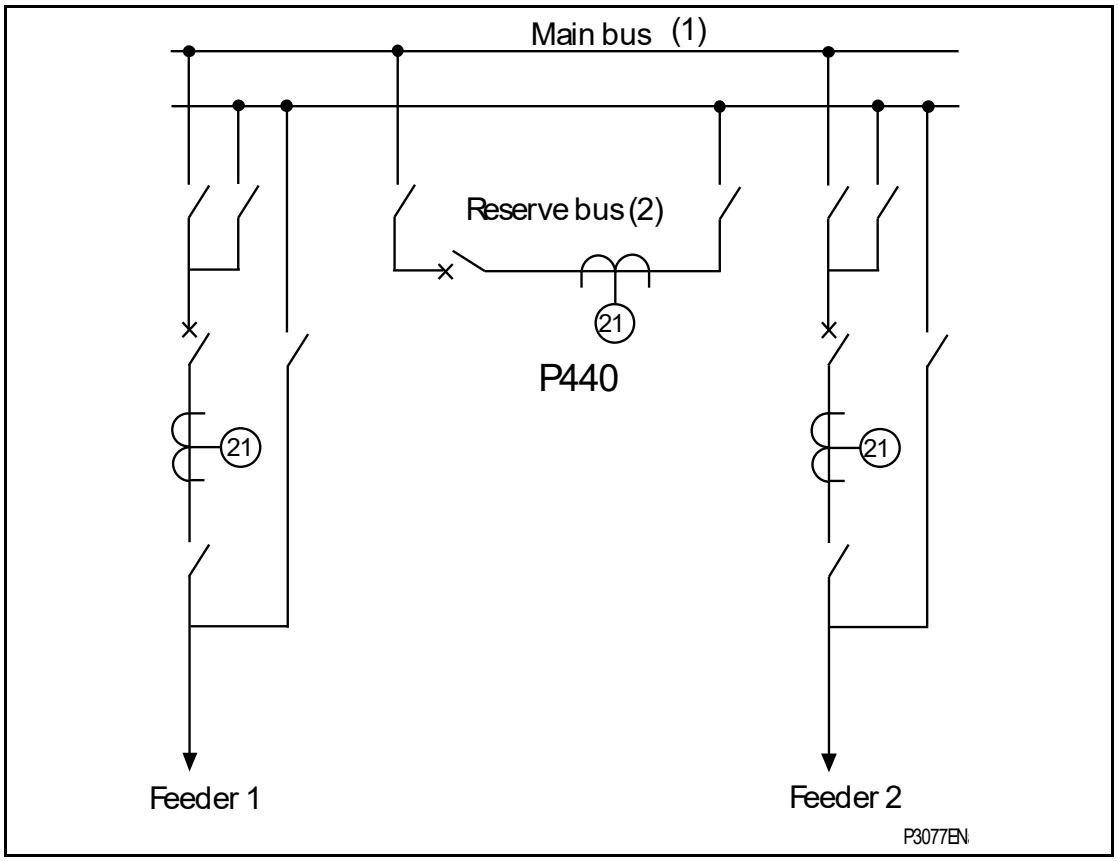


Figure 1 - Typical Double Bus Installation with Bypass Facilities

A further use for this feature is the ability to provide alternative settings for teed feeders or double circuit lines with mutual coupling. Similar alternative settings could be required to cover different operating criteria in the event of the channel failing, or an alternative system configuration (ie. lines being switched in or out).

1.2.2 Selection of Setting Groups

Setting groups can be changed by one of two methods:

Automatic group selection by state changes of two opto-isolated inputs, assigned to Setting Group Change bit 0 (opto 1), and Setting Group Change bit 1 (opto 2), as shown in Table 1 below. The new setting group binary code must be maintained for 2 seconds before a group change is implemented, therefore rejecting spurious induced interference. (See also hysteresis value for logic level 0 & logic level 1 in section 4.1 of this document).
When this selection is made, the two opto-isolated inputs assigned to **this function are opto inputs 1 and 2 and they must not be connected to any output signal in the PSL**.
Special care should be taken to avoid using them for another purpose (i.e please note that in the default PSL they have been used for another functions: DIST/DEF Chan. Recv. for opto 1 and DIST/DEF carrier out of service for opto 2).

Default PSL: To enable the setting group via logic inputs, the opto inputs 1 and 2 must be dedicated only to the group selection (remove Opto-Label 01 and Opto-Label 02 from the PSL). (If assigned in the PSL, instead of Dist DEF Carrier Receive Logic Start, a setting group change occurs)

Note that each setting group has its own dedicated PSL, which should be configured and sent to the relay independently.

Or using the relay operator interface / remote communications. Should the user issue a menu command to change group, the relay transfers to that settings group, and then ignores future changes in state of the bit 0 and bit 1 opto inputs. Therefore, the user is given greater priority than automatic setting group selection.

Binary State of SG Change bit 1 Opto 2	Binary State of SG Change bit 0 Opto 1	Setting Group Activated
0	0	1
0	1	2
1	0	3
1	1	4

Table 1 - Setting Group Selection

REMINDER: IF SELECTED IN THE MENU (CHANGE BY OPTOS), OPTO 1 & 2 MUST BE REMOVED FROM THE PSL (THEY ARE DEDICATED TO GROUP SELECTION)

2 PROTECTION FUNCTIONS

2.1 Distance zone settings ("Distance" menu)

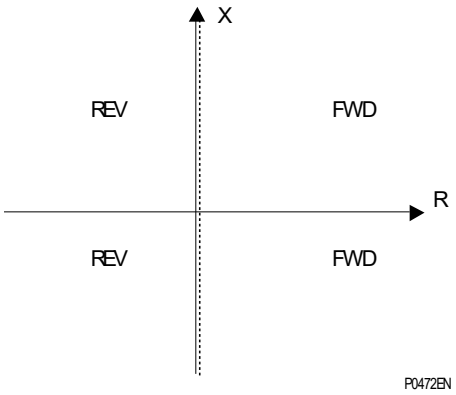
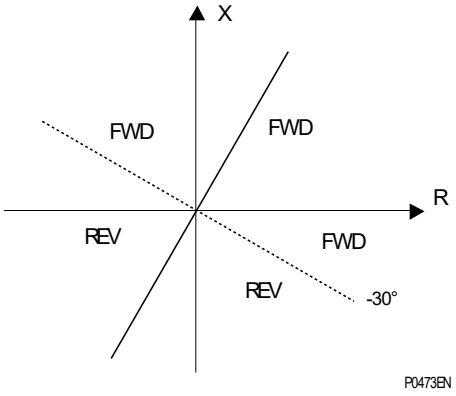
The "Distance elements" menu setting is used to set the line protection (line and zone setting). The Zone setting menu allows 6 zones setting.

Refer to P44x/EN AP chapter for complete explanation of the following menu.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – DISTANCE ELEMENTS				
LINE SETTING				
Line Length	1000 km (625 miles)	0.3 km (0.2 mile)	1000 km (625 miles)	0.010 km (0.005 mile)
Setting of the protected line/cable length in km or in miles. This setting is available if MEASURE'T SETUP column is selected as **Visible** in the CONFIGURATION column. The unit (km or miles) depends on the 'Distance unit' setting in the MEASURE'T SETUP column.				
Line Impedance	12/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω
Setting for protected line/cable positive sequence impedance in either primary or secondary terms, depending on the "Setting Values" reference chosen in the CONFIGURATION column. The set value is used for Fault locator, and for all distance zone reaches calculation if 'Simple' setting mode under "GROUP x LINE PARAMETERS" is selected. This line parameter can be set in polar or rectangular form (see section P44x/EN AP for a complete description).				
Line Angle	70°	–90°	+90°	0.1°
Setting of the line angle (line positive sequence impedance angle). This setting can be set in polar or rectangular form (see section P44x/EN AP).				
ZONE SETTING				
Zone Status	110110	Bit 0 (last digit): Z1X Enable, Bit 1: Z2 Enable, Bit 2: Zone P Enable, Bit 3: Zone Q Enable, Bit 4: Z3 Enable, Bit 5 (first digit): Z4 Enable.		
Zone Status: Distance protection zones can be enabled or disabled individually. Setting the relevant bit to 1 enables the zone. Zone 1 should be always enabled. The other zones should be enabled when required (for use in channel aided schemes). If Z3 is disabled, the forward limit element becomes the smaller zone (Zp if selected forward) If Z3 & Zp Fwd are disabled, the forward limit element becomes Z2 If Z3 & Zp Fwd & Z2 are disabled, the forward limit element becomes Z1 If Z4 is disabled, the directional limit for the fordward zone is 30°. Z4 is always reverse. The following settings are displayed when the relevant zone is enabled. See P44x/EN AP for complete description and calculation for these elements.				
KZ1 Res Comp	1	0	7	0.001
KZ1 Angle	0°	0°	360°	0.1°
Zone 1 compensation (KZ1 residual compensation and kZ1 angle, refer to section P44x/EN AP for zone setting).				
Z1	10/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – DISTANCE ELEMENTS				
Z1X	15/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω
R1G	10/In Ω	0	400/In Ω	0.01/In Ω
R1G: Resistive reach (Earth fault element, refer to P44x/EN AP for resistive reach calculation (earth and phase) setting).				
R1Ph	10/In Ω	0	400/In Ω	0.01/In Ω
R1Ph: Resistive reach (phase fault element, refer to P44x/EN AP for resistive reach calculation (earth and phase) settings).				
tZ1	0	0	10s	0.002s
Zone 1 time delay (TZ1): Zone 1 time delay setting (refer to P44x/EN AP for setting).				
KZ2 Res Comp	1	0	7	0.001
KZ2 Angle	0°	0°	360°	0.1°
Zone 2 compensation (KZ2 residual compensation and kZ2 angle) setting.				
Z2	20/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω
R2G	20/In Ω	0	400/In Ω	0.01/In Ω
R2G: resistive reach – Earth fault element setting for zone 2.				
R2Ph	20/In Ω	0	400/In Ω	0.01/In Ω
R2Ph: Resistive reach – phase fault elements setting for zone 2.				
tZ2	0.2s	0	10s	0.01s
Zone 2 time delay (TZ2) setting.				
KZ3/4 Res Comp	1	0	7	0.01
KZ3/4 Angle	0°	0°	360°	0.1°
Zone 3 and 4 compensations (KZ3/4 residual compensation and kZ3/4 angle) setting.				
Z3	30/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω
R3G - R4G	30/In Ω	0	400/In Ω	0.01/In Ω
R3G – R4G: Resistive reach – Earth fault elements setting for zones 3 and 4.				
R3Ph - R4Ph	30/In Ω	0	400/In Ω	0.01/In Ω
R3Ph – R4Ph: resistive reach – Phase fault elements setting for zones 3 and 4.				
tZ3	0.6s	0	10s	0.01s
Zone 3 time delay (TZ3) setting.				
Z4	40/In Ω	0.001/In Ω	500/In Ω	0.01/In Ω
tZ4	1s	0	10s	0.01s
Zone 4 time delay (TZ4) setting.				
Zone P - Direct.	Directional Fwd	Directional Fwd or Directional Rev		
KZp Res Comp	1	0	7	0.001
KZp Angle	0°	0°	360°	0.1°
Zone P compensation (KZp residual compensation and kZp angle).				
Zp	25/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – DISTANCE ELEMENTS				
RpG	25/In Ω	0	400/In Ω	0.01/In Ω
RpG: Resistive reach – Earth fault element for zone P.				
RpPh	25/In Ω	0	400/In Ω	0.01/In Ω
RpPh: Resistive reach – phase fault element for zone p.				
tZp	0.4s	0	10s	0.01s
Zone P time delay (TZp)				
Zone Q – Direct	Directional Fwd	Directional Fwd or Directional Rev		
Zone q is a further distance zone. It can be faster or slower than any other zone (except zone 1), and it can be in either direction. The only constraint is that it must be inside the overall Z3/Z4 start-up zone.				
KZq Res Comp)	1	0	7	0.001
KZq Angle	0°	-180°	180°	0.1°
Zone Q compensation (KZq residual compensation and kZq angle).				
Zq	27*V1/I1	0.001*V1/I1	500*V1/I1	0.001*V1/I1
RqG	27*V1/I1	0	400*V1/I1	0.01*V1/I1
RqG: Resistive reach – Earth fault element for zone Q.				
RqPh	27*V1/I1	0	400*V1/I1	0.01*V1/I1
RqPh: Resistive reach – phase fault element for zone Q.				
tZq	0.5s	0	10s	0.01s
Zone Q time delay (TZq)				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – DISTANCE ELEMENTS				
OTHER PARAMETERS				
Serial Cmp.line	Disable	Enable	Disable	
Serial Compensated Line: If enabled, the Directional Line used in the Delta Algorithms is set at 90° (Fwd = Quad1&4 / Rev = Quad 2&3).  If disabled, the Directional Line of the Delta algorithms is set at -30° like conventional algorithms.  				
Overlap Z Mode	Disable	Enable	Disable	
Overlap Z Mode: If enabled, for a fault in Zp (fwd), then Z1 & Z2 will be displayed in LCD/Events/Drec – The internal logic is not modified.				
Z1m Tilt Angle	0°	-45°	45°	1°
Z1p Tilt Angle	0°	-45°	45°	1°
The settings dealing with the tilt (‘Z1m Tilt Angle’, ‘Z1p Tilt Angle’, ‘Z2p/Zp/Zq Tilt Angle’) and the evolving forward zone detection to zone1 (to avoid a Z1 detection in case of impedance locus getting out from the quad, due to remote CB operating) but crossing the Z1 before being out from the quad (with enough points that a Z1 decision) can be confirmed if that timer has been set to 0ms. Z1m and Z1p Tilt Angle: The tilt angles can be independently set (±45°) for phase-to-ground and phase-to-phase setting.				
Z2/Zp/Zq Tilt Angle	0°	-45°	45°	1°
Tilt characteristic for zone 2, zone P and zone Q (common setting for phase-to-ground and phase-to-phase).				
Fwd Z Chgt Delay	30ms	0	100ms	1ms
This time delay is set to prevent maloperation due to zone evolution from zone $_n$ to zone $_{n-1}$ by CB operation.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – DISTANCE ELEMENTS				
Vmem Validity	10s	0	10s	10mss
The duration of the voltage memory availability after fault detection can be set. When the voltage memory is declared unavailable (e.g. the V Mem Validity set duration has expired, SOTF Mode, no healthy network to record memory voltage), other polarizing quantities can be considered. These include zero, negative and positive sequence (if voltage is sufficient). Otherwise directional decision is forced to forward.				
Earth I Detect	0.05*I1	0*I1	0.1*I1	0.01*I1
The residual current threshold (Earth I Detect.) is used by the conventional algorithm to detect earth faults.				
Fault Locator				
KZm Mutual Comp	0	0	7	0.001
KZm Angle	0°	0°	360°	0.1°
Load Blinder En				
R< Blinder Lim	15/In Ω	0.001/In Ω	500/In Ω	0.001/In Ω
Load/B Angle	45°	15°	65°	1°
Load Blinder V	15 V	1 V	70 V	0.5 V

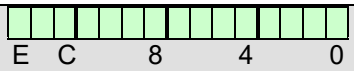
- Remark: The settings dealing with the tilt (‘Z1m Tilt Angle’, ‘Z1p Tilt Angle’, ‘Z2p/Zp/Zq Tilt Angle’) and the evolving forward zone detection to zone1 (to avoid a Z1 detection in case of impedance locus getting out from the quad (due to remote CB operating) but crossing the Z1 before being out from the quad (with enough points that a Z1 decision can be confirmed if that timer has been set to 0 ms).

2.2 Distance protection schemes (“Distance Scheme” menu)

The option of using separate channels for Directional Earth Fault (DEF) aided tripping, and distance protection schemes, is offered in the P442 and P444 relays. Alternatively, the aided DEF protection can share the distance protection signalling channel, and the same scheme logic. In this case, a permissive overreach or blocking distance scheme must be used. The aided tripping schemes can perform single pole tripping. The relays include basic five-zone distance scheme logic for stand-alone operation (where no signalling channel is available) and logic for a number of optional additional schemes. The features of the basic scheme are available even if an additional scheme has been selected or not.

The function is based on a specification with a dedicated application equivalent to a customised weak infeed.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DISTANCE SCHEMES				
Program Mode	Standard Scheme	Standard Scheme Open Scheme		
The 'Program Mode' cell is used to select the standard program mode or open program mode. When Standard program mode is set, a standard basis scheme is selectable. When a scheme is not covered in the Standard modes, the open programming mode can be selected. The user then has the facility to decide which distance relay zone is to be used to program the signalling channel, and what type of aided scheme runs when the channel is received. The signal send zone options, and the aided scheme options on channel receipt are settable.				
Standard Mode	Basic + Z1X	Basic + Z1X, POP Z1, POP Z2, PUP Z2, PUP Fwd, BOP Z1, BOP Z2.		
The following schemes are available when the Standard program mode is selected: – Basic + Zone 1 extended (see section P44x/EN AP), – Permissive Underreach Transfer Trip Schemes PUP Z2 and PUP Fwd, – Permissive Overreach Transfer Trip Schemes POP Z2 and POP Z1; – Blocking Schemes BOP Z2 and BOP Z1. The PUP, POP and BOP schemes are detailed in section P44x/EN AP.				
Fault Type	Both Enabled	Phase to Ground, Phase to Phase, Both Enabled.		
Trip Mode	Force 3 Poles	Force 3 Poles, 1 Pole Z1 & CR, 1 Pole Z1 Z2 & CR.		
Sets the tripping mode: 1-pole trip or 3-pole trip.				
Sig. Send Zone	None	None, CsZ1, CsZ2, CsZ4.		
The 'Signal Send Zone' option is available when an open scheme program mode is set. The user can decide which distance relay zone is used to send the signalling channel: – CsZ1 or CsZ2 ('Carrier send' from Z1 or Z2): when a fault is detected in zone 1, or zone 2, the 'Carrier Send' is emitted from this zone to the relay. These settings are used to configure a permissive scheme. – CsZ4 ('Carrier send' from Z4) when a fault is detected in zone 4 (reverse). This setting can be used to configure a blocking scheme. See section decision logic in the section P44x/EN AP.				
Dist CR	None	None, PermZ1, PermZ2, PermFwd, BlkZ1, BlkZ2.		
The 'Distance Carrier received' option is available when an open scheme program mode is set. Aided scheme options on CR receipt: – Select 'None' to configure a basic scheme, – Select 'PermZ1' or 'PermZ2' to configure a permissive scheme where Zone 1 or Zone 2 can only trip (without waiting tZ1 or tZ2 timeout) if a signal is received, – Select 'BlkZ1' or 'BlkZ2' to configure a blocking scheme where Zone 1 or Zone 2 can only trip if a Distance Carrier is NOT received, – Select 'PermFwd' to configure a permissive scheme where any forward distance zone start causes an aided trip if a Distance Carrier is received.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DISTANCE SCHEMES				
Aid dist. Delay	0.02s	0	1s	0.002s
Available with PUP Z2, PUP FWD, POP Z1 and POP Z2 schemes. This time-delay represents the end of transmission time in blocking scheme: if the remote relay has picked up in zone 2, then it will trip after the “Aid Dist. Delay” on reception of the permissive signal from the other end of the line.				
tReversal Guard	0.02s	0	0.15s	0.002s
Where appropriate, the tReversal Guard and ‘Aid Dist Delay’ (transmission time in blocking scheme) time-delays (in the case of a blocking scheme covering the transmission time) settings will appear in the relay menu. Further customising of distance schemes can be achieved using the Programmable Scheme Logic to condition send and receive logic.				
Unblocking Logic	None	None, Loss of Guard, Loss of Carrier.		
Three modes of unblocking logic are available for use with permissive schemes (blocking schemes are excluded): – None (basic mode), – Loss of Guard mode, – Loss of carrier mode. See section P44x/EN AP for details.				
TOR-SOTF Mode	00000000110000	 E C 8 4 0 Where: Bit 00 = TOR Z1 enabled TOR Z2 enabled TOR Z3 enabled TOR All Zones Bit 04 = TOR Dist. Scheme SOTF All Zones SOTF Lev. Detect. SOTF Z1 enabled Bit 08 = SOTF Z2 enabled SOTF Z3 enabled SOTF Z1 + Rev SOTF Z2 + Rev Bit 0C = SOTF Dist. Scheme SOTF I>3 enabled Bit 0E = SOTF Disabled		
Sets individual protection zones to enable or disable the TOR / SOTF protection. Setting the relevant bit to 1 will enable that zone, setting bits to 0 will disable distance zones: – TOR (or SOTF) Zi enabled: TOR or SOTF logic enabled in case of fault in zone i, – TOR (or SOTF) All Zones: TOR or SOTF logic enabled for all zone, – TOR (or SOTF) Dist. Scheme: Distance scheme in aided trip logic applied, – SOTF I>3 enabled: TOR and SOTF initiated after detection by I>3 overcurrents, – SOTF Lev. Detect.: SOTF initiated by level detectors. See SOTF / TOR section P44x/EN AP for TOR-SOFT logic and SOFT-TOR trip logic.				
SOTF Delay	110s	10.00s	3600s	1s
The Switch On To Fault (SOTF) protection (high speed clearance of any detected fault immediately following **manual closure** of the circuit breaker) and Trip On Reclose (TOR) protection (high speed clearance of any fault detected immediately following **autoreclosure** of the circuit breaker). It is possible to set the time-delay to trip when, for example, the relay has detected a fault that is still present on a feeder after energising.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DISTANCE SCHEMES				
Z1 Ext. on Chan. Fail	Disabled	Disabled or Enabled		
Enable or disable the “Z1X extension on channel fail”: For the duration of any alarm condition (loss of guard, loss of carrier), the “zone 1 extension” trip logic will be invoked if this option has been enabled.				
Weak Infeed				
WI: Mode Status	Disabled	Disabled, Echo, WI Trip & Echo, PAP		
Weak infeed logic can be enabled with weak infeed echo option or weak infeed trip option (PAP is a specific customer application). Refer to Weak Infeed section (P44x/EN AP) for mode status and settings.				
WI: Single Pole	Disabled	Disabled, Enabled		
Setting that defines the Weak Infeed tripping mode. When disabled, any WI trip will be converted to a 3 phase trip.				
WI: V< Thres.	45V	10V	70V	5V
Setting of Weak Infeed level detector. If phase – ground voltage in any phase drops below the threshold and with insufficient phase current for the protection to operate, the end is declared as a weak infeed terminal.				
WI: Trip Time Delay	0.06s	0	1s	0.002s
Setting for Weak Infeed trip time delay. For weak infeed trip options, see section P44x/EN AP.				
PAP: Del Trip En	Disabled	Disabled, Enabled		
PAP: P1 / P2 / P3	Disabled	Disabled, Enabled		
PAP: 1P / 2P / 3P Time Del	500 ms	100ms	1500s	100.0ms
PAP: IN Thres	500 mA	100mA	1A	10mA
PAP: K (%Vn)	500 e-3	500e-3	1.000	50e-3
PAP : Dist Block	Enabled	Disabled, Enabled		
If set to Enabled, the PAP scheme is blocked in case the distance start characteristic is asserted.				
Loss of Load				
The loss of load (LoL) provides fast fault clearance for faults (see P44x/EN AP, LOL section).				
LoL: Mode Status	Disabled	Disabled or Enabled		
Setting that enables (turns on) or disables (turns off) the Loss of Load scheme. When enabled, the loss of load logic provides fast fault clearance for faults over the whole of a double end fed protected circuit for all types of fault, except three phases.				
LoL: Chan. Fail	Disabled	Disabled or Enabled		
The Loss of Load logic can be chosen to be enabled when the channel associated with an aided scheme has failed.				
LoL: I<	0.5 x In	0.05 x In	1 x In	0.05 x In

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: DISTANCE SCHEMES				
LOL undercurrent detector that indicates a loss of load condition on the unfaulted phases, indicating that the remote end has just opened.				
LoL: Window	0.04s	0.01s	0.1s	0.01s
Length of LOL window - the time window in which Zone 2 accelerated tripping can occur following LOL undercurrent detector operation.				

2.3 Power Swing detection and blocking (PSB) (“Power swing” menu)

Power swings are oscillations in the power flow after a power system disturbance, caused by sudden removal of faults, loss of synchronism or power flow direction changing (as a result of switching). Such disturbances can cause generators acceleration or deceleration adapted to power flow, which in turn leads to power swinging.

A power swing may cause the impedance presented to a distance relay to move away from the normal load area and into one or more of its tripping characteristics. Depending on the setting or power swing stability, the relay should trip or not.

See section P44x/EN AP for power Swing complete description.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: POWER SWING				
Delta R	0.5 / In Ω	0	400 / In Ω	0.01 / In Ω
Power swing detection Resistive band which surrounds phase fault trip characteristic (see section P44x/EN AP, section 4.1). Typically, the ΔR and ΔX band settings are both set between 10 - 30% of R3Ph. This gives a secondary impedance between 0.6 and 1.8Ω. For convenience, 1.0Ω could be set. The width of the power swing band is calculated as follows: $\Delta R = 1.3 \times \tan(\pi \times \Delta f \times \Delta t) \times R_{LOAD}$ Assuming that the load corresponds to 60° angles between sources and if the resistive reach is set so that Rlim = $R_{LOAD}/2$, the following is obtained: $\Delta R = 0.032 \times \Delta f \times R_{LOAD}$ To ensure that a power swing frequency of 5Hz is detected, the following is obtained: $\Delta R = 0.16 \times R_{LOAD}$ Where: ΔR: width of the power swing detection band Δf: power swing frequency ($f_A - f_B$) Rlim resistive reach of the starting characteristic (=R3ph-R4ph) Z: network impedance corresponding to the sum of the reverse (Z4) and forward (Z3) impedances.				
Delta X	0.5 / In Ω	0	400 / In Ω	0.01 / In Ω
Power swing detection Reactive band which surrounds phase fault trip characteristic (see section P44x/EN AP…).				
IN > Status	Enabled	Disabled or Enabled		
Residual current power swing unblocking criteria activation: Enables or disables the earth fault protection during Power Swing Blocking. When enabled, the relay will trip when IN > ‘IN > (% Imax)’ or when IN < 0.1 × In.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: POWER SWING				
IN > (% Imax)	40%	10%	100%	1%
Residual current threshold for power swing unblocking. It is a percentage of the highest measured current on any phase. – Typical setting: 40% – Minimum setting (to avoid maloperation for asymmetric in power swing currents): > 30% – Maximum setting (to ensure unblocking for line faults): < 100%				
I2 > Status	Enabled	Disabled or Enabled		
Negative Sequence current power swing unblocking criteria activation: Enables or disables the phase-phase fault protection during Power Swing Blocking. When enabled, the relay will trip when I_2 > 'I2 > (% Imax)' or when I_2 < 0.1 × In.				
I2 > (% Imax)	30%	10%	100%	1%
Negative Sequence current threshold for power swing unblocking. It is a percentage of the highest measured current on any phase. – Typical setting: 30% – Minimum setting (to avoid maloperation for asymmetric in power swing currents): > 10% – Maximum setting (to ensure unblocking for line faults): < 50%				
Imax line > Status	Enabled	Disabled or Enabled		
Phase current power swing unblocking criteria activation: Enables or disables the three-phase fault protection during Power Swing Blocking. When enabled, the relay will trip when phase current threeshold exceeds Imax line >.				
Imax line >	3 x In	1 x In	20 x In	0.01 x In
Phase current threshold for power swing unblocking (unit:A) – Minimum setting: 1.2 × [maximum power swing current] – Maximum setting: 0.8 × [minimum phase fault current level]				
Delta I Status	Enabled	Disabled or Enabled		
Delta I criterion status activation: Enables or disables the unblocking logic three-phase fault protection during Power Swing Blocking. Time delay is settable.				
Unblocking Time delay	30s	0	30s	0.1s
Time-delay after which blocking criteria is automatically removed. Typical setting: – 30s if a near permanent block is required, – 2s if unblocking is required to split the system.				
Blocking Zones	00000000	Bit 0: Z1/Z1X Block, Bit 1: Z2 Block, Bit 2: Zp Block, Bit 3: Zq Block, Bit 4: Z3 Block, Bit 5: Z4 Block		
Allow zone blocking in case of a power swing. The Blocked Zones function bits are set to 1 to block zone tripping or are set to 0 to allow tripping as normal. When the criteria for power swing detection are met (3 single phase loop inside the quad & crossing the ∆R band in less than 5 ms in a 50 Hz network), and when out of step tripping is selected, then the distance protection with all of its stages is blocked – to prevent tripping by the distance protection (the relay can operate normally for any fault occurring during a power swing as there are different criteria which can be used by monitoring current & delta current).				
Out of Step	1	1	255	1
Threshold of number of out of steps. Triggers DDB #352 when reached. Setting of the number of steps to confirm Out Of Step (OOS) condition.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: POWER SWING				
Stable swing	1	1	255	1
Threshold of number of Stable Swings. Triggers DDB #353 when reached. Setting of the number of steps to confirm Stable Swing condition.				

2.4 Directional and non-directional overcurrent protection ("Back-up I>" menu)

The overcurrent protection included in the P442 and P444 relays provides two stage non-directional / directional three-phase overcurrent protection and two non-directional stages (I>3 and I>4), with independent time-delay characteristics. One or more stages may be enabled to complement the relay distance protection. All overcurrent and directional settings apply to all three-phases but are independent for each of the four stages. The first two stages of overcurrent protection, **I>1** and **I>2** have time-delayed characteristics that are selectable between inverse definite minimum time (IDMT), or definite time (DT).

All the stages trip three-phase only. They could be used for back up protection during a VT failure.

The following table shows the relay menu for overcurrent protection, including the available setting ranges and factory defaults.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – BACK-UP I>				
I>1 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse		
Sets the first phase overcurrent threshold (I>1) characteristics. The conditions are 'disabled', definite time (DT) or inverse definite minimum time (IDMT, see section P44x/EN AP).				
I>1 Direction	Directional Fwd	Non-Directional, Directional Fwd, Directional Rev		
Sets the directional control for the first stage overcurrent element.				
I>1 VTS Block	Non-Directional	Block, Non-Directional		
When the directional control for the 'I>1' is set, sets the Voltage Transformer Supervision (VTS) directionality (see section P44x/EN AP). The operation of the VTS will block the stage or will revert to Non-directional on operation of the VTS.				
I>1 Current Set	1.50 x In	0.08 x In	10.00 x In	0.01 x In
Sets the value for the overcurrent threshold.				
I>1 Time delay	1 s	0 s	100 s	0.01 s
Sets the time delay associated with I>1.				
I>1 Time delay VTS	0.2 s	0 s	100 s	0.01 s
Sets the VTS time-delay. The VTS alarm will occur if VT fault occurs during more than the VTS time-delay.				
I>1 TMS	1	0.025	1.2	0.005
Sets the Time Multiplier Setting (TMS), to adjust the operating time of the IEC IDMT characteristics.				
I>1 Time Dial	7	0.5	15	0.1
Sets the time dial settings, to adjust the operating time of the IEEE/ US IDMT curves. The Time Dial is a multiplier of the standard curve equation, to achieve the required tripping				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – BACK-UP I>				
time. The reference curve is based on Time Dial = 1. Care: Certain manufacturer's use a mid-range value of time dial = 5 or 7. So; it may be necessary to divide by 5 or 7 to achieve parity.				
I>1 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset / release characteristics of IEEE / US curves.				
I>1 tRESET	0	0	100 s	0.01 s
Setting that determines the reset / release time reset characteristics (see section P44x/EN AP).				
I>2 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse		
I>2 Direction	Non Directional	Non-Directional, Directional Fwd, Directional Rev		
Sets the second phase overcurrent threshold (I>2) characteristics. The conditions are 'disabled', definite time (DT) or inverse definite minimum time (IDMT, see chapter P44x/EN AP). Settings are the same as for the first stage overcurrent element.				
I>2 VTS Block	Non-Directional	Block, Non-Directional		
I>2 Current Set	2.00 x In	0.08 x In	10.00 x In	0.01 x In
I>2 Time delay	2 s	0 s	100 s	0.01 s
I>2 Time delay VTS	2 s	0 s	100 s	0.01 s
I>2 TMS	1	0.025	1.2	0.005
I>2 Time Dial	7	0.5	15	0.1
I>2 Reset Char	DT	DT or Inverse		
I>2 tRESET	0	0 s	100 s	0.01 s
I>3 Status	Enabled	Disabled or Enabled		
The third element is fixed as non-directional, for instantaneous or definite time delayed tripping.				
I>3 Current Set	3 x In	0.08 x In	32 x In	0.01 x In
I>3 Time delay	3 s	0 s	100 s	0.01 s
I>4 Status	Disabled	Disabled or Enabled		
The fourth element is only used for stub bus protection, where it is fixed as non-directional, and only enabled when the opto input Stub Bus Isolator Open (**Stub Bus Enable**) is energised. If the "stub bus enable" input is equal to 0, the I>4 function is still active, if the "stub bus enable" input is equal to 1, only the I>4 function is active (not I>1, I>2 and I>3).				
I>4 Current Set	4 x In	0.08 x In	32 x In	0.01 x In
I>4 Time Delay	4 s	0 s	100 s	0.01 s

I>4 should be used as a normal overcurrent stage if no stub bus condition is activated through the binary input Stub Bus Enabled.

2.5 Negative sequence overcurrent protection ("NEG sequence O/C" menu)

When applying traditional phase overcurrent protection, the overcurrent elements must be set higher than maximum load current, thereby limiting the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which

improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes.

Any unbalanced fault condition will produce negative sequence current of some magnitude. Therefore, a negative phase sequence overcurrent element can operate for both phase-to-phase and phase to earth faults.

The following section describes how negative phase sequence overcurrent protection may be applied in conjunction with standard overcurrent and earth fault protection to alleviate some less common application difficulties.

- Negative phase sequence overcurrent elements give greater sensitivity to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault relay due to the system configuration. For example, an earth fault relay applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element can be employed to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.
- Where rotating machines are protected by fuses, loss of a fuse produces a large amount of negative sequence current. This is a dangerous condition for the machine due to the heating effects of negative phase sequence current and so an upstream negative phase sequence overcurrent element may be applied to provide back-up protection for dedicated motor protection relays.
- It may be required to simply alarm for the presence of negative phase sequence currents on the system. Operators may then investigate the cause of the unbalance.

The negative phase sequence overcurrent element has a current pick up setting ‘I2> Current Set’, and is time delayed in operation by the adjustable timer ‘I2> Time Delay’. The user may choose to directionalise operation of the element, for either forward or reverse fault protection for which a suitable relay characteristic angle may be set. Alternatively, the element may be set as non-directional.

The relay menu for the negative sequence overcurrent element is shown below:

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – NEG SEQUENCE O/C				
I2>1 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse		
Sets the first negative sequence overcurrent (I2>1) characteristics. The conditions are ‘disabled’, definite time (DT) or inverse definite minimum time (IDMT).				
I2>1 Directional	Non-directional	Non-directional, Directional FWD, Directional REV		
Sets the directional control for the fault.				
I2>1 VTS Block	Block	Block, Non-directional		
When the directional control for the ‘I2>1’ is set, sets the Voltage Transformer Supervision (VTS) directionality. The operation of the VTS will block the stage or will revert to Non-directional on operation of the VTS.				
I2>1 Current Set	0.20 x In	0.08 x In	4.00 x In	0.01 x In
Sets the value for the negative sequence current threshold.				
I2>1 Time Delay	10.00 s	0 s	100.0 s	0.01 s
Sets the time delay associated with I2>1.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – NEG SEQUENCE O/C				
I2>1 Time VTS	0.200 s	0 s	100.0 s	0.01 s
Sets the VTS time-delay. The VTS alarm will occur if VT fault occurs during more than the VTS time-delay.				
I2>1 TMS	1.000	0.025	1.200	0.005
Sets the Time Multiplier Setting (TMS), to adjust the operating time of the IEC IDMT characteristics.				
I2>1 Time Dial	1.000	0.01	100.0	0.01
Sets the time dial settings, to adjust the operating time of the IEEE/ US IDMT curves. The Time Dial is a multiplier of the standard curve equation, to achieve the required tripping time. The reference curve is based on Time Dial = 1. Care: Certain manufacturer's use a mid-range value of time dial = 5 or 7. So; it may be necessary to divide by 5 or 7 to achieve parity.				
I2>1 Reset Char	DT	DT, Inverse		
Setting to determine the type of reset / release characteristics of IEEE / US curves.				
I2>1 tReset	0 s	0 s	100.0 s	0.01 s
Setting that determines the reset / release time reset characteristics.				
I2>2 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse		
I2>2 Directional	Non Directional	Non-Directional, Directional FWD, Directional REV		
Sets the second phase overcurrent threshold (I2>2) characteristics. The conditions are 'disabled', definite time (DT) or inverse definite minimum time (IDMT). Settings are the same as for the first stage overcurrent element.				
I2>2 VTS Block	Block	Block, Non-directional		
I2>2 Current Set	0.20 x In	0.08 x In	4.00 x In	0.01 x In
I2>2 Time Delay	10.00 s	0 s	100.0 s	0.01 s
I2>2 Time VTS	0.200 s	0 s	100.0 s	0.01 s
I2>2 TMS	1.000	0.025	1.200	0.005
I2>2 Time Dial	1.000	0.01	100.0	0.01
I2>2 Reset Char	DT	DT, Inverse		
I2>2 tReset	0 s	0 s	100.0 s	0.01 s
I2>3 Status	Disabled	Disabled, Enabled		
The third element is fixed as non-directional, for instantaneous or definite time delayed tripping.				
I2>3 Directional	Non Directional	Non-directional, Directional FWD, Directional REV		
I2>3 VTS Block	Block	Block, Non-directional		
I2>3 Current Set	0.20 x In	0.08 x In	4.00 x In	0.01 x In
I2>3 Time Delay	10.00 s	0 s	100.0 s	0.01 s
I2>3 Time VTS	0.200 s	0 s	100.0 s	0.01 s

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – NEG SEQUENCE O/C				
I2>4 Status	Disabled	Disabled, Enabled		
I2>4 Directional	Non Directional	Non-directional, Directional FWD, Directional REV		
I2>4 VTS Block	Block	Block, Non-directional		
I2>4 Current Set	0.20 x In	0.08 x In	4.00 x In	0.01 x In
I2>4 Time Delay	10.00 s	0 s	100.0 s	0.01 s
I2>4 Time VTS	0.200 s	0 s	100.0 s	0.01 s
I2> Char angle	- 45°	-95°	95°	1°
Where negative phase sequence current may flow in either direction through a relay location, such as parallel lines or ring main systems, directional control of the element should be employed (see section P44x/EN AP).				

2.6 Maximum of Residual Power Protection – Zero Sequence Power Protection ("Zero Seq Power" menu)

The 'Zero Seq Power' menu is displayed when 'CONFIGURATION/Earth Fault Prot' cell is set to "Zero Seq Power".

The following chart shows the adjustment menu for the zero-sequence residual overcurrent protection, the adjustment ranges and the default in-factory adjustments.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1 – ZERO-SEQ. POWER				
Zero Seq. Power Status	Activated	Activated / Disabled		
Setting that enables or disables the zero sequence power protection.				
K Time Delay Factor	0	0	2	0.2
Setting for the K time delay factor. The K time delay factor adjusts the IDMT T(s) time-delay. T(s) = K × (S_{ref}/S_r) where: – S_{ref} = Reference residual power – S_r = Residual power generated by the fault				
Basis Time Delay	1s	0 s	10 s	0.01s
Setting for the basis time delay.				
Residual Current	100mA	50mA	1A	10mA
Setting for the residual current.				
Residual power	500 mVA	300 mVA	6.0 VA	30.0 mVA
Setting to adjust the residual power threshold.				

2.7 Broken conductor detection

The following table shows the relay menu for the Broken Conductor protection, including the available setting ranges and factory defaults:

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – BROKEN CONDUCTOR				

Menu text	Default setting	Setting range		Step size
		Min	Max	
Broken Conductor	Enabled	Enabled, Disabled		
Setting that enables or disables the broken conductor protection.				
I2/I1	0.2	0.2	1	0.01
Setting to determine the pick-up level of the negative to positive current ratio.				
I2/I1 Time Delay	60 s	0 s	100 s	1 s
Setting for the function operating time-delay.				
I2/I1 Trip	Disabled	Enabled, Disabled		
Enables or disables the negative to positive current ratio protection. If disabled, only a Broken Conductor Alarm is possible.				

2.8 Directional and non-directional earth fault protection ("Earth fault O/C" menu)

The 'Earth fault O/C' menu is displayed when 'CONFIGURATION/Earth Fault Prot' cell is set to "Earth Fault O/C".

The following elements of earth fault protection are available, as follows:

- IN> element – Channel aided directional earth fault protection;
- IN>1 element – Directional or non-directional protection, definite time (DT) or IDMT time-delayed.
- IN>2 element – Directional or non-directional, DT and IDMT delayed.
- IN>3 element – Directional or non-directional, DT delayed.
- IN>4 element – Directional or non-directional, DT delayed.

The MiCOM P44x earth fault protection elements include four thresholds. The first and the second thresholds can be set as DT or IDMT trip delay time. The curves are the same as for the directional and non directional overcurrent protection (see section 2.4).

The IN> element may only be used as part of a channel-aided scheme, and is fully described in the Aided DEF section of the Application Notes.

The IN>1, IN>2, IN>3 and IN>4 backup elements always trip three pole, and have an optional timer hold facility on reset, as per the phase fault elements. (The IN> element can be selected to trip single and/or three pole).

All Earth Fault overcurrent elements operate from a residual current quantity which is derived internally from the summation of the three phase currents.

These current thresholds are activated as an exclusive choice with Zero sequence Power Protection:

The following table shows the relay menu for the Earth Fault protection, including the available setting ranges and factory defaults.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – EARTH FAULT O/C				
IN>1 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse		
Sets the first stage earth fault overcurrent (IN>1) characteristics. The conditions are 'disabled', definite time (DT) or inverse definite minimum time (IDMT).				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – EARTH FAULT O/C				
IN>1 Directional	Directional Fwd	Non-Directional, Directional Fwd, Directional Rev		
Sets the directional control for the first stage overcurrent element.				
IN>1 VTS Block	Non directional	Block, Non directional		
When the directional control for the 'IN>1' is set, sets the Voltage Transformer Supervision (VTS) directionality. The operation of the VTS will block the stage or will revert to Non-directional on operation of the VTS.				
IN>1 Current Set	0.2 x In	0.08 x In	10.0 x In	0.01 x In
Sets the value for the negative sequence current threshold.				
IN>1 Time Delay	1 s	0 s	200 s	0.01 s
Sets the time delay associated with IN>1. The setting is available only when DT function is selected.				
IN>1 Time Delay VTS	0.2 s	0 s	200 s	0.01 s
Sets the VTS time-delay. The VTS alarm will occur if VT fault occurs during more than the VTS time-delay.				
IN>1 TMS	1	0.025	1.2	0.005
Sets the Time Multiplier Setting (TMS) to adjust the operating time of the IEC IDMT characteristic.				
IN>1 Time Dial	7	0.5	15	0.1
Sets the time dial settings, to adjust the operating time of the IEEE/ US IDMT curves. The Time Dial is a multiplier of the standard curve equation, to achieve the required tripping time. The reference curve is based on Time Dial = 1. Care: Certain manufacturer's use a mid-range value of time dial = 5 or 7. So; it may be necessary to divide by 5 or 7 to achieve parity.				
IN>1 Reset Char	DT	DT, Inverse		
Setting that determines the reset / release time reset characteristics.				
IN>1 tRESET	0 s	0 s	100 s	0.01s
Sets the Time Hold Facility. The tReset is displayed when 'IN>1 Reset Char' definite time is selected (IEEE/US inverse curves).				
IN>2 Function	DT	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse		
Sets the second phase overcurrent threshold (IN>2) characteristics. The conditions are 'disabled', definite time (DT) or inverse definite minimum time (IDMT). Settings are the same as for the first stage overcurrent element.				
IN>2 Directional	Non Directional	Non-Directional, Directional Fwd, Directional Rev		
IN>2 VTS Block	Non directional	Block, Non directional		
IN>2 Current Set	1	0.025	1.2	0.005
IN>2 Time Delay	2 s	0 s	200 s	0.01 s
IN>2 Time Delay VTS	2 s	0 s	200 s	0.01 s
IN>2TMS	1	0.025	1.2	0.005

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – EARTH FAULT O/C				
IN>3 Status	Enabled	Disabled, Enabled		
The third element is fixed as non-directional, for instantaneous or definite time delayed tripping.				
IN>3 Directional	Non Directional	Non-Directional, Directional Fwd, Directional Rev		
This setting determines the direction of measurement for the earth fault overcurrent element.				
IN>3 VTS Block	Non directional	Block, Non directional		
IN>3 Current Set	0.3 x In	0.08 x In	32 x In	0.01 x In
IN>3 Time Delay	2 s	0 s	200 s	0.01 s
IN>3 Time Delay VTS	0.2 s	0 s	200 s	0.01 s
IN>4 Status	Enabled	Disabled, Enabled		
IN>4 Directional	Non Directional	Non-Directional, Directional Fwd, Directional Rev		
IN>4 VTS Block	Non directional	Block, Non directional		
IN>4 Current Set	0.3 x In	0.08 x In	32 x In	0.01 x In
IN>4 Time Delay	2 s	0 s	200 s	0.01 s
IN>4 Time Delay VTS	0.2 s	0 s	200 s	0.01 s
IN> DIRECTIONAL				
IN> Char Angle	–45°	–95°	95°	1°
Polarisation	Zero Sequence	Zero Sequence, Negative Sequence		
The applications of zero sequence and negative sequence polarisation are described in chapter P44x/EN AP (section Directional and non directional Earth Fault Protection).				
IN> BLOCKING				
IN> Block Pole Dead	Enabled	Disabled, Enabled		
This setting is to block IN> in case of Any Pole Dead or All Pole Dead.				

2.9 Aided Directional Earth Fault (DEF) protection schemes (“Aided D.E.F” menu)

The relay has aided scheme settings as shown in the following table:

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – AIDED D.E.F.				
Aided DEF Status	Enabled	Disabled, Enabled		
To enable (activate) or disable (turn off) the Directional Earth Fault Element that is used in an aided scheme.				
Polarisation	Zero Sequence	Zero Sequence, Negative Sequence		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – AIDED D.E.F.				
Setting that defines the method of DEF polarisation. Either zero, or negative sequence voltage can be taken as the directional reference. The applications of zero sequence and negative sequence polarisation are described in chapter P44x/EN AP, section Directional Directional and non directional Earth Fault Protection).				
V> Voltage Set	1 V	0.5 V	20 V	0.01 V
The V> threshold defines the minimum residual voltage required to enable the aided DEF directional decision. A residual voltage measured below this setting would block the directional decision, and so there would be no tripping from the scheme.				
IN Forward	0.1 × In	0.05 × In	4 × In	0.01 × In
Time Delay	0 s	0 s	10 s	0.1 s
Scheme Logic	Shared	Shared, Blocking, Permissive		
To select shared, blocking or permissive scheme logic.				
Tripping	Three Phase	Three Phase, Single Phase		
Tp	2 ms	0 ms	1s	2 ms
Aid Dist Delay (if blocking scheme not shared) Transmission time in blocking scheme. The Aided distribution time-delay (in the case of a blocking scheme covering the transmission time) settings will appear in the relay menu. Further customising of distance schemes can be achieved using the Programmable Scheme Logic to condition send and receive logic.				
IN Rev Factor	0,6	0	1	0.1
'IN Rev Factor' enhances the sensitivity for the residual current in case of reverse fault (for instance to create a faster blocking logic scheme).				
Block. Time Add.	0	0	10s	0.15s
"Block. Time Add." is an additional time-delay, set to extend a pole dead or convergence detection.				

2.10 Thermal overload ("Thermal overload" menu)

The following table shows the menu settings for the thermal protection element:

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – THERMAL OVERLOAD				
Thermal Char	Single	Disabled, Single, Dual		
Thermal characteristic setting. Available choices are: 'Disabled", 'Single' (for line and cable protection) and 'Dual' (for oil-filled transformers with natural air cooling protection).				
Thermal Trip	1In	0.08In	3.2In	0.01In
Sets the full load current (I_{FLC}) allowed and the pick-up threshold of the thermal characteristic.				
Thermal Alarm	70%	50%	100%	1%
An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be 'Thermal Trip' = 70% of thermal capacity.				
Time Constant 1	10 mn	1 mn	200 mn	1 mn
Setting for the thermal time constant (τ1) for a single time constant characteristic, or the first				

Menu text	Default setting	Setting range		Step size
		Min	Max	
time constant for the dual time constant characteristic.				
Time Constant 2	5 mn	1 mn	200 mn	1 mn
Setting for the second time constant (τ2) for the dual time constant characteristic.				

2.11 Residual overvoltage (neutral displacement) protection ("Residual overvoltage" menu)

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – RESIDUAL OVER-VOLTAGE				
VN Type	Residual	Residual, Homopolar		
Select residual or homopolar voltage.				
VN>1 Function	DT	Disabled, DT, IDMT		
Select the residual overvoltage stage 1 as either Inverse Definite Minimum Time (IDMT), Definite Time (DT) or disabled. The following submenus are visible according to this setting.				
VN>1 Voltage Set residual: homopolar (C7.x):	 5 V 1.5 V	 1 V 0.5 V	 80 V or 180V* 60 V	 1 V 0.5 V
Pick-up setting for the first stage residual overvoltage characteristic.				
VN>1 Time Delay	5.00 s	0 s	100.0 s	0.01 s
Operating time delay setting for the first stage definite time residual overvoltage element.				
VN>1 TMS	1.0	0.5	100.0	0.5
Setting for the Time Multiplier Setting to adjust the operating time of the IDMT characteristic. where K = Time Multiplier Setting (TMS), K = Operating time (in second) and M = measured voltage / relay setting voltage (V<).				
VN>1 tReset	0 s	0 s	100.0 s	0.5 s
Setting to determine the reset/release definite time for the first stage characteristic.				
VN>2 Status	Disabled	Enabled, Disabled		
Setting to enable or disable the second stage definite time residual overvoltage element.				
VN>2 Voltage Set residual: homopolar (C7.x):	 10 V 3 V	 1 V 0.5 V	 80 V or 180V* 60 V	 1 V 0.5 V
Pick-up setting for the second stage residual overvoltage element.				
VN>2 Time Delay	10.00 s	0 s	100.0 s	0.01 s
Operating time delay setting for the second stage residual overvoltage element.				

2.12 Undercurrent protection ("I< protection" menu)

This menu contains undercurrent protection functions.

2.12.1 Undercurrent protection

The undercurrent protection included within the P442 and P444 relays consists of two independent stages.

Two stages are included to provide both alarm and trip stages, where required. Alternatively, different time settings may be required depending on the severity of the current dip.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – I< PROTECTION				
I< mode	00	00	11	1
The protection is activated with: – first digit = 1 activates I<1 status, – second digit = 1 activates I<2 status.				
I<1 Status	Disabled	Disabled / Enabled		
Activates or deactivates the first stage undercurrent status. The two following submenus are visible when I<1 status is enabled.				
I<1 Current Set	0.05	0.08*I1	4*I1	0.01*I1
Pick-up setting for first stage undercurrent element.				
I<1 time Delay	1	0	100	0.01
Setting for the first stage undercurrent time-delay.				
I<2 Status	Disabled	Disabled / Enabled		
Activates or deactivates the second stage undercurrent status. The two following submenus are visible when I<2 status is enabled.				
I<2 Current Set	0.1	0.08*I1	4*I1	0.01*I1
Pick-up setting for second stage undercurrent element.				
I<2 Time Delay	2	0	100	0.01
Setting for the first stage undercurrent time-delay.				

2.13 Voltage protection (“Volt protection” menu)

This protection menu contains undervoltage and overvoltage protection.

2.13.1 Undervoltage protection

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – VOLT Protection				
V< & V> MODE	00000000	00000000	11111111	1
Activates individually undervoltage or overvoltage threshold, according to the following table:				

	1st digit							Last digit
V< & V> mode=	1	1	1	1	1	1	1	1
activates:	V<1 function	V<2 Status	V<3 Status	V<4 Status	V>1 function	V>2 Status	V>3 Status	V>4 Status

UNDER VOLTAGE		
V< Measur't Mode	Phase-Neutral	Phase-phase, Phase-neutral
Select the undervoltage protection to operate from a phase to phase voltage or phase to earth measurement.		
V<1 Function	DT	Disabled, DT, IDMT
Select the first undervoltage threshold as either Inverse Definite Minimum Time (IDMT), Definite Time (DT) or disabled. The three following submenus (Voltage, time delay and time multiplier setting) are visible according to this setting.		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – VOLT Protection				
V<1 Voltage Set	50 V	10 V	120 V	1 V
Sets the pick-up setting for first stage undervoltage element.				
V<1 Time Delay	10 s	0 s	100 s	0.01 s
Setting for the operating time-delay for the first stage definite time undervoltage element.				
V<1 TMS	1	0.5	100	0.5
The following formula defines the IDMT characteristics: t = K / (1 – M), where K = Time Multiplier Setting (TMS), K = Operating time (in second) and M = measured voltage / relay setting voltage (V<).				
V<2 Status	Disabled	Disabled, Enabled		
Enable or disable the second undervoltage threshold. The voltage and time-delay (following submenus) are settable when V<2 status is enabled. Stage 2 is DT only.				
V<2 Voltage Set	38 V	10 V	120 V	1 V
V<2 Time Delay	5 s	0 s	100 s	0.01 s
V<3 Status	Disabled	Disabled, Enabled		
Enable or disable 3rd undervoltage threshold. The voltage and time-delay (following submenus) are settable when V<3 status is enabled. Stage 3 is DT only.				
V<3 Voltage Set	30 V	10 V	120 V	1 V
V<3 Time Delay	1 s	0 s	100 s	0.01 s
V<4 Status	Disabled	Disabled, Enabled		
Enable or disable 4th undervoltage threshold. The voltage and time-delay (following submenus) are settable when V<4 status is enabled. Stage 4 is DT only.				
V<4 Voltage Set	25 V	10 V	120 V	1 V
V<4 Time Delay	1 s	0 s	100 s	0.01 s

2.13.2 Overvoltage protection

The following table shows the overvoltage section of this menu along with the available setting ranges and factory defaults. As can be seen, the setting cells for the overvoltage protection are identical to those previously described for the undervoltage protection.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – VOLT PROTECTION				
V< & V> MODE	0X700	V<1 Trip, V<2 Trip, V<3 Trip, V<4 Trip, V>1 Trip, V>2 Trip, V>3 Trip, V>4 Trip, V>1 A-AB Start, V>1 B-BC Start, V>1 C-CA Start		
This setting is a field type which allows both trip and start settings to be selected.				
OVERVOLTAGE				
V> Measur't Mode	Phase-Neutral	Phase-phase, Phase-neutral, Independent		
Select the overvoltage protection to operate from a phase to phase voltage, phase to earth measurement or Independent.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – VOLT PROTECTION				
V> % Hysteresis	2	0.1	2	1
Reset Ratio of all Overvoltage Stages.				
V>1 Function	DT	Disabled, DT, IDMT		
Select the first overvoltage threshold as either Inverse Definite Minimum Time (IDMT), Definite Time (DT) or disabled (see setting guidelines, section 2.4). The three following submenus (Voltage, time delay and time multiplier setting) are visible according to this setting.				
V>1 Voltage Set	75V	60V	185V	1V
Sets the pick-up setting for first stage overvoltage element.				
V>1 Time Delay	10s	0s	100s	0.01s
Setting for the operating time-delay for the first stage definite time overvoltage element.				
V>1 TMS	1	05	100	0.5
The following formula defines the IDMT characteristics: t = K / (M – 1), where K = Time Multiplier Setting (TMS), K = Operating time (in second) and M = measured voltage / relay setting voltage (V>).				
V>2 Status	Enabled	Disabled, Enabled		
Enable or disable the second overvoltage threshold. The voltage and time-delay (following submenus) are settable when V>2 status is enabled. Stage 2 is DT only.				
V>2 Voltage Set	90V	60V	185V	1V
V>2 Time Delay	0.5s	0s	100s	0.01s
V>3 Status	Enabled	Disabled, Enabled		
Enable or disable 3rd overvoltage threshold. The voltage and time-delay (following submenus) are settable when V>3 status is enabled. Stage 3 is DT only.				
V>3 Voltage Set	100V	60V	185V	1V
V>3 Time Delay	1s	0s	100s	0.01s
V>4 Status	Enabled	Disabled, Enabled		
Enable or disable 4th overvoltage threshold. The voltage and time-delay (following submenus) are settable when V>4 status is enabled. Stage 4 is DT only.				
V>4 Voltage Set	105V	60V	185V	1V
V>4 Time Delay	1s	0s	100s	0.01s
V>1 Measur't Mode	Phase-Neutral	Phase-phase, Phase-neutral		
This setting is to select the measurement mode Phase-Phase or Phase-Neutral for stage 1 of the Overvoltage Protection.				
V>2 Measur't Mode	Phase-Neutral	Phase-phase, Phase-neutral		
This setting is to select the measurement mode Phase-Phase or Phase-Neutral for stage 2 of the Overvoltage Protection.				
V>3 Measur't Mode	Phase-Neutral	Phase-phase, Phase-neutral		
This setting is to select the measurement mode Phase-Phase or Phase-Neutral for stage 3 of the Overvoltage Protection.				
V>4 Measur't Mode	Phase-Neutral	Phase-phase, Phase-neutral		
This setting is to select the measurement mode Phase-Phase or Phase-Neutral for stage 4				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – VOLT PROTECTION				
of the Overvoltage Protection.				

2.14 Frequency protection (“Freq protection” menu)

The frequency protection menu contains underfrequency and overfrequency protections, individually activated when the corresponding status is activated.

2.14.1 Underfrequency protection

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – FREQ PROTECTION				
UNDERFREQUENCY				
F<1 Status	Disabled	Disabled / Enabled		
Setting to enable or disable the first underfrequency element. The F<1 threshold setting and time-delay (following submenus) are settable when F<1 status is enabled.				
F<1 Setting	49.5Hz	45Hz	65Hz	0.01Hz
Setting that determines the pick-up threshold for the first stage underfrequency element.				
F<1 Time delay	4s	0s	100s	0.01s
Setting that determines the minimum operating time-delay for the first stage underfrequency element.				
F<2 Status	Disabled	Disabled / Enabled		
Setting to enable or disable the second underfrequency threshold (same setting as stage 1).				
F<2 Setting	49Hz	45Hz	65Hz	0.01Hz
F<2 Time delay	3s	0s	100s	0.01s
F<3 Status	Disabled	Disabled / Enabled		
Setting to enable or disable the 3rd underfrequency threshold (same setting as stage 1).				
F<3 Setting	48.5Hz	45Hz	65Hz	0.01Hz
F<3 Time delay	2s	0s	100s	0.01s
F<4 Status	Disabled	Disabled / Enabled		
Setting to enable or disable the 4th underfrequency threshold (same setting as stage 1).				
F<4 Setting	48Hz	45Hz	65Hz	0.01Hz
F<4 Time delay	1s	0s	100s	0.01s

2.14.2 Overfrequency protection

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – FREQ PROTECTION				
OVERFREQUENCY				
F>1 Status	Disabled	Disabled / Enabled		
Setting to enable or disable the first overfrequency element. The F>1 threshold setting and				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – FREQ PROTECTION				
time-delay (following submenus) are settable when F>1 status is enabled.				
F>1 Setting	50.5Hz	45Hz	65Hz	0.01Hz
Setting that determines the pick-up threshold for the first stage overfrequency element.				
F>1 Time delay	2s	0s	100s	0.01s
Setting that determines the minimum operating time-delay for the first stage overfrequency element.				
F>2 Status	Disabled	Disabled / Enabled		
Setting to enable or disable the second overfrequency threshold (same setting as stage 1).				
F>2 Setting	51Hz	45Hz	65Hz	0.01Hz
F>2 Time delay	1s	0s	100s	0.01s

1.1 Circuit breaker fail protection (CBF) (“CB Fail & I<” menu)

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – CB FAIL & I<				
BREAKER FAIL				
CB Fail 1 Status	Enabled	Enabled, Disabled		
Setting to enable or disable the first stage of the circuit breaker function.				
CB Fail 1 Timer	0.2 s	0 s	10 s	0.01 s
Setting for the circuit breaker fail timer stage 1, during which breaker opening must be detected.				
CB Fail 2 Status	Disabled	Enabled, Disabled		
Setting to enable or disable the second stage of the circuit breaker function.				
CB Fail 2 Timer	0.4 s	0 s	10 s	0.01 s
Setting for the circuit breaker fail timer stage 2, during which breaker opening must be detected.				
CBF Non I Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<, Prot Reset or I<, Disable		
Setting which determines the elements that will reset the circuit breaker fail time for undercurrent protection function initiated circuit breaker fail conditions.				
CBF Ext Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<, Prot Reset or I<, Disable		
Setting which determines the elements that will reset the circuit breaker fail time for external protection function initiated circuit breaker fail conditions.				

UNDER CURRENT I<				
I< Current Set	0.05 × In	0.05 × In	3.2 × In	0.01 × In
Setting that determines the circuit breaker fail timer reset current for overcurrent based protection circuit breaker fail initiation.				

3 NON-PROTECTION FUNCTIONS

3.1 Circuit breaker condition monitoring ("CB Condition" and "CB monitor setup" menus)

3.1.1 Circuit Breaker Condition Monitoring Features

For each circuit breaker trip and autoreclose operation the relay, records statistics. The '**CB condition'** and '**CB monitor setup**' menu cells are counter values only. The Min/Max values show the range of the counter values. These cells can be disabled:

Menu text	Default setting	Setting range		Step size
		Min	Max	
CB CONDITION				
CB Operations {3 pole tripping}	0	0	10000	1
Displays the total number of 3 pole trips issued by the relay.				
CB A Operations {1 & 3 pole tripping}	0	0	10000	1
Displays the total number of pole A trips issued by the relay (CB pole A).				
CB B Operations {1 & 3 pole tripping}	0	0	10000	1
Displays the total number of pole B trips issued by the relay (CB pole B).				
CB C Operations {1 & 3 pole tripping}	0	0	10000	1
Displays the total number of pole C trips issued by the relay (CB pole C).				
Total IA Broken	0	0	25000In^	1In^
Displays the total fault current interrupted by the relay for the A phase.				
Total IB Broken	0	0	25000In^	1In^
Displays the total fault current interrupted by the relay for the B phase.				
Total IC Broken	0	0	25000In^	1In^
Displays the total fault current interrupted by the relay for the C phase.				
CB Operate Time	0	0	0.5s	0.001
Displays the calculated Circuit Breaker operating time.				
Reset CB Data	No	Yes, No		
Allows the user to reset the calculated circuit breakers counters.				
Total 1P Reclosures	0	0	0.5s	0.001
Number of autoreclosures (1P)				
Total 3P Reclosures	0	0	0.5s	0.001
Number of autoreclosures (3P)				
Reset Total A/R	No	Yes, No		
Allows the user to reset the auto-reclose counters.				

3.1.2 CB condition monitoring

The following table, detailing the options available for the CB condition monitoring, includes the setup of the current broken facility and those features which can be set to raise an alarm or CB lockout.

Menu text	Default setting	Setting range		Step size
		Min	Max	
CB MONITOR SETUP				
Broken I^	2	1	2	0.1
This sets the factor to be used for the cumulative I^ counter calculation that monitors the cumulative severity of the duty placed on the interrupter. This factor is set according to the type of Circuit Breaker used.				
I^ Maintenance	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Setting which determines if an alarm will be raised or not when the cumulative I^ maintenance counter threshold is exceeded.				
I^ Maintenance	1000In^	1In^	25000In^	1In^
Setting that determines the threshold for the cumulative I^ maintenance counter monitors.				
I^ Lockout	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Setting which determines if an alarm will be raised or not when the cumulative I^ lockout counter threshold is exceeded.				
I^ Lockout	2000In^	1In^	25000In^	1In^
Setting that determines the threshold for the cumulative I^ lockout counter monitor. Set that should maintenance not be carried out, the relay can be set to lockout the autoreclose function on reaching a second operations threshold.				
N° CB Ops Maint	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Setting to activate the number of circuit breaker operations maintenance alarm.				
N° CB Ops Maint	10	1	10000	1
Sets the threshold for number of circuit breaker operations maintenance alarm, indicating when preventative maintenance is due.				
N° CB Ops Lock	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Setting to activate the number of circuit breaker operations lockout alarm.				
N° CB Ops Lock	20	1	10000	1
Sets the threshold for number of circuit breaker operations lockout. The relay can be set to lockout the auto-reclose function on reaching a second operations threshold.				
CB Time Maint	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Setting to activate the circuit breaker operating time maintenance alarm.				
CB Time Maint	0.1s	0.005s	0.5s	0.001s
Setting for the circuit operating time threshold which is set in relation to the specified interrupting time of the circuit breaker.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
CB Time Lockout	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Setting to activate the circuit breaker operating time lockout alarm.				
CB Time Lockout	0.2s	0.005s	0.5s	0.001s
Setting for the circuit breaker operating time threshold which is set in relation to the specified interrupting time of the circuit breaker. The relay can be set to lockout the auto-reclose function on reaching a second operations threshold.				
Fault Freq Lock	Alarm Disabled	Alarm Disabled, Alarm Enabled		
Enables the excessive fault frequency alarm.				
Fault Freq Count	10	0	9999	1
Sets a circuit breaker frequent operations counter that monitors the number of operations over a set time period.				
Fault Freq Time	3600s	0	9999s	1s
Sets the time period over which the circuit breaker operations are to be monitored. Should the set number of trip operations be accumulated within this time period, an alarm can be raised. Excessive fault frequency/trips can be used to indicate that the circuit may need maintenance attention (e.g. Tree-felling or insulator cleaning).				
Lockout reset	No	Yes / No		
Allows the user to reset the Lockout condition counters.				
Reset lockout by	CB Close	CB Close / User interface		
Setting that determines if a lockout condition will be reset by a manual circuit breaker close command or via the user interface.				
Man Close RstDly	5	0.01	600	0.01
The manual close time, time delay, that is used to reset a lockout automatically from a manual close.				

3.2 Circuit Breaker Control ("CB Control" menu)

The relay includes the following options for control of a single circuit breaker:

- Local tripping and closing, via the relay menu
- Local tripping and closing, via relay opto-isolated inputs
- Remote tripping and closing, using the relay communications

The following table shows the available settings and commands associated with circuit breaker control. Depending on the relay model some of the cells may not be visible:

Menu text	Default setting	Setting range		Step size
		Min	Max	
CB CONTROL				
CB Control by	Disabled	Disabled, Local, Remote, Local+Remote, Opto, Opto+local, Opto+Remote,		

Menu text	Default setting	Setting range		Step size
		Min	Max	
CB CONTROL				
		Opto+Rem+local		
This setting selects the type of circuit breaker control that be used in the logic (trip and close): – Local: Local trip or close of the circuit breaker using the front panel of the relay ('System Data / CB Trip/Close' menu), – Remote: Remote trip and close using MiCOM S1 Agile and communications, – Opto: Local trip and close using DDB:'Man. Trip CB' or 'Man. Close CB'				
Close Pulse Time	0.5s	0.1s	10s	0.01s
Defines the duration of the close pulse.				
Trip Pulse Time	0.5s	0.1s	5s	0.01s
Defines the duration of the trip pulse.				
Man Close Delay	10s	0.01s	600s	0.01s
This defines the delay time before the close pulse is executed.				
Healthy Window	5s	0.01s	9999s	0.01s
A settable time delay included for manual closure with this circuit breaker check. If the circuit breaker does not indicate a healthy condition in this time period following a close command then the relay will lockout and alarm.				
C/S Window	5s	0.01s	9999s	0.01s
A user settable time delay is included for manual closure with check synchronizing. If the check sync. criteria are not satisfied in this time period following a close command the relay will lockout and alarm.				
A/R Single Pole {P442/P444): 1&3 pole A/R only}	Disabled	Disabled, Enabled Enables the 1-pole trip mode function when autoreclose (A/R) is enabled, refer to Autoreclose notes for further information		
Enable or disable AR for single phase fault types. Care: This setting also applies when auto-reclose is configured in 3 pole tripping applications. Even though the trip mode may be 3 pole only, the fact that the initiation was a single phase fault type is memorized.				
A/R Three Pole	Disabled	Disabled, Enabled Enables the 3-pole trip mode function when autoreclose (A/R) is enabled,, refer to Autoreclose notes for further information		
Enable or disable AR for multi-phase faults. 'A/R Single Pole' and 'A/R Three pole' cells are only displayed when internal autoreclose is enabled ('Configuration / Internal A/R' cell).				

Menu text	Default setting	Setting range		Step size
		Min	Max	
CB CONTROL				
'A/R Single Pole' and 'A/R Three pole' must be enabled for validating the autoreclose function ("Autoreclose" menu, 1 pole (1P) and 3 poles (3P) cells. If "three pole autoreclose (A/R TPAR Enable') or single pole autoreclose ('A/R SPAR Enable') opto inputs are assigned in the PSL, these inputs have priority and will enable or disable the single or three poles autoreclose function (regardless of the MiCOM S1 Agile or front panel settings).				

3.3 CT and VT ratio

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
CT AND VT RATIOS				
Main VT Primary	110.0 V	100.0 V	1.000 MV	1.000 V
Sets the phase Voltage Transformer input primary voltage rating.				
Main VT's Sec'y	110.0 V	80.00 V	140.0 V	1.000 V
Sets the phase Voltage Transformer input secondary voltage rating.				
4th VT Primary	110.0 V	100.00 V	1.000 MV	1.000 V
Sets the 4th Voltage Transformer input primary current rating. This VT can be used either for synchro-check or residual voltage measurement.				
4th VT Secondary	110.0 V	100.00 V	140.0 V	1.000 V
Sets the Check Synchronisation Voltage Transformer input secondary current rating.				
Phase CT Primary	1.000 A	1.000 A	30.00 kA	1.000 A
Sets the phase Current Transformer input primary current rating.				
Phase CT Sec'y	1.000 A	1 A / 5 A		
Sets the phase Current Transformer input secondary current rating.				
MComp CT Primary	1.000 A	1.000 A	30.00 kA	1.000 A
Sets the mutual compensation Current Transformer input primary current rating: Analysis of an earth fault on one circuit of a parallel over-head line shows that a fault locator positioned at one end of the faulty line will tend to over-reach while that at the other end will tend to under-reach. In cases of long lines with high mutual inductance, mutual zero sequence compensation can be used to improve the fault locator accuracy. The compensation is achieved by taking an input to the relay from the residual circuit of the current transformers in the parallel line. This CT can be used either for mutual compensation or residual current measurement.				
MComp CT Sec'y	1.000 A	1 A / 5 A		
Sets the mutual compensation Current Transformer input secondary current rating.				
C/S input	A-N	A-N / B-B / C-N / A-B / B-C / C-A		
The check synchronism VT input may be connected to either a phase to phase or phase-to-neutral voltage and for correct synchronism check operation, the relay has to be programmed with the required connection. The "C/S Input" setting should be set to A-N, B-N, C-N, A-B, B-C or C-A as appropriate.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
CT AND VT RATIOS				
Main VT Location	Line	Line / Bus		
The Check Sync VT may be connected to either a phase to phase or phase to neutral voltage. Depending on the particular system arrangement, the main three phase VT for the relay may be located on either the busbar or the line. Therefore, the relay needs to be programmed with the location of the main voltage transformer.				
CT polarity	Standard	Standard / Inverted		
Standard or reverse phase sequence can be selected. This menu sets this phase sequence.				
Measured VN *	Disabled	Enabled or Disabled		
This setting specifies if the neutral voltage is measured or derived from the sum of three phase voltages. If this setting is set to Enabled, all function related with synchro-check function become invisible.				
Measured IN *	Disabled	Enabled or Disabled		
This setting specifies if the neutral current is measured or derived from the sum of three phase currents. If this setting is set to Enabled, all function related with Mutual Coupling become invisible.				

3.4 “Record control” column

It is possible to disable the reporting of events from all interfaces that supports setting changes. The settings that control the various types of events are in the “Record Control” column. The effect of setting each to disabled is as follows:

This column is visible when the “Record Control” setting (“Configuration” column) = “visible”.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
RECORD CONTROL				
Clear Event	No	No or Yes		
Selecting “Yes” will cause the existing event log to be cleared and an event will be generated indicating that the events have been erased.				
Clear Faults	No	No or Yes		
Selecting “Yes” will cause the existing fault records to be erased from the relay.				
Clear Maint.	No	No or Yes		
Selecting “Yes” will cause the existing maintenance records to be erased from the relay.				
Alarm Event	Enabled	Enabled or Disabled		
Disabling this setting means that all the occurrences that produce an alarm will result in no event being generated.				
Relay O/P Event	Enabled	Enabled or Disabled		
Disabling this setting means that no event will be generated for any change in logic input state.				
Opto Input Event	Enabled	Enabled or Disabled		
Disabling this setting means that no event will be generated for any change in logic input state.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
RECORD CONTROL				
System Event	Enabled	Enabled or Disabled		
Disabling this setting means that no System Events will be generated.				
Fault Rec. Event	Enabled	Enabled or Disabled		
Disabling this setting means that no event will be generated for any fault that produces a fault record.				
Maint. Rec. Event	Enabled	Enabled or Disabled		
Disabling this setting means that no event will be generated for any occurrence that produces a maintenance record.				
Protection Event	Enabled	Enabled or Disabled		
Disabling this setting means that any operation of protection elements will not be logged as an event.				
Clear Dist Recs	No	No or Yes		
Selecting “Yes” will cause the existing disturbance records to be cleared and an event will be generated indicating that the disturbance records have been erased.				
DDB 31 - 0	11111111111111111111111111111111			
Displays the status of DDB signals 0 – 31.				
DDB 2047 - 2016	11111111111111111111111111111111			
Displays the status of DDB signals2016– 2047.				

3.5 Disturbance recorder (“Disturb recorder” menu)

The integral disturbance recorder has an area of memory specifically set aside for record storage. The number of records that may be stored is dependent on the selected recording duration but the relays typically have the capability of storing a minimum of 20 records, each of 10.5 second duration.

NOTE:
1. Compressed Disturbance Recorder used for Kbus/Modbus/DNP3 reach that typical size value (10.5 sec duration)
2. Uncompressed Disturbance Recorder used for IEC 60870-5/103 could be limited to 2 or 3 seconds.

Disturbance records continue to be recorded until the available memory is exhausted, at which time the oldest record(s) are overwritten to make space for the newest one.

The recorder stores actual samples which are taken at a rate of 48 samples per cycle.

Each disturbance record consists of eight analogue data channels and 64 digital data channels. Note that the relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities).

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
DISTURB RECORDER				
Duration	600 s	100.0 ms	10.5 s	10.00 ms
This sets the overall recording time.				
Trigger Position	33.3%	0.0%	100.0%	0.10 %

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
DISTURB RECORDER				
This sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1.0 s post fault recording times.				
Trigger Mode	Single	Single / Extended		
When set to single mode, if a further trigger occurs whilst a recording is taking place, the recorder will ignore the trigger.				
"ANALOG CHANNEL" submenus				
Analog. Channel 1 to Analog Channel 8	VA	VA, VB, VC, VN, IA, IB, IC, IN, IM, V Checksync1, unassigned or V Checksync 2		
Assign an analogue input of the relay to an analogue channel.				
"DIGITAL INPUT" and "INPUT TRIGGER" submenus				
Digital Input xx	Relay xx or 'Not used'	Any O/P Contacts or Any Opto Inputs or Internal Digital Signals		
The relay 1 output digital channel is assigned to digital input 1 channel. The digital channel will trigger the disturbance recorder when the corresponding assigned fault will occur. In this case, the digital recorder will trigger when the output R1will change. Following lines indicate default signals for the 64 Channels.				
Input xx Trigger	No Trigger	No Trigger, Trigger L/H, Trigger H/L		
This digital channel will not trigger the Disturbance recorder. When "Trigger L/H" is selected, the channel will trigger the disturbance recorder when changing from '0' (low Level) to '1' (High level). If "Trigger H/L" is selected, it will trigger when changing from '1' (high level) to '0' (low level).				

Note

The available analogue and digital signals differ between relay types and models.

The pre and post fault recording times are set by a combination of the 'Duration' and 'Trigger Position' cells. 'Duration' sets the overall recording time and the 'Trigger Position' sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

If a further trigger occurs whilst a recording is taking place, the recorder will ignore the trigger if the 'Trigger Mode' has been set to 'Single'. However, if this has been set to 'Extended', the post trigger timer will be reset to zero, thereby extending the recording time.

As can be seen from the menu, each of the analogue channels is selectable from the available analogue inputs to the relay. The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to a number of internal relay digital signals, such as protection starts, LEDs etc. The complete list of these signals may be found by viewing the available settings in the relay menu or via a setting file in MiCOM S1 Agile. Any of the digital channels may be selected to trigger the disturbance recorder on either a low to high or a high to low transition, via the 'Input Trigger' cell. The default trigger settings are that any dedicated trip output contacts (e.g. relay 3) will trigger the recorder.

3.6 Measurements (“Measure’t setup” column)

This column is visible when the “Measure’t Setup” setting (“Configuration” column) = “visible”.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
MEASUREMENT SETUP				
Default Display	Description	Description / Plant Reference / U – I – Freq / P – Q / Date and Time		
This setting can be used to select the default display from a range of options, note that it is also possible to view the other default displays whilst at the default level using the 4□ and 6 keys. However once the 15 minute timeout elapses the default display will revert to that selected by this setting.				
Local Values	Secondary	Primary/Secondary		
This setting controls whether measured values are displayed as primary or secondary quantities.				
Remote Values	Primary	Primary/Secondary		
This setting controls whether measured values are displayed as primary or secondary quantities.				
Measurement Ref	VA	VA / VB / VC / IA / IB or IC		
Using this setting the phase reference for all angular measurements by the relay can be selected.				
Measurement Mode	0	0 / 1 / 2 or 3		

This setting is used to control the signing of the real and reactive power quantities; the signing convention used is defined in the following table:

Measurement Mode	Parameter	Signing
0 (Default, P = VI*)	Export Power	+
	Import Power	–
	Lagging VArs	+
	Leading VArs	–
1	Export Power	–
	Import Power	+
	Lagging VArs	+
	Leading VArs	–
2	Export Power	+
	Import Power	–
	Lagging VArs	–
	Leading VArs	+
3	Export Power	–
	Import Power	+
	Lagging VArs	–
	Leading VArs	+

Demand Interval	30 min	1.00 mn	99.00 mn	1 mn
This setting defines the length of the fixed demand window.				
Distance Unit	Kilometres	Kilometres / Miles		
This setting is used to select the unit of distance for fault location purposes, note that the length of the line is preserved when converting from km to miles and visa versa.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
MEASUREMENT SETUP				
Fault Location	Distance	Distance / Ohm / % of Line		
The calculated fault location can be displayed using one of several options selected using this setting.				

3.7 "Communications" column

The communications settings are available in the menu 'Communications' column and are displayed when the "Comms Settings" setting ("Configuration" column) = "visible".

3.7.1 Communications settings for courier protocol

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	Courier			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	255	7	34	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
Physical Link	Copper	Copper, (RS485), Fibre optic		
This cell defines whether an electrical connection ("Copper" or "RS485" according to software version) or fiber optic connection is being used for communication between the master station and relay. The optional fiber optic communications board will be required if 'Fiber optic' is to be selected.				
RP1 Status	Data			
This cell indicates the status of the rear communication board.				
RP1 Port Config.	KBus	KBus or EIA(RS)485		
This cell defines whether an electrical KBus or EIA(RS)485 is being used for communication between the master station and relay.				
RP1 Comms. Mode	IEC60870 FT1.2	IEC60870 FT1.2 or 10-Bit No Parity		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				

3.7.2 Communication settings for IEC 60870-5-103

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	IEC60870-5-103			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	255	7	34	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
Measur't period	10s	1s	60s	1s
This cell controls the time interval that the relay will use between sending measurement data to the master station.				
Physical Link	RS485	RS485, Fibre optic		
This cell defines whether an electrical connection ("Copper") or fiber optic connection is being used for communication between the master station and relay. The optional fiber optic communications board will be required if 'Fiber optic' is to be selected.				
CS103 Blocking	Disabled	Disabled, Monitor blocking, Command blocking		
There are three settings associated with this cell: Disabled – No blocking selected. Monitor Blocking – When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the relay returns a "termination of general interrogation" message to the master station. Command Blocking – When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the relay returns a "negative acknowledgement of command" message to the master station.				
RP1 Status	Data			
This cell indicates the status of the rear communication board.				
RP1 Port Config.	KBus	KBus or EIA(RS)485		
This cell defines whether an electrical KBus or EIA(RS)485 is being used for communication between the master station and relay.				
RP1 Comms. Mode	IEC60870 FT1.2	IEC60870 FT1.2 or 10-Bit No Parity		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				

3.7.3 Communication settings for Modbus protocol

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	Modbus			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	255	7	34	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
Parity	None	Odd, Even or None		
This cell controls the parity format used in the data frames. It is important that both relay and master station are set with the same parity setting.				
Physical Link	RS485	RS485, Fibre optic		
This cell defines whether an electrical connection (“Copper”) or fiber optic connection is being used for communication between the master station and relay. The optional fiber optic communications board will be required if ‘Fiber optic’ is to be selected.				
Date/Time Format	Disabled	Disabled, Enabled		
This cell allows the user to set the “Modbus IEC Time and Date format” at the user interface and front/2nd port besides the Modbus 1st rear port. When ‘Disabled’ is selected, the “Standard IEC” time format complies with IEC 60870-5-4 requirements such that byte 1 of the information is transmitted first, followed by bytes 2 through 7. When ‘Enabled’ is selected, the transmission of information is reversed (Reverse IEC time format).				
RP1 Status	Data			
This cell indicates the status of the rear communication board.				
RP1 Port Config.	KBus	KBus or EIA(RS)485		
This cell defines whether an electrical KBus or EIA(RS)485 is being used for communication between the master station and relay.				
RP1 Comms. Mode	IEC60870 FT1.2	IEC60870 FT1.2 or 10-Bit No Parity		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				

3.7.4 Communication settings for DNP3.0 protocol

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	Protocol			
Indicates the communications protocol that will be used on the rear communications port.				
RP1 Address	255	7	34	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
Parity	None	Odd, Even or None		
This cell controls the parity format used in the data frames. It is important that both relay and master station are set with the same parity setting.				
Measur't period	10s	1s	60s	1s
This cell controls the time interval that the relay will use between sending measurement data to the master station.				
Physical Link	RS485	RS485, Fibre optic		
This cell defines whether an electrical connection ("Copper") or fiber optic connection is being used for communication between the master station and relay. The optional fiber optic communications board will be required if 'Fiber optic' is to be selected.				
Time Sync	Disabled	Disabled, Enabled		
This setting enables or disables time synchronization with master Clock.				
Date/Time Format	Disabled	Disabled, Enabled		
This cell allows the user to set the "Modbus IEC Time and Date format" at the user interface and front/2nd port besides the Modbus 1st rear port. When 'Disabled' is selected, the "Standard IEC" time format complies with IEC 60870-5-4 requirements such that byte 1 of the information is transmitted first, followed by bytes 2 through 7. When 'Enabled' is selected, the transmission of information is reversed (Reverse IEC time format).				
RP1 Status	Data			
This cell indicates the status of the rear communication board.				
RP1 Port Config.	KBus	KBus or EIA(RS)485		
This cell defines whether an electrical KBus or EIA(RS)485 is being used for communication between the master station and relay.				
RP1 Comms. Mode	IEC60870 FT1.2	IEC60870 FT1.2 or 10-Bit No Parity		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
If RP1 Status = “EIA(RS)485” or “K bus OK”: This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
Scale Value	IEC61850			
Indicates the Scale value (IEC61850 or DNP3.0).				
Message Gap (ms)	0	0	50	1
This setting allows the master station to have an interframe gap.				
DNP Need Time	10	1	30	1
Sets the time duration before next time synchronization request from the master.				
DNP App Fragment	2048	100	2048	1
Maximum message length (application fragment size) transmitted by the relay.				
DNP App Timeout	2	1	120	1
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master.				
DNP SBO Timeout	10s	1s	10s	1s
Duration of time waited (Select Before Operate mode), after receiving a select command and awaiting an operate confirmation from the master.				
DNP Link Timeout	0s	0s	120s	1s
Duration of time that the relay will wait for a Data Link Confirm from the master. A value of 0 means data link support disabled and 1 to 120 seconds is the timeout setting.				

3.7.5 Communications for Ethernet port – IEC 61850 protocol

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	IEC61850			
Indicates the communications protocol that will be used on the rear communications port.				
Scale Value	IEC61850			
Indicates the Scale value (IEC61850 or DNP3.0)				
NIC Protocol	DNP3.0	Courier, IEC60870-5-103, Modbus or DNP 3.0		
The NIC (Network Interface Cards) protocol cell Indicates that IEC 61850 will be used on the rear Ethernet port.				
NIC MAC Address	*Ethernet MAC Address*			
Indicates the MAC (Media Access Control) address of the rear Ethernet port. This address is formatted as a six-byte hexadecimal number, and is unique.				
NIC Tunl Timeout	5 mins	1 min	30 mins	1 min

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
Duration of time waited before an inactive tunnel to MiCOM S1 Agile is reset.				
NIC Link Report	Alarm	Alarm, Event, None		
Configures how a failed/unfitted network link (copper or fiber) is reported: Alarm - an alarm is raised for a failed link Event - an event is logged for a failed link None - nothing reported for a failed link				

3.7.5.1 Communications settings for Ethernet port – DNP3.0

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
NIC Protocol	DNP3.0			
The NIC (Network Interface Cards) protocol cell Indicates that IEC 61850 will be used on the rear Ethernet port.				
IP Address	*IP Address*			
Indicates the IP (Internet Protocol) address of the rear Ethernet port. This address is formatted as a six-byte hexadecimal number, and is unique.				
Subnet mask	*Subnet mask*			
Displays the sub-network that the relay is connected to.				
NIC MAC Address	*Ethernet MAC Address*			
Indicates the MAC (Media Access Control) address of the rear Ethernet port. This address is formatted as a six-byte hexadecimal number, and is unique.				
Gateway	*Gateway Address*			
Displays the IP address of the gateway (proxy) that the relay is connected to, if any.				
DNP Time Sync	Disabled	Disabled, Enabled		
If set to 'Enabled', the DNP3.0 master station can be used to synchronize the time on the relay. If set to 'Disabled' either the internal free running clock, or IRIG+B input are used.				
DNP Meas scaling	Primary	Primary, secondary or Normalized		
Setting to report values in terms of primary, secondary or normalized (with respect to the CT/VT ratio setting) values.				
NIC Tunl Timeout	5 mins	1 min	30 mins	1 min
Duration of time waited before an inactive tunnel to MiCOM S1 Agile is reset.				
NIC Link Report	Alarm	Alarm, Event, None		
Configures how a failed/unfitted network link (copper or fiber) is reported: Alarm - an alarm is raised for a failed link Event - an event is logged for a failed link None - nothing reported for a failed link				

SNTP Parameters				
SNTP Server 1	*SNTP server 1 Address*			
Time synchronization is supported using SNTP (Simple Network Time Protocol); this protocol is used to synchronize the internal real time clock of the relays. This cell displays the IP address of the primary SNTP server.				
SNTP Server 2	*SNTP server 21 Address*			
Displays the IP address of the secondary SNTP server.				
SNTP Poll rate	64s	64s	1024s	1s
Duration of SNTP poll rate in seconds.				
SNTP Need Time	10 mins	1 min	30 mins	1 min
Sets the time duration before next time synchronization request from the master.				
SNTP App Fragment	2048	100	2048	1
Maximum message length (application fragment size) transmitted by the relay.				
SNTP App Timeout	2s	1s	120s	1s
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master.				
SNTP SBO Timeout	10s	1s	10s	1s
Duration of time waited (Select Before Operate mode), after receiving a select command and awaiting an operate confirmation from the master.				

3.7.5.2 Rear port 2 connection settings

The settings shown are those configurable for the second rear port which is only available with the courier protocol.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
REAR PORT2 (RP2)				
RP2 Protocol	Courier			
Indicates the communications protocol that will be used on the rear communications port.				
RP2 Card Status.	data			
This cell indicates the status of the rear communication board.				
RP2 Port Config.	EIA RS232	EIA RS232, EIA RS485 or KBus		
This cell defines whether an electrical EIA(RS)232, EIA(RS)485 or KBus is being used for communication.				
RP2 Comms. Mode	IEC60870 FT1.2	IEC60870 FT1.2 or 10-bit		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP2 Address	255	0	255	1
This cell sets the unique address for the relay such that only one relay is accessed by master station software.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
COMMUNICATIONS				
REAR PORT2 (RP2)				
RP2 Inactivity Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP2 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				

3.8 "Commissioning tests" column

To help minimising the time required to test MiCOM relays the relay provides several test facilities under the 'COMMISSION TESTS' menu heading.

There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal digital data bus (DDB) signals and user-programmable LEDs to be monitored. Additionally there are cells to test the operation of the output contacts, user-programmable LEDs.

This column is visible when the "Commission tests" setting ("Configuration" column) = "visible".

Menu Text	Default Setting	Available Settings
COMMISSION TESTS		
Opto I/P Status	00000000000000000000000000000000	
This menu cell displays the status of the relay's opto-isolated inputs as a binary string, a '1' indicating an energized opto-isolated input and a '0' a de-energized one		
Relay Status 1	00000000000000000000000000000000	
Relay Status 2	00000000000000000000000000000000	
This menu cell displays the status of the digital data bus (DDB) signals that result in energisation of the output relays as a binary string, a **1** indicating an operated state and **0** a non-operated state. When the **Test Mode** cell (see below) is set to **Enabled**, the **Relay Status 1/2** cell does not show the current status of the output relays and so can not be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.		
Test Port Status	00000000	
This menu cell displays the status of the eight digital data bus (DDB) signals that have been allocated in the 'Monitor Bit' cells.		
LED Status	00000000	
This menu cell displays the status of the LEDs. that have been allocated in the 'Monitor Bit' cells, a '1' indicating a particular LED is lit and a '0' not lit.		

Menu Text	Default Setting	Available Settings
COMMISSION TESTS		
Monitor Bit 1	Relay Label 01	0 to 2047 See P44x/EN PL section for details of digital data bus signals
Monitor Bit 8	Relay Label 08	0 to 2047
The eight ‘Monitor Bit’ cells allow the user to select the status of which digital data bus signals can be observed in the ‘Test Port Status’ cell or via the monitor/download port.		
Test Mode	Disabled	Disabled / Test Mode/ Blocked
The Test Mode menu cell is used to ease the maintenance of another feeder relay or to allow secondary injection testing to be performed on the relay without operation of the connected zone. It also enables a facility to directly test the output contacts by applying menu controlled test signals. To select a test mode, select ‘Test Mode’. It causes an alarm condition to be recorded and the yellow ‘Out of Service’ LED to illuminate and an alarm message. However the output contacts are still active in this mode. To disable the output contacts in addition to the above, select ‘Blocked’. Once testing is complete the cell must be set back to ‘Disabled’ to restore the relay back to service. **WHEN THE ‘TEST MODE’ CELL IS SET TO ‘BLOCKED’ THE RELAY SCHEME LOGIC DOES NOT DRIVE THE OUTPUT RELAYS AND SO THE PROTECTION WILL NOT TRIP THE ASSOCIATED CIRCUIT BREAKER IF A FAULT OCCURS.** **HOWEVER, THE COMMUNICATIONS CHANNELS WITH REMOTE RELAYS REMAIN ACTIVE WHICH, IF SUITABLE PRECAUTIONS ARE NOT TAKEN, COULD LEAD TO THE REMOTE ENDS TRIPPING WHEN CURRENT TRANSFORMERS ARE ISOLATED OR INJECTION TESTS ARE PERFORMED.**		
Test Pattern 1	00000000000000000000	0 = Not Operated 1 = Operated
Test Pattern 2	00000000000000000000	0 = Not Operated 1 = Operated
Visible when “Test Mode” is disabled This cell is used to select the output relay (or high break relay) contacts that will be tested when the ‘Contact Test’ cell is set to ‘Apply Test’.		
Contact Test	No Operation	No Operation, Apply Test, Remove Test
Visible when “Test Mode“ is disabled. When the ‘Apply Test’ command in this cell is issued the contacts set for operation (set to ‘1’) in the ‘Test Pattern’ cell change state. After the test has been applied the command text on the LCD will change to ‘No Operation’ and the contacts will remain in the Test State until reset issuing the ‘Remove Test’ command. The command text on the LCD will again revert to ‘No Operation’ after the ‘Remove Test’ command has been issued. Note: When the ‘Test Mode’ cell is set to ‘Enabled’ the ‘Relay O/P Status’ cell does not show the current status of the output relays and so can not be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.		
Test LEDs	No Operation	No Operation Apply Test
When the ‘Apply Test’ command in this cell is issued the eighteen user-programmable LEDs will illuminate for approximately 2 seconds before they extinguish and the command text on the LCD reverts to ‘No Operation’.		

Menu Text	Default Setting	Available Settings
COMMISSION TESTS		
Autoreclose test	No Operation	No operation / 3 pole test / Pole A Test / Pole B test / pole C test
Where the relay provides an auto-reclose function, this cell will be available for testing the sequence of circuit breaker trip and auto-reclose cycles with the settings applied. Issuing the command 'Trip 3 Pole' will cause the relay to perform the first three phase trip/reclose cycle so that associated output contacts can be checked for operation at the correct times during the cycle. Once the trip output has operated the command text will revert to 'No Operation' whilst the rest of the auto-reclose cycle is performed. To test subsequent three phase auto-reclose cycles repeat the '3 Pole Trip' command. Similarly, where single pole auto-reclosing is available, the cycles for each single pole can be checked by sequentially issuing the 'Trip Pole A', 'Trip Pole B' or 'Trip Pole C', as appropriate. Note: The factory settings for the relay's programmable scheme logic has the 'AR Trip Test' signal mapped to relay 3. If the programmable scheme logic has been changed, it is essential that this signal remains.		
Red LED Status	000000000000000000	
This cell is an eighteen bit binary string that indicates which of the user-programmable LEDs on the relay are illuminated with the Red LED input active when accessing the relay from a remote location, a '1' indicating a particular LED is lit and a '0' not lit.		
Green LED Status	000000000000000000	
This cell is an eighteen bit binary string that indicates which of the user-programmable LEDs on the relay are illuminated with the Green LED input active when accessing the relay from a remote location, a '1' indicating a particular LED is lit and a '0' not lit.		
DDB 31 - 0	11111111111111111111111111111111	
Displays the status of DDB signals 0 – 31.		
DDB 2047 - 2016	11111111111111111111111111111111	
Displays the status of DDB signals 2016 – 2047.		

3.9 Opto inputs configuration ("Universal Input" menu)

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
Universal Inputs				
Global Nominal V	48/54V	24/27V, 30/34V, 48/54V, 110/125V, 220/250V, Custom		
Sets the nominal battery voltage for all opto inputs by selecting one of the five standard ratings in the Global Nominal V settings. If Custom is selected then each opto input can individually be set to a nominal voltage value.				
Opto Input 1 – 32	24/27V	24/27V, 30/34V, 48/54V, 110/125V, 220/250V		
Each opto input can individually be set to a nominal voltage value if custom is selected for the global setting.				
Opto Filter Ctrl	0×FFFFFFFF			
This menu is used to control the relay's opto-isolated inputs L1 (last digit) to L32 (first digit). Hexadecimal values, from 0 (hexa) = 0000 (binary) to F= "1111", are used to control four opto-isolated inputs. . A binary '1' indicates an energized and operating relay, a binary '0' indicates a de-energized.				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
Universal Inputs				
Characteristics	Standard 60%-80%	50% - 70 % / Standard 60%-80%		
Controls the changement of state of opto isolated inputs, according to the nominal voltage value.				

3.10 HOTKEYS / Control inputs ("Control input", "Ctrl I/P config" and "Ctrl I/P label" menus)

There are three setting columns associated with the control inputs which are: "CTRL INPUTS", "CTRL I/P CONFIG" and "CTRL I/P LABELS".

The "CTRL INPUTS" column is visible when the "Commission tests" setting ("Configuration" column) = "visible".

Menu Text	Default Setting	Available Setting
CTRL INPUTS		
Ctrl I/P Status	00000000000000000000000000000000	
Displays the status of the opto-isolated inputs from L1 (last digit) to L32 (first digit): "0" = Reset and "1" = Set. The control inputs can also be set and reset by setting a "1" to set or "0" to reset a control input.		
Control Input 1	No Operation	Set / Reset / No Operation
Sets or resets control input 1.		
Control Input 2 to 32	No Operation	Set / Reset / No Operation
Sets or resets control inputs 2 to 32 individually.		

The "CTRL I/P CONFIG" column is visible when the "Control I/P Config" setting ("Configuration" column) = "visible".

Menu Text	Default Setting	Available Setting
CTRL I/P CONFIG.		
Hotkey Enabled	11111111111111111111111111111111	
Setting to allow the control inputs to be individually assigned to the "Hotkey" menu by setting '1' in the appropriate bit in the "Hotkey Enabled" cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the "CONTROL INPUTS" column.		
Control Input 1	Latched	Latched, Pulsed
Configures the control inputs as either 'latched' or 'pulsed'. A latched control input will remain in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input, however, will remain energized for 10ms after the set command is given and will then reset automatically (i.e. no reset command required).		
Ctrl Command 1	Set/Reset	Set/Reset, In/Out, Enabled/Disabled, On/Off
Allows the SET / RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as "ON / OFF", "IN / OUT" etc.		

Menu Text	Default Setting	Available Setting
CTRL I/P CONFIG.		
Control Input 2 to 32	Latched	Latched, Pulsed
Configures the control inputs as either ‘latched’ or ‘pulsed’.		
Ctrl Command 2 to 32	Set/Reset	Set/Reset, In/Out, Enabled/Disabled, On/Off
Allows the SET / RESET text to be changed to “ON / OFF”, “IN / OUT” etc.		

The “CTRL I/P Labels” column is visible when the “Control I/P Labels” setting (“Configuration” column) = “visible”.

Menu Text	Default Setting	Setting Range	Step Size
CTRL I/P LABELS			
Control Input 1	Control Input 1	16 Character Text	
Setting to change the text associated with each individual control input. This text will be displayed when a control input is accessed by the hotkey menu, or it can be displayed in the programmable scheme logic.			
Control Input 2 to 32	Control Input 2 to 32	16 Character Text	
As “Control input 1” for control inputs 2 to 32.			

3.11 InterMiCOM Teleprotection (P442/P444 only, “InterMiCOM comms” and “InterMiCOM conf” menus)

3.11.1 InterMiCOM communication channel

The “INTERMICOM COMMS” column contains all the information to configure the communication channel and also contains the channel statistics and diagnostic facilities.

Menu Text	Default Setting	Setting Range		Step Size
		Min	Max	
INTERMICOM COMMS				
IM Output Status	00000000			
IM Input Status	00000000			
The two cells display the InterMiCOM input and Output status.				
Source Address	1	1	10	1
Received Address	2	1	10	1
The “source” and “receive” addresses are used to synchronize remote and local relays. Both relays must be programmed with a unique pair of addresses that correspond with each other in the “Source Address” and “Receive Address” cells.				
Baud Rate	9600	600 / 1200 / 2400 / 4800 / 9600 / 19200		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set at the same speed setting.				
Ch Statistics	Invisible	Invisible / Visible		
Activates or hides the channel statistics. When visible is selected, the following menus are displayed. Otherwise, next menu is “Ch Diagnostics”.				

Menu Text	Default Setting	Setting Range		Step Size
		Min	Max	
INTERMICOM COMMS				
Rx Direct count	Data			
Number of Permissive Tripping messages received with the correct message structure.				
Rx Block Count	Data			
Number of Blocking messages received with the correct message structure.				
Rx Newdata count	Data			
Number of different messages received.				
Rx Errored count	Data			
Number of incomplete or incorrectly formatted messages received.				
Lost Messages	Data			
Number of messages lost within the previous time period set in “Alarm Window” cell.				
Elapsed Time	Data			
Time in seconds since the InterMiCOM channel statistics were reset.				
Reset Statistics	No	No / Yes		
Reset channel statistics command.				
Ch Diagnostics	Invisible	Invisible / Visible		
Activates or hides the channel diagnostics. When visible is selected, the following menus are displayed. Otherwise, next menu is “loopback mode”.				
Data CD Status	OK / Fail / Absent / Unavailable			
Indicates when the “Data Carrier Detect” (DCD) line (pin 1) is energised. OK = DCD is energised, FAIL = DCD is de-energised, Absent = InterMiCOM board is not fitted, Unavailable = hardware error present.				
FrameSync Status	OK / Fail / Absent / Unavailable			
Indicates when the message structure and synchronisation is valid. OK = valid message structure and synchronisation, FAIL = synchronisation has been lost, Absent = InterMiCOM board is not fitted, Unavailable = hardware error present.				
Message Status	OK / Fail / Absent / Unavailable			
Indicates when the percentage of received valid messages has fallen below the “IM Msg Alarm Lvl” setting within the alarm time period. OK = acceptable ratio of lost messages, FAIL = unacceptable ratio of lost messages, Absent = InterMiCOM board is not fitted, Unavailable = hardware error present.				
Channel Status	OK / Fail / Absent / Unavailable			
Indicates the state of the InterMiCOM communication channel. OK = channel healthy, FAIL = channel failure, Absent = InterMiCOM board is not fitted, Unavailable = hardware error present.				
IM H/W Status	OK / Fail / Absent / Unavailable			
Indicates the state of the InterMiCOM hardware OK = InterMiCOM hardware healthy, Read Error = InterMiCOM hardware failure, Write Error = InterMiCOM hardware failure, Absent = InterMiCOM board is either not fitted or failed to initialise.				

Menu Text	Default Setting	Setting Range		Step Size
		Min	Max	
INTERMICOM COMMS				
Loopback Mode	Disabled	Disabled / Internal / External		
By selecting “Loopback Mode” to “Internal”, only the internal software of the relay is checked whereas “External” will check both the software and hardware used by InterMiCOM (In the latter case, it is necessary to connect the transmit and receive pins together and ensure that the DCD signal is held high).				
Test pattern	11111111	00000000	11111111	-
A test pattern can be entered which is then transmitted through the software and/or hardware.				
Loopback Status				
Providing all connections are correct and the software is working correctly, the “Loopback Status” cell will display “OK”. An unsuccessful test would be indicated by “FAIL”, whereas a hardware error will be indicated by “UNAVAILABLE”.				

3.11.2 InterMiCOM configuration

The “INTERMICOM CONF” column selects the format of each signal and its fallback operation mode.

InterMiCOM provides 8 commands over a single communications link, with the mode of operation of each command being individually selectable within the “IM# Cmd Type” cell (# = 1 to 8).

Menu Text	Default Setting	Setting Range		Step Size
		Min	Max	
INTERMICOM CONF				
IM Msg Alarm Lvl	25%	0%	100%	1%
The “IM ¨Msg Alam Lvl” sets the level of invalid messages received compared to the total number of messages that should have been received. If this value exceeds the selected level, an alarm will be raised.				
IM1 Cmd Type	Blocking	Disabled/ Blocking/ Direct		
“Blocking” mode provides the fastest signalling speed (available on commands 1 – 4), “Direct Intertrip” mode provides the most secure signalling (available on commands 1 – 8) and “Permissive” mode provides the most dependable signalling (available on commands 5 – 8). Each command can be disabled so that it has no effect in the logic of the relay.				
IM1 Fallback Mode	Default	Default/ Latched		
Visible if “IM1 Cmd type” ≠ “Disabled” When “Latched”, during periods of extreme where the synchronization of a message structure is lost or is cannot be decoded, the last good command can be maintained until a new valid message is received. When “Default”: if the synchronisation is lost, after a time period, a known fallback state can be assigned to the command. In this latter case, the time period will need to be set in the “IM# FrameSynTim” cell and the default value will need to be set in “IM# DefaultValue” cell. As soon as a full valid message is seen by the relay all the timer periods are reset and the new valid command states are used. An alarm is provided if the noise on the channel becomes excessive.				
IM1 DefaultValue	1	0	1	1

Menu Text	Default Setting	Setting Range		Step Size
		Min	Max	
INTERMICOM CONF				
Visible if “IM1 Fallback Mode” = “Default”. Sets the default value to assign to the command after a time period.				
IM1 FrameSyncTim	20ms	10ms	1500ms	10ms
Visible if “IM1 Fallback Mode” = “Default”. Sets the time period to assign the known default value to the relay.				
IM2 to IM4	*(Cells as for IM1 above)*			
IM5 Cmd Type	Direct	Disabled/ Permissive/ Direct		
IM5 Fallback Mode	Default	Default/ Latched		
IM5 DefaultValue	0	0	1	1
IM5 FrameSyncTim	10ms	10ms	1500ms	10ms
IM6 to IM8	*(Cells as for IM5 above)*			
As IM1 Cmd Type. Note: Setting choices ere diffrent from IM2 to IM8 (see IM1 Cmd type). When Cmd Type is enabled, Fallback Mode is enabled. Default values and frameSync type are settable when fallback mode selection is “latched”.				

3.12 Programmable function keys and tricolour LEDs (“Function key” menu)

The lock setting allows a function key output that is set to toggle mode to be locked in its current active state. In toggle mode a single key press will set/latch the function key output as high or low in programmable scheme logic. This feature can be used to enable/disable relay functions. In the normal mode the function key output will remain high as long as the key is pressed. The Fn. Key label allows the text of the function key to be changed to something more suitable for the application.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
FUNCTION KEYS				
Fn. Key Status	0000000000			
Displays the status of each function key.				
Fn. Key 1 Status	Unlocked	Disabled, Locked, Unlocked		
Setting to activate function key. The ‘Lock’ setting allows a function key output that is set to toggle mode to be locked in its current active state.				
Fn. Key 1 Mode	Toggled	Toggled, Normal		
Sets the function key in toggle or normal mode. In ‘Toggle’ mode, a single key press will set/latch the function key output as ‘high’ or ‘low’ in programmable scheme logic. This feature can be used to enable/disable relay functions. In the ‘Normal’ mode the function key output will remain ‘high’ as long as key is pressed.				
Fn. Key 1 Label	Function Key 1			
Allows the text of the function key to be changed to something more suitable for the application.				
Fn. Key 2 to 10 Status	Unlocked	Disabled, Locked, Unlocked		
Setting to activate function key (see “Fn. Key 1 Status”).				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
FUNCTION KEYS				
Fn. Key 2 to 10 Mode	Toggled	Toggled, Normal		
Sets the function key in toggle or normal mode (see “Fn. Key 1 mode”).				
Fn. Key 2 to 10 Label	Function Key 2 to 10			
Allows the text of the function key to be changed.				

3.13 Ethernet NCIT (IEC 61850-9-2 Etherne board option only)

The IEC 61850-9-2 board must be configured to the system and application by means of appropriate settings. The sequence in which the settings are listed and described in this section will be the “ETHERNET NCIT” submenu in the IED submenu.

Refer to the Px4x/EN 9-2 user guide documentation for complete setting information.

Menu Text	Default Setting	Available Settings
ETHERNET NCIT		
Physical Link	Copper	Copper / Fibre Optic
This cell defines whether an electrical connection (“Copper” selection) or fiber optic connection is being used for communication.		
AntiAlias Filter	Disabled	Disabled / Enabled
This cell activates or deactivates the anti-aliasing filter.		
Merge unit Delay	0 s	0 to 3.000ms, in steps of 250.0µs
This cell adjusts the maximum time-delay starting at the reception of the Ethernet message from the “first” Merging Units (MU) to the reception of the Ethernet message from the “last” Merging Units (MU). This time-delay should be adjusted to receive the messages from all the MUs on time. The signal processing will start at the end of the Merge Unit delay. If a message is not received in that specified time, a synchronisation alarm will appear.		
LN Arrangement	VL,IL,IN	VL,IL,IN / VL,IL,IN2 / VL,IL,IN,VB/ VL,IL,IN2,VB / VL,IL,IN2,IN,VB VL,Sum(2xIL) / VL,IL,IN,2×VB VL,IL,IN2,2×VB’
This cell is used to select the logical node arrangement.		
LN1 Name	MiCOM Logical Node 1	
LN2 Name	MiCOM Logical Node 2	
LN3 Name	MiCOM Logical Node 3	
LN4 Name	MiCOM Logical Node 4	
Name of the Logical Nodes LN1 to LN4, to identify it (up to 34 characters). Note: It is important for each Logical Node name to be exactly the same as the one set in the Merging Unit that broadcasts it.		
Synchro Alarm	No Sync clk	‘No Sync clk’ / ‘Global 1 PPS’ / ‘Local 1 PPS’
Lost of the synchronization alarm in accordance with the following values. ‘Global 1 PPS’ = the Sample Values (SV) are synchronized with a global area clock (GPS like clock). ‘Local 1 PPS’ = the SV are synchronized with a local area clock signal (substation). No Sync clk’ = the SV are not synchronized with an external clock signal (internal synchronization).		

3.14 "IED configurator" column (P442 / P444 only)

The contents of the IED CONFIGURATOR column (for IEC 61850 configuration) are mostly data cells, displayed for information but not editable. to edit the configuration, it is necessary to use the IED (Intelligent Electronic Device) configurator tool within MiCOM S1 Agile.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
IED CONFIGURATOR				
Switch Conf.Bank	No Action	No Action, Switch Banks		
Setting which allows the user to switch between the current configuration, held in the Active Memory Bank (and partly displayed below), to the configuration sent to and held in the Inactive Memory Bank.				
Restore MCL	No action	No action / Restore MCL		
Used to restore data from MCL binary file. MCL (MiCOM Configuration Language) files are specific, containing a single devices IEC61850 configuration information, and used for transferring data to/from the MiCOM IED.				
Active Conf.Name	Data			
The name of the configuration in the Active Memory Bank, usually taken from the SCL file.				
Active Conf.Rev	Data			
Configuration Revision number of the Active Memory Bank, used for version management.				
Inact.Conf.Name	Data			
The name of the configuration in the Inactive Memory Bank, usually taken from the SCL file.				
Inact.Conf.Rev	Data			
Configuration Revision number of the Inactive Memory Bank, used for version management.				
IP PARAMETERS				
IP Address	Data			
Displays the unique network IP address that identifies the relay.				
Subnet Mask	Data			
Displays the sub-network that the relay is connected to.				
Gateway	Data			
Displays the IP address of the gateway (proxy) that the relay is connected to.				
SNTP PARAMETERS				
SNTP Server 1	Data			
Displays the IP address of the primary SNTP server.				
SNTP Server 2	Data			
Displays the IP address of the secondary SNTP server.				
IEC61850 SCL				
IED Name	Data			
8 character IED name, which is the unique name on the IEC 61850 network for the IED, usually taken from the SCL (Substation Configuration Language for XML) file.				
IEC61850 GOOSE				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
IED CONFIGURATOR				
GoEna	00000000	00000000	11111111	1
GoEna (GOose ENAble) is a setting to enable GOOSE (Generic Object Orientated Substation Event, for high-speed inter-device messaging) publisher settings. This setting enables (“1”) or disables (“0”) GOOSE control blocks from 08 (first digit) to 01 (last digit).				
Test Mode	00000000	00000000	11111111	1
The Test Mode cell allows the test pattern to be sent in the GOOSE message, for example for testing or commissioning. The setting enables (“1”) or disables (“0”) test mode for GOOSE control block from 08 (first digit) to 01 (last digit). Once testing is complete the cell must be set back to ‘Disabled’ to restore the GOOSE scheme back to normal service.				
Ignore Test Flag	No	No, Yes		
When set to ‘Yes’, the test flag in the subscribed GOOSE message is ignored, and the data treated as normal.				

3.15 Supervision (“Supervision” menu)

The “Supervision” menu contains 3 sections:

- the Voltage Transformer Supervision (VTS) section, for analog ac voltage inputs failures supervision,
- the Current Transformer Supervision (CTS) section, for ac phase current inputs failures supervision,
- the Capacitive Voltage Transformer Supervision (CVT) section, for voltage dividers capacitors supervision.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
SUPERVISION – GROUP 1				
VT Supervision – Group 1				
VTS Time Delay	5.00 s	1.00 s	20.00 s	1.00 s
The VTS function issues an alarm signal when the Voltage Transformer is lost, when the VTS time-delay has elapsed. If an opto input is used to detect a VT failure, the blocking protection is instantaneous.				
VTS I2 & I0 Inh	50.00 mA	0.00 A	1.00 A	10 mA
Sets negative sequence current and zero sequence current thresholds. If negative sequence and zero sequence currents exceed the threshold, the VTS alarm is inhibited (see section “Supervision / Loss of one or two phases voltages” below – P44x/EN AP).				
Detect 3P	Disabled	Enabled / Disabled		
Disables or enables the loss of the three phase voltages.				
Threshold 3P	30.00 V	10.00 V	70.00 V	1.00 V
Sets the phase voltage level.				
Delta I>	100.0 mA			

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
SUPERVISION – GROUP 1				
Sets the sensitivity of the superimposed current elements.				
CT Supervision – Group 1				
CTS Status	Disabled	Enabled / Disabled		
Enables or disables the Circuit Transformer Supervision.				
CTS VN< Inhibit	1	0.5 / 2V	22 / 88V	0.5 / 2 V
Sets the VN< inhibition threshold. The CTS alarm is inhibited if the residual voltage is lower than this value.				
CTS IN> Set	0.1	0.08 × In	4 × In	0.01 × In
Sets the residual current threshold.				
CTS Time Delay	5	0s	10s	1s
Sets the time delay alarm.				
CVT Supervision – Group 1				
CVTS Status	Disabled	Enabled / Disabled		
Enables or disables the capacitive voltage transformers supervision.				
CVTS VN>	1V	0.5V	22V	0.5V
Sets the residual overvoltage threshold. A CVTS alarm is sent out if residual voltage is greater than this value.				
CVTS Time Delay	100s	0s	300s	0.01s
Sets the CVTS time delay alarm.				
CVTS V2 Status	Disabled	Enabled / Disabled		
This setting is to enable the citeria of the negative sequence voltage control.				
CVTS V2>	1V	0.5V	22V	0.5V
Sets the negative sequence voltage threshold. A CVTS alarm is sent out providing *CVTS V2 Status* is enabled and the negative sequence voltage is greater than this value.				

3.16 Check synchronisation (“System check” menu)

The SYSTEM CHECKS menu contains all of the check synchronism settings for auto (“A/R”) and manual (“Man”) reclosure and is shown in the table below along with the relevant default settings:

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – SYSTEM CHECK				
C/S Check Scheme for A/R	111	Bit 0 (last bit): Live Bus / Dead Line, Bit 1: Dead Bus / Live Line, Bit 2 (first bit): Live Bus / Live Line.		
Check synchronism scheme for Autoreclosure. At least, one condition must be selected to activate the synchronism check logic. The Dead Bus / Dead Line can only be created using PSL.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – SYSTEM CHECK				
C/S Check Scheme for Man CB	111	Bit 0: Live Bus / Dead Line, Bit 1: Dead Bus / Live Line, Bit 2: Live Bus / Live Line.		
Check synchronism scheme for Manual CB Closure. At least, one condition must be selected to activate the synchronism check logic. The Dead Bus / Dead Line can only be created using PSL. The check synchronism condition is only taken into account if a SOTF condition has been enabled. Otherwise, a dedicated PSL can be created using DDB (live line or live bus/dead line) – live/live cannot be managed – in that case.				
V< Dead Line	13V	5V	30V	1V
V> Live Line	32V	30V	120V	1V
V< Dead Bus	13V	5V	30V	1V
V> Live Bus	32V	30V	120V	1V
The Live Line and Dead Line settings define the thresholds which dictate whether or not the line or bus is determined as being live or dead by the relay logic.				
Diff Voltage	6.5V	0.5V	40V	0.1V
Differential voltage between Line VT and Busbar VT measurements.				
Diff Frequency	0.05Hz	0.02Hz	1Hz	0.01Hz
Differential frequency between Line VT and Busbar VT measurements.				
Diff Phase	20°	5°	90°	2.5°
Differential voltage between Line VT and Busbar VT measurements.				
Bus-Line Delay	0.2s	0.1s	2s	0.1s
Bus Line time delay: The Check synchronism is not verified when 'V> Live Bus', 'V> Live Line', 'Diff Voltage', 'Diff Frequency' or 'Diff Phase' threshold is exceeded for longer than 'Bus-Line delay' time-delay.				

3.17 Autorecloser ("autoreclose" menu)

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – AUTORECLOSE				
The '**A/R TPAR Enable**' or '**A/R SPAR Enable**' opto inputs (assigned in the PSL) have priority and enables or disables the single or three poles autoreclose function. Otherwise, set '**A/R Single Pole**' and '**A/R Three pole**' ('**CB Control**' menu) to enable Autoreclose.				
AUTORECLOSE MODE				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – AUTORECLOSE				
1P Trip Mode	1	1 – Single 1/3 – Single/Three 1/3/3 – Single/Three/Three 1/3/3/3 – Single/Three/Three/Three		
Number of shots, single pole trip mode (displayed if “A/R single pole” is enabled (‘**CB Control**’ column)). This setting is enabled if the first fault is a single phase fault. The first shot is a single mode high speed autoreclose shot and, if the relay has been set to allow more than one reclose, then the second, third and fourth shots are converted to three-pole time-delayed autoreclose trips.				
3P Trip Mode	1	3 – Three 3/3 – Three/Three 3/3/3 – Three/Three/Three 3/3/3/3 – Three/Three/Three/Three		
Number of shots, three-pole trip mode (displayed if “A/R Three pole” is enabled (‘**CB Control**’ column)). This cell sets three-pole autoreclose shots. Up to four three-pole autoreclose shots are settable (1 high speed and three time-delayed autoreclose shots).				
1P - Dead Time 1	1s	0.1s	5s	0.01s
3P - Dead Time 1	1s	0.1s	60s	0.01s
Single-/ Three-pole dead time is displayed if “A/R single / Three pole” is enabled (‘**CB Control**’ column). This setting is enabled if the first fault is a multi phase fault. Dead Times 1 (1P or 3P) set the dead time for the first high speed shot of the single pole or three-pole reclosure.				
Dead Time 2	60s	1s	3600s	1s
Dead Time 3	180s	1s	3600s	1s
Dead Time 4	180s	1s	3600s	1s
Dead Times for second, 3rd and 4th shot (when set). The dead times are independently adjustable. The CB close signal is given at the end of this time-delay.				
Reclaim Time	180s	1s	600s	1s
Set the reclaim time. The reclaim time starts when the CB is closed. The reclaim time should be set according to the fault incidence, the CB spring charging time, the switchgear maintenance and the tZ2 zone delay.				
Reclose Time Delay	0.1s	0.1s	10s	0.1s
Set the time-delay before CB reclosure. The Reclose time-delay maintains the linked reclose contact closed for a time sufficient to ensure reliable CB mechanism operation				
Discrimination Time	5s	0.1s	5s	0.01s
The discrimination time-delay is used to differentiate between an evolving fault from a second fault in the power system and a long circuit breaker operation.				
A/R Inhibit Wind (CB healthy application)	5s	1s	3600s	1s
The "A/R Inhibit Wind" timer setting can be used to prevent autoreclose being initiated when the CB is manually closed onto a fault. Autoreclose is disabled for the AR Inhibit Wind following manual CB Closure.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1 – AUTORECLOSE				
C/S on 3P Rcl DT1	Enabled	Enabled, Disabled		
Check synchronism on 3-pole reclosure during Dead Time 1 Enables or disables the control by the check synchronism logic of the 3P high speed autoreclosure (HSAR) cycle during dead time 1 (check synchro 3P HSAR).				
AUTORECLOSE LOCKOUT				
Block A/R (Bit = 1 means autoreclose blocked)	1111 1111 1111 1111 1111 1111 1111 111	Bit 0: block at T2 Bit 1: block at T3 Bit 2: block at Tzp Bit 3: block for LoL Trip Bit 4: block for I>1 Trip Bit 5: block for I>2 Trip Bit 6: block for V<1 Trip Bit 7: block for V<2 Trip Bit 8: block for V>1 Trip Bit 9: block for V>2 trip Bit 10 (0A): block for IN>1 Trip Bit 11 (0B): block for IN>2 Trip Bit 12 (0C): block for Aided D.E.F Trip Bit 13 (0D): block for Zero. Seq. Power Trip Bit 14 (0E): block for IN>3 Trip Bit 15 (0F): block for IN>4 Trip Bit 16 (10): block for PAP Trip Bit 17 (11): block for Thermal Trip Bit 18 (12): block for I2>1 Trip Bit 19 (13): block for I2>2 Trip Bit 20 (14): block for I2>3 Trip Bit 21 (15): block for I2>4 Trip Bit 22 (16): block for VN>1 Trip Bit 23 (17): block for VN>2 Trip Bit 24 (18): block at Tzq Bit 25 (19): block for V<3 Trip Bit 26 (1A): block for V<4 Trip Bit 27 (1B): block for V>3 Trip Bit 28 (1C): block for V>4 trip Bit 29 (1D): block for I<1 Trip Bit 30 (1E): block for I<2 Trip		
Block A/R 2	111111	Bit 0: block for F<1 Trip Bit 1: block for F<2 Trip Bit 2: block for F<3 Trip Bit 3: block for F<4 Trip Bit 4: block for F>1 Trip Bit 5: block for F>2 Trip		
Set to 1 the relevant bit to block the autoreclose when the relevant fault occurs. It will cause a lockout if autoreclose is in progress.				

3.18 Security configuration (“SECURITY CONFIG” menu, if option avalable)

The SECURITY CONFIG column contains the main configuration settings for Security functions. This column is used to set the password attempts number and duration. When these limits expire, access to the interface is blocked until timer has expired. This setting enables or disables port access.

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
SECURITY CONFIG				
ACCESS ONLY FOR AUTHORISED USERS				
Attempts Limit	2	0	3	1
Adjust the number of attempts to enter a valid password. When the maximum number of attempts has been reached, access is blocked.				
Attempts Timer	2	1	3	1
Adjust the time limit (minutes) to enter the correct password.				
Blocking Timer	5	1	30	1
Adjust the blocking timer (minutes) after a password blocking. Once the password is blocked, this blocking timer is initiated. Only after the blocking timer has expired will access to the interface be unblocked, where on the attempts counter is reset to zero.				
Front Port	Enabled	Enabled or Disabled		
Enable or disable the front port access. A level 3 password is needed to perform this action. To prevent accidental disabling of a port, a warning message “FRONT PORT TO BE DISABLED, CONFIRM” is required to be disabled.				
Rear Port 1	Enabled	Enabled or Disabled		
Enable or disable the rear port 1 access. A level 3 password is needed to perform this action. To prevent accidental disabling of a port, a warning message “REAR PORT 1 TO BE DISABLED, CONFIRM” is required to be disabled.				
Rear Port 2	Enabled	Enabled or Disabled		
When fitted, enable or disable the rear port 2 access. A level 3 password is needed to perform this action. To prevent accidental disabling of a port, a warning message “REAR PORT 2 TO BE DISABLED, CONFIRM” is required to be disabled.				
Ethernet Port	Enabled	Enabled or Disabled		
When fitted, enable or disable the Ethernet port access. A level 3 password is needed to perform this action. To prevent accidental disabling of a port, a warning message “ETHERNET TO BE DISABLED, CONFIRM” is required to be disabled. **Caution: disabling the Ethernet port disables all Ethernet based communications.**				
Courier Tunnel	Enabled	Enabled or Disabled		
Enable or disable the Courier tunneling logical port access. A level 3 password is needed to perform this action. Note: if this protocol is enabled or disabled, the Ethernet card reboots.				
IEC61850	Enabled	Enabled or Disabled		
Enable or disable the IEC61850 logical port access. A level 3 password is needed to perform this action. Note: if this protocol is enabled or disabled, the Ethernet card reboots.				
DNP3 OE	Enabled	Enabled or Disabled		
Enable or disable the DNP3 logical port access. A level 3 password is needed to perform this action. Note: if this protocol is enabled or disabled, the Ethernet card reboots.				
Attempts Remain	Data			
Indicates the number of attempts to enter a password.				
Blk Time Remain	Data			
Indicates the blocking time remain (in minute).				

Menu Text	Default Setting	Setting Range		Step Size
		Min.	Max.	
Password Fallback Level	0	1	3	3
The 'fallback level' is the password level adopted by the relay after an inactivity timeout, or after the user logs out. This will be either the level of the highest level password that is blank, or level 0 if no passwords are blank.				
Security Code	Data			
Indicates the security code (user interface only). The security code is a 16-character string of upper case characters. It is a read-only parameter. The IED generates its own security code randomly. This Security Code should be noted for password recovery.				

3.19 "PSL Timers" configuration.

The "PSL Timers" menu sets the pick up or drop off time of a timer in the PSL (see P44x/EN PL). This menu allows setting or changes using HMI.

Menu Text	Default Setting	Setting Range		Step Size
PSL Timers				
Timer 1	10ms	1ms	14400s	1ms
Set the first pick-up or Drop-off time of a timer in the PSL. When the "PSL timers" menu is not used to set the PSL, this value can be set using the "Pickup/Drop-off value (ms)" (timer properties) in the PSL. When Timer is set using this menu, the "Allow changes in setting menu" option box is ticked. The "Available timers" window.				
Timer 2 to 32	10ms	1ms	14400s	1ms
As "Timer 1" for timers 2 to 32.				

4 PROGRAMMABLE SCHEME LOGIC DEFAULT SETTINGS

The relay includes Programmable Scheme Logic (PSL) - one PSL by Group of settings enabled (maximum 4 groups of PSL Logic can be assigned in the relay).

The purpose of this logic is multi-functional and includes the following:

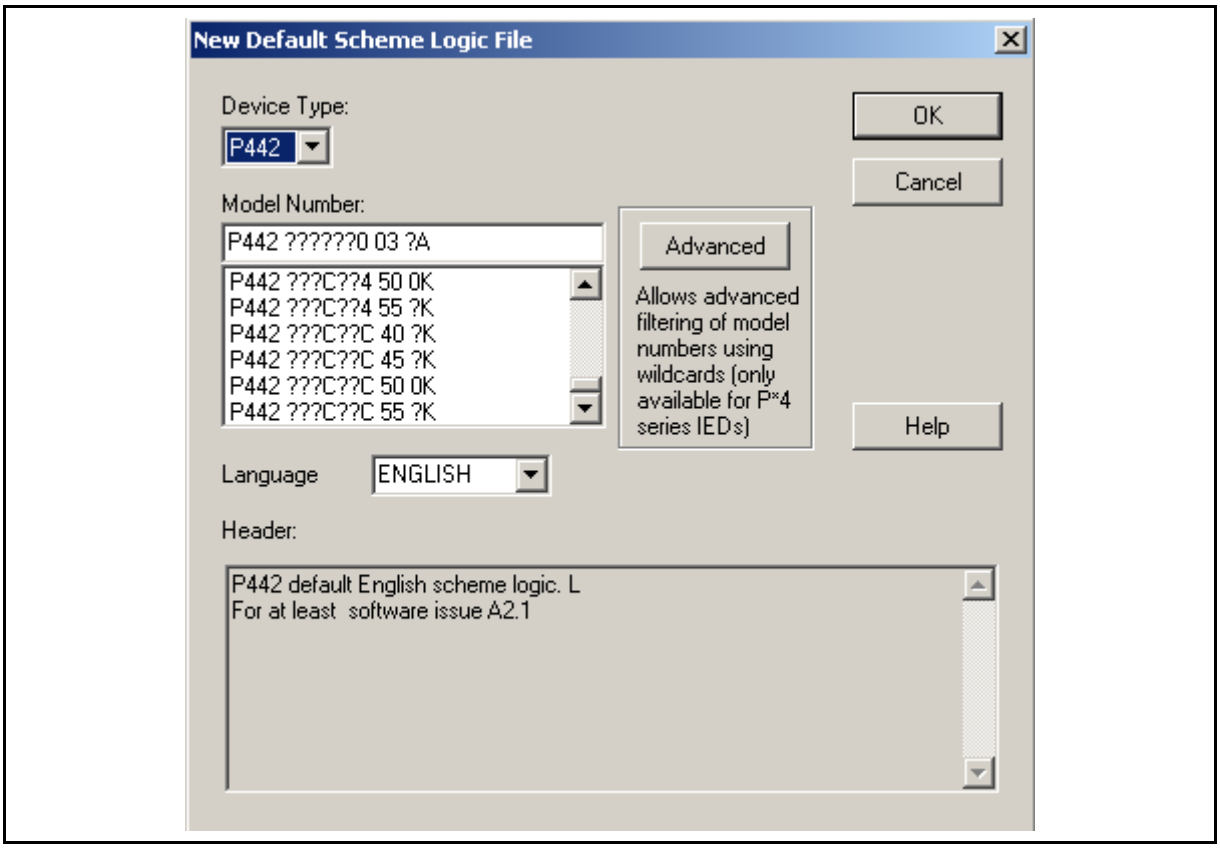
- Mapping of opto-isolated inputs, relay output contacts and the programmable LEDs.
- Relay output conditioning (delay on pick-up/drop-off, dwell time, latching or self-reset).
- Fault Recorder start mapping, i.e. which internal signals initiate a fault record.
- Generation of customer specific scheme logic through the use of the PSL Editor inbuilt into the MiCOM S1 Agile support software (Section P44x/EN PL).

Further information regarding editing and using PSL can be found in the MiCOM S1 Editor help menu. The following section details the default settings of the PSL. Note that changes to these default settings can only be carried out using the PSL Editor and not via the relay front panel.

4.1 How to use the PSL Editor

Off-Line method:

- Launch the free application software (PSL Editor Application or, using MiCOM S1 Agile, “Tools > PSL Editor” menu) provided with the relay: MiCOM S1 Agile (also downloadable from the internet).
- Launch the PSL Editor application.
- Open a blank scheme or a default scheme with the correct model / version number (File\New\Default Scheme or Blank Scheme).



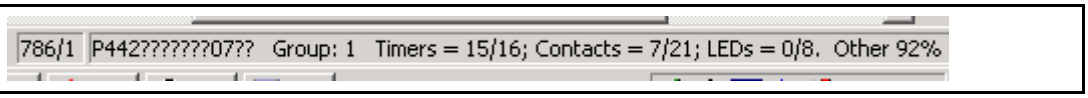
Select the relay type and model number (software version is displayed for compatibility)

On-Line method:

- Communication with the relay can be started (Device \ open connection \ address1 \ pword AAAA) and the PSL activated in the internal logic of the relay can be extracted, displayed, modified and uploaded again to the relay.
- Any group from 1 to 4 can be modified (ref of group must be validated before resenting the file from PC to relay)

Before creating a dedicated PSL for covering customised applications, please see the DDB description cell by cell (set & reset conditions) in the table at the end of the technical guide (Courier Database).

The type of model used by the relay in the settings or in the PSL is displayed at the bottom of the screen in the status bar:



It indicates:

- Model number used (last 2 digits:???07??)
- PSL activated for Group1 logic
- Number of timers still available (15 out of a total of 16)
- Number of contacts still available (7 out of a total of 21 for P442 model)
- Number of LEDs still available (0 to 8 if all already assigned in the PSL)
- Memory capacity still available (decreases with the numbers of cells and logic gates linked in the dedicated PSL)

(See also the section Commissioning document for further information on the tools)

4.2 Logic input mapping

The default mapping for each of the opto-isolated inputs are as shown in the following table:

- Version A: Opto inputs are in 48 VDC polarised (can be energised with the internal field voltage offered by the relay
- Version B: Opto inputs are universal and opto input range can be selected in MiCOM S1 Agile by:

Opto A – 48 VDC:

The opto inputs are specified to operate between 30 and 60 V to ensure there is enough current flowing through the optocoupler diode to guarantee operation with component tolerances, temperature and CTR (Current Transfer Ratio) downgrading over time.

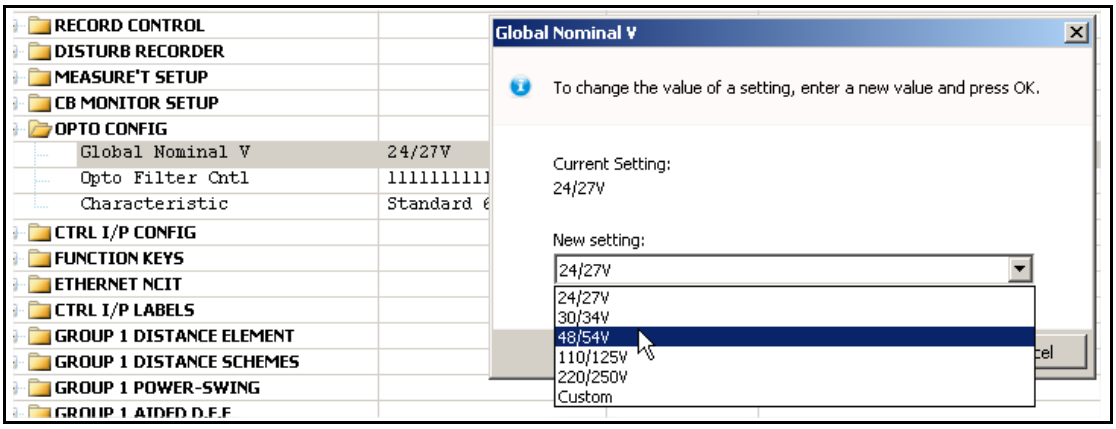
Between 13-29 V lies the uncertainty band.

Below 12 V, the guaranteed logic state is Off

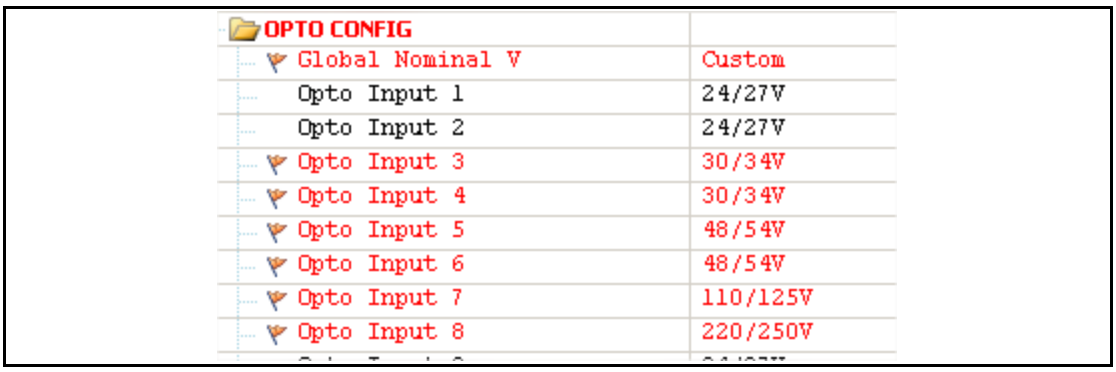
Opto B – Universal opto inputs:

Setting	Guaranteed No Operation	Guaranteed Operation
24/27	<16,2	>19,2
30/34	<20,4	>24,0
48/54	<32,4	>38,4
110/125	<75,0	>88,0
220/250	<150	>176,0

These margins ensure that ground faults on substation batteries do not cause maloperation of the opto inputs.



Or “Custom” can be selected in the menu to set a different voltage pick-up for any opto inputs:



The default mappings for each of the inputs are shown in section P44x/EN PL.

4.3 Relay output contact mapping

The default mappings and conditioning for each of the relay output contacts are shown in the following table (PSL are equivalent for 442/444):

Relay Contact N°	P442 Relay	P444 Relay
1	TripA+B+C & Z1 [straight]	TripA+B+C & Z1 [straight]
2	Any Trip Phase A [straight]	Any Trip Phase A [straight]
3	Any Trip Phase B [straight]	Any Trip Phase B [straight]
4	Any Trip Phase C [straight]	Any Trip Phase C [straight]
5	Signal send (Dist. or DEF) [straight]	Signal send (Dist. or DEF) [straight]
6	Any Protection Start [straight]	Any Protection Start [straight]
7	Any Trip [straight]	Any Trip [straight]
8	General Alarm [straight]	General Alarm [straight]
9	DEF A+B+C Trip + IN>1Trip + IN>2Trip [straight]	DEF A+B+C Trip + IN>1Trip + IN>2Trip [straight]
10	Dist. Trip &Any Zone&DistUnb CR [straight]	Dist. Trip &Any Zone&DistUnb CR [straight]
11	Autoreclose lockout [straight]	Autoreclose lockout [straight]
12	Autoreclose 1P+3P cycle in progress [straight]	Autoreclose 1P+3P cycle in progress [straight]

Relay Contact N°	P442 Relay	P444 Relay
13	A/R Close [straight]	A/R Close [straight]
14	Power Swing Detected [straight]	Power Swing Detected [straight]
15	Not allocated	Not allocated
16	Not allocated	Not allocated
17	Not allocated	Not allocated
18	Not allocated	Not allocated
19	Not allocated	Not allocated
20	Not allocated	Not allocated
21	Not allocated	Not allocated
22	Not allocated	Not allocated
23		Not allocated
24		Not allocated
25		Not allocated
26		Not allocated
27		Not allocated
28		Not allocated
29		Not allocated
30		Not allocated
31		Not allocated
32		Not allocated

Note that when 3-pole tripping is selected in the relay's menu, all trip contacts: Trip A, Trip B, Trip C, and Any Trip close simultaneously.

Note: Other relay logic conditions are available in the PSL relay design:
– Pulse Timer
– Pick UP/Drop Off Timer
– Dwell Timer
– Pick Up Timer
– Drop Off Timer
– Latching
– Straight (Transparent)

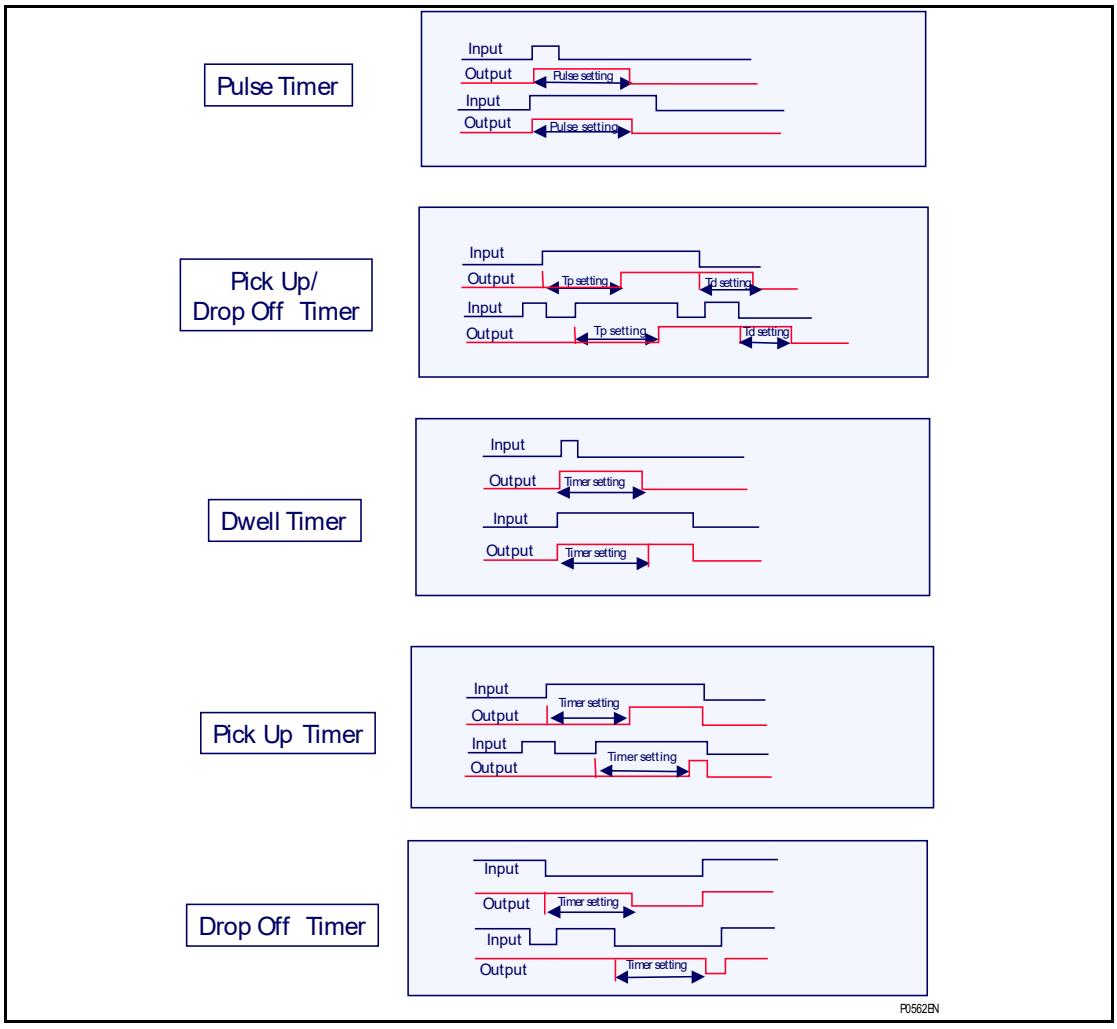


Figure 2 – Time-delay definition in psl

4.4 Programmable LED output mapping

The default mappings for each of the programmable LEDs are as shown in the following table:

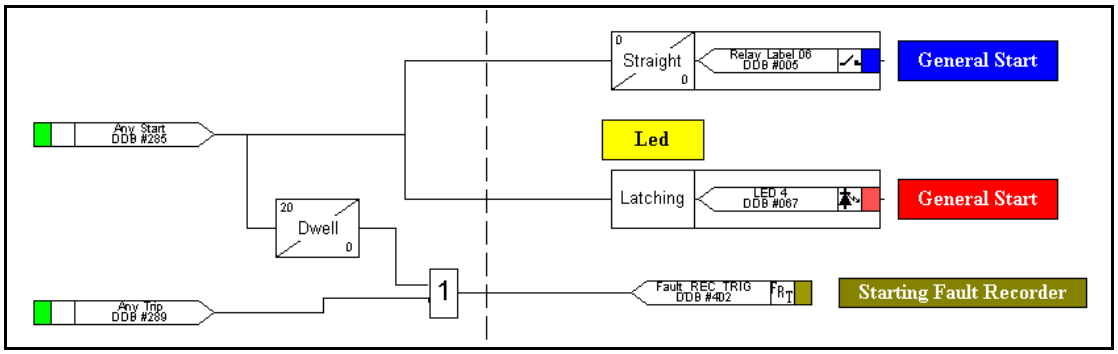
LED No.	P442 Relay	P444 Relay
1	Any Trip A	Any Trip A
2	Any Trip B	Any Trip B
3	Any Trip C	Any Trip C
4	Any Start	Any Start
5	Z1+Aided Trip	Z1+Aided Trip
6	Dist Fwd	Dist Fwd
7	Dist Rev	Dist Rev
8	A/R Enable	A/R Enable

Note: All the LEDs are latched in the default PSL

4.5 Fault recorder trigger

The default PSL trigger which initiates a fault record is shown in the following table:

P442 Relay	P444 Relay
Any Start	Any Start
Any Trip	Any Trip



If the fault recorder trigger is not assigned in the PSL, no Fault recorder can be initiated and displayed in the list by the LCD front panel.

5 CURRENT TRANSFORMER REQUIREMENTS

Two calculations must be performed – one for the three phase fault current at the zone 1 reach, and one for earth (ground) faults. The higher of the two calculated Vk voltages must be used:

5.1 CT Knee Point Voltage for Phase Fault Distance Protection

$Vk \geq K_{RPA} \times I_{F\,Z1} \times (1+ X/R) . (R_{CT} + R_L)$

Where:

Vk = Required CT knee point voltage (volts),

K_{RPA} = Fixed dimensioning factor = always **0.6**

$I_{F\,Z1}$ = Max. secondary phase fault current at Zone 1 reach point (A),

X/R = Primary system reactance / resistance ratio,

R_{CT} = CT secondary winding resistance (Ω),

R_L = Single lead resistance from CT to relay (Ω).

5.2 CT Knee Point Voltage for Earth Fault Distance Protection

$Vk \geq K_{RPA} \times I_{Fe\,Z1} \times (1+ Xe/Re) . (R_{CT} + 2R_L)$

Where:

K_{RPA} = Fixed dimensioning factor = always **0.6**

$I_{Fe\,Z1}$ = Max. secondary earth fault current at Zone 1 reach point (A),

Xe/Re = Primary system reactance / resistance ratio for earth loop.

5.3 Recommended CT classes (British and IEC)

Class X current transformers with a knee point voltage greater than or equal to the calculated one can be used.

Class 5P protection CTs can be used, noting that the equivalent knee point voltage they offer can be approximated from:

$Vk = (VA \times ALF) / In + (R_{CT} \times ALF \times In)$

Where:

VA = Volt-ampere load rating,

ALF = Accuracy Limit Factor,

In = CT nominal secondary current.

5.4 Determining Vk for an IEEE “C" class CT

Where American/IEEE standards are used to specify CTs, the C class voltage rating can be checked to determine the equivalent Vk (knee point voltage according to the IEC). The equivalence formula is:

$Vk = [\text{ (C rating in volts) } \times 1.05] + [\ 100 \times R_{CT}]$

APPLICATION NOTES

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1 INTRODUCTION

1.1 Protection of overhead lines and cable circuits

Overhead lines are amongst the most fault susceptible items of plant in a modern power system. It is therefore essential that the protection associated with them provide secure and reliable operation. For distribution systems, continuity of supply is of paramount importance. The majority of faults on overhead lines are transient or semi-permanent in nature, and multi-shot autoreclose cycles are commonly used in conjunction with instantaneous tripping elements to increase system availability. Therefore, high speed, fault clearance is often a fundamental requirement of any protection scheme on a distribution network. The protection requirements for sub-transmission and higher voltage systems must also take into account system stability. Where systems are not highly interconnected the use of single phase tripping and high speed autoreclosure is commonly used. This in turn dictates the need for high speed protection to reduce overall fault clearance times.

Underground cables are vulnerable to mechanical damage, such as disturbance by construction work or ground subsidence. Also, faults can be caused by ingress of ground moisture into the cable insulation, or its buried joints. Fast fault clearance is essential to limit extensive damage, and to avoid the risk of fire.

Many power systems use earthing arrangements designed to limit the passage of earth fault current. Methods such as resistance earthing make the detection of earth faults difficult. Special protection elements are often used to meet such onerous protection requirements.

Physical distance must also be taken into account. Overhead lines can be hundreds of kilometres in length. If high speed, discriminative protection is to be applied it is necessary to transfer information between the line ends. This puts the onus on the security of signalling equipment and on the protection in the event of loss of this signal. Therefore, backup protection is an important feature of any protection scheme. In the event of equipment failure, maybe of signalling equipment or switchgear, it is necessary to provide alternative forms of fault clearance. It is desirable to provide backup protection which can operate with minimum time delay and yet discriminate with the main protection and protection elsewhere on the system.

1.2 MiCOM distance relay

MiCOM relays are a range of products from GE Vernova. Using advanced numerical technology, MiCOM relays include devices designed for application to a wide range of power system plant such as motors, generators, feeders, overhead lines and cables.

Each relay is designed around a common hardware and software platform to achieve a high degree of commonality between products. One such product in the range is the series of distance relays. The relay series has been designed to cater for the protection of a wide range of overhead lines and underground cables from distribution to transmission voltage levels.

The relay also includes a comprehensive range of non-protection features to aid with power system diagnosis and fault analysis. All these features can be accessed remotely from one of the relays remote serial communications options.

1.2.1 Protection Features

The distance relays offer a comprehensive range of protection functions, for application to many overhead line and underground cable circuits. There are 3 separate models available, P441, P442 and P444. The P442 and P444 models can provide single and three pole tripping. The P441 model provides three pole tripping only. This manual is applicable just for P442 and P442 relays. The protection features of each model are summarised below:

- 21G/21P: Phase and earth fault distance protection, each with up to 6 independent zones of protection. Standard and customised signalling schemes are available to give fast fault clearance for the whole of the protected line or cable.
- Load Blinding (Load Avoidance) for both phase and ground distance elements
- 50/51: Instantaneous and time-delayed overcurrent protection - Four elements are available, with independent directional control for the 1st and 2nd element. The 3rd

element can be used for SOFT/TOR logic. The fourth element can be configured for stub bus protection in 1½ circuit breaker arrangements.

- 50N/51N: Instantaneous and time-delayed neutral overcurrent protection. Four elements are available.
- 67N: Directional earth fault protection (DEF) - This can be configured for channel aided protection, plus two elements are available for backup DEF.
- 67 / 46: Directional or non-directional negative sequence overcurrent protection - This element can provide backup protection for many unbalanced fault conditions.
- 32N: Maximum of Residual Power Protection - Zero sequence Power Protection This element provides protection against high resistance faults, cleared without using a communications channel.
- 27 / 59: Undervoltage and overvoltage protections - Four-stage, configurable as either phase to phase or phase to neutral measuring. Stage 1 may be selected as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT) and stage 2 is DT only.
- 37: Undercurrent Protection – this element consists of two independ stages protection, with two independent time-delay setting.
- 81U / 81O: Underfrequency and overfrequency protection – This element can provides a four-stage time-delayed underfrequency protection and two-stage time-delayed overfrequency protection.
- 49: Thermal overload Protection - with dual time constant. This element provides separate alarm and trip thresholds.
- 50 / 27: Switch on to fault (SOTF) and Trip On Reclose (TOR) protections - These settings enhance the protection applied for manual circuit breaker closure.
- 78 / 68: Power swing blocking - Selective blocking of distance protection zones ensures stability during the power swings experienced on sub-transmission and transmission systems (stable swing or Out of Step condition = loss of synchronism). The relay can differentiate between a stable power swing and a loss of synchronism (out-of-step).
- 85: Channel Aided schemes with basic schemes, Permissive Underreach (PUP) and Permissive Overreach (POP) transfer trip schemes and Blocking schemes.
- Weak infeed echo logic.
- Accelerated Trip features (Loss of Load – Zx extension).
- 46 BC: Broken conductor detection - To detect network faults such as open circuits, where a conductor may be broken but not in contact with another conductor or the earth.
- 50 BF: Circuit breaker failure protection - Generally set to backtrip upstream circuit breakers, should the circuit breaker at the protected terminal fail to trip. Two stages are provided.
- VTS: Voltage transformer supervision (VTS). - To detect VT fuse failures. This prevents maloperation of voltage dependent protection on AC voltage input failure.
- CTS: Current transformer supervision - To raise an alarm should one or more of the connections from the phase CTs become faulty.
- CVTS: Capacitive Voltage Transformer Supervision – to supervise voltage divider capacitors supervision when residual voltage is greater than the set value.

1.2.2 Non-Protection Features

The P442 and P444 relays have the following non-protection features:

- 79/25: Autoreclosure with Check synchronism - This permits up to 4 reclose shots, with voltage synchronism, differential voltage, live line/dead bus, and dead bus/live line interlocking available. Check synchronism is optional.
- Measurements - Selected measurement values polled at the line/cable terminal, available for display on the relay or accessed from the serial communications facility.

- Fault/Event/Disturbance Records - Available from the serial communications or on the relay display (fault and event records only).
- Distance to fault locator - Reading in km, miles or % of line length.
- Four Setting Groups - Independent setting groups to cater for alternative power system arrangements or customer specific applications.
- Remote Serial Communications - To allow remote access to the relays. The following communications protocols are supported: Courier, MODBUS, IEC 60870-5/103 and DNP3.
- Continuous Self Monitoring - Power on diagnostics and self checking routines to provide maximum relay reliability and availability.
- Circuit Breaker State Monitoring - Provides indication of any discrepancy between circuit breaker auxiliary contacts.
- Circuit Breaker Control - Opening and closing of the circuit breaker can be achieved either locally via the user interface / opto inputs, or remotely via serial communications.
- Circuit Breaker Condition Monitoring - Provides records / alarm outputs regarding the number of CB operations, sum of the interrupted current and the breaker operating time.
- Commissioning Test Facilities.

1.2.3 Additional Features for the P442 Relay Model

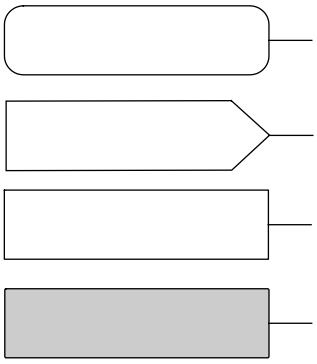
- Single pole tripping and autoreclose.
- Real Time Clock Synchronisation - Time synchronisation is possible from the relay IRIG-B input. (IRIG-B must be specified as an option).
- Fibre optic converter for IEC 60870-5/103 communication (optional).
- Second rear port in COURIER Protocol (KBus/RS232/RS485)
- 16 Logic Inputs - For monitoring of the circuit breaker and other plant status.
- Up to 21 Output relay contacts - For tripping, alarming, status indication and remote control.
- Communication protocols available (ordering specification): K-Bus/Courier, MODBUS, VDEW (IEC 60870-5-103), DNP3.0, IEC 61850 + Courier, IEC 61850 + IEC 60870-5-103) or DNP3.0 + Courier.

1.2.4 Additional Features for the P444 Relay Model

- Single pole tripping and autoreclose.
- Real Time Clock Synchronisation - Time synchronisation is possible from the relay IRIG-B input. (IRIG-B must be specified as an option).
- Fibre optic converter for IEC 60870-5/103 communication (optional).
- Second rear port in COURIER Protocol (KBus/RS232/RS485)
- 24 Logic Inputs - For monitoring of the circuit breaker and other plant status.
- Up to 46 output relay contacts (with 12 high break relays)- For tripping, alarming, status indication and remote control:
- Communication protocols available: K-Bus/Courier, MODBUS, VDEW (IEC 60870-5-103), DNP3.0, IEC 61850 + Courier, IEC 61850 + IEC 60870-5-103) or DNP3.0 + Courier.

1.3 Explanation about specific symbols used in the logic diagrams

The following specific symbols are used in the logic diagrams. General symbols are shown in section P44x/EN SG ‘Symbol and Glossary’:



Internal logic status from the logic of the protection (« the line is dead » or « the pole is dead »)

User setting, adjustment or selection (IHM or MiCOM S1 Agile)

Command / logical external status linked to an opto input from the protection, or logical output.

Digital Data Bus (DDB) within the Programmable Scheme Logic (PSL) corresponding to a command, a logical external status or a logical output.

Check the DDB table for the reference number of each cell, included in P44x/EN PL.

2 DISTANCE ALGORITHMS

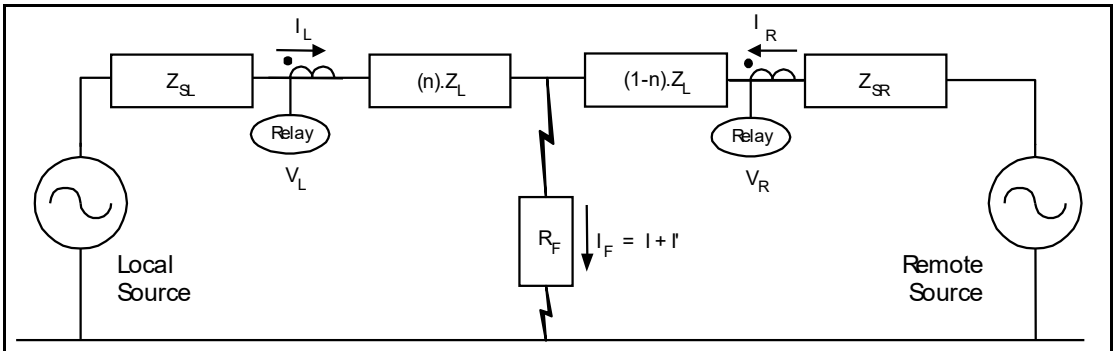
The operation is based on the combined use of two types of algorithms:

- "Delta" algorithms, also called High Speed algorithms, using the superimposed current and voltage values that are characteristic of a fault. These are used for phase selection and directional determination. The fault distance calculation is performed by the "impedance measurement algorithms" using Gauss-Seidel.
- "Conventional" algorithms using the impedance values measured while the fault occurs. These are also used for phase selection and directional determination. The fault distance calculation is performed by the "impedance measurement algorithms" using Gauss-Seidel.

The fastest algorithm gives the immediate directional decision.

2.1 Distance and Resistance Measurement

MiCOM P44x distance protection is a full scheme distance relay. To measure the distance and apparent resistance of a fault, the following equation is solved on the faulted loop:



$$V_L = (Z_L x I x D) + R_F x I_F$$
$$= ((r + jx) x I x D) + R_F x I_F \quad \text{where}$$

V_L = local terminal relay voltage
r = line resistance (ohm/mile)
x = line reactance (ohm/mile)
I_F = current flowing in the fault (I + I')
I = current measured by the relay on the faulty phase
= current flowing into the fault from local terminal
I' = current flowing into the fault from remote terminal
D = fault location (permile or km from relay to the fault)
R = fault resistance
R_F = apparent fault resistance at relay; R x (1 + I'/I)

Assumed Fault Currents:
For Phase to Ground Faults (ex., A-N), $I_F = 3I_0$ for 40ms, then I_A after 40 ms
For Phase to Phase Faults (ex., A-B), $I_F = I_{AB}$

P3030ENa

Figure 1: Distance and fault resistance estimation

The impedance measurements are used by High Speed and Conventional Algorithms.

The following describes how to solve the above equation (determination of D fault distance and R fault resistance). The line model used is the 3×3 matrix of the symmetrical line impedances (resistive and inductive) of the three phases, and mutual values between phases.

Raa + jω Laa	Rab + jω Lab	Rac + jω Lac
Rab + jω Lab	Rbb + jω Lbb	Rbc + jω Lbc
Rac + jω Lac	Rbc + jω Lbc	Rcc + jω Lcc

Where:

Raa=Rbb=Rcc and Rab=Rbc=Rac

$\omega Laa = \omega Lbb = \omega Lcc = \frac{2.x_1 + x_0}{3}$ and $\omega Lab = \omega Lbc = \omega Lac = \frac{x_0 + x_1}{3}$

and

X1: positive sequence reactance

X0: zero-sequence reactance

The line model is obtained from the positive and zero-sequence impedance. Four different residual compensation factor settings can be used on the relay, as follows:

kZ1: residual compensation factor used to calculate faults in zones 1 and 1X.

kZ2: residual compensation factor used to calculate faults in zone 2.

kZp: residual compensation factor used to calculate faults in zone p.

kZ3/4: residual compensation factor used to calculate faults in zones 3 and 4.

The solutions "Dfault" and "Rfault" solutions are obtained by solving the system of equations (one equation per step of the calculation) using the Gauss Seidel method.

$$\text{Rfault (n)} = \frac{\sum_{n0}^{n}(V_L.I_{fault}) - D_{fault}.(n-1).\sum_{n0}^{n}(Z_1.I_I.I_{fault})}{\sum_{n0}^{n}(I_{fault})^2}$$

$$\text{Dfault (n)} = \frac{\sum_{n0}^{n}(V_L.Z_1.I_I) - R_{fault}.(n-1).\sum_{n0}^{n}(Z_1.I_I.I_{fault})}{\sum_{n0}^{n}(Z_1.I_I)^2}$$

Rfault and Dfault are computed for every sample (24 samples per cycle).

Note: See also in § 2.3.1 the Rn and Dn (Xn) conditions of convergence.

With IL equal to Iα + k0 x 3I0 for phase-to-earth loop or IL equal to Iαβ for phase-to-phase loop.

2.1.1 Phase-to-earth loop impedance

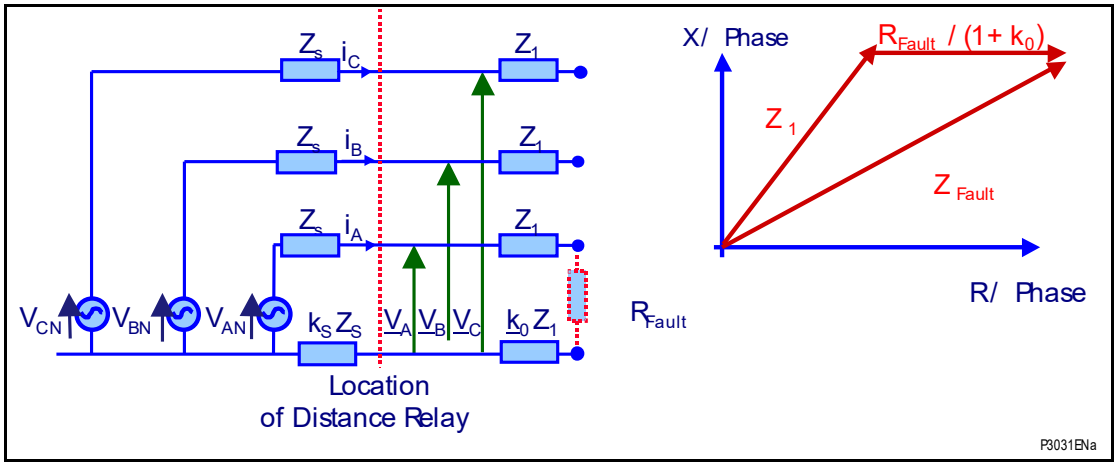


Figure 2: Phase-to-earth loop impedance

The impedance model for the phase-to-earth loop is:

$$V\alpha N = Z1 \times Dfault \times (I\alpha + k_0 \times 3I_0) + Rfault \times Ifault$$

with α = phase A, B or C

The ($3I_0$) current is used for the first 40 ms to model the fault current, therefore eliminating the load current before the circuit breakers are operated during the 40 ms (one pole tripping). After the 40 ms, the phase current is used.

$$V_{AN} = Z_1.Dfault.(I_A + k_0 \times 3I_0) + R_{fault}.I_{fault}$$

$$V_{BN} = Z_1.Dfault.(I_B + k_0 \times .3I_0) + R_{fault}.I_{fault}$$

$$V_{CN} = Z_1.Dfault.(I_C + k_0 \times 3I_0) + R_{fault}.I_{fault}$$

x 5 k_0 residual compensation factors

= 15 phase-to-earth loops are continuously monitored and computed for each samples.

$V_{\alpha N} = Z_1.D_{fault}.(I_\alpha + k0.3I0) + R_{fault}.I_{fault}$

$$V_{\alpha N} = Z_1.D_{fault}.(I_\alpha + Ia + \frac{Z_0 - Z_1}{3}.3I0 + R_{fault}.I_{fault}$$

$$V_{\alpha N} = (R_1+j.X_1).D_{fault}.(I_\alpha + \frac{R_0 - R_1 + (X_0 - X_1)}{3.(R_1 - jX_1)}.3I0) + R_{fault}.I_{fault}$$

$$V_{\alpha N} = (R_1+j.X_1).D_{fault}.I_\alpha + \frac{R_0 - R_1 + j(X_0 - X_1)}{3}.D_{fault}.3I0 + R_{fault}.I_{fault}$$

$$V_{\alpha N} = R_1.D_{fault}.I_\alpha + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + j.X1.\ D_{fault}.I_\alpha + j\frac{(X_0 - X_1)}{3}.D_{fault}.3I0 + R_{fault}.I_{fault}$$

$$V_{\alpha N} = R_1.D_{fault}.I_\alpha + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + j.X1.\ D_{fault}.I_\alpha + j\frac{(X_0 - X_1)}{3}.D_{fault}.(I_A+I_B+I_C) + R_{fault}.I_{fault}$$

$$V_{AN} = R_1.D_{fault}.I_A + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + \quad .D_{fault}.I_A + j\left(\frac{X_0 - X_1}{3}\right).D_{fault}.(I_B+I_C) + R_{fault}.I_{fault}$$

$$V_{AN} = R_1.D_{fault}.I_A + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + \left(\frac{X_0 + 2.X_1}{3}\right).D_{fault}.\frac{dI_A}{dt} + \left(\frac{X_0 + X_1}{3}\right).D_{fault}.\frac{dI_B}{dt} + \left(\frac{X_0 + X_1}{3}\right).D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault}$$

$$V_{AN} = R_1.D_{fault}.I_A + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + L_{AA}.D_{fault}.\frac{dI_A}{dt} + L_{AB}.D_{fault}.\frac{dI_B}{dt} + L_{AC}.D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault}$$

$$V_{BN} = R_1.D_{fault}.I_B + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + L_{AB}.D_{fault}.\frac{dI_A}{dt} + L_{BB}.D_{fault}.\frac{dI_B}{dt} + L_{BC}.D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault}$$

$$V_{CN} = R_1.D_{fault}.I_C + \frac{R_0 - R_1}{3}.D_{fault}.3I0 + L_{AC}.D_{fault}.\frac{dI_A}{dt} + L_{BC}.D_{fault}.\frac{dI_B}{dt} + L_{CC}.D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault}$$

2.1.2 Impedance measurement algorithms work with instantaneous values (current and voltage). The derived current value (dI/dt) is obtained by using a FIR filter.

2.1.3 Phase-to-phase loop impedance

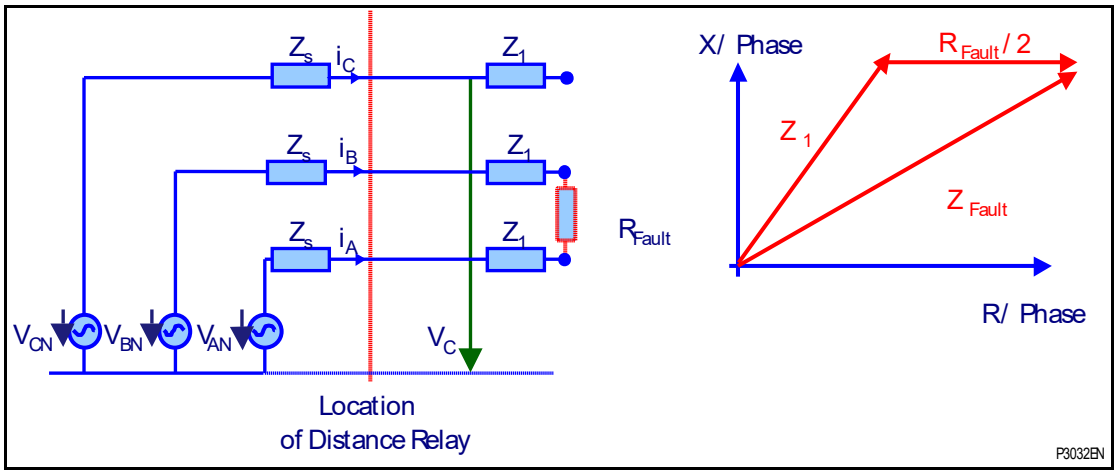


Figure 3: Phase-to-phase loop impedance

The impedance model for the phase-to-phase loop is:

$V\alpha\beta = ZL \times Dfault \times I\alpha\beta + Rfault /2 \times Ifault$

with $\alpha\beta$ = phase AB, BC or CA

The model for the current Ifault circulating in the fault $I\alpha\beta$.

$V_{AB} = 2Z_1.D_{fault}.I_{AB} + R_{fault}.I_{fault}$

$V_{BC} = 2Z_1.D_{fault}.I_{BC} + R_{fault}.I_{fault}$

$V_{CA} = 2Z_1.D_{fault}.I_{CA} + R_{fault}.I_{fault}$

= 3 phase-to-phase loops are continuously monitored and computed for each sample.

$V_{\alpha\beta} = 2Z_1.D_{fault}.I_{\alpha\beta} + R_{fault}.I_{fault}$

$V_{\alpha\beta} = 2(R_1 + j.\ X_1).D_{fault}.I_{\alpha\beta} + R_{fault}.I_{fault}$

$V_{\alpha\beta} = 2R_1.D_{fault}.I_{\alpha\beta} + 2j.\ X_1.D_{fault}.I_{\alpha\beta} + R_{fault}.I_{fault}$

$$V_{\alpha\beta} = 2R_1.D_{fault}.I_{\alpha\beta} + 2X_1.D_{fault}.\frac{dI\alpha\beta}{dt} + R_{fault}.I_{fault}$$

$$V_{AB} = R_1.D_{fault}.(I_A - I_B) + (L_{AA}-L_{AB}).D_{fault}.\frac{dI_A}{dt} + (L_{AB}-L_{BB}).D_{fault}.\frac{dI_B}{dt} + (L_{AC}-L_{BC}).D_{fault}.\frac{dI_C}{dt} + \frac{R_{fault}}{2}.I_{fault}$$

$$V_{BC} = R_1.D_{fault}.(I_B - I_C) + (L_{AB}-L_{AC}).D_{fault}.\frac{dI_A}{dt} + (L_{BB}-L_{BC}).D_{fault}.\frac{dI_B}{dt} + (L_{BC}-L_{CC}).D_{fault}.\frac{dI_C}{dt} + \frac{R_{fault}}{2}.I_{fault}$$

$$V_{CA} = R_1.D_{fault}.(I_C - I_A) + (L_{AC}-L_{AA}).D_{fault}.\frac{dI_A}{dt} + (L_{BC}-L_{AB}).D_{fault}.\frac{dI_B}{dt} + (L_{CC}-L_{AC}).D_{fault}.\frac{dI_C}{dt} + \frac{R_{fault}}{2}.I_{fault}$$

Impedance measurement algorithms work with instantaneous values (current and voltage).

The derived current value (dI/dt) is obtained by using a FIR filter.

2.2 "Delta" Algorithm

The patented high-speed algorithm has been proven with at least 20 years of service at all voltage levels from MV to EHV networks. The P44x relay has ultimate reliability of phase selection and directional decision far superior to standard distance techniques using superimposed algorithms. These algorithms or delta algorithms are based on transient components and they are used for the following functions which are computed in parallel:

Detection of the fault

By comparing the superimposed values to a threshold which is low enough to be crossed when a fault occurs and high enough not to be crossed during normal switching outside of the protected zones.

Establishing the fault direction

Only a fault can generate superimposed values; therefore, it is possible to determine direction by measuring the transit direction of the superimposed energy.

Phase selection

As the superimposed values no longer include the load currents, it is possible to make high-speed phase selection.

2.2.1 Fault Modelling

Consider a stable network status-the steady-state load flow prior to any start. When a fault occurs, a new network is established. If there is no other modification, the differences between the two networks (before and after the fault) are caused by the fault. The network after the fault is equivalent to the sum of the values of the status before the fault and the values characteristic of the fault. The fault acts as a source for the latter, and the sources act as passive impedance in this case.

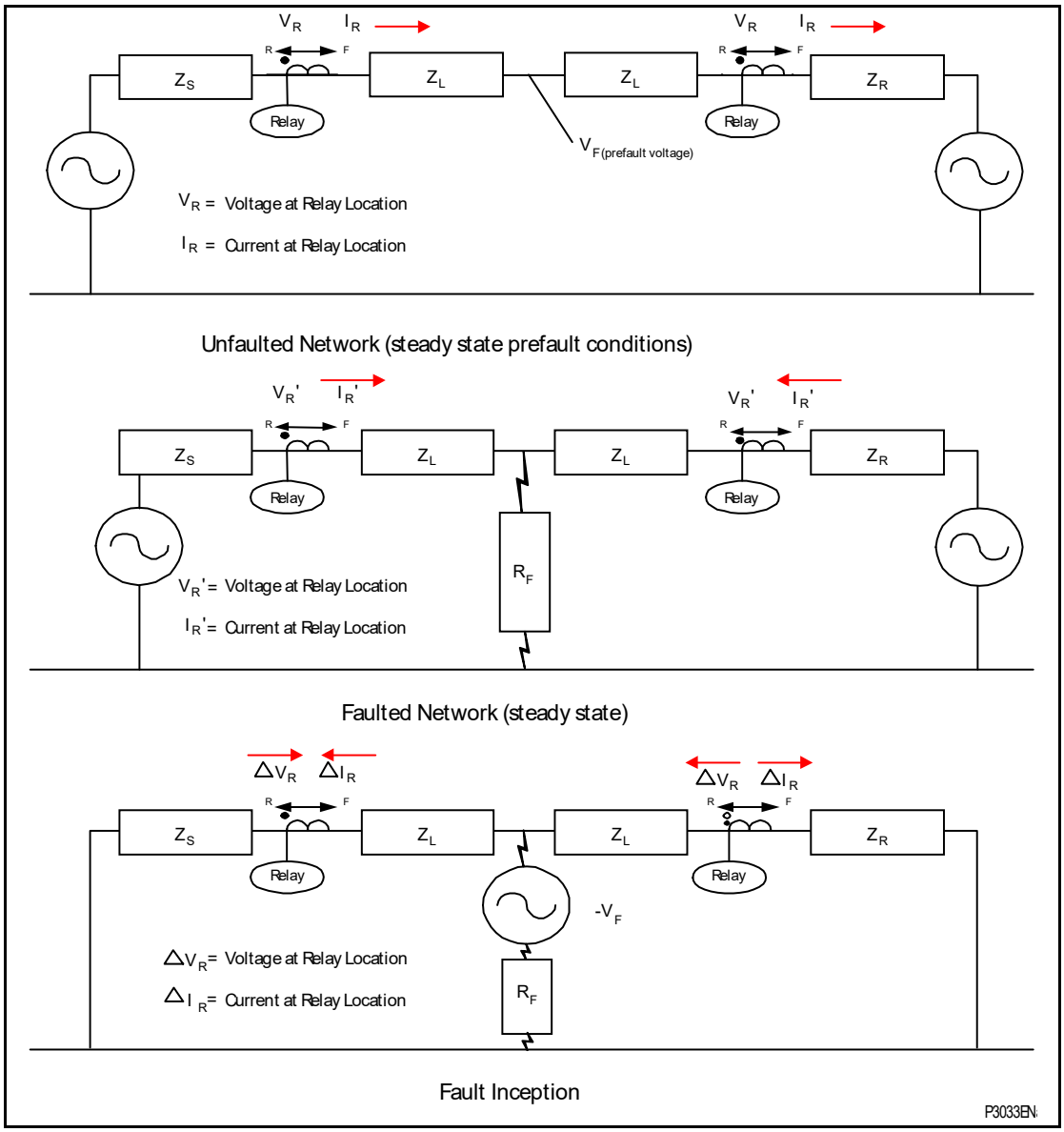


Figure 4: Prefault and fault inception value

Network Status Monitoring

The network status is monitored continuously to determine whether the "Deltas" algorithms can be used. The network must be "healthy". This is characterised by the following:

- The circuit breaker(s) should be closed just prior to fault inception (2 cycles of healthy pre-fault data should be stored) – the line is energised from one or both ends,
- The source characteristics should not change noticeably (there is no power swing or out-of-step detected).

- Power System Frequency is being measured and tracked (48 samples per cycle at 50 or 60 Hz).

No fault is detected:

- all nominal phase voltages are between 70% and 130% of the nominal value.
- the residual voltage (3V0) is less than 10% of the nominal value
- the residual current (3I0) is less than 10% of the nominal value + 3.3% of the maximum load current flowing on the line

The measured loop impedance is outside the characteristics, when these requirements are fulfilled, the superimposed values are used to determine the fault inception (start), faulty phase selection and fault direction. The network is then said to be "healthy" before the fault occurrence.

2.2.2 Detecting a Transition

To detect a transition, the MiCOM P442 and P444 compares sampled current and voltage values at the instant "t" with the values predicted from those stored in the memory one period and two periods earlier.

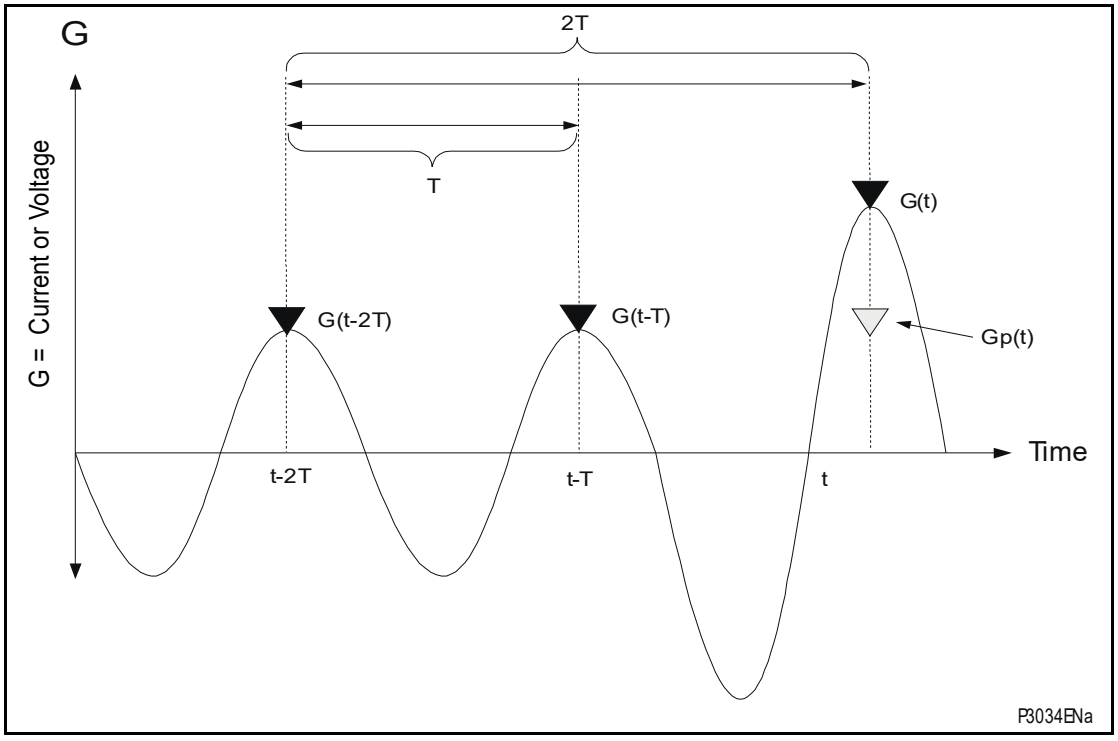


Figure 5: Transition detection

Gp(t) = 2G(t-T) - G(t-2T) where Gp(t) are the predicted values of either the sampled current or voltage

A transition is detected on one of the current or voltage input values if the absolute value of (G(t) - Gp(t)) exceeds a threshold of 0.2 x IN (nominal current) or 0.1 x UN / √3 = 0.1x VN (nominal voltage)

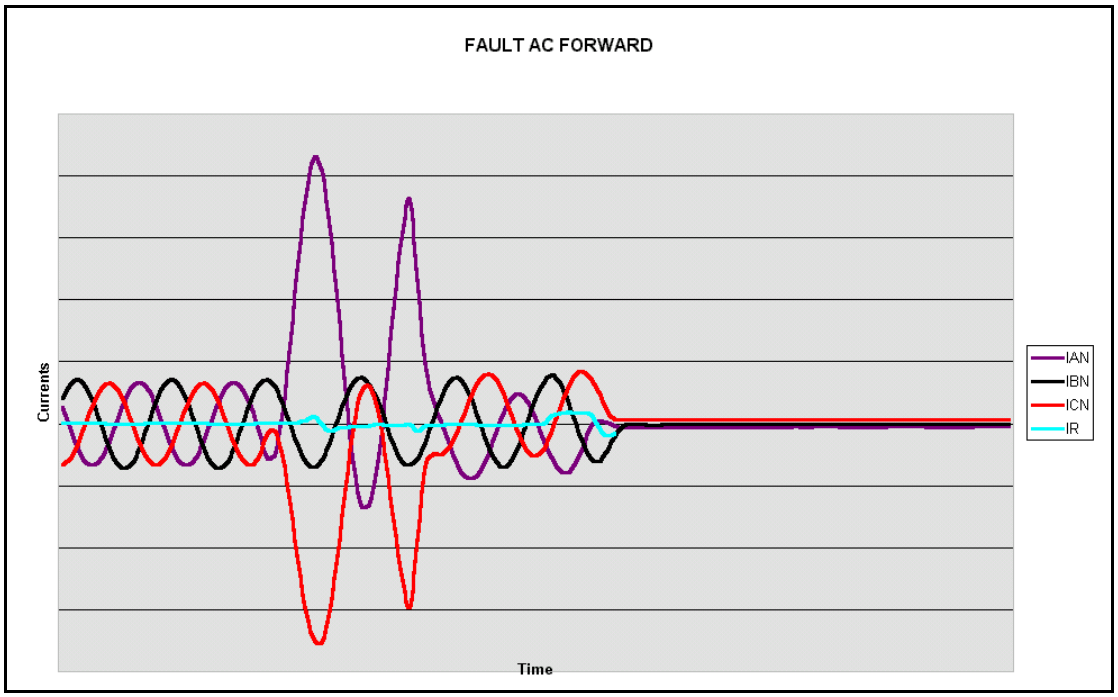
With: U = phase-to-phase voltage

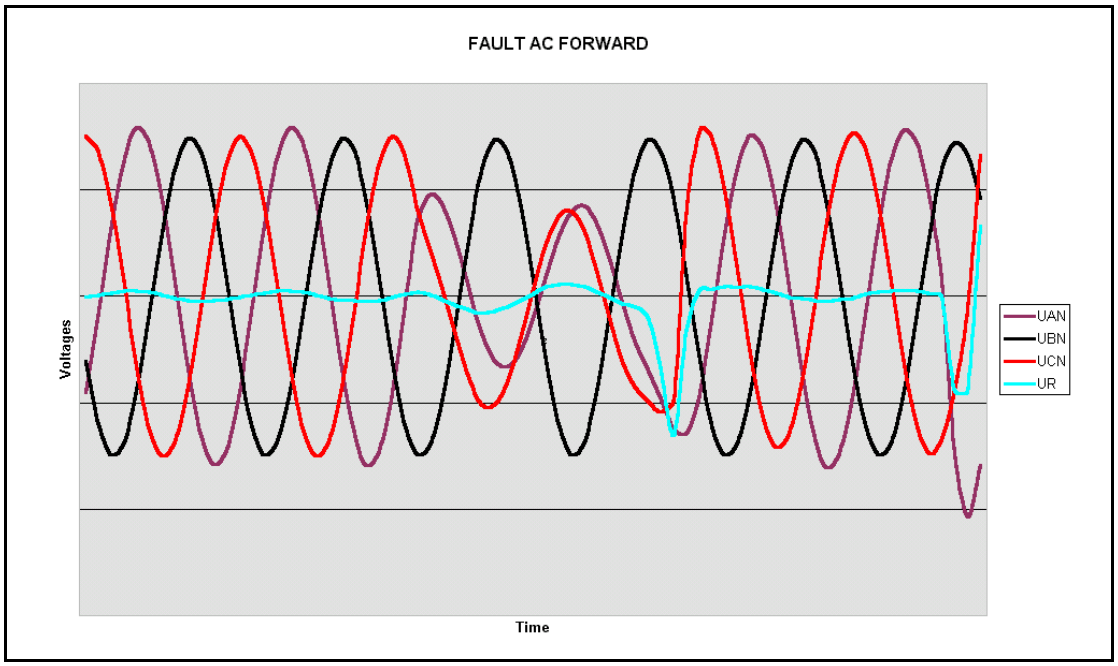
V = phase-to-ground voltage = U / √3

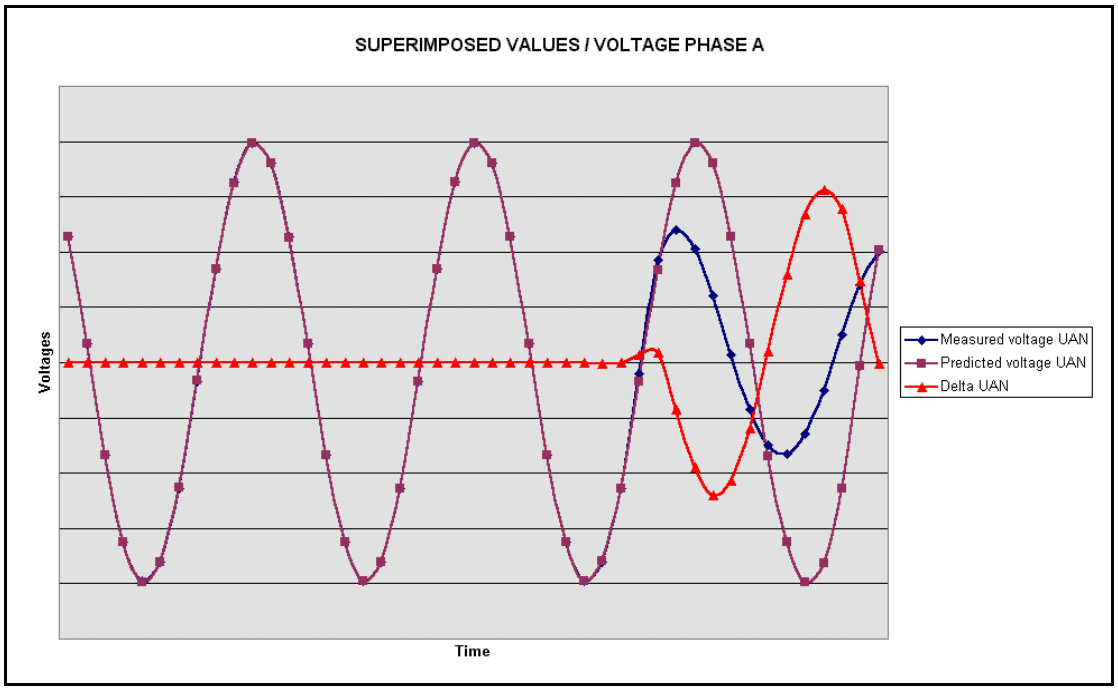
G(t) = G(t) - Gp(t) is the transition value of the reading G.

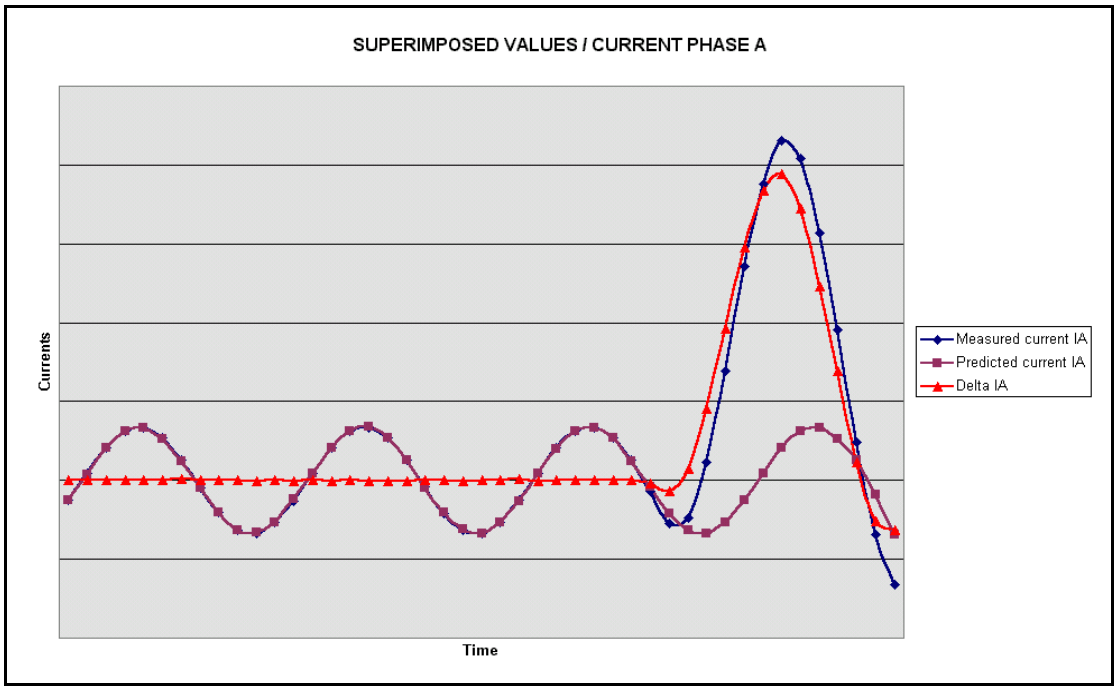
The high-speed algorithms will start if either DU OR DI is detected on one sample.

Example: isolated AC fault






SUPERIMPOSED VALUES / VOLTAGE PHASE A
Voltages
Time
Measured voltage UAN
Predicted voltage UAN
Delta UAN


SUPERIMPOSED VALUES / CURRENT PHASE A
Currents
Time
Measured current IA
Predicted current IA
Delta IA

2.2.3 Confirmation

To eliminate the transitions generated by possible operations or by high frequencies, the transition detected over a succession of three sampled values is confirmed by checking for at least one loop for which the two following conditions are met:

- ΔV > threshold V, where threshold V = 0.1 Un /√3 = 0.1 Vn

and

- ΔI > threshold I, where threshold I = 0.2 In.

The start-up of the high-speed algorithms are confirmed if ΔU AND ΔI are detected on three consecutive samples.

If Load Blinder feature is enabled, The ΔV > threshold V will change depending on “Load Blinder V<” setting. Refer to section 4.2 Load blinding (load avoidance)

2.2.4 Directional Decision

The "Delta" detection of the fault direction is determined from the sign of the energy per phase for the transition values characterising the fault.

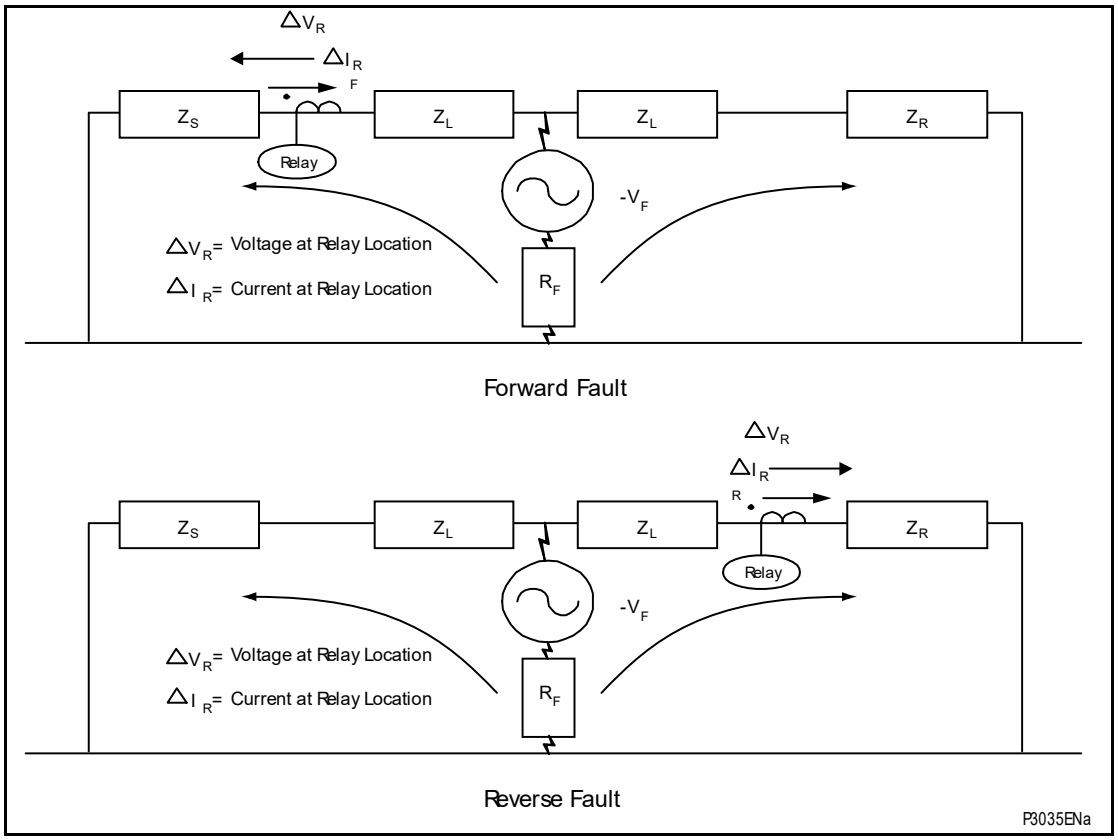


Figure 6: Directional determination using superimposed values

To do this, the following sum per phase is calculated:

$$SA = \sum_{n0}^{ni \geq n0+5} (\Delta V_{ANi}.\Delta I_{Ai}) \qquad SB = \sum_{n0}^{ni \geq n0+5} (\Delta V_{BNi}.\Delta I_{Bi}) \qquad SC = \sum_{n0}^{ni \geq n0+5} (\Delta V_{CNi}.\Delta I_{Ci})$$

where no is the instant at which the fault is detected, ni is the instant of the calculation and S is the calculated transition energy.

If the fault is in the forward direction, then S i <0 (i = A, B or C phase).

If the fault is in the reverse direction, then S i >0.

The directional criterion is valid if

S >5 x (10% x Vn x 20% x In x cos (85°)

This sum is calculated on five successive samples.

the RCA angle of the delta algorithms is equal to 60° (-30°) if the protected line is not serie compensated (otherwise RCA is equal to 0°).

2.2.5 Phase Selection

Phase selection is made on the basis of a comparison between the transition values for the derivatives of currents IA, IB and IC:

ΔI'A, ΔI'B, ΔI'C, ΔI'AB, ΔI'BC, ΔI'CA

> *Note: The derivatives of the currents are used to eliminate the effects of the DC current component.*

Therefore:

$$S_{AN} = \sum_{n0}^{ni \geq n0+4} (\Delta I'_{A_i})^2 \qquad S_{AB} = \sum_{n0}^{ni \geq n0+4} (\Delta I'_{AB_i})^2$$

$$S_{BN} = \sum_{n0}^{ni \geq n0+4} (\Delta I'_{B_i})^2 \qquad S_{BC} = \sum_{n0}^{ni \geq n0+4} (\Delta I'_{BC_i})^2$$

$$S_{CN} = \sum_{n0}^{ni \geq n0+4} (\Delta I'_{C_i})^2 \qquad S_{CA} = \sum_{n0}^{ni \geq n0+4} (\Delta I'_{CA_i})^2$$

The phase selection is valid if the sum ($S_{AB}+S_{BC}+S_{CA}$) is higher than a threshold. This sum is not valid if the positive sequence impedance on the source side is far higher than the zero sequence impedance. In this case, the conventional algorithms are used to select the faulted phase(s).

Sums on one-phase and two-phase loops are performed. The relative magnitudes of these sums determine the faulted phase(s).

For example, assume:

If $S_{AB}<S_{BC}<S_{CA}$ and If $S_{AB}<<S_{BC}$, the fault has had little effect on the loop A to B. If $S_{AN}<S_{BN}<S_{CN}$, the fault declared as single phase fault C.

If the fault is not detected as single-phase by the previous criterion, the fault conditions are multi-phase.

If $S_{AN}<S_{BN}<S_{CN}$ and If $S_{AB}<<S_{BC}$, the fault is B to C.

If $S_{AN}<S_{BN}<S_{CN}$ and If $S_{AB}\approx S_{BC}\approx S_{CA}$ and if $S_{AN}\approx S_{BN}\approx S_{CN}$, the fault is three-phase (the fault occurs on the three phases).

2.2.6 Summary

A transition is detected if ΔI > 20% x In or ΔV >10% x Vn

Then three tasks are starting in parallel:

- Fault confirmation: ΔI and ΔV (3 consecutive samples)
- Faulty phase selection (4 consecutive samples)
- Fault directional decision (5 consecutive samples)

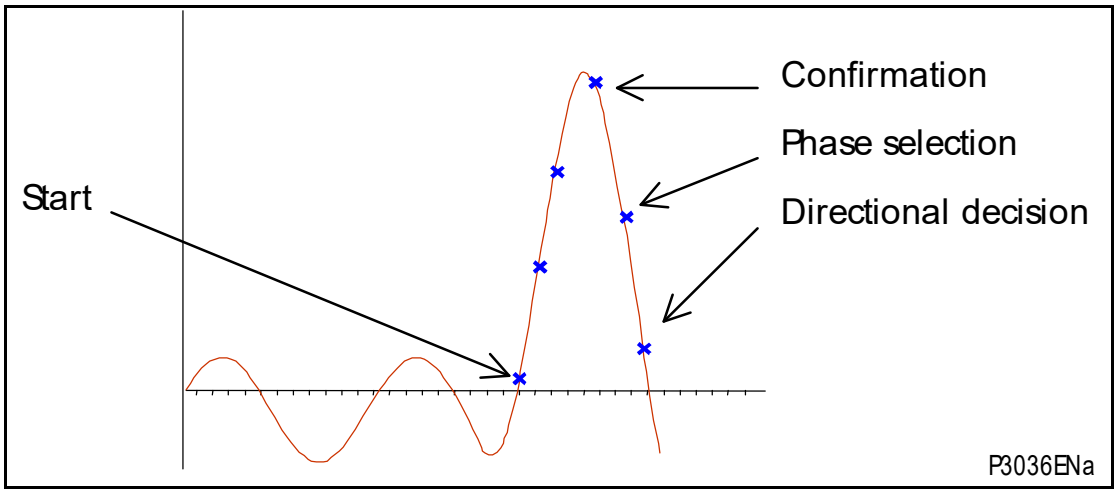


Figure 7: Deltas algorithms

High speed algorithms are used only during the first 2 cycles following a fault detection.

2.3 "Conventional" Algorithms

These algorithms do not use the superimposed values but use the impedance values measured under fault conditions. They are based on fault distance and resistance measurements.

They are used in the following circumstances:

- The condition before the fault could not be modelled.
- The superimposed values are not exclusively generated by the fault.

This may be true if the following occurs:

- A circuit breaker closing occurs during a fault. For SOTF, only the Conventional Algorithms can be used as there are not 2 cycles of healthy network stored.
- The fault is not recent and so the operating conditions of the generators have changed, or corrective action has been taken, that is, opening the circuit breakers. This occurs generally after the first trip. High Speed algorithms are used only during the first 2 cycles after the fault detection.
- operating conditions are not linear.

The conventional algorithms are also suited to detect low current faults that do not have the required changes in current and voltage for the "high-speed" (superimposed) algorithms. Therefore, their use assures improved coverage.

The "Conventional" algorithms run continuously with "high-speed" algorithms. If the "high speed" algorithms cannot declare faulted phase(s) and direction, the conventional algorithms will.

Note:	*The distance measurement of the fault is taken on the loop selected by the "Delta" or "conventional" phase selection algorithms. This measurement uses the fault values which are computed by Gauss Seidel method.*

2.3.1 Convergence Analysis

This analysis is based on the measurements of distance and resistance of the fault. These measurements are taken on each phase-ground and phase-phase loops (18 loops in total). They determine the convergence of these loops within a parallelogram-shaped, start-up characteristic.

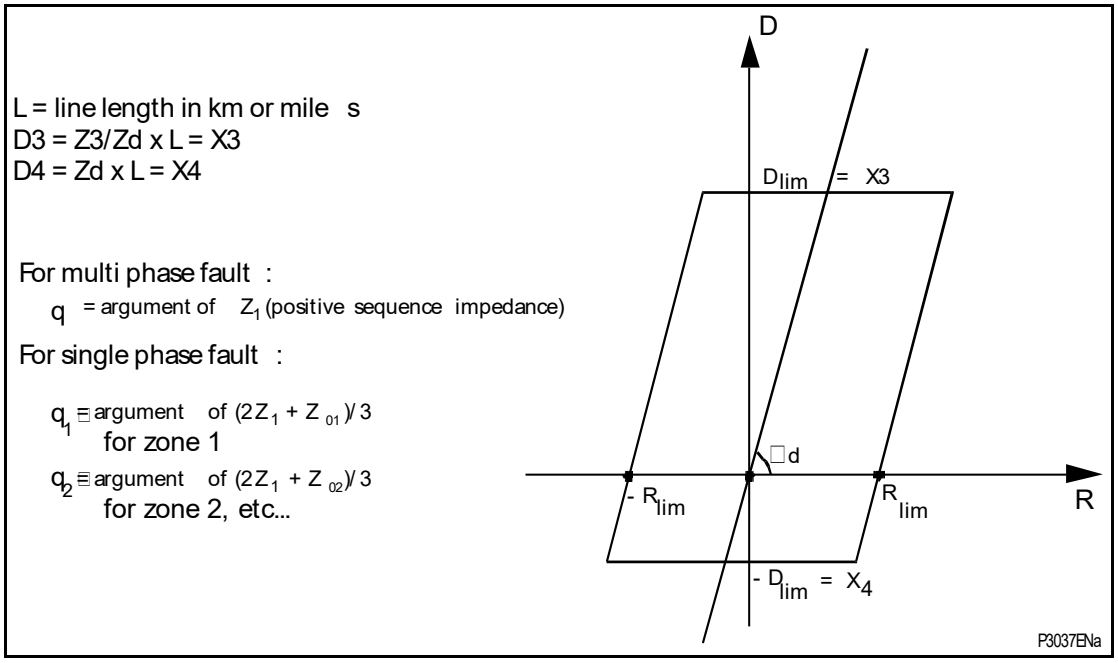


Figure 8: Start-up characteristic

Let R_{lim} and D_{lim} be the limits of the starting characteristic.

The pair of solutions (D_{fault} (n-1), R_{fault} (n-1)) and (D_{fault} (n), R_{fault} (n)):

- R_{fault} (n-1)< R_{lim}, and R_{fault} (n)< R_{lim}, and R_{fault} (n-1) - R_{fault} (n)< 10% x R_{lim}
- D_{fault} (n-1)< D_{lim} and D_{fault} (n) < D_{lim} and D_{fault} (n-1) - D_{fault} (n) < 10% x D_{lim}

where R_{lim} is the resistance limit for the single and multi phase faults. This convergence requires the equations to be collinear, therefore allowing the terms in D_{fault} and R_{fault} to be discriminated.

Theoretically, zone limits are Z3, Z4, +/- R3G-R4G or +/- R3Ph-R4Ph, if zones 3 and 4 are enabled. The slope of the characteristic mimics the characteristic of the line.

To model the fault current:

- Phase-phase loops: the values (I_A - I_B), (I_B - I_C), or (I_C - I_A) are used.
- Phase-ground loops: (I_A+ k_0 x $3I_0$), (I_B + k_0 x $3I_0$), or (I_C + k_0 x $3I_0$) are used.

The results of these algorithms are mainly used as a backup; consequently, the circuit breaker located at the other end is assumed to be open.

2.3.2 Start-Up

Start-up is initiated when at least one of the six measuring loops converges in the characteristic (Z_{AN}, Z_{BN}, Z_{CN}, Z_{AB}, Z_{BC}, Z_{CA}).

2.3.3 Phase Selection

If the fault currents are high enough with respect to the maximum load currents current-based phase selection is used; if not, impedance-based phase selection is required.

Current Phase Selection

Amplitudes I'A, I'B, I'C are derived from the three measured phase currents IA, IB, IC. These values are then compared to each other and to the two thresholds S1 and S2:

- First threshold is S1= 3 x I'n
- Second threshold is S2 = 5 x I'n

Example:

If I'A< I'B < I' C:

- If I'_C > S2 and I'_A > S1, the fault is three-phase.
- If I'_C > S2, I'B > S1 and I'_A < S1, the fault is two-phase, on phases B and C.
- If I'_C > S2 and I'_B < S1, the fault is single-phase, on phase C.
- If I'_C < S2, the current phase selection cannot be used. Impedance phase selection should then be used.

Impedance Phase Selection

Impedance phase selection is obtained by checking the convergence of the various measuring loops within the start-up characteristic, as follows:

- T = Presence of zero-sequence voltage or current (logic Information: 0 or 1).
- Z_{AN} = Convergence within the characteristic of the loop A (logic Information).
- Z_{BN} = Convergence within the characteristic of the loop B (logic Information).
- Z_{CN} = Convergence within the characteristic of the loop C (logic Information).
- Z_{AB} = Convergence within the characteristic of the loop AB (logic Information).
- Z_{BC} = Convergence within the characteristic of the loop BC (logic Information).
- Z_{CA} = Convergence within the characteristic of the loop CA (logic Information).

In addition, the following are also defined:

- $R_{AN} = Z_{AN} \times \overline{Z_{BC}}$ where ZBC = convergence within the characteristic of the loop BC (Logic Information).
- $R_{BN} = Z_{BN} \times \overline{Z_{CA}}$ where ZCA = convergence within the characteristic of the loop CA (Logic Information).
- $R_{CN} = Z_{CN} \times \overline{Z_{AB}}$ where ZAB = convergence within the characteristic of the loop AB (Logic Information).
- $R_{AB} = Z_{AB} \times \overline{Z_{CN}}$ where ZCN = convergence within the characteristic of the loop C (Logic Information).
- $R_{BC} = Z_{BC} \times \overline{Z_{AN}}$ where ZAN = convergence within the characteristic of the loop A (Logic Information).
- $R_{CA} = Z_{CA} \times \overline{Z_{BN}}$ where ZBN= convergence within the characteristic of the loop B (Logic Information).

Following are the different phase selections:

- $S_{AN} = T \times R_{AN} \times \overline{R_{BN}} \times \overline{R_{CN}}$ single-phase A to earth fault
- $S_{BN} = T \times R_{BN} \times \overline{R_{AN}} \times \overline{R_{CN}}$ single-phase B to earth fault
- $SCN = T \times RCN \times \overline{R_{BN}} \times \overline{R_{CN}}$ single-phase C to earth fault
- $S_{ABN} = T \times R_{AB} \times Z_{AN} \times Z_{BN}$ double-phase A to B to earth fault
- $S_{BCN} = T \times R_{BC} \times Z_{BN} \times Z_{CN}$ double-phase B to C to earth fault
- $S_{CAN} = T \times R_{CA} \times Z_{AN} \times Z_{CN}$ double-phase C to A to earth fault
- $S_{AB} = \overline{T} \times R_{AB} \times \overline{R_{BC}} \times \overline{R_{CA}}$ double-phase A to B fault
- $BC = \overline{T} \times R_{BC} \times \overline{R_{AB}} \times \overline{R_{CA}}$ double-phase B to C fault
- $CA = \overline{T} \times R_{CA} \times \overline{R_{AB}} \times \overline{R_{BC}}$ double-phase B to C fault
- $S_{ABC} = Z_{AN} \times Z_{BN} \times Z_{CN} \times Z_{AB} \times Z_{BC} \times Z_{CA}$ three-phase fault

For a three-phase fault, if the fault resistance of one of the two-phase loops is less than half of the fault resistances of the other two-phase loops, it will be used for the directional and distance measuring function. If not, the loop AB will be used.

Note:	*Impedance phase selection is used only if current phase selection is unable to make a decision.*

2.3.4 Directional Decision

The fault direction is defined on the basis of the calculation of the phase shift between the stored voltage and the derivative of a current. The current and the voltage used are those of the measuring loop(s) defined by the phase selection.

For the two-phase loops, the calculation of the phase shift between the stored voltage and the derivative of the current on the faulty two-phases.

For the single-phase loops, the calculation of the phase shift between the stored voltage and the current (I'x + k0 x 3I'0), where:

I'x = derivative of current on the faulted single-phase where x = A, B, or C

3I'0 = derivative of residual current

k0 = residual compensation factor, where for example k01 = (Z0–Z1)/3Z1

The directional angle is fixed between-30° and +150° (RCA =60°).

2.3.5 Directional Decision during SOTF-TOR (Switch On To Fault/Trip On Reclose)

The directional information is calculated from the stored voltage values if the network is detected as healthy. The calculations vary depending on the type of fault, i.e., single-phase or multiphase.

If the network frequency cannot be measured and tracked, the directional element cannot be calculated from the stored voltage. A zero sequence directional is calculated if there are enough zero-sequence voltage and current. If the zero-sequence directional is not valid, a negative-sequence directional is calculated if there are enough negative sequence voltage and current. If both directions cannot be calculated, the directional element is forced forward.

Single-phase fault

The reference voltage is stored in memory when the fault appears. When the fault is eliminated by single-phase tripping, the high-speed single-phase auto-reclose (HSAR) is started.

If a fault appears less than three cycles after the AR starts, the stored voltage value remains valid as the reference and is used to calculate direction.

If no fault appears during the three cycles after the AR starts, the reference voltage value becomes that of one of the healthy phases.

If a fault appears during the continuation of the AR cycle or reclosure occurs, the stored voltage value remains valid for 10 seconds.

If a stored voltage does not exist (SOTF) when one or more loops are convergent within the start-up characteristic, the directional is forced forward and the trip is instantaneous (if “SOTF All Zones” is set or according to the zone location if SOTF Zone 2, etc. is set). If the settable switch on to fault current threshold I>3 is exceeded on reclosure, the relay instantaneously trips three-phase (No timer I>3 is applied).

Two-phase or three-phase fault

The reference voltage is stored in memory when the fault appears. When the fault is cleared, the stored voltage value remains valid for 10 seconds. If reclosure occurs during these 10 seconds, the direction is calculated using the stored voltage value.

If a stored voltage does not exist when one or more loops are convergent within the start-up characteristic, the forward direction is forced and the trip is instantaneous when protection starts (SOTF All Zones). If the switch on to fault current threshold I>3 is exceeded on reclosure, the relay instantaneously trips three-phase (TOR All Zones).

The distance element trips immediately as soon as one or more loops converge in the start-up characteristic during SOTF (SOTF All Zones).

Other modes can be selected to trip selectively by SOTF or TOR according to the fault location. There are 15 bits of settings in TOR-SOTF logic.

2.4 Faulted Zone Decision

The Decision of the faulted zone is determined by either the zone "Deltas" or "Conventional" algorithms.

The zones are defined for a convergence between the Dfault and Rfault limits related to each zone. So, the solution pair (Rfault, Dfault) is said to be convergent if:

- R_{fault} (n-1) < R_{fault} (i) and R_{fault} (n) < R_{fault} (i) and |R_{fault} (n-1) – R_{fault} (n)| < 10% x R_{fault} (i)
- D_{fault} (n-1) < D_{fault} (i) and D_{fault} (n) < D_{fault} (i) and |D_{fault} (n-1) - D_{fault} (n)| < k% x D_{fault} (i)

where:

k= 5% for zones Z1 and Z1X

and

10% for other zones Z2, Z3, Zp, Zq and Z4.

i= 1, 1X, 2, p, q, 3 and 4.

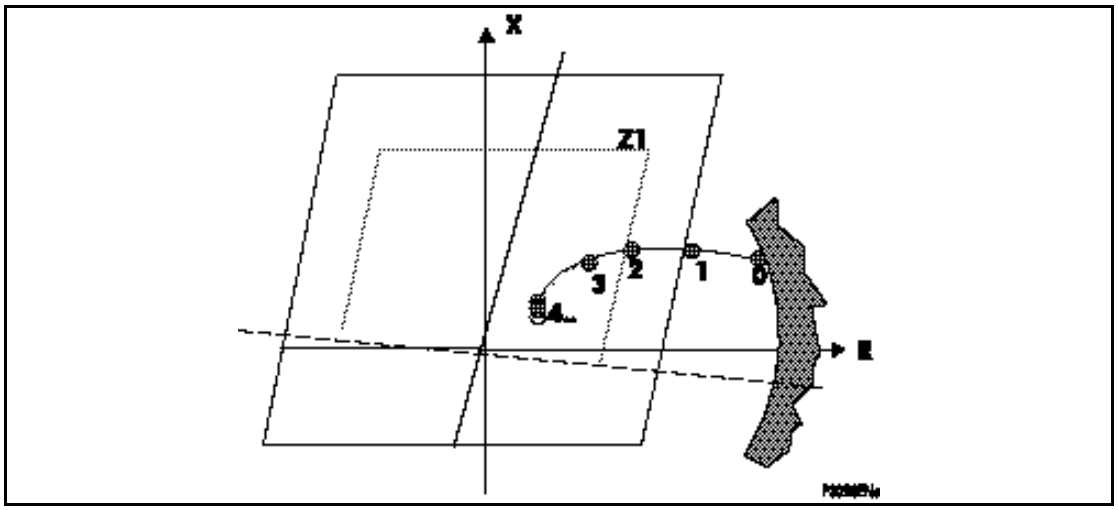


Figure 9: Phase-to-earth loop impedance

2.5 Tripping Logic

2.5.1 General

Three tripping modes can be selected ('Distance Scheme\Trip Mode' setting):

Single-pole trip at T1 (if “1P. Z1 & CR” is set): Single-pole trip for fault in zone 1 at T1 and channel-aided trip at T1. All other zones trip three-phase at their respective times for any fault types (∅-G, ∅-∅, ∅-∅-G, ∅-∅-∅, ∅-∅-∅-G).

Single-pole trip at T1 and T2 (if “1P. Z1Z2 & CR” is set): Single-pole trip for Z1 at T1, channel-aided trip at T1, and Z2 at T2. All other zones trip three-phase at their respective times for any fault types (∅-G, ∅-∅, ∅-∅-G, ∅-∅-∅, ∅-∅-∅-G).

Three-pole trip for all zones (Forces 3 poles): Three-phase trip for all zones at their respective times for all fault types (∅-G, ∅-∅, ∅-∅-G, ∅-∅-∅, ∅-∅-∅-G). Channel-aided trips will be three-phase with times corresponding to the pilot logic applied.

Zone	Time
Z1	T1
Z1X	T1
Z2	T2
Zp	Tp
Zq	Tq
Z3	T3
Z4	T4

There are six time delays associated with the seven zones present. Zone 1 and extended zone 1 have the same time delay.

Note: All the timers are initiated when the general start of the relay picks up (Z3Z4 convergence).

2.5.2 DDB inputs / outputs for General trip logic

The following DDB are available for CB monitoring (see section P44x/EN PL):

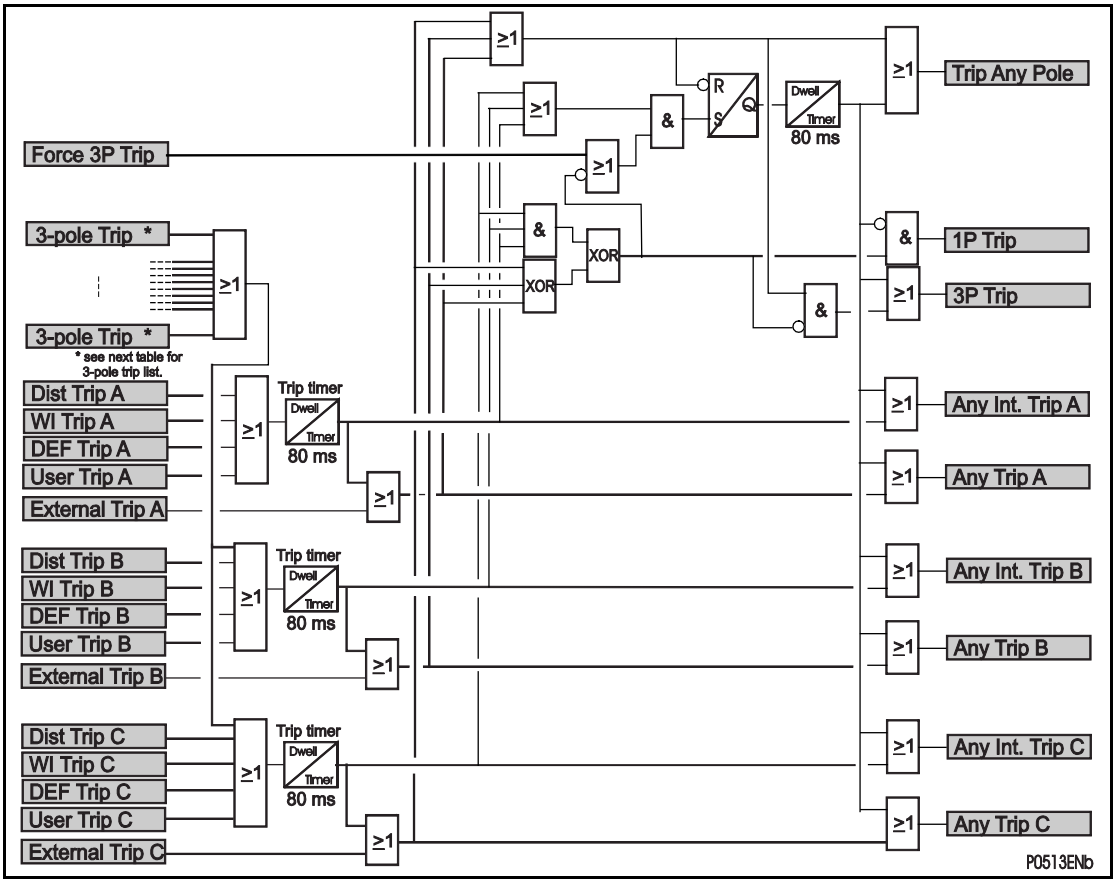
- Inputs
  - Three-pole trips (refer to the list in the logic diagram
  - Force 3P trip (see autoreclose section)
  - Dist trip a, Dist Trip B and Dist Trip C (see section “distance protection”),
  - WI trip A, WI Trip B and WI trip C (see section “weak infeed”)

- DEF Trip A, DEF Trip B and DEF Trip C (Directional Earth fault section),
- User Trip A, User Trip B and User Trip C (trip logic),
- External Trip A, External Trip B and External trip C (PSL)

- Outputs:
- 1P Trip,
  - 3P Trip,
  - Any Trip A, Any Trip B and Any Trip C,
  - Any Int. TripA, Any Int. TripB and Any Int. TripC.

2.5.2.1 Logic diagram

The next diagram shows general trip logic:



3-pole trip list:

IN>1 Trip	IN>2 Trip	I2> Trip	SOTF/TOR Trip
Loss. Load Trip	I>1 Trip	I>2 Trip	I>3 Trip
I>4 Trip	V<1 Trip	V<2 Trip	V<3 Trip
V<4 Trip	V>1 Trip	V>2 Trip	V>3 Trip
V>4 Trip	ZSP Trip	F<1 Trip	F<2 Trip
F<3 Trip	F<4 Trip	F>1 Trip	F>2 Trip

Figure 10: General trip logic

2.6 Fault Locator

The relay has an integral fault locator that uses information from the current and voltage inputs to provide a distance-to-fault measurement. The fault locator measures the distance by applying the same distance calculation principle as that used for the fault-clearing, distance-measurement algorithm.

The dedicated fault locator measurement is more accurate as it is based on a greater number of samples, and it uses the fault currents Ifault as models, as shown below:

- For a single-phase fault
  - AN : IfaultΔ (IA – I0)
  - BN : IfaultΔ (IB – I0)
  - CN : IfaultΔ (IC – I0)
- For a two-phase fault
  - AB : IfaultΔ (IA–IB)
  - BC : IfaultΔ (IB–IC)
  - CA : IfaultΔ (IC–IA)
- For a three-phase fault
  - ABC : IfaultΔ (IA–IB)

The sampled data from the analogue input circuits is written to a cyclic buffer until a fault condition is detected. The data in the input buffer is then held to allow the fault calculation to be made. When the fault calculation is complete the fault location information is available in the relay fault record.

When applied to parallel circuits, mutual flux coupling can alter the impedance seen by the fault locator. The coupling will contain positive, negative and zero sequence components. In practice the positive and negative sequence coupling is insignificant. The effect on the fault locator of the zero sequence mutual coupling can be eliminated by using the mutual compensation feature provided. This requires that the residual current on the parallel line is measured, as shown in Appendix B.

The calculation for single phase loop is based on the following equation:

$$V_{AN} = R_1.D_{fault}.I_A + \frac{R_0 - R_1}{3}.D_{fault}.3I_0 + L_{AA}.D_{fault}.\frac{dI_A}{dt} + L_{AB}.D_{fault}.\frac{dI_B}{dt} + L_{AC}.D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault} + R_m.I_m + L_m.\frac{dI_m}{dt}$$

$$V_{BN} = R_1.D_{fault}.I_B + \frac{R_0 - R_1}{3}.D_{fault}.3I_0 + L_{AB}.D_{fault}.\frac{dI_A}{dt} + L_{BB}.D_{fault}.\frac{dI_B}{dt} + L_{BC}.D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault} + R_m.I_m + L_m.\frac{dI_m}{dt}$$

$$V_{CN} = R_1.D_{fault}.I_C + \frac{R_0 - R_1}{3}.D_{fault}.3I_0 + L_{AC}.D_{fault}.\frac{dI_A}{dt} + L_{BC}.D_{fault}.\frac{dI_B}{dt} + L_{CC}.D_{fault}.\frac{dI_C}{dt} + R_{fault}.I_{fault} + R_m.I_m + L_m.\frac{dI_m}{dt}$$

Where:

R_m: zero-sequence mutual resistance

L_m: zero-sequence mutual inductance

I_m: zero-sequence mutual current

I_{fault}: fault current = ΔI – I0

The calculation for phase-to-phase loop is based on the following equation:

$$V_{AB} = R_1.D_{fault}.(I_A - I_B) + (L_{AA} - L_{AB}).D_{fault}.\frac{dI_A}{dt} + (L_{AB} - L_{BB}).D_{fault}.\frac{dI_B}{dt} + (L_{AC} - L_{BC}).D_{fault}.\frac{dI_C}{dt} + \frac{R_{fault}}{2}.I_{fault}$$

$$V_{BC} = R_1.D_{fault}.(I_B - I_C) + (L_{AB} - L_{AC}).D_{fault}.\frac{dI_A}{dt} + (L_{BB} - L_{BC}).D_{fault}.\frac{dI_B}{dt} + (L_{BC} - L_{CC}).D_{fault}.\frac{dI_C}{dt} + \frac{R_{fault}}{2}.I_{fault}$$

$$V_{AC} = R_1.D_{fault}.(I_C - I_A) + (L_{AC} - L_{AA}).D_{fault}.\frac{dI_A}{dt} + (L_{BC} - L_{AB}).D_{fault}.\frac{dI_B}{dt} + (L_{CC} - L_{AC}).D_{fault}.\frac{dI_C}{dt} + \frac{R_{fault}}{2}.I_{fault}$$

Where:

$I_{fault} = \Delta I$ ($\Delta I = \Delta I' - \Delta I''$)

$\Delta I_A - \Delta I_B$
$\Delta I_B - \Delta I_C$
$\Delta I_C - \Delta I_A$

2.6.1 Selecting the fault location data

Selection of the analogue data that is used depends on:

- How the fault is processed by the algorithms.
- The line model.

2.6.2 Processing algorithms

Distance to fault calculation will use the high speed algorithms if:

- A fault is detected by the high-speed algorithms
- The tripping occurred within the T1 or T2 time delays
- The distance to the fault is less than 105% of the line.

In this case, the distance to fault saved in the fault report will be displayed as:

Distance to the fault = 24.48km (L) accuracy 3%

If all three of these conditions are not met, the distance to fault value will be the same value used by the distance protection. The format of the display will then be as follows:

Distance to the fault = 31.02km accuracy 5%

Note: The more accurate fault location will be post scripted with an (L). This will occur when conditions are favourable for using the more accurate algorithm for distance to fault calculation.

2.6.2.1 Line Model Selection

The fault locator can distinguish between two types of line, as follows:

- Single lines.
- Parallel lines with mutual coupling.

Mutual coupling between transmission lines is common on power systems. Significant effects on distance relay operation during faults involving earth may occur. Typically, the positive and negative, mutual-sequence impedances are negligible, but zero-sequence

mutual coupling may be large, and either must be factored into the settings, or accommodated by measurement of the parallel, mutually-coupled lines residual (earth) current, where zero-sequence current information is available. The value of the residual currents from parallel lines is then integrated into the distance measurement equation.

The relay is capable of measuring and using mutually-coupled residual current information from parallel lines. The mutual current is measured by a dedicated analogue input.

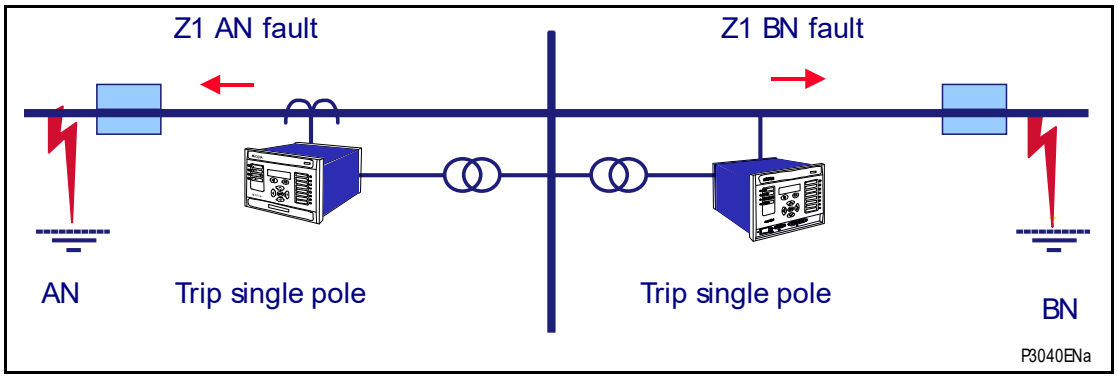
2.7 Double Circuit Lines

Double circuit lines must be taken into account in the operating principle of the protection scheme to avoid unwanted tripping of “sound” phases, which could be the result of an excessively general phase selection.

Phase selection for an inter-circuit fault

During a two-phase fault selection, for example on loop AB, the P44x checks direction on the two adjacent earth loops, (A to Neutral and B to Neutral). The direction is determined using either the conventional algorithm or the high-speed algorithm (using superimposed quantities), depending on fault severity. If superimposed components are used, the transient (fault) energy is summated phase by phase.

$$\text{FaultDirectionLoop_AN} = \sum_{n0}^{n} (\Delta V_{AN}.\Delta I_{A}) \text{ and FaultDirectionLoop_BN} = \sum_{n0}^{n} (\Delta V_{BN}.\Delta I_{B})$$



The directions of the two adjacent ground loops are compared, as follows:

- If the two directions are forward, the fault is a two-phase fault on the protected line.
- If only one of the directions is forward, for instance Sa, the fault is single-phase (A to Neutral) on the protected line.
- If the two directions are reverse, the fault is not on the protected line.

Protection against Current Reversal (Transient Blocking)

When a fault occurs on a line, which is parallel to the protected line, the pilot schemes on the protected line may be subjected current reversals from sequential clearing on the parallel line. A fault on the parallel line may start by appearing external to the protected line in the reverse direction, and then, after a sequential operation of one of the parallel line circuit-breakers, the fault appears forward. This situation can affect security of certain channel-aided schemes on the protected line.

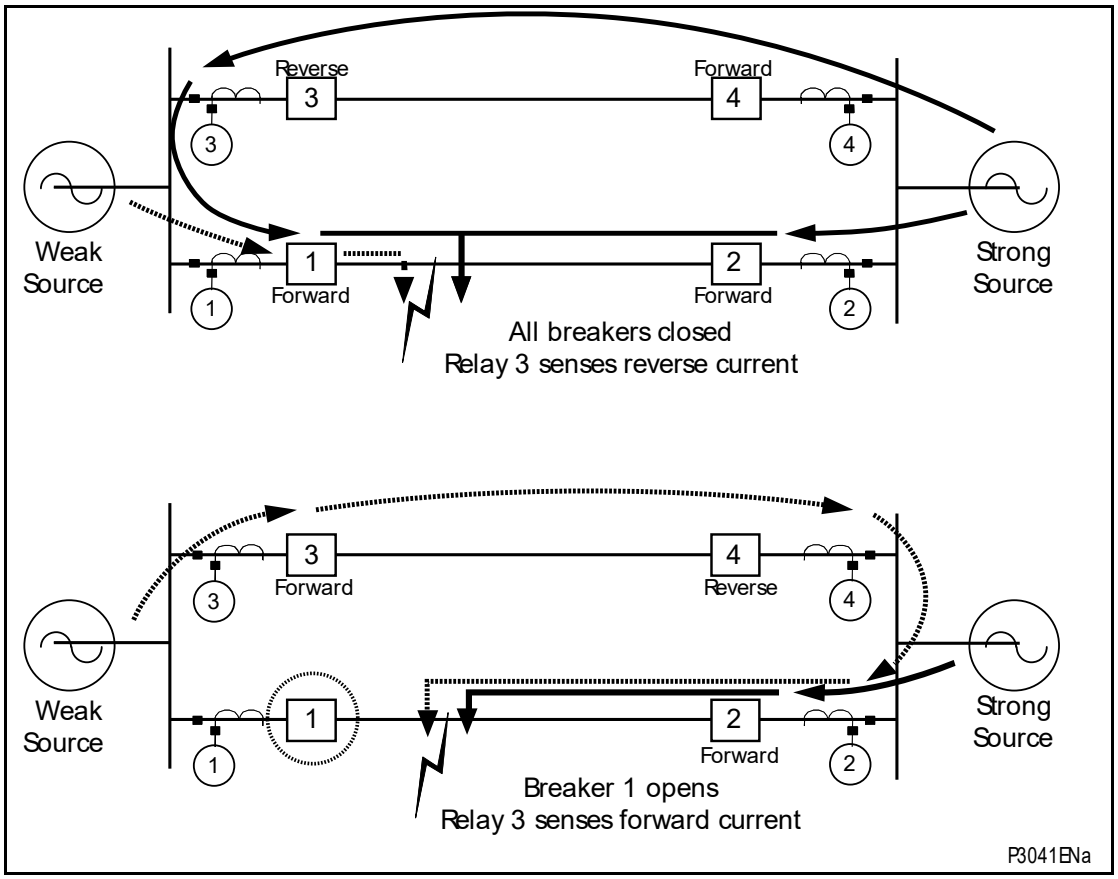


Figure 11: Direction reversal from sequential clearing of parallel lines

The P44x provides protection against the effects of this phenomenon by employing transient blocking. An adjustable timer is available that will block direct and permissive transfer trip signals from being used in the P44x logic, and will also block the P44x from sending direct or permissive transfer trip signals. This timer is designated as “Reverse Guard Timer”.

This provides protection against fault current reversal and will still allow fast tripping in the event of faults occurring in zone 1, if zone 1 is independent (not used as overreach zone).

3 DISTANCE PROTECTION AND DISTANCE SCHEME FUNCTIONS

The following sections detail the individual protection functions in addition to where and how they may be applied.

The following section details the individual distance protection functions, in addition to where they may be applied. It completes the P44x/EN ST section, where distance settings are detailed. This section details:

- The “distance protection” menu setting: This section explains how the line characteristics and the protection zones settings are applied to the relay,
- The “distance scheme” menu setting, where scheme setting are explained,
- Distance protection settings example, where:
  - A double circuit line protection is shown,
  - Additional details are given for three terminal lines applications,

Internal logic and an overview of the distance protection.

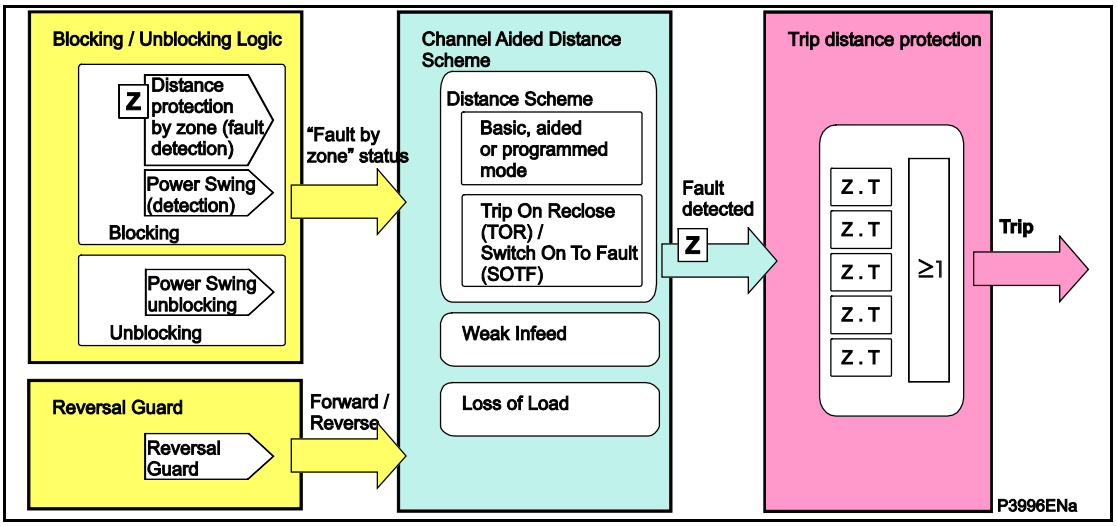


Figure 12: Distance protection

3.1 Fault distance characteristics (“Distance elements” menu setting)

This section explains in detail the “Distance elements” menu setting. This menu is used to set the line protection. The following sections contain line and zone setting application. A general example of setting (distance elements and schemes) is presented in section 3.4. Section 3.5 presents the logic of the distance protection (expert section).

The fault protection principle by zone is shown in the following diagram (basic distance fault protection). Relay A and relay B cover the line protection by zone. In general, zones 1 and 2 provide main protection for the line or cable, with zone 3 (or zone 4) reaching further to provide back up protection for faults on adjacent circuits.

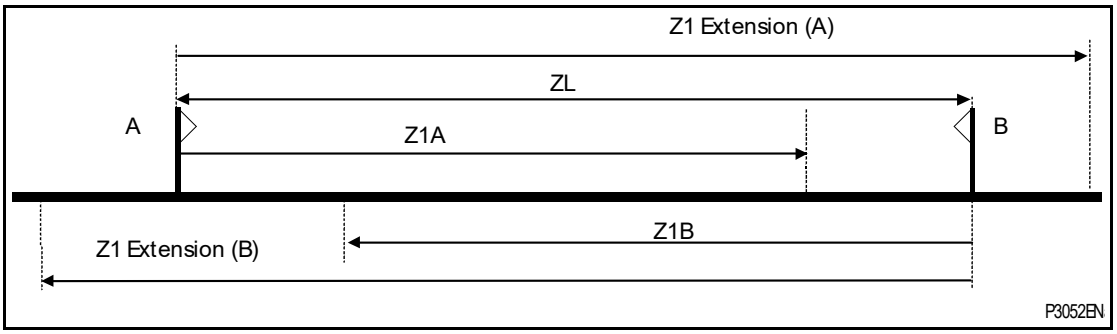


Figure 13: Main protection principle

3.1.1 Line setting

All impedance reaches for phase fault protection are calculated in polar form: Z ∠θ, where Z is the reach in ohms, and θ is the line angle setting in degrees, common to all zones.

The line parameters can be set in polar or rectangular form to give the total positive impedance of the protected line:

3.1.2 Zone setting

As shown in the following figure, the blocking / unblocking logic is based on a distance protection by zone:

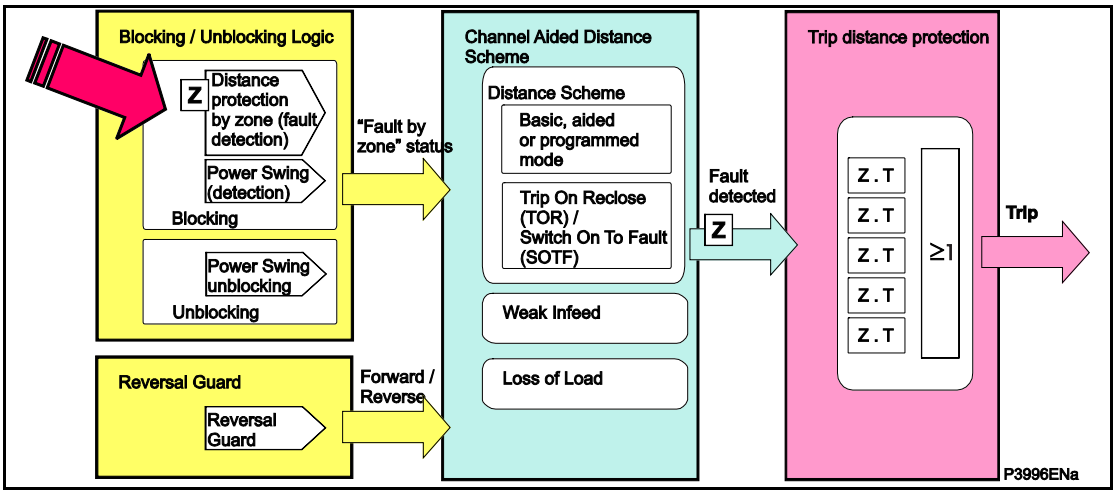


Figure 14: Fault detection by zone in the distance protection diagram

The Zone setting menu of the relay allows 6 zones setting.

3.1.2.1 Zone setting – Zone Status

The P442 and P444 relays have 6 zones of phase or earth fault protection, as shown in the impedance plots below. The fault protections are completed by a tilt characteristic (tilt angle).

The following impedance plot shows the phase fault characteristics:

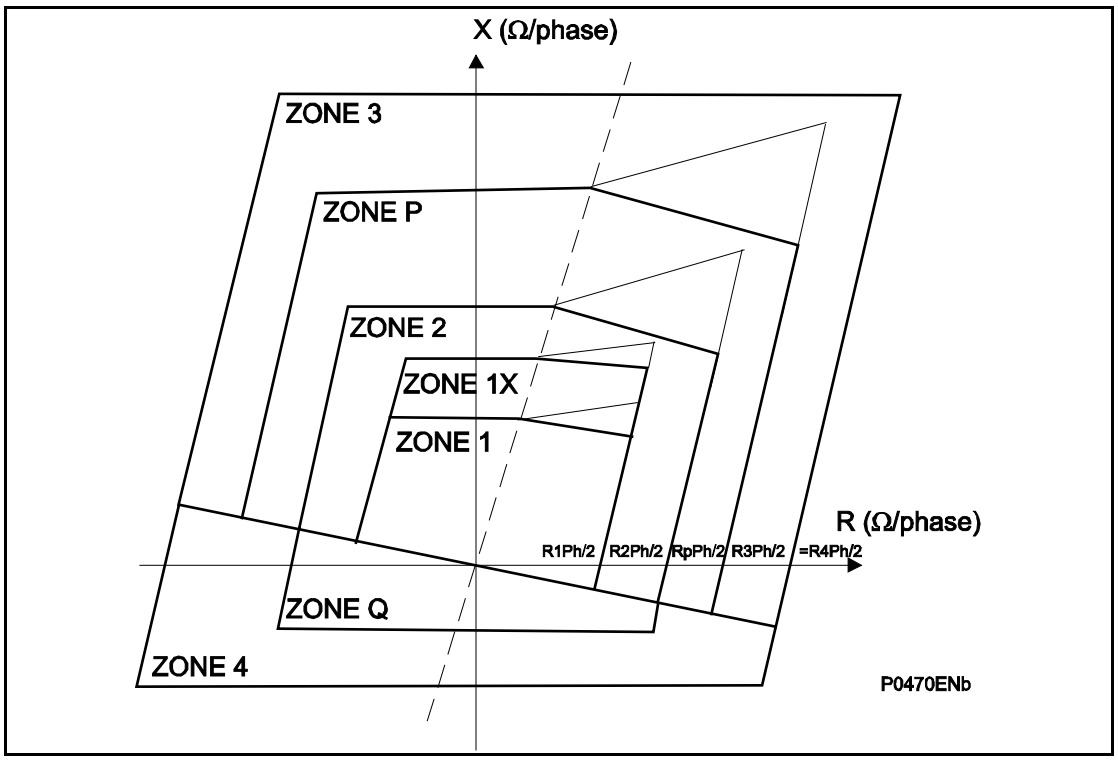


Figure 15: Phase/phase fault quadrilateral characteristics (Ω/phase scheme)

Note:	*1.*	*Z1 (zone 1) is programmed in ohm/loop. R limit setting is in ohms loop and Z limit setting is in ohms phase.*
	2.	*In a Ω/phase scheme, R must be divided by 2 (for a phase/phase diagram).*
	3.	*The angle of the start element (Quad) is the angle of the positive impedance of the line (settable)*
	4.	*TILT angle protection is only applied with conventional protection*

The earth fault characteristic is shown with the following impedance plot:

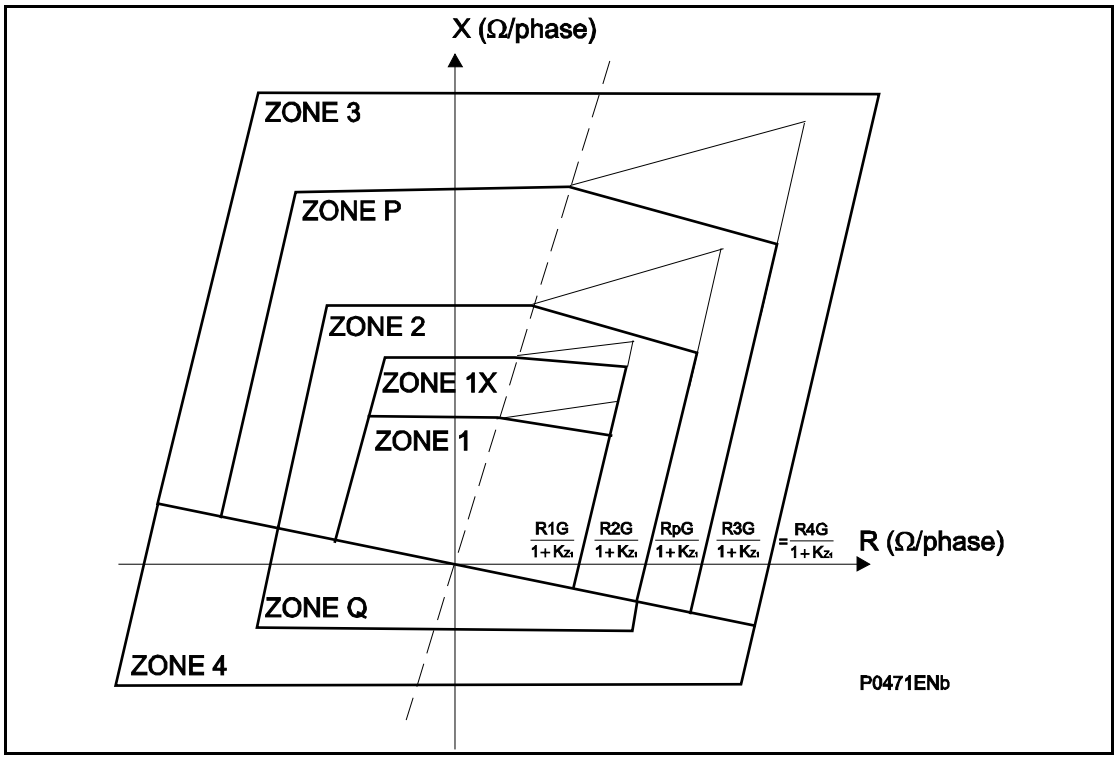


Figure 16: Phase/ground fault quadrilateral characteristics (Ω/phase scheme)

Note:	*1.*	*In a Ω/phase scheme, R must be divided by 1+K_Z (for a phase/ground diagram*
	2.	*The angle of the start element (Quad) is the angle of the $2Z_1+Z_0$ (Z_1: positive sequence Z, Z_0: zero sequence Z)*

3.1.2.1.1 Setting

"Zone Setting" menu is used to activate or deactivate individually the 6 zones. The following text will help you to set the zones:

- The zone 1 elements of a distance relay should be set to cover as much of the protected line as possible, allowing instantaneous tripping for as many faults as possible. In most applications the zone 1 reach (Z1) should not be able to respond to faults beyond the protected line. For an underreaching application the zone 1 reach must therefore be set to account for any possible overreaching errors. These errors come from the relay, the VTs and CTs and inaccurate line impedance data. It is therefore recommended that the reach of the zone 1 distance elements is restricted to 80 - 85% of the protected line impedance (positive phase sequence line impedance), with zone 2 elements set to cover the final 20% of the line. (Note: Two of the channel aided distance schemes described later, schemes POP Z1 and BOP Z1 use overreaching zone 1 elements, and the previous setting recommendation does not apply).
- The zone 2 elements should be set to cover the 20% of the line not covered by zone 1. Allowing for underreaching errors, the zone 2 reach (Z2) should be set in excess of 120% of the protected line impedance for all fault conditions. Where aided tripping schemes are used, fast operation of the zone 2 elements is required. It is therefore beneficial to set zone 2 to reach as far as possible, such that faults on the protected line are well within reach. A constraining requirement is that, where possible, zone 2 does not reach beyond the zone 1 reach of adjacent line protection. Where this is not possible, it is necessary to time grade zone 2 elements of relays on adjacent lines. For this reason the zone 2 reach should be set to cover ≤50% of the shortest adjacent line impedance, if possible. When setting zone 2 earth fault elements on parallel circuits, the effects of zero sequence mutual coupling will need to be accounted for. The mutual coupling results in the Zone 2 ground fault elements underreaching. To ensure adequate coverage an extended reach setting may be required, this is covered in Section 3.1.2.1.2.

- The zone 3 elements would usually be used to provide overall back-up protection for adjacent circuits. The zone 3 reach (Z3) is therefore set to approximately 120% of the combined impedance of the protected line plus the longest adjacent line. A higher apparent impedance of the adjacent line may need to be allowed where fault current can be fed from multiple sources or flow via parallel paths.
- Zones p and q are reversible directional zones. The setting chosen for zone p (q), if used at all, will depend upon its application. Typical applications include its use as an additional time delayed zone or as a reverse back-up protection zone for busbars and transformers. Use of zone p(q) as an additional forward zone of protection may be required by some users to line up with any existing practice of using more than three forward zones of distance protection. Zone p(q) may also be useful for dealing with some mutual coupling effects when protecting a double circuit line, which will be discussed in section 3.1.2.1.2
- The zone 4 elements would typically provide back-up protection for the local busbar, where the offset reach is set to 25% of the zone 1 reach of the relay for short lines (<30km) or 10% of the zone 1 reach for long lines. Setting zone 4 in this way would also satisfy the requirements for Switch on to Fault, and Trip on Reclose protection, as described in later sections. Where zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, zone 4 must reach further behind the relay than zone 2 for the remote relay. This can be achieved by setting: Z4 ≥ ((Remote zone 2 reach) x 120%) minus the protected line impedance.

To understand the distance zones interactions, it should be considered:

- If Zp is a forward zone:
  - Z1 ⩽ Z2 < Zp < Z3
  - T1 < T2 < tZp < T3 (
  - R1G < R2G < RpG < R3G = R4G
  - R1Ph < R1extPh < R2Ph < RpPh < R3Ph
- If Zp is a reverse zone:
  - Z1 < Z2 < Z3
  - Zp > Z4
  - T1 < T2 < T3
  - tZp < T4
  - R1G < R2G < R3G
  - RpG < R3G = R4G
  - R1Ph < R2Ph < R3Ph
  - RpPh < R3Ph = R4Ph
  - R3G < U_N / (1.2 X √3 I_N)
  - R3Ph < U_N / (1.2 X √3 I_N)



Note: 1. *If Z3 is disabled, the forward limit element becomes the smaller zone Z2 (or Zp if selected forward)*
2. *If Z4 is disabled, the directional limit for the forward zone is 30°.*

3.1.2.1.2 Zone 1 Extension Scheme

Auto-reclosure is widely used on radial overhead line circuits to re-establish supply following a transient fault. A Zone 1 extension scheme may therefore be applied to a radial overhead feeder to provide high speed protection for transient faults along the whole of the protected line. Figure 17 shows the alternative reach selections for zone 1: Z1 or the extended reach Z1X.

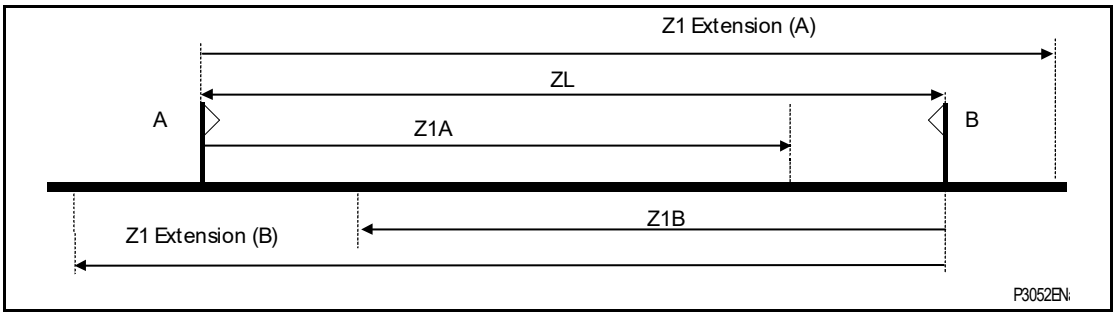


Figure 17: Zone 1 extension scheme

$$Z1 < Z1X < Z2 \quad \text{or} \quad Z1 < Z2 < Z1X$$
$$(\text{with } Z1 < ZL < Z1X)$$

In this scheme, zone 1X is enabled and set to overreach the protected line. A fault on the line, including one in the end 20% not covered by zone 1, will now result in instantaneous tripping followed by autoreclosure. Zone 1X has resistive reaches and residual compensation similar to zone 1. The autorecloser in the relay is used to inhibit tripping from zone 1X such that on reclosure the relay will operate with Basic scheme logic only, to coordinate with downstream protection for permanent faults. Therefore, transient faults on the line will be cleared instantaneously, which will reduce the probability of a transient fault becoming permanent. The scheme can, however, operate for some faults on an adjacent line, although this will be followed by autoreclosure with correct protection discrimination. Increased circuit breaker operations would occur, together with transient loss of supply to a substation.

The time delays associated with extended zone Z1X are:

Scenario	Z1X Time delay
First fault trip	= tZ1
Fault trip for persistent fault on autoreclose	= tZ2

Table 1: Trip time delays associated with zone 1X

The Zone 1 Extension scheme is selected by setting the **Z1X Enable** bit in the Zone Status (distance scheme menu) function links to 1.



*Note: To enable the Z1X logic (see section 3.5.2), the DDB: '**Z1X extension**' cell must be linked in the PSL (to an opto input or to reclaim time…)*

3.1.2.1.3 Effects of Mutual Coupling on Distance Settings

Where overhead lines are connected in parallel or run in close proximity for the whole or part of their length, mutual coupling exists between the two circuits. The positive and negative sequence coupling is small and can be neglected. The zero sequence coupling is more significant and will affect relay measurement during earth faults with parallel line operation.

Zero sequence mutual coupling causes a distance relay to underreach or overreach, depending on the direction of zero sequence current flow in the parallel line. However, it can be shown that this underreach or overreach will not affect relay discrimination during parallel line operation (ie. it is not be possible to overreach for faults beyond the protected line and neither will it be possible to underreach to such a degree that no zone 1 overlap exists). A channel-aided scheme will still respond to faults in the protected line and remain secure during external faults. Some applications exist, however, where the effects of mutual coupling should be addressed.

Effect of Mutual Coupling on Zone 1 Setting:

For the case shown in Figure 18, where one circuit of a parallel line is out of service and earthed at both ends, an earth fault at the remote bus may result in incorrect operation of the zone 1 earth fault elements. It may be desirable to reduce the zone 1 earth loop reach for this application. This can be achieved using an alternative setting group within the relay, in

which the residual compensation factor kZ1 is set to a lower value than normal (typically ≤ 80% of normal kZ1).

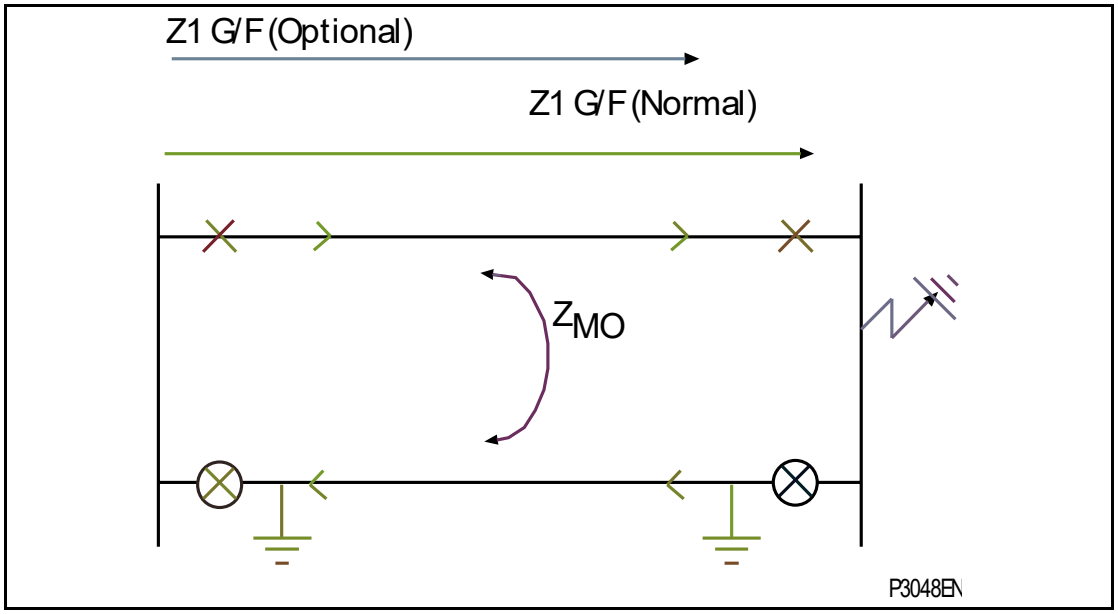


Figure 18: Zone 1 reach considerations

Effect of Mutual Coupling on Zone 2 Setting:

If the double circuit line to be protected is long and there is a relatively short adjacent line, it is difficult to set the reach of the zone 2 elements to cover 120% of the protected line impedance for all faults, but not more than 50% of the adjacent line. This problem can be exacerbated when a significant additional allowance has to be made for the zero-sequence mutual impedance in the case of earth faults. For parallel circuit operation the relay Zone 2 earth fault elements will tend to underreach. Therefore, it is desirable to boost the setting of the earth fault elements such that they will have a comparable reach to the phase fault elements. Increasing the residual compensation factor kZ2 for zone 2 will ensure adequate fault coverage.

Under single circuit operation, no mutual coupling exists, and the zone 2 earth fault elements may overreach beyond 50% of the adjacent line, necessitating time discrimination with other Zone 2 elements. Therefore, it is desirable to reduce the earth fault settings to that of the phase fault elements for single circuit operation, as shown in Figure 19. Changing between appropriate settings can be achieved by using the alternative setting groups available in the relay series relays.

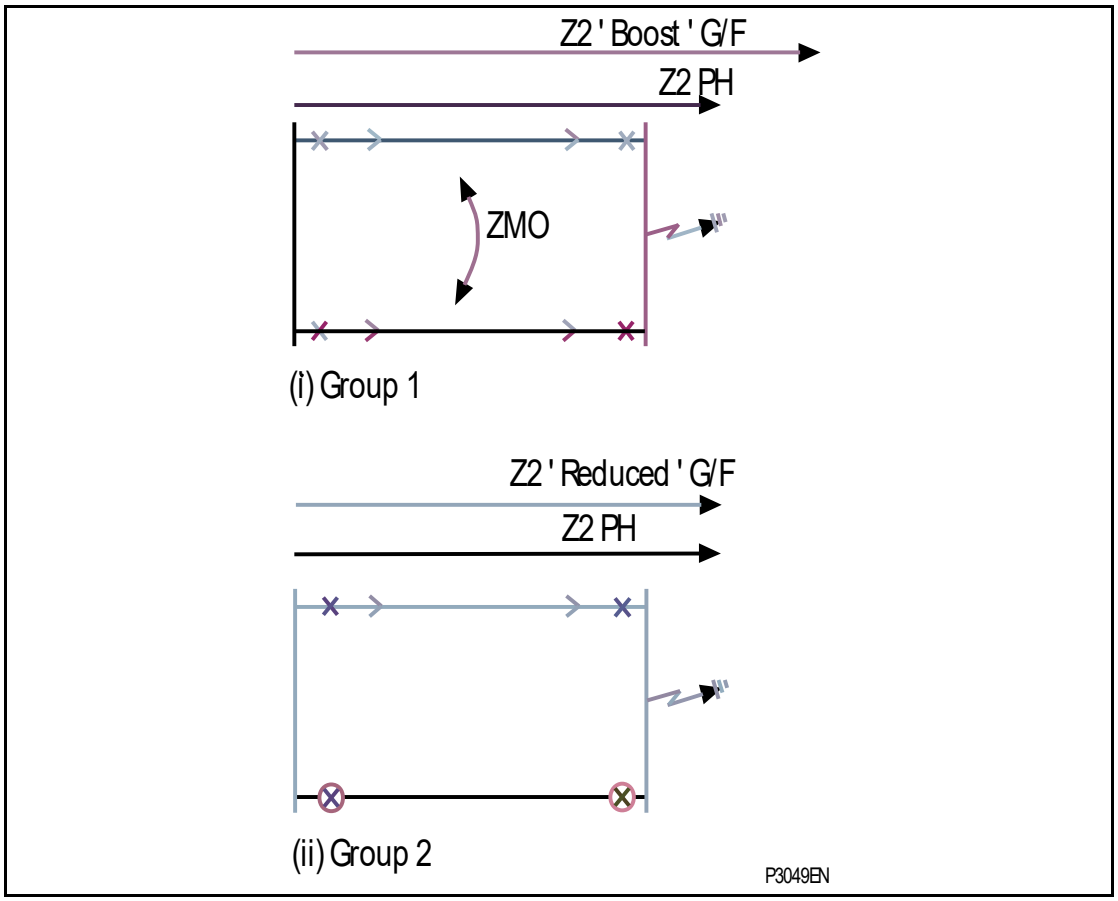


Figure 19: Mutual Coupling example - zone 2 reach considerations

3.1.2.2 Zone setting – KZ Residual compensation for Earth Fault Elements and KZ Angle

The reaches of the earth fault elements use residual compensation of the corresponding phase fault reach. The residual compensation factors are:

- kZ1 - For zone 1 and zone 1X;
- kZ2 - For zone 2;
- kZ3/4 - Shared by zones 3 and 4;
- kZp - For zone p;
- kZq - For zone q.

For earth faults, residual current either measured or derived as the vector sum of phase current inputs (Ia + Ib + Ic) is assumed to flow in the residual path of the earth loop circuit. Therefore, the earth loop reach of any zone must generally be extended by a multiplication factor of (1 + kZ0) compared to the positive sequence reach for the corresponding phase fault element. kZ0 is designated as the residual compensation factor, and is calculated as:

kZ0 Res. Comp, $|kZ0| = (Z_0 - Z_1) / 3.Z_1$ Set as a ratio.

kZ0 Angle, $\angle kZ0 = \angle (Z_0 - Z_1) / 3.Z_1$ Set in degrees.

Where:

Z_1 = Positive sequence impedance for the line or cable;

Z_0 = Zero sequence impedance for the line or cable.

kZ0 CALCULATION DESCRIPTION

If we consider a phase to earth fault AN with analogue values VA and IA.

Using symmetrical components, VA is described as follows:

(1) VA = V1 + V2 + V0 = Z1I1 + Z2I2 + Z0I0

On a line or on a cable, Z2 = Z1. It results:
(2) VA = Z1 (I1 + I2) + Z0I0

We can write also: IA = I1 + I2 + I0
(3) (I1 + I2) = IA – I0

If equation (3) is combined with equation (2), we obtain:
(4) VA = Z1 (IA – I0) + Z0I0

The physical fault current is IR = 3I0. The equation (4) becomes:
VA = Z1 [IA – IR/3 + Z0IR/3Z1] = Z1 [IA + IR (Z0–Z1)/3Z1]

With: (Z0 – Z1)/3Z1 = kZ0
(5) VA = Z1 [IA + kZ0 IR]
(6) Z1 = VA/(IA + kZ0 IR)

Special cases:

Resistive fault where:
Rfault = fault resistance (loop) (Rfault = Rloop)
Ifault: current crossing the fault resistance

(7) VA = Z1 [IA + kZ0 IR] + Rfault . Ifault

(8) Z1 = (VA – Rfault . Ifault) / (IA + kZ0 IR)

Open line (Ifault = IR = IA):

(9) VA = Z1 . IA (1 + kZ0) + Rfault . IA

(10) Z1 = (VA / IA – Rfault) / (1 + kZ0)

The detected impedance will be:
Z = Z1 (1 + kZ0) + Rfault

This is the form used for the result of Z measured with an injector providing U, I, φ

Separate compensation for each zone (KZ1, KZ2, KZ3/4, KZp and KZq) allows more accurate earth fault reach control for elements which are set to overreach the protected line, such that they cover other circuits that may have different zero sequence to positive sequence impedance ratios (example: underground cable and overhead line in the protected line).

3.1.2.3 Zone setting – Z

All phase or earth fault protection elements are quadrilateral shaped, and are directionalised as follows:

- Zones 1, 2 and 3 - Directional forward zones, as used in conventional three zone distance schemes. Note that Zone 1 can be extended to Zone 1X when required in zone 1 extension schemes.
- Zone p and q - Programmable. Selectable (Distance scheme\Fault type) as a directional forward or reverse zone.
- Zone 4 - Directional reverse zone. Note that zone 3 and zone 4 can be set with same Rloop value to provide a general start of the relay.

  Note: If any zone i presents an Rloop i greater than R3=R4, the limit of the start is always given by R3. See also the "Commissioning Test" section.

3.1.2.4 Zone setting – Resistive reach calculation

3.1.2.4.1 Resistive reach calculation – Phase fault Element



Resistances are set per loop

The P442 and P444 relays have quadrilateral distance elements therefore the resistive reach (RPh) is set independently of the impedance reach along the protected line/cable. RPh defines the maximum amount of fault resistance additional to the line impedance for which a distance zone will trip, regardless of the location of the fault within the zone. Therefore, the

right hand and left hand resistive reach constraints of each zone are displaced by +RPh and -RPh either side of the characteristic impedance of the line, respectively. RPh is generally set on a per zone basis, using R1Ph, R2Ph, RpPh and RqPh. Note that zones 3 and 4 share the resistive reach R3Ph-R4Ph.

When the relay is set in primary impedance terms, RPh must be set to cover the maximum expected phase-to-phase fault resistance. In general, RPh must be set greater than the maximum fault arc resistance for a phase-phase fault, e.g. calculated as follows:

$R_a = (28710 \times L) / I_f^{1.4}$

$RPh \geq R_a$

Where:

I_f = Minimum expected phase-phase fault current (A);

L = Maximum phase conductor spacing (m);

R_a = Arc resistance, calculated from the van Warrington formula (Ω).

Typical figures for R_a are given in Table 2 below, for different values of minimum expected phase fault current.

Conductor spacing (m)	Typical system voltage (kV)	I_f = 1kA	I_f = 5kA	I_f = 10kA
2	33	3.6 Ω	0.4 Ω	0.2 Ω
5	110	9.1 Ω	1.0 Ω	0.4 Ω
8	220	14.5 Ω	1.5 Ω	0.6 Ω

Table 2: Typical arc resistances calculated using the Van Warrington formula

The maximum phase fault resistive reach must be limited to avoid load encroachment trips. Therefore, R3Ph and other phase fault resistive reach settings must be set to avoid the heaviest allowable loading on the feeder. An example is shown in Figure 20 below, where the worst case loading has been determined as point "Z", calculated from:

Impedance magnitude, $|Z| = kV^2 / MVA$

Leading phase angle, $\angle Z = \cos^{-1}(PF)$

Where:

kV = Rated line voltage (kV);

MVA = Maximum loading, taking the short term overloading during out ages of parallel circuits into account (MVA);

PF = Worst case lagging power factor.

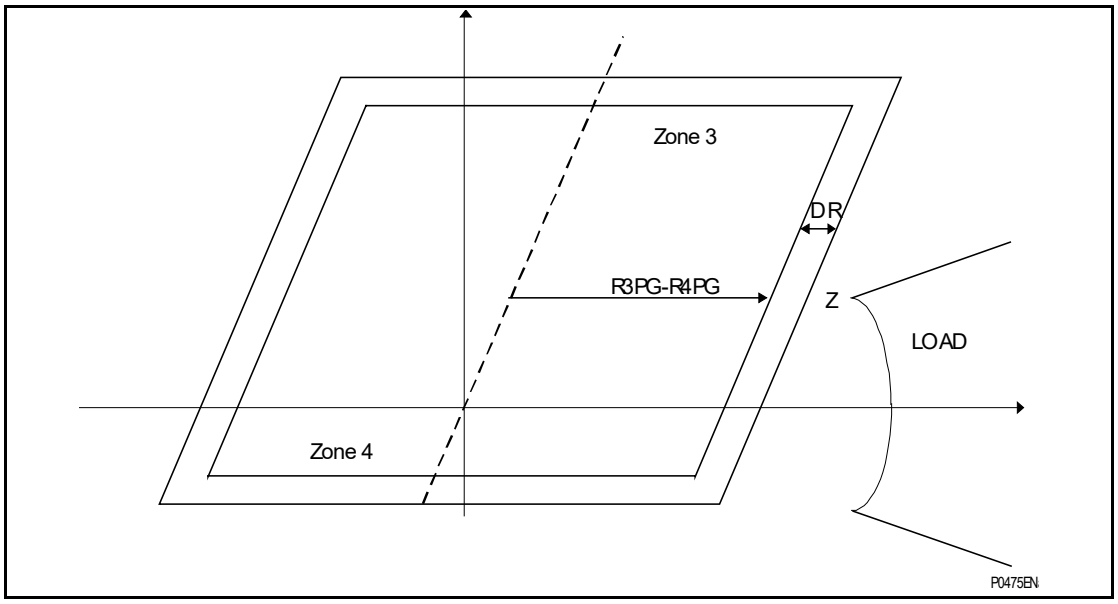


Figure 20: Resistive reaches for load avoidance

As shown in the Figure, R3Ph-R4Ph is set such as to avoid point Z by a suitable margin. Zone 3 must never reach more than 80% of the distance from the line characteristic impedance (shown dotted), towards Z. However, where power swing blocking is used, a larger impedance (including ∆R) characteristic surrounds zones 3 and 4, and it is essential also that load does not encroach upon this characteristic. For this reason, R3Ph would be set ≤ 60% of the distance from the line characteristic impedance towards Z. A setting between the calculated minimum and maximum should be applied.

R/Z ratio: For best zone reach accuracy, the resistive reach of each zone would not normally be set greater than 10 times the corresponding zone reach. This avoids relay overreach or underreach where the protected line is exporting or importing power at the instant of fault inception. The resistive reach of any other zone cannot be set greater than R3Ph, and where zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, the zone 2 elements used in the scheme must satisfy R2Ph ≤ (R3Ph-R4Ph) x 80%.

3.1.2.4.2 Resistive reach calculation – Earth fault Element

The resistive reach setting of the relay earth fault elements (RG) should be set to cover the desired level of earth fault resistance, but to avoid operation with minimum load impedance. Fault resistance would comprise arc-resistance and tower footing resistance. In addition, for best reach accuracy, the resistive reach of any zone of the relay would not normally be greater than 10 times the corresponding earth loop reach.

EXPERT SECTION

As shown in Figure 20, R3G – R4G is set such as to avoid point Z (minimum load impedance) by a suitable margin.

$$R3G - R4G \leq 80\% \; Z \text{ minimum load impedance}$$

$$\leq 80\% \; \frac{Umin/\sqrt{3};1}{2 \times Imax}$$

- Vmin: minimum phase/phase voltage in normal conditions without fault
- Imax: maximum load current in normal conditions without fault

However, where Power swing blocking is used, a larger impedance surrounds zone 3 and zone 4, and it is also essential for the load not to encroach upon the characteristic.

The earth detection criteria (10% IN + 5% IphaseMax) blocks the relay starting if residual current is not detected (it secures the relay in case of load encroachment for Delta algorithms).

When Phase-Phase detectors are used, phase ground start could be higher compared to previous version, because ∆R is only applied to the phase-phase loops.

$[(R3G - R4G) - \Delta R] \leq 80\%$ Z min load

With $\Delta R = 0{,}032 \times \Delta f \times R$ load min
Δf: power swing frequency
R load min: minimum load resistance

A typical resistive reach coverage would be 40 Ω on the primary system. The same load impedance as in section 3.1.2.4.1 must be avoided. Therefore R3G is set such as to avoid point Z by a suitable margin. Zone 3 must never reach more than 80% of the distance from the line characteristic impedance (shown as dotted line in Figure 20), towards Z.

For high resistance earth faults, the situation may arise where no distance elements could operate. In this case it will be necessary to provide supplementary earth fault protection, for example using the relay Channel Aided DEF protection.

3.1.2.5 Zone setting – Zone time delay

(initiated with CVMR (General Start Convergency))

- The zone 1 time delay (tZ1) is generally set to zero, giving instantaneous operation. However, a time delay might be employed in cases where a large transient DC component is expected in the fault current, and older circuit breakers may be unable to break the current until zero crossings appear.
- The zone 2 time delay (tZ2) is set to co-ordinate with zone 1 fault clearance time for adjacent lines. The total fault clearance time will consist of the downstream zone 1 operating time plus the associated breaker operating time. Allowance must also be made for the zone 2 elements to reset following clearance of an adjacent line fault and also for a safety margin. A typical minimum zone 2 time delay is of the order of 200 ms. This time may have to be adjusted where the relay is required to grade with other zone 2 protection or slower forms of back-up protection for adjacent circuits.
- The zone 3, zone P or zone Q time delays (tZ3, tZp, tZq) are typically set with the same considerations made for the zone 2 time delay, except that the delay needs to coordinate with the downstream zone 2 fault clearance (or reverse busbar protection fault clearance). A typical minimum operating time would be about 400 ms. Again, this may need to be modified to co-ordinate with slower forms of back-up protection for adjacent circuits.
- The zone 4 time delay (tZ4) needs to co-ordinate with any protection for adjacent lines in the relay's reverse direction. If zone 4 is required merely for use in a Blocking scheme, tZ4 may be set high.

  Remark: The DDBs corresponding to "tZi" (for zone i) time-delays are noted "Ti" in the PSL.

The following conventional rules are applied:

- Distance timers are initiated as soon as the relay has picked up – CVMR pickup distance (**CVMR = Start & Convergence**)
- The minimum tripping time even with carrier receive is T1.
  This applies only for standard distance scheme, while in teleprotection schemes minimum tripping time is separately settable.
- Zone 4 is always reverse

3.1.3 Fault locator

The relay has an integral fault locator that uses information from the current and voltage inputs to provide a distance to fault measurement. When the fault calculation is complete the fault location information is available in the relay fault record.

When applied to parallel circuits, mutual flux coupling (section 3.1.2.1.3) can alter the impedance seen by the fault locator. The coupling will contain positive, negative and zero sequence components. In practice the positive and negative sequence coupling is insignificant. The effect on the fault locator of the zero sequence mutual coupling can be eliminated by using the mutual compensation feature provided. This requires that the

residual current on the parallel line is measured. It is extremely important that the polarity of connection for the mutual CT input is correct, as shown.

The system assumed for the distance protection worked example will be used here, refer to section 3.3. The Green Valley – Blue River line is considered.

Line length: 100 km

CT ratio: 1 200 / 5

VT ratio: 230 000 / 115

Line impedances: Z_1 = 0.089 + j0.476 = 0.484 / 79.4° Ω/km

ZM_0 = 0.107 + j0.571 = 0.581 / 79.4° Ω/km (Mutual)

Ratio of secondary to primary impedance = $\frac{1200/5}{230000/115}$ = 0.12

Line Impedance = 100 x 0.484 / 79.4° x 0.12

= 5.81 / 79.4° Ω secondary.

Relay Line Angle settings 0° to 360° in 1° steps. Therefore, select Line Angle = 80° for convenience.

Therefore set **Line Impedance and Line Angle: = 5.81 / 80° Ω** (secondary).

No residual compensation needs to be set for the fault locator, as the relay automatically uses the kZ0 factor applicable to the distance zone which tripped.

Should a CT residual input be available for the parallel line, mutual compensation could be set as follows:

kZm Mutual Comp, $|kZm| = ZM_0 / 3.Z_1$ Ie: As a ratio.

kZm Angle, $\angle kZm = \angle ZM_0 / 3.Z_1$ Set in degrees.

The CT ratio for the mutual compensation may be different from the Line CT ratio. However, for this example we will assume that they are identical.

$kZm = ZM_0 / 3.Z_1$ = 0.581 / 79.4° / (3 x 0.484 / 79.4°)

= 0.40 / 0°

Therefore set **kZm Mutual Comp** = 0.40

kZm Angle = 0°

3.2 Channel Aided distance schemes

The following diagram gives the logic of the distance protection:

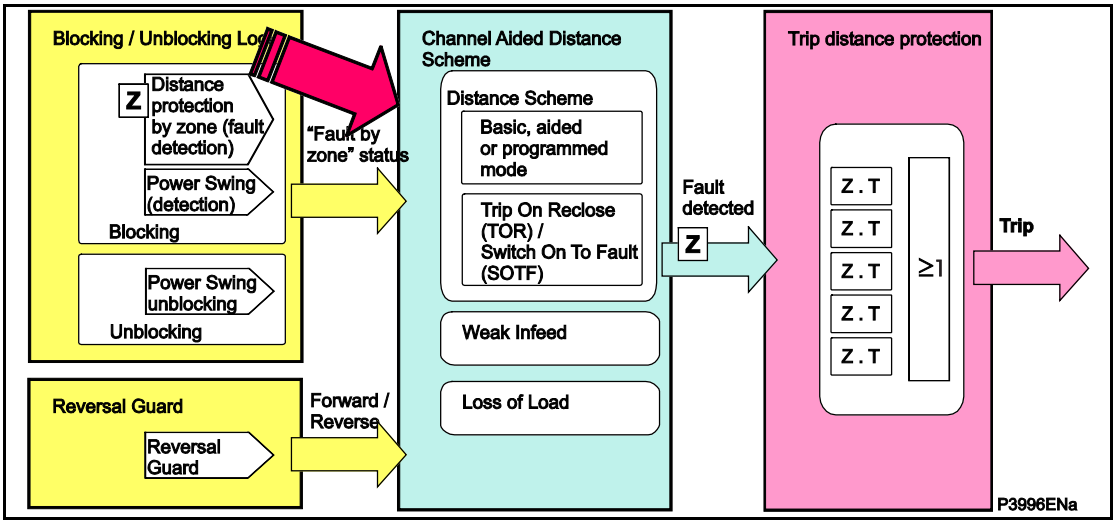


Figure 21: Channel aided distance scheme in the distance protection diagram

This section details the “Channel Aided Distance schem” path.

The blocking / unblocking logic with power swing manages the distance protection logic.

- If enabled, the unblocking function carries out a function similar to Carrier receive logic,
- Weak infeed allows for the case where there may be no zone pick up from local end,
- TOR & SOTF (Trip On Reclose and Switch On To Fault) applies specific logic in case of manual closing or AR closing logic,
- Trip Distance Protection issues the trip order according to the distance algorithm outputs, the type of trip 1P (1-phase) or 3P (3-phases), the distance timers, and the logic data such as power swing blocking,
- Loss of Load manages a specific logic for tripping 3P in accelerated Z2 in the absence of a carrier,

This section details the scheme configuration of the distance protection.

3.2.1 Standard Scheme

The following channel aided distance tripping schemes are available when the Standard program mode is selected:

- Basic (+ zone 1 extended) schemes,
- Permissive Underreach Transfer Trip Schemes PUP Z2 and PUP Fwd;
- Permissive Overreach Transfer Trip Schemes POP Z2 and POP Z1;
- Weak infeed logic to supplement permissive overreach schemes;
- Unblocking logic to supplement permissive schemes;
- Blocking Schemes BOP Z2 and BOP Z1;
- Current reversal guard logic to prevent maloperation of any overreaching zone used in a channel aided scheme, when fault clearance is in progress on the parallel circuit of a double circuit line.

3.2.1.1 Standard Mode: Basic

The Basic distance scheme is suitable for applications where no signalling channel is available. Zones 1, 2 and 3 are set as described in this section. In general, zones 1 and 2

provide main protection for the line or cable as shown in Figure 22 below, with zone 3 reaching further to provide back up protection for faults on adjacent circuits.

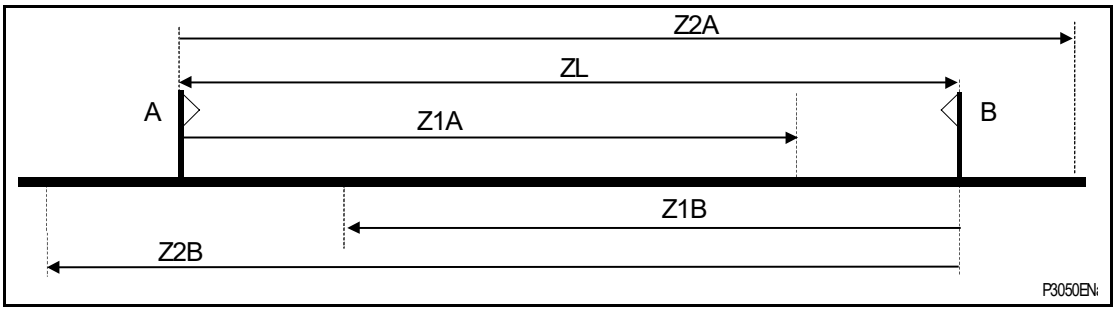


Figure 22: Main protection in the basic scheme (no requirement for signalling channel)

Key:

A, B = Relay locations;

ZL = Impedance of the protected line.

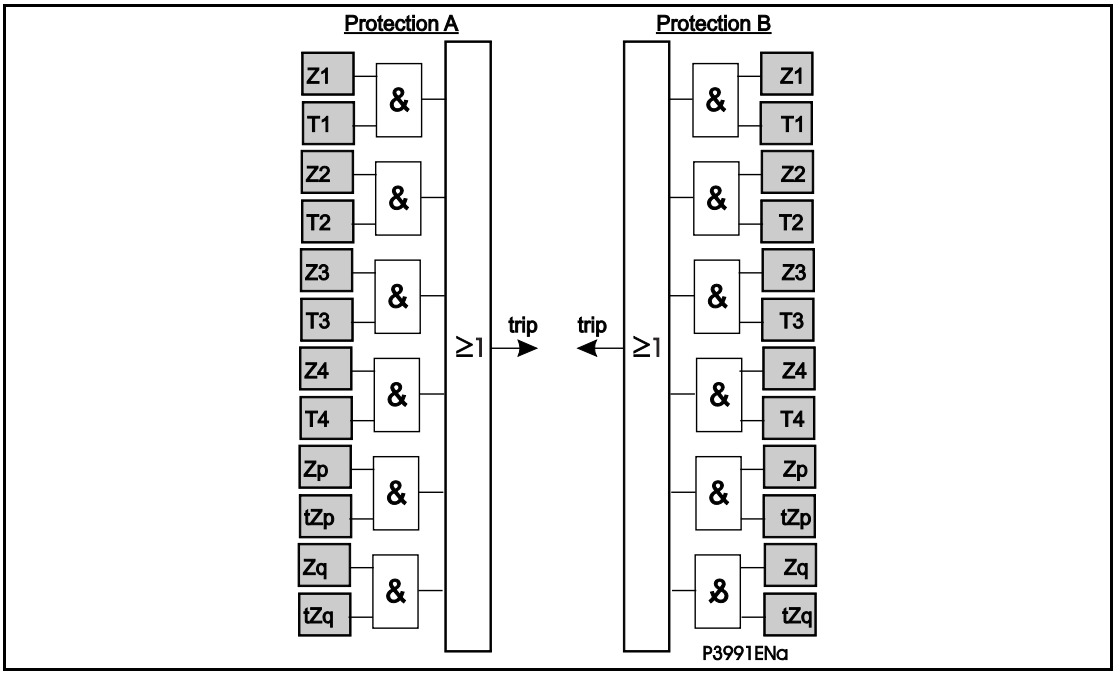


Figure 23: Logic diagram for the basic scheme

Figure 23 shows the tripping logic for the Basic scheme. Note that for the P442 and P444 relays, Zone time-delays are started at the instant of fault detection (T1 to T4, tZp and tZq start at the end of this time delay). Protection zones are stabilised to avoid maloperation for transformer magnetising inrush current. The method used to achieve stability is based on second harmonic current detection.

The Basic scheme incorporates the following features:

- Instantaneous zone 1 tripping. Alternatively, zone 1 can have an optional time delay of 0 to 10 s.
- Time delayed tripping by zones 2, 3, 4, p and q. Each with a time delay set between 0 and 10 s.

The Basic scheme is suitable for single or double circuit lines fed from one or both ends. The limitation of the Basic scheme is that faults in the end 20% sections of the line will be cleared after the zone 2 time delay. Where no signalling channel is available, then improved fault clearance times can be achieved through the use of a zone 1 extension scheme or by using loss of load logic, as described below. Under certain conditions however, these two schemes

will still result in time delayed tripping. Where high speed protection is required over the entire line, then a channel aided scheme will have to be employed.

3.2.1.2 Permissive Underreach Transfer Trip Schemes PUP Z2 and PUP Fwd

To provide fast fault clearance for all faults, both transient and permanent, along the length of the protected circuit, it is necessary to use a signal aided tripping scheme. The simplest of these is the permissive underreach protection scheme (PUP), of which two variants are offered in the P442 and P444 relays. The channel for a PUP scheme is keyed by operation of the underreaching zone 1 elements of the relay. If the remote relay has detected a forward fault upon receipt of this signal, the relay will operate with no additional delay. Faults in the last 20% of the protected line are therefore cleared with no intentional time delay.

Listed below are some of the main features/requirements for a permissive underreaching scheme:

- Only a simplex signalling channel is required.
- The scheme has a high degree of security since the signalling channel is only keyed for faults within the protected line.
- If the remote terminal of a line is open then faults in the remote 20% of the line will be cleared via the zone 2 time delay of the local relay.
- If there is a weak or zero infeed from the remote line end, (ie. current below the relay sensitivity), then faults in the remote 20% of the line will be cleared via the zone 2 time delay of the local relay.
- If the signalling channel fails, Basic distance scheme tripping will be available.

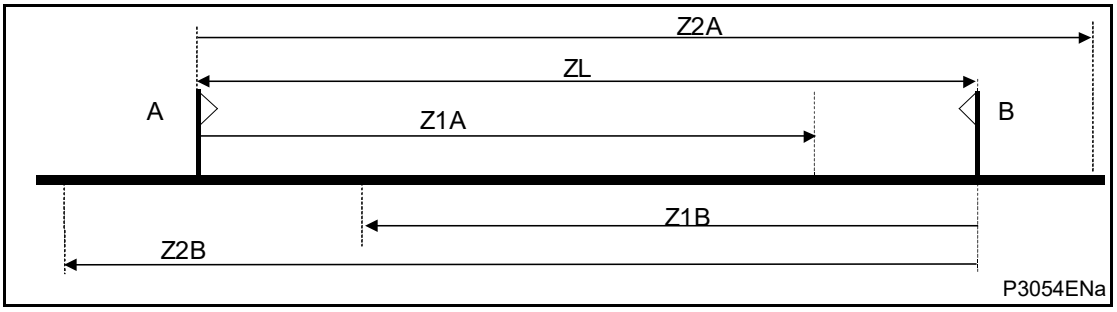


Figure 24: Zone 1 and 2 reaches for permissive underreach schemes

3.2.1.2.1 Permissive Underreach Protection, Accelerating Zone 2 (PUP Z2)

This scheme allows an instantaneous Z2 trip on receipt of the signal from the remote end protection. Figure 25 shows the simplified scheme logic.

Send logic: Zone 1

Permissive trip logic: Zone 2 plus Channel Received.

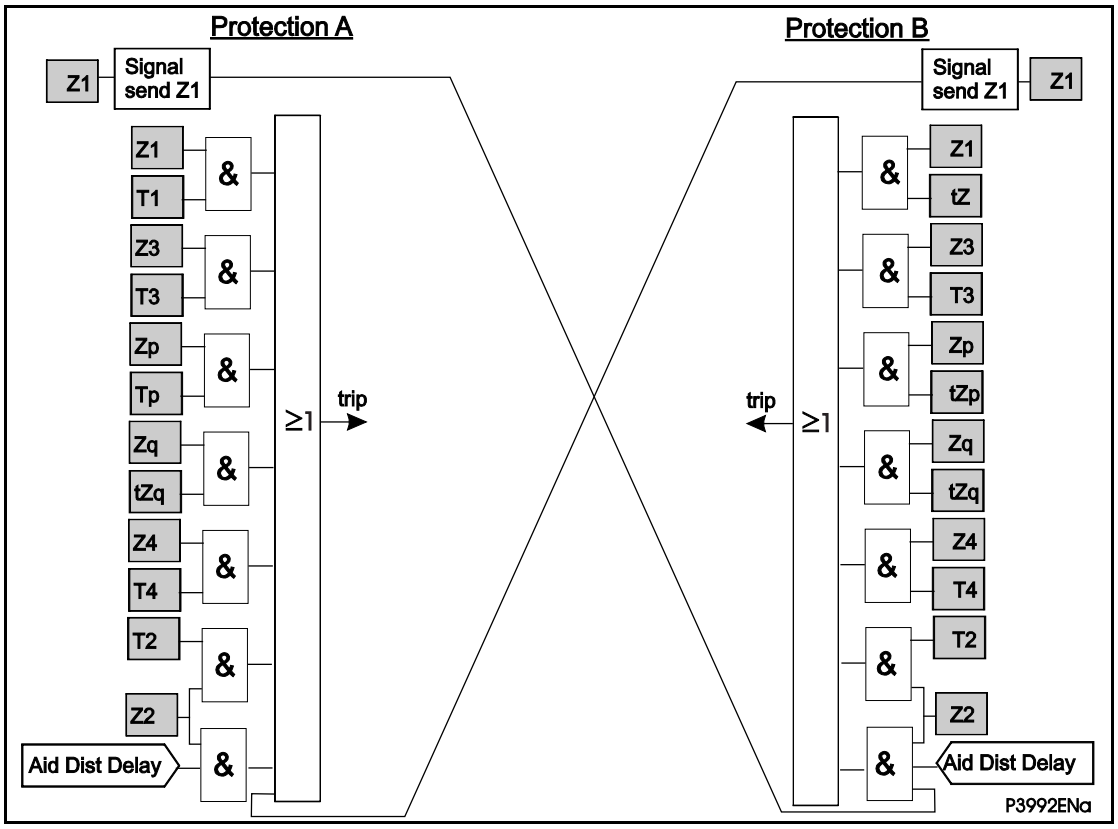


Figure 25: PUP Z2 permissive underreach scheme

Trip logic:

IEC Standard		Carrier Send	Trip Logic	Application	User setting
448.15.13	PUR or AUP	Z1	Z2.CR.'Aid Dist Delay' + Z1.T1 + Z2.T2 + Z3.T3...	Z1 = 80% ZL	PUP Z2

3.2.1.2.2 Permissive Underreach Protection Tripping via Forward Start (PUP Fwd)

This scheme allows an instantaneous Z2 or Z3 trip on receipt of the signal from the remote end protection. Figure 26 shows the simplified scheme logic.

If the remote relay has picked up in a forward zone and the underimpedance element has started, then it will trip after the transmission time delay ('Distance schemes / Aid Dist Delay' setting) upon reception of the permissive signal from the other end of the line.

Send logic: Zone 1

Permissive trip logic: Underimpedance Start within any Forward Distance Zone, plus Channel Received.

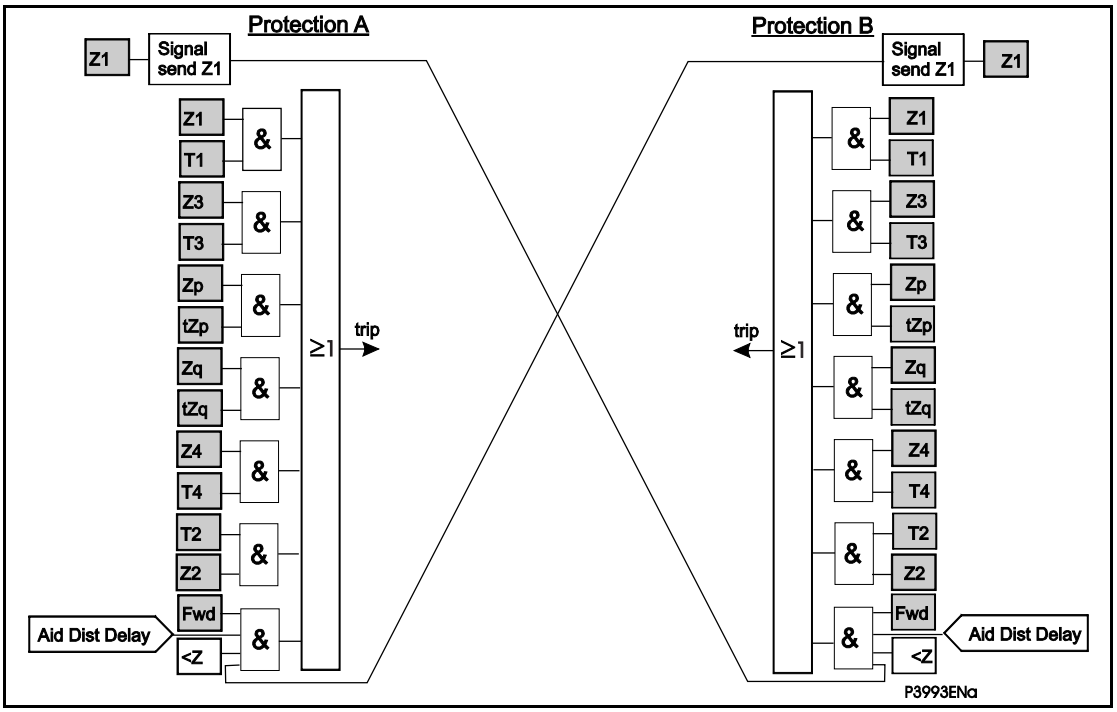


Figure 26: PUP fwd permissive underreach scheme

Key:

Fwd = Forward fault detection (DDB: '**Dist Fwd**' or '**DEF Fwd**');

<Z = Underimpedance Started: Z2 or Z3.

Trip logic:

IEC Standard		Carrier Send	Trip Logic	Application	User setting
448.15.11	PUP or PUTT	Z1	Fwd.CR.'Aid Dist Delay' + Z1.T1 + Z2.T2 +...	Z1 = 80% ZL	PUP Fwd

3.2.1.3 Permissive Overreach Transfer Trip Schemes POP Z2 and POP Z1

The P442 and P444 relays offer two variants of permissive overreach protection schemes (POP), having the following common features/requirements:

- The scheme requires a duplex signalling channel to prevent possible relay maloperation due to spurious keying of the signalling equipment. This is necessary because the signalling channel is keyed for faults external to the protected line.
- The POP Z2 scheme may be more advantageous than permissive underreach schemes for the protection of short transmission lines, since the resistive coverage of the Zone 2 elements may be greater than that of the Zone 1 elements.
- Current reversal guard logic is used to prevent healthy line protection maloperation for the high speed current reversals experienced in double circuit lines, caused by sequential opening of circuit breakers.
- If the signalling channel fails, Basic distance scheme tripping will be available.

3.2.1.3.1 Permissive Overreach Protection with Overreaching Zone 2 (POP Z2)

Figure 27 shows the zone reaches, and Figure 28 the simplified scheme logic. The signalling channel is keyed from operation of the overreaching zone 2 elements of the relay. If the remote relay has picked up in zone 2, then it will operate with no additional delay upon receipt of this signal. The POP Z2 scheme also uses the reverse looking zone 4 of the relay as a reverse fault detector. This is used in the current reversal logic and in the optional weak infeed echo feature.

The signaling channel is keyed from operation of zone 2 elements of the relay. If the remote relay has picked up in zone 2, then it will operate with Transmission Time ('Distance schemes / Aid Dist Delay') delay on reception of the permissive signal.

Send logic:	Zone 2
Permissive trip logic:	Zone 2 plus Channel Received.

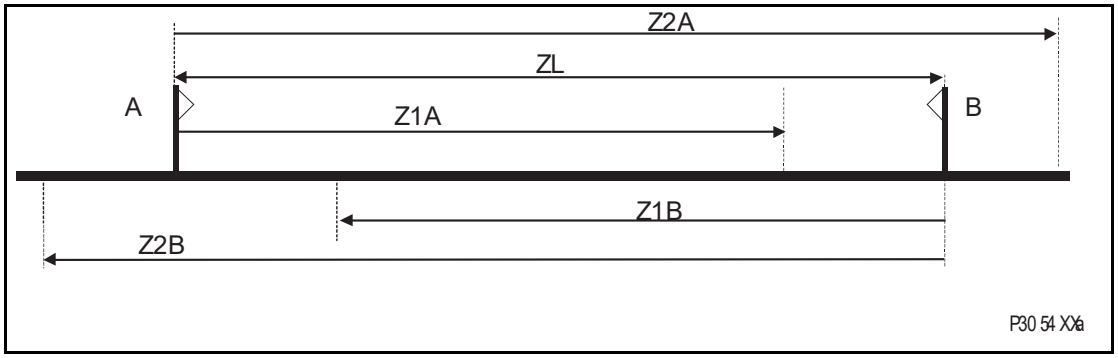


Figure 27: Main protection in the POP Z2 scheme

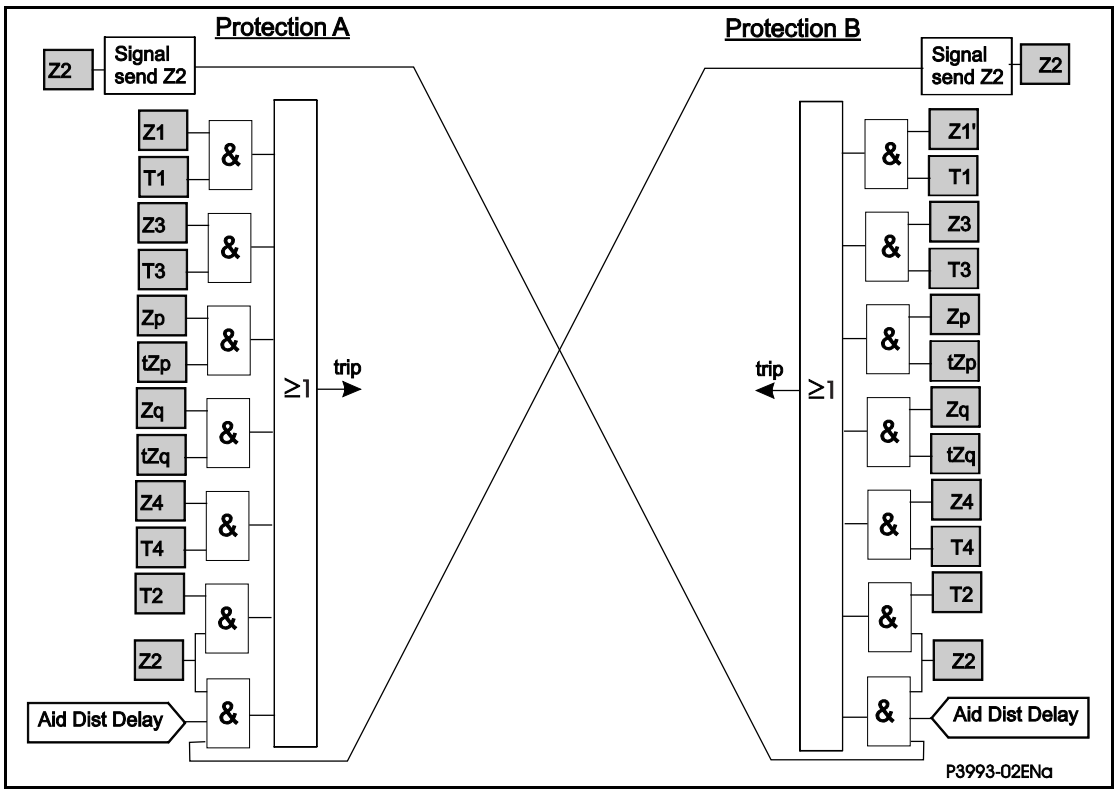


Figure 28: Logic diagram for the POP Z2 scheme

Trip logic:

IEC Standard		Carrier Send	Trip Logic	Application	User setting
	PUR2 or POR2	Z2	Z2.CR.'Aid Dist Delay' + Z1.T1 + Z2.T2 + Z3.T3...	Z1 = 80% ZL	POP Z2

3.2.1.3.2 Permissive Overreach Protection with Overreaching Zone 1 (POP Z1)

Figure 29 shows the zone reaches, and Figure 30 the simplified scheme logic. The signalling channel is keyed from operation of zone 1 elements set to overreach the protected line. If the remote relay has picked up in zone 1, then it will operate with no additional delay upon receipt of this signal. The POP Z1 scheme also uses the reverse looking zone 4 of the relay

as a reverse fault detector. This is used in the current reversal logic and in the optional weak infeed echo feature.

> *Note: Should the signalling channel fail, the fastest tripping in the Basic scheme will be subject to the tZ2 time delay.*

The signaling channel is keyed from operation of zone 1 elements set to overreach the protected line. If the remote relay has picked up in zone 1, then it will operate with Transmission Time ('Distance schemes / Aid Dist Delay') delay upon reception of the permissive signal.

Send logic: Zone 1

Permissive trip logic: Zone 1 plus Channel Received.

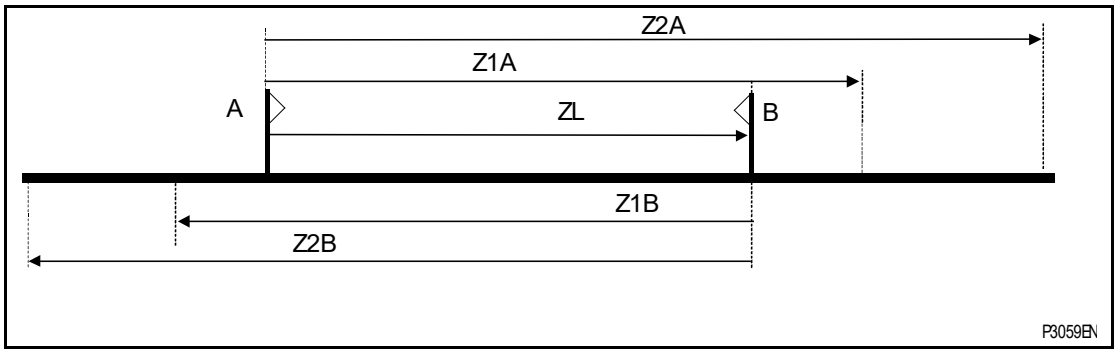


Figure 29: Main protection in the POP Z1 scheme

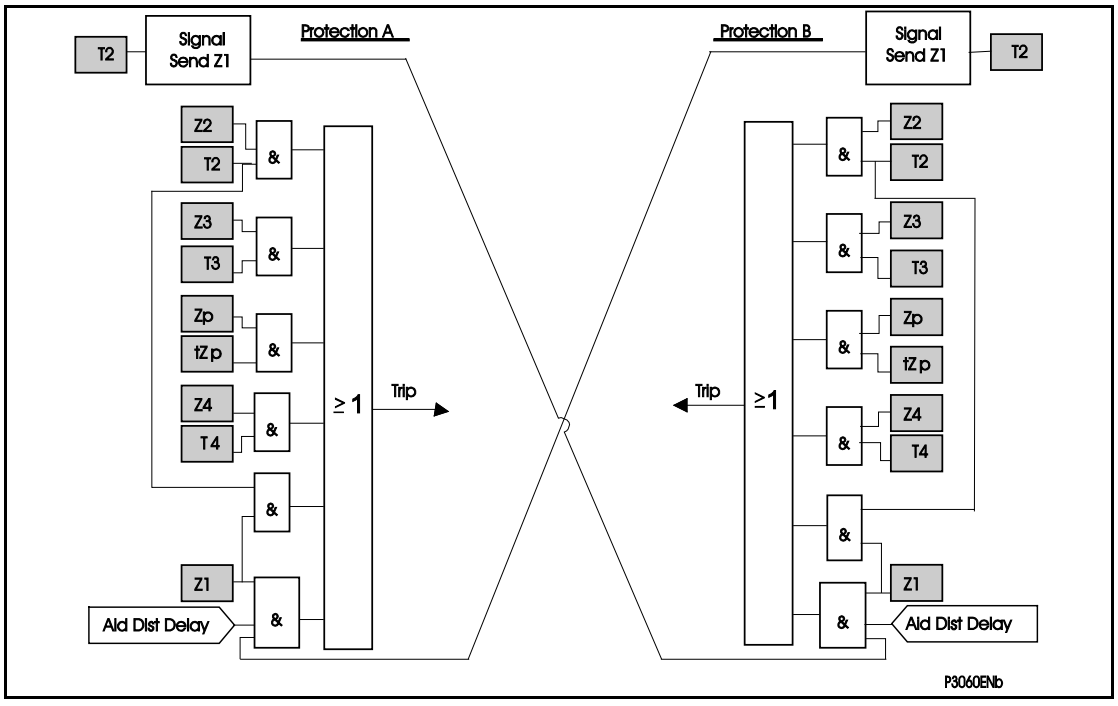


Figure 30: Logic diagram for the POP Z1 scheme

Trip logic:

IEC Standard		Carrier Send	Trip Logic	Application	User setting
448.15.16	POR1 or POP or POTT	Z1	Z1.CR.'Aid Dist Delay' + Z1.T2 + Z2.T2 + Z3.T3...	Z1 > ZL	POP Z1

3.2.1.4 Blocking Schemes BOP Z2 and BOP Z1

The P442 and P444 relays offer two variants of blocking overreach protection schemes (BOP). With a blocking scheme, the signalling channel is keyed from the reverse looking zone 4 element, which is used to block fast tripping at the remote line end. Features are as follows:

- BOP schemes require only a simplex signalling channel.
- Reverse looking Zone 4 is used to send a blocking signal to the remote end to prevent unwanted tripping.
- When a simplex channel is used, a BOP scheme can easily be applied to a multi-terminal line provided that outfeed does not occur for any internal faults.
- The blocking signal is transmitted over a healthy line, and so there are no problems associated with power line carrier signalling equipment.
- BOP schemes provide similar resistive coverage to the permissive overreach schemes.
- Fast tripping will occur at a strong source line end, for faults along the protected line section, even if there is weak or zero infeed at the other end of the protected line.
- If a line terminal is open, fast tripping will still occur for faults along the whole of the protected line length.
- If the signalling channel fails to send a blocking signal during a fault, fast tripping will occur for faults along the whole of the protected line, but also for some faults within the next line section.
- If the signalling channel is taken out of service, the relay will operate in the conventional Basic mode.
- A current reversal guard timer is included in the signal send logic to prevent unwanted trips of the relay on the healthy circuit, during current reversal situations on a parallel circuit.
- To allow time for a blocking signal to arrive, a short time delay on aided tripping, Aided distribution transmission delay time, must be used, as follows:

Recommended 'Aid Dist Delay' setting: Max. signalling channel operating time + 14ms

3.2.1.4.1 Blocking Overreach Protection with Overreaching Zone 1 (BOP Z1)

This scheme is similar to that used in the Alstom Grid EPAC and PXLN relays. Figure 31 shows the zone reaches, and Figure 32 the simplified scheme logic. The signalling channel is keyed from operation of the reverse zone 4 elements of the relay. If the remote relay has picked up in overreaching zone 1, then it will operate after the Transmission Time ('Distance schemes / Aid Dist Delay') time-delay if no block is received.

Note:	*The fastest tripping is always subject to the aided distance time-delay ('Aid Dist Delay').*

Send logic: Reverse Zone 4

Trip logic: Zone 1, plus Channel NOT Received, delayed by 'Aid Dist Delay'.

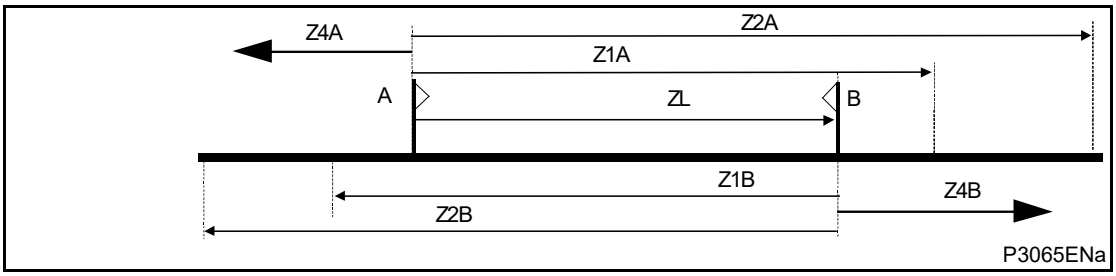


Figure 31: Main protection in the BOP Z1 scheme

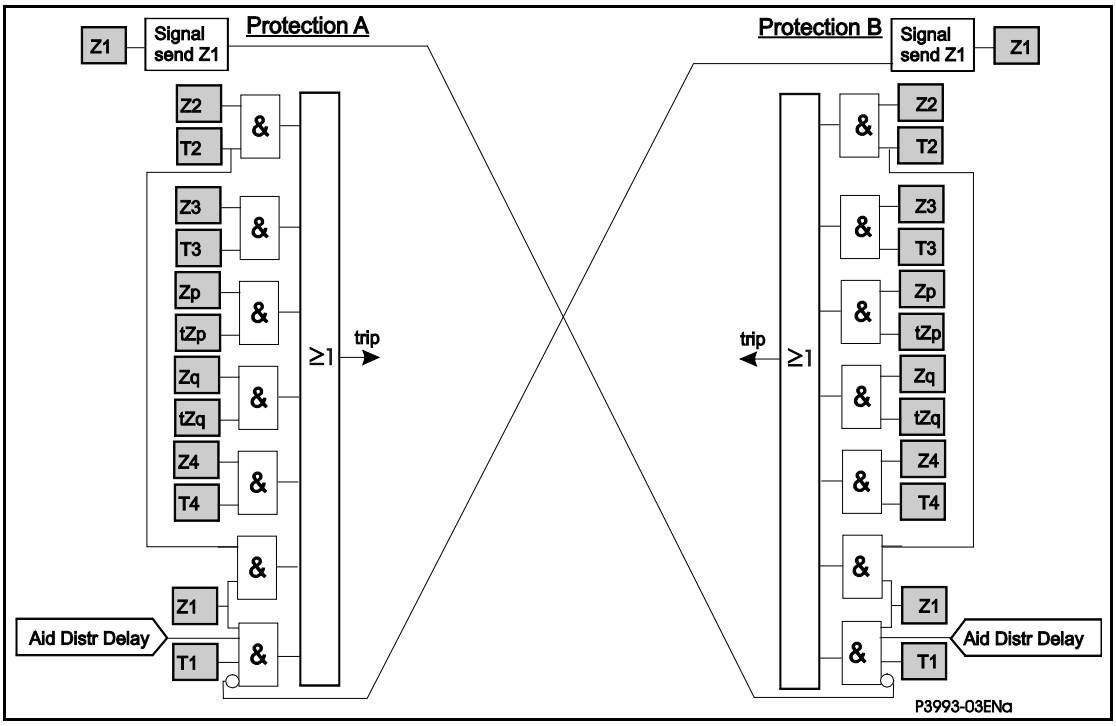


Figure 32: Logic diagram for the BOP Z1 scheme

Trip logic:

IEC Standard		Carrier Send	Trip Logic	Application	User setting
448.15.14	BOR1 or BOP	Z4	Z1. $\overline{CR}$ .T1.'Aid Dist Delay' + Z1.T2 + Z2.T2 + Z3.T3...	Z1 > ZL	BOP Z1

3.2.1.4.2 Blocking Overreach Protection with Overreaching Zone 2 (BOP Z2)

Figure 33 shows the zone reaches, and Figure 34 the simplified scheme logic. The signalling channel is keyed from operation of the reverse zone 4 elements of the relay. If the remote relay has picked up in zone 2, then it will operate after the aided distribution time-delay if no block is received.

Send logic: Reverse Zone 4

Trip logic: Zone 2, plus Channel NOT Received, delayed by 'Aid Dist Delay'.

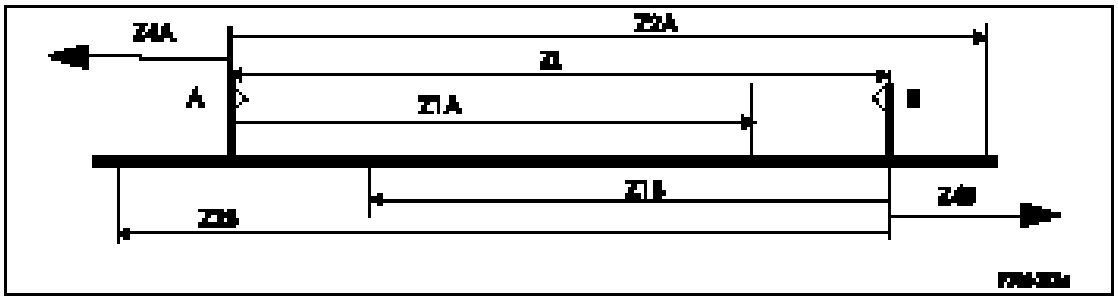


Figure 33: Main protection in the BOP Z2 scheme

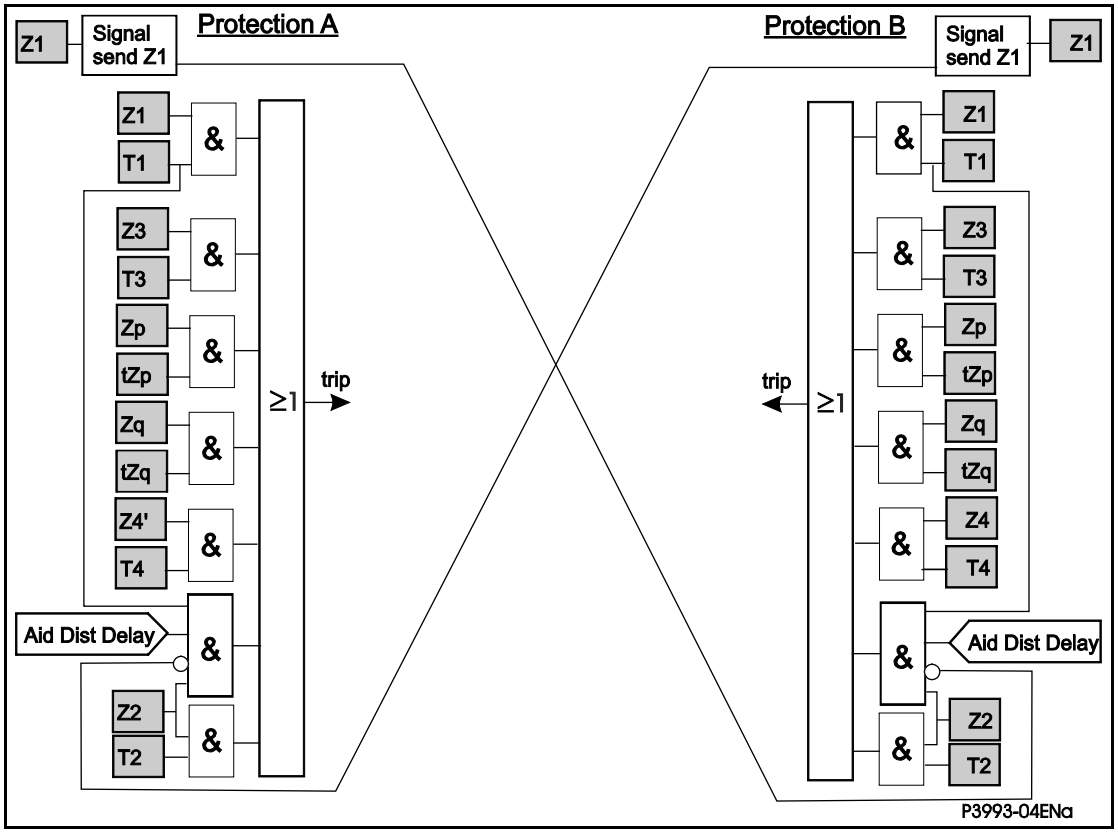


Figure 34: Logic diagram for the BOP Z2 scheme

Trip logic:

IEC Standard		Carrier Send	Trip Logic	Application	User setting
	BOR2 or BLOCK2	Z4	Z2. $\overline{CR}$ .T1. 'Aid Dist Delay' + Z1.T1 + Z2.T2 + Z3.T3...	Z1 = 80% ZL	BOP Z2

3.2.2 Trip Mode

The tripping mode is settable using the three following modes:



- **Force 3 Poles**: three-pole trip (in all cases)
- **1 Pole Z1 & CR**: single pole trip at T1 when a fault is detected in zone 1 (Z1) or at CR (Carrier Receive) reception. Otherwise, three pole trip.
- **1 Pole Z1 Z2 & CR**: single pole trip at T1 when a fault is detected in zone 1 (Z1) or in zone 2, or at CR (Carrier Receive) reception. Otherwise, three pole trip.

The following table summarizes the tripping zones:

Tripping mode	T1	T2	Tzp	T3	T4
1 Pole Z1 Z2 & CR	1P	1P	3P	3P	3P
1 Pole Z1 & CR	1P	3P	3P	3P	3P
Force 3 Poles	3P	3P	3P	3P	3P

1P: 1-pole trip, 3P: 3-pole trip.
T1…T4: End of distance time-delay for the zone

Several preset aided trip logic schemes can be selected or an open logic scheme can be designed by user.

3.2.3 Carrier send Zone (open scheme)

When a fault is detected in zone 1 or zone 2, the CsZ1 or CsZ2 (Carrier Sent by Zone 1 or 2) signal is emitted from the zone to the relay. As shown in the following zone logic configuration diagram, zone 4, behind the relay, will provide a reverse directional decision faster than zone 2. So, the CsZ4 signal used for Carrier Send mode is a reverse signal.

The zone decision logic is described as below:

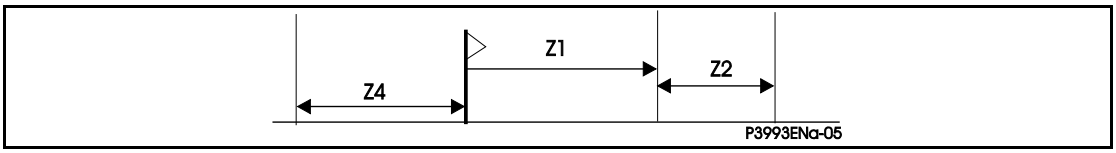


Figure 35: "Carrier SenD" zones

When a scheme is required which is not covered in the Standard modes above, the Open programming mode can be selected. The user then has the facility to decide which distance relay zone is to be used to key the signal, and what type of aided scheme runs when the signal is received.

Setting	Signal Send Zone	Function
None	No Signal Send	To configure a Basic scheme.
CsZ1	Zone 1	To configure a Permissive scheme.
CsZ2	Zone 2	To configure a Permissive scheme.
CsZ4	Zone 4	To configure a Blocking scheme.

Table 3: Carrier send zones in open schemes

Carrier send can be triggered by Zone1 (CsZ1), Zone2 (CsZ2) or Zone4 (Reverse, CsZ4). The following decision logic

The "carrier send" signal drop off is time-delayed (10ms) to avoid an interaction with zone pick-up.

When activated, Z2 can overlap Z1. The following equation decribes the carrier send (CS) logic, including Weak Infeed Carrier Send (WI_CS) echo:

CS (Main channel Carrier send) = (Z1' + Z2').CsZ2 + Z1'.CsZ1 + Reverse.CsZ4 + WI_CS

Where:

- CsZ1, CsZ2 and CsZ4 = Carrier send for zone 1, zone 2 or zone 4,
- Reverse' = Reverse Fault detected,
- Z1 to Z4 = Zone 1 to 4 decision (blocked by Power swing or Reversal guard),
- WI_CS = Weak infeed carrier send (Echo)

3.2.4 Distance Carrier Received (Dist CR)

The aided scheme options on Distance carrier receipt are shown in the next table:

Setting	Aided Scheme	Function
None	None	To configure a Basic scheme.
PermZ1	To configure a Permissive scheme where Zone 1 can only trip if a Distance Carrier is received.	
PermZ2	To configure a Permissive scheme where Zone 2 can trip without waiting for tZ2 timeout if a Distance Carrier is received.	
PermFwd	To configure a Permissive scheme where any forward distance zone start will cause an aided trip if a Distance Carrier is received.	
BlkZ1	To configure a Blocking scheme where Zone 1 can only trip if a Distance Carrier is NOT received.	
BlkZ2	To configure a Blocking scheme where Zone 2 can trip without waiting for tZ2 timeout if a Distance Carrier is NOT received.	

Table 4: Aided scheme options on distance carrier receipt

3.2.5 Current reversal guard logic

Where appropriate, the tReversal Guard and 'Aid Dist Delay' (transmission time in blocking scheme) time-delays (in the case of a blocking scheme covering the transmission time) settings will appear in the relay menu. Further customising of distance schemes can be achieved using the Programmable Scheme Logic to condition send and receive logic.

For double circuit lines, the fault current direction can change in one circuit when circuit breakers open sequentially to clear the fault on the parallel circuit. The change in current direction causes the overreaching distance elements to see the fault in the opposite direction to the direction in which the fault was initially detected (settings of these elements exceed 150% of the line impedance at each terminal). The race between operation and resetting of the overreaching distance elements at each line terminal can cause the Permissive Overreach, and Blocking schemes to trip the healthy line. A system configuration that could result in current reversals is shown in Figure 36. For a fault on line L1 close to circuit breaker B, as circuit breaker B trips it causes the direction of current flow in line L2 to reverse.

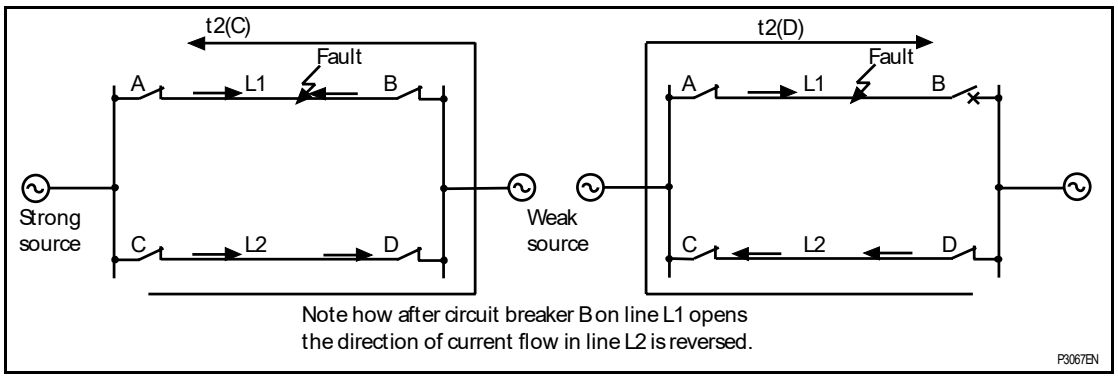


Figure 36: Current reversal in double circuit lines

The basic unblocking / blocking logic scheme is detailed in section 3.5.1.2.

3.2.5.1 Permissive Overreach Schemes Current Reversal Guard

The current reversal guard incorporated in the POP scheme logic is initiated when the reverse looking Zone 4 elements operate on a healthy line. Once the reverse looking Zone 4 elements have operated, the relay's permissive trip logic and signal send logic are inhibited

at substation D (circuit breaker D, Figure 36). The reset of the current reversal guard timer is initiated when the reverse looking Zone 4 resets. A time delay tREVERSAL GUARD is required in case the overreaching trip element at end D operates before the signal sent from the relay at end C has reset. Otherwise this would cause the relay at D to over trip. Permissive tripping for the relays at D and C substations is enabled again, once the faulted line is isolated and the current reversal guard time has expired. The recommended setting is:

tREVERSAL GUARD = Maximum signal reset time + 35 ms.

Note:	*The reverse guard begins when "reverse" falls and not when the directional is reverse and immediately forward. It is validated if the directional becomes forward.*

3.2.5.2 Blocking Scheme Current Reversal Guard

The current reversal guard incorporated in the BOP scheme logic is initiated when a blocking signal is received to inhibit the channel-aided trip. When the current reverses and the reverse looking Zone 4 elements reset, the blocking signal is maintained by the timer tREVERSAL GUARD. The relays in the healthy line are prevented from over tripping because of the sequential opening of the circuit breakers in the faulted line. See Figure 36. After the faulty line is isolated, the reverse-looking Zone 4 elements at substation C –circuit breaker C) and the forward looking elements at substation D will reset. The recommended setting is:

Where Duplex signalling channels are used:
tREVERSAL GUARD = Maximum signalling channel operating time
+ 14 ms.

Where Simplex signalling channels are used:
tREVERSAL GUARD = Maximum signalling channel operating time
- minimum signalling channel reset time
+ 14 ms.

3.2.6 Unblocking logic (permissive scheme)

Two modes of unblocking logic are available with permissive schemes (blocking schemes are excluded).

The unblocking logic issues (see section P44x/EN PL for DDB description):

- The Main and Directional Earth Fault alarm ('**COS alarm**' digital output),
- The internal Carrier Received signal (main distance or Directional Earth Fault unblocking signal) (DDB '**DIST. UNB CR**' or '**DEF. UNB CR**').

The output DDBs '**COS alarm**' and '**DIST.** (or **DEF.**) **UNB CR**' depend on:

- The distance or DEF inputs signals: Carrier Received and Carrier Out of Service inputs,
- distance and DEF channel-aided trip settings,
- Shared or independent logic between the DEF and Distance functions,
- Carrier Out of Service (COS) detected.

Three settings are available in the menu:

- None (basic mode). In this case, the opto input state is copied directly,
- Loss of Guard mode,
- Loss of Carrier mode.

3.2.6.1 None

The Logic equations for this mode are:

'COS alarm' = 'DIST. COS' + 'DEF. COS' (main alarm when carrier is out of service),

'DIST. UNB CR' = 'DIST. Chan Recv' (CR unblocked when "distance carrier received" is present),

'DEF. UNB CR' = 'DEF. Chan Recv' (DEF CR unblocked when "DEF carrier received" is present).

3.2.6.2 Loss of Guard Mode

This mode is designed for use with Frequency Shift Keyed (FSK) power line carrier communications. When the protected line is healthy a guard frequency is sent between line ends, to verify that the channel is in service. However, when a line fault occurs and a permissive trip signal must be sent over the line, the power line carrier frequency is shifted to a new (trip) frequency. Therefore, distance relays should receive either the guard, or trip frequency, but not both together. With any permissive scheme, the Power Line Carrier (PLC) communications are transmitted over the power line that may contain a fault. So, for certain fault types the line fault can attenuate the PLC signals, so that the permissive signal is lost and not received at the other line end. To overcome this problem, when the guard is lost and no "trip" frequency is received, the relay opens a window of time during which the permissive scheme logic acts as though a "trip" signal had been received. Two opto inputs to the relay need to be assigned, one is the Channel Receive opto input, the second is designated Loss of Guard (the inverse function to guard received). The function logic is summarised in Table 5: .

System Condition	Permissive Channel Received	Loss of Guard	Permissive Trip Allowed	Alarm Generated
Healthy Line	No	No	No	No
Internal Line Fault	Yes	Yes	Yes	No
Unblock	No	Yes	Yes, during a 150ms window	Yes, delayed on pickup by 150ms
Signalling Anomaly	Yes	No	No	Yes, delayed on pickup by 150ms

Table 5: Logic for the loss of guard function

The window of time during which the unblocking logic is enabled starts 10ms after the guard signal is lost, and continues for 150 ms. The 10 ms delay gives time for the signalling equipment to change frequency as in normal operation.

For the duration of any alarm condition (DDB: '**COS Alarm'**), the "zone 1 extension" trip logic will be invoked if the option 'Distance schemes / Z1 Ext on Chan. Fail' has been enabled.

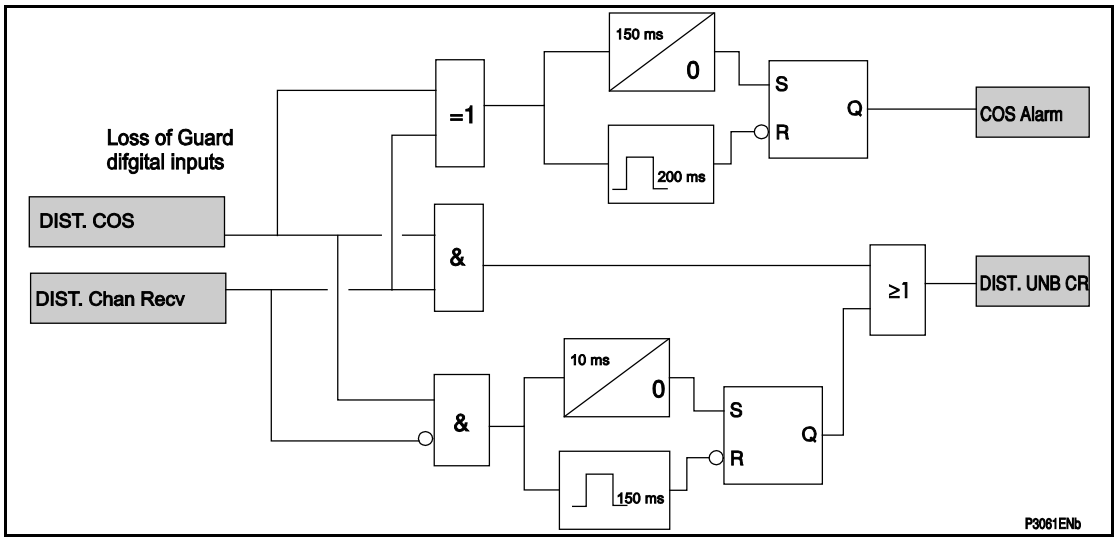


Figure 37: Loss of guard logic

'DIST. Chan Recv' 'DEF. Chan Recv'	'DIST. COS' 'DEF. COS'	'DIST. UNB CR' 'DEF. UNB CR'	'COS alarm'
0	0	0	0
1	1	1	0
0	1	1 (Window)	1 (delayed)
1	0	0	1 (delayed)

3.2.6.3 Loss of Carrier

In this mode the signalling equipment used is such that a carrier/data messages are continuously transmitted across the channel, when in service. For a permissive trip signal to be sent, additional information is contained in the carrier (eg. a trip bit is set), such that both the carrier and permissive trip are normally received together. Should the carrier be lost at any time, the relay must open the unblocking window, in case a line fault has also affected the signalling channel. Two opto inputs to the relay need to be assigned, one is the Channel Receive opto input, the second is designated Loss of Carrier (the inverse function to carrier received). The function logic is summarised in Table 6: .

System Condition	Permissive Channel Received	Loss of Guard	Permissive Trip Allowed	Alarm Generated
Healthy Line	No	No	No	No
Internal Line Fault	Yes	No	Yes	No
Unblock	No	Yes	Yes, during a 150ms window	Yes, delayed on pickup by 150ms
Signalling Anomaly	No	Yes	No	Yes, delayed on pickup by 150ms

Table 6: Logic for the loss of carrier function

The window of time during which the unblocking logic is enabled starts 10ms after the guard signal is lost, and continues for 150ms.

For the duration of any alarm condition (DDB: '**COS Alarm**'), the "zone 1 extension" trip logic will be invoked if the option 'Distance schemes / Z1 Ext on Chan. Fail' has been enabled.

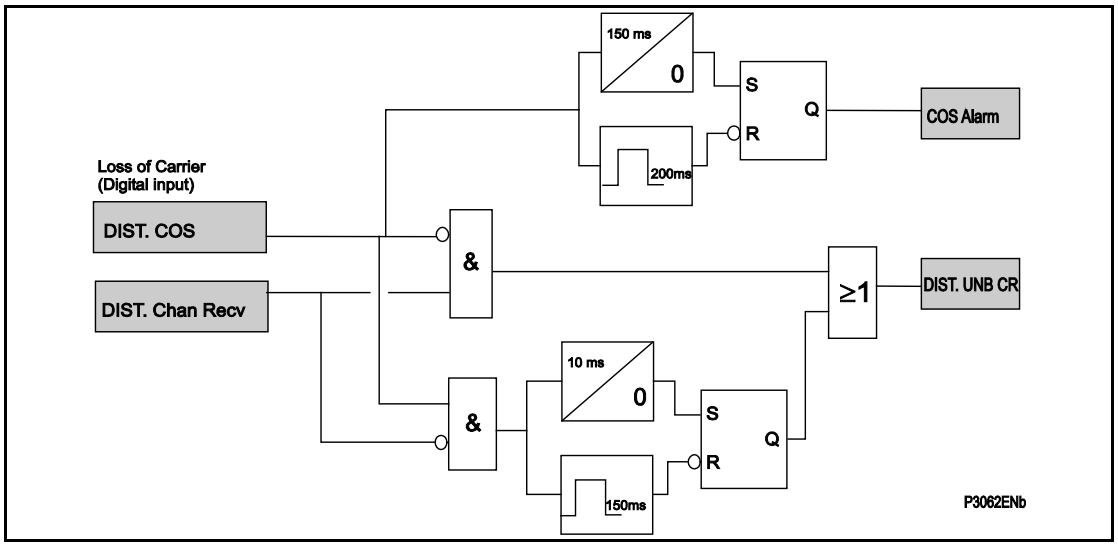


Figure 38: Loss of carrier

'DIST. Chan Recv' 'DEF. Chan Recv'	'DIST. COS' 'DEF. COS'	'DIST. UNB CR' 'DEF. UNB CR'	'COS alarm'
0	0	0	0
0	1	1 (Window)	1 (delayed)
1	0	1	0
1	1	0	1 (delayed)

Note: For DEF the logic used will depend upon which settings are enabled:

- Same channel (shared)

In this case, the DEF channel is the Main Distance channel signal (the scheme & contacts of carrier received will be identical)

- Independent channel (2 Different channels) – (2 independent contacts)

3.2.7 Trip on Reclose (TOR) / Switch On To Fault (SOTF) modes

Switch on to fault protection (SOTF) is provided for high speed clearance of any detected fault immediately following **manual closure** of the circuit breaker. SOTF protection remains enabled for 500ms following circuit breaker closure, detected via the CB Man Close input or CB close with CB control or Internal detection with all poles dead (see Figure 40), or for the duration of the close pulse on internal detection.

Instantaneous three pole tripping (and auto-reclose blocking) can also be selected

Trip on reclose protection (TOR) is provided for high speed clearance of any fault detected immediately following **autoreclosure** of the circuit breaker.

Instantaneous three pole tripping (TOR logic) can be selected for faults detected by various elements, (see the settings description above). TOR protection remains enabled for 500ms following circuit breaker closure. The use of a TOR scheme is usually advantageous for most distance schemes, since a persistent fault at the remote end of the line can be cleared instantaneously after reclosure of the breaker, rather than after the zone 2 time delay.

3.2.7.1 Setting Guidelines

- When the overcurrent option is enabled, the I>3 current setting applied should be above load current, and > 35% of peak magnetising inrush current for any connected transformers as this element has no second harmonic blocking. Setting guidelines for the I>3 element are shown in more detail in Table below.
- When a Zone 1 Extension scheme is used along with autoreclosure, it must be ensured that only Zone 1 distance protection can trip instantaneously for TOR. Typically, TOR-SOTF Mode bit 0 only would be set to “1”. Also the I>3 element must be disabled to avoid overreaching trips by level detectors.

3.2.7.2 Initiating TOR-SOTF Protection

SOTF-TOR Activation

The logic (Figure 40) issues 2 signals **TOR Enable - SOTF Enable**. There is a difference between these 2 signals as the autorecloser (whether internal or external) which must be blocked for the SOTF logic.

The detection of an open pole is enabled by the **Any Pole Dead** signal (at least one pole is open). It is an OR logic of the internal analogue detection (level detectors) and of the external detection (given by CB status: 52A/52B, which is required in the case of a VT on the Bus side).

The V< and I< Dead Pole Level Detectors are settable per phase as described belows:

- **V<** is either a fixed threshold **20% Vn** or equal to the **V Dead Line threshold** of the check synchronism function if enabled, (default value for V< dead line = 20% V_N)
- **I<** is either a fixed threshold **of 5% In** or equal to **the ‘I< Current Set’ threshold** of the Breaker Failure protection function (default value for I< CB fail = 5% I_N)**.**

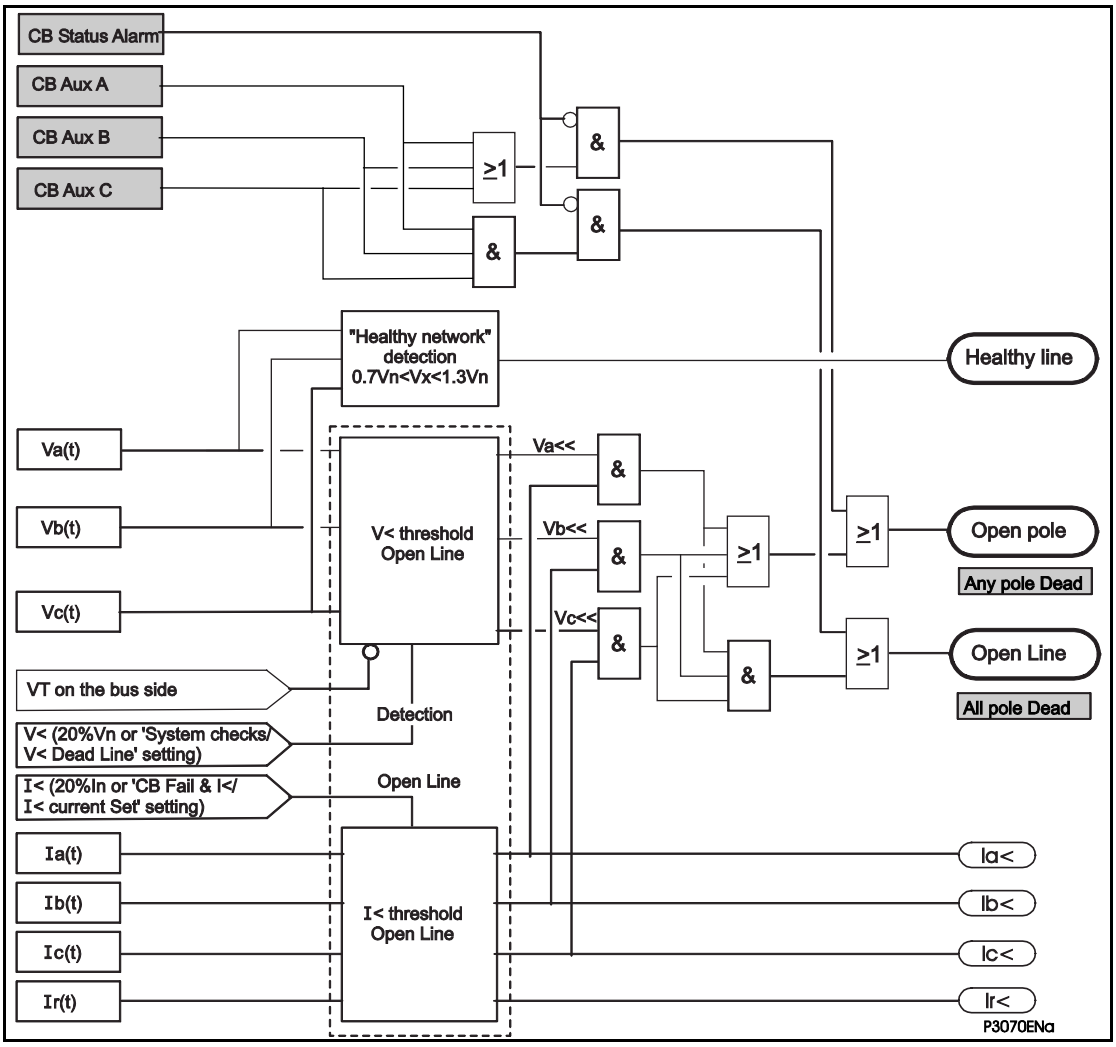


Figure 39: SOTF-TOR activation logic

TOR Enable logic is activated in 2 cases:

1. When the internal autorecloser is enabled or when the reclaim signal from an external autorecloser is connected to a logic input (opto input):

As soon as the reclaim time starts, the “TOR Enable” is activated. It will be reset at the end of the internal or external reclaim time.

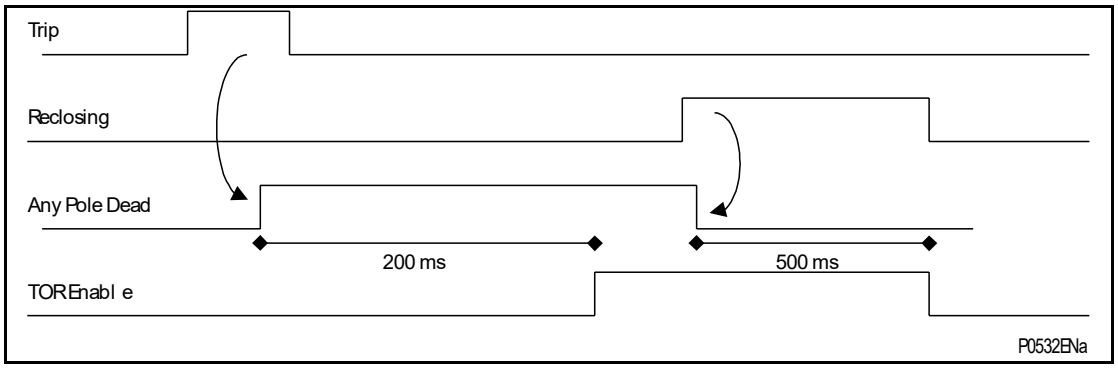
2. Without any reclaim time (internal AR disabled or external opto input Reclaim Time not assigned in the PSL):

TOR Enable will be activated during a 200 ms time window, following the pole dead detection. The TOR logic will reset (TOR Enable) **ONLY** 500 ms after the drop off of the “any pole dead” detection.

This behaviour has been designed to avoid any maloperation on a parallel line, in case of an incorrect Any Pole Dead detection performed by the internal level detectors (e.g. fault in front of a busbar on a parallel line and weak infeed at the other end of the line)

A 200 ms delay will permit tripping of the adjacent line. The level detectors will then reset the timer:

- The **TOR protection logic** is enabled when any circuit breaker pole has been open for longer than 200 ms but not longer than the 110 s default value (ie. autoreclose first shot in progress) - the timer is settable. It allows a variation of time between the detection of a dead pole condition and when the internal logic detects a “dead line” and activates the SOTF logic or when the relay’s logic detects that further time-delayed autoreclose shots are in progress.



- The SOTF protection is enabled when the circuit breaker has been open 3 pole for longer than 110 s. This time-delay is settable. It allows a variation of the time between the detection of a dead pole condition and when the internal logic detects a “dead line” and activates the SOTF logic if no autoreclose cycle is in progress. Therefore, the SOTF function is enabled for manual reclosures, not for autoreclosure.

The SOTF Enable logic is activated in 2 cases:

3. If no external close command (manual or by remote communications via a control system) is issued:

When the internal leels detectors have detected a **three pole open condition for longer than SOTF Delay (default value is 110 s**); when all the poles are closed, SOTF is enabled for a duration of 500 ms and then resets,

4. When an external close command (manual or by remote communications via a control system) is issued:

The SOTF logic is activated immediately. When all the poles are closed (after the external close command if a check synchronism condition is used in the PSL); SOTF is enabled for 500 ms and then resets.

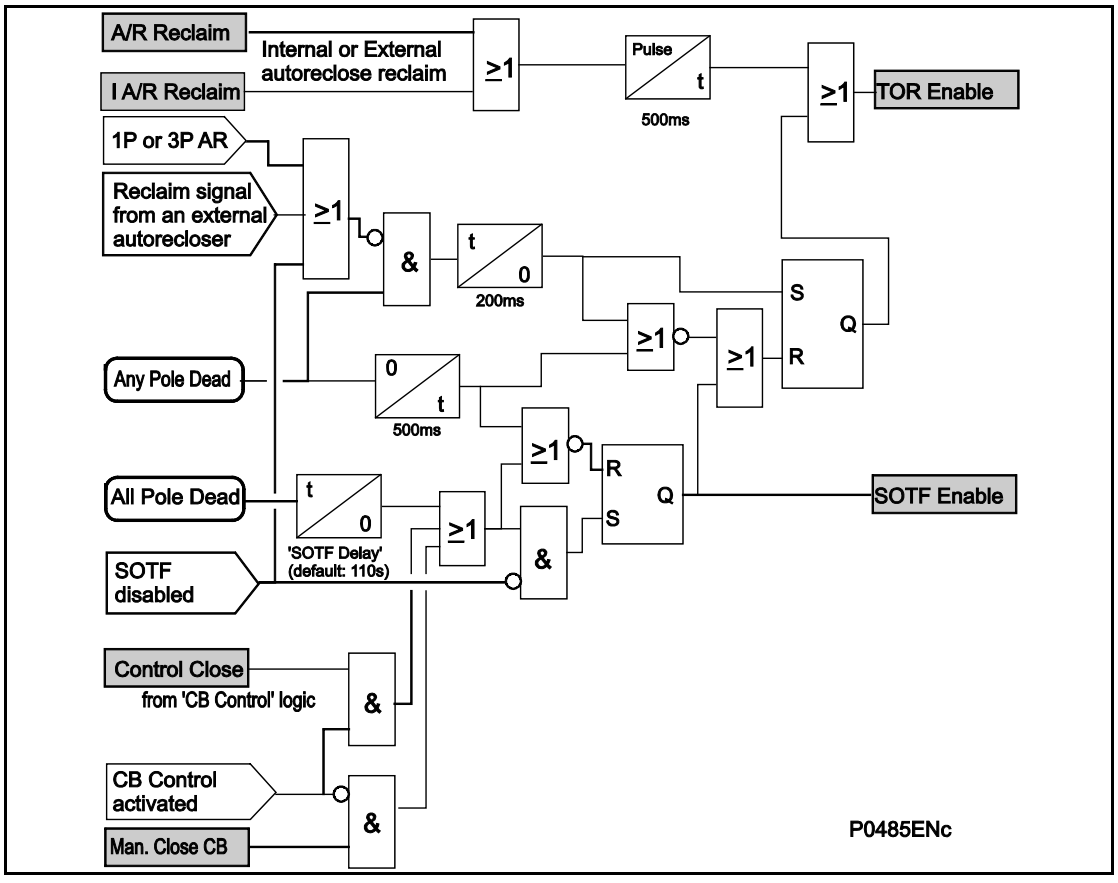


Figure 40: SOTF-TOR logic - start

3.2.7.3 TOR-SOTF Trip Logic

During the TOR-SOTF 500 ms window, individual distance protection zones can be enabled or disabled using the TOR-SOTF Mode ('**Distance schemes**' menu) function links (TOR logic Bit0 to Bit4 & SOTF logic Bit5 to Bit0E, see Figure 43 for SOTF-TOR trip logic). Setting the relevant Bit to 1 will enable that zone, setting Bits to 0 will disable distance zones. When enabled (Bit = 1), the zones will trip without waiting for their usual time delays. Therefore tripping can even occur for close-up three phase short circuits where line connected VTs are used, and memory voltage for a directional decision is unavailable. Setting "All Zones Enabled" allows instantaneous tripping to occur for all faults within the trip characteristic shown in Figure 41 below. Note, the TOR-SOTF element has second harmonic current detection, to avoid maloperation where power transformers are connected in-zone, and inrush current would otherwise cause problems. Harmonic blocking of distance zones occurs when the magnitude of the second harmonic current exceeds **25%** of the fundamental.

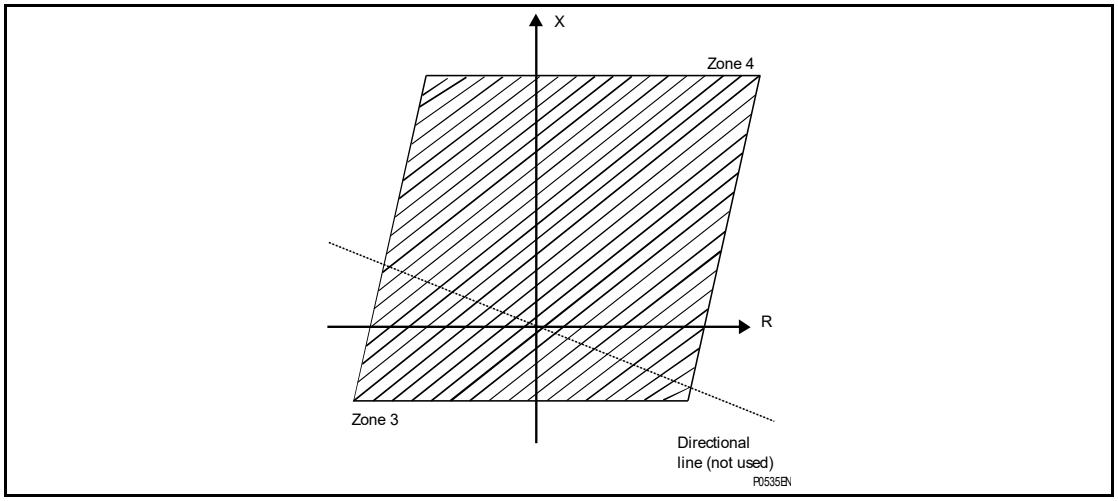


Figure 41: "All Zones" distance characteristic available for SOTF-TOR tripping

Test results from different settings (see P44x/EN ST, '**Distance schemes / TOR-SOTF Mode'**).

WARNING: Settings are not dynamically modified: one setting could affect another one.

In the following trip logic results, the following acronyms are used:

Type of Fault / **selected Logic**	**Fault in Zone X**
TOR-SOTF	SOTF trip / TOR trip / Dist trip T0, T1, T2, Tzp (Tzq), T3, T4
Name of the selection and setting	– SOTF trip (trip by SOTF (manual reclose)) / TOR trip (autoreclose): An instantaneous 3-pole trip will occur for a fault in a zone without waiting for the distance timer to expire – Dist. Trip: trip by distance protection logic – T0 (instantaneous trip) and T1, T2, Tzp (Tzq), T3, T4 (Distance time-delays, for a zone.

The fault is maintained with a duration higher than the 500 ms SOTF time, until a trip occurs.

TOR Trip logic results

Type of Fault / TOR selected Logic	Fault in Z1	Fault in Z2	Fault in Zp (Zq) forward	Fault in Zp (Zq) reverse	Fault in Z3	Fault in Z4
TOR Z1 Enabled	TOR trip T0	Dist trip T2	Dist trip TZp	Dist trip TZp	Dist trip T3	Dist trip T4
TOR Z2 Enabled	TOR trip T0	TOR trip T0	Dist trip TZp	Dist trip TZp	Dist trip T3	Dist trip T4
TOR Z3 Enabled	TOR trip T0	TOR trip T0	TOR trip T0	Dist trip TZp	TOR trip T0	Dist trip T4
TOR All Zone	TOR trip T0	TOR trip T0	TOR trip T0	TOR trip T0	TOR trip T0	TOR trip T0
TOR Dist.Scheme (logic POP/PUP)	Dist trip T1	Dist trip T2	Dist trip TZp	Dist trip TZp	Dist trip T3	Dist trip T4

SOTF Trip logic results

Type of Fault / SOTF selected Logic	Fault in Z1	Fault in Z2	Fault in Zp (Zq) forward	Fault in Zp (Zq) reverse	Fault in Z3	Fault in Z4
SOTF All Zone	SOTF trip T0	SOTF trip T0	SOTF trip T0	SOTF trip T0	SOTF trip T0	SOTF trip T0
SOTF Z1 enabled	SOTF trip T0	DIST trip T2 (2)	DIST trip TZp (2)		DIST trip T3 (2)	DIST trip T4 (2)
SOTF Z2 enabled	SOTF trip T0	SOTF trip T0	DIST trip TZp (2)		DIST trip T3 (2)	DIST trip T4 (2)
SOTF Z3 enabled	SOTF trip T0	SOTF trip T0	SOTF trip T0		SOTF trip T0	DIST trip T4 (2)
SOTF Z1+Rev (with Zp forward)	SOTF trip T0	DIST trip T2 (2)	DIST trip TZp(TZq) (2)		DIST trip T3 (2)	SOTF trip T0
SOTF Z2+Rev (with Zp forward)	SOTF trip T0	SOTF trip T0	DIST trip TZp(TZq) (2)		DIST trip T3 (2)	SOTF trip T0
SOTF Z1+Rev (with Zp reverse)	SOTF trip T0	DIST trip T2		SOTF trip T0	DIST trip T3 (2)	DIST trip T4 (2)
SOTF Z2+Rev (with Zp reverse)	SOTF trip T0	SOTF trip T0		SOTF trip T0	DIST trip T3 (2)	DIST trip T4 (2)
SOTF Dist. Sch. (Zp fwd) (With a 3Plogic)	SOTF trip T1	SOTF trip T2	SOTF trip TZp(TZq)		SOTF trip T3	SOTF trip T4
SOTF Disabled (Dist. scheme & 1P)	DIST trip T1 (1)	DIST trip T2	DIST trip(1) TZp(TZq)		DIST trip T3	DIST trip T4
No setting in SOTF (3) (All Bits at 0) & No I>3	DIST trip T1 (1)	DIST trip T2	DIST trip TZp(TZq)		DIST trip T3	DIST trip T4
Level detectors	SOTF trip T0	SOTF trip T0	SOTF trip T0		SOTF trip T0	SOTF trip T0

(1): the distance trip logic is applied (trip 1 pole is autorized)
(2): if Tx < 500 ms
(3): if SOTF-TOR by the I>3 overcurrents is deactivated (next section).

3.2.7.4 Switch-on-to-Fault and Trip-on-Reclose by the I>3 Overcurrent Element (not filtered for inrush current):

Inside the 500 ms time window initiated by the SOTF-TOR logic, an instantaneous 3 phases trip logic signal will be issued if a fault current is measured exceeding the I>3 threshold value (‘**Group 1/Back-up I>**’ menu) is measured.

After the 500 ms TOR-SOTF time windows has ended, the I>3 overcurrent element remains in service with a trip time delay equal to the setting '**Group 1/Back-up I>/I>3 Time Delay**'. This element would trip for close-up high current faults, such as those where maintenance earth clamps are inadvertently left in position on line energisation.

The 'I>3 Time Delay' element can be permanently enabled, or enabled only for SOTF or TOR (Figure 43). It is also used to detect close-up faults (in SOTF-TOR tripping logic no time-delay is applied, DDB:'**I>3start**').

3.2.7.5 Switch on to Fault by Level Detectors

The SOTF level detectors (Bit 6 in the SOTF logic), allows an instantaneous 3-phase trip from any low set I< level detector (Figure 43), provided that its corresponding Live Line level detector has not picked up within 20 ms. When closing a circuit breaker to energise a healthy line, current would normally be detected above setting, but no trip results as the system voltage rapidly recovers to near nominal. Only when a line fault is present will the voltage fail to recover, resulting in a trip.

SOTF trip by level detectors per phase: If V_{phase}< 70% Vn **AND if** I_{phase} > 5% In for 20 ms (to avoid any maloperation due to an unstable contact during the reclose command signal), an instantaneous trip command is issued.

3.2.7.6 Inputs /Outputs in TOR / SOTF Logic

The following DDB are used or available for TOR / SOTF logic (see section P44x/EN PL):

- Inputs:
  - Man Close CB,
  - AR Reclaim,
  - CB aux A,
  - CB aux B,
  - CB aux C.

- Outputs:
  - SOTF Enable,
  - TOR Enable,
  - TOC Start A,
  - TOC Start B,
  - TOC Start C,
  - Any Pole Dead,
  - All Pole Dead,
  - SOTF-TOR Trip.

3.2.7.7 Logic Diagram

In the SOTF-TOR logic diagram, the following logic name accronyms are used:

- Ia<, Ib< or Ic<: No current detected (I< threshold, by default 5% In, or I< CB Fail),
- Va>, Vb> or Vc>: Live voltage detected (V Live Line threshold, fixed at 70% Vn),
- Z1, Z1 + Z2, Z1 + Z2 + Z3, Z4, Zp, All Zones: Zones detected (+ = OR),
- '**Dist Trip A**', '**B**' or '**C**' (DDB): Trip (phase A, B or C) by distance logic,
- '**I3> Start**' (DDB): Detection by I>3 overcurrents (not filtered by inrush),
- '**TOC Start A**', '**B**' or '**C**' (DDB): Trip On Close on phase A, B or C,
- '**TOR** (or **SOTF**) **All Zones**': TOR (or SOTF) logic enabled for all zones (distance start).

Settings are set using 'Distance schemes / TOR-SOTF Mode' cell.

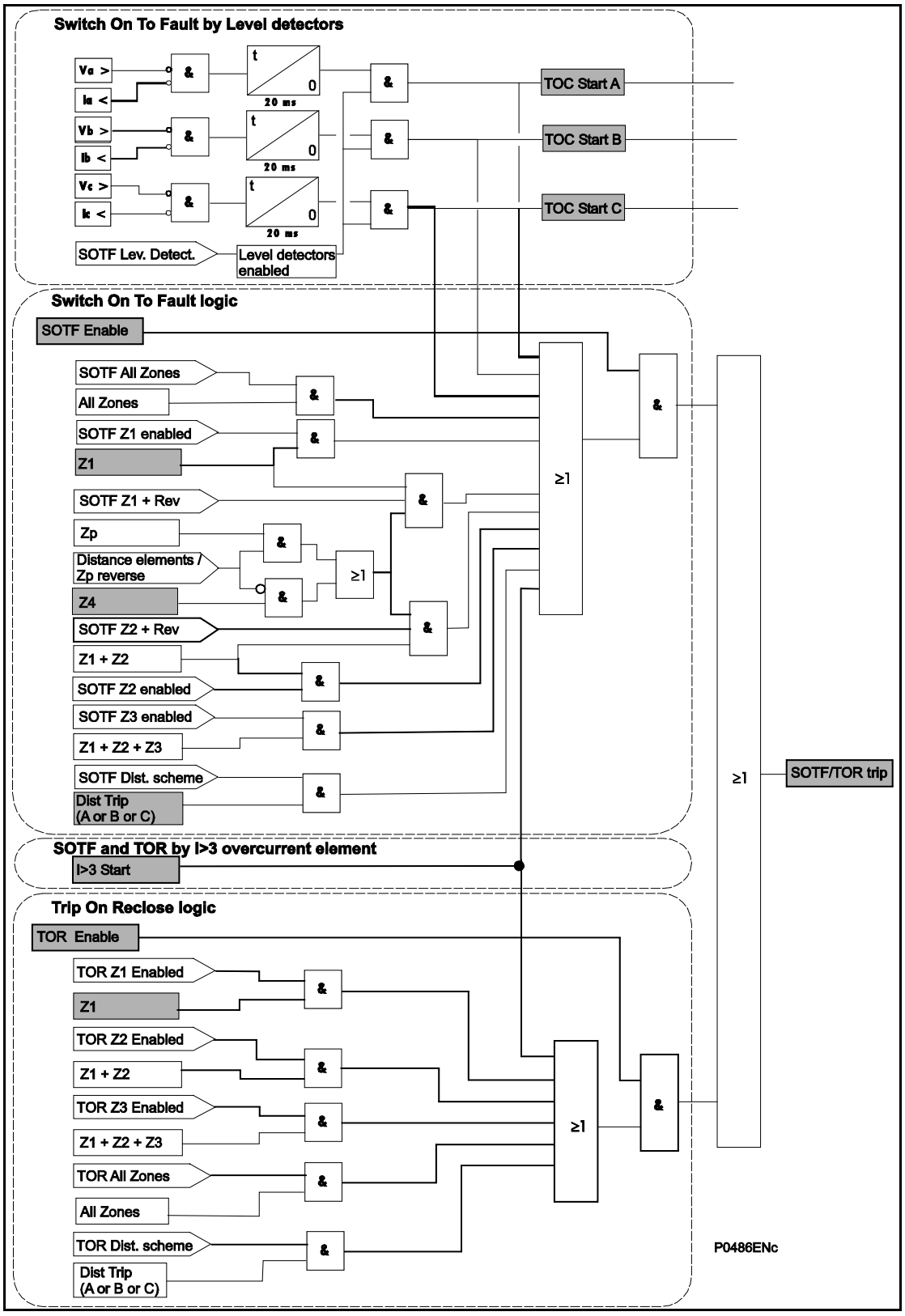


Figure 42: Switch on to fault and trip on reclose logic diagram

3.2.8 Zone 1 Ext. on Channel Fail

See section 3.1.

3.2.9 Permissive Overreach Schemes Weak Infeed (WI) Features

Weak Infeed (WI) logic can be enabled to run in parallel with all the permissive schemes. Two options are available: WI Echo, and WI Tripping.

Note: The 2 modes are blocked during Fuse failure conditions.

3.2.9.1 Weak Infeed Activation

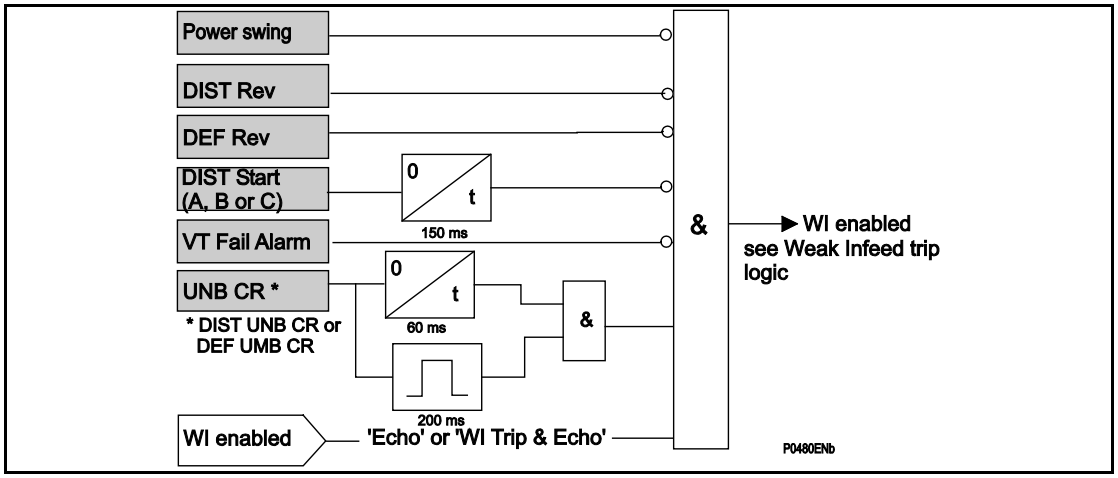


Figure 43: Weak Infeed mode activation logic

3.2.9.2 Weak Infeed Echo

For permissive schemes, a signal would only be sent if the required signal send zone were to detect a fault. However, the fault current infeed at one line end may be so low as to be insufficient to operate any distance zones, and risks a failure to send the signal. Also, if one circuit breaker had already been left open, the current infeed would be zero. These are termed weak infeed conditions, and may result in slow fault clearance at the strong infeed line end (tripping after time tZ2). To avoid this slow tripping, the weak infeed relay can be set to “echo” back any channel received to the strong infeed relay (ie. to immediately send a signal once a signal has been received). This allows the strong infeed relay to trip instantaneously in its permissive trip zone. The additional signal send logic is (“UNB CR” for DDB: ‘**Dist UNB CR**’ or DDB: ‘**DEF UNB CR**’):

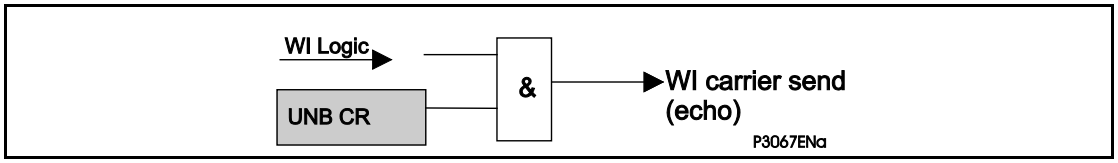


Figure 44: Weak infeed echo

3.2.9.3 Weak Infeed Tripping

Weak infeed echo logic ensures an aided trip at the strong infeed terminal but not at the weak infeed. The P442 and P444 relays also have a setting option to allow tripping of the weak infeed circuit breaker of a faulted line.

Three undervoltage elements, Va<, Vb< and Vc< are used to detect the line fault at the weak infeed terminal, with a common setting typically 70% of rated phase-neutral voltage. This voltage check prevents tripping during spurious operations of the channel or during channel testing.

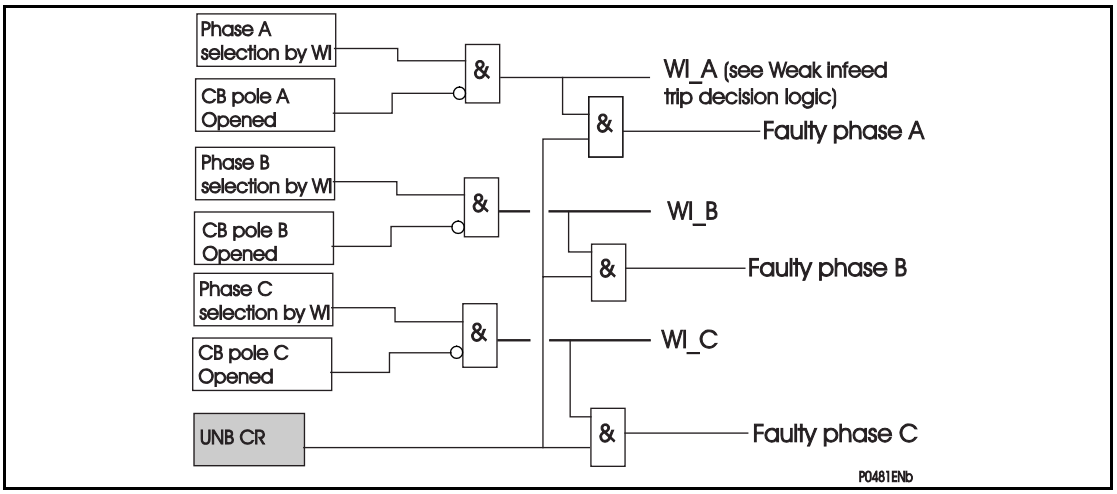


Figure 45: Weak infeed phase selection logic

DDB: '**DIST. UNB CR**' (or '**DEF. UNB CR**') is used as a filter to avoid a permanent phase selection which could be maintained if CBaux signals are not mapped in the PSL (when line is opened).

The additional weak infeed trip logic is:

Weak infeed trip: No Distance Zone Operation, plus reverse directional decision, plus V<, plus Channel Received.

Weak infeed tripping is time delayed according to the 'WI: Trip time delay' value, usually set to 60 ms. Due to the use of phase segregated undervoltage elements, single pole tripping can be enabled for WI trips (DDB: '**WI Trip A**', '**WI Trip B**' or '**WI Trip C**') if required. If single pole tripping is disabled a three pole trip will result after the time delay.

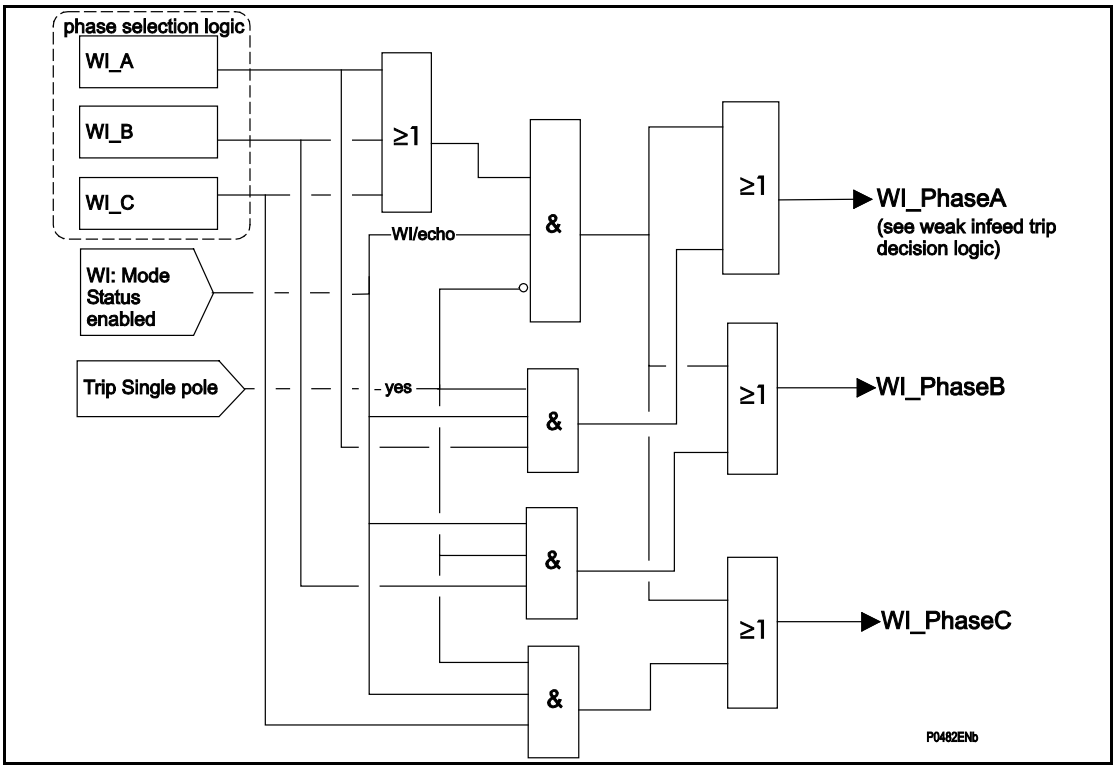


Figure 46: Weak infeed trip decision logic

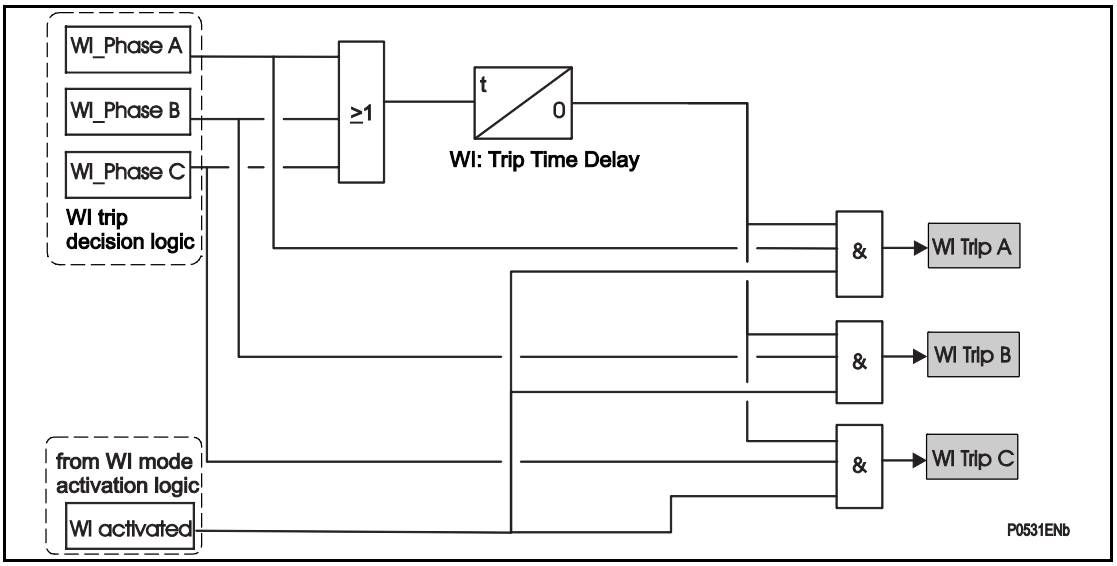


Figure 47: Weak infeed trip logic

3.2.10 Loss of Load (LoL)

3.2.11 Loss of Load Accelerated Tripping (LoL)

The loss of load logic provides fast fault clearance for faults over the whole of a double end fed protected circuit for all types of fault, except three phases. The scheme has the advantage of not requiring a signalling channel. Alternatively, the logic can be chosen to be enabled when the channel associated with an aided scheme has failed. This failure is detected by permissive scheme unblocking logic, or a Channel Out of Service (COS) opto input.

Any fault located within the reach of Zone 1 will result in fast tripping of the local circuit breaker. For an end zone fault with remote infeed, the remote breaker will be tripped in Zone 1 by the remote relay and the local relay can recognise this by detecting the loss of load current in the healthy phases. This, coupled with operation of a Zone 2 comparator causes tripping of the local circuit breaker.

Before an accelerated trip can occur, load current must have been detected prior to the fault. The loss of load current opens a window during which time a trip will occur if a Zone 2 comparator operates. A typical setting for this window is 40 ms as shown in Figure 48, although this can be altered in the menu LoL: Window cell. The accelerated trip is delayed by 18ms to prevent initiation of a loss of load trip due to circuit breaker pole discrepancy occurring for clearance of an external fault. The local fault clearance time can be deduced as follows:

t = Z1d + 2CB + LDr + 18ms

Where:

Z1d = maximum downstream zone 1 trip time

CB = Breaker operating time

LDr = Upstream level detector (LoL: I<) reset time

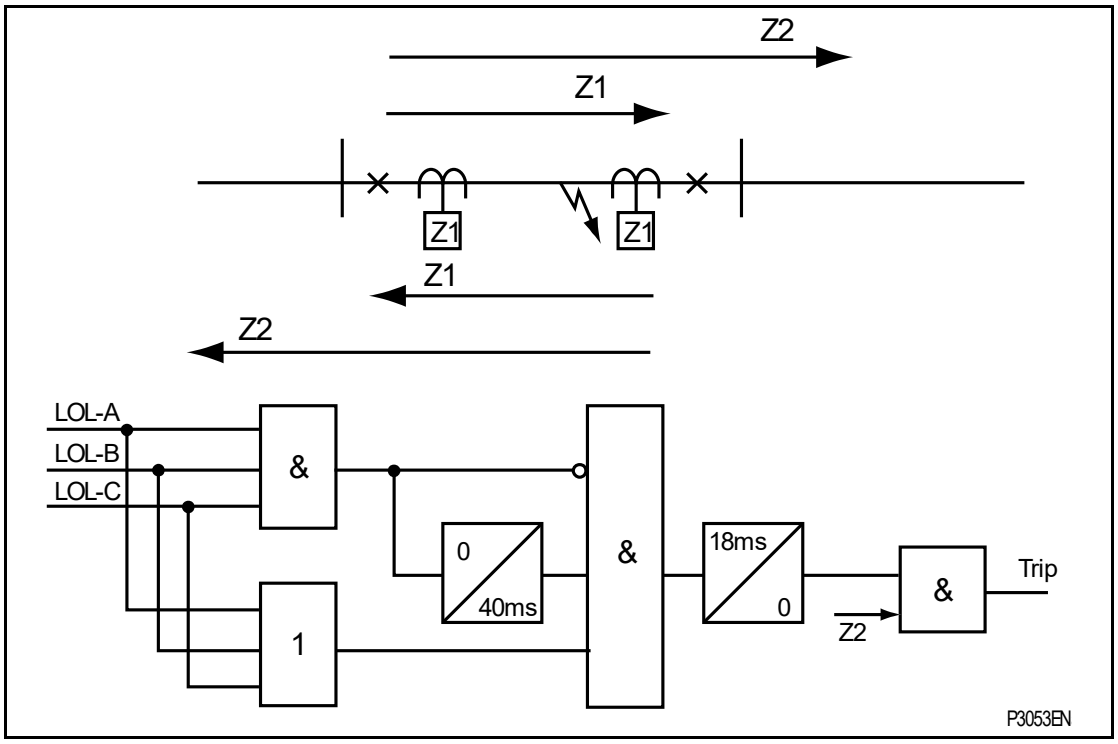


Figure 48: Loss-of-load accelerated trip scheme

For circuits with load tapped off the protected line, care must be taken in setting the loss of load feature to ensure that the I< level detector setting is above the tapped load current. When selected, the loss of load feature operates in conjunction with the main distance scheme that is selected. In this way it provides high speed clearance for end zone faults when the Basic scheme is selected or, with permissive signal aided tripping schemes, it provides high speed back-up clearance for end zone faults if the channel fails.

Note: Loss of load tripping is only available where 3 pole tripping is used.

3.3 Power Swing

See section 4.1.

3.4 Other protection considerations - settings example

3.4.1 Distance Protection Setting Example

3.4.1.1 Objective

To protect the 100km double circuit line between the Green Valley and Blue River substations using relay protection in the POP Z2 Permissive Overreach mode and to set the relay at Green Valley substation, as shown in Figure 49.

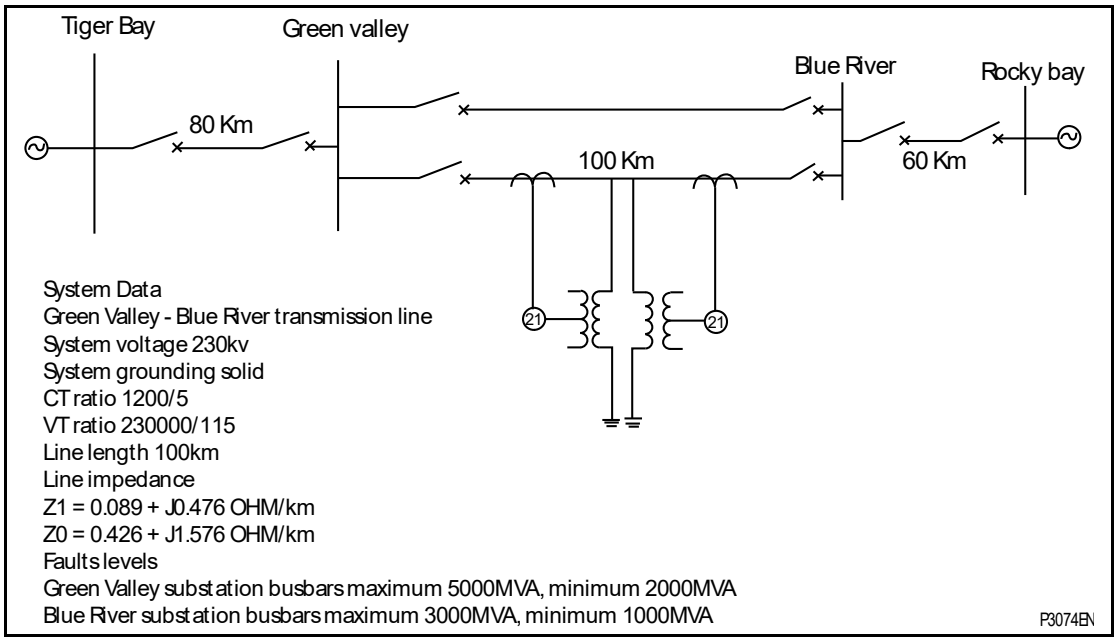


Figure 49: System assumed for worked example

3.4.1.2 System Data

Line length: 100km

Line impedances: $Z_1 = 0.089 + j0.476 = 0.484 / \underline{79.4°}\ \Omega/km$

$Z_0 = 0.426 + j1.576 = 1.632 / \underline{74.8°}\ \Omega/km$

$Z_0/Z_1 = 3.372 / \underline{-4.6°}$

CT ratio: 1 200 / 5

VT ratio: 230 000 / 115

3.4.1.3 Relay Settings

It is assumed that Zone 1 Extension is not used and that only three forward zones are required. Settings on the relay can be performed in primary or secondary quantities and impedances can be expressed as either polar or rectangular quantities (menu selectable). For the purposes of this example, secondary quantities are used.

3.4.1.4 Line Impedance

Ratio of secondary to primary impedance $\frac{1200/5}{230000/115} = 0.12$

Line impedance secondary = ratio CT/VT x line impedance primary.

Line Impedance = 100 x 0.484 / $\underline{79.4°}$ (primary) x 0.12

= 5.81 / $\underline{79.4°}\ \Omega$ secondary.

Relay Line Angle settings -90° to 90° in 1° steps. Therefore, select Line Angle = 80° for convenience.

Therefore set Line Impedance and Line Angle: = 5.81 / $\underline{80°}\ \Omega$ secondary.

3.4.1.5 Zone 1 Phase Reach Settings

Required Zone 1 reach is to be 80% of the line impedance between Green Valley and Blue River substations.

Required Zone 1 reach = 0.8 x 100 x 0.484 / $\underline{79.4°}$ x 0.12

Z1 = 4.64 / 79.4° Ω secondary.

Z2 = 100 x 0.484 / 79.4° + 50% x 60 x 0.484 / 79.4°

The Line Angle = 80°.

Therefore actual Zone 1 reach, Z1 = 4.64 / 80° Ω secondary.

3.4.1.6 Zone 2 Phase Reach Settings

Required Zone 2 impedance =

(Green Valley-Blue River) line impedance + 50% (Blue River-Rocky Bay) line impedance

Z2 = (100+30) x 0.484 / 79.4° x 0.12

= 7.56 / 79.4° Ω secondary.

The Line Angle = 80°.

Actual Zone 2 reach setting = 7.56 / 80° Ω secondary

3.4.1.7 Zone 3 Phase Reach Settings

Required Zone 3 forward reach =

(Green Valley-Blue River + Blue River-Rocky Bay) x 1.2

= (100+60) x 1.2 x 0.484 / 79.4° x 0.12

Z3 = 11.15 / 79.4° ohms secondary

Actual Zone 3 forward reach setting = 11.16 / 80° ohms secondary

3.4.1.8 Zone 4 Reverse Settings with no Weak Infeed Logic Selected

Required Zone 4 reverse reach impedance = Typically 10% Zone 1 reach

= 0.1 x 4.64 / 79.4°

Z4 = 0.464 / 79.4°

Actual Zone 4 reverse reach setting = 0.46 / 80° ohms secondary

3.4.1.9 Zone 4 Reverse Settings with Weak Infeed Logic Selected

Where zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, zone 4 must reach further behind the relay than zone 2 for the remote relay. This can be achieved by setting: Z4 ≥ ((Remote zone 2 reach) x 120%) minus the protected line impedance:

Remote Zone 2 reach =

(Blue River-Green Valley) line impedance + 50% (Green Valley-Tiger Bay) line impedance

= (100+40) x 0.484 / 79.4° x 0.12

= 8.13 / 79.4° Ω secondary.

Z4 ≥ ((8.13 / 79.4°) x 120%) - (5.81 / 79.4°)

= 3.95 / 79.4°

Minimum zone 4 reverse reach setting = 3.96 / 80° ohms secondary

3.4.1.10 Residual Compensation for Earth Fault Elements

The residual compensation factor can be applied independently to certain zones if required. This feature is useful where line impedance characteristics change between sections or where hybrid circuits are used. In this example, the line impedance characteristics do not change and as such a common KZ0 factor can be applied to each zone. This is set as a ratio “kZ0 Res. Comp”, and an angle “kZ0 Angle”:

kZ0 Res. Comp, $|kZ0|$ = $(Z_0 - Z_1) / 3.Z_1$ Ie: As a ratio.

kZ0 Angle, $\angle kZ0$ = $\angle (Z_0 - Z_1) / 3.Z_1$ Set in degrees.

$Z_{L0} - Z_{L1}$ = (0.426 + j1.576) - (0.089 + j0.476)

= 0.337 + j1.1

= 1.15 / 72.9°

$$kZ0 = \frac{1.15 / 72.9°}{3x0.484 / 79.4°}$$ = 0.79 / –6.5°

Therefore, select:

kZ0 Res. Comp = 0.79 (Set for kZ1, kZ2, kZp, kZ4).

kZ0 Angle = –6.5° (Set for kZ1, kZ2, kZp, kZ4).

3.4.1.11 Resistive Reach Calculations

All distance elements must avoid the heaviest system loading. Taking the 5A CT secondary rating as a guide to the maximum load current, the minimum load impedance presented to the relay would be:

$Vn_{(phase-neutral)} / In$ = $(115 / \sqrt{3}) / 5$ = 13.3 Ω (secondary)

Typically, phase fault distance zones would avoid the minimum load impedance by a margin of ≥40% if possible (bearing in mind that the power swing characteristic surrounds the tripping zones), earth fault zones would use a ≥20% margin. This allows maximum resistive reaches of 7.9 Ω, and 10.6 Ω, respectively.

From Table 2: (see § 3.1.2.4), taking a required primary resistive coverage of 14.5Ω for phase faults, and assuming a typical earth fault coverage of 40Ω, the minimum secondary reaches become:

RPh (min) = 14.5 x 0.12 = 1.74 Ω (secondary);

RG (min) = 40 x 0.12 = 4.8 Ω (secondary).

Resistive reaches could be chosen between the calculated values as shown in Table 10. The zone 2 elements satisfy R2Ph ≤ (R3Ph x 80%), and R2G ≤ (R3G x 80%).

	Minimum	Maximum	Zone 1	Zone 2	Zones 3 & 4
Phase (RPh) Ω	1.74	7.9	R1Ph = 3	R1Ph = 4	R3Ph-4Ph = 8
Earth (RG) Ω	4.8	10.6	R1G = 5	R1G = 6	R3G-4G = 10

Table 7: Selection of resistive reaches

R3Ph/2 = R4Ph/2 should be set ≤ 80% Z minimum load – ΔR.

3.4.1.12 Power Swing Band

Typically, the ΔR and ΔX band settings are both set between 10 - 30% of R3Ph. This gives a secondary impedance between 0.6 and 1.8 Ω. For convenience, 1.0 Ω could be set.

The width of the power swing band is calculated as follows:

$\Delta R = 1.3 \times \tan(\pi \times \Delta f \times \Delta t) \times R_{LOAD}$

Assuming that the load corresponds to 60° angles between sources and if the resistive reach is set so that Rlim = $R_{LOAD}/2$, the following is obtained:

$\Delta R = 0.032 \times \Delta f \times R_{LOAD}$

To ensure that a power swing frequency of 5 Hz is detected, the following is obtained:

$\Delta R = 0.16 \times R_{LOAD}$

Where:

ΔR width of the power swing detection band

Δf power swing frequency ($f_A - f_B$)

Rlim resistive reach of the starting characteristic (=R3ph-R4ph)

Z network impedance corresponding to the sum of the reverse (Z4) and forward (Z3) impedances

R_{LOAD} load resistance

3.4.1.13 Current Reversal Guard

The current reversal guard timer available with POP schemes needs a non-zero setting when the reach of the zone 2 elements is greater than 1.5 times the impedance of the protected line. In this example, their reach is only 1.3 times the protected line impedance. Therefore, current reversal guard logic does not need to be used and the recommended settings for scheme time-delays are:

tREVERSAL GUARD = 0

'Aid Dist Delay' = 98 ms (typical).

3.4.1.14 Instantaneous Overcurrent Protection

To provide parallel high-speed fault clearance to the distance protection, it is possible to use the I>3 element as an instantaneous highset. It must be ensured that the element will only respond to faults on the protected line. The worst case scenario for this is when only one of the parallel lines is in service.

Two cases must be considered. The first case is a fault at Blue River substation with the relay seeing fault current contribution via Green Valley. The second case is a fault at Green Valley with the relay seeing fault current contribution via Blue River.

Case 1:

Source Impedance = $230^2 / 5000$ = 10.58 Ω

Line Impedance = 48.4Ω

Fault current seen by relay = $(230000 / \sqrt{3}) / (10.58 + 48.4)$

= 2251A

Case 2:

Source Impedance = $230^2 / 3000$ = 17.63 Ω

Line Impedance = 48.4 Ω

Fault current seen by relay = $(230000 / \sqrt{3}) / (17.63 + 48.4)$

= 2011A

The overcurrent setting must be in excess of 2251A. To provide an adequate safety margin a setting ≥120% the minimum calculated should be chosen, say 2800A.

3.4.2 Teed feeder protection

The application of distance relays to three terminal lines is fairly common. However, several problems arise when applying distance protection to three terminal lines.

3.4.2.1 Apparent Impedance

Figure 50 shows a typical three terminal line arrangement. For a fault at the busbars of terminal B the impedance seen by a relay at terminal A will be equal to:

$Z_a = Z_{at} + Z_{bt} + [Z_{bt}.(I_c/I_a)]$

Relay A will underreach for faults beyond the tee-point with infeed from terminal C. When terminal C is a relatively strong source, the underreaching effect can be substantial. For a zone 2 element set to 120% of the protected line, this effect may result in non-operation of the element for internal faults. This not only effects time delayed zone 2 tripping but also channel-aided schemes. Where infeed is present, it will be necessary for Zone 2 elements at all line terminals to overreach both remote terminals with allowance for the effect of tee-point infeed. Zone 1 elements must be set to underreach the true impedance to the nearest terminal without infeed. Both these requirements can be met through use of the alternative setting groups in the P442 and P444 relays.

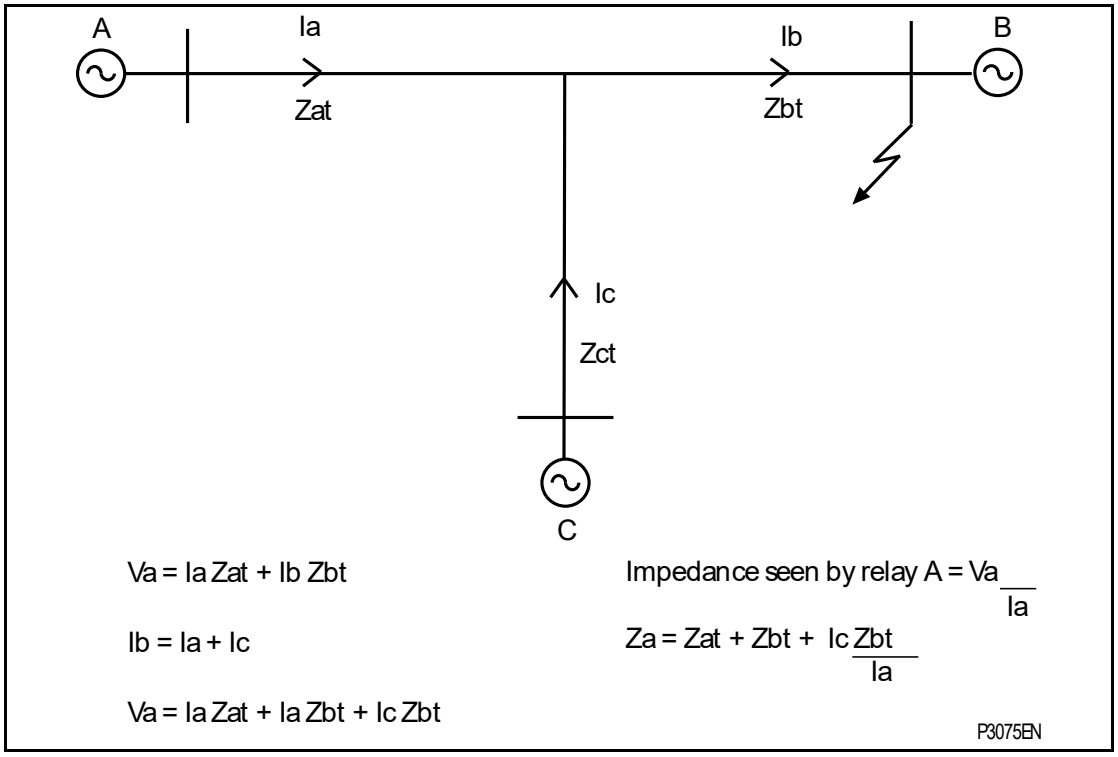


Figure 50: Teed feeder application - apparent impedances seen by relay

3.4.2.2 Permissive Overreach Schemes

To ensure operation for internal faults in a POP scheme, the relays at the three terminals should be able to see a fault at any point within the protected feeder. This may demand very large zone 2 reach settings to deal with the apparent impedances seen by the relays.

A POP scheme requires the use of two signalling channels. A permissive trip can only be issued upon operation of zone 2 and receipt of a signal from both remote line ends. The requirement for an 'AND' function of received signals must be realised through use of contact logic external to the relay, or the internal Programmable Scheme Logic. Although a POP scheme can be applied to a three terminal line, the signalling requirements make its use unattractive.

3.4.2.3 Permissive Underreach Schemes

For a PUP scheme, the signalling channel is only keyed for internal faults. Permissive tripping is allowed for operation of zone 2 plus receipt of a signal from either remote line end. This makes the signalling channel requirements for a PUP scheme less demanding than for a POP scheme. A common power line carrier (PLC) signalling channel or a triangulated signalling arrangement can be used. This makes the use of a PUP scheme for a teed feeder a more attractive alternative than use of a POP scheme.

The channel is keyed from operation of zone 1 tripping elements. Provided at least one zone 1 element can see an internal fault then aided tripping will occur at the other terminals if the overreaching zone 2 setting requirement has been met. There are however two cases where this is not possible:

Figure 51 (i) shows the case where a short tee is connected close to another terminal. In this case, zone 1 elements set to 80% of the shortest relative feeder length do not overlap. This leaves a section not covered by any zone 1 element. Any fault in this section would result in zone 2 time delayed tripping.

Figure 51 (ii) shows an example where terminal 'C' has no infeed. Faults close to this terminal will not operate the relay at 'C' and hence the fault will be cleared by the zone 2 time-delayed elements of the relays at 'A' and 'B'.

Figure 51 (iii) illustrates a further difficulty for a PUP scheme. In this example current is outfeed from terminal 'C' for an internal fault. The relay at 'C' will therefore see the fault as reverse and not operate until the breaker at 'B' has opened; i.e. sequential tripping will occur.

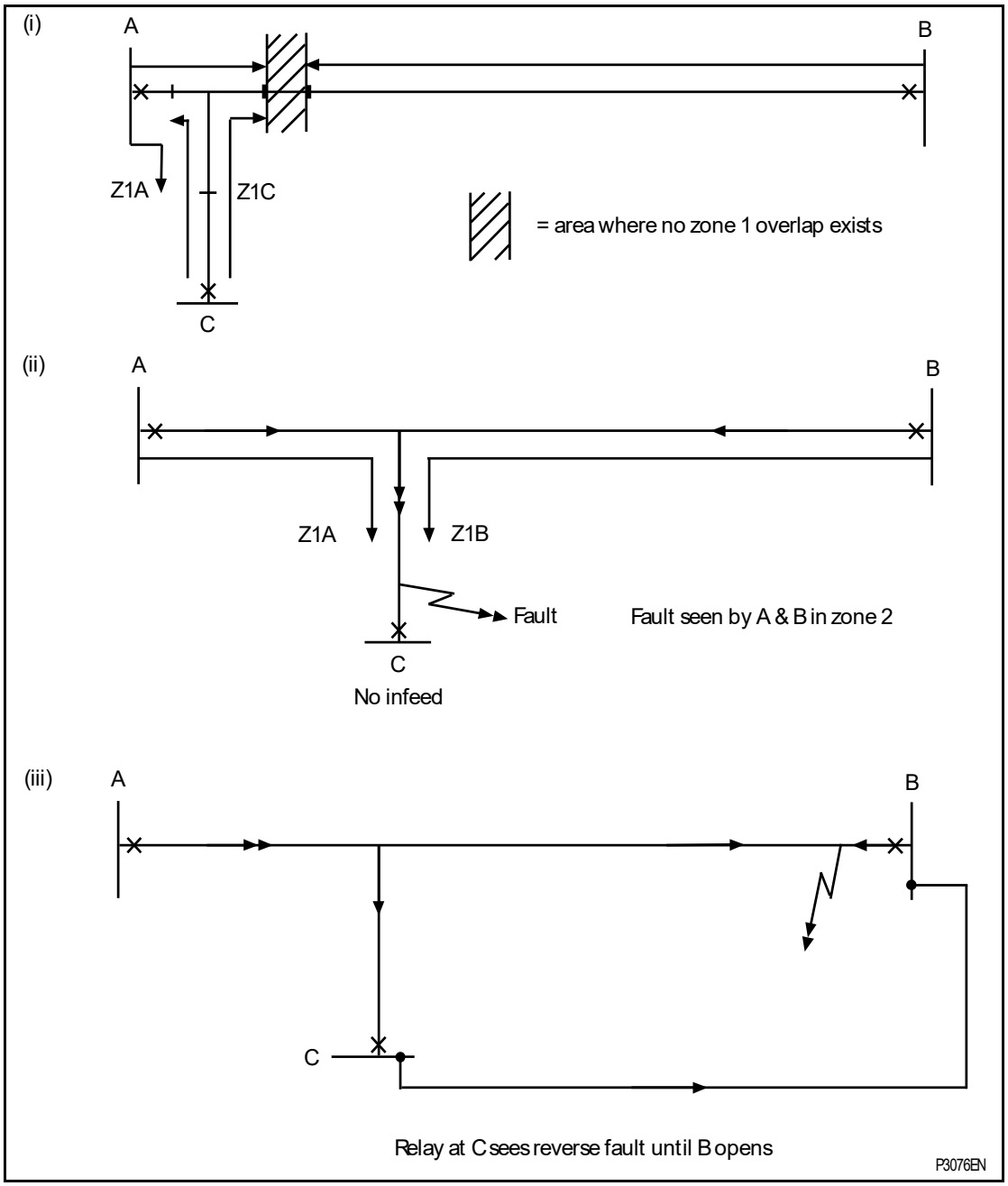


Figure 51: Teed feeder applications

3.4.2.4 Blocking Schemes

Blocking schemes are particularly suited to the protection of teed feeders, since high speed operation can be achieved where there is no current infeed from one or more terminals. The scheme also has the advantage that only a common simplex channel or a triangulated simplex channel is required.

The major disadvantage of blocking schemes is highlighted in Figure 51 (iii) where fault current is outfeed from a terminal for an internal fault condition. relay 'C' sees a reverse fault condition. This results in a blocking signal being sent to the two remote line ends, preventing tripping until the normal zone 2 time delay has expired.

3.5 Distance protection logic

The following diagram gives the logic of the distance protection:

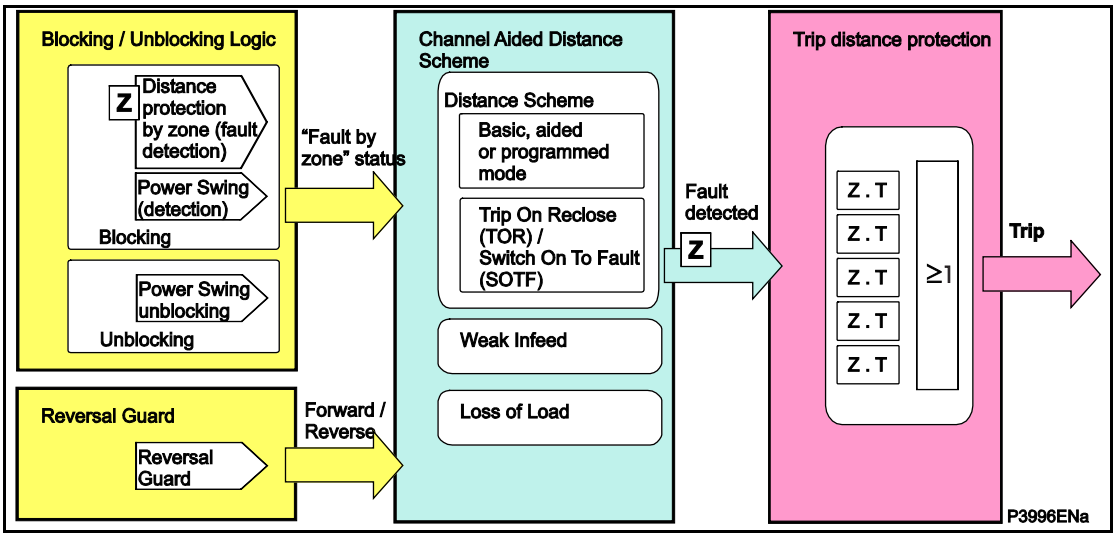


Figure 52: Mimic diagram

3.5.1 Blocking / unblocking logic

The zones unblocking/blocking logic with power swing are managed as explained in the section 3.2.

3.5.1.1 Distance protection by zones and unblocking / blocking logic with power swing

The logic of the distance protection by zones (including power swing basic unblocking / blocking logic) is shown in the following diagram:

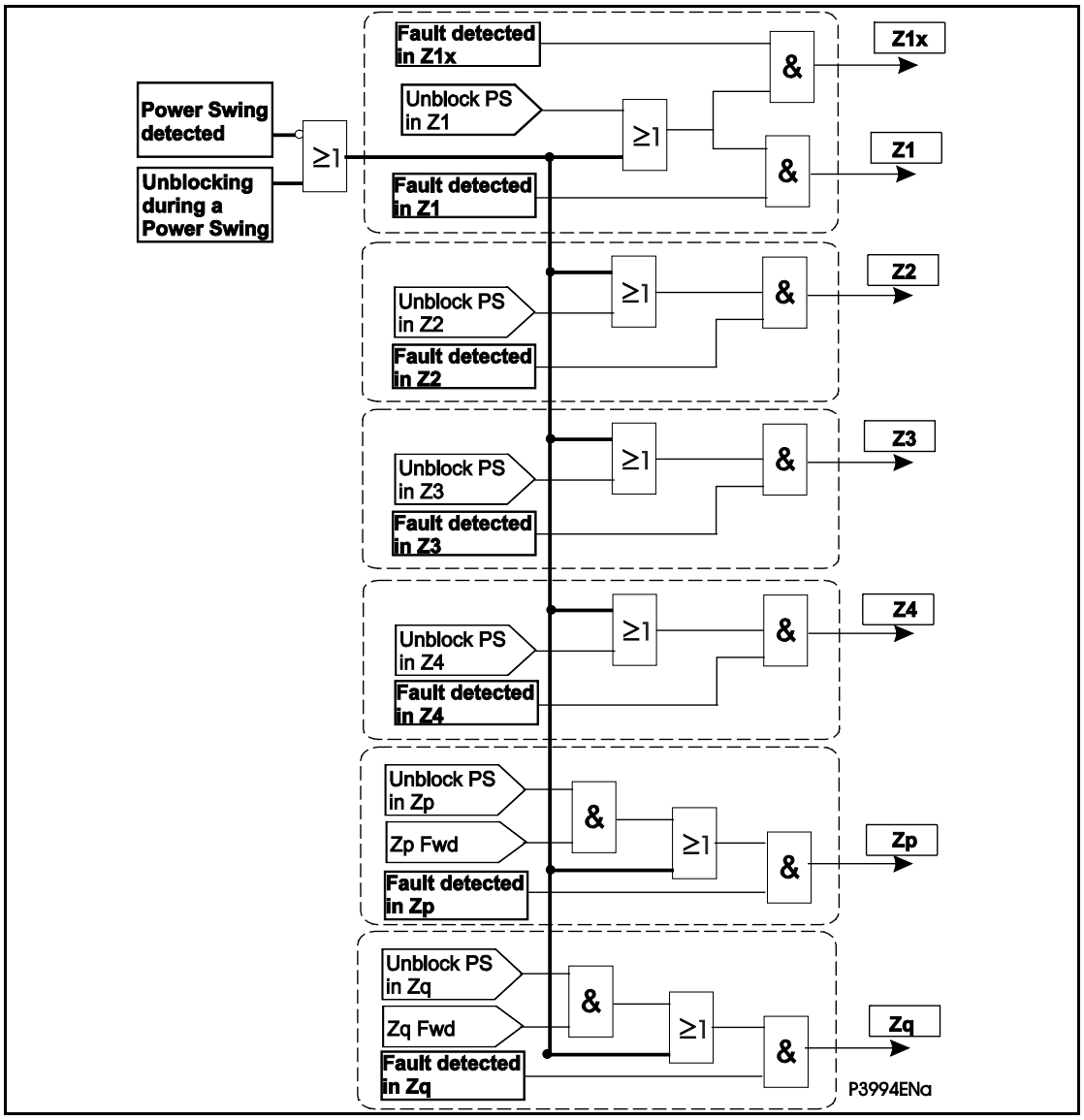


Figure 53: logic of the distance protection by zones

Where:

Unblock PS Z1, Z2, Z3, Z4, Zp or Zq:	Unblocking of Zone 1 (Z1), Z2, Z3, Z4, Zp or Zq during a power swing ('Power swing / Blocking zone' menu) 0 => Zx blocked during power swing 1 => Zx unblocked during power swing
DDB: **Z1**,**Z1x**, **Z2**, **Z3**, **Z4**, **Zp**, **Zq**:	Fault detected in zone 1, Z1x, 2, 3, 4, p or q and filtered by blocking/unblocking Power Swing

The fault detection is modified when the following conditions are met:

- Power swing detection (in this case, power swing detected or unblocking during a power swing),
- Blocking logic settings during power swing,
- Type of teleprotection scheme.

When zones are blocked during the power swing, those can be unblocked by:

- Start of unblocking logic,
- Unblocking logic enabled for the concerned zone or all zones (setting).

3.5.1.2 Unblocking / blocking logic with power swing or reversal guard

For double circuit lines, the fault current direction can change in one circuit when circuit breakers open sequentially to clear the fault on the parallel circuit. The change in current direction causes the overreaching distance elements to see the fault in the opposite direction to the direction in which the fault was initially detected. (settings of these elements exceed 150% of the line impedance at each terminal). The race between operation and resetting of the overreaching distance elements at each line terminal can cause the Permissive Overreach, and Blocking schemes to trip the healthy line. A system configuration that could result in current reversals is shown in Figure 54. For a specific fault (see distance scheme for details) on line L1 close to circuit breaker B, as circuit breaker B trips it causes the direction of current flow in line L2 to reverse.

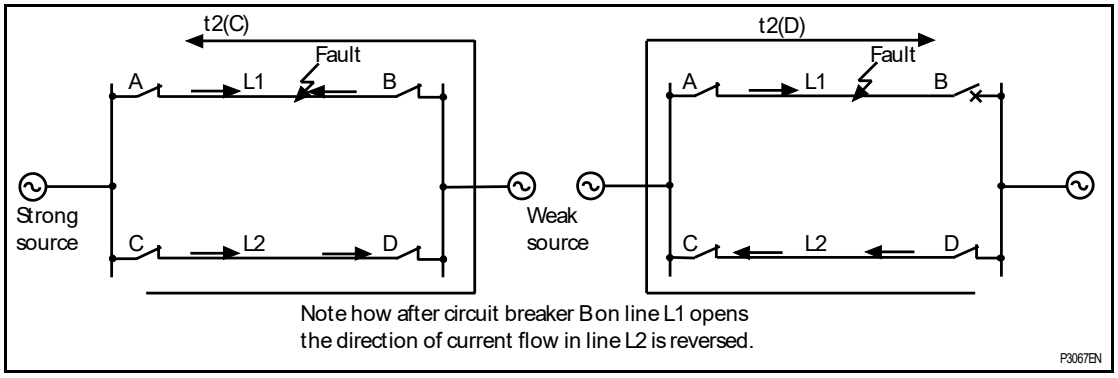


Figure 54: Current reversal in double circuit lines

In this case, zones & directionality are modified when the following conditions are met (basic unblocking / blocking logic in the Figure 55):

- Power swing detection (in this case, power swing detected or unblocking during a power swing),
- Blocking logic settings during power swing,
- Reversal Guard time-delay (DDB: '**Reversal Guard**'),
- Type of teleprotection scheme.

When zones are blocked during the power swing, those can be unblocked by:

- Start of unblocking logic,
- Unblocking logic enabled for the concerned zone or all zones (setting).

In the next figure, the following acronyms are used

Unblock PS Z1, Z2, Z3, Z4, Zp or Zq:	Unblocking of Zone 1 (Z1), Z2, Z3, Z4, Zp or Zq during a power swing ('Power swing / Blocking zone' menu) 0 => Zx blocked during power swing 1 => Zx unblocked during power swing
DDB: **Z1**,**Z1x**, **Z2**, **Z3**, **Z4**, **Zp**, **Zq**:	Fault detected in zone 1, Z1x, 2, 3, 4, p or q and filtered by blocking/unblocking Power Swing
Z1<ZL	Setting: internal configuration that determines that Z1 is smaller than the length of the line ZL.

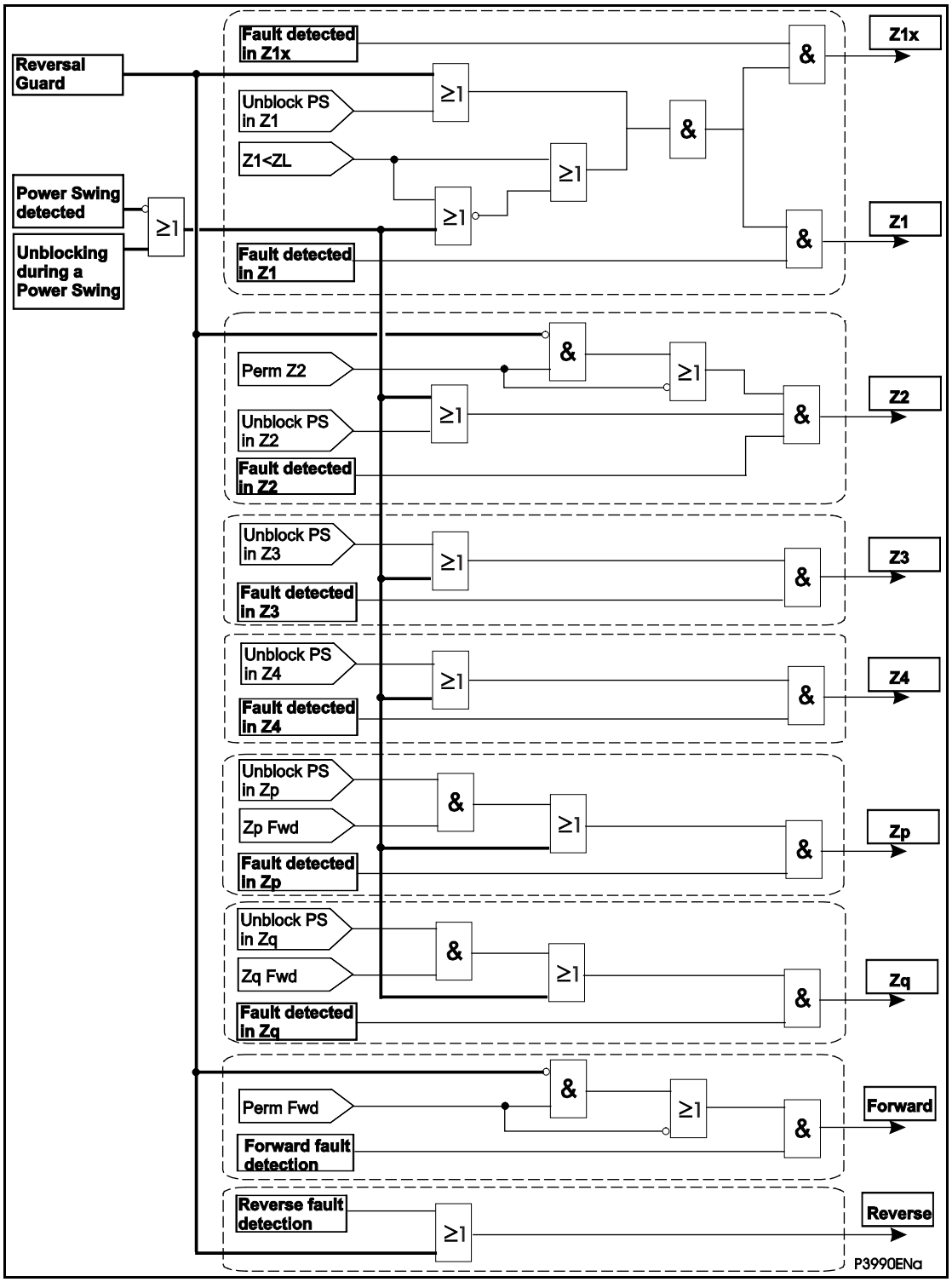


Figure 55: Current reversal in double circuit lines zones blocking / unblocking with power swing or reversal guard

During the reversal guard logic (in the case of parallel lines with overreaching teleprotection scheme - Z1x>ZL), the reverse direction decision is latched (until that timer is elapsed) from the change from reverse to forward fault direction.

3.5.1.3 Zone 1 extended

The following trip logic represents the zone 1 extended logic:

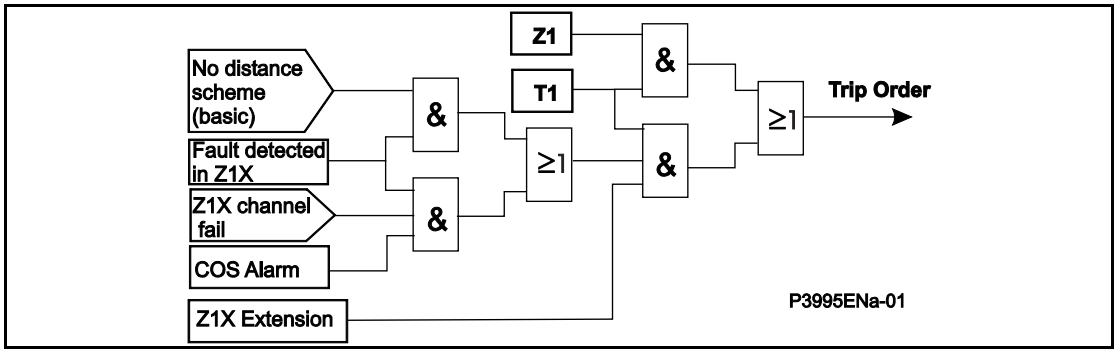


Figure 56: Zone 1 extended (Z1X) trip logic

Z1X can be used as well as the default scheme logic in case of UNB _Alarm-carrier out of service (See unblocking logic – Section 3.2.6)

Where:

	Description
'COS alarm'	Alarm channel (main and DEF)
Z1x, Z1	Z1X, Z1 Decision (lock out by Power Swing)
T1	distance timer 1, 2, 3, 4, p or q elapsed

3.5.2 Channel Aided distance scheme logic

3.5.2.1 Loss of Load

The next figure shows the loss of load trip logic:

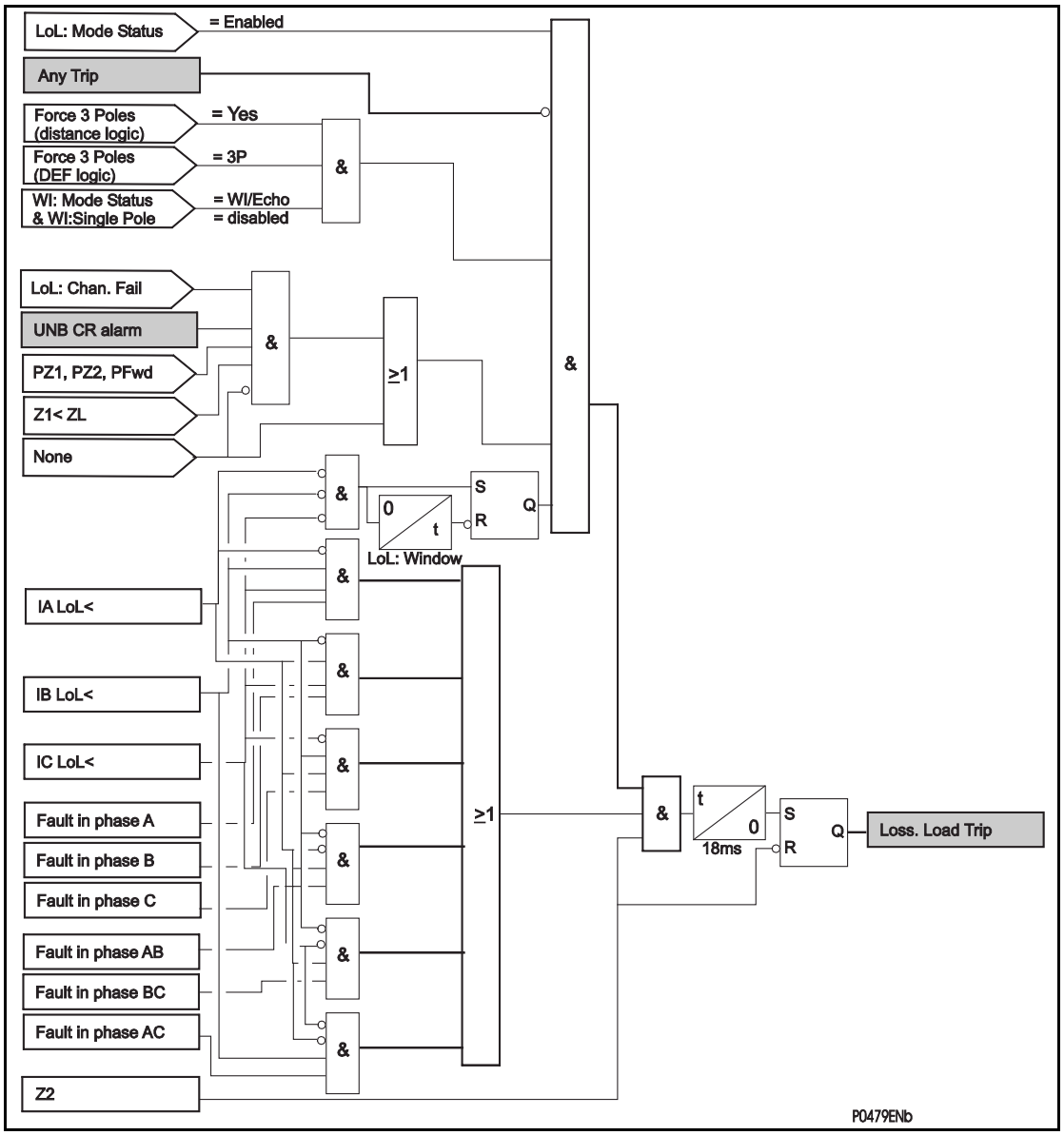


Figure 57: Loss of load trip logic

Where:

	Description
PZ1, PZ2, PFwd, None	Underreach scheme: Z1 < ZL: Permissive underreach Z1, Z2 or forward None: no distance scheme (basic scheme)
Z1<ZL	Underreach scheme in Z1
Z2'	Fault in Z2 (lockout by Power swing or Reversal Guard)

3.5.3 Trip logic and Zone 1 extension logic

The following trip logic completes the distance protection by zone:

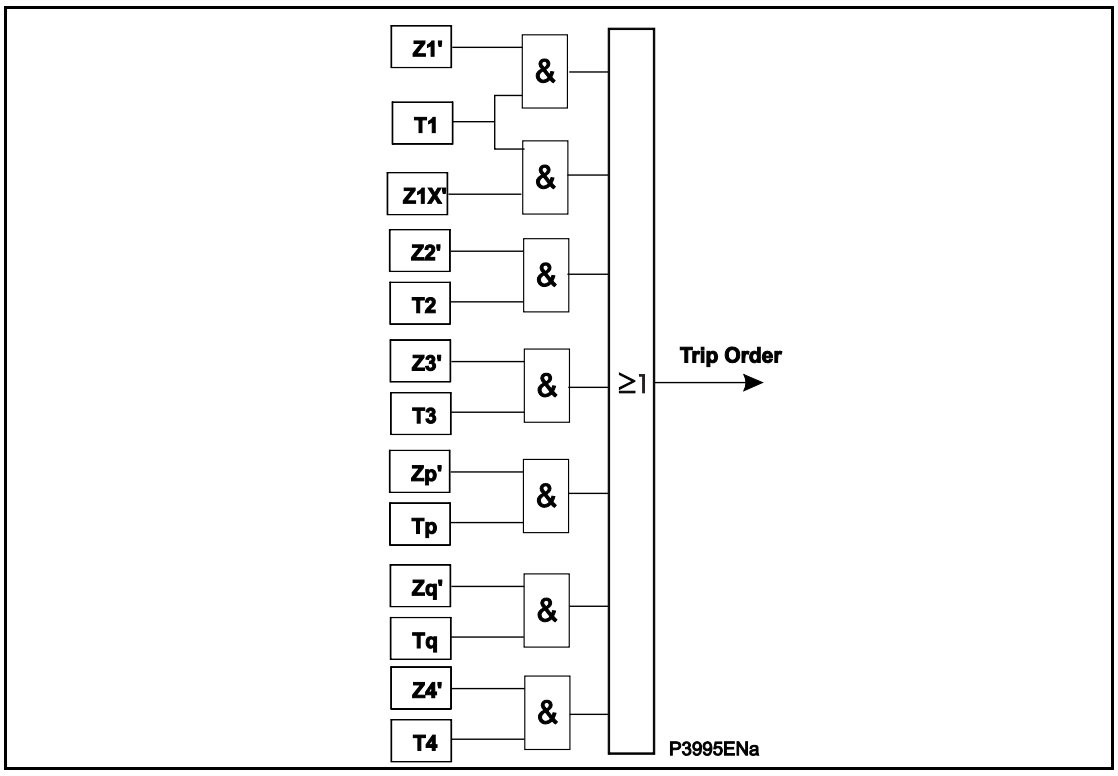


Figure 58: Trip and Z1X trip logic

Z1X can be used as well as the default scheme logic in case of UNB _Alarm-carrier out of service (See unblocking logic – Section 3.2.6)

3.5.4 Distance trip equation

The following equation summarizes the distance trip equation (previously shown in logic diagrams):

Distance Trip logic (*) =

Z1 . T1 . $\overline{BZ1}$. $\overline{PZ1}$

\+ Z1x' . (None + Z1xChannel_Fail . 'COS alarm').(T1 . INP_Z1EXT)

\+ 'DIST. UNB CR' . T1 . [PZ1 . Z1' + PZ2 . Z2' + PFwd . Aval']

\+ $\overline{UNB_CR}$. T1 . 'Aid Dist Delay' + 'DIST. COS') . [Z1' . BZ1 + (Z2' . BZ2 . $\overline{INP_COS}$ **Error! Bookmark not defined.**)]

\+ T2 [Z2' + PZ1 . Z1' + BZ1 . Z1']

\+ Z3' . T3

\+ Zp' . TZp

\+ Zq' . TZq

\+ Z4'. T4

Remarks:
1. In case of Carrier Out of Service (COS), the logic swaps back to a basic scheme.
2. inputs Zx must be polarised for activating Zx logic.

Remarks:
1. In case of COS (carrier out of service), the logic swap back to a basic scheme.
2. The inputs Z1X must be polarised for activating Z1X the logic.
3 For the 1P – 3P trip logic check in the Tripping logic section.

Accronyms used in the previous equation:

- Inputs:

	Description
T1 to, T2, T3, T4, TZp, TZq	Elapsed of Distance Timer 1 to 4 (T1 / T2 / T3 / TZp / TZq / T4)
'Aid Dist Delay'	Elapse of d transmission time in blocking scheme
Z1', Z2', Z3', ' to Z4' (*), Zp', Zq'	Detection of fault in zones 1 to 4 (lock out by PSWing or Rev Guard).
Forward'	Forward Fault Detection I (lockout by reversal guard)
UNB_CR	Carrier Received
INP_COS	Carrier Out of Service
None	Scheme without carrier
PZ1	Permissive scheme Z1
PZ2	Permissive scheme Z2
PFwd	Permissive Scheme with directional Fwd
BZ1	Blocking scheme Z1
BZ2	Blocking scheme Z2
INP_Z1EXT	Zone extension (digital input assigned to an opto input by dedicated PSL)
Z1xChannel Fail	Z1x logic enabled if channel fail detected (Carrier out of service = COS)
UNBAlarm	Carrier Out Of Service

- Outputs:

	Description
PDist_Dec	Distance protection Trip trip
CsZ1	Carrier send in case of zone 1 decision
CsZ2	Carrier send in case of zone 2 decision
CsZ4	Carrier send in case of zone 4 decision (Reverse)

4 APPLICATION OF INDIVIDUAL PROTECTION FUNCTIONS

4.1 Power Swing detection and blocking (PSB)

Power swings are caused by a lack of stability in the network with sudden load fluctuations. A power swing may cause the two sources connected by the protected line to go out of step (loss of synchronism) with each other.

The power swing detection element may be used to selectively prevent when the measured impedance point moves into the start-up characteristic from a power swing and still allows tripping for a fault (fault evolving during a power swing). The power swing detection element may also be used to selectively trip once an out-of-step condition has been declared.

Power swings are oscillations in power flow which can follow a power system disturbance. They can be caused by sudden removal of faults, loss of synchronism across a power system or changes in direction of power flow as a result of switching. Such disturbances can cause generators on the system to accelerate or decelerate to adapt to new power flow conditions, which in turn leads to power swinging. A power swing may cause the impedance presented to a distance relay to move away from the normal load area and into one or more of its tripping characteristics.

4.1.1 Power Swing Detection

A power swing is characterized by:

- A 3 successive impedance points in start-up zone of the biphase characteristic,
- A slow variation of current,
- A slow variation of voltage.

On the contrary a fault is characterized by a rapid (instantaneous) and “exaggerated” variation of current.

Power Swing detection uses a ΔR (resistive) and ΔX (reactive) impedance band which surrounds the entire biphase fault trip characteristic.

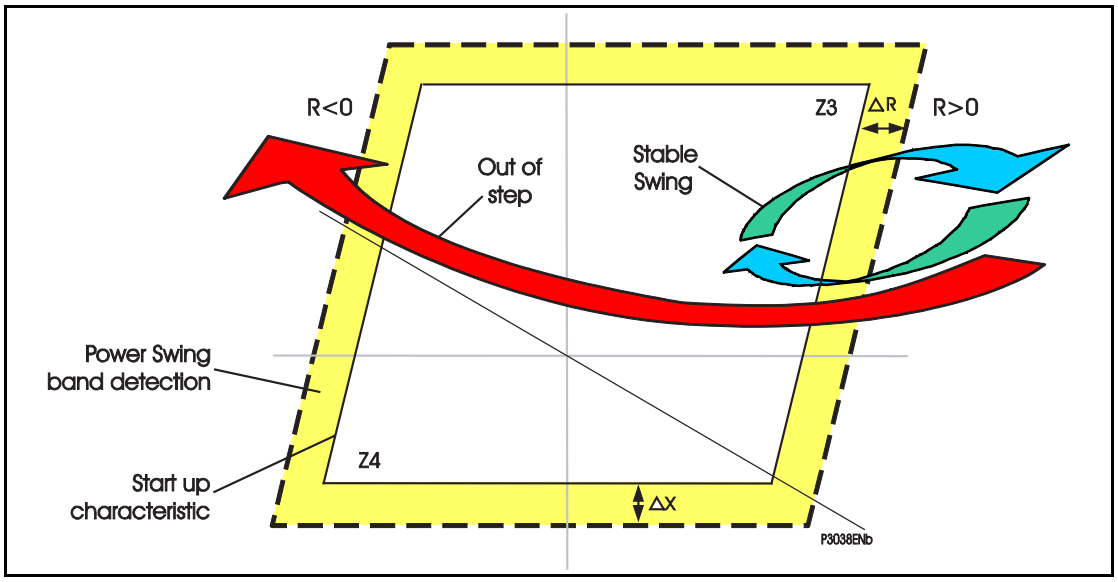


Figure 59: Biphase power swing characteristic

A power swing is detected when all 3 phase to phase impedances have remained within the ΔR for at least 3 acquisition samples (5 ms at 50Hz) and have taken longer than 5 ms to reach the trip characteristic.

More precisely, a power swing is detected and declared if:

- At least one phase-phase impedance is within the start-up zone after having crossed the power swing band in more than 5 ms.

- The three impedance points have been in the power swing band for more than 5ms.
- At least two poles of the breaker are closed (impedance measurement possible on two phases).

Note:	*During Power swing the residual compensation factors k0 are not applied in the detection of the characteristic.(the extended limit in R gives: R1=R2=R3=RpFwd)*

4.1.1.1 Line in one pole open condition (during single-pole trip)

In this case, the power swing occurs only on two phases. A power swing is detected if:

- At least one phase-phase impedance is within the start-up zone after having crossed the power swing band in more than 5ms.
- The two impedance points have been in the power swing band for more than 5 ms.

Note:	*During an open-pole condition, the P44x monitors the power swing on the healthy phase-phase loop. No external information is needed if the voltage transformers are on the line side. If the voltage transformers are on the bus side, the "pole discrepancy" signal should be used. The "pole discrepancy" input represents a "one-circuit-breaker-pole-open" condition.*

4.1.1.2 Conditions for isolating lines

If there is a power swing, it may be necessary to disconnect the two out-of-step sources. There are various tripping and blocking options available that are used to select if the line has to be tripped for power swings or not.

The selective blocking of back up zones only allows the P44x to separate the network near the electrical zero by tripping zone 1 only. Therefore, in the example given below, the relay D trips out.

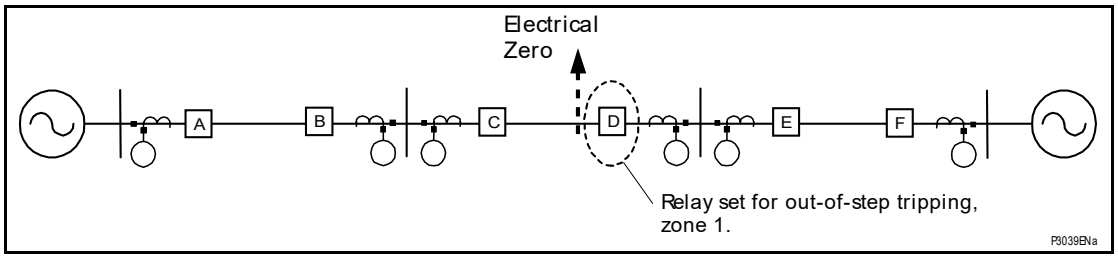


Figure 60: Selective protection blocking

4.1.1.3 Power Swing inside the Load Blinder Area

If the Impedance locus is located in the Load Blinder area (refer to section 4.2), either due to a Load condition or a Power Swing (detected as previously described) and start to move, the following alternative calculation for power swing takes place:

Simplified formula:

Power swing condition will be raised if the all three phase to phase impedance loops move between min and max speed,

With:

Min speed (ohm/Sec) = $25/\sqrt{Unblocking\ Delay}$

Max speed (ohm/sec) = 225 * ((Delta R + 2*Delta X)/2)

Unblocking delay setting under Power Swing Setting Column in seconds

Delta R (ΔR) and Delta X (ΔX) Settings under Power Swing Setting Column in ohms

For instance:

If Delta R and DeltaX selected are around 1 ohm (Delta X=1ohm, Delta R=2 ohms as it is the full loop),

From section 3.4.1.12 Power Swing Band:

$\Delta R = 0.032 \times \Delta f \times RLOAD$ (Formula for middle Power Swing point i.e. Electrical Centre)

And estimating RLoad for a 1 Amp relay as $((115 / \sqrt{3})V / 1A) = 63.5$ ohms,

We will be expecting frequency Swings from 0.5 to 1 Hz and an unblocking delay equal 2 or 3 seconds is adequated setting.

Power swing wave will be detected if speed is 15 Ohm/sec < Speed < 450 Ohm/sec

4.1.2 Stable Swing and Out Of Step

The relay is able to distinguish 2 types of Power Swing:

- Stable Swing
- Out Of Step (OOS).

In case of a “Stable Swing” the sigh of the resistance value at the instant the impedance enters the characteristic is the same as the sign of the resistance value at the instant the impedance goes out from the characteristic (see Figure 59)

In case of an Out Of Step, the sign of the resistance value at the instant the impedance enters the characteristic is opposite to the sign of the resistance value at the instant the impedance goes out from the characteristic (see Figure 59).

An out of Step is a loss of synchronism.

In both cases the considered characteristic is the biphase loop characteristic. In other words the phase to phase impedance is considered to perform Power Swing detection.

The Protection relay is able to count how many Stable Swings and how many Out of step Occurs.

It is possible in MiCOM S1 Agile to set a number of out of step threshold above which a DDB (Out Of Step Conf DDB#352) is triggered

4.1.3 Biphase loop

To decide what loop (what phases) has to be monitored 2 distinct algorithms are run:

- An exaggerated Delta current algorithm
- A Flat algorithm

4.1.4 Power Swing blocking

As soon as a power swing is detected the protection relay is blocked (“Power swing blocking”). The Power Swing blocking algorithm prevents the protection relay from tripping due to a power swing.

Power Swing blocking can be enabled or disabled per zone through “Blocking Zones” setting.

If any or all of the distance zones are blocked, related trips are blocked including aided trip logic.

For non-blocked zones, the swing indication is provided without tripping.

It is possible to limit the time for which blocking of any distance protection zones is applied. For example, unblocking timer is used to override any blocked zone. Therefore, certain

locations on the power system can be designed as split points, where circuit breakers will trip 3 phase in to stabilize.

Power swing blocking is automatically removed after “unblocking delay”.

This is used to separate the sources (open the breaker, 3-phase trip) in the event that a block was taking place, and the impedance remained in the blocked zone for a relatively long time. This would indicate a serious overcurrent condition as a result of too great a power transfer after a disturbance (a power swing that does not pass through or recover). If the impedance point moves out of the start-up characteristic again before the time delay expires, a trip is not issued and the adjustable time delay is reset.

Note:	*Power Swing Blocking can be disabled (for distribution systems). Power Swings should not happen at Distribution voltage levels.*

4.1.5 Power Swing unblocking (unblocking of the relay for faults during power swing)

If a fault occurs while the power swing blocking algorithm is on going the Power Swing blocking algorithm is unblocked so that the protection relay can protect from the occurring fault (by tripping).

- The relay operates normally for any fault occurring during a power swing

4 fault detection criteria can unblock the “Power Swing blocking”:

- **Residual Current** (IN> status setting) criterion:
  This allows tripping for earth faults occurring during a power swing

  0.1 In + (kr x Imax(t)) *

  If Residual current condition is true for more than 40ms, then Power Blocking is unblocked.
- **Negative Sequence Current** (I2> status setting) criterion:
  This allows tripping for phase to phase faults occurring during a power swing.

  0.1 In + (ki x Imax(t)) *

  If Negative Sequence Current condition is true for more than 40ms, then Power Blocking is unblocked.
- * Where:
  kr = an adjustable coefficient for residual or zero sequence current (3I0),
  ki: = an adjustable coefficient for negative sequence current (I2),
  Imax(t): maximum instantaneous current detected on one phase (A, B or C),
  In: nominal current
- **Phase current threshold** (ImaxLine> status setting) criterion:
  This allows tripping for 3 phase faults occurring during a power swing.
- **Delta I criterion** (‘Delta I status’ setting)
  This allows tripping for 3 phase faults occurring during a power swing even if the fault current is lower than ImaxLine>
  - condition 1: There is an exaggerated Delta I
  - condition 2: There is an absence of current variation on biphases loop.

If there is a delta exaggerated current (condition1 = true) and there is an absence of variation of current (condition 2 = true) for more than 100ms then Power Swing blocking is unblocked.

If there isn’t any delta exaggerated current (condition1 = false) and there is an absence of variation of current (condition 2) for more than 200ms then Power Swing blocking is unblocked.

4.1.6 What loop is faulty?

The delta quantity calculated by delta exaggerated algorithm is used to determine which loop is chosen.

The identified faulty loop will lead to a trip in case of the power swing blocking is unblocked. This step is a way to accelerate the determination of the faulty loop an, therefore, a trip.

Note:	*Even if Delta I status is disabled, exaggerated delta current is always internally calculated.*

Regarding the presence of negative sequence current or residual current the exaggerated delta current detection are calculated on the phase to phase loop or phase to ground loop.

On what phase(s) is there the fault?

Input : I_AB, I_BC, I_CA (rms values)
I_AB = IB – IA

If I_AB > ($\sqrt{3}$ × 0.6 × In) then a ‘CN Fault is detected.

If I_BC > ($\sqrt{3}$ × 0.6 × In) then a ‘AN Fault is detected.

If I_CA > ($\sqrt{3}$ × 0.6 × In) then a ‘BN Fault is detected.

Caution: **During a Power Swing, all Directional elements are disabled (it is not possible to determine fault direction during a Power Swing).**

4.1.6.1 Power Swing detection and blocking logic

The next figure summarizes power swing logic (detection and blocking):

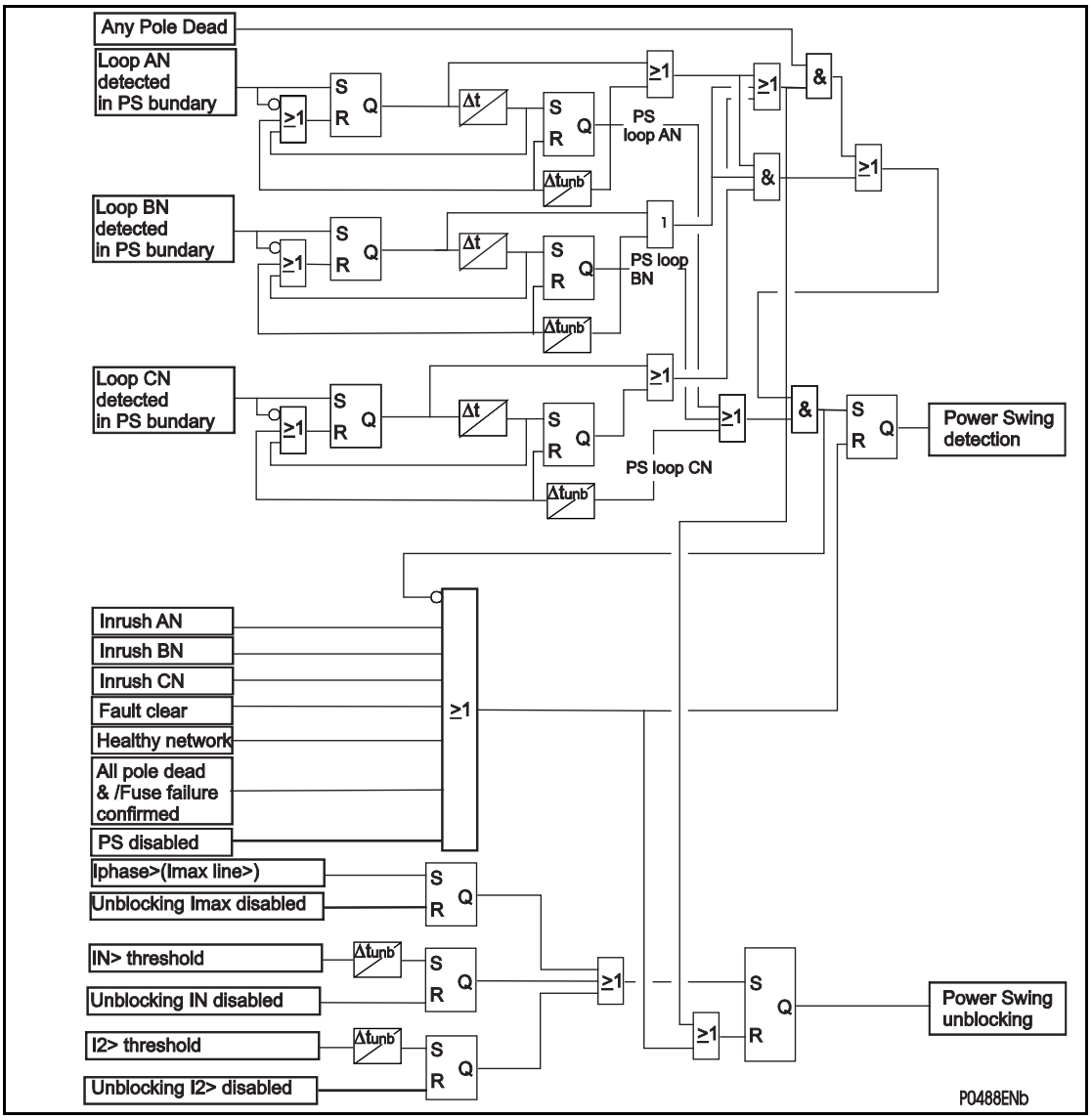


Figure 61: Power swing detection & unblocking logic

4.2 Load blinding (load avoidance)

Load blinders are provided for both phase and ground fault distance elements, to prevent misoperation (mal-tripping) for heavy load flow. The purpose is to configure a blinder envelope which surrounds the expected worst case load limits, and to block tripping for any impedance measured within the blinded region. Only a fault impedance which is outside of the load area is allowed to cause a trip. The blinder characteristics are shown in Figure 62: Load blinder characteristics.

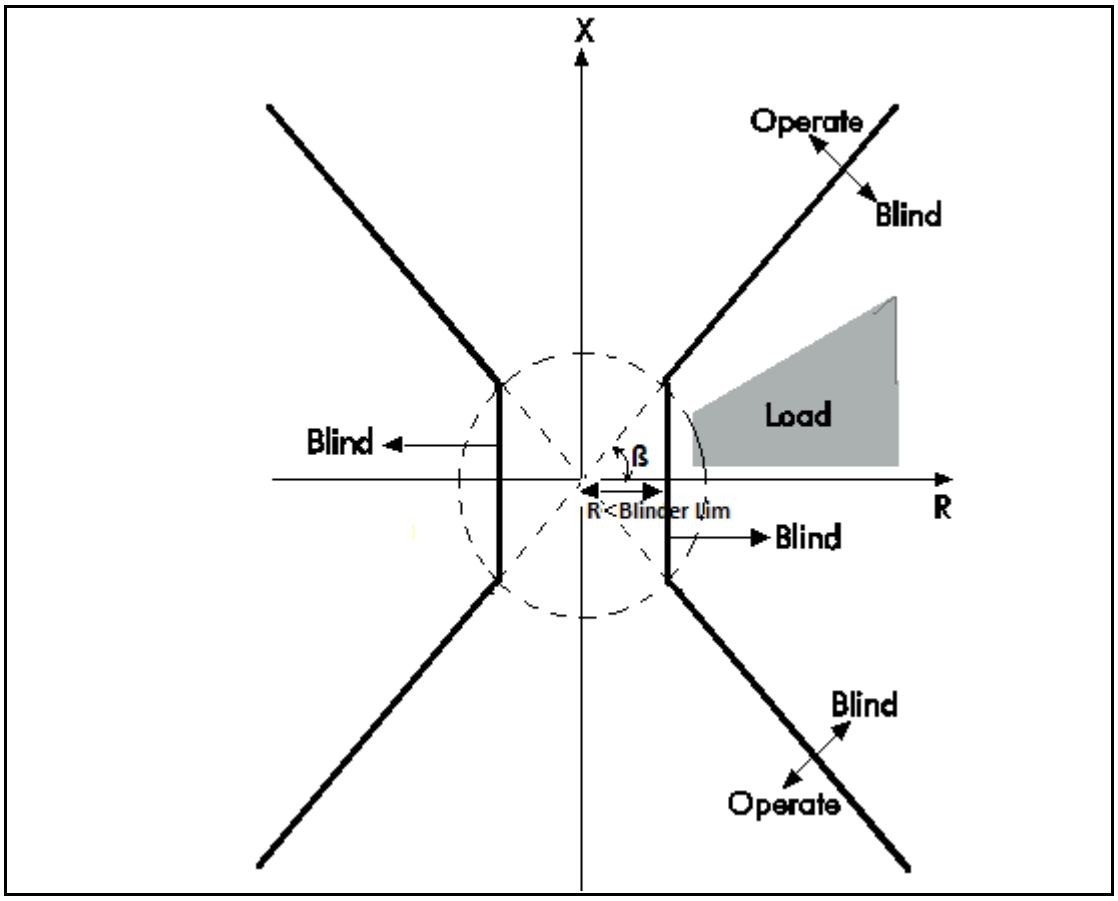


Figure 62: Load blinder characteristics

- R< Blinder Lim denotes the Load/B Resistance setting. This sets the cutoff of the underimpedance .
- ß denotes the Load/B Angle setting. This sets the angle of the two blinder boundary lines - the gradient of the rise or fall with respect to the resistive axis.

The P44x has a facility to allow the load blinder to be bypassed any time if:

- The measured voltage for the phase in question falls below an undervoltage V< setting.
- A Delta Transition is confirmed. If load Blinder is enabled, an alternative Voltage Delta threshold is used. A transition is confirmed by checking the values of ΔV AND ΔI. If three consecutive samples for at least one loop are:

ΔV > threshold VLB,

where threshold VLB = [((Un - Load Blinder V<) / Un) – 0.1] Un

ΔV threshold VLB is limited to 10% to 50% of Un

and

ΔI > threshold I, where threshold I = 0.2 In.

The start-up of the high-speed algorithms are confirmed

Under such circumstances, the low voltage could not be explained by normal voltage excursion tolerances on-load. A fault is definitely present on the phase in question, and it is acceptable to override the blinder action and allow the distance zones to trip according to the entire zone shape. The benefit is that the resistive coverage for faults near to the IED location can be higher.

For security, it is highly recommended that the blinder is Enabled, especially for lines above 150 km (90 miles), to prevent non-harmonic low-frequency transients causing load encroachment problems, and for any networks where power swings might be experienced.

The impedance blinder radius i.e. R<Blinder Lim/Cos ß, must lower than the worst-case loading as shown in the figure below. This is often taken as 120% overloading in one line, multiplied by two to account for increased loading during outages or fault clearance in an adjacent parallel circuit. Then an additional allowance for measuring tolerances results in a recommended setting typically 1/3rd of the rated full load current:

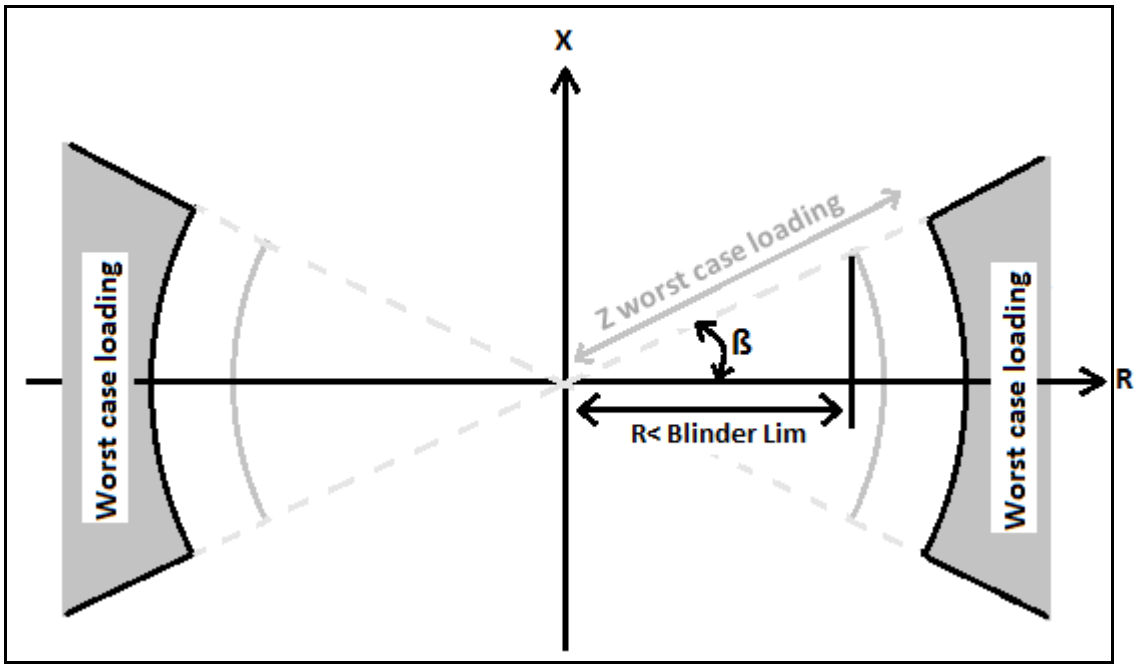


Figure 63: Load blinder setting

Z < (Rated phase voltage Vn)/(IFLC x 3) , Therefore;

R< Blinder Lim < (Rated phase voltage Vn * Cosß)/(IFLC x 3)

FLC = Full Load Current

When the load is at the worst-case power factor, it should remain below the beta setting. So, if we assume a typical worst-case 0.85 power factor, then:

ß > Cos-1 (0.85) plus 15° margin > 47°

and to ensure that line faults are detected, ß < (Line Angle -15°).

In practice, an angle half way between the worst-case leading load angle, and the protected line impedance angle, is often used.

The undervoltage setting“ Load Blinder V< “ must be lower than the lowest phase-neutral voltage under heavy load flow and depressed system voltage conditions. The typical maximum V< setting is 70% Vn.

Load Blinder V<

4.3 Directional and non-directional overcurrent protection

4.3.1 Inverse time characteristics

The inverse time-delay characteristics listed above comply with the following formula:

$$t = T \times \left(\frac{K}{(I/Is)^{a} - 1} + L \right)$$

Where:

t = operation time
K = constant
I = measured current
Is = current threshold setting
α = constant
L = ANSI/IEEE constant (zero for IEC curves)
T = Time multiplier Setting

Curve description	Standard	K constant	α constant	L constant
Standard Inverse	IEC	0.14	0.02	0
Very Inverse	IEC	13.5	1	0
Extremely Inverse	IEC	80	2	0
Long Time Inverse	UK	120	1	0
Moderately Inverse	IEEE	0.0515	0.02	0.0114
Very Inverse	IEEE	19.61	2	0.491
Extremely Inverse	IEEE	28.2	2	0.1217
Inverse	US	5.95	2	0.18
Short Time Inverse	US	0.02394	0.02	0.1694

The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is employed for the IEEE/US curves. Both the TMS and Time Dial settings act as multipliers on the basic characteristics but the scaling of the time dial is 10 times that of the TMS, as shown in the previous menu. The menu is arranged such that if an IEC/UK curve is selected, the **I> Time Dial** cell is not visible and vice versa for the **TMS** setting.

4.3.2 Application of Timer Hold Facility

The first two stages of overcurrent protection in the P442 and P444 relays are provided with a timer hold facility, which may either be set to zero or to a definite time value (Note that if an IEEE/US operate curve is selected, the reset characteristic may be set to either definite or inverse time in cell **I>1 Reset Char**; otherwise this setting cell is not visible in the menu). Setting of the timer to zero means that the overcurrent timer for that stage will reset instantaneously once the current falls below 95% of the current setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. This may be useful in certain applications, for example when grading with upstream electromechanical overcurrent relays that have inherent reset time delays.

Another possible situation where the timer hold facility may be used to reduce fault clearance times is where intermittent faults may be experienced. An example of this may occur in a plastic insulated cable. In this application it is possible that the fault energy melts and reseals the cable insulation, thereby extinguishing the fault. This process repeats to give a succession of fault current pulses, each of increasing duration with reducing intervals between the pulses, until the fault becomes permanent. When the reset time of the overcurrent relay is instantaneous the relay may not trip until the fault becomes permanent. By using the timer hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time.

Note that the timer hold facility should not be used where high speed autoreclose with short dead times are set.

The timer hold facility can be found for the first and second overcurrent stages as settings **I>1 tRESET** and **I>2 tRESET**. Note that these cells are not visible if an inverse time reset characteristic has been selected, as the reset time is then determined by the programmed time dial setting.

4.3.3 Directional Overcurrent Protection

If fault current can flow in both directions through a relay location, it is necessary to add directional control to the overcurrent relays to obtain correct discrimination. Typical systems that require such protection are parallel feeders and ring main systems. Where I>1 or I>2 stages are directionalised, no characteristic angle needs to be set as the relay uses the same directionalising technique as for the distance zones (fixed superimposed power technique).

4.3.4 Time Delay VTS

Should the Voltage Transformer Supervision function detect an ac voltage input failure to the relay, such as due to a VT fuse blow, this will affect operation of voltage dependent protection elements. Distance protection will not be able to make a forward or reverse decision, and so will be blocked. As the I>1 and I>2 overcurrent elements in the relay use the same directionalising technique as for the distance zones, any directional zones would be unable to trip.

To maintain protection during periods of VTS detected failure, the relay allows an **I> Time Delay VTS** to be applied to the I>1 and I>2 elements. On VTS pickup, both elements are forced to have non-directional operation, and are subject to their revised definite time delay.

4.3.5 Setting Guidelines

I>1 and I>2 Overcurrent Protection

When applying the overcurrent or directional overcurrent protection provided in the P442 and P444 relays, standard principles should be applied in calculating the necessary current and time settings for co-ordination. In general, where overcurrent elements are set, these should also be set to time discriminate with downstream and reverse distance protection. The I>1 and I>2 elements are continuously active. However, tripping is blocked if the distance protection function starts. An example is shown in Figure 64.

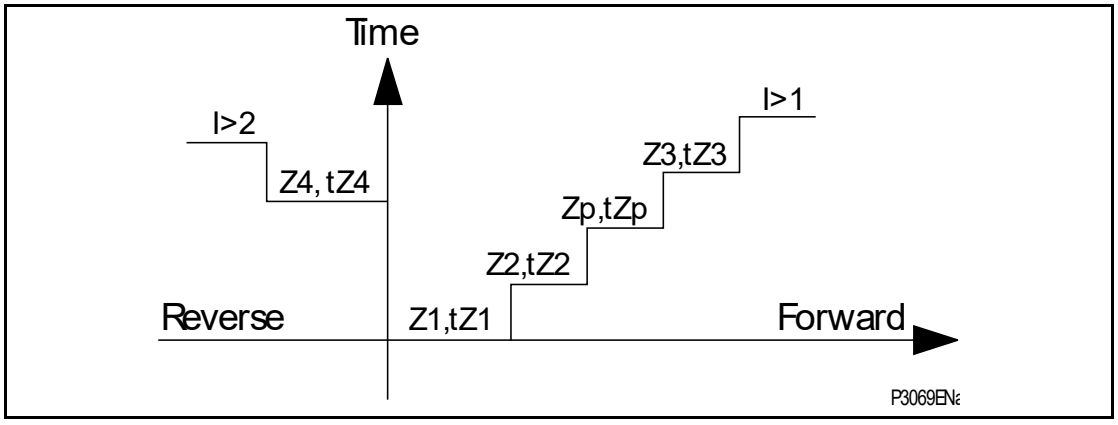


Figure 64: Time grading overcurrent protection with distance protection (DT example)

I>1 and I>2 Time Delay VTS

The I>1 and I>2 overcurrent elements should be set to mimic operation of distance protection during VTS pickup. This requires I>1 and I>2 current settings to be calculated to approximate to distance zone reaches, although operating non-directional. If fast protection is the main priority then a time delay of zero or equal to tZ2 could be used. If parallel current-based main protection is used alongside the relay, and protection discrimination remains the priority, then a DT setting greater than that for the distance zones should be used. An example is shown in Figure 65.

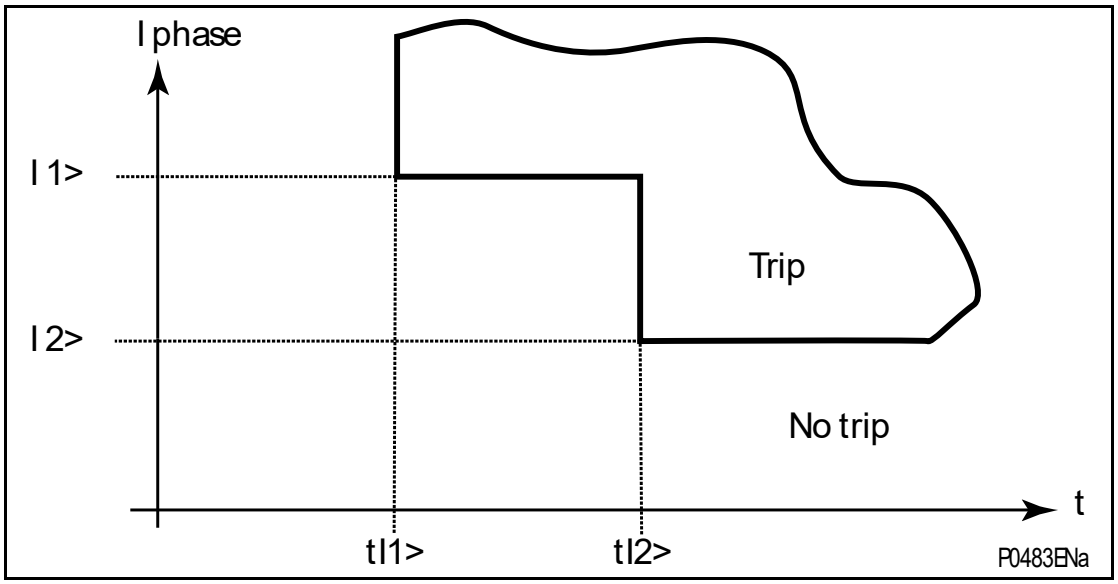


Figure 65: Tripping logic for phase overcurrent protection

I>3 Highset Overcurrent and Switch on to Fault Protection

The I>3 overcurrent element of the P442 and P444 relays can be Enabled as an instantaneous highset just during the TOR/SOTF period. After this period has ended, the element remains in service with a trip time delay setting **I>3 Time Delay**. This element would trip for close-up high current faults, such as those where maintenance earth clamps are inadvertently left in position on line energisation.

The I>3 current setting applied should be above load current, and > 35% of peak magnetising inrush current for any connected transformers as this element has no second harmonic blocking. If a high current setting is chosen, such that the I>3 element will not overreach the protected line, then the I>3 Time Delay can be set to zero. The remote source should not not be sufficiently strong to cause element pickup for a close-up reverse fault.

If a low current setting is chosen, I>3 will need to discriminate with local and remote distance protection. This principle is shown in Table 8: .

I>3 Current Setting	Instantaneous TOR/SOTF Function	Function After TOR/SOTF Period	Time Delay Required
Above load and inrush current but LOW	Yes - sensitive.	Time delayed backup protection.	Longer than tZ3 to grade with distance protection.
HIGH, ≥ 120% of max. fault current for a fault at the remote line terminal and max. reverse fault current	Yes - may detect high current close-up faults.	Instantaneous highset to detect close-up faults.	I>3 Time Delay = 0. (Note #.)

Table 8: Current and Time delay settings for the I>3 element

Key:

As the instantaneous highset trips three pole it is recommended that the I>3 Time Delay is set ≥ tZ2 in single pole tripping schemes, to allow operation of the correct single pole autoreclose cycle.

I>4 Stub Bus Protection

When the protected line is switched from a breaker and a half arrangement it is possible to use the I>4 overcurrent element to provide stub bus protection. When stub bus protection is selected in the relay menu, the element is only enabled when the opto input Stub Bus Isolator Open (**Stub Bus Enable**) is energised. Therefore, a set of 52b auxiliary contacts (closed when the isolator is open) is required.

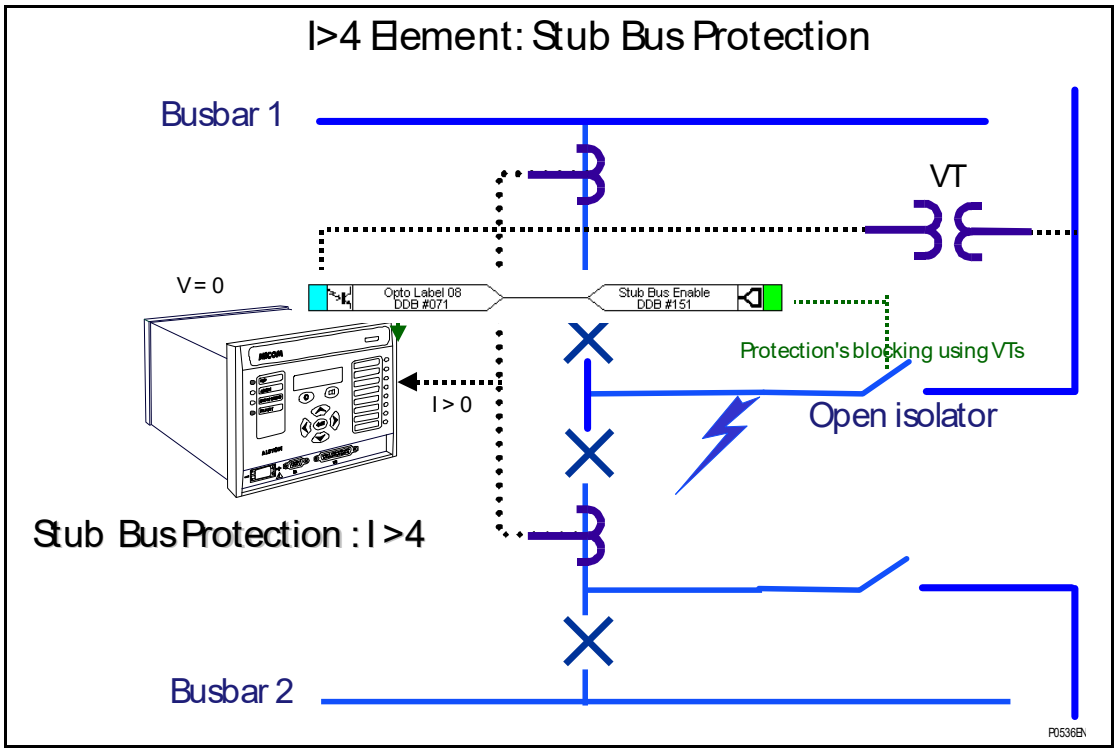


Figure 66: I>4 stub bus protection

Although this element would not need to discriminate with load current, it is still common practice to apply a high current setting. This avoids maloperation for heavy through fault currents, where mismatched CT saturation could present a spill current to the relay. The I>4 element would normally be set instantaneous, t>4 = 0 s.

4.4 Negative Sequence Overcurrent Protection

4.4.1 Setting guidelines

The MiCOM P44x negative sequence overcurrent protection elements include four thresholds. The first and the second thresholds can be set as DT or IDMT trip delay time. The curves are the same as for the directional and non directional overcurrent protection.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load unbalance on the system. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

Where the negative phase sequence element is required to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based upon an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

Note that in practice, if the required fault study information is not available, the setting must adhere to the minimum threshold previously outlined, employing a suitable time delay for co-ordination with downstream devices. This is vital to prevent unnecessary interruption of the supply resulting from inadvertent operation of this element.

A correct setting of the time delay is vital. It should also be noted that this element is applied primarily to provide back-up protection to other protective devices or to provide an alarm. Hence, in practice, it would be associated with a long time-delay.

It must be ensured that the time delay is set greater than the operating time of any other protective device (at minimum fault level) on the system which may respond to unbalanced faults, such as:

- Phase overcurrent elements

- Earth fault elements
- Broken conductor elements
- Negative phase sequence influenced thermal elements

4.4.2 Directionalising the Negative Phase Sequence Overcurrent Element

Directionality is achieved by comparison of the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (**I2> Char Angle**) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (- V_2), to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent upon the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the RCA should be set equal to -60°
- For a distribution system the RCA should be set equal to -45°

4.5 Maximum of Residual Power Protection – Zero Sequence Power Protection ("Zero Seq Power" menu)

The aim of this protection is to provide the system with selective and autonomous protection against resistive phase to ground faults. High resistive faults such as vegetation fires cannot be detected by distance protection.

When a phase to ground fault occurs, the fault can be considered as a zero-sequence power generator. Zero-sequence voltage is at maximum value at the fault point. Zero-sequence power is, therefore, also at maximum value at the same point. Supposing that zero-sequence current is constant, zero-sequence power will decrease along the lines until null value at the source's neutral points (see below).

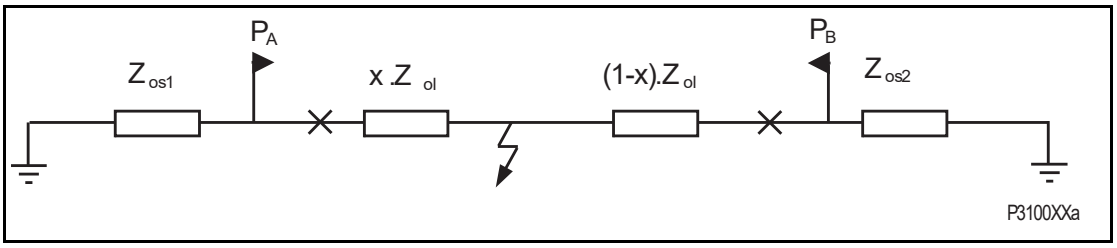


Figure 67: Zero sequence

Where:
Zos1: = Zero-sequence source side 1 impedance
Zol = Zero-sequence line impedance
Zos2 = Zero-sequence source side 2 impedance
x = Distance to the fault from P_A.

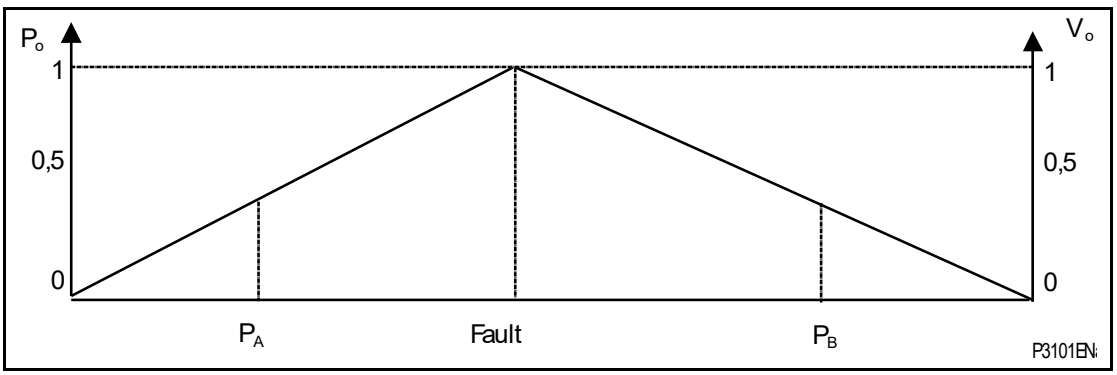


Figure 68: Zero sequence decreasing along the line

Selective fault clearance of the protection for forward faults is provided by the power measurement combined with a time-delay inversely proportional to the measured power.

This protection function does not issue any trip command for reverse faults.

In compliance with sign conventions (the zero-sequence power flows from the fault towards the sources) and with a mean characteristic angle of the zero-sequence source impedances of the equal to 75°, the measured power is determined by the following formula:

$$Sr = Vr_{r.m.s} \times Ir_{r.m.s} \times \cos(\varphi - \varphi_0)$$

Where:

φ = Phase shift between Vr and Ir

φ_0 = 255° or – 75°

$Vr_{r.m.s}$, $Ir_{r.m.s}$ = R.M.S values of the residual voltage and current

The Vr and Ir values are filtered to eliminate the effect of the 3rd and 5th harmonics.

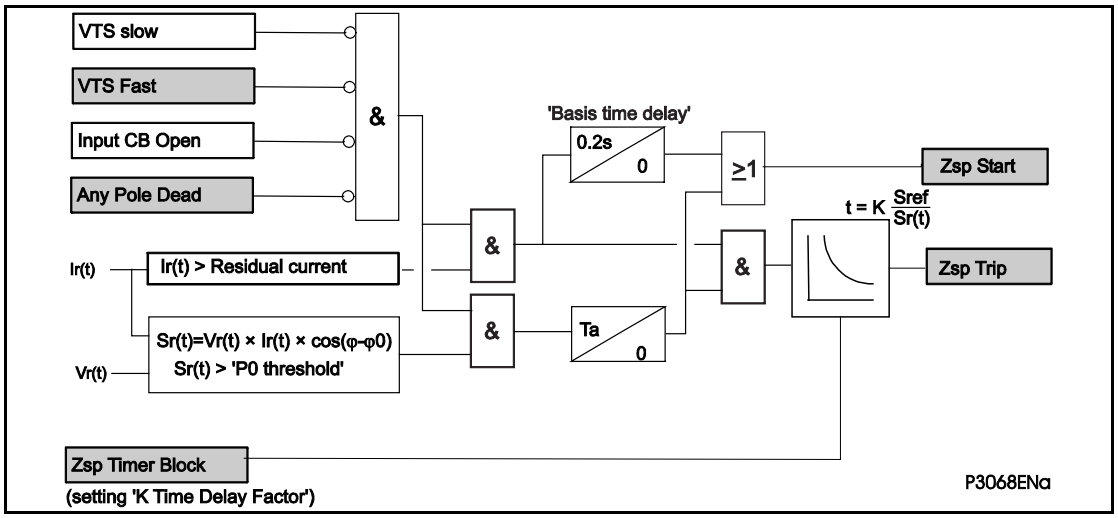


Figure 69: Zero sequence power logic

3-pole trip is sent out when the residual power threshold “Residual Power" is overshot, after a time-delay (‘**Basis Time Delay**’) and an IDMT time-delay adjusted by the “K” time delay factor.

The basis time-delay is set at a value greater than the second stage time of the distance protection of the concerned feeder if the 3-pole trip is active, or at a value greater than the single-phase cycle time if single-pole autorecloser shots are active.

Ta time-delay is fixed (200 ms) and starts with residual current.

The IDMT time-delay is determined by the following formula:

$$t = K \times (S_{ref}/S_r)$$

Where:

K = Adjustable time constant from 0 to 2sec (‘**K Time Delay Factor**’ setting)

S_{ref} = Reference residual power, depending on the CT:
10 VA for In = 1A
50 VA for In = 5A

S_r = Residual power generated by the fault

1.1 Broken conductor detection

The majority of faults on a power system occur between one phase and ground or two phases and ground. These are known as shunt faults and arise from lightning discharges and other overvoltages which initiate flashovers. Alternatively, they may arise from other causes such as birds on overhead lines or mechanical damage to cables etc. Such faults result in an appreciable increase in current and hence in the majority of applications are easily detectable.

Another type of unbalanced fault which can occur on the system is the series or open circuit fault. These can arise from broken conductors, maloperation of single phase switchgear, or the operation of fuses. Series faults will not cause an increase in phase current on the system and hence are not readily detectable by standard overcurrent relays. However, they will produce an unbalance and a resultant level of negative phase sequence current, which can be detected.

It is possible to apply a negative phase sequence overcurrent relay to detect the above condition. However, on a lightly loaded line, the negative sequence current resulting from a series fault condition may be very close to, or less than, the full load steady state unbalance arising from CT errors, load unbalance etc. A negative sequence element therefore would not operate at low load levels.

The relay incorporates an element which measures the ratio of negative to positive phase sequence current (I_2/I_1). This will be affected to a lesser extent than the measurement of negative sequence current alone, since the ratio is approximately constant with variations in load current. Therefore, a more sensitive setting may be achieved.

The following table shows the relay menu for the Broken Conductor protection, including the available setting ranges and factory defaults:

4.5.1 Setting guidelines

In the case of a single point earthed power system, there will be little zero sequence current flow and the ratio of I2/I1 that flows in the protected circuit will approach 100%. In the case of a multiple earthed power system (assuming equal impedances in each sequence network), the ratio I2/I1 will be 50%.

It is possible to calculate the ratio of I2/I1 that will occur for varying system impedances, by referring to the following equations:

$$I_{1F} = \frac{E_g\left(Z_2 + Z_0\right)}{Z_1Z_2 + Z_1Z_0 + Z_2Z_0}$$

$$I_{2F} = \frac{-E_gZ_0}{Z_1Z_2 + Z_1Z_0 + Z_2Z_0}$$

Where:

E_g	=	System Voltage
Z_0	=	Zero sequence impedance
Z_1	=	Positive sequence impedance
Z_2	=	Negative sequence impedance

Therefore:

$$\frac{I_{2F}}{I_{1F}} = \frac{Z_0}{Z_0 + Z_2}$$

It follows that, for an open circuit in a particular part of the system, I2/I1 can be determined from the ratio of zero sequence to negative sequence impedance. It must be noted however, that this ratio may vary depending upon the fault location. It is desirable therefore to apply as sensitive a setting as possible. In practice, this minimum setting is governed by the levels of standing negative phase sequence current present on the system. This can be determined from a system study, or by making use of the relay measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single phase loads are accounted for.

Note that a minimum value of 8% negative phase sequence current is required for successful relay operation.

Since sensitive settings have been employed, it can be expected that the element will operate for any unbalance condition occurring on the system (for example, during a single pole autoreclose cycle). Hence, a long time-delay is necessary to ensure co-ordination with other protective devices. A 60 second time-delay setting may be typical.

4.5.2 Setting example

The following information was recorded by the relay during commissioning:

- $I_{full\ load}$ = 1000A
- I_2 = 100A

therefore the quiescent I2/I1 ratio is given by:

- I_2/I_1 = 100/1000 = 0.1

To allow for tolerances and load variations a setting of 200% of this value may be typical: Therefore set **I2/I1** = 0.2

Set **I2/I1 Time Delay** = 60 s to allow adequate time for short circuit fault clearance by time delayed protections.

4.6 Directional and non-directional earth fault protection

1.1.1 Setting guidelines

The MiCOM P44x negative sequence overcurrent protection elements include four thresholds. The first and the second thresholds can be set as DT or IDMT trip delay time. The curves are the same as for the directional and non directional overcurrent protection.

Note that the elements are set in terms of residual current, which is three times the magnitude of the zero sequence current (Ires = $3I_0$). The IDMT time-delay characteristics available for the IN>1 element, and the grading principles used will be as per the phase fault overcurrent elements.

To maintain protection during periods of VTS detected failure, the relay allows an **IN> Time Delay VTS** to be applied to the IN>1 and IN>2 elements. On VTS pickup, both elements are forced to have non-directional operation, and are subject to their revised definite time-²delay.

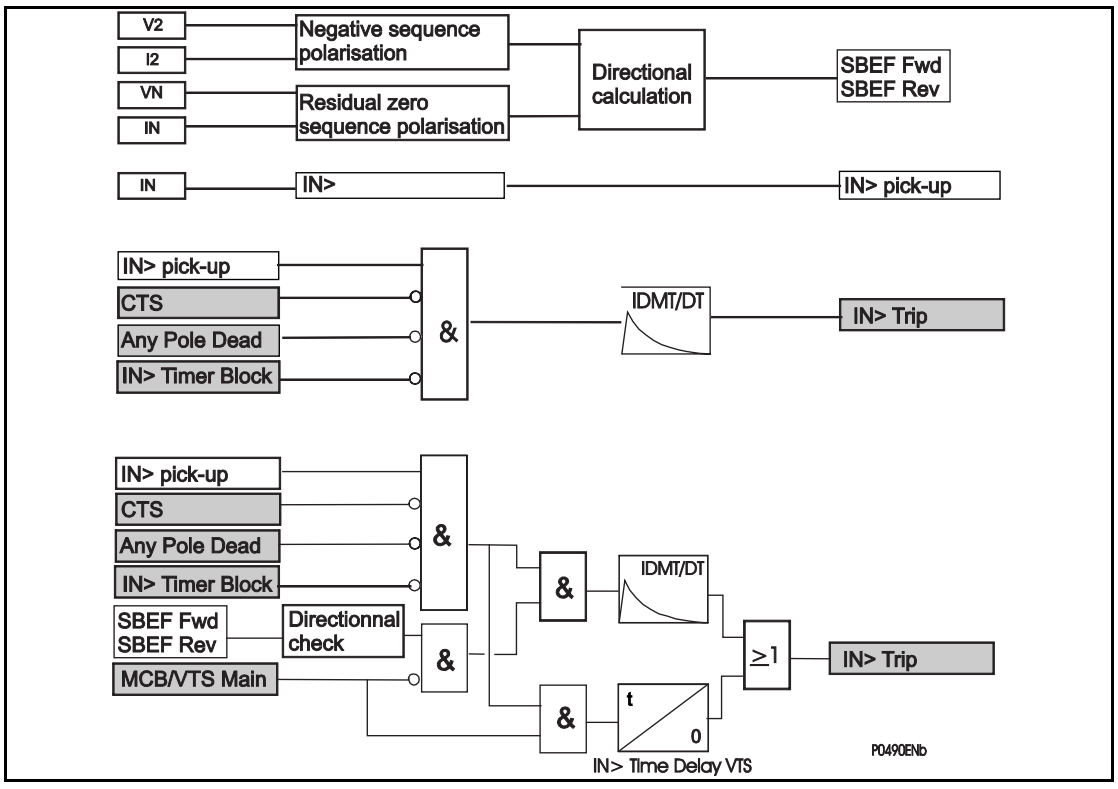


Figure 70: SBEF calculation & logic

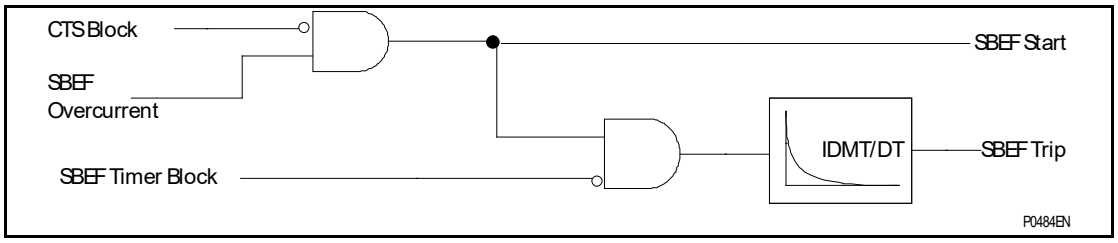


Figure 71: Logic without directionality

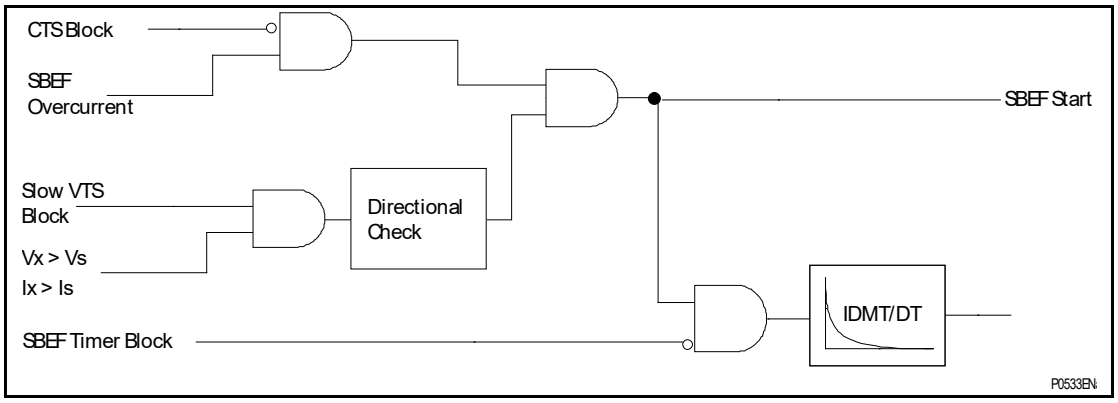


Figure 72: Logic with directionality

1.1.2 Directional Earth Fault Protection (DEF)

The method of directional polarising selected is common to all directional earth fault elements, including the channel-aided element. There are two options available in the relay menu:

- Zero sequence polarising - The relay performs a directional decision by comparing the phase angle of the residual current with respect to the inverted residual voltage: (–Vres = –(Va + Vb + Vc)) derived or measured by the relay. The application of zero sequence polarising is detailed in section 1.1.2.1.
- Negative sequence polarising - The relay performs a directional decision by comparing the phase angle of the derived negative sequence current with respect to the derived negative sequence voltage. The application of negative sequence polarising is detailed in section 1.1.2.2.

  Note: Even though the directional decision is based on the phase relationship of I_2 with respect to V_2, the operating current quantity for DEF elements remains the residual current.

1.1.2.1 Application of Zero Sequence Polarising

This is the conventional option, applied where there is not significant mutual coupling with a parallel line, and where the power system is not solidly earthed close to the relay location. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise DEF elements. The relay internally derives this voltage from the 3 phase voltage input which must be supplied from either a 5-limb or three single phase VT's. These types of VT design allow the passage of residual flux and consequently permit the relay to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. A three limb VT has no path for residual flux and is therefore incompatible with the use of zero sequence polarising.

The required characteristic angle (RCA) settings for DEF will differ depending on the application. Typical characteristic angle settings are as follows:

- Resistance earthed systems generally use a 0° RCA setting. This means that for a forward earth fault, the residual current is expected to be approximately in phase with the inverted residual voltage (-Vres).
- When protecting solidly-earthed distribution systems or cable feeders, a -45° RCA setting should be set.

- When protecting solidly-earthed transmission systems, a -60° RCA setting should be set.

1.1.2.2 Application of Negative Sequence Polarising

In certain applications, the use of residual voltage polarisation of DEF may either be not possible to achieve, or problematic. An example of the former case would be where a suitable type of VT was unavailable, for example if only a three limb VT were fitted. An example of the latter case would be an HV/EHV parallel line application where problems with zero sequence mutual coupling may exist. In either of these situations, the problem may be solved by the use of negative sequence quantities for polarisation. This method determines the fault direction by comparison of negative sequence voltage with negative sequence current. The operate quantity, however, is still residual current.

When negative sequence polarising is used, the relay requires that the Characteristic Angle is set. The Application Notes section for the Negative Sequence Overcurrent Protection better describes how the angle is calculated - typically set at - 45° (I_2 lags ($-V_2$)).

4.7 Aided Directional Earth Fault (DEF)

4.7.1 DEF Protection Against High Resistance Earth Faults

Protection against high-resistance earth faults, also called DEF (Directional Earth Fault), is used to protect the network against highly resistive faults. High resistance faults may not be detected by distance protection. DEF Protection can be applied in one of the two following modes: faults using the following:

- The main operating mode, directional comparison protection uses the signalling channel and is a communication-aided scheme.
- In backup-operating mode SBEF (Stand-By Earth Fault), an inverse/definite time earth overcurrent element with 4 stages is selectable.

Both the main and backup mode can use different methods for fault detection and directional determination (negative or zero sequence polarisation, RCA angle settable for backup SBEF protection, etc.)

The use of Aided-Trip logic in conjunction with the DEF element allows faster trip times, and can facilitate single-phase tripping if single-phase tripping is applied to the breaker.

The DEF directional comparison protection may be applied on the same signal channel as the distance protection, or it may be applied on an independent channel (ability to use two different aided-trip logics for the distance and DEF elements).

When used on the same signalling channel (shared scheme selected by MiCOM S1 Agile) as the distance protection, if the distance protection picks up, it has priority (the output from the DEF element is blocked from asserting the Carrier Send common output).

The use of directional comparison protection with an independent signalling channel allows the distance functions and DEF function to operate in parallel. Each function is routed to its own Carrier Send output. If an earth fault is present where both the distance and DEF elements pick up, the faster of the two functions will perform the trip.

4.7.1.1 High Resistance Earth Fault Detection

A high resistance fault is detected when residual or zero sequence voltage (3V0) and current thresholds are exceeded or using the high speed algorithms:

- $\Delta I \geq 0.05$ In
- $\Delta V \geq 0.1$ Vn (Ph-N)

A fault is confirmed if these thresholds are exceeded for more than 1 ½ cycles.

4.7.1.2 Directional determination

The fault direction is determined by measuring the angle between the residual voltage and the residual current derivative. The fault is forward if the angle is between –14° and +166°. A negative or zero-sequence polarisation is selectable to determinate the earth fault direction.

4.7.1.3 Phase selection

The phase is selected in the same way as for distance protection except that the current threshold is reduced ($\Delta I \geq 0.05$ x In and $\Delta V \geq 0.1$ x Vn)

> *Note: If the phase has not been selected within one cycle, a three-phase selection is made automatically.*

1.1.3 Tripping Logic

Legend for Tripping Logic Diagrams (DEF)

Abbreviation	Definition
Vr>	Threshold of residual or zero sequence voltage (3V0)
IRev	**Threshold of residual current (Setting, 0,6IN)**
Forward	Forward directional with zero/negative sequence polarisation
Reverse	Reverse directional with zero/negative sequence polarisation
DEF blocking	Blocking of DEF element
Carrier Receive DEF	Carrier received for the principal line protected (same channel as distance protection)
Iev	Threshold of residual current (0.6 x Ied)
Tripping mode	Single or three-phase tripping (selectable)
Z< starting	Convergence of at least 1 of the 6 loops within the tripping characteristic (internal starting of the distance element)
t_cycle	Additional time delay (150 ms) of 1 pole AR cycle
t_delay	Tripping time delay
t_trans	Carrier Send delay

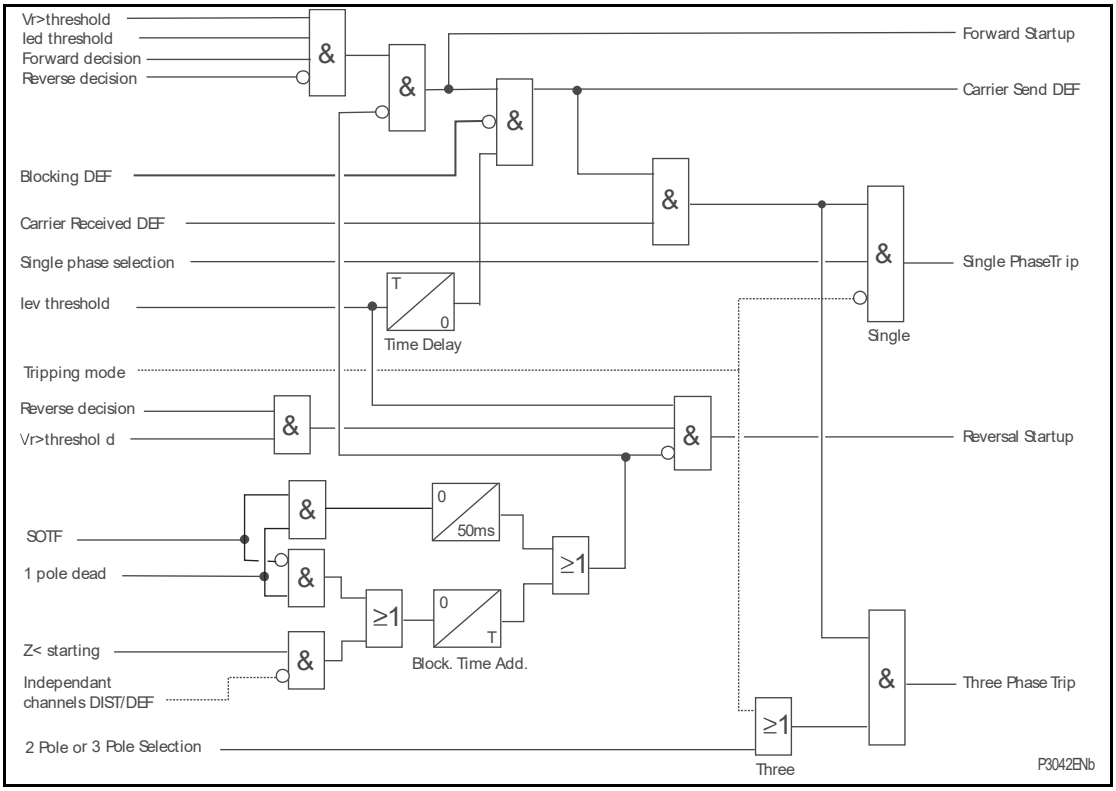


Figure 73: Directional comparison protection permissive scheme

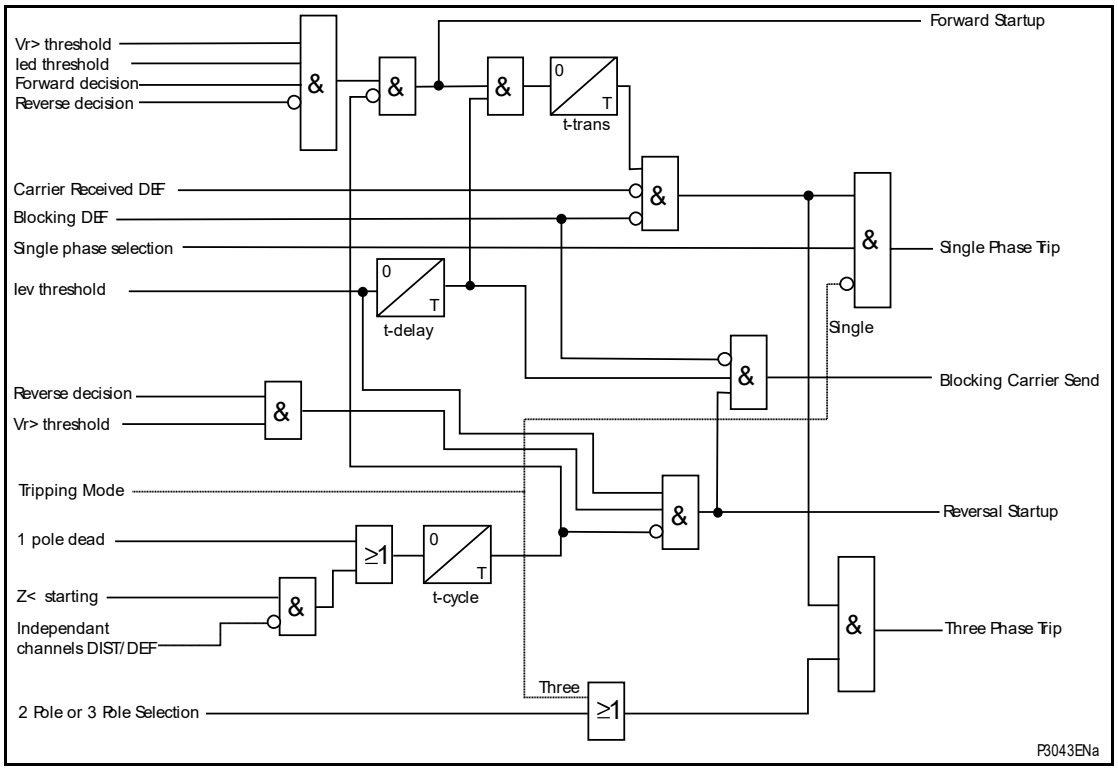


Figure 74: Directional comparison protection blocking scheme

If the DEF directional comparison transmission is selected on the same channel that is used to transmit distance aided-trip messages, the DEF will have the same tripping logic as the main protection (permissive or blocking).

4.7.1.4 SBEF – Stand-By earth fault (not communication-aided)

This protection trips the local breaker directly, without an aided-trip signal, if a high resistance fault remains after a time delay. The time delay varies inversely with the value of the fault current. The selectable inverse time curves comply with the ANSI and IEC standards (see Appendix A).

This protection three-pole trips and can block autoreclosing.

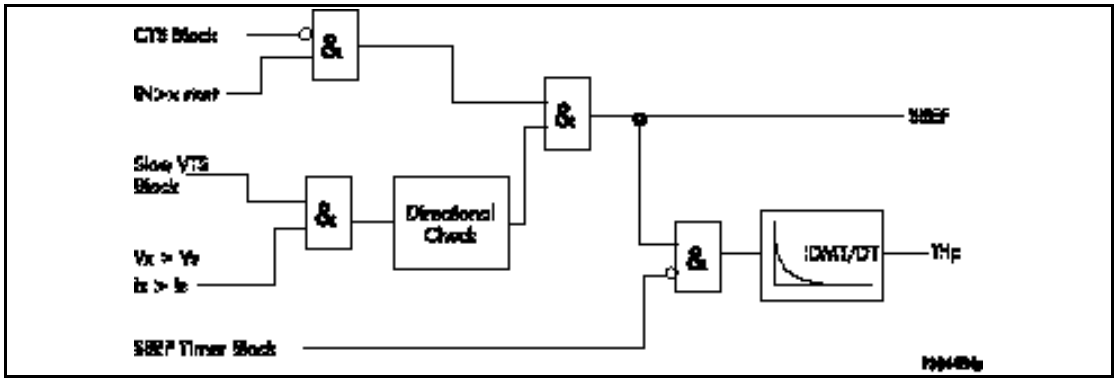


Figure 75: SBEF – stand-by earth fault

4.7.2 Aided Directional Earth Fault (DEF) protection schemes

The option of using separate channels for Directional Earth Fault (DEF) aided tripping, and distance protection schemes, is offered in the P442 and P444 relays.

When a separate channel for DEF is used, the DEF scheme is independently selectable. When a common signalling channel is employed, the distance and DEF must **share** a common scheme. In this case a permissive overreach or blocking distance scheme must be used. The aided tripping schemes can perform single pole tripping.

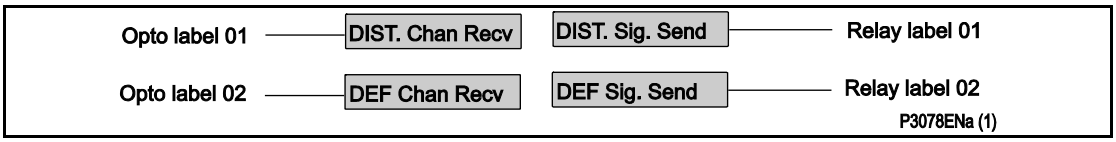


Figure 76: PSL required to activate DEF logic with an independant channel

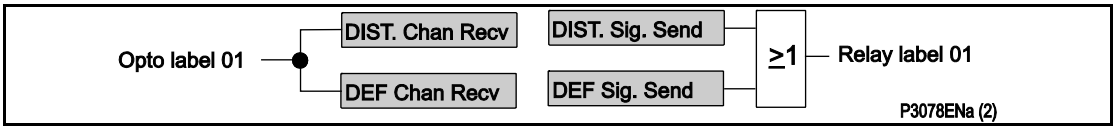


Figure 77: PSL required to activate DEF logic with shared channel

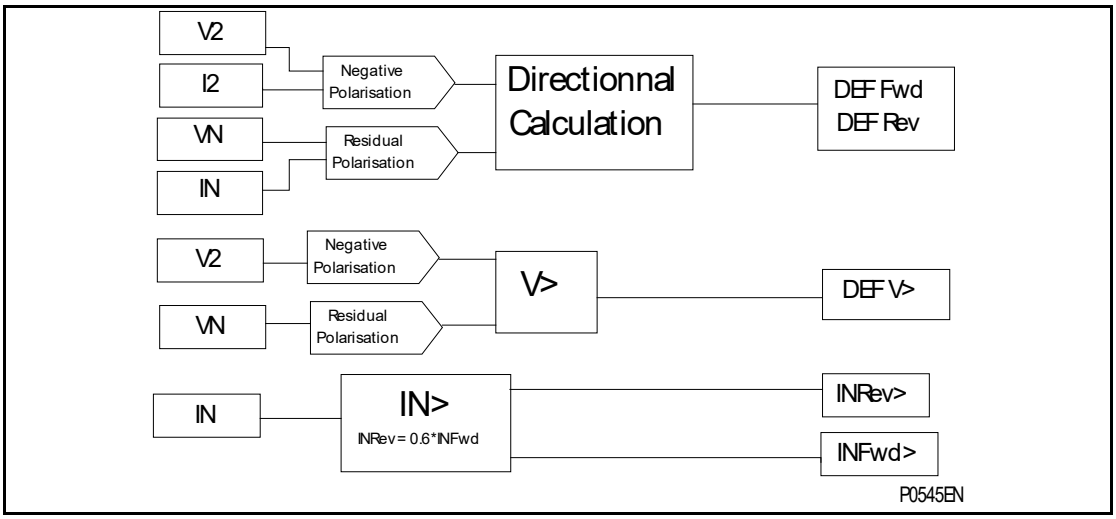


Figure 78: DEF calculation

Note:	*The DEF is blocked in case of VTS or CTS.*

4.7.2.1 Polarising the Directional Decision

The relative advantages of zero sequence and negative sequence polarising are outlined in the section 1.1.2. Note how the polarising chosen for aided DEF is independent of that chosen for backup earth fault elements.

The V> threshold is set above the standing residual voltage on the protected system, to avoid operation for typical power system imbalance and voltage transformer errors. In practice, the typical zero sequence voltage on a healthy system can be as high as 1% (ie: 3% residual), and the VT error could be 1% per phase. This could equate to an overall error of up to 5% of phase-neutral voltage, although a setting between 2% and 4% is typical. On high resistance earthed and insulated neutral systems the settings might need to be as high as 10% or 30% of phase-neutral voltage, respectively.

When negative sequence polarising is set, the V> threshold becomes a V2> negative sequence voltage detector.

The characteristic angle for aided DEF protection (Figure 79) is fixed at **–14°**, suitable for protecting all solidly earthed and resistance earthed systems.

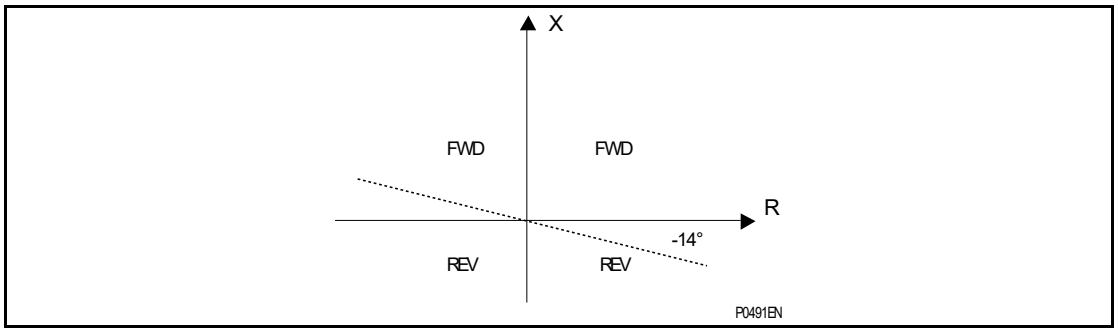


Figure 79: Characteristic angle for aided DEF protection

4.7.2.2 Aided DEF Schemes

4.7.2.2.1 Aided DEF Permissive Overreach Scheme

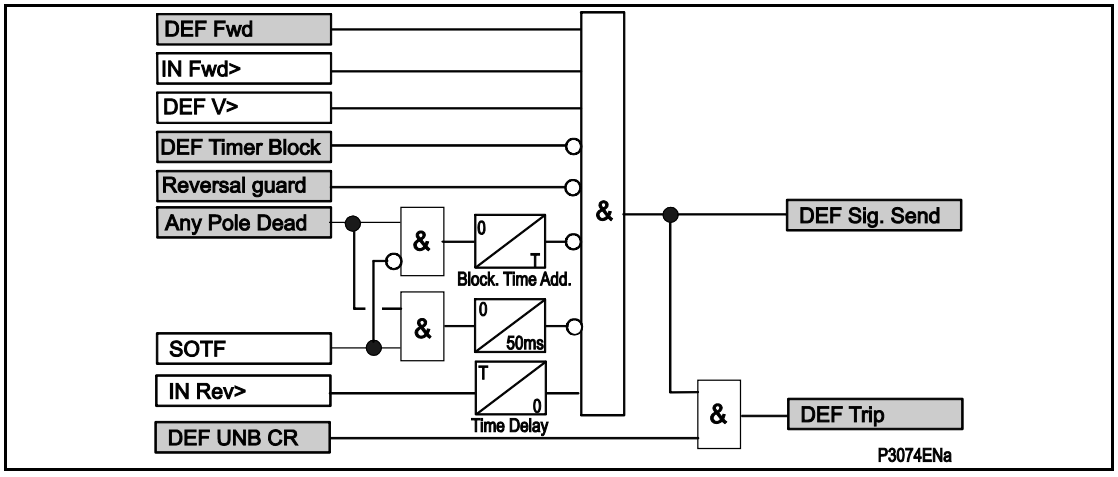


Figure 80: Independent channel – permissive scheme

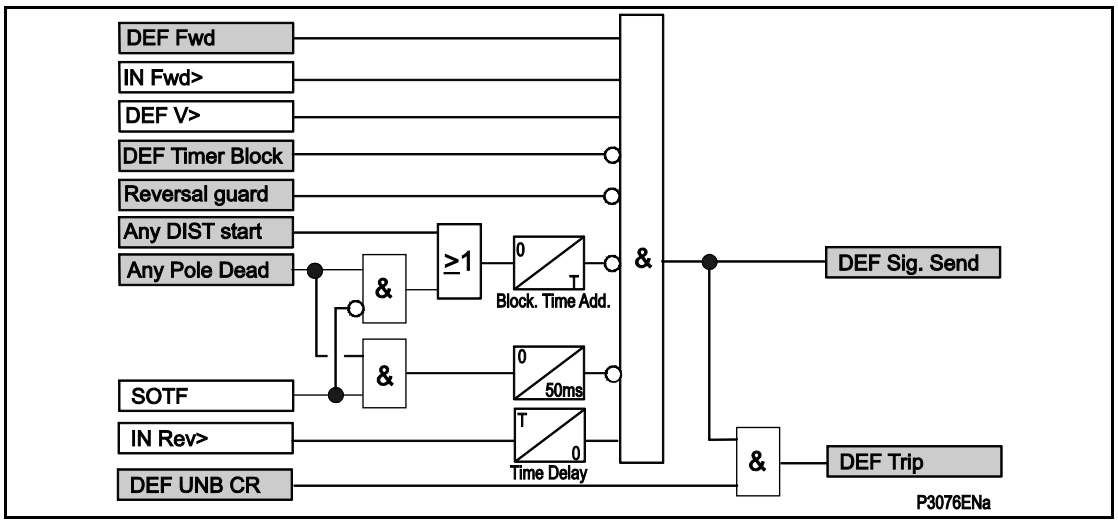


Figure 81: Shared channel – permissive scheme

Figure 82 shows the element reaches. The signalling channel is keyed from operation of the forward IN> DEF element of the relay. If the remote relay has also detected a forward fault, then it will operate with no additional delay upon receipt of this signal.

Send logic: IN> Forward pickup

Permissive trip logic: IN> Forward plus Channel Received.

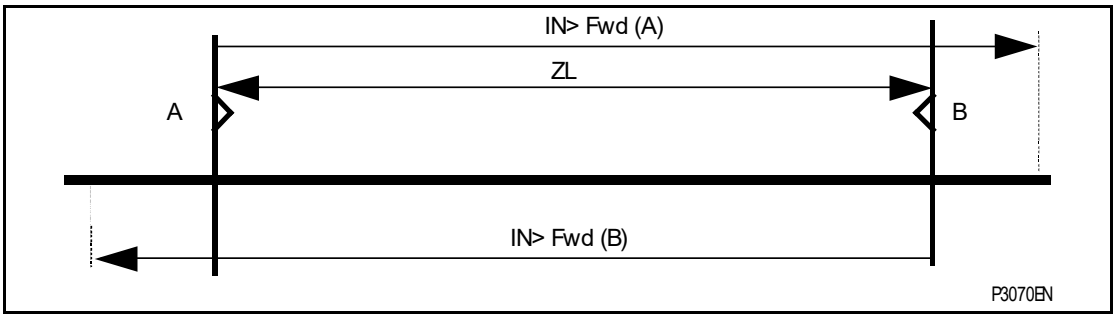


Figure 82: The DEF permissive scheme

The scheme has the same features/requirements as the corresponding distance scheme and provides sensitive protection for high resistance earth faults.

Where “t” is shown in the diagram this signifies the time delay associated with an element, noting that the time-delay for a permissive scheme aided trip would normally be set to zero.

4.7.2.2.2 Aided DEF Blocking Scheme

Figure 85 shows the element reaches, and Figure 86 the simplified scheme logic. The signalling channel is keyed from operation of the reverse DEF element of the relay. If the remote relay forward IN> element has picked up, then it will operate after the set time delay if no block is received.

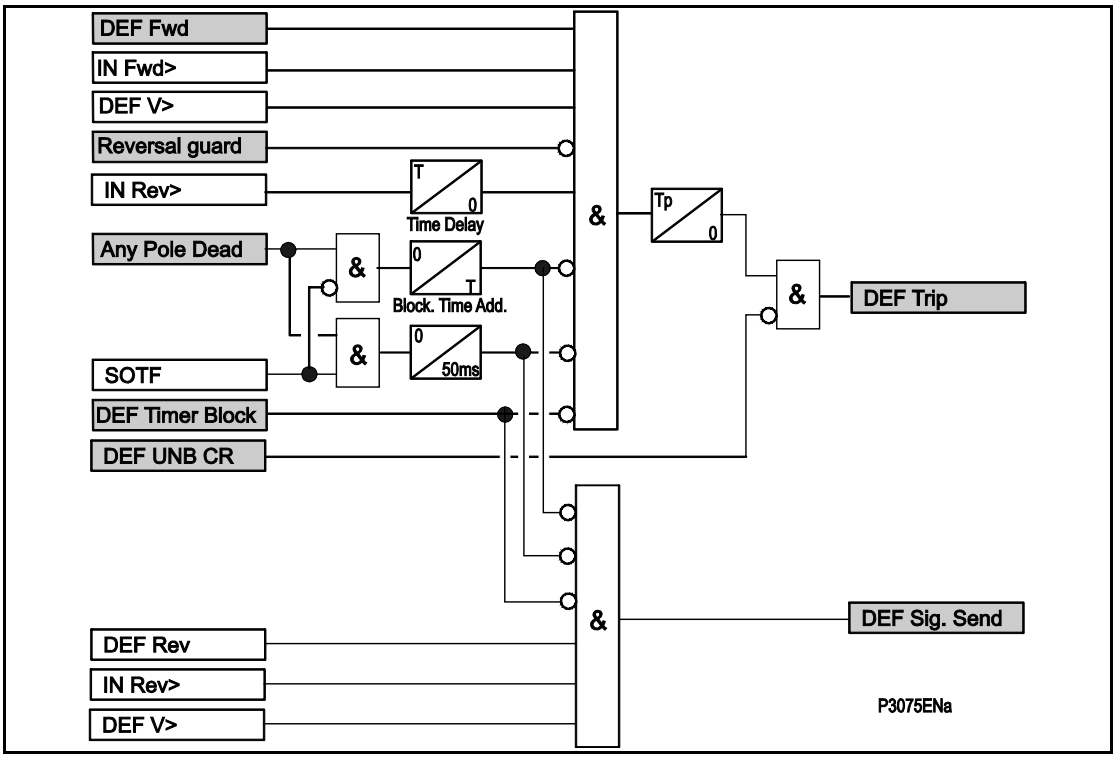


Figure 83: Independent channel – blocking scheme

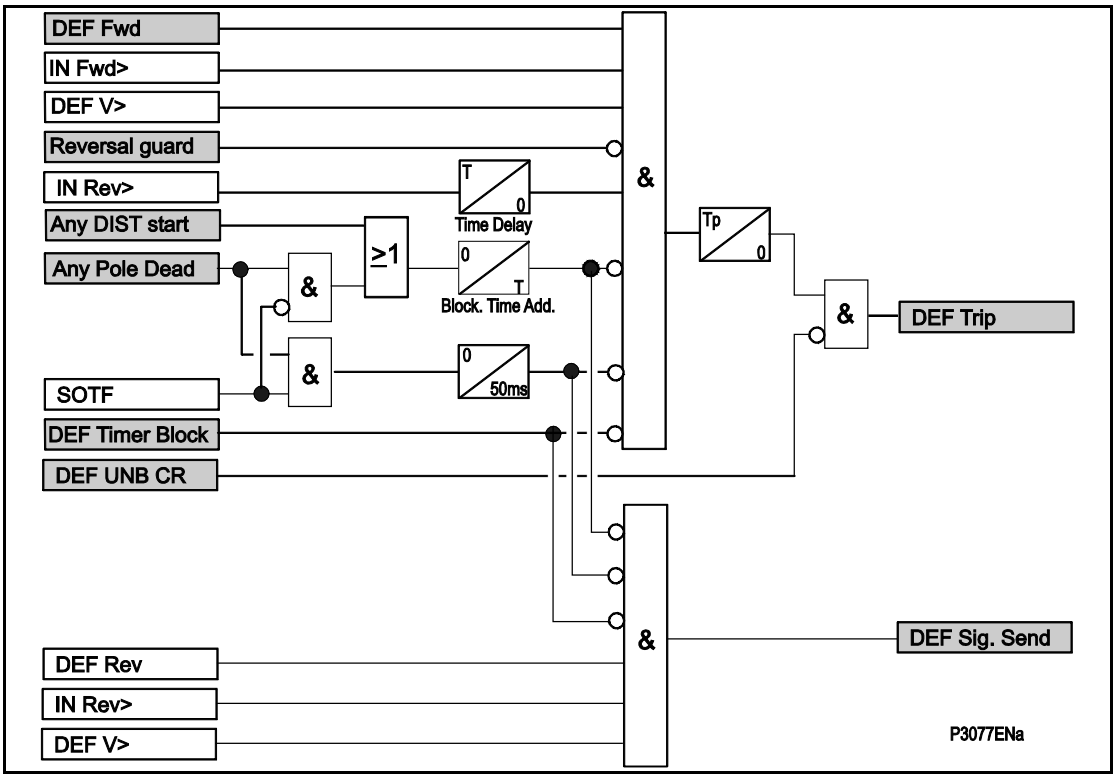


Figure 84: Shared channel – blocking scheme

Send logic: DEF Reverse

Trip logic: IN> Forward, plus Channel NOT Received, with small set delay.



Figure 85: The DEF blocking scheme

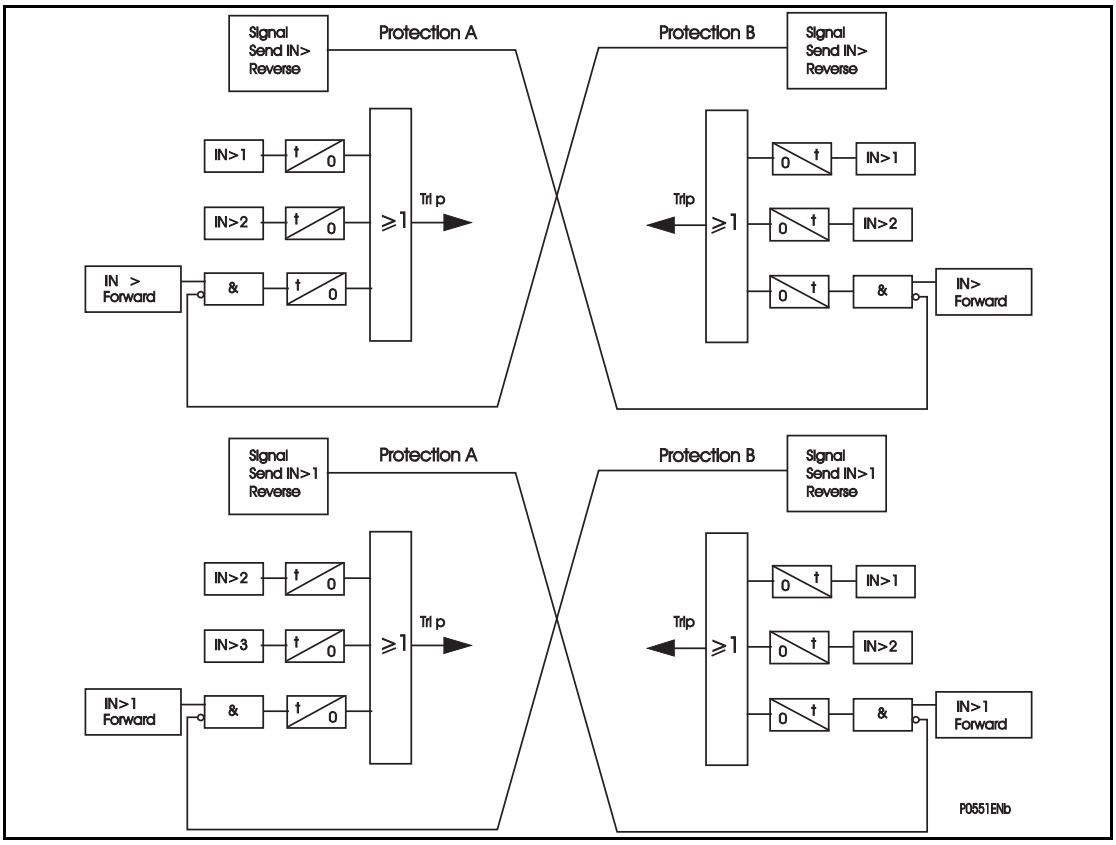


Figure 86: Logic diagram for the DEF blocking scheme

The scheme has the same features/requirements as the corresponding distance scheme and provides sensitive protection for high resistance earth faults.

Where “t” is shown in the diagram this signifies the time delay associated with an element. To allow time for a blocking signal to arrive, a short time delay on aided tripping must be used. The recommended Time Delay setting = max. signalling channel operating time + 14 ms.

4.8 Thermal overload

Thermal overload protection can be used to prevent electrical plant from operating at temperatures in excess of the designed maximum withstand. Prolonged overloading causes excessive heating, which may result in premature ageing of the insulation, or in extreme cases, insulation failure.

The relay incorporates a current based thermal replica, using load current to model heating and cooling of the protected plant. The element can be set with both alarm and trip stages.

The heat generated within an item of plant, such as a cable or a transformer, is the resistive loss ($I^2R \times t$). Therefore, heating is directly proportional to current squared. The thermal time characteristic used in the relay is therefore based on current squared, integrated over time. The relay automatically uses the largest phase current for input to the thermal model.

Equipment is designed to operate continuously at a temperature corresponding to its full load rating, where heat generated is balanced with heat dissipated by radiation etc. Over temperature conditions therefore occur when currents in excess of rating are allowed to flow for a period of time.

The thermal protection also provides an indication of the thermal state in the measurement column of the relay. The thermal state canbe reset by either an opto input (if assigned to this function using the programmable scheme logic) or the relay menu, for example to reset after injection testing. The reset function in the menu is found in the measurement column with the thermal state.

4.8.1 Time constant characteristic

4.8.1.1 Single time constant characteristic

This characteristic is the recommended typical setting for line and cable protection. The thermal time characteristic is given by:

$$\exp(-t/\tau) = (I^2 - (k.I_{FLC})^2) / (I^2 - I_P^2)$$

Where:

t = Time to trip, following application of the overload current, I;
τ = Heating and cooling time constant of the protected plant;
I = Largest phase current;
I_{FLC} = Full load current rating (relay setting 'Thermal Trip');
k = 1.05 constant, allows continuous operation up to < 1.05 I_{FLC}.
I_P = Steady state pre-loading before application of the overload.

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from «hot» or «cold».

The current setting is calculated with Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

Typical time constant values are given in the following table.

	Time constant 1 τ (mN)	**Limits**
Air-core reactors	40	
Capacitor banks	10	
Overhead lines	10	Cross section ≥ 100 mm^2 Cu or 150 mm^2 Al
Cables	60 – 90	Typical, at 66 kV and above
Busbars	60	

Table 9: Typical protected plant thermal time constants

1.1.3.1 Dual time constant characteristic (Typically not applied for MiCOMho P443)

This characteristic is used to protect oil-filled transformers with natural air cooling (e.g. type ONAN). The thermal model is similar to that with the single time constant, except that two time constants must be set. The thermal curve is defined as:

$$0.4 \exp(-t/\tau 1) + 0.6 \exp(-t/\tau 2) = (I^2 - (k.I_{FLC})^2) / (I^2 - I_P^2)$$

Where:

$\tau 1$ = Heating and cooling time constant of the transformer windings;
$\tau 2$ = Heating and cooling time constant for the insulating oil.

For marginal overloading, heat will flow from the windings into the bulk of the insulating oil. Therefore, at low current, the replica curve is dominated by the long time constant for the oil. This provides protection against a general rise in oil temperature.

For severe overloading, heat accumulates in the transformer windings, with little opportunity for dissipation into the surrounding insulating oil. Therefore, at high current, the replica curve is dominated by the short time constant for the windings. This provides protection against hot spots developing within the transformer windings.

Overall, the dual time constant characteristic provided within the relay serves to protect the winding insulation from ageing, and to minimise gas production by overheated oil. Note, however, that the thermal model does not compensate for the effects of ambient temperature change.

The current setting is calculated wuth Thermal Trip = Permissible continuous loading of the transformer / CT ratio.

Typical time constants:

	τ1 (minutes)	τ2 (minutes)	Limits
Oil-filled transformer	5	120	Rating 400 - 1600 kVA

The thermal time constants given in the above tables are typical only. Reference should always be made to the plant manufacturer for accurate information.

4.9 Residual overvoltage protection

On a healthy three phase power system, the summation of all three phase to earth voltages is normally zero, as it is the vector addition of three balanced vectors at 120° to one another. However, when an earth (ground) fault occurs on the primary system this balance is upset and a 'residual' voltage is produced.

Note: This condition causes a rise in the neutral voltage with respect to earth which is commonly referred to as "neutral voltage displacement" or NVD.

The voltage setting applied to the elements is dependent upon the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependent upon the method of system earthing employed and may be calculated by using the formulae's previously given in the above figures. It must also be ensured that the relay is set above any standing level of residual voltage that is present on the healthy system.

Note: IDMT characteristics are selectable on the first stage of NVD and a time delay setting is available on the second stage of NVD in order that elements located at various points on the system may be time graded with one another.

The following figures show the residual voltages that are produced during earth fault conditions occurring on a solid and impedance earthed power system respectively:

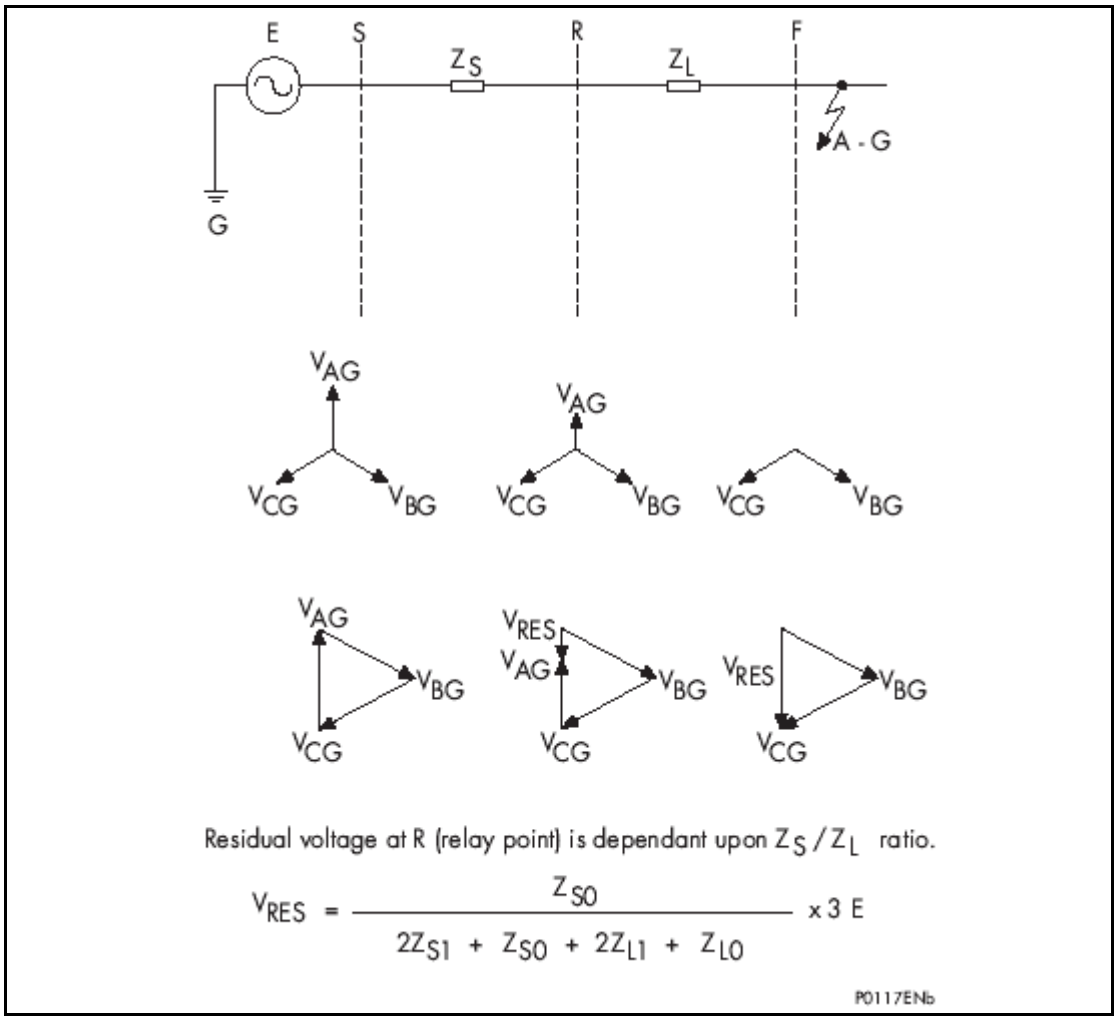


Figure 87: Residual voltage, solidly earthed system

As can be seen in the previous figure, the residual voltage measured by a relay for an earth fault on a solidly earthed system is solely depending on the ratio of source impedance behind the relay to line impedance in front of the relay, up to the point of fault. For a remote fault, the ZS/ZL ratio will be small, resulting in a correspondingly small residual voltage. As such, depending upon the relay setting, such a relay would only operate for faults up to a certain distance along the system. The value of residual voltage generated for an earth fault condition is given by the general formula shown.

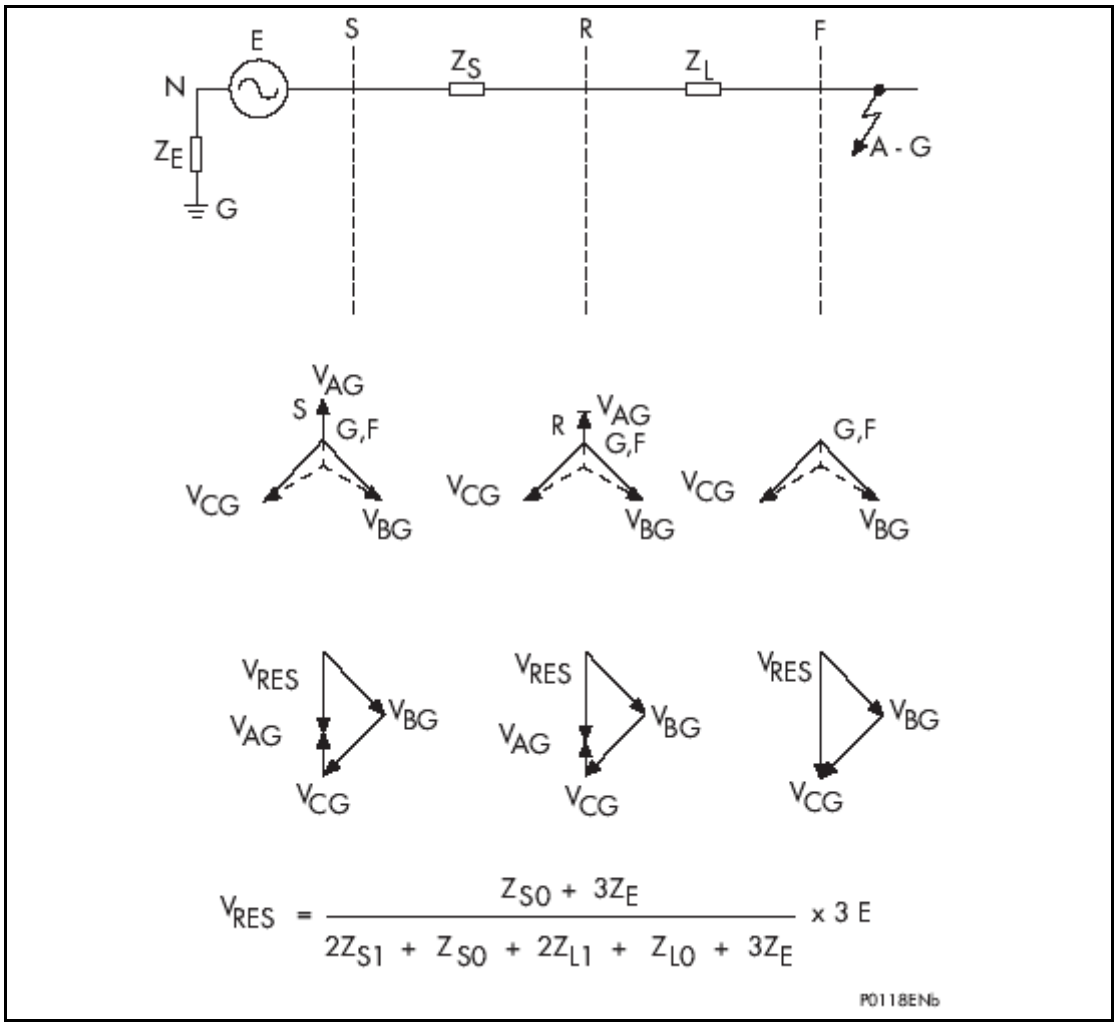


Figure 88: Residual voltage, resistance earthed system

As shown in the figure above, a resistance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then, that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

From the above information it can be seen that the detection of a residual overvoltage condition is an alternative means of earth fault detection, which does not require any measurement of zero sequence current. This may be particularly advantageous at a tee terminal where the infeed is from a delta winding of a transformer (and the delta acts as a zero sequence current trap).

Where residual overvoltage protection is applied, such a voltage will be generated for a fault occurring anywhere on that section of the system and hence the NVD protection must co-ordinate with other earth/ground fault protection.

4.10 Undercurrent protection

The undercurrent protection is activated when the current lower than a threshold. It uses definite delay time undercurrent protection.

The undercurrent protection included within the P442 and P444 relays consists of two independent stages. These stages may be selected or disabled within the “I<1 Status” and “I<2 Status” cells.

Two stages are included to provide both alarm and trip stages, where required. Alternatively, different time settings may be required depending upon the severity of the current dip.

4.11 Voltage protection

Voltage protection contains undervoltage and overvoltage protection.

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Increased system loading. Generally, some corrective action would be taken by voltage regulating equipment such as AVRs or On Load Tap Changers, to bring the system voltage back to its nominal value. If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping using an undervoltage relay is required following a suitable time delay.
- Faults occurring on the power system result in a reduction in voltage of the phases involved in the fault. The proportion by which the voltage decreases is directly dependent on the type of fault, method of system earthing and its location with respect to the relaying point. Consequently, co-ordination with other voltage and current-based protection devices is essential to achieve correct discrimination.

This function will be blocked with Voltage Transformer Supervision (VTS) logic or could be disabled if CB open.

Both the under and overvoltage protection functions can be found in the relay menu “Volt Protection”. The following table shows the undervoltage section of this menu along with the available setting ranges and factory defaults. Different time settings may be required depending upon the severity of the voltage dip.

In the majority of applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case, the element should be selected in the menu to operate from a phase to phase voltage measurement, as this quantity is less affected by single-phase voltage depressions due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions which may be expected under normal system operating conditions. This threshold is dependent upon the system in question but typical healthy system voltage excursions may be in the order of -10% of nominal value.

Similar comments apply with regard to a time setting for this element, i.e. the required time delay is dependent upon the time for which the system is able to withstand a depressed voltage.

The inclusion of the stages in the settings and their respective operating characteristics allows for a number of possible applications:

- Use of the IDMT characteristic gives the option of a longer time delay if the overvoltage condition is only slight but results in a fast trip for a severe overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time delayed alarm stage if required.
- Alternatively, if preferred, both stages could be set to definite time and configured to provide the required alarm and trip stages.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled within the relay menu.

This type of protection must be co-ordinated with any other overvoltage relays at other locations on the system. This should be carried out in a similar manner to that used for grading current operated devices.

4.12 Frequency protection

The frequency protection menu contains underfrequency and overfrequency protections, individually activated when the corresponding status is activated.

4.12.1 Underfrequency protection

Frequency variations on a power system are an indication that the power balance between generation and load has been lost. In particular, underfrequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the

capacity of the generators in that particular subsystem. Industrial plants that are dependent on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

An underfrequency condition at nominal voltage can result in over-fluxing of generators and transformers and many types of industrial loads have limited tolerances on the operating frequency and running speeds e.g. synchronous motors. Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may lead to damage to frequency sensitive equipment and even blackouts, if the underfrequency condition is not corrected sufficiently fast.

To minimize the effects of underfrequency on a system, a multi stage load shedding scheme may be used with the plant loads prioritized and grouped. During an underfrequency condition, the load groups are disconnected sequentially depending on the level of underfrequency, with the highest priority group being the last one to be disconnected.

The effectiveness of each stage of load shedding depends on what proportion of the power deficiency it represents. If the load shedding stage is too small compared to the prevailing generation deficiency, then the improvement in frequency may be non-existent. This aspect should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. This should be balanced against the system survival requirement since excessive time delays may jeopardize system stability.

The relatively long time delays are intended to provide time for the system controls to respond and will work well in a situation where the decline of system frequency is slow. For situations where rapid decline of frequency is expected, the load shedding scheme should be supplemented by rate of change of frequency protection elements.

4.12.2 Overfrequency protection

Overfrequency running of a generator arises when the mechanical power input to the machine exceeds the electrical output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load center. Under such over speed conditions, the governor should respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Over frequency protection is required as a back-up to cater for slow response of frequency control equipment.

Following faults on the network, or other operational requirements, it is possible that various subsystems will be formed within the power network and it is likely that each of these subsystems will suffer from a generation to load imbalance. The “islands” where generation exceeds the existing load will be subject to overfrequency conditions, the level of frequency being a function of the percentage of excess generation. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected.

The relatively long time delays are intended to provide time for the system controls to respond and will work well in a situation where the increase of system frequency is slow.

For situations where rapid increase of frequency is expected, the protection scheme above could be supplemented by rate of change of frequency protection elements, possibly utilized to split the system further.

4.13 Circuit breaker fail protection

Following inception of a fault one or more main protection devices will operate and issue a trip output to the circuit breaker(s) associated with the faulted circuit. Operation of the circuit breaker is essential to isolate the fault, and prevent damage / further damage to the power system. For transmission/sub-transmission systems, slow fault clearance can also threaten system stability. It is therefore common practice to install circuit breaker failure protection, which monitors that the circuit breaker has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, breaker failure protection (CBF) will operate.

CBF operation can be used to backtrip upstream circuit breakers to ensure that the fault is isolated correctly. CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

The ‘CBF Blocks I>‘ and ‘CBF Blocks IN>‘ settings are used to remove starts issued from the overcurrent and earth elements respectively following a breaker fail time out. The start is removed when the cell is set to Enabled.

4.13.1 Typical settings

4.13.1.1 Breaker Fail Timer Settings

Typical time-delay settings to use are as follows:

CB Fail Reset Mechanism	tBF time delay	Typical delay for 2½ cycle circuit breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element operating time (max.) + safety margin	50 + 25 + 50 = 125 ms

Note that all CB Fail resetting involves the operation of the undercurrent elements. Where element reset or CB open resetting is used the undercurrent time setting should still be used if this proves to be the worst case.

The examples above consider direct tripping of a 2½ cycle circuit breaker. Note that where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.

4.13.1.2 Breaker Fail Undercurrent Settings

The phase undercurrent settings (I<) must be set less than load current, to ensure that I< operation indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20% In, with 5% In common for generator circuit breaker CBF.

4.13.2 Breaker Failure Protection Configurations

Resetting of the CBF is possible from a breaker open indication (from the relay’s pole dead logic) or from a protection reset. In these cases resetting is only allowed provided the undercurrent elements have also been reset. The resetting options are summarised in the following table.

Initiation (Menu selectable)	CB fail timer reset mechanism
Current based protection - (eg. 50/51/46/21/87..)	The resetting mechanism is fixed. [IA< operates] AND [IB< operates] AND [IC< operates] AND [IN< operates]
Non-current based protection (eg. 27/59/81/32L..)	Three options are available. The user can select from the following options. [All I< and IN< elements operate] [Protection element reset] AND [All I< and IN< elements operate] CB open (all 3 poles) AND [All I< and IN< elements operate]

Initiation (Menu selectable)	CB fail timer reset mechanism
External protection -	Three options are available. The user can select any or all of the options. [All I< and IN< elements operate] [External trip reset] AND [All I< and IN< elements operate] CB open (all 3 poles) AND [All I< and IN< elements operate]

The phase selection must be performed by creating dedicated PSL.

The circuit breaker failure protection incorporates two time-delays, '**CB Fail 1 Timer**' and '**CB Fail 2 Timer**', allowing configuration for the following scenarios:

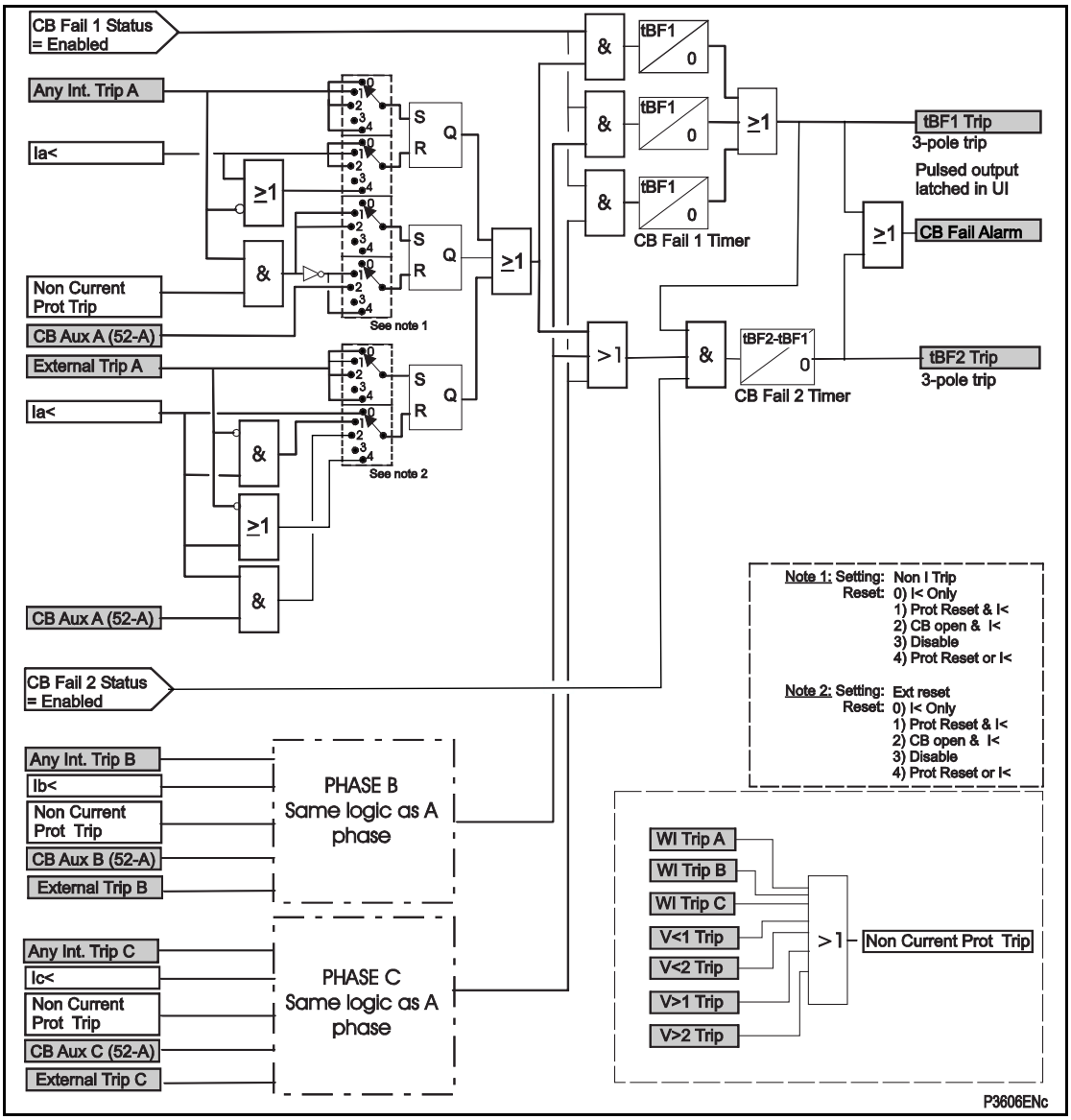


Figure 89: CB Fail general logic

- Simple CBF, where only 'CB Fail 1 Timer' is enabled. For any protection trip, the 'CB Fail 1 Timer' is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, 'CB Fail 1 Timer' times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to backtrip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A re-tripping scheme, plus delayed back-tripping. Here, 'CB Fail 1 Timer' is used to route a trip to a second trip circuit of the same circuit breaker. This requires duplicated

circuit breaker trip coils, and is known as re-tripping. Should re-tripping fail to open the circuit breaker, a back-trip may be issued following an additional time delay. The back-trip uses ‘CB Fail 2 Timer’, which is also started at the instant of the initial protection element trip.

CBF elements ‘CB Fail 1 Timer’ and ‘CB Fail 2 Timer’ can be configured to operate for trips triggered by protection elements within the relay or via an external protection trip. The latter is achieved by allocating one of the relay opto-isolated inputs to ‘External Trip’ using the programmable scheme logic.

1.1.4 Reset Mechanisms for Breaker Fail Time-Delays

It is common practice to use low set undercurrent elements in protection relays to indicate that circuit breaker poles have interrupted the fault or load current, as required. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied upon to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the relay uses operation of undercurrent elements (I<) to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting circuit breaker fail in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. Detecting drop-off of the initiating protection element might be a more reliable method. (in that case setting will be: "Prot. Reset or I<")
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely upon the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and hence drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

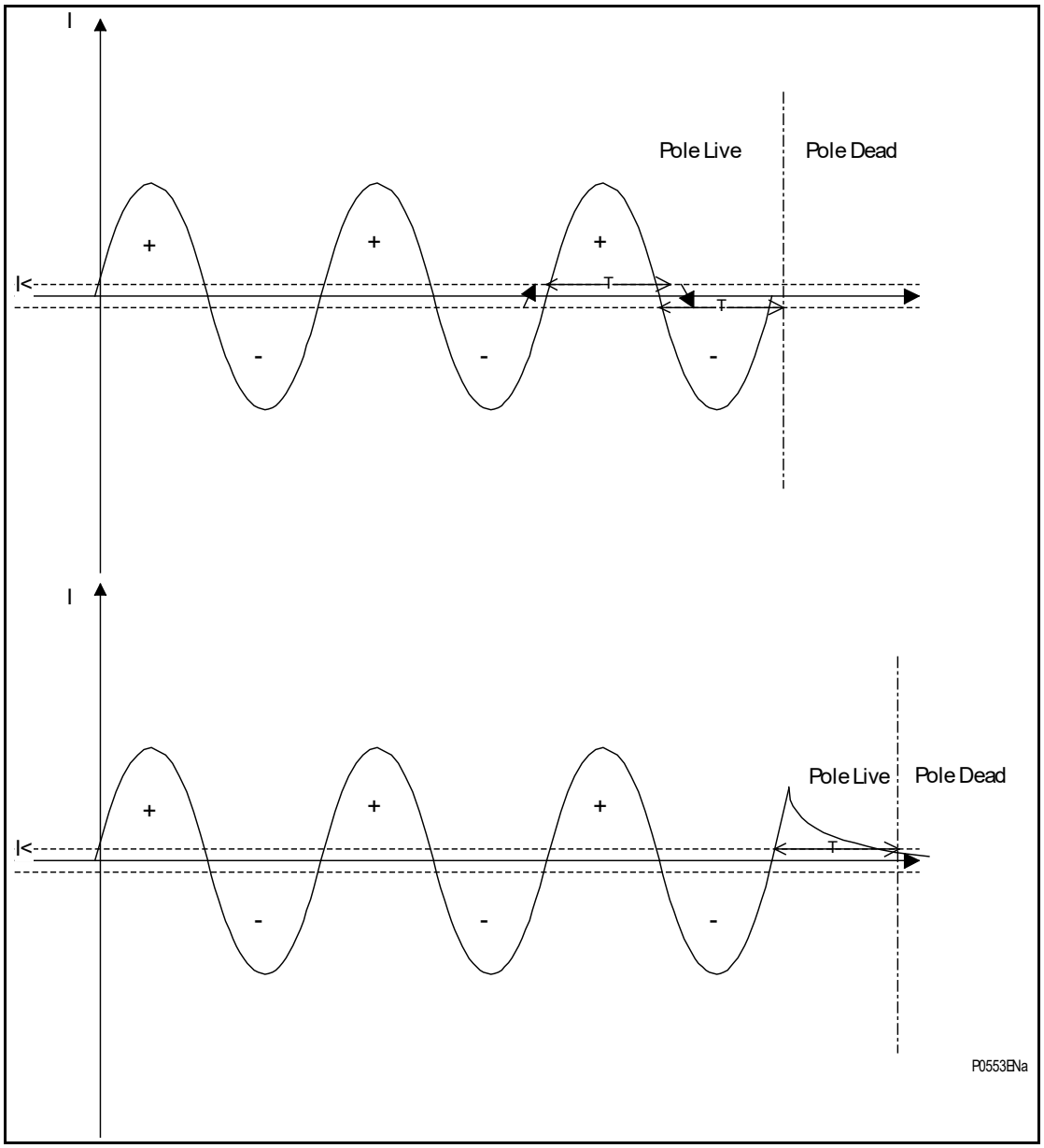


Figure 90: Algorithm for pole dead detection

Description of the open pole detection algorithm:

Each half cycle after the current crosses zero, the algorithm detects whether the current is higher than the I< threshold. If it is, then the detection timer is restarted, if it is lower than the set value then nothing is done.

At the end of the detection timer, open pole decision is given by the algorithm.

Time delay value given by: **(Number of Samples/2 + 2) * ((1/Freq)/Number of Samples)**

Where:
T = 13,3 ms (50 Hz)
or
T = 11,1 ms (60 Hz)

The current used is the unfiltered current (only the analog low pass filter is used)

Example:

In the first example, the line current is broken by the opening of the circuit breaker.

The detection is confirmed 3ms after the pole is opened.

In the second example, some residual current remains due to the CT. The detection is confirmed 12 / 15 ms after the pole is opened.

5 NON PROTECTION FUNCTIONS

5.1 Circuit breaker condition monitoring

Periodic maintenance of circuit breakers is necessary to ensure that the trip circuit and mechanism operate correctly and also that the interrupting capability has not been compromised due to previous fault interruptions. Generally, such maintenance is based on a fixed time interval, or a fixed number of fault current interruptions. These methods of monitoring circuit breaker condition give a rough guide only and can lead to excessive maintenance.

The relays record various statistics related to each circuit breaker trip operation, allowing a more accurate assessment of the circuit breaker condition to be determined. These monitoring features are discussed in the following section.

5.1.1 Circuit Breaker Condition Monitoring Features

For each circuit breaker trip and autoreclose operation the relay, records statistics. The '**CB condition'** and '**CB monitor setup**' menu cells are counter values only. The Min/Max values show the range of the counter values. These cells can be disabled.

The counters may be reset to zero, for example, following a maintenance inspection and overhaul.

The circuit breaker condition monitoring counters will be updated every time the relay issues a trip command. The number of operation is displayed phase by phase.

These operating values are compared to two thresholds (setting with '**CB Monitor Setup**' menu): Maintenance Alarm or LockOut Alarm can be generated. Counters can be re-initiated with the command Reset all values.

When the breaker is tripped by an external protection device, it is also possible to update the CB condition monitoring. This is achieved by allocating one of the relays opto-isolated inputs (via the programmable scheme logic) to accept a trigger from an external device. The DDB signal that is mapped to the opto is called '**External TripA** or **B** or **C**'.

> *Note: When the relay is in Commissioning test mode, the CB condition monitoring counters will not be updated.*

5.1.2 CB condition monitoring

5.1.2.1 Setting the Σ I^ thresholds guidelines

Where overhead lines are prone to frequent faults and are protected by oil circuit breakers (OCB's), oil changes account for a large proportion of the life cycle cost of the switchgear. Generally, oil changes are performed at a fixed interval of circuit breaker fault operations. However, this may result in premature maintenance where fault currents tend to be low, and hence oil degradation is slower than expected. The Σ I^ counter monitors the cumulative severity of the duty placed on the interrupter allowing a more accurate assessment of the circuit breaker condition to be made.

For OCB's, the dielectric withstand of the oil generally decreases as a function of ΣI^2t, where 'I' is the fault current broken, and 't' is the arcing time within the interrupter tank (not the interrupting time). As the arcing time cannot be determined accurately, the relay would normally be set to monitor the sum of the broken current squared, by setting '**Broken I^**' = 2 (I^2 or "I^2").

For other types of circuit breaker, especially those operating on higher voltage systems, practical evidence suggests that the value of '**Broken I^**' = 2 may be inappropriate. In such applications '**Broken I^**' may be set lower, typically 1.4 or 1.5. An alarm in this instance may be indicative of the need for gas/vacuum interrupter HV pressure testing, for example.

The setting range for '**Broken I^**' is variable between 1.0 and 2.0 in 0.1 steps. It is imperative that any maintenance program must be fully compliant with the switchgear manufacturer's instructions.

5.1.2.2 Setting the Number of Operations Thresholds

Every operation of a circuit breaker results in some degree of wear for its components. Therefore, routine maintenance, such as oiling of mechanisms, may be based upon the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventive maintenance is due. Should maintenance not be carried out, the relay can be set to lockout the autoreclose function on reaching a second operations threshold. This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Certain circuit breakers, such as oil circuit breakers (OCB's) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonising of the oil, degrading its dielectric properties. The maintenance alarm threshold ('**N° CB Ops Maint**') may be set to indicate the requirement for oil sampling for dielectric testing, or for more comprehensive maintenance. Again, the lockout threshold ('**N° CB Ops Lock**') may be set to disable autoreclosure when repeated further fault interruptions could not be guaranteed. This minimises the risk of oil fires or explosion.

5.1.2.3 Setting the Operating Time Thresholds

Slow CB operation is also indicative of the need for mechanism maintenance. Therefore, alarm and lockout thresholds ('**CB Time Maint**' and '**CB Time Lockout**') are provided and are settable in the range of 5 to 500 ms. This time is set in relation to the specified interrupting time of the circuit breaker.

5.1.2.4 Setting the Excessive Fault Frequency Thresholds

A circuit breaker may be rated to break fault current a set number of times before maintenance is required. However, successive circuit breaker operations in a short period of time may result in the need for increased maintenance. For this reason it is possible to set a frequent operations counter on the relay which allows the number of operations ('**Fault Freq Count**') over a set time period ('**Fault Freq Time**') to be monitored. A separate alarm and lockout threshold can be set.

5.1.2.5 Lockout reset

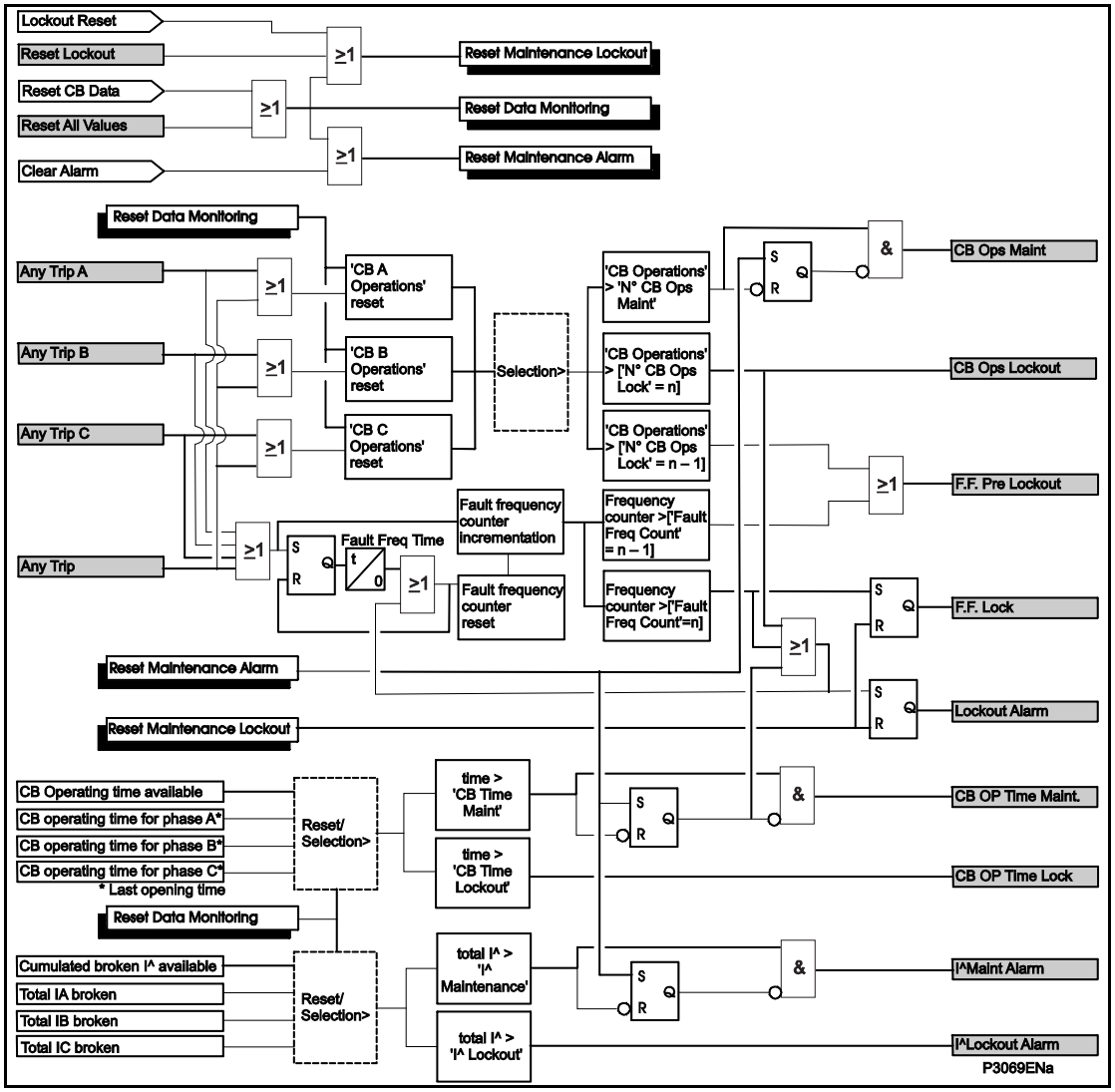
The '**Lockout Reset**' and '**Reset Lockout by**' setting cells in the menu are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example) and auto-reclose lockouts.

5.1.2.6 Inputs/Outputs for CB Monitoring logic

The following DDB are available for CB monitoring (see section P44x/EN PL):

- Inputs
  - Reset Lockout
  - Reset All Values
- Outputs
  - I^Maint Alarm
  - I^Lock Out Alarm
  - CB Ops Maint
  - CB Ops Lockout
  - CB Op Time Maint
  - CB Op Time Lock
  - F.F. Pre Lockout
  - F.F. Lock
  - Lockout Alarm

5.1.2.7 Logic diagram



5.2 Circuit Breaker Control

The relay includes the following options for control of a single circuit breaker:

- Local tripping and closing, via the relay menu
- Local tripping and closing, via relay opto-isolated inputs
- Remote tripping and closing, using the relay communications

It is recommended that separate relay output contacts are allocated for remote circuit breaker control and protection tripping. This enables the control outputs to be selected via a local/remote selector switch. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

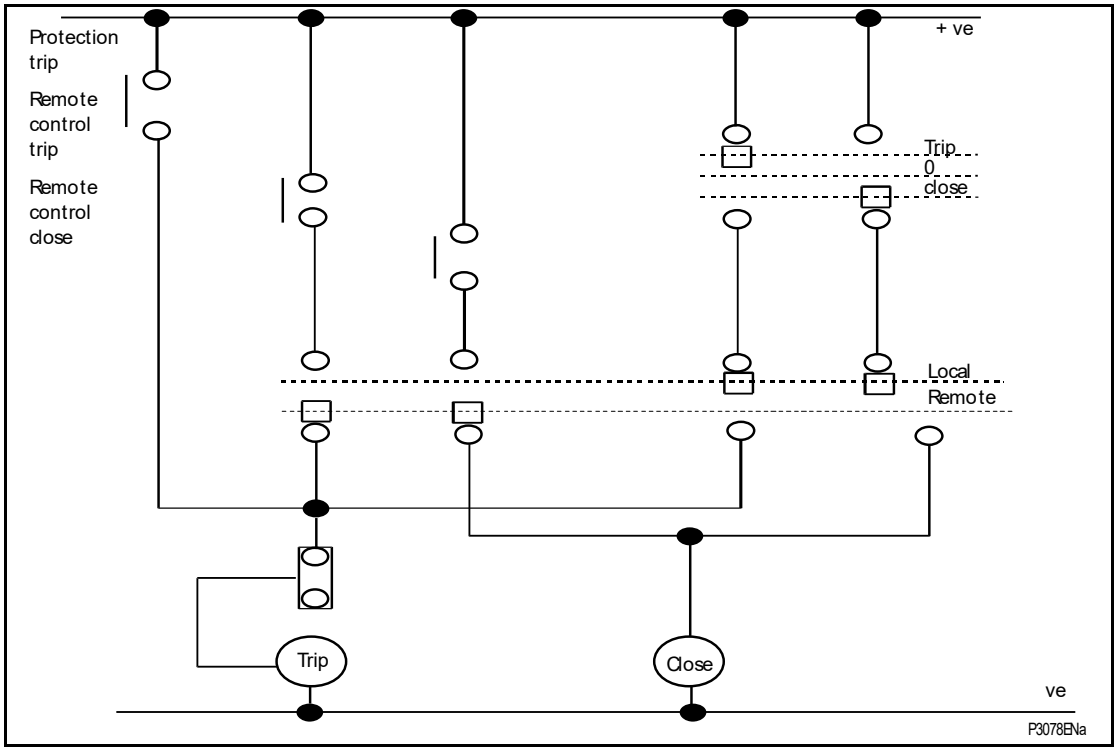


Figure 91: Remote control of circuit breaker

A manual trip will be possible if the circuit breaker is closed. Likewise, a close command can only be issued if the CB is initially open.

Therefore, it will be necessary to use the breaker positions 52a and/or 52b contacts via PSL. If no CB auxiliary contacts are available, no CB control (manual or auto) will be possible. (See the different solutions proposed in the CBAux logic section 5.10)

Once a CB Close command is initiated the output contact can be set to operate following a user defined time delay **('Man Close Delay'**). This would give personnel time to move away from the circuit breaker following the close command. This time delay will apply to all manual CB Close commands.

The length of the trip or close control pulse can be set via the '**Trip Pulse Time**' and '**Close Pulse Time'** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

Note:	*CB close command is in the '**System Data**' column ('**CB Trip/Close**' cell).*

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

When the check synchronisation function ('**System check**' menu) is enabled, it can be used to control manual circuit breaker close commands. When the check synchronism criteria are satisfied, '**CBC Close**' pulse is emitted. The '**C/S Window**' time delay is used to set manual

closure according to system check logic. If the system check criteria are not satisfied before that time-delay elapses, the relay will lockout and issue alarm.

In addition, a CB Healthy information (from the CB), connected to one of the relay's opto-isolators, will indicate the circuit breaker condition for closing availability. When "CB Healthy input" (DDB: '**CB Healthy**') is used, the '**Healthy Window**' time-delay can be set to adjust the manual close of the CB. If the CB does not indicate a healthy condition during this time-delay period, the relay will lockout and issue an alarm.

Where auto-reclose is used it may be desirable to block its operation when performing a manual close. In general, the majority of faults following a manual closure will be permanent faults and it will be undesirable to auto-reclose. The "man close" input without CB Control selected OR the "CBClose in progress" with CB control enabled: will initiate the SOTF logic for which auto-reclose will be disabled following a manual closure of the breaker during 500 msec (see SOTF logic in section P44x/EN AP).

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) a '**CB Fail Trip Control**' or '**CB Fail Close Control**' alarm will be generated (Figure 92) after the relevant trip (1) or close (2) command has expired. These alarms can be viewed on the relay LCD display, remotely via the relay communications, or can be assigned to operate output contacts for annunciation using the relays programmable scheme logic (PSL).

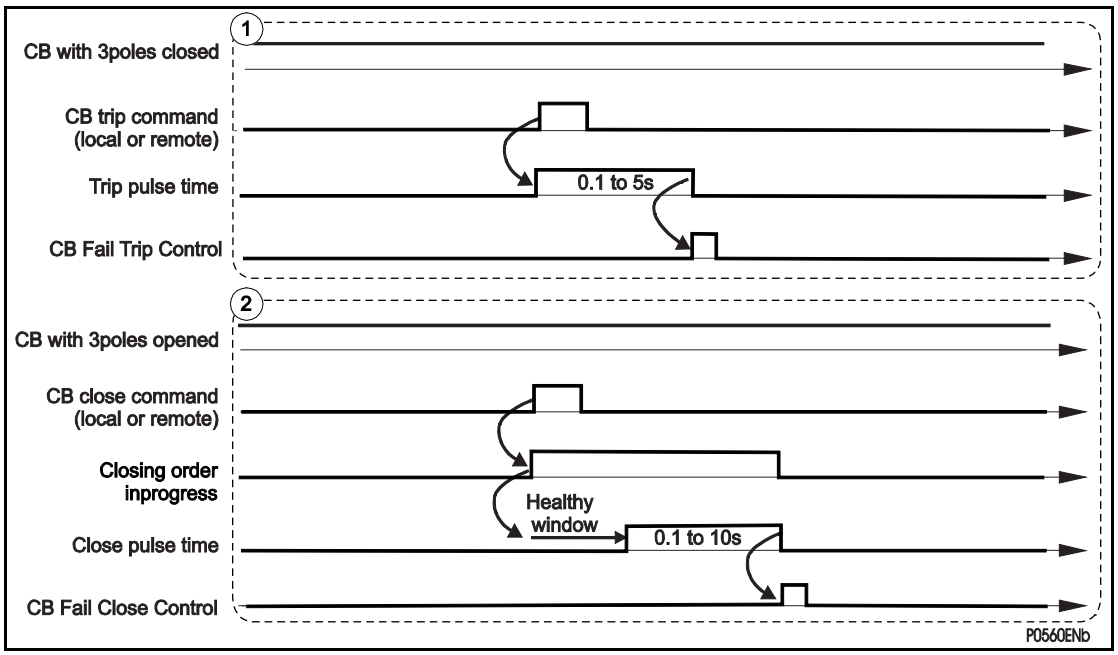


Figure 92: CB Fail to trip or to close

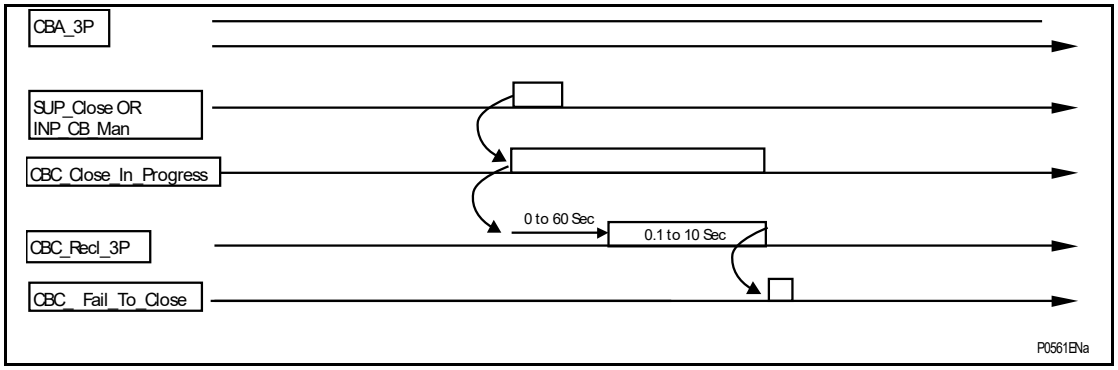


Figure 93: Status of CB is incorrect CBA3P (3Poles are opened) stays – an alarm is generated "CB Fail to Close"

Note that the '**Healthy Window**' and '**C/S Window**' time-delay settings are applicable to manual circuit breaker operations only. These are duplicated in the Auto-reclose menu for Auto-reclose applications.

5.2.1 Logic Inputs / outputs used by the CB Control logic

The following DDB are available for CB Control logic (see section P44x/EN PL):

- Inputs:
  - Man. Trip CB
  - Man.Close CB
  - All pole dead
  - CB Status alarm,
  - A/R 1P In prog
  - A/R 3P In prog
  - A/R Close
  - CB Healthy
  - Check Synck OK
  - Any Trip
  - Any pole Dead
  - CB Discrepancy

- Outputs:
  - Control close
  - Control No C/S
  - Control Trip
  - Ctrl Cls In Prog
  - Man CB Cls Fail
  - Man CB trip Fail

5.2.1.1 General CB Control logic

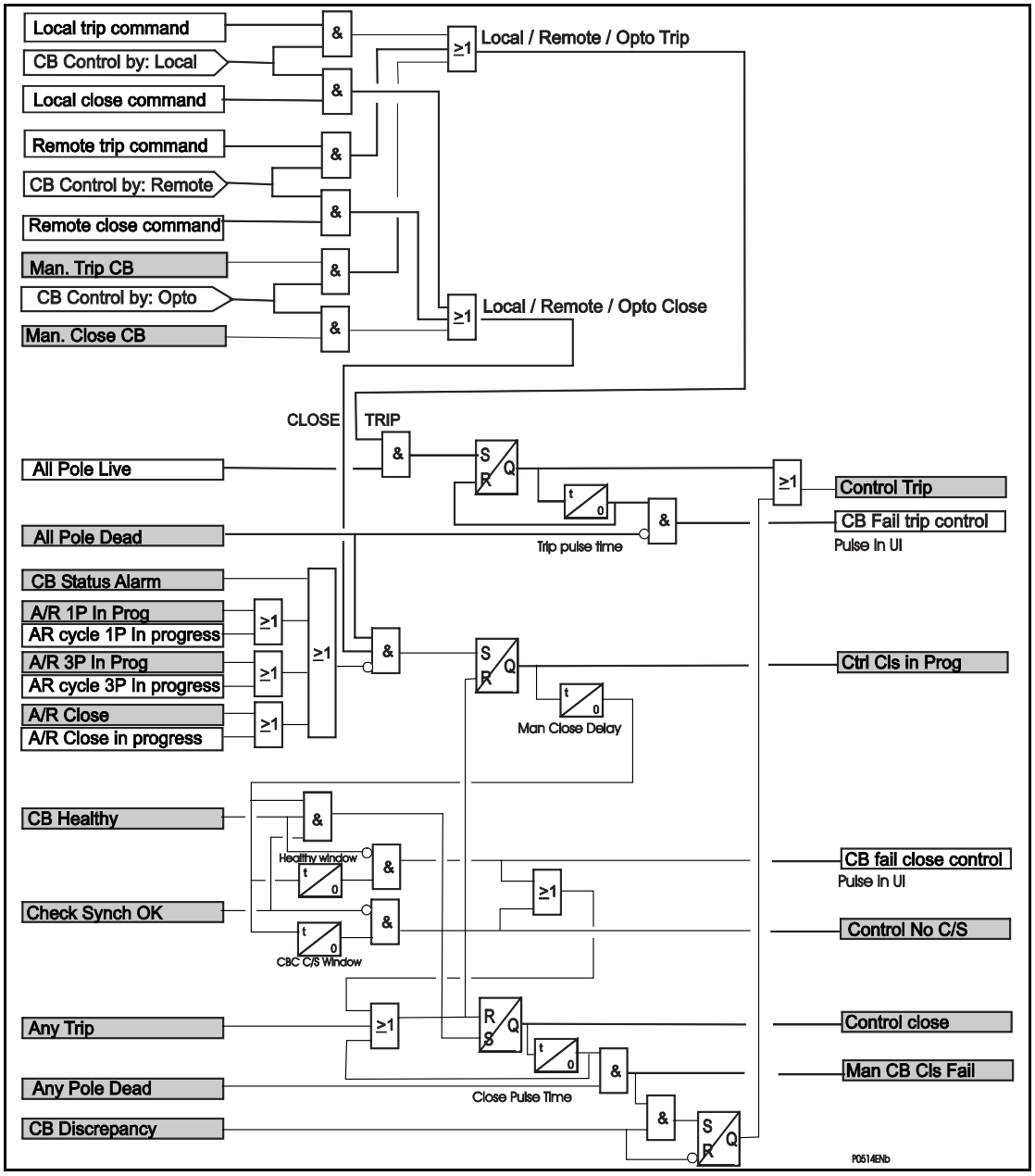


Figure 94: General circuit breaker control logic

5.3 CT and VT ratio

For each Terminal (connected to the secondary of a High voltage CT), the following values have to be known.

1.1.5 CT Ratios

Only **3 values** have to be known and entered:

1. Phase CT Primary current (from 1 to 30000 A) given by the manufacturer.
2. Phase CT secondary current (1 or 5 A) given by the manufacturer.
3. Polarity (Standard (towards the bar) or Inverted (opposite the bar)

Note:	*For the busbar protection reference **2 values** have to be entered:*

4. Phase reference CT Primary current (from 1 to 30000 A).
5. Phase reference CT secondary current (1 or 5 A).

1.1.6 VT Ratios

Only **2 values** have to be known and entered:

1. Phase VT Primary current (from 100 to 100 kV) given by the manufacturer.
2. Phase VT secondary current (80 or 140 V) given by the manufacturer.

5.4 Opto inputs configuration

The MiCOM P44x is fitted with universal opto-isolated logic inputs (opto inputs) that can be programmed for the nominal battery voltage of the circuit of which they are a part i.e. thereby allowing different voltages for different circuits e.g. signalling, tripping. They can also be programmed as Standard 60% - 80% or **50% - 70%** to satisfy different operating constraints (**Dual Opto**).

Threshold levels are as follows:

Nominal Battery Voltage (Vdc)	Standard 60% - 80%		50% - 70%	
	No Operation (logic 0) Vdc	Operation (logic 1) Vdc	No Operation (logic 0) Vdc	Operation (logic 1) Vdc
24 / 27	<16.2	>19.2	<12.0	>16.8
30 / 34	<20.4	>24.0	<15.0	>21.0
48 / 54	<32.4	>38.4	<24.0	>33.6
110 / 125	<75.0	>88.0	<55.0	>77.0
220 / 250	<150.0	>176.0	<110	>154

Table 10: Opto-config threshold levels

This lower value eliminates fleeting pickups that may occur during a battery earth fault, when stray capacitance may present up to 50% of battery voltage across an input.

Each input also has selectable filtering which can be utilised. This allows use of a pre-set filter of ½ cycle which renders the input immune to induced noise on the wiring: although this method is secure it can be slow, particularly for intertripping. This can be improved by switching off the ½ cycle filter in which case one of the following methods to reduce ac noise should be considered. The first method is to use double pole switching on the input, the second is to use screened twisted cable on the input circuit.

5.5 HOTKEYS / Control inputs

5.5.1 Control inputs

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL. There are three setting columns associated with the control inputs which are: “CONTROL INPUTS”, “CTRL I/P CONFIG” and “CTRL I/P LABELS”. The function of these columns is described below.

The Control Input commands can be found in the ‘Control Input’ menu. In the ‘Ctrl I/P status’ menu cell there is a 32 bit word which represent the 32 control input commands. The status of the 32 control inputs can be read from this 32 bit word. The 32 control inputs can also be set and reset from this cell by setting a 1 to set or 0 to reset a particular control input. Alternatively, each of the 32 Control Inputs can be set and reset using the individual menu setting cells ‘Control Input 1, 2, 3’ etc. The Control Inputs are available through the relay menu as described above and also via the rear communications.

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL.

The two hotkeys in the front panel can perform a direct command if a dedicated PSL has been previously created using DDB: **'CONTROL INPUT'** cells (see P44x/EN PL). The MiCOM P44x offers 32 control inputs which can be activated by the Hotkey manually or by the IEC 103 remote communication.

5.5.2 Control I/P Configuration

The “CTRL I/P CONFIG” column has several functions one of which allows the user to configure the control inputs as either ‘latched’ or ‘pulsed’. A latched control input will remain in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input, however, will remain energised for 10ms after the set command is given and will then reset automatically (i.e. no reset command required).

In addition to the latched / pulsed option this column also allows the control inputs to be individually assigned to the “Hotkey” menu by setting ‘1’ in the appropriate bit in the “Hotkey Enabled” cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the “CONTROL INPUTS” column. The “Ctrl Command” cell also allows the SET / RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as “ON / OFF”, “IN / OUT” etc.

5.5.3 Control I/P Labels

The “CTRL I/P LABELS” column makes it possible to change the text associated with each individual control input. This text will be displayed when a control input is accessed by the hotkey menu, or it can be displayed in the PSL.

Note:	*With the exception of pulsed operation, the status of the control inputs is stored in battery backed memory. In the event that the auxiliary supply is interrupted the status of all the inputs will be recorded. Following the restoration of the auxiliary supply the status of the control inputs, prior to supply failure, will be reinstated. If the battery is missing or flat the control inputs will set to logic 0 once the auxiliary supply is restored*

5.6 InterMiCOM Teleprotection

InterMiCOM is a protection signalling system that is an optional feature of MiCOM Px40 relays and provides a cost-effective alternative to discrete carrier equipment. InterMiCOM sends eight signals between the two relays in the scheme, with each signal having a selectable operation mode to provide an optimal combination of speed, security and dependability in accordance with the application. Once the information is received, it may be assigned in the Programmable Scheme Logic to any function as specified by the user’s application.

5.6.1 Protection Signalling

To achieve fast fault clearance and correct discrimination for faults anywhere within a high voltage power network, it is necessary to signal between the points at which protection relays are connected. Two distinct types of protection signalling can be identified:

5.6.1.1 Unit protection Schemes

In these schemes the signalling channel is used to convey analog data concerning the power system between relays, typically current magnitude and/or phase. These unit protection schemes are not covered by InterMiCOM, with the MiCOM Px4x range of current differential and phase comparison relays available.

5.6.1.2 Teleprotection – Channel Aided Schemes

In these schemes the signalling channel is used to convey simple ON/OFF data (from a local protection device) thereby providing some additional information to a remote device which can be used to accelerate in-zone fault clearance and/or prevent out-of-zone tripping. This kind of protection signalling has been discussed earlier in this chapter, and InterMiCOM provides the ideal means to configure the schemes in the P443 relay.

In each mode, the decision to send a command is made by a local protective relay operation, and three generic types of InterMiCOM signal are available:

Intertripping In intertripping (direct or transfer tripping applications), the command is not supervised at the receiving end by any protection relay and simply causes CB operation. Since no checking of the received signal by another protection device is performed, it is absolutely essential that any noise on the signalling

channel isn't seen as being a valid signal. In other words, an intertripping channel must be very secure.

Permissive — In permissive applications, tripping is only permitted when the command coincides with a protection operation at the receiving end. Since this applies a second, independent check before tripping, the signalling channel for permissive schemes do not have to be as secure as for intertripping channels.

Blocking — In blocking applications, tripping is only permitted when no signal is received but a protection operation has occurred. In other words, when a command is transmitted, the receiving end device is blocked from operating even if a protection operation occurs. Since the signal is used to prevent tripping, it is imperative that a signal is received whenever possible and as quickly as possible. In other words, a blocking channel must be fast and dependable.

The requirements for the three channel types are represented pictorially in Figure 95.

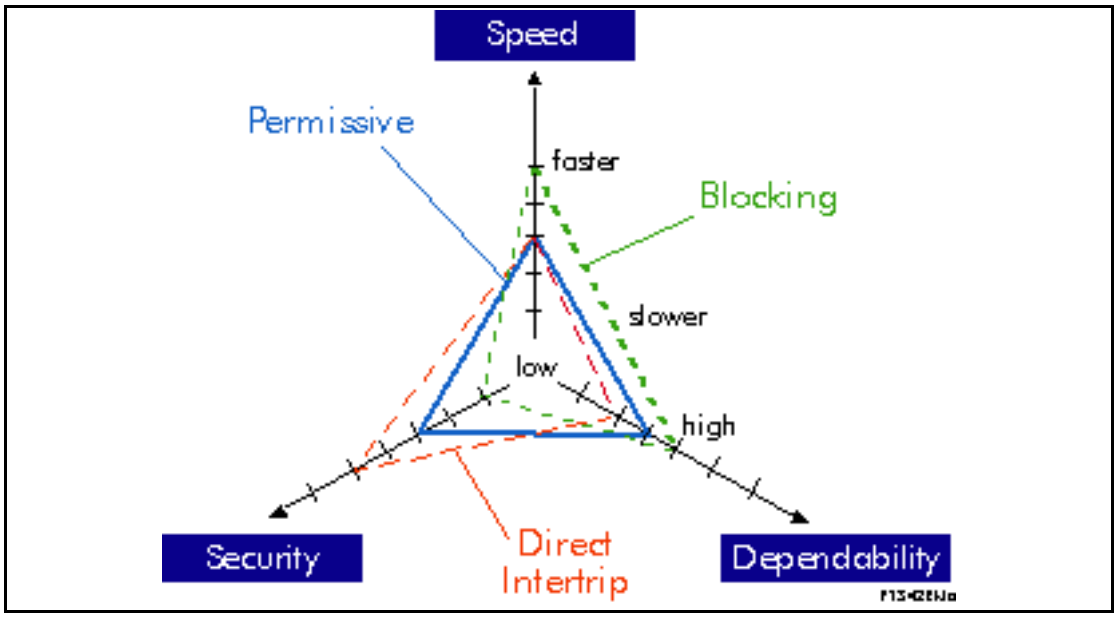


Figure 95: Pictorial comparison of operating modes

This diagram shows that a blocking signal should be fast and dependable; a direct intertrip signal should be very secure and a permissive signal is an intermediate compromise of speed, security and dependability.

5.6.1.3 Communications Media

InterMiCOM is capable of transferring up to 8 commands over one communication channel. Due to recent expansions in communication networks, most signalling channels are now digital schemes utilising multiplexed fibre optics and for this reason, InterMiCOM provides a standard EIA(RS)232 output using digital signalling techniques. This digital signal can then be converted using suitable devices to any communications media as required.

Note:	*The MiCOM P442/P444 relays only use electrical connections (EIA(RS)232, port SK5)*

The EIA(RS)232 output may alternatively be connected to a MODEM link.

Regardless of whether analogue or digital systems are being used, all the requirements of teleprotection commands are governed by an international standard IEC60834-1:1999 and InterMiCOM is compliant with the essential requirements of this standard. This standard governs the speed requirements of the commands as well as the probability of unwanted commands being received (security) and the probability of missing commands (dependability).

5.6.1.4 General Features & Implementation

InterMiCOM provides 8 commands over a single communications link, with the mode of operation of each command being individually selectable within the “IM# Cmd Type” cell. “Blocking” mode provides the fastest signalling speed (available on commands 1 – 4), “Direct Intertrip” mode provides the most secure signalling (available on commands 1 – 8) and “Permissive” mode provides the most dependable signalling (available on commands 5 – 8). Each command can also be disabled so that it has no effect in the logic of the relay.

Since many applications will involve the commands being sent over a multiplexed communications channel, it is necessary to ensure that only data from the correct relay is used. Both relays in the scheme must be programmed with a unique pair of addresses that correspond with each other in the “Source Address” and “Receive Address” cells. For example, at the local end relay if we set the “Source Address” to 1, the “Receive Address” at the remote end relay must also be set to 1. Similarly, if the remote end relay has a “Source Address” set to 2, the “Receive Address” at the local end must also be set to 2. All four addresses must not be set identical in any given relay scheme if the possibility of incorrect signalling is to be avoided.

It must be ensured that the presence of noise in the communications channel isn’t interpreted as valid messages by the relay. For this reason, InterMiCOM uses a combination of unique pair addressing described above, basic signal format checking and for “Direct Intertrip” commands an 8-bit Cyclic Redundancy Check (CRC) is also performed. This CRC calculation is performed at both the sending and receiving end relay for each message and then compared to maximise the security of the “Direct Intertrip” commands.

Most of the time the communications will perform adequately and the presence of the various checking algorithms in the message structure will ensure that InterMiCOM signals are processed correctly. However, careful consideration is also required for the periods of extreme noise pollution or the unlikely situation of total communications failure and how the relay should react.

During periods of extreme noise, it is possible that the synchronization of the message structure will be lost and it may become impossible to decode the full message accurately. During this noisy period, the last good command can be maintained until a new valid message is received by setting the “IM# FallBackMode” cell to “Latched”. Alternatively, if the synchronisation is lost for a period of time, a known fallback state can be assigned to the command by setting the “IM# FallBackMode” cell to “Default”. In this latter case, the time period will need to be set in the “IM# FrameSynTim” cell and the default value will need to be set in “IM# DefaultValue” cell. As soon as a full valid message is seen by the relay all the timer periods are reset and the new valid command states are used. An alarm is provided if the noise on the channel becomes excessive.

When there is a total communications failure, the relay will use the fallback (failsafe) strategy as described above. Total failure of the channel is considered when no message data is received for four power system cycles or if there is a loss of the DCD line.

5.6.1.5 Physical Connections

InterMiCOM on the Px40 relays is implemented using a 9-pin ‘D’ type female connector (labelled SK5) located at the bottom of the second Rear communication board. This connector on the Px40 relay is wired in DTE (Data Terminating Equipment) mode, as indicated below:

Pin	Acronym	InterMiCOM Usage
1	DCD	“Data Carrier Detect” is only used when connecting to modems otherwise this should be tied high by connecting to terminal 4.
2	RxD	“Receive Data”
3	TxD	“Transmit Data”
4	DTR	“Data Terminal Ready” is permanently tied high by the hardware since InterMiCOM requires a permanently open communication channel.
5	GND	“Signal Ground”
6	Not used	-

7	RTS	“Ready To Send” is permanently tied high by the hardware since InterMiCOM requires a permanently open communication channel.
8	Not used	-
9	Not used	-

Table 11: InterMICOM D9 port pin-out connections

Depending on whether a direct or modem connection between the two relays in the scheme is being used, the required pin connections are described below.

5.6.1.6 Direct Connection

The EIA(RS)232 protocol only allows for short transmission distances due to the signalling levels used and therefore the connection shown below is limited to less than 15m. However, this may be extended by introducing suitable EIA(RS)232 to fiber optic convertors, such as the CILI 204. Depending upon the type of convertor and fiber used, direct communication over a few kilometres can easily be achieved.

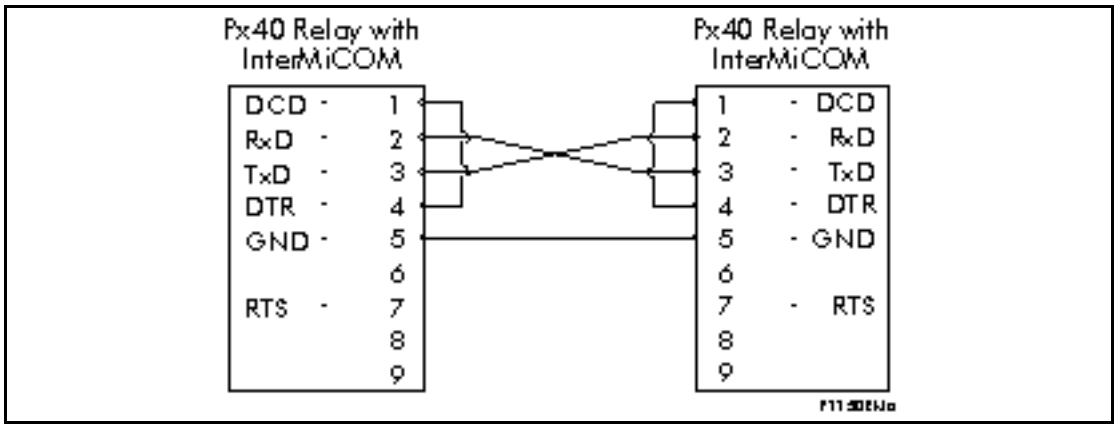


Figure 96: Direct connection within the local substation

This type of connection should also be used when connecting to multiplexers which have no ability to control the DCD line.

5.6.1.7 Modem Connection

For long distance communication, modems may be used in which the case the following connections should be made.

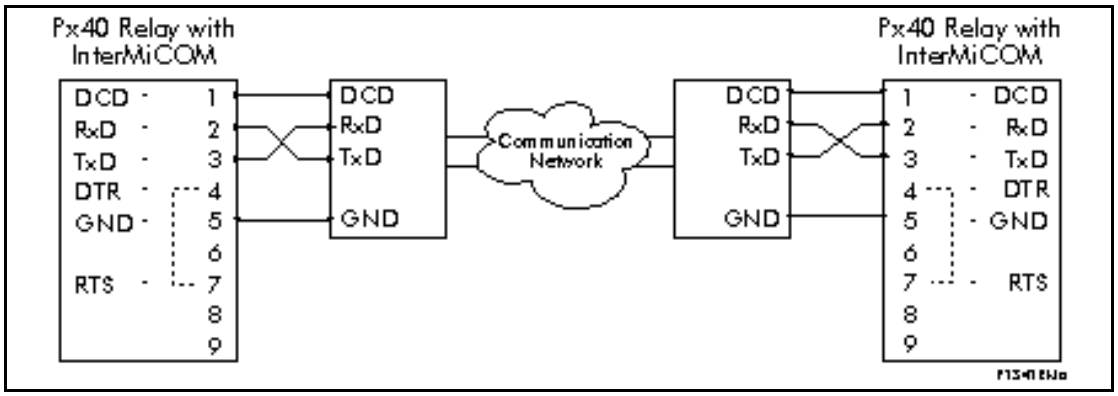


Figure 97: InterMICOM teleprotection via a MODEM link

This type of connection should also be used when connecting to multiplexers which have the ability to control the DCD line.

With this type of connection the maximum distance between the Px40 relay and the modem should be 15m, and that a baud rate suitable for the communications path used should be selected.

1.1.7 Functional Assignment

Even though settings are made on the relay to control the mode of the intertrip signals, it is necessary to assign interMiCOM input and output signals in the relay Programmable Scheme Logic (PSL) if InterMiCOM is to be successfully implemented. Two icons are provided on the PSL editor of MiCOM S1 Agile for “Integral tripping In” and “Integral tripping out” which can be used to assign the 8 intertripping commands.

It should be noted that when an InterMiCOM signal is sent from the local relay, only the remote end relay will react to this command. The local end relay will only react to InterMiCOM commands initiated at the remote end.

1.1.8 InterMiCOM Settings

The settings necessary for the implementation of InterMiCOM are contained within two columns of the relay menu structure. The first column entitled “INTERMICOM COMMS” contains all the information to configure the communication channel and also contains the channel statistics and diagnostic facilities. The second column entitled “INTERMICOM CONF” selects the format of each signal and its fallback operation mode. The following tables show the relay menus including the available setting ranges and factory defaults.

Once the relay operation has been confirmed using the loopback test facilities, it will be necessary to ensure that the communications between the two relays in the scheme are reliable. To facilitate this, a list of channel statistics and diagnostics are available in the InterMiCOM COMMS column:

1.1.8.1 Setting Guidelines

The settings required for the InterMiCOM signalling are largely dependant upon whether a direct or indirect (modem/multiplexed) connection between the scheme ends is used.

Direct connections will either be short metallic or dedicated fiber optic (using CILI204) based and hence can be set to have the highest signalling speed of 19200 b/s. Due to this high signalling rate, the difference in operating speed between the direct, permissive and blocking type signals is so small that the most secure signalling (direct intertrip) can be selected without any significant loss of speed. In turn, since the direct intertrip signalling requires the full checking of the message frame structure and CRC checks, it would seem prudent that the “IM# Fallback Mode” be set to “Default” with a minimal intentional delay by setting “IM# FrameSyncTim” to 10 msecs. In other words, whenever two consecutive messages have an invalid structure, the relay will immediately revert to the default value until a new valid message is received.

For indirect connections, the settings that should be applied will become more application and communication media dependent. As for the direct connections, it may be appealing to consider only the fastest baud rate but this will usually increase the cost of the necessary modem/multiplexer.

In addition, devices operating at these high baud rates may suffer from “data jams” during periods of interference and in the event of communication interruptions, may require longer re-synchronization periods.

Both of these factors will reduce the effective communication speed thereby leading to a recommended baud rate setting of 9600 b/s. It should be noted that as the baud rate decreases, the communications become more robust with fewer interruptions, but that overall signalling times will increase.

Since it is likely that slower baud rates will be selected, the choice of signalling mode becomes significant. However, once the signalling mode has been chosen it is necessary to consider what should happen during periods of noise when message structure and content can be lost.

If “Blocking” mode is selected, only a small amount of the total message is actually used to provide the signal, which means that in a noisy environment there is still a good likelihood of receiving a valid message. In this case, it is recommended that the “IM# Fallback Mode” is set to “Default” with a reasonably long “IM# FrameSyncTim”.

If “Direct Intertrip” mode is selected, the whole message structure must be valid and checked to provide the signal, which means that in a very noisy environment the chances of receiving

a valid message are quite small. In this case, it is recommended that the “IM# Fallback Mode” is set to “Default” with a minimum “IM# FrameSyncTim” setting i.e. whenever a non-valid message is received, InterMiCOM will use the set default value.

If “Permissive” mode is selected, the chances of receiving a valid message is between that of the “Blocking” and “Direct Intertrip” modes. In this case, it is possible that the “IM# Fallback Mode” is set to “Latched”. The table below highlights the recommended “IM# FrameSyncTim” settings for the different signalling modes and baud rates:

Baud Rate	Minimum Recommended “IM# FrameSyncTim” Setting		Minimum Setting	Maximum Setting
	Direct Intertrip Mode	Blocking Mode		
600	100	250	100	1500
1200	50	130	50	1500
2400	30	70	30	1500
4800	20	40	20	1500
9600	10	20	10	1500
19200	10	10	10	1500

Table 12: Recommended frame synchronism time settings

Note: No recommended setting is given for the Permissive mode since it is anticipated that “Latched” operation will be selected. However, if “Default mode” is selected, the “IM# FrameSyncTim” setting should be set greater than the minimum settings listed above. If the “IM# FrameSyncTim” setting is set lower than the minimum setting listed above, there is a danger that the relay will monitor a correct change in message as a corrupted message.
A setting of 25% is recommended for the communications failure alarm.

5.6.1.8 InterMiCOM Statistics & Diagnostics

It is possible to hide the channel diagnostics and statistics from view by setting the “Ch Statistics” and/or “Ch Diagnostics” cells to “Invisible”. All channel statistics are reset when the relay is powered up, or by user selection using the “Reset Statistics” cell.

5.6.2 Testing InterMiCOM Teleprotection

5.6.2.1 InterMiCOM Loopback Testing & Diagnostics

A number of features are included within the InterMiCOM function to assist a user in commissioning and diagnosing any problems that may exist in the communications link.

“Loopback” test facilities, located within the INTERMICOM COMMS column of the relay menu, provide a user with the ability to check the software and hardware of the InterMiCOM signalling. By selecting “Loopback Mode” to “Internal”, only the internal software of the relay is checked whereas “External” will check both the software and hardware used by InterMiCOM. In the latter case, it is necessary to connect the transmit and receive pins together (pins 2 and 3) and ensure that the DCD signal is held high (connect pin 1 and pin 4 together). When the relay is switched into “Loopback Mode” the relay will automatically use generic addresses and will inhibit the InterMiCOM messages to the PSL by setting all eight InterMiCOM message states to zero. The loopback mode will be indicated on the relay frontplate by the amber Alarm LED being illuminated and a LCD alarm message, “IM Loopback”.

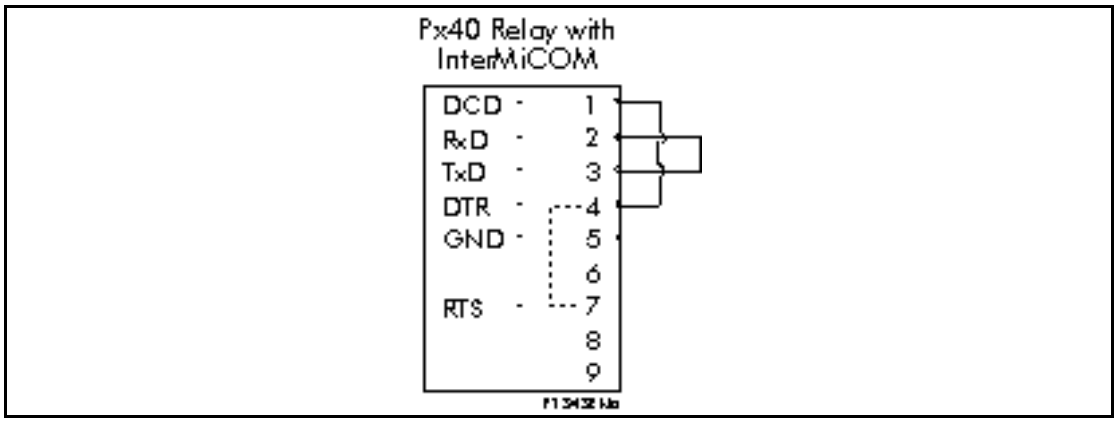


Figure 98: Connections for external loopback mode

Once the relay is switched into either of the Loopback modes, a test pattern can be entered in the “Test Pattern” cell which is then transmitted through the software and/or hardware. Providing all connections are correct and the software is working correctly, the “Loopback Status” cell will display “OK”. An unsuccessful test would be indicated by “FAIL”, whereas a hardware error will be indicated by “UNAVAILABLE”. Whilst the relay is in loopback test mode, the “IM Output Status” cell will only show the “Test Pattern” settings, whilst the “IM Input Status” cell will indicate that all inputs to the PSL have been forced to zero.

Care should be taken to ensure that once the loopback testing is complete, the “Loopback Mode” is set to “Disabled” thereby switching the InterMiCOM channel back in to service. With the loopback mode disabled, the “IM Output Status” cell will show the InterMiCOM messages being sent from the local relay, whilst the “IM Input Status” cell will show the received InterMiCOM messages (received from the remote end relay) being used by the PSL.

Once the relay operation has been confirmed using the loopback test facilities, it will be necessary to ensure that the communications between the two relays in the scheme are reliable. To facilitate this, a list of channel statistics and diagnostics are available in the InterMiCOM COMMS column – see section 10.2. It is possible to hide the channel diagnostics and statistics from view by setting the “Ch Statistics” and/or “Ch Diagnostics” cells to “Invisible”. All channel statistics are reset when the relay is powered up, or by user selection using the “Reset Statistics” cell.

Another indication of the amount of noise on the channel is provided by the communications failure alarm. Within a fixed 1.6 second time period the relay calculates the percentage of invalid messages received compared to the total number of messages that should have been received based upon the “Baud Rate” setting. If this percentage falls below the threshold set in the “IM Msg Alarm Lvl” cell, a “Message Fail” alarm will be raised.

5.7 Programmable function keys and tricolour LEDs (“Function key” menu)

The relay has 10 function keys for integral scheme or operator control functionality such as circuit breaker control, auto-reclose control etc. via PSL. Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands can be found in the ‘Function Keys’ menu. In the ‘Fn. Key Status’ menu cell there is a 10 bit word which represent the 10 function key commands and their status can be read from this 10 bit word. In the programmable scheme logic editor 10 function key signals, DDB 676 – 685, which can be set to a logic 1 or On state are available to perform control functions defined by the user.

The “Function Keys” column has ‘Fn. Key n Mode’ cell which allows the user to configure the function key as either ‘Toggled’ or ‘Normal’. In the ‘Toggle’ mode the function key DDB signal output will remain in the set state until a reset command is given, by activating the function key on the next key press. In the ‘Normal’ mode, the function key DDB signal will remain energized for as long as the function key is pressed and will then reset automatically.

A minimum pulse duration can be programmed for a function key by adding a minimum pulse timer to the function key DDB output signal. The “Fn. Key n Status” cell is used to enable/unlock or disable the function key signals in PSL. The ‘Lock’ setting has been

specifically provided to allow the locking of a function key therefore preventing further activation of the key on consequent key presses. This allows function keys that are set to 'Toggled' mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical relay functions. The "Fn. Key Labels" cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of the function keys is stored in battery backed memory. In the event that the auxiliary supply is interrupted the status of all the function keys will be recorded. Following the restoration of the auxiliary supply the status of the function keys, prior to supply failure, will be reinstated. If the battery is missing or flat the function key DDB signals will set to logic 0 once the auxiliary supply is restored. The relay will only recognise a single function key press at a time and that a minimum key press duration of approximately 200msec. is required before the key press is recognised in PSL. This deglitching feature avoids accidental double presses.

DDB: '**Function Key**' (see P44x/EN PL)

The activation of the function key will drive an associated DDB signal. The DDB signal will remain active depending on the programmed setting i.e. toggled or normal. Toggled mode means the DDB signal will remain latched or unlatched on key press and normal means the DDB will only be active for the duration of the key press.

DDB: '**FnKey LED 1 Red**'

Ten programmable tri-colour LEDs associated with each function key are used to indicate the status of the associated pushbutton's function. Each LED can be programmed to indicate red, yellow or green as required. The green LED is configured by driving the green DDB input. The red LED is configured by driving the red DDB input. The yellow LED is configured by driving the red and green DDB inputs simultaneously. When the LED is activated the associated DDB signal will be asserted. For example, if FnKey Led 1 Red is activated, DDB will be asserted.

DDB '**FnKey LED 1 Grn**'

The same explanation as for Fnkey 1 Red applies.

DDB '**LED 1 Red**'

Eight programmable tri-colour LEDs that can be programmed to indicate red, yellow or green as required. The green LED is configured by driving the green DDB input. The red LED is configured by driving the red DDB input. The yellow LED is configured by driving the red and green DDB inputs simultaneously. When the LED is activated the associated DDB signal will be asserted. For example, if Led 1 Red is activated, DDB #640 will be asserted.

DDB '**LED 1 Grn**'

The same explanation as for LED 1 Red applies.

5.8 Supervision

The "Supervision" menu contains 3 sections:

- the Voltage Transformer Supervision (VTS) section, for analog ac voltage inputs failures supervision,
- the Current Transformer Supervision (CTS) section, for ac phase current inputs failures supervision,
- the Capacitive Voltage Transformer Supervision (CVT) section, for voltage dividers capacitors supervision.

1.1.9 Voltage transformer supervision (VTS) – Main VT for minZ measurement

1.1.9.1 VTS description

The voltage transformer supervision (VTS) feature is used to detect failure of the analog ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in maloperation of the distance element.

The VTS logic in the relay is designed to detect the voltage failure (with internal thresholds or external opto input), and automatically adjust the configuration of protection elements (the distance element is blocked but may be unblocked by I1, I2 or I0 conditions in the event of a fault during VTS conditions) whose stability would otherwise be compromised (Distance, DEF, Weak infeed, Directionnal phase current & all directional elements used in the internal logic).

A settable time-delayed (VTS Time Delay) alarm output is also available (min 1s to max 20s). This alarm is instantaneous if an opto inputs is energised by an external fuse blowing signal (for instance from a micro circuit breaker contact). This external information is secure, and will instantaneously block the distance function and the functions using directional elements.

In the absence of load, the time-delay covers the duration of the Dead time-delay 1 of the autoreclose cycle which could be detected as a 1-pole VT failure.

Where a miniature circuit breaker (MCB) is used to protect the voltage transformer ac output circuits, it is common to use MCB auxiliary contacts to indicate a three phase output disconnection. As described previously, it is possible for the VTS logic to operate correctly without this input. However, this facility has been provided for compatibility with the current practices of various utilities. Energising an opto-isolated input assigned to “MCB Open” on the relay will therefore provide the necessary block.

Fuse failure conditions are confirmed instantaneously if the opto input receiving the fuse blowing signal is energised and assigned in the PSL, or after elapse of the VTS Time delay in case of 1-, 2- or 3-phase Fuse Failure.

Confirmed Fuse Failure blocks all protection functions which use the voltage measurement (Distance, Weak infeed, Directional overcurrent,etc.). The directional overcurrent element may be blocked or set to become non-directional with a dedicated time-delay ('I>1 Time Delay VTS' or 'IN>1 Time Delay VTS' setting).

An unconfirmed Fuse Failure will be a detection of an internal fuse failure before the time-delay has expired. In that case a fault can be detected by the I2>,I0>,I1>, ΔI> criteria and will force the unblocking functions:

- Distance Protection
- DEF Protection
- Weak-infeed Protection
- I> Directional
- U>, U<

1.1.9.2 Loss of one, two or three voltages (‘VTS I2 & I0 Inh’ and ‘Detect 3P’)

The three main aspects to consider regarding the failure of the VT supply are:

- Loss of one or two phase voltages
- Loss of all three phase voltages under load conditions
- Absence of three phase voltages upon line energisation

1.1.9.2.1 Loss of One or Two Phase Voltages

The VTS feature within the relay operates on detection of residual voltage without the presence of zero and negative phase sequence current, and earth fault current (ΣIph). This

gives operation for the loss of one or two phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of I0 and/or I2 current. Also, VTS operation is blocked (and distance element unblocked) when any phase current exceeds 2.5 × In.

Zero Sequence VTS Element:

The thresholds used by the element are:

- Fixed operate threshold: $V_N \geq$ 0.75 x Vn;
- Blocking current thresholds, I_0 = I_2 = 0 to 1 x In; settable (default 0.05In), and Iph = 2.5 x In.

1.1.9.2.2 Loss of All Three Phase Voltages Under Load Conditions

Under the loss of all three phase voltages to the relay, there will be no zero phase sequence quantities present to operate the VTS function. However, under such circumstances, a collapse of the three phase voltages will occur. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), then a VTS condition will be raised. In practice, the relay detects the presence of superimposed current signals (delta I), which are changes in the current applied to the relay. These signals are generated by comparison of the present value of the current with the value one cycle before. Under normal load conditions, the value of superimposed current should therefore be zero. Under a fault condition a superimposed current signal will be generated which will prevent operation of the VTS.

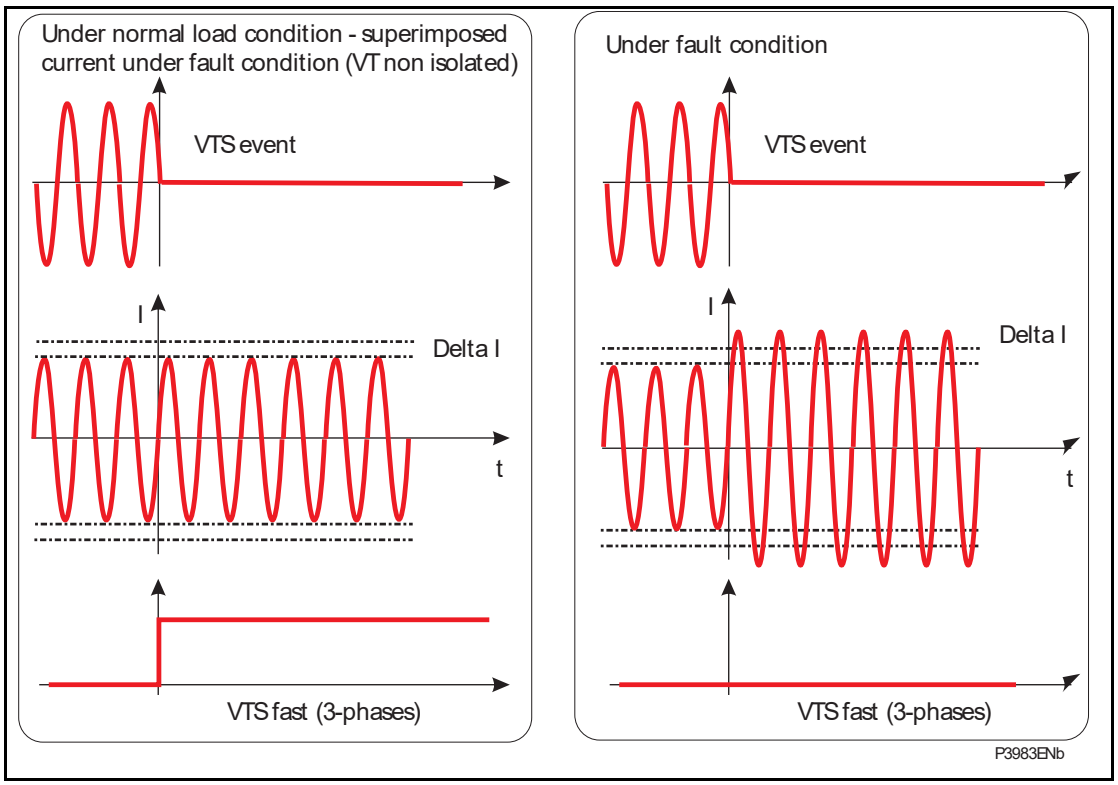


Figure 99: Line energisation – superimposed current under fault condition (VT non isolated)

If a VT were inadvertently left isolated prior to line energisation, on line energisation will change in current. If the phase currents do not exceed nominal current (superimposed current – delta – is null), VTS condition will be raised. If a fault condition is detected, superimposed current signal is generated and prevents operation of the VTS:

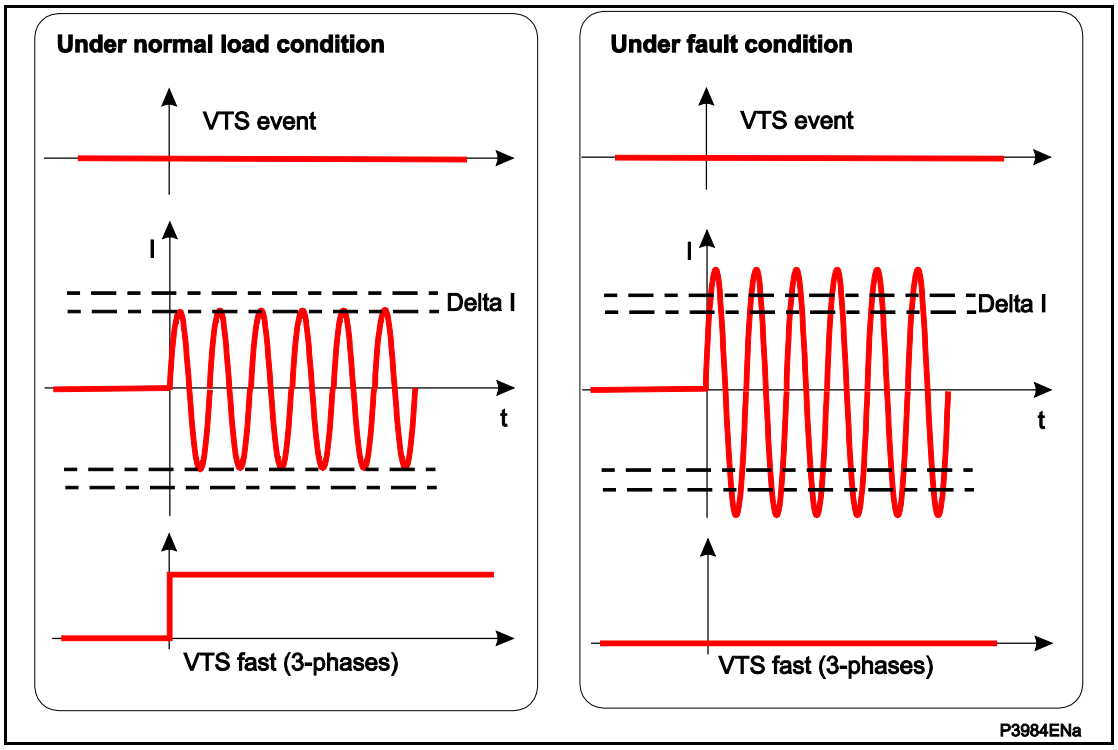


Figure 100: Line energisation – superimposed current under fault condition (VT isolated)

The phase voltage level detector is settable ('**Threshold 3P**' setting)).

The sensitivity of the superimposed current – '**delta I>**'– elements is settable and default value is set to 0.1In.

Caution: If line is energised at nominal current, delta I> has to be set at In + 20% for instance.

1.1.9.2.3 Absence of Three Phase Voltages on Line Energisation

If a VT were inadvertently left isolated prior to line energisation, incorrect operation of voltage dependent elements could result. The previous VTS element detected three phase VT failure by absence of all 3-phase voltages with no corresponding change in current. On line energisation there will, however, be a change in current (as a result of load or line charging current for example). An alternative method of detecting 3-phase VT failure is therefore required on line energisation: in that case the SOTF logic is applied.

1.1.9.3 Internal logic of the VT Failure detection

The VT failure (fuse blowing or fuse failure detection) alarm is given when the following conditions are met:

- VT Failure is internally detected and the VTS time-delay is elapsed (VT failure & VTS_Time_delay)
- Or the opto input dedicated to the function receives a fuse blowing signal (VTS opto input energised).

The equation (Figure 101) of the VT failure is:

Fuse Failure (confirmation of the fuse blowing) =
("Fuse Failure detected" AND "VTS Time-Delay")
OR "opto input energized"

The VT protection fuse blowing is detected when the following conditions are met:

- VN>: The residual voltage is higher than a fixed threshold:= 0,75Vn
- NOT I0>: The zero-sequence current is higher than I0> threshold:
- NOT I2>: The negative sequence current is higher than a I2> threshold (identical to the I0 threshold).

- NOT I>: The direct current is higher than a fixed threshold equal to 2,5In.
- V<: All the voltages are lower than a V< threshold.
- NOT ΔI>: The line currents' variation are higher than "Delta I" value.
- Detect 3P: setting that which allows the FFU three pole detection.
- Any pole dead: Cycle in progress.
  - The I0 criterion (zero sequence current threshold) makes it possible to UNBLOCK the distance protection in the event of phase-to-ground fault (if the fuse failure has not yet been confirmed).
  - The I2 criterion (negative sequence current threshold) makes it possible to UNBLOCK the distance protection in the event of insulated phase to phase fault (if the fuse failure has not been yet confirmed).
  - The (V< AND /ΔI) criterion makes it possible to detect the 3-pole Fuse Failure (no phase voltage and no current variation) (no specific line energisation logic).

Fuse Failure detected =
(VN> AND "NOT I0>" AND "NOT I2>" AND "NOT I>")
OR
("Detect 3P" AND "NOT Any pole dead" AND V< AND "NOT ΔI")

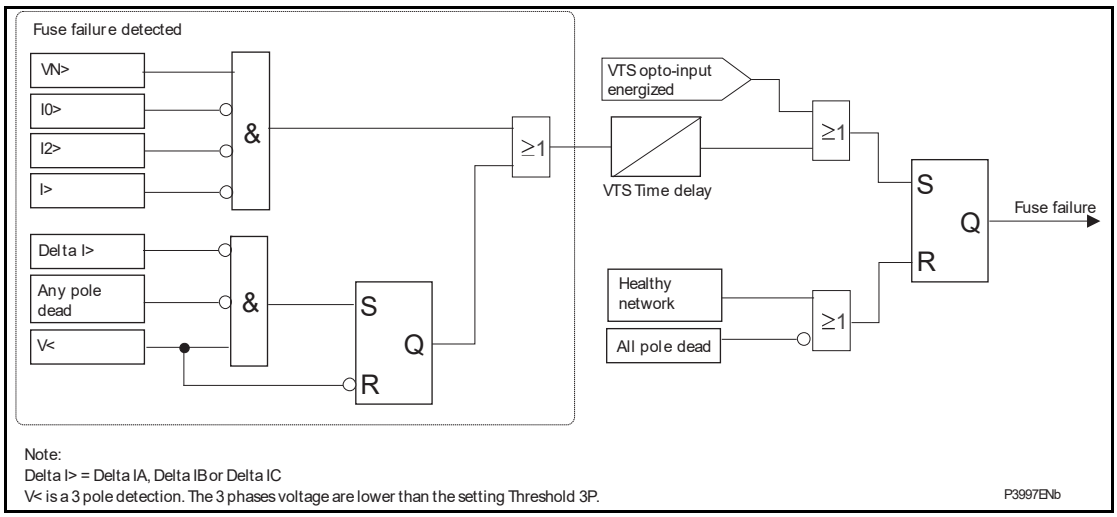


Figure 101: VTS logic

1.1.9.4 Fuse Failure Alarm reset

In the event of of a confirmed Fuse Failure, the condition which manages the reset is given by (Figure 101):

Fuse Failure (reset) =
"No Fuse Failure detected"
AND "NO opto input energized"
AND "Healthy netwotk"
AND "NO All Pole dead"

where:

- "All Pole dead" means "All circuit breaker poles dead (breaker open 3 phase)":
  All Pole Dead =
  "No current" AND "no voltage"
  OR CB Opened ((52a) if assigned in PSL)
- Healthy Network =
  "Rated Line voltage"
  AND "No V0" AND "No I0"
  AND "No start element" ∗
  AND "No Power Swing"

∗ = no CVMR (no General Start Convergency).

Healthy Network = U_N AND $\overline{V_0}$ AND $\overline{I_0}$ AND $\overline{CVMR}$ AND $\overline{PSWING}$

1.1.9.5 INPUT / OUTPUT DDBs used in the PSL:

The following DDBs are associated to VTS in the PSL (see section P44x/EN PL)

Inputs:

- MCB/VTS Main
- MCB/VTS Synchro

Outputs:

- VTS Fast
- VT Fail Alarm
- Any Pole Dead
- All Pole Dead

1.1.10 Current Transformer Supervision (CTS)

The current transformer supervision feature is used to detect failure of one or more of the ac phase current inputs to the relay. Failure of a phase CT or an open circuit of the interconnecting wiring can result in incorrect operation of any current operated element. Additionally, interruption in the ac current circuits risks dangerous CT secondary voltages being generated.

1.1.10.1 The CT Supervision Feature

The CT supervision feature operates on detection of derived (or measured) zero sequence current, in the absence of corresponding derived (or measured) zero sequence voltage that would normally accompany it. In this case, distance protection is blocked.

The voltage transformer connection used must be able to refer zero sequence voltages from the primary to the secondary side. Therefore, this element should only be enabled where the VT is of five limb construction, or comprises three single phase units, and has the primary star point earthed.

Operation of the element will produce a time-delayed alarm visible on the LCD and event record (DDB '**CT Fail Alarm**' will be high), with an instantaneous block for inhibition of protection elements. Protection elements operating from derived quantities (Broken Conductor, Earth Fault, Neg Seq O/C) are always blocked on operation of the CT supervision element.

1.1.10.2 Setting the CT Supervision Element

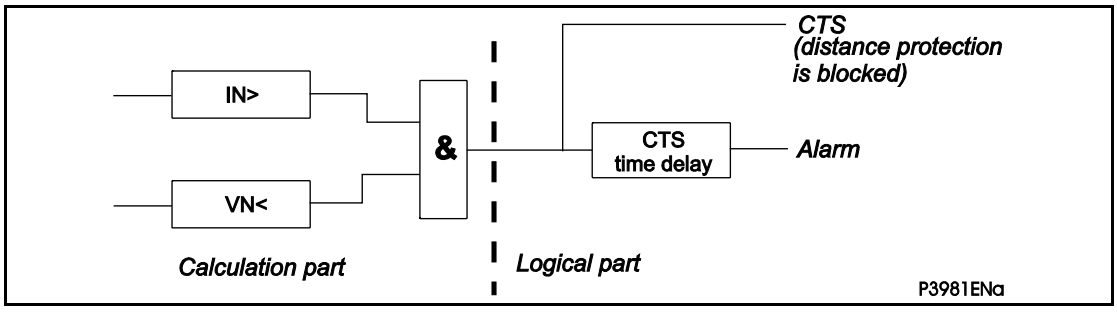


Figure 102: Basic CT supervision diagram

A "CTS fault" signal is sent out, after a settable time-delay if the conditions are as follows:

- The residual voltage is greater than the setting threshold during a delay greater then time delay
- The residual current is greater than the setting threshold.

The residual voltage setting, **CTS VN< Inhibit** and the residual current setting, **CTS IN> set**, should be set to avoid unwanted operation during healthy system conditions. For example **CTS VN< Inhibit** should be set to 120% of the maximum steady state residual voltage. The **CTS IN> set** will typically be set below minimum load current. The time-delayed alarm, **CTS Time delay**, is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element must be disabled to prevent a protection elements being blocked during fault conditions.

The DDB: '**CT Fail Alarm**' output is associated to CTS in the PSL (see section P44x/EN PL).

1.1.11 Capacitive Voltage Transformers Supervision (CVTS)

1.1.11.1 Function description

This Capacitive Voltage Transformers (CVT) Supervision will detect the degradation of one or several capacitors of voltage dividers. It is based on permanent detection of residual voltage.

A "CVT fault" signal is sent out, after a settable time-delay if the conditions are as follows:

- The residual voltage is greater than the setting threshold
- The 3 phase-phase voltages have a value greater than 0.4 Un
- If CVTS V2 Status > is set to Enabled and the negative sequence voltage is greater than setting CVTS V2>

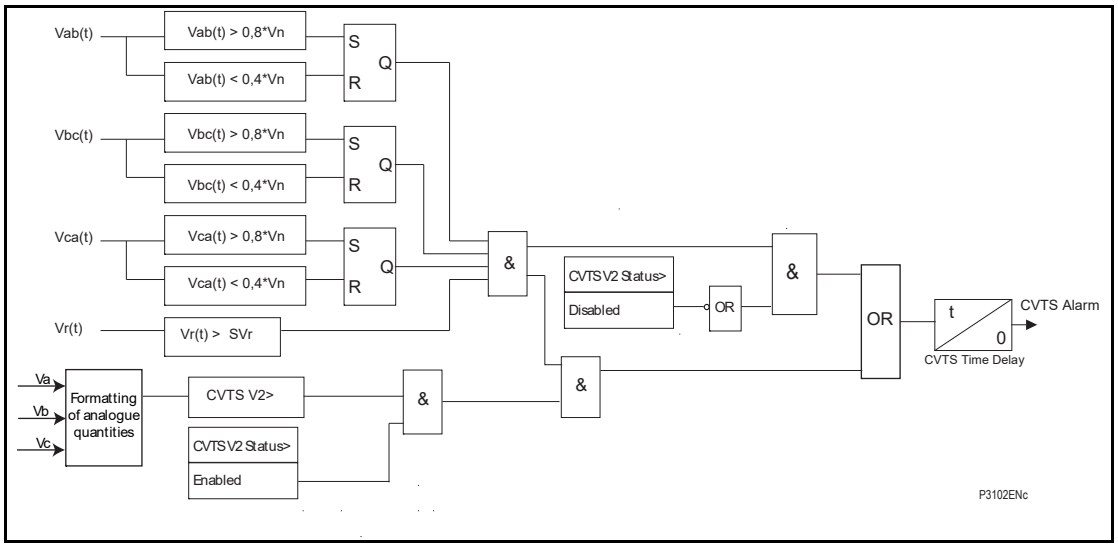


Figure 103: Basic CVT supervision diagram

1.1.11.2 OUTPUT DDB used in the PSL

The DDB: '**CVT ALARM**' is associated to CVTS in the PSL (see section P44x/EN PL).

1.2 Check synchronisation

The check synchronism option is used to qualify reclosure of the circuit breaker so that it can only occur when the network conditions on the busbar and line side of the open circuit breaker are acceptable. If a circuit breaker were closed when the two system voltages were out of synchronism with one another, ie. a difference in voltage magnitudes or phase angles existed, the system would be subjected to an unacceptable 'shock', resulting in loss of stability and possible damage to connected machines.

Check synchronism therefore involves monitoring the voltage on both sides of a circuit breaker and, if both sides are 'live', the relative synchronism between the two supplies. Such checking may be required to be applied for both automatic and manual reclosing of the circuit breaker and the system conditions which are acceptable may be different in each case. For this reason, separate check synchronism settings are included within the relay for both manual and automatic reclosure of the circuit breaker. With manual closure, the CB

close signal is applied into the logic as a pulse to ensure that an operator cannot simply keep the close signal applied and wait for the system to come into synchronism. This is often referred to as guard logic and requires the close signal to be released and then re-applied if the closure is unsuccessful.

The check synchronism element provides two 'output' signals which feed into the manual CB control and the auto reclose logic respectively. These signals allow reclosure provided that the relevant check synchronism criteria are met.

Note that if check-synchronisim is disabled, the DDB: '**Check synch. OK**' signal is automatically asserted and becomes invariant (logical state always forced to 1).

For an interconnected power system, tripping of one line should not cause a significant shift in the phase relationship of the busbar and line side voltages. Parallel interconnections will ensure that the two sides remain in synchronism, and that autoreclosure can proceed safely. However, if the parallel interconnection(s) is/are lost, the frequencies of the two sections of the split system will begin to slip with respect to each other during the time that the systems are disconnected. Therefore, a live busbar / live line synchronism check prior to reclosing the breaker ensures that the resulting phase angle displacement, slip frequency and voltage difference between the busbar and line voltages are all within acceptable limits for the system. If they are not, closure of the breaker can be inhibited.

The SYSTEM CHECKS menu contains all of the check synchronism settings for auto ("A/R") and manual ("Man") reclosure.



- If SOTF is disabled in S1, a dedicated PSL must be created using Deb B (live line or live bus/dead line) – live/live cannot be managed – in that case.

Note that the combination of the Diff Phase and Bus-Line Delay settings can also be equated to a differential frequency, as shown below:

- Diff Phase angle set to +/-20°, Bus-Line Delay set to 0.2 s.
- The phase angle 'window' is therefore 40°, which corresponds to 40/360ths of a cycle = 0.111 cycle. This equates to a differential frequency of:

$$0.111 / 0.2 = 0.55 \text{ Hz}$$

Therefore it is essential that the time delay chosen before an "in synchronism" output can be given is not too long, otherwise the synchronising conditions will appear more restrictive than the actual Diff Frequency setting.

The Live Line and Dead Line settings define the thresholds which dictate whether or not the line or bus is determined as being live or dead by the relay logic. Under conditions where either the line or bus is dead, check synchronism is not applicable and closure of the breaker may or may not be acceptable. Therefore, setting options are provided which allow for both manual and auto-reclosure under a variety of live/dead conditions. The following paragraphs describe where these may be used.

WARNING: Voltage setting is always calculated in phase to ground – even if phase/phase ref has been selected.



If the live line threshold has been set too high, the relay will never detect a healthy network (as the line voltage is always measured below the voltage threshold). Without the live line condition, the distance protection cannot use the delta algorithms as no pre-fault detection has been previously made.

1.2.1 Live Busbar and Dead Line

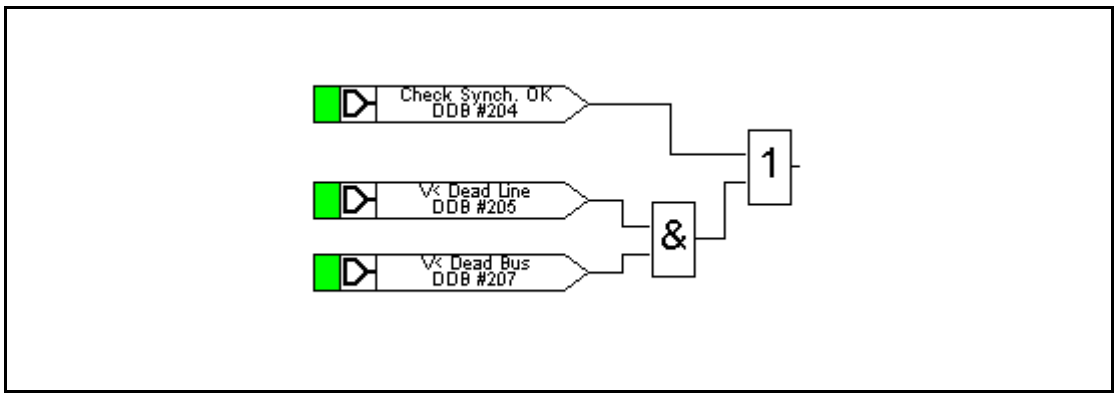
Where a radial feeder is protected, tripping the circuit breaker will isolate the infeed, and the feeder will be dead. Provided that there is no local generation which can backfeed to energise the feeder, reclosure for live busbar / dead line conditions is acceptable. This setting might also be used to allow re-energisation of a faulted feeder in an interconnected power system, which had been isolated at both line ends. Live busbar / dead line reclosing allows energising from one end first, which can then be followed by live line / live busbar reclosure with voltages in synchronism at the remote end.

1.2.2 Dead Busbar and Live Line

If there is a circuit breaker and busbar at the remote end of the radial feeder mentioned above, the remote breaker might be reclosed for a dead busbar / live line condition.

1.2.3 Dead Busbar and Dead Line

This mode is not integrated in the internal logic, however it can be created using a dedicated PSL:



This setting may also be used to allow manual close with specific test conditions on the CB.

1.2.4 Check Synchronism Settings

The main three phase VT location (busbar or line is set in the '**CT & VT RATIOS / Main VT Location**' setting to allow the previously described logic to operate correctly. (see DDB description below)

Note that the check synchronism VT input may be driven from either a phase to phase or phase-to-neutral voltage '**CT & VT Ratios / C/S Input**' cell.

If the VTS feature internal to the relay operates, the check synchronism element is inhibited from giving an 'Allow Reclosure' output. This avoids allowing reclosure in instances where voltage checks are selected and a VT fuse failure has made voltage checks unreliable.

Measurements of the magnitude angle and delta frequency (slip frequency) – system rated frequency is displayed by default in the event of problems with the delta f calculation: No line voltage or no bus voltage or neither of the check synchronism voltages are displayed in the '*MEASUREMENTS 1*' column.

Individual System Check logic features can be enabled or disabled by means of the **C/S Check Scheme** function links. Setting the relevant bit to 1 will enable the logic, setting bits to 0 will disable that part of the logic. Voltage, frequency, angle and time-delay thresholds are shared for both manual and autoreclosure, it is the live/dead line/bus logic which can differ.

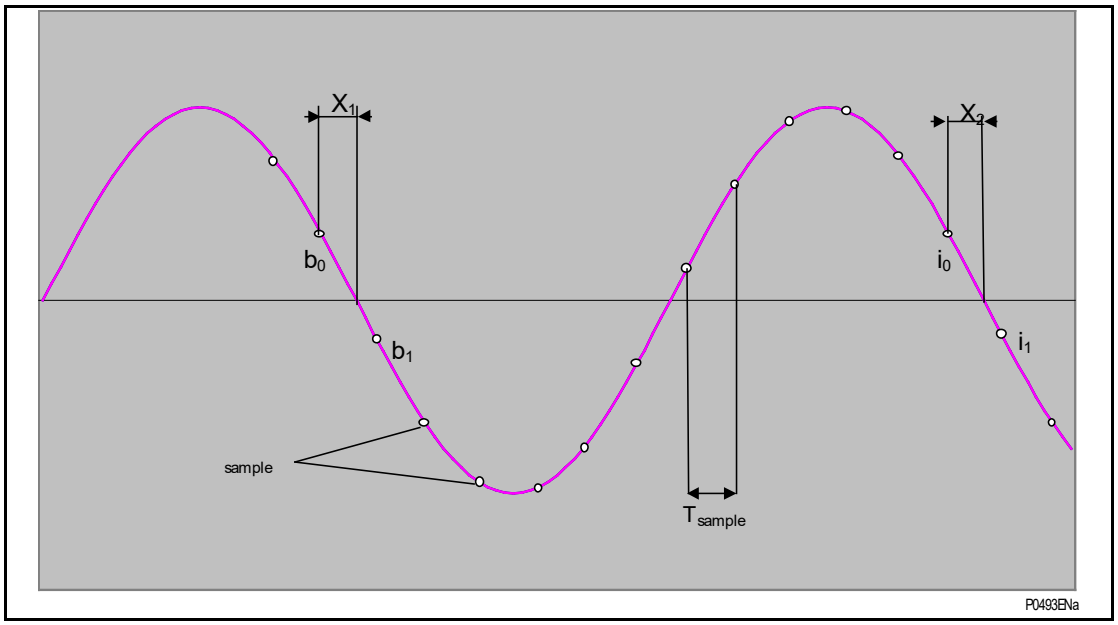


Figure 104: Frequency calculation

Frequency tracking is calculated by: $freq=1/((X_2-X_1+ Nb_{samples})* T_{samples})$

With $X_1 = b_0 /(b_0 – b_1)$ et $X_2 = I_0 /(I_0 – I_1)$.

$T_{samples}$ is the sampling period.

$Nb_{samples}$ is the number of samples per period (between b1 and i1 (b1 being excluded))

The Line & Bus frequencies are calculated with the same principle (described here after).

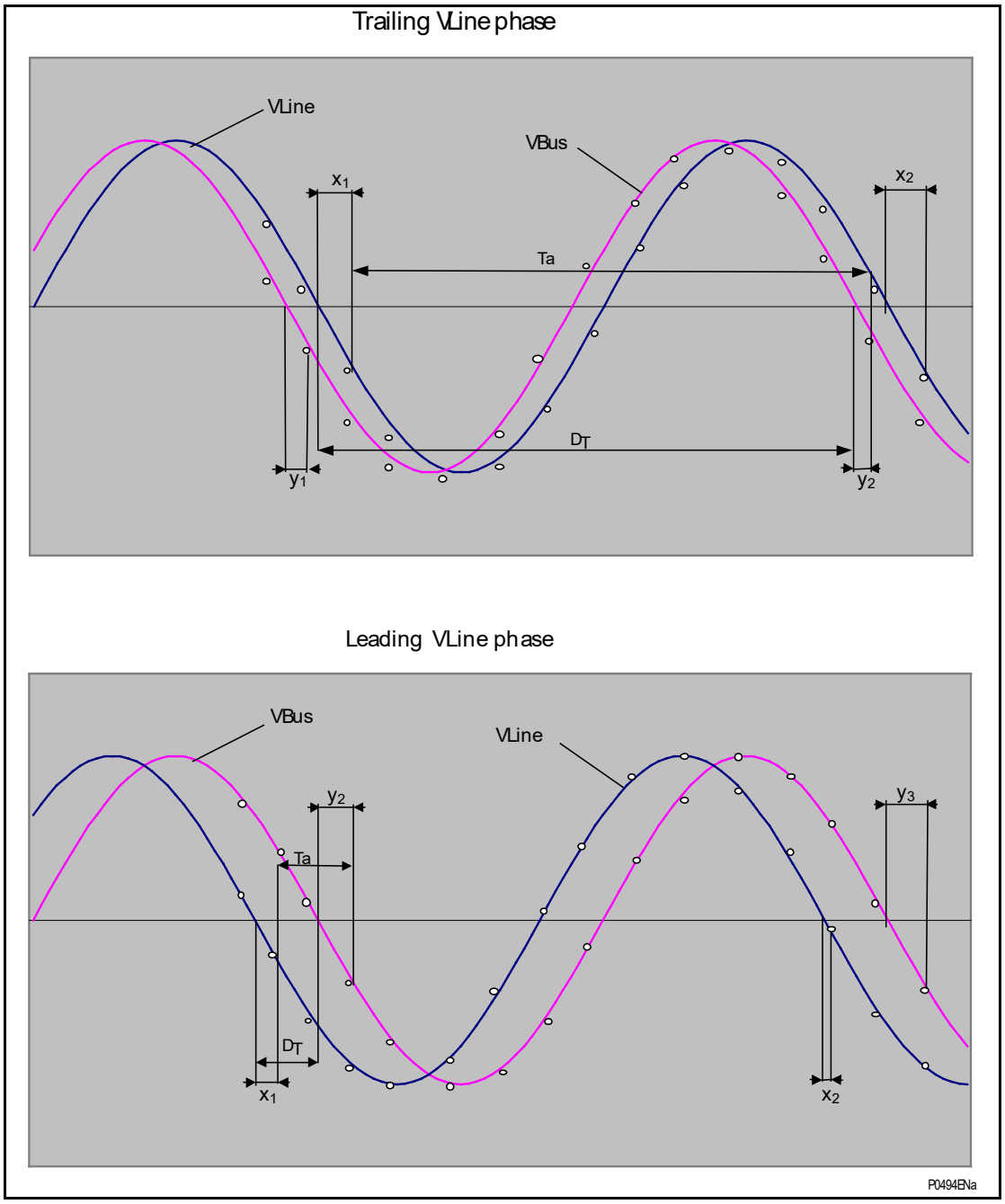


Figure 105: Calculation of Diff. phase

Phase shift = (ΔT/ T) *360

ΔT = Ta + (x1-y2)

A phase shift calculation requires a change of sign of both signals.

All the angles will be between 0° and 180°. For a phase shift of 245°, (360 –245) = 115° will be displayed

1.2.5 DDBs from Check Synchronism function used in the PSL

The following DDBs are associated with the the check synchronization logic in the PSL (see P44x/EN PL).

Logic inputs used by the check synchronism logic:

- MCB/VTS Synchro,
- MCB/VTS Main,

are managed dynamically (regarding where the main VT are located:bus side or line side – then the Csync ref is assigned to the other VT which is managed as the Csync ref)

Logic DDB outputs issued by the check sync logic

- Check Sync OK [Used with AR close in the relevant PSL – "AND" gate: [(AR Close) & (CheckSync OK)]
- A/R Force Sync,
- V<Dead Line
- V>Live Line
- V<Dead Bus
- V>Live Bus
- Control No C/S
- Ext Chk Synch OK



WARNING: TO ENSURE THAT THE AUTORECLOSE COMMAND IS CONTROLLED BY THE CHECK SYNCHRONISM CONDITIONS, THE ABOVE PSL SHOULD BE SET.

(Different schemes can be created with internal AR & external CSync or internal Csync & external AR)

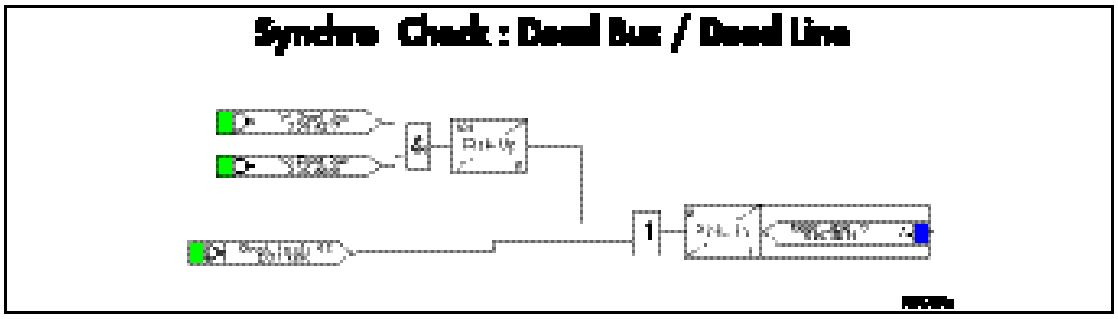


Figure 106: Check sync psl logic

Logic Diagram:

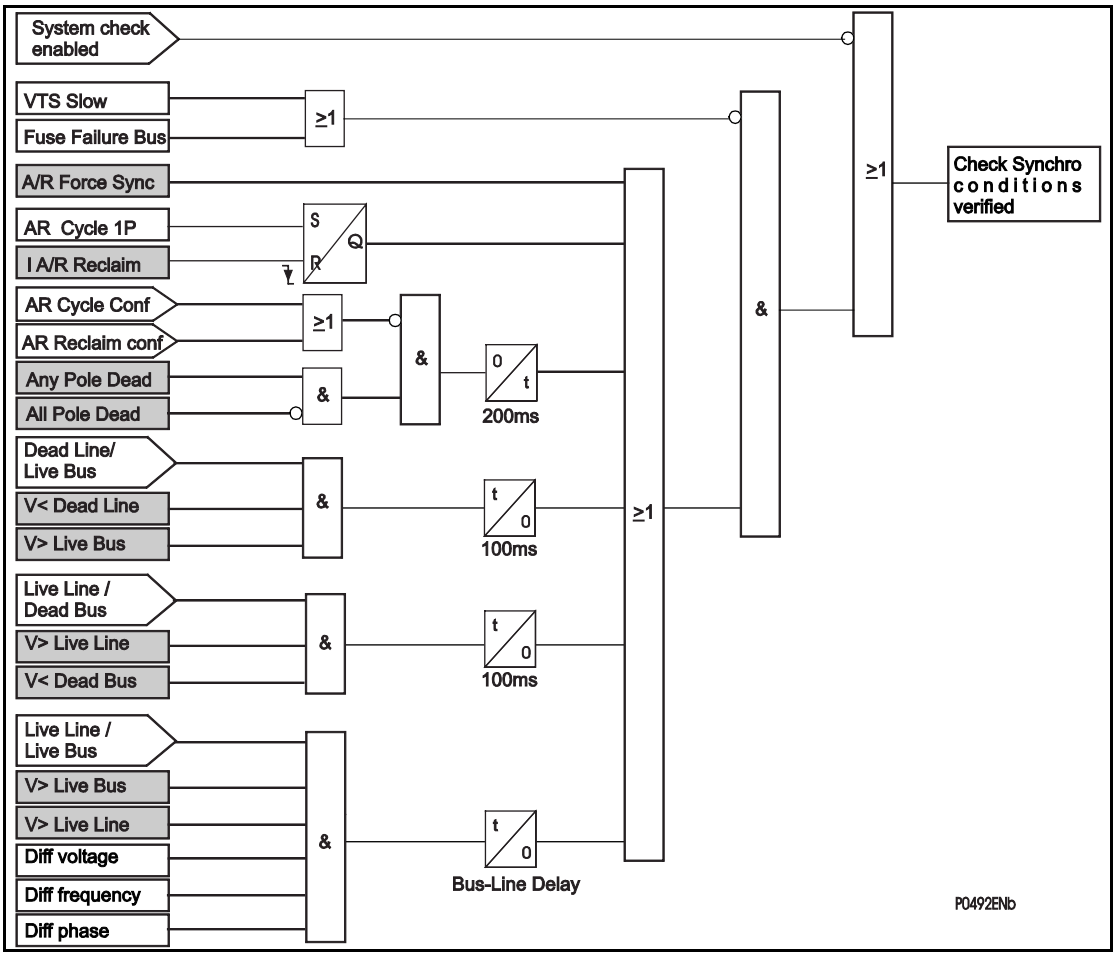


Figure 107: Check sync logic description

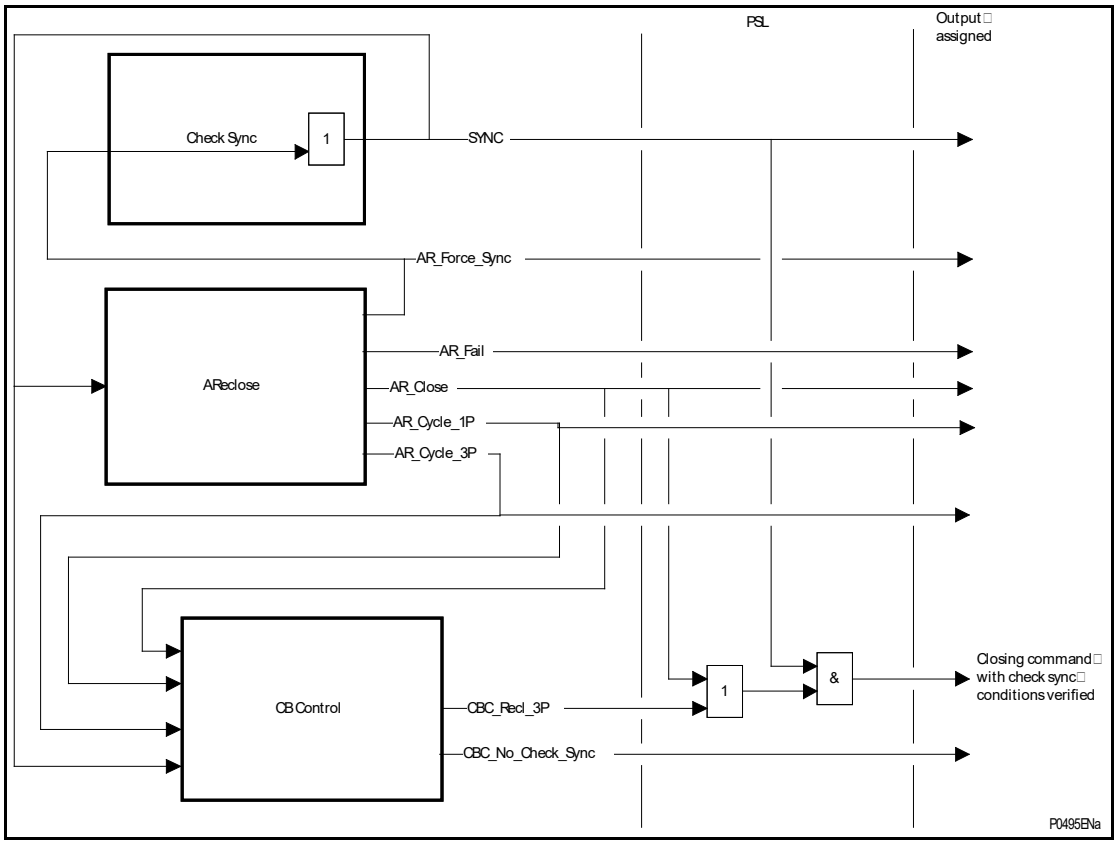


Figure 108: Internal check synchronism and internal autoreclose logic

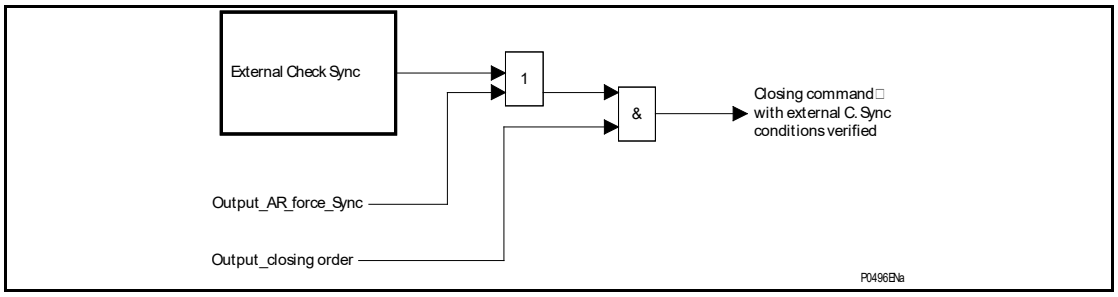


Figure 109: Logic with external synchronisation check

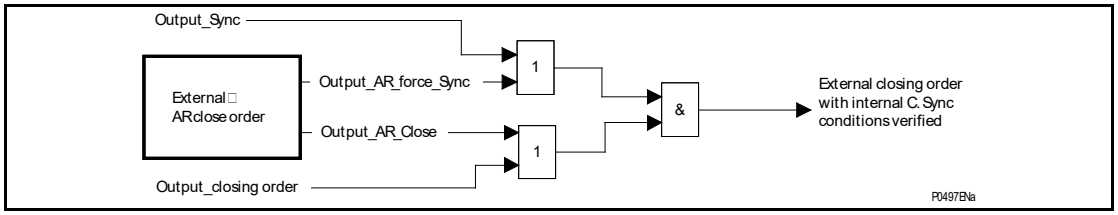


Figure 110: Logic with external autoreclose

5.9 Autorecloser

The relay autorecloser provides selectable multishot reclosure of the line circuit breaker. The standard scheme logic is configured to permit control of one circuit breaker. Autoreclosure of two circuit breakers in a 1½ circuit breaker or mesh corner scheme is not supported by the standard logic (Dedicated PSL must be created & tested by user). The autorecloser can be adjusted to perform a single shot, two shot, three shot or four shot cycle. Dead times for all shots (reclose attempts) are independently adjustable (using setting).

Where the relay is configured for single and three pole tripping, the recloser can perform a high speed single pole reclose shot, for a single phase to earth fault. This single pole shot may be followed by up to three delayed autoreclose shots, each with three phase tripping and reclosure. For a three pole trip, up to four reclose shots are available in the same scheme. Where the relay is configured for three pole tripping only, up to four reclose shots are available, each performing three phase reclosure.

An analysis of faults on any overhead line network has shown that 80-90% are transient in nature. Lightning is the most common cause, other possibilities being clashing conductors and wind blown debris. Such faults can be cleared by the immediate tripping of one or more circuit breakers to isolate the fault, followed by a reclose cycle for the circuit breakers. As the faults are generally self clearing ‘non-damage’ faults, a healthy restoration of supply will result.

The remaining 10 - 20% of faults are either semi-permanent or permanent. A semi-permanent fault could be caused by a small tree branch falling on the line. The cause of the fault may not be removed by the immediate tripping of the circuit, but could be burnt away/thrown clear after several further reclose attempts or “shots”. Therefore several time delayed shots may be required in forest areas.

Permanent faults could be broken conductors, transformer faults or cable faults which must be located and repaired before the supply can be restored.

In the majority of fault incidents, if the faulty line is immediately tripped out, and time is allowed for the fault arc to de-ionise, reclosure of the circuit breakers will result in the line being successfully re-energised, with obvious benefits. The main advantages to be derived from using autoreclose can be summarised as follows:

- Minimises interruptions in supply to the consumer;
- A high speed trip and reclose cycle clears the fault without threatening system stability.

When considering feeders which are partly overhead line and partly underground cable, any decision to install auto-reclosing would be influenced by any data known on the frequency of transient faults. When a significant proportion of the faults are permanent, the advantages of auto-reclosing are small, particularly since reclosing on to a faulty cable is likely to aggravate the damage.

At subtransmission and transmission voltages, utilities often employ single pole tripping for earth faults, leaving circuit breaker poles on the two unfaulted phases closed. High speed single phase autoreclosure then follows. The advantages and disadvantages of such single pole trip/reclose cycles are:

- Synchronising power flows on the unfaulted phases, using the line to maintain synchronism between remote regions of a relatively weakly interconnected system.
- However, the capacitive current induced from the healthy phases can increase the time taken to de-ionise fault arcs.

1.2.6 Functional description

The following diagram summarizes the autoreclose process:

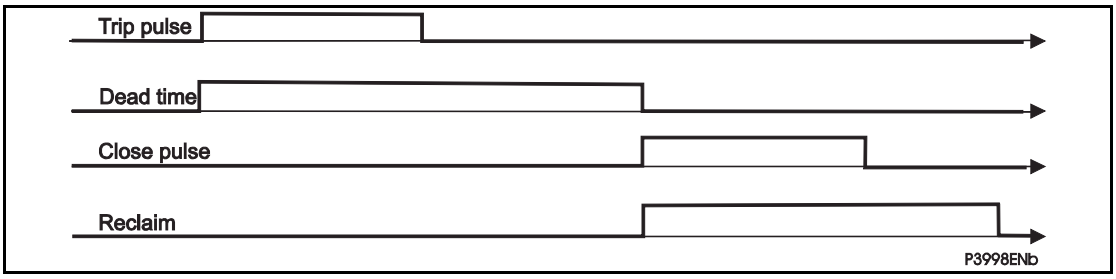


Figure 111: Autoreclose timing diagram

Should autoreclosure not be required, the function may be Disabled in the relay **Configuration** menu. Disabling the autorecloser does not prevent the use of the internal check synchronism element to supervise manual circuit breaker closing.

An autoreclose cycle is internally initiated by operation of a protective element (could be started by an internal trip or external trip), provided the circuit breaker is closed at the instant of protection operation. The appropriate dead time-delay for the shot is started (**Dead Time 1, 2, 3 or 4;** noting that separate dead times are provided for the first high speed shot of single pole (1P), and three pole (3P), reclosure). At the end of the dead time, a CB close pulse command of **'Close Pulse Time**' duration (see section 5.1: '**CB Control**" menu) is given, provided system conditions are suitable.

The reclaim time (**Reclaim Time**) starts with the CB Close pulse. If the circuit breaker has not been retripped, the autoreclose logic is reset at the end of the reclaim time. The autorecloser is ready again to start a new cycle again from the first shot a new cycle again (for future faults). If the protection retrips during the reclaim time, the relay either advances to the next shot in the programmed autoreclose cycle, or, if all programmed reclose attempts have been made, goes to lockout.

The following timing diagram illustrates the P44x autoreclose cycle (1P / 3P trip) in normal condition:

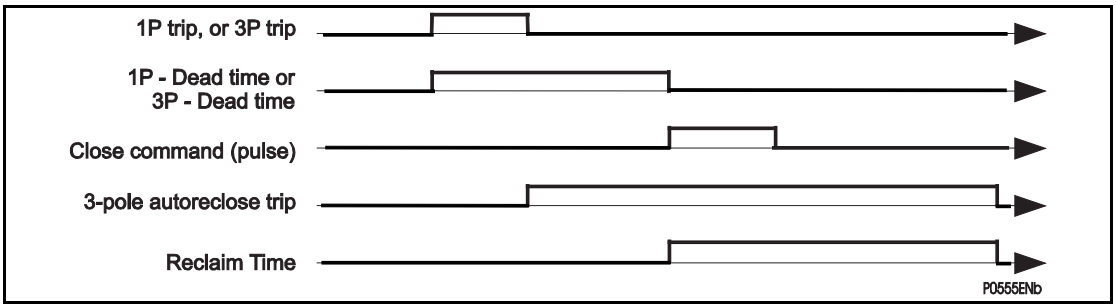


Figure 112: Autoreclose cycle – general description

The conditions to be met for closing are that the system voltages satisfy the internal check synchronism criteria (see Check synchronisation section), and that the circuit breaker closing spring, or other energy source, is fully charged. The following diagram illustrates a second trip command before the end of reclaim time:

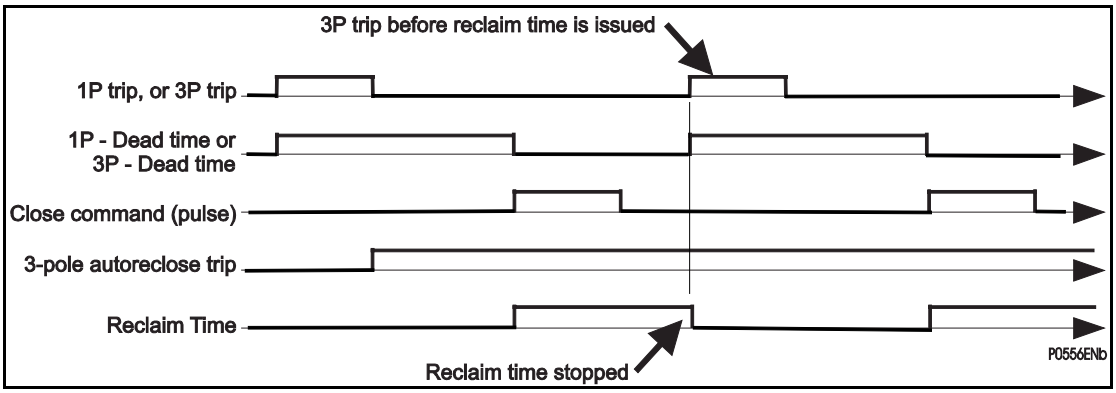


Figure 113: Successive autoreclose cycles

If protection operates during the reclaim time, after the final reclose attempt, the relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition is reset. This will produce an alarm, **AR Lockout**. Then, the DDB: '**BAR**' input will block the autorecloser and cause a lockout if a reclose cycle is in progress. Lockout will also occur if the CB energy is low and that the CB fails to close. Once the autorecloser is locked out, it will not function until a Reset Lockout or CB Manual Close command is received (depending on the Reset Lockout method chosen in **CB Monitor Setup**).

Note:	*Lockout can also be caused by the CB condition monitoring functions maintenance lockout, excessive fault frequency lockout, broken current lockout, CB failed to trip and CB failed to close, manual close no check synchronism and CB unhealthy.*

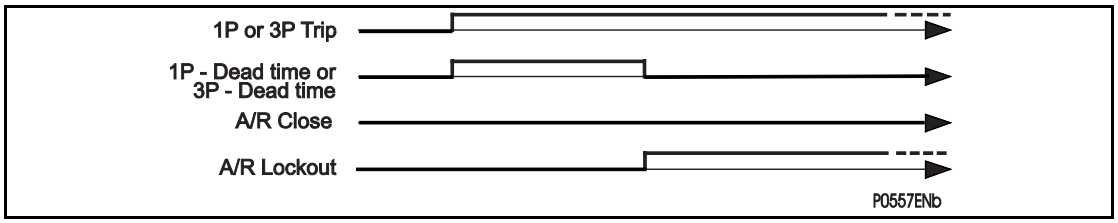


Figure 114: Trip signal still present when dead time elapses will force AR lockout

1.2.6.1 Number of shot (trip mode cells) setting

There are no clear-cut rules for defining the number of shots for any particular application. To determine the required number of shots, the following factors must be taken into account:

- An important consideration is the ability of the circuit breaker to perform several trip close operations in quick succession and the effect of these operations on the maintenance period.
- The fact that 80 - 90% of faults are transient highlights the advantage of single shot schemes. If statistical information for the power system shows that a moderate percentage of faults are semi-permanent, further time-delayed autoreclose shots may be used provided that system stability is not threatened.

The relay allows up to four reclose shots, ie. one high speed single pole autoreclose shot, plus up to three time-delayed shots. All time-delayed shots have three-pole operation. The scheme is selected in the relay menu as follows:

"1P Trip Mode"	**first shot**	**second shot**	**3rd shot**	**4th shot**
1	1P	--	--	--
1 / 3	1P	3P	--	--
1 / 3 / 3	1P	3P	3P	--
1 / 3 / 3 / 3	1P	3P	3P	3P
"3P Trip Mode"				
1	3P	--	--	--
1 / 3	3P	3P	--	--
1 / 3 / 3	3P	3P	3P	--
1 / 3 / 3 / 3	3P	3P	3P	3P

"1P": Single Pole autoreclose shot
"3P": Three Pole autoreclose shot
"--": No shot.

Table 13: Reclosing scheme for single phase trips

If single pole and three pole autoreclose are enabled, then:

- If the first fault is a single phase fault, a single pole autoreclose sequence will start,
- If the first fault is a multi phase fault, the first autoreclose sequence a three pole autoreclose sequence will start.

1.2.6.2 Dead-time setting

At the end of the relevant dead time, the autoreclose single phase or three phase in progress signal is reset and a CB close signal is given, provided system conditions are suitable. The system conditions to be met for closing are that the system voltages are in synchronism or dead line/live bus or live line/dead bus conditions exist, indicated by the internal check synchronism element and that the circuit breaker closing spring, or other energy source, is fully charged indicated from the DDB: '**CB Healthy**' input. The CB close signal is cut-off when the circuit breaker closes. For single pole autoreclose no voltage or synchronism check is required as synchronising power is flowing in the two healthy phases. Check synchronism for the first three phase cycle is controlled by a setting.

High speed autoreclose may be required to maintain stability on a network with two or more power sources. For high speed autoreclose, the system disturbance time should be minimised by using fast protection, <50 ms, such as distance or feeder differential protection and fast circuit breakers <100 ms. For stability between two sources a system dead time of <300 ms may typically be required. The minimum system dead time considering just the CB is the trip mechanism reset time plus the CB closing time.

Minimum relay dead time settings are governed primarily by two factors:

- Time taken for de-ionisation of the fault path (see specific section below);
- Circuit breaker characteristics.

Also it is essential that the protection fully resets during the dead time, so that correct time discrimination will be maintained after reclosure onto a fault. For high speed autoreclose instantaneous reset of protection is required.

For highly interconnected systems synchronism is unlikely to be lost by the tripping out of a single line. Here the best policy may be to adopt longer dead times, to allow time for power swings on the system resulting from the fault to settle.

Should a single phase fault evolve to affect other phases during the single pole dead time, the recloser will then move to the appropriate three phase cycle.

1.2.6.2.1 De-Ionising Time

The de-ionisation time of a fault arc depends on circuit voltage, conductor spacing, fault current and duration, wind speed and capacitive coupling from adjacent conductors. As circuit voltage is generally the most significant, minimum de-ionising times can be specified as in the Table below.

NOTE: For single pole autoreclose shot, the capacitive current induced from the healthy phases can increase the time taken to de-ionise fault arcs.

Line Voltage (kV)	Minimum De-Energisation Time (s)
66	0.1
110	0.15
132	0.17
220	0.28
275	0.3
400	0.5

Table 14: Minimum fault arc de-ionising time (three pole tripping)

Example Minimum Dead Time Calculation

The following circuit breaker and system characteristics are to be used:

- CB Operating time (Trip coil energised → Arc interruption): 50ms (a);

- CB Opening + Reset time (Trip coil energised → Trip mechanism reset): 200ms (b);
- Protection reset time: < 80ms (c);
- CB Closing time (Close command → Contacts make): 85ms (d).

De-ionising time for 220kV line:

- 280ms (e) for a three phase trip. (560ms for a single pole trip).

The minimum relay dead time setting is the greater of:

(a) + (c) = 50 + 80 = 130ms, to allow protection reset;

(a) + (e) - (d) = 50 + 280 - 85 = 245ms, to allow de-ionising (three pole);

= 50 + 560 - 85 = 525ms, to allow de-ionising (single pole).

In practice a few additional cycles would be added to allow for tolerances, so **3P - Dead Time 1** could be chosen as ≥ 300ms, and **1P - Dead Time 1** could be chosen as ≥ 600ms. The overall system dead time is found by adding (d) to the chosen settings, and then subtracting (a). (here this gives 335ms and 635ms respectively).

1.2.6.3 Reclaim time

When the CB has closed, the reclaim time ("Reclaim Time") starts. If the circuit breaker does not trip again, the autoreclose function resets at the end of the reclaim time. If the protection operates during the reclaim time the relay either advances to the next shot in the programmed autoreclose cycle, or, if all programmed reclose attempts have been made, goes to lockout. The reclaim time is reset on expiry of the reclaim time-delay (setting) or if a new 1P or 3P trip command is issued (see logic diagram).

A number of factors influence the choice of the reclaim timer, such as;

- Fault incidence/Past experience - Small reclaim times may be required where there is a high incidence of recurrent lightning strikes to prevent unnecessary lockout for transient faults.
- Spring charging time - For high speed autoreclose the reclaim time may be set longer than the spring charging time. A minimum reclaim time of >5s may be needed to allow the CB time to recover after a trip and close before it can perform another trip-close-trip cycle. This time will depend on the duty (rating) of the CB. For delayed autoreclose there is no need as the dead time can be extended by an extra CB healthy check **AR Inhibit Wind** window time if there is insufficient energy in the CB.
- Switchgear Maintenance - Excessive operation resulting from short reclaim times can mean shorter maintenance intervals.
- The Reclaim Time setting is always set greater than the tZ2 distance zone delay.

1.2.6.4 Discrimination time setting

When a single pole trip is issued by the relay, a 1-pole autoreclose cycle is initiated. The Dead time1 and Discrimination timer are started.

If the autoreclose logic detects a single pole or three-pole trip (internal or external) during the discrimination time-delay, the 1P high speed autoreclose cycle is disabled and replaced by a 3P high speed autoreclose cycle (if 3P trip mode is enabled, otherwise, the relay trips 3-poles and the autorecloser is blocked):

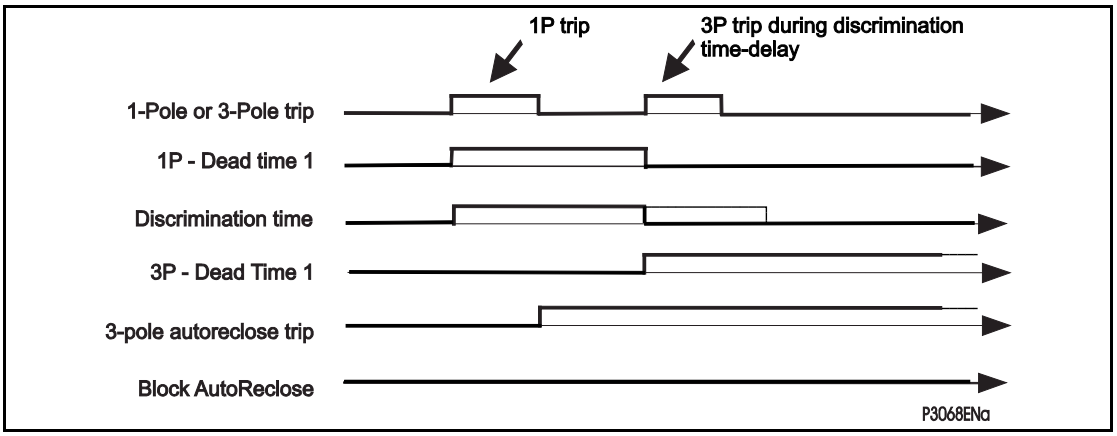


Figure 115: Fault during an autoreclose cycle during (discrimination Time-delay has not expired)

If the autoreclose logic detects a 3-pole trip (internal or external) on expiry of the discrimination time-delay, and during the 1P dead time; the single pole autoreclose cycle is stopped and the relay trips 3-pole and blocks the autorecloser (see Figure 116).

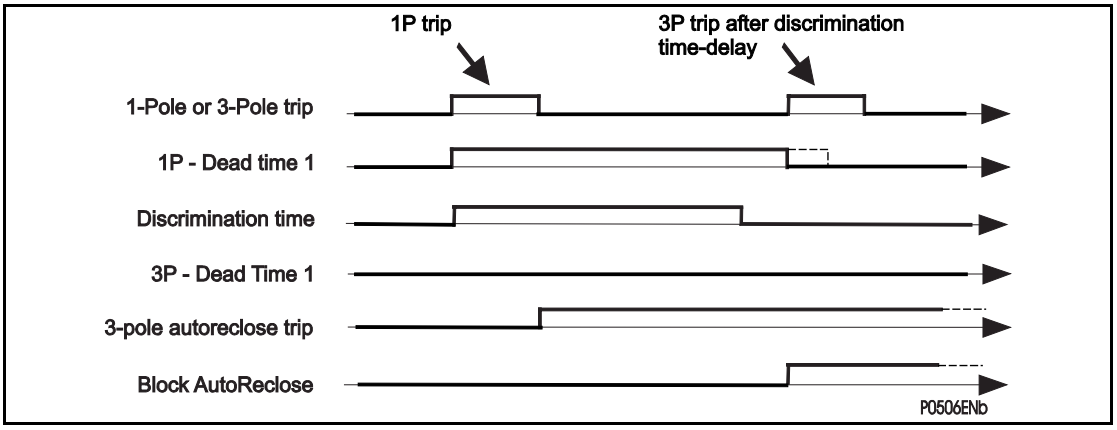


Figure 116: Fault during an autoreclose 1P cycle (discrimination time-delay has expired)

5.9.1.1 Autoreclose inhibit window

Most circuit breakers are only capable of providing one trip-close-trip cycle. It is necessary to re-establish sufficient energy in the circuit breaker before the CB can be reclosed. The CB healthy information from the CB (DDB: '**CB Healthy**') is used to ensure that there is sufficient energy available to close and trip the CB before initiating a CB close command.

If on completion of the dead time (1), the relay does not detect sufficient energy within a period given by the autoreclose inhibition window (3) – ('**A/R Inhibit Wind**' setting), lockout will result (4) and the CB will remain open (Blocking Autoreclose, DDB: '**BAR**').

If the CB energy becomes healthy again within the time window (2), autoreclosure will occur.

This check can be disabled by not allocating it any opto input. In this case, the DDB cell '**CB Healthy**' is considered invariant in the relay's logic. This means that the signal is always high within the relay when the logic requires a high level and at 0 if low level is required. It is an invariant state for the firmware (same logic is applied for every optional opto input – if not linked in the PSL these cells are managed as invariant data by the internal logic).

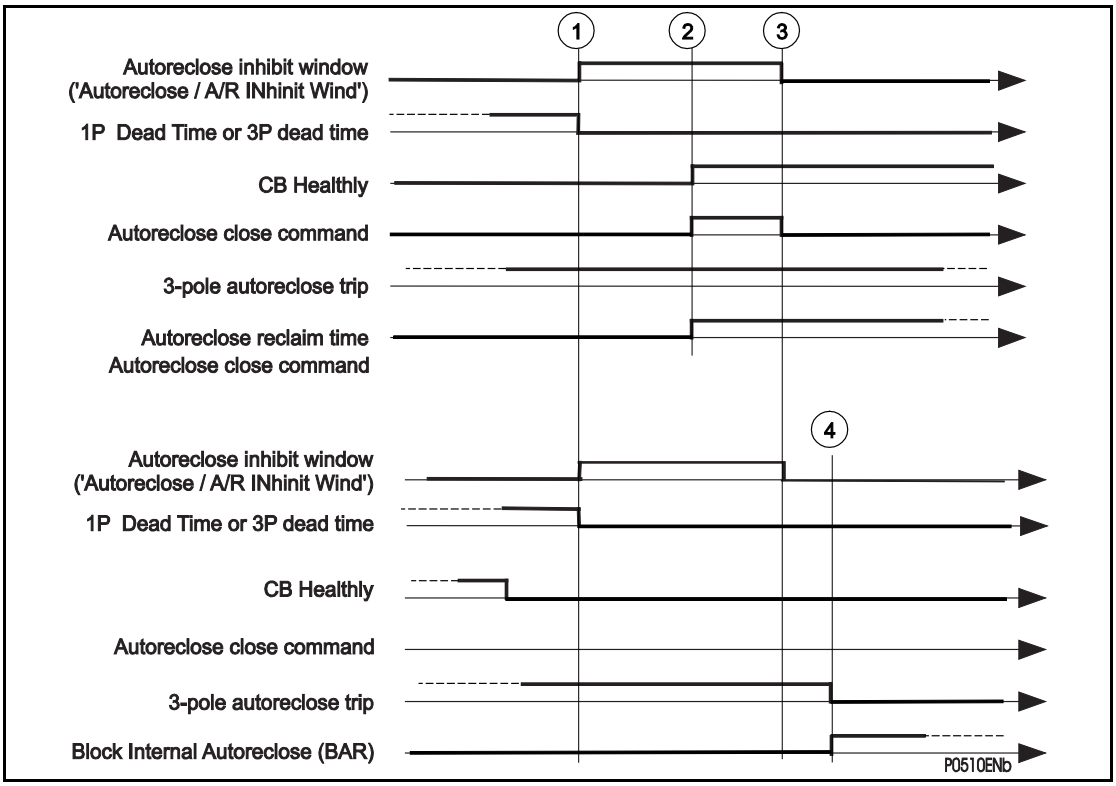


Figure 117: Autoreclose inhibit window

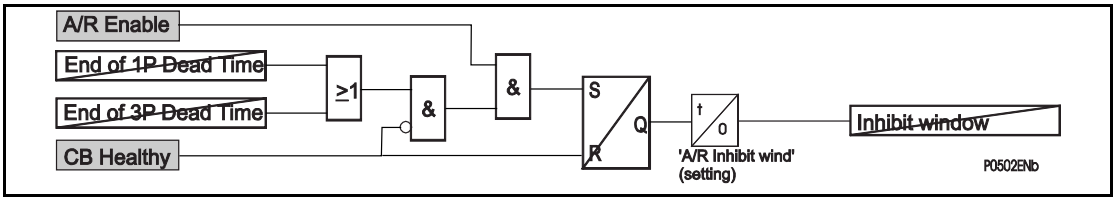


Figure 118: Autoreclose inhibit window logic

The inhibit time-delay is started at the end of dead time if CB healthy is absent

5.9.1.2 Check synchronism on 3-pole reclosure

The Check synchronism on 3-pole reclosure ('**C/S on 3P Rcl DT1**') setting is used to "Enable/Disable" system checks for the first reclose after a 3 pole trip in an autoreclose cycle. When the "SysChk on Shot 1" is set to "Disabled", no system checks are required for the first reclose which may be preferred when high speed autoreclose is applied to avoid the extra time for a system check. Subsequent reclose attempts in a multi-shot cycle will still require a system check.

5.9.1.3 Block autoreclose

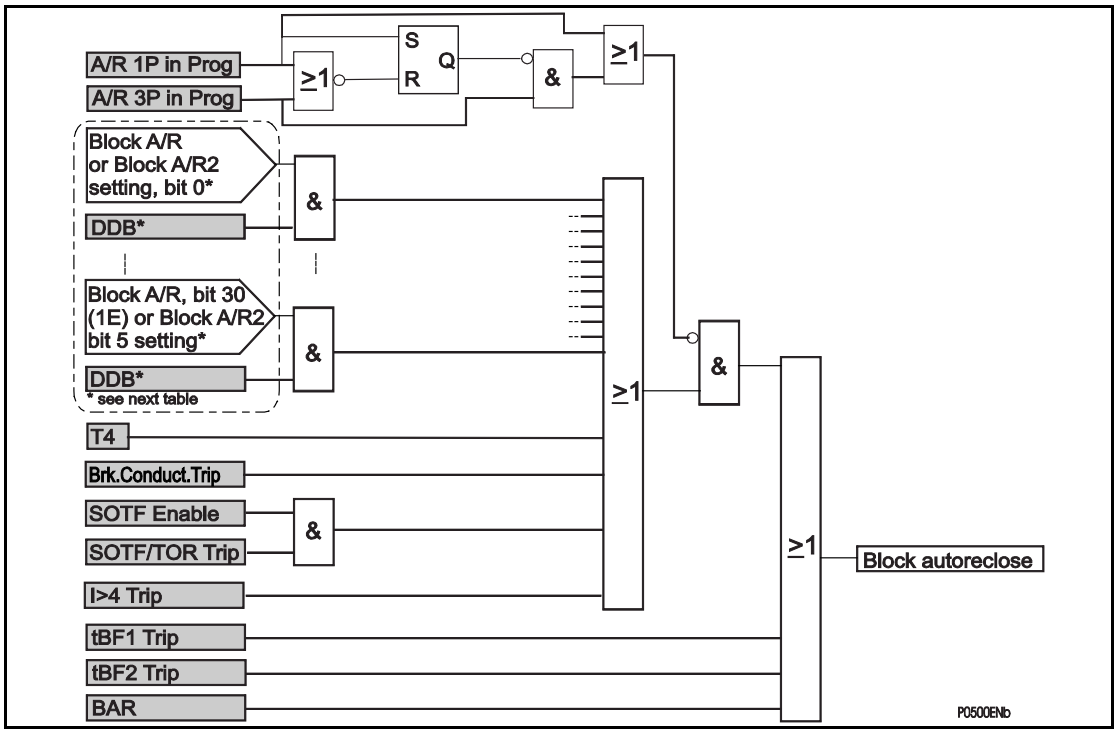
When enabled (the relevant bit is set to 1), the detected fault will block the autoreclose, and cause a lockout if autoreclose is in progress. If a single-pole is in progress, a three-pole trip will be issued and the autorecloser will lock-out.

It can be set when protection operation is required without autoreclose. A typical example is for a transformer feeder, where autoreclosing may be initiated by the feeder's protection relay but blocked by the transformer's protection relay. Similarly, where a circuit breaker low gas pressure or loss of vacuum alarm occurs during the dead time, autoreclosure should be blocked – and '**Block A/R**' can be used to perform this blocking logic.

Autoreclose logic is partly fixed, so that autoreclosure is always blocked for any Switch on to Fault, Stub Bus Protection, Broken Conductor or Zone 4 trip. Autoreclosure is also blocked when relay Supervision functions detect a Circuit Breaker Failure or Voltage Transformer/Fuse Failure. All other protection trips initiate autoreclosure (when blocking bit is set to 0).

When autoreclosure is not required for multiphase faults, DDB signals '**2Ph Fault**' and '**3Ph Fault**' can be mapped via the PSL in a logic OR combination onto input DDB: '**BAR**' (Block internal AutoReclose, section 5.9.1.5). When blocking is only required for a three phase fault, the DDB signal '**3Ph Fault**' is mapped to '**BAR**' alone. Three phase faults are more likely to be persistent, so many utilities may not wish to initiate autoreclose in such instances.

The next diagram shows the block autoreclose logic.



bit	setting	DDB
Autoreclose lockout / Block A/R		
00	At T2	T2
01	At T3	T3
02	At Tzp	tZp
03	LoL Trip	Loss. Load Trip
04	I>1 Trip	I>1 Trip
05	I>2 Trip	I>2 Trip
06	V<1 Trip	V<1 Trip
07	V<2 Trip	V<2 Trip
08	V>1 Trip	V>1 Trip
09	V>2 trip	V>2 Trip
0A	IN>1 Trip	IN>1 Trip
0B	IN>2 Trip	IN>2 Trip
0C	Aided D.E.F Trip	DEF Trip A C OR DEF Trip B OR DEF Trip C
0D	Zero. Seq. Power Trip	ZSP Trip
0E	IN>3 Trip	IN>3 Trip
0F	IN>4 Trip	IN>4 Trip
10	PAP Trip	PAP Trip A OR PAP Trip B OR PAP Trip C

bit	setting	DDB
11	Thermal Trip	Trip Thermal
12	I2>1 Trip	I2> Trip
13	I2>2 Trip	I2>2 Trip
14	I2>3 Trip	I2>3 Trip
15	I2>4 Trip	I2>4 Trip
16	VN>1 Trip	VN>1 Trip
17	VN>2 Trip	VN>2 Trip
18	At Tzq	tZq
19	V<3 Trip	V<3 Trip
1A	V<4 Trip	V<4 Trip
1B	V>3 Trip	V>3 Trip
1C	V>4 trip	V>4 trip
1D	I<1 Trip	I<1 Block
1E	I<2 Trip	I<2 Block
Autoreclose lockout / Block A/R 2		
00	F<1 Trip	F<1 Trip
01	F<2 Trip	F<2 Trip
02	F<3 Trip	F<3 Trip
03	F<4 Trip	F<4 Trip
05	F>2 Trip	F>2 Trip

Figure 119: Block autoreclose logic

- When “autoreclose Lockout / Block A/R” is enabled, the autoreclose does not initiate any additional A/R cycle. If the autorecloser locks out during a cycle, ‘**A/R close**’ is blocked.
- A dedicated PSL can be created for performing an autoreclose lockout in case of confirmed Fuse Failure.

5.9.1.4 Autoreclose force Sync

The DDB: ‘**A/R Force Sync**’ forces synchronism check to be made.

It simulates the check synchronisation control and forces the logical DDB output '**CheckSync OK**' at 1 during a 1 pole or 3 poles high speed AR cycle.

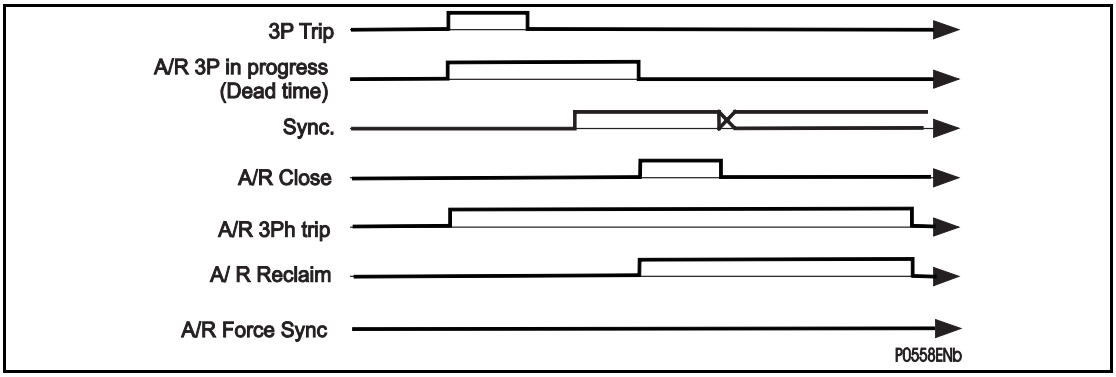


Figure 120: No pick-up at the end of the dead time

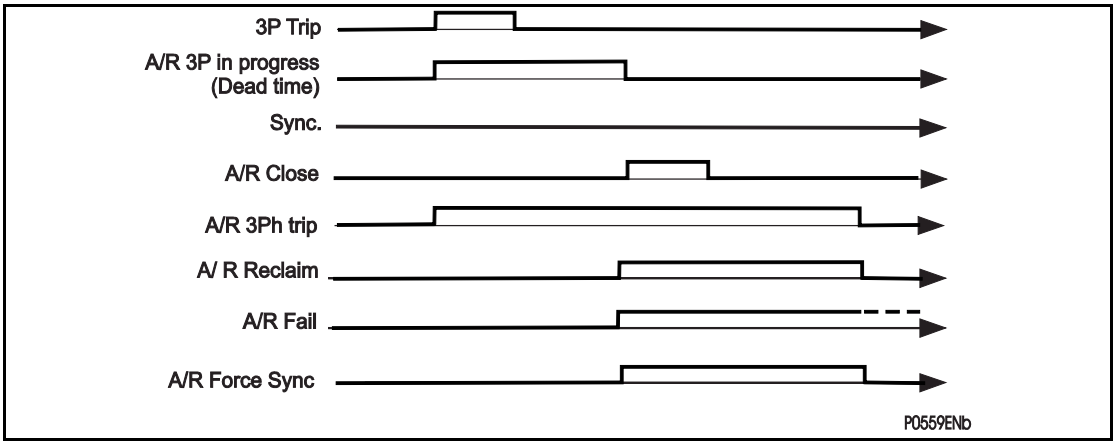


Figure 121: Check sync signal will be forced at the end of dead time

5.9.1.5 CB Discrepancy

The DDB: ‘**CB Discrepancy**’ signal informs the protection of a pole discrepancy status (one pole opened and the other two poles closed). It must be set to high logical level before Dead time 1 has elapsed – it can also be generated internally (see Cbaux logic).

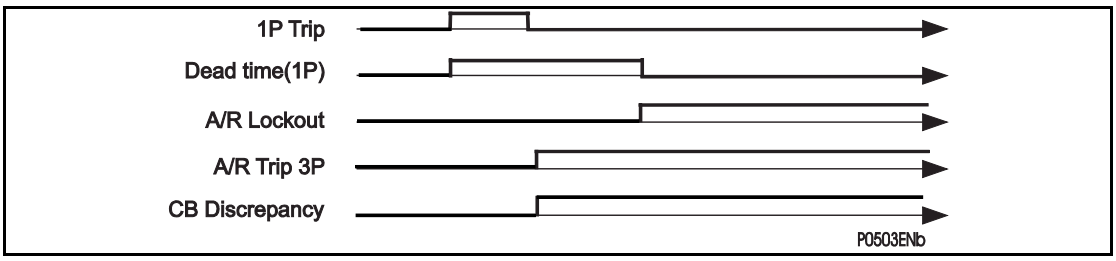


Figure 122: Pole discrepancy (CBA-Disc)

5.9.2 Logic Inputs / outputs used by the Autoreclose logic

5.9.2.1 Logic inputs used by the Autoreclose logic

Contacts from external equipment (External protection or external Check Synchronism or external Autoreclose) may be used to influence the autorecloser via opto-isolated inputs. Such functions can be allocated to any of the opto-isolated inputs on the relay via the programmable scheme logic (Ensure that *optos1&2 are not set for setting group change*- Otherwise, these opto inputs cannot be mapped to functions in the PSL. The inputs can be selected to accept either a normally open or a normally closed contact, programmable via the PSL editor (see section P44x/EN PL for complete description).

- A/R SPAR Enable (the opto input must be be energised for over 1.2 s),
- A/R TPAR Enable (the opto input must be energised for over 1.2 s),



Note: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the "A/R enable" logic sate).

- A/R Internal
- I A/R 1p In Prog (internal autoreclose single-pole in progress)
- I A/R 3p In Pr. (internal autoreclose three-pole in progress)
- I A/R Close (Circuit Breaker closing order from external autoreclose)
- I A/R Reclaim (Autoreclose in reclaim)
- BAR (Block internal Autoreclose)
- Ext Chk Synch OK (external check synchronisation OK),
- Force 3P trip
- Man. Close CB (circuit breaker manual close)
- Man. Trip CB (circuit breaker manual trip),
- CB Discrepancy
- External Trip A, External Trip B and External Trip C

5.9.2.2 Logic outputs generated by the Autoreclose logic

The following DDB signals can be masked to a relay contact in the PSL or assigned to a Monitor Bit in **Commissioning Tests**, to provide information about the autoreclose cycle status. They are described below, and identified by their DDB signal label (see section P44x/EN PL for complete description).

- A/R 1P In Prog,
- A/R 234 in Prog,
- A/R Close,
- A/R Enable,
- A/R Fail,
- A/R first in Prog.,
- A/R Force Sync,
- A/R Lockout,
- A/R Reclaim,
- A/R SPAR Enable,
- A/R TPAR Enable,
- A/R Trip 3 P,
- AR 3P In Prog.,

- AR Discrim,
- AR Lockout Shot>,
- Check Sync;OK
- Control Close
- Control Trip
- Ctrl Cls In Prog
- Ext Chk Synch OK,
- V<Dead Bus
- V<Dead Line
- V>Live Bus
- V>Live Line

5.9.2.3 Logic diagrams

Autoreclose activation:

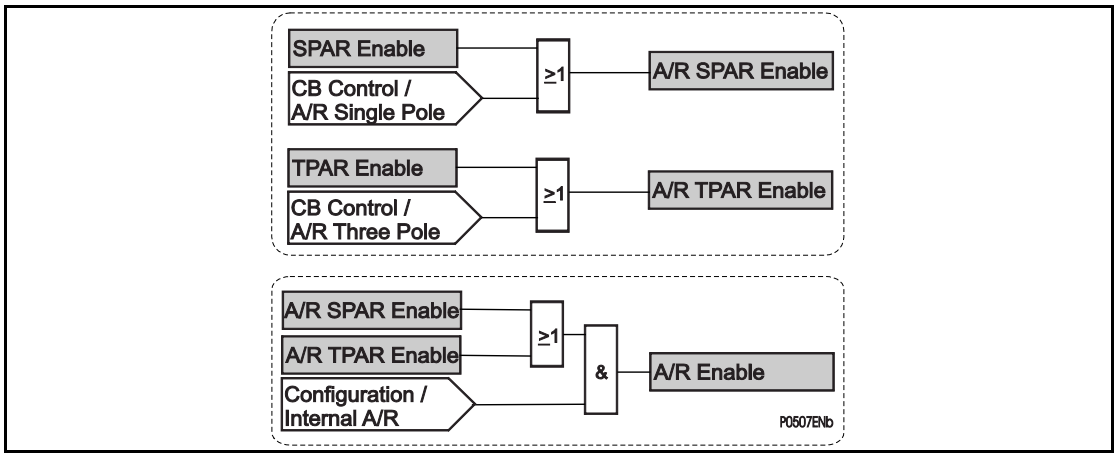


Figure 123: SPAR, TPAR and AR activation

The next diagram illustrates the logic for **A/R close**, **A/R fail** and **A/R Force Sync**. Note that A/R fail is reset with 3 poles closed:

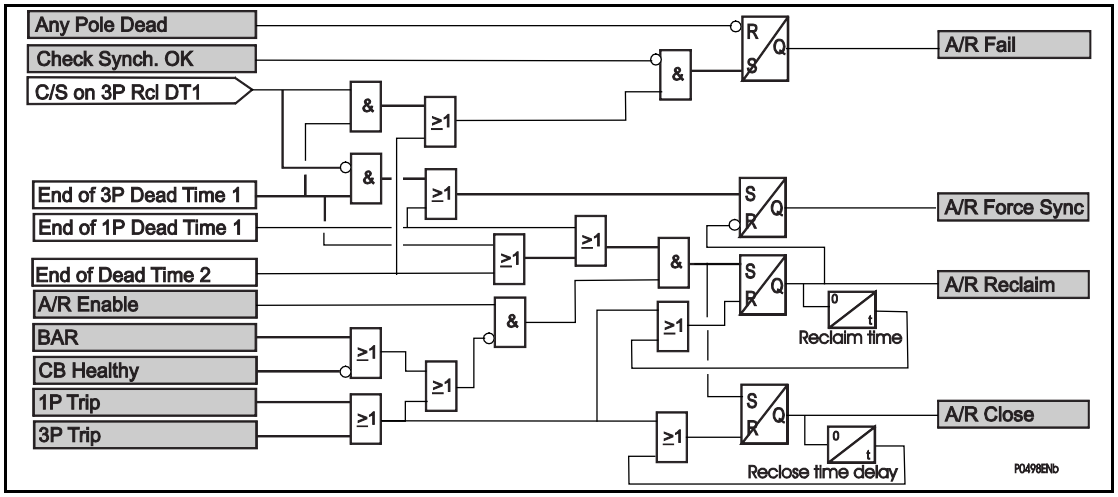


Figure 124: Logic for reclaim time /A/R close / A/R fail and A/R force sync

Forces the Check Sync conditions to the high logic level – used for SPAR or TPAR with SYNC AR3 fast (Enabled using setting) – The signal is reset with AR reclaim

In the next diagram, **A/R lockout** logic picks up by

- block autoreclose logic (**BAR**)
- or **A/R lockout Shots>**
- or Inhibit window logic
- or no pole discrepancy detected at the end of dead time1
- or trip command still present at the end of Dead time
- or Trip3P issued during 1P cycle after Discrimination Timer
- or Trip3P issued during 1P cycle with no 3PAR enabled.

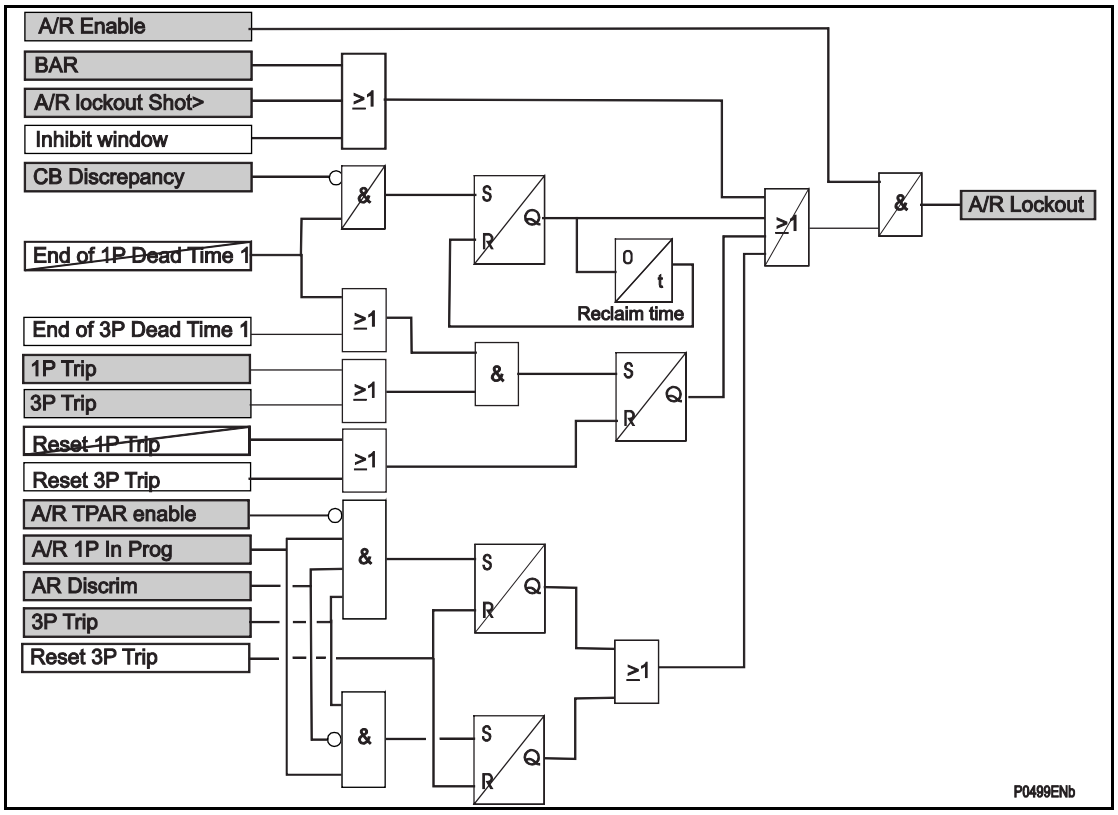


Figure 125: Internal logic of AR lockout

The next diagram illustrates AR Lockout Shots> logic:

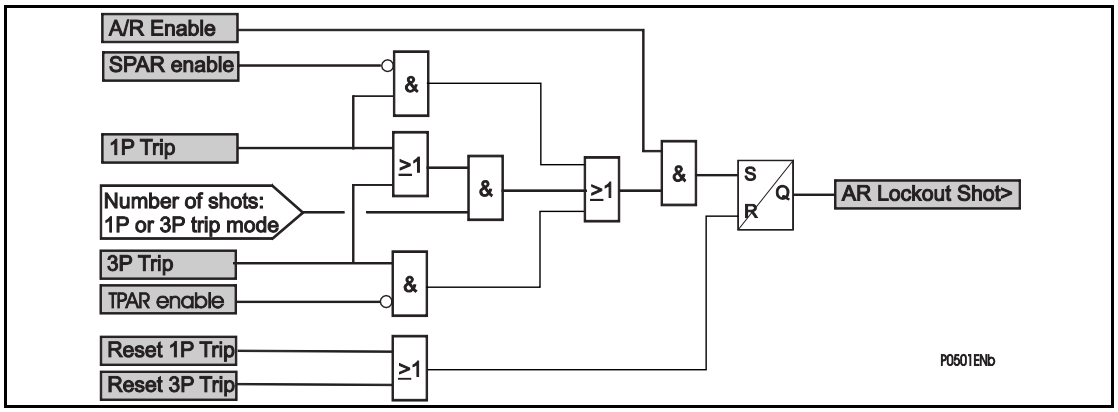


Figure 126: AR lockout by number of shots

The CB healthy logic is used as a negative logic (due to an inverter in the scheme – see Figure 118 inhibit window logic) but the DDB considers CB healthy as a positive logic [1=opto input energised during inhwind (setting) =AR close pulse]

One-pole autoreclose cycle in progress (**A/R 1P in Prog**) and **AR discrimination** (discrimination time-delay window in progress, starts with the trip command) logic:

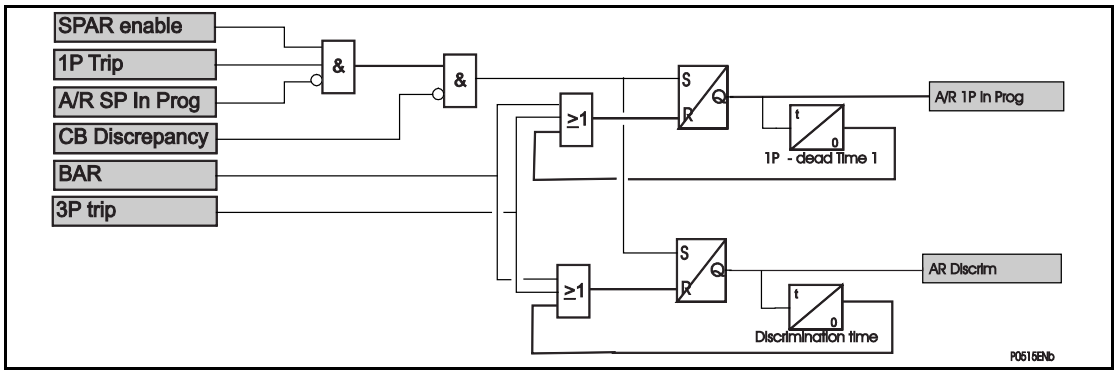
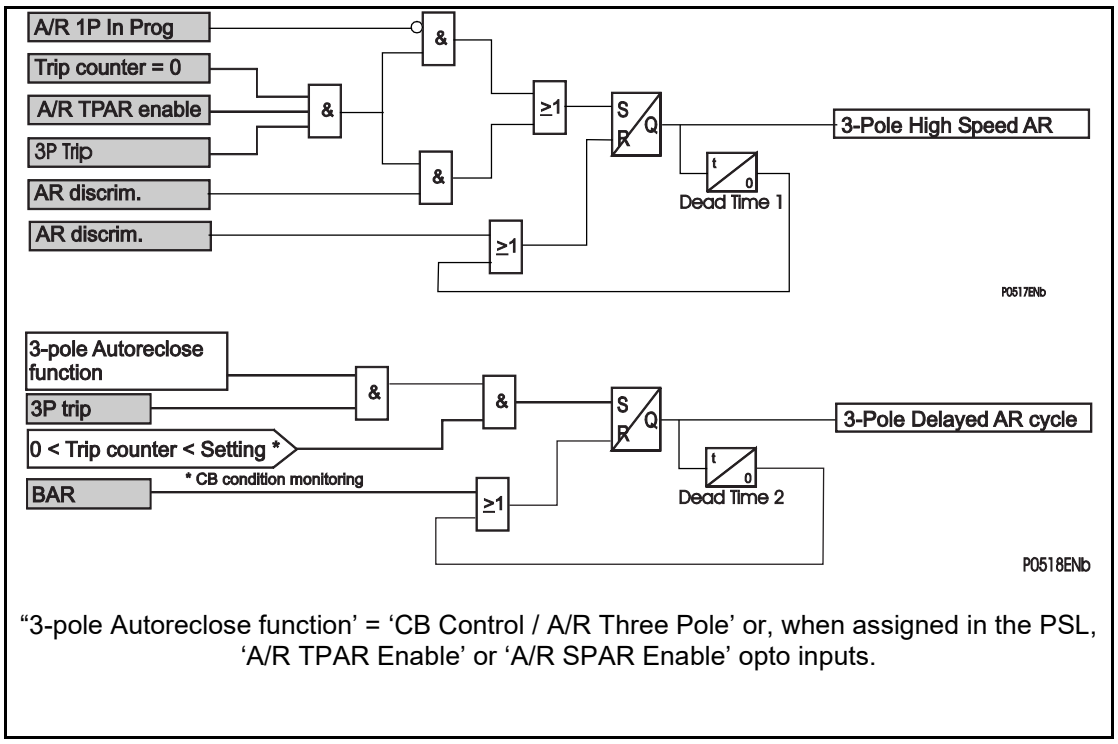


Figure 127: A/R 1 pole in progress and A/R discrim logic



"3-pole Autoreclose function' = 'CB Control / A/R Three Pole' or, when assigned in the PSL, 'A/R TPAR Enable' or 'A/R SPAR Enable' opto inputs.

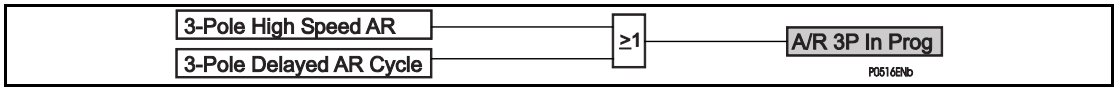


Figure 128: 3-Pole AR in progress

Where single-pole tripping is enabled, a fixed logic converts single-phase trips for faults on autoreclosure to three-pole trips:

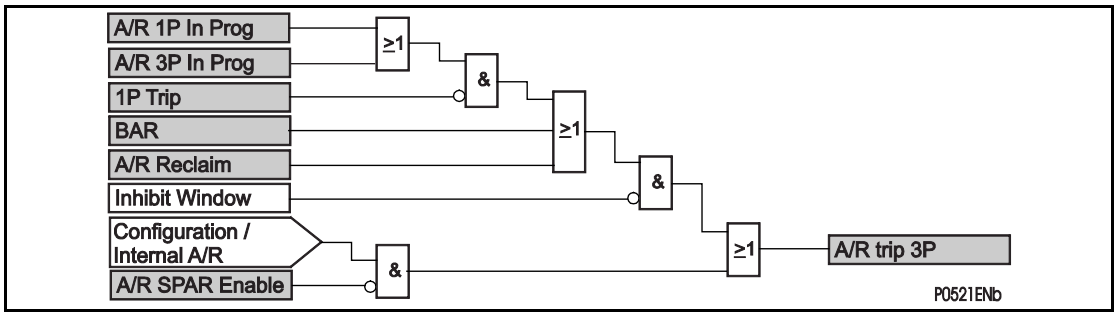


Figure 129: AR logic for 3p trip decision

Further autoreclose cycles (cycles 2, 3 and 4) in progress (**AR 234 In Prog**) logic:

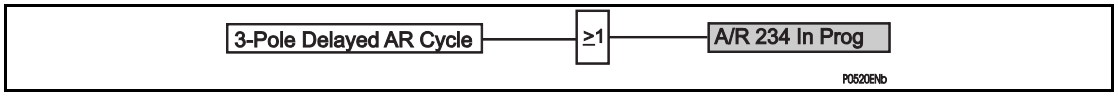


Figure 130: Output dealayed autoreclose (for dead time 2, 3, 4)

If it is assigned to an opto input in the PSL and energised, The DDB: '**Force 3P Trip**' signal will force the internal single-phase protection to trip three-poles. (external order from Main1 to Main2 (P44x)) – the next trip will be three-pole.

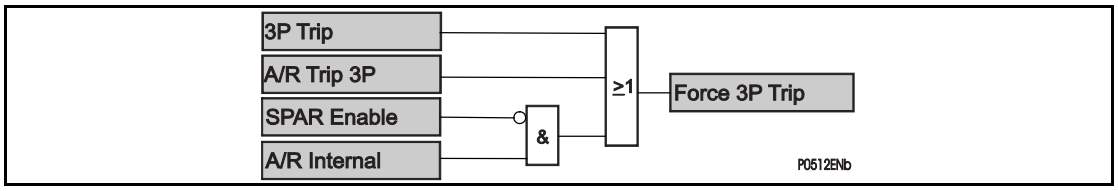


Figure 131: Force 3P trip logic

5.10 Circuit breaker state monitoring

An operator at a remote location requires a reliable indication of the state of the switchgear. Without an indication that each circuit breaker is either open or closed, the operator has insufficient information to decide on switching operations. The relay incorporates circuit breaker state monitoring, giving an indication of the position of the circuit breaker, or, if the state is unknown, an alarm is raised.

The Circuit Breaker state can be locally displayed in the "**System data / Plant status**" menu.

5.10.1 Circuit Breaker State Monitoring Features

MiCOM relays can be set to monitor normally open (52a) and normally closed (52b) auxiliary contacts of the circuit breaker. Under healthy conditions, these contacts will be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts / wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

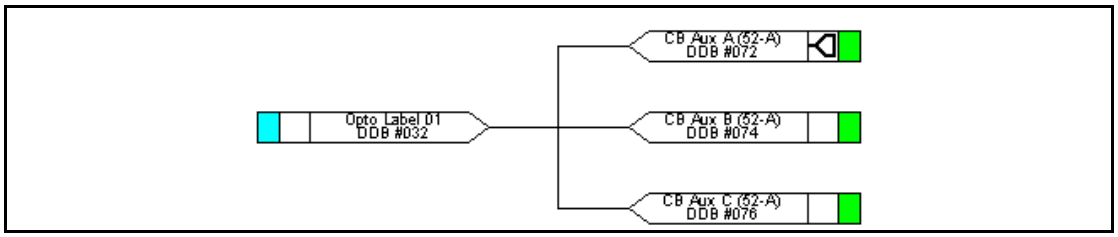
- Auxiliary contacts / wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5s time delay. A normally open / normally closed output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

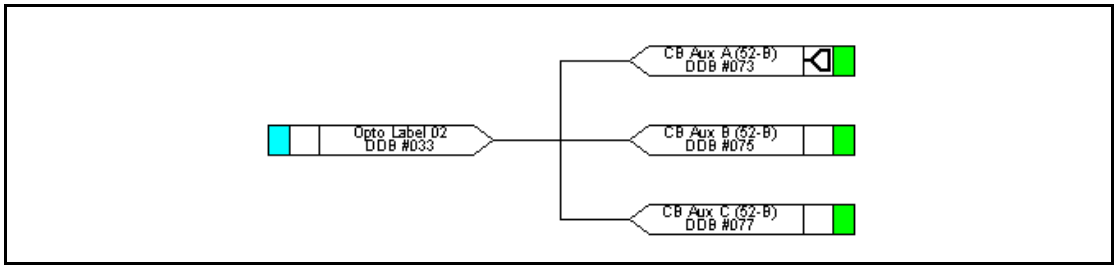
In the PSL, CB AUX can be used or not, according to the four options below:

- None
- 52A (1 or 3 opto inputs for a single pole logic)
- 52B (1 or 3 opto inputs)
- Both 52A and 52B (2 opto inputs or 6 opto inputs)

Sol1: One opto input used for 52a (3-pole circuit breaker)



Sol2: One opto input used for 52b (3-pole circuit breaker)



Sol3: Two opto inputs used for 52a & 52b (3-pole circuit breaker)

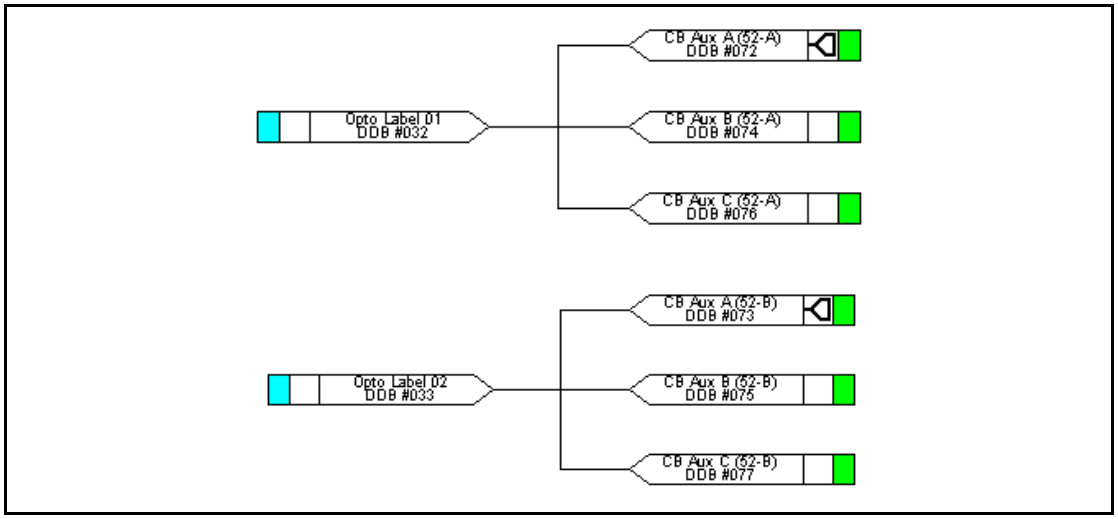
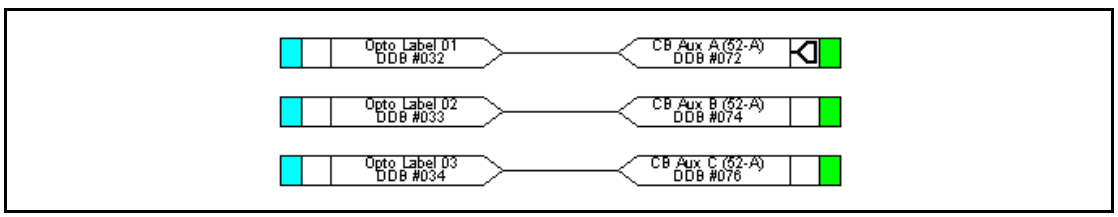
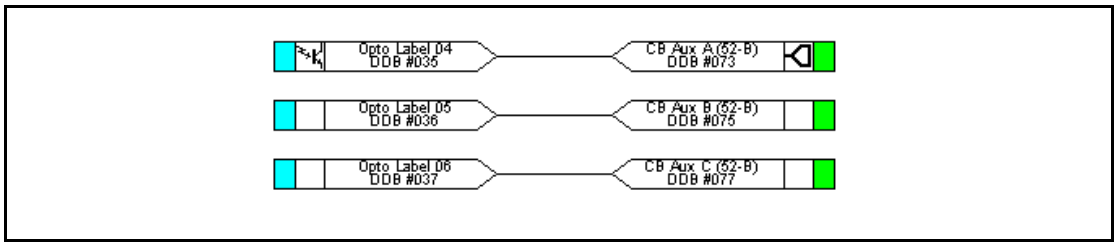


Figure 132: Different opto inputs / CB aux schemes

Sol4: Three opto inputs used for 52a (1-pole circuit breaker)



Sol5: Three opto inputs used for 52b (1-pole circuit breaker)



Sol6: Six opto inputs used for 52a &52b (1-pole cicuit breaker)

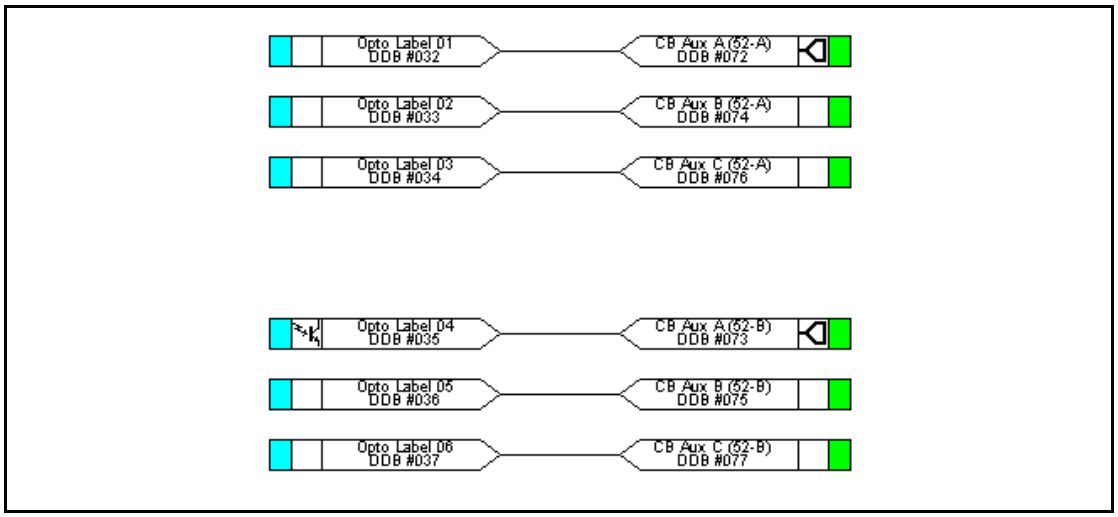


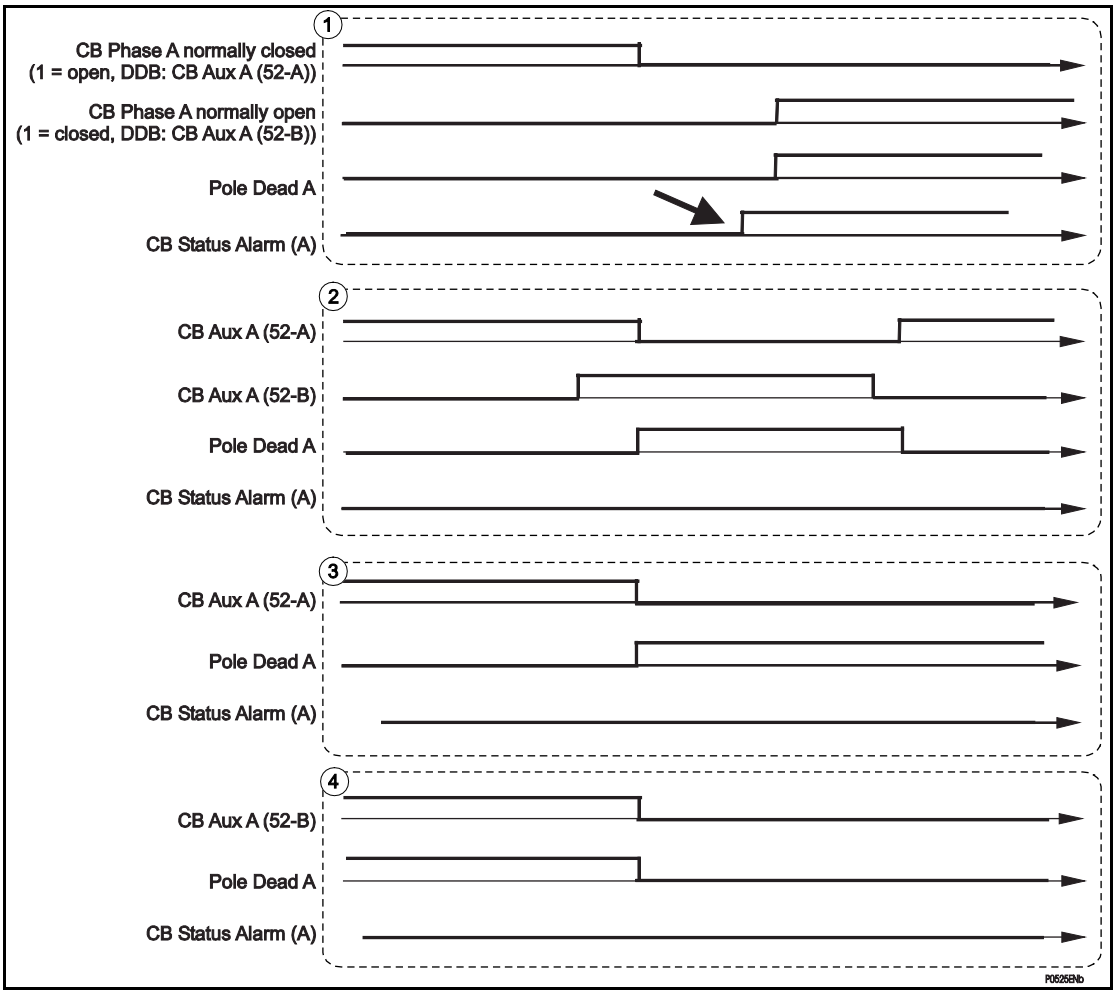
Figure 133: Different opto inputs / CB aux schemes (cont'd)

Where 'None' is selected no CB status will be available. This will directly affect any function within the relay that requires this signal, for example CB control, auto-reclose, etc. Where only 52a is used on its own then the relay will assume a 52b signal from the absence of the 52a signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52b is used. If both 52a and 52b are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table. 52a and 52b inputs are assigned to relay opto-isolated inputs via the PSL.

Auxiliary Contact Position		CB State Detected	Action
52a	52b		
Open	Closed	Breaker Open	Circuit breaker healthy
Closed	Open	Breaker Closed	Circuit breaker healthy
Closed	Closed	CB Failure	Alarm raised if the condition persists for greater than 5s
Open	Open	State Unknown	Alarm raised if the condition persists for greater than 5s

Where single pole tripping is used (available on P442 and P444) then an open breaker condition will only be given if all three phases indicate and open condition. Similarly for a closed breaker condition indication that all three phases are closed must be given. For single pole tripping applications 52a-A, 52a-B and 52a-C and/or 52b-A, 52b-B and 52b-C inputs should be used.

With 52a and 52b both present, the relay stores in memory the last valid state of the 2 inputs (52a=/52b). If no valid state is present (52a=52b) on expiry of the Alarm time-delay (value=150ms), the CB Status Alarm is issued.



1 – Coherence of 52-A/52-B long enough to raise the alarm
2 – Discrepancy of 52-A/52-B too brief to raise the alarm
3 – Pole dead logic With one opto input 52A
3 – Pole dead logic With one opto input 52A

Figure 134: Circuit breaker state monitoring

5.10.2 DDB Inputs / outputs for CB logic

5.10.2.1 Inputs

- External TripA
- External TripB
- External TripC

From External Protection Devices (via opto inputs) - see General trip logic.

If these optos inputs are assigned to **External Trip A**, **External Trip B** and **External Trip C** – their change of state will update the CB Operation counter (External trip is integrated in the DDB: '**Any Trip**'. As for an internal trip, no Dwell timer is associated.

- CB aux A(52a)
- CB aux B(52a)
- CB aux C(52a)
- CB aux A(52b)
- CB aux B(52b)
- CB aux C(52b)

If it is assigned to an opto input in the PSL and energised, the DDB: '**CB Aux**' signal will be used for Any pole dead & All pole dead internal logic & Discrepancy logic.

- CB Discrepancy: Used for internal CBA Disc issued by external (opto input) or internal detection (CB Aux)

5.10.2.2 Outputs

- CB Status Alarm

Picks up when CB Discrepancy status is detected after CBA timer issued externally by opto or internally by CB Aux

- CB aux A
- CB aux B
- CB aux C

Pole A+B+C detected Dead pole by the internal logic or CB status

- Any Pole Dead

If it is assigned in the PSL, the DDB: '**Any Pole Dead**' signal indicates that one or more poles are open.

- All Pole Dead

If it is assigned in the PSL, The DDB: '**All Pole Dead**' signal indicates that all poles are dead (all 3 poles are open).

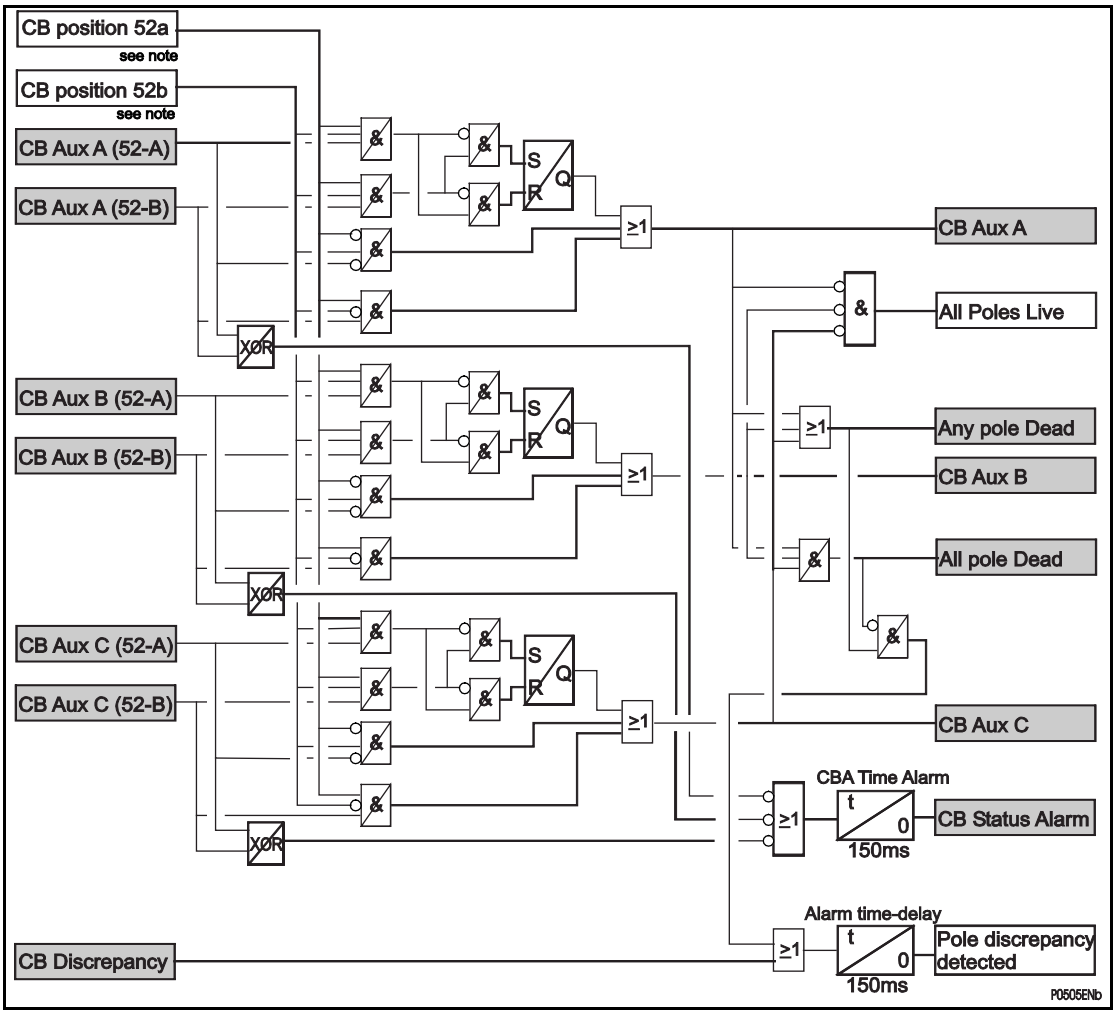


Figure 135: Logic CBAUX scheme

CBA time disc=150msec fixed value

Dead Pole Logic:

- CBA_A = Pole A Dead

- CBA_3P = All pole Dead
- CBA_3P_C = All poles Live
- ‘Any Pole Dead’= Minimum 1 Pole dead

The total number of autoreclosures is shown in the “CB Condition” LCD menu under **Total Reclosures**. Separate counters for single pole and three pole reclosures are available. The counters can be reset to zero with the **Reset Total A/R** command (HMI).

PROGRAMMABLE LOGIC

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1 PROGRAMMABLE LOGIC (PSL)

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised internal logic. This is done by combining the IED's digital inputs with internally generated digital signals using logic gates and timers, then mapping the resultant signals to the IED's digital outputs and LEDs.

The Programmable Scheme Logic (PSL) Editor allows you to create and edit scheme logic diagrams to suit your own particular application.

Further information is available in the Help system and in the Settings Application Software Guide P40-M&CR-UG-EN-n, where n is the latest version of the settings application software.

1.1 Description of P442 and P444 Logic Nodes

1.1.1 Sorted by DDB number

Ordinal	English Text	Description	Source
0 to 63	Relay Label 01 to Relay Label 64	OUTPUT RELAY 1 to OUTPUT RELAY 64 High level when a DDB cell (linked by PSL logic) is at 1. State depends on the logic set in the PSL (MiCOM S1 Agile) These programmable relays are assigned in the default PSL, with the following logic conditions (see section 1.8.2): - Pulse time-delay - Pick Up/Drop Off Time-delay - Dwell Time-delay - Pick Up Time-delay - Drop Off Time-delay - Latching - Straight (used in default PSL)	RELAY
64	Opto Label 01	OPTO ISOLATOR 1 Set to 1 when the opto input is energised for a minimum time: 7 ms (48 Vdc), 10 ms (universal) to be validated by internal logic To enable the selection of a setting group by state change of the opto isolated logic inputs 1 and 2, disconnect Opto inputs 01 and 02 in the PSL (Opto inputs 01 and 02 must not be connected to any output signal)	OPTO
65	Opto Label 02	OPTO ISOLATOR 2 Set to 1 when the opto input is energised for a minimum time: 7 ms (48 Vdc), 10 ms (universal) to be validated by internal logic To enable the selection of a setting group by state change of the opto isolated logic inputs 1 and 2, disconnect Opto inputs 01 and 02 in the PSL (Opto inputs 01 and 02 must not be connected to any output signal)	OPTO
66 to 95	Opto Label 03 to Opto Label 32	OPTO ISOLATOR 3 to OPTO ISOLATOR 32 Set to 1 when the opto input is energised for a minimum time:7 ms (48 Vdc), 10 ms (universal) to be validated by internal logic	OPTO
96 to 173	--	Unused	
174	General Alarm	Groupment of all alarms	PSL (OUT)
175	Prot'n Disabled	Protection is disabled and test mode enabled	PSL (OUT)
176	F out of Range	Frequency tracking does not work correctly (provides a Frequency Out-of-Range indication)	PSL (OUT)
177	VT Fail Alarm	Fuse failure indication (VT alarm). High when the opto input is energised (copy of MCB) OR an internal Fuse Failure is confirmed when the VTS timer elapses.	PSL (OUT) VT Supervision

Ordinal	English Text	Description	Source
178	CT Fail Alarm	Current transformers supervision indication: Indicates a CT Fail detected after time delay has elapsed is issued	PSL (OUT) CT Supervision
179	CB Fail Alarm	Circuit breaker failure on any trip	PSL (OUT) Breaker Fail
180	I^ Maint Alarm	Broken current maintenance alarm (1st level): An alarm maintenance is issued when the maximum broken current (1st level) calculated by the CB monitoring function is reached (see setting: 'CB monitor setup / I^ Maintenance')	PSL (OUT) CB monitoring
181	I^ Lockout Alarm	Broken current lockout alarm (2nd level): An alarm Lock Out is issued when the maximum broken current (2nd level) calculated by the monitoring function is reached	PSL (OUT) CB monitoring
182	CB Ops Maint	Circuit breaker operations number alarm (1st level): An alarm is issued when the maximum of CB operations is reached. This alarm is initiated by internal (any protection function) or external trip (via opto input). The Alarm can be set with 'CB Monitor Setup / N° CB Ops Maint.' setting. Set to 0: Until number of operations is below the 'N° CB 0ps Maint.' setting. The DDB:'Reset all values' resets this counter.	PSL (OUT) CB monitoring
183	CB Ops Lockout	Circuit breaker operation number lockout (2nd level alarm): An alarm is issued when the maximum of CB operations is reached [initiated by internal or external trip, see setting: 'CB Monitor Setup\N° CB Ops Lockt.] Set to 0: Until number of operations is below the 'N° CB Ops Lockt." setting. The DDB:'Reset all values' resets this counter.	PSL (OUT) CB monitoring
184	CB Op Time Maint	CB excessive operating time alarm: An alarm is issued when the operating tripping time on any phase pass over the 'CB monitor setup / CB Time Maint' setting (slowest pole detection calculated by I< from CB Fail logic)	PSL (OUT) CB monitoring
185	CB Op Time Lock	CB locked out, due to excessive operating time: An alarm is issued when the operating tripping time on any phase pass over the 'CB monitor setup / CB Time Lockout' setting (slowest pole detection calculated by I< from CB Fail logic)	PSL (OUT) CB monitoring
186	F.F. Pre Lockout	Excessive Fault Frequency CB Trip lockout Alarm (maximum number of fault): An alarm is issued at (n-1) value in the counters of Main lock out or Fault frequency	PSL (OUT) CB monitoring
187	F.F. Lock	Excessive Fault Frequency CB Trip pre lockout Alarm (maximum number of fault): An alarm is issued at (n) value in the counters of Main lock out or Fault frequency	PSL (OUT) CB monitoring
188	Lockout Alarm	Lockout alarm: An alarm is issued with: 'Man CB Unhealthy'or no 'Check Sync OK' (CB conditioning) or 'Man CB Cls Fail' or 'Man CB Fail Trip' or 'F.F. Lock' or 'CB Op Time Lock' or 'CB Ops Lockout'	PSL (OUT)
189	CB Status Alarm	Circuit Breaker Alarm Displayed when a CB Failure or CB State unknown condition is detected (the 'System data / Plant Status' two last digits = 00 or 11). The CB discrepancy status is detected after CBA time-delay issued by opto input or internally by CBAux logic – Alarm issued after 5 s	PSL (OUT)
190	Man CB Trip Fail	Alarm CB Fail for manual trip command	PSL (OUT)
191	Man CB Cls Fail	Alarm CB fail for manual closing command	PSL (OUT)
192	Man CB Unhealthy	Alarm CB performed by unhealthy condition	PSL (OUT)
193	Control No C/S	Autoreclosed works without check synchronism (high when the internal Check Synchronism conditions are not met).	PSL (OUT)

Ordinal	English Text	Description	Source
194	AR Lockout Shot>	Autoreclose lockout following final programmed attempt: Indicates a failed autoreclose (definitive trip following the last reclosing shot). The relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition has been reset. An alarm, "AR Lockout Shots>" (along with AR Lockout) will be raised. 1 = 'A/R Enable' & [('1Ptrip & No 'SPAR Enable') + (3P Trip & No 'TPAR enable) + ('1P Trip' + '3P Trip') & (Number of shots=setting)]	PSL (OUT) Autorecloser
195	SG-opto Invalid	Setting group (selected via opto inputs 1 & 2) invalid	PSL (OUT)
196	A/R Fail	No check sync / autorecloser failed: If the check sync conditions are not met prior to reclosing within the time window, the 'A/R Fail' alarm will be raised.	PSL (OUT) Autorecloser
197	V<1 Alarm	1st stage undervoltage alarm picks up when V<1 starts	PSL (OUT) V<1
198	V<2 Alarm	2nd stage undervoltage alarm picks up when V<21 starts	PSL (OUT) V<2
199	V>1 Alarm	1st stage overvoltage alarm picks up when V>1 starts	PSL (OUT) V>1
200	V>2 Alarm	2nd stage overvoltage alarm picks up when V>2 starts	PSL (OUT) V>2
201	COS Alarm	HF carrier anomaly alarm (Carrier out of service)	PSL(OUT) Unblocking logic
202	Brok. Cond. Alarm	Broken Conductor Alarm	PSL(OUT) Broken conductor
203	CVT Alarm	Alarm for capacitive voltage Transformer: Indicates the residual voltage is greater than the threshold adjusted in the settings, during a time-delay greater than the adjustment. That alarm is also included in the general alarm.	PSL (OUT)
204	NCIT Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) IEC 61850 9-2 Alarm - Frame from Merge Units missing. If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL (OUT)
205	Val/Fail Acq Al.	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x Alarm NCIT (9-2 Ethernet) - Frame from Merge Units failed. Any Logical Node is synchronized with Internal (local) synchronization	PSL (OUT)
205	--	Unused (software version D5.x)	
206	Test Mode Acq	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x - Any Logical Node is in “Test Mode”	PSL (OUT)
206	--	Unused (software version D5.x)	
207	Synchro Acq Al.	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x - Any Logical Node is synchronized with external (global) synchronization	PSL (OUT)
207	--	Unused (software version D5.x)	
208	alarm user 1	Alarm user for dedicated PSL	PSL(IN)
209	alarm user 2	Alarm user for dedicated PSL	PSL(IN)
210	alarm user 3	Alarm user for dedicated PSL	PSL(IN)
211	alarm user 4	Alarm user for dedicated PSL	PSL(IN)
212	alarm user 5	Alarm user for dedicated PSL	PSL(IN)

Ordinal	English Text	Description	Source
213	V3< Alarm	Third undervoltage stage Alarm	PSL(IN)
214	V4< Alarm	Fourth undervoltage stage Alarm	PSL(IN)
215	V3> Alarm	Third overvoltage stage Alarm	PSL(IN)
216	V4> Alarm	Fourth overvoltage stage Alarm	PSL(IN)
217 to 222	--	Unused	
223	A/R Close	Autorecloser Close command to CB: Initiates the reclose command pulse to the circuit breaker. This output feeds a signal to the Reclose time-delay, which maintains the linked reclose contact closed for a time sufficient to ensure reliable CB mechanism operation. This DDB signal may also be useful during relay commissioning to check the operation of the autoreclose cycle. Where three single pole circuit breakers are used, the AR Close contact will need to energise the closing circuits for all three breaker poles (or alternatively assign three CB Close contacts).	PSL (OUT) Autorecloser
224	A/R 1P In Prog	One-pole autoreclose cycle in progress: A single pole autoreclose cycle is in progress. This output will remain activated from the initial protection trip until the circuit breaker is closed successfully or the autoreclose function is Locked Out, indicating that a dead time timeout is in progress. This signal may be useful during relay commissioning to check the operation of the autoreclose cycle.	PSL (OUT) Autorecloser
225	A/R 3P In Prog	Three-pole autoreclose cycle in progress: A three phase autoreclose cycle is in progress. This output will remain activated from the initial protection trip until the circuit breaker is closed successfully or the AR function is Locked Out, indicating that a dead time timeout is in progress. This signal may be useful during relay commissioning to check the operation of the autoreclose cycle.	PSL (OUT) Autorecloser
226	A/R 1st In Prog	First high speed autoreclose cycle in progress: Used to indicate the autorecloser is timing out its first dead time, either a high-speed single-pole shot or a high speed three-pole shot.	PSL (OUT) Autorecloser
227	A/R 234 In Prog	Further autoreclose cycles in progress: Used to indicate the autorecloser is timing out delayed autoreclose dead times for shots 2, 3 or 4. Where some protection elements should not initiate autoreclosure for Delayed Autoreclose (DAR) shots, the protection element operation is combined with 'A/R 234 in Prog' as a logic AND operation in the Programmable Scheme Logic, and then set to assert the DDB:'BAR' input, forcing lockout.	PSL (OUT) Autorecloser
228	A/R Trip 3P	Autorecloser signal to force all trips to be 3 Ph: This is an internal logic signal used to condition any protection trip command to the circuit breaker(s). Where single-pole tripping is enabled, a fixed logic converts single-phase trips for faults on autoreclosure to three-pole trips. A/R Trip 3P can be connected to Main2 as an external "Force 3-pole" 1 = ('Internal A/R' setting enabled) AND (No 'A/R SPAR Enable') 0 = 'A/R SPAR Enable' AND ('Internal A/R' setting enabled)+ ('Inhibit Window' at 0)	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
229	A/R Reclaim	Internal autoreclose reclaim in progress (reclaim time timeout in progress). If it is assigned to an opto input in the PSL and when energised, the DDB:‘A/R Reclaim’ signal will start the internal logic TOR enable (External AR logic applied). The DDB indicates the reclaim time following a particular autoreclose shot is timing out. The DDB:'AR Reclaim' output would be energised at the same instant as any Cycle outputs are reset. ‘A/R Reclaim’ may be used to block low-set instantaneous protection on autoreclosure, when it has not been time-graded with a downstream protection. This technique is commonly used when the downstream devices are fuses, and fuse saving is implemented. This avoids fuse blowing for transient faults. ‘A/R reclaim’ can be connected to Main2 for cycle in progress external information. It initiates the internal TOR logic	PSL (OUT) Autorecloser
230	AR Discrim.	'Discrimination time' window in progress (starts with the trip command). When a single pole trip is issued by the relay, a 1-pole AR cycle is initiated. The 'Dead time 1' and 'Discrimination time' are started. If the autoreclose logic detects a single pole or three-pole trip (internal or external) during the discrimination time-delay, the single pole high speed autoreclose cycle is disabled and replaced by a three pole high speed autoreclose cycle, if enabled. If no three-pole autoreclose is enabled, the relay trips 3-pole and the autoreclose is blocked. If the autoreclose logic detects a 3-pole trip (internal or external) when the Discrimination time-delay has elapsed and during the 1-pole dead time; the single pole AR cycle is stopped and the relay trips 3-pole and blocks the autoreclose.	PSL (OUT) Autorecloser
231	A/R Enable	Indicates the autoreclose function is in service 1 = [If 'A/R SPAR Enable' OR 'A/R TPAR Enable'] AND "Internal A/R' = enabled (setting) Reset to 0: If 'A/R SPAR Enable'=0 AND 'A/R TPAR Enable'=0 (if assigned in PSL) + "Internal A/R' = disabled (setting)	PSL (OUT) Autorecloser
232	A/R SPAR Enable	Single pole autorecloser (SPAR) activated: If it is assigned to an opto input in the PSL (by default PSL is inverted and linked to opto 8) and energized, The DDB:'A/R SPAR Enable' will enable the 1-pole autoreclose logic (the priority of this input is higher than the 'CB Control/A/R single pole' setting) - this means the 1-pole autoreclose logic can be disabled even if it has been activated; if the relevant opto input is not energized (to be valid, the opto must be energised for over1.2s). NOTE: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the “A/R enable” logic state). Set to 1: 1P AR activated (copy of 'SPAR Enable' opto input OR 'CB Control/ A/R Single pole' enabled) Reset to 0: if 'SPAR Enable' = 0 OR (A/R Single pole' disabled)	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
233	A/R TPAR Enable	Three pole autorecloser (TPAR) activated: If it is assigned to an opto input in the PSL (by default, the PSL is inverted and linked to opto 8) and energized, the DDB:'A/R TPAR Enable' will enable the 3-pole autoreclose logic (the priority is higher than the 'CB Control / A/R three pole' setting) - this means the 3-pole autoreclose logic can be disabled even if it has been activated; if the relevant opto input is not energised (to be valid, the opto input must be energised for over 1.2s). NOTE: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the “AR enable” logic sate). Set to 1: 3P AR activated (copy of 'TPAR enable' opto input OR 'CB Control/ A/R Three pole' enabled) Reset to 0: if 'TPAR enable' = 0 OR ('A/R Three pole' disabled)	PSL (OUT) Autorecloser
234	A/R Lockout	Autorecloser locked-out (no autoreclosure possible until reset), If protection operates during the reclaim time, after the final reclose attempt, the relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition is reset. This will produce an alarm: A/R Lockout. Then, the DDB:'BAR' input will block the autorecloser and cause a lockout if a reclose cycle is in progress. Lockout will also occur if the CB energy is low and the CB fails to close. Once the autorecloser is locked out, it will not function until a Reset Lockout or CB Manual Close command is received (depending on the Reset Lockout method chosen in CB Monitor Setup). NOTE: Lockout can also be caused by the CB condition monitoring functions maintenance lockout, excessive fault frequency lockout, broken current lockout, CB failed to trip and CB failed to close, manual close no check synchronism and CB unhealthy. Set to 1 = 'A/R Enable' AND [('BAR' =1 (see internal logic) OR 'A/R lockout shot> (AR lockout by number of shots) OR (No CB Healthy at the end of Inhibit Window (setting)) OR (No 'CB discrepancy' (opto input or internal by CBAux if present in PSL) at the end of 1P Dead time1) OR Trip 1P or3P maintained / still present at the end of the1P or 3P Dead time) or after discrimination time-delay if a 3-pole trip occurs during a 1-Pole AR Cycle] At 0: AR activated Reset to 0 = ('Reset 1P Trip' OR 'Reset 3P Trip') AND (End of reclaim time) AND Reset (BAR) AND Reset (A/R lockout shot>) AND Reset (No CB Healthy) AND Reset (No Discrepancy)	PSL (OUT) Autorecloser
235	A/R Force Sync.	Force synchronism check to be made (simulate the CheckSync control and forces the DDB:'CheckSync OK' (logic output) to 1 during a 1-pole or 3-pole high speed autoreclose cycle) The signal is reset with A/R reclaim	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
236	Check Synch. OK	If linked to an opto input in a dedicated PSL and energised, it indicates that external synchronism conditions are met – This can be linked afterwards to an internal autoreclose logic	PSL (OUT) Synchro Check
237	V< Dead Line	Dead Line: high when the Dead Line condition is met (voltage below the 'V< Dead Line' threshold value (setting) – The measured voltage is always calculated as a single phase voltage	PSL (OUT) Synchro Check
238	V> Live Line	Live Line: high when the Live line condition is met (voltage above the 'V> Live Line' threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
239	V< Dead Bus	Dead Bus: high when the Dead Bus condition is met (voltage below the V<Dead Bus threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
240	V> Live Bus	Live Bus: high when the Live Bus condition is met (voltage above the V>Live Bus threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
241	Ctrl Cls In Prog	Manual (control) close in progress - using CB control (time-delay manual closing delay in progress).	PSL (OUT) CB Control
242	DIST Sig. Send	Distance protection schemes - Signal Send (default PSL: Relay 05)	PSL (OUT) Distance
243	DIST UNB CR	Unblock main channel received Internal Carrier Received signal (main Distance unblocking signal) received.	PSL(OUT) Unblocking Logic
244	DIST Fwd	Distance protection: Forward fault detected (default PSL: LED6) Set to 1: Directional Forward detected in distance algorithms (Deltas or Conventional) AND (Distance Start) Set to 0: With reset of Any Start/Dist Start	PSL (OUT) Distance
245	DIST Rev	Distance protection: Reverse fault detected (default PSL: LED7) Set to 1: Directional Reverse detected in distance algorithms (Deltas or Conventional) AND (Distance Start) Set to 0: With reset of Any Start/Dist Start	PSL (OUT) Distance
246	DIST Trip A	Distance protection: Phase A trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80 ms)	PSL (OUT) Distance
247	DIST Trip B	Distance protection: Phase B trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80 ms)	PSL (OUT) Distance
248	DIST Trip C	Distance protection: Phase C trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80 ms)	PSL (OUT) Distance
249	DIST Start A	Distance protection started on phase A Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
250	DIST Start B	Distance protection started on phase B Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10 ms requested)	PSL (OUT) Distance

Ordinal	English Text	Description	Source
251	DIST Start C	Distance protection started on phase C Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10 ms requested)	PSL (OUT) Distance
252	DIST Sch. Accel.	Distance scheme Accelerating	PSL (OUT) Distance
253	DIST Sch. Perm.	Distance scheme Permissive	PSL (OUT) Distance
254	DIST Sch. Block.	Distance scheme Blocking	PSL (OUT) Distance
255	Z1	Fault in zone 1 (convergence of loop in Z1) Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection (default PSL: LED 5, Relays 01 / 10)	PSL (OUT) Distance
256	Z1X	Fault in zone 1 extended Z1x (convergence of loop in Z1x) and filtered by blocking/unblocking Power Swing/Reversal guard logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
257	Z2	Fault in zone 2 (convergence of loop in Z2) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
258	Z3	Fault in zone 3 (convergence of loop in Z3) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
259	Z4	Fault in zone 4 (convergence of loop in Z4) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
260	Zp	Fault in zone P Zp (convergence of loop in Zp) logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
261	T1	Distance time-delay in zone 1 tZ1 elapsed (1 = end of timer) If T1=0 picks up when the relay starts (Distance Start or preset)	PSL (OUT) Distance
262	T2	Distance time-delay in zone 2 tZ2 elapsed (1 = end of timer)	PSL (OUT) Distance
263	T3	Distance time-delay in zone 3 tZ3elapsed (1 = end of timer)	PSL (OUT) Distance
264	T4	Distance time-delay in zone 4 tZ4 elapsed (1 = end of timer)	PSL (OUT) Distance
265	Tzp	Distance time-delay in zone p tZp elapsed (1 = end of timer)	PSL (OUT) Distance
266	WI Trip A	Phase A trip on weak infeed	PSL (OUT) Distance
267	WI Trip B	Phase B trip on weak infeed	PSL (OUT) Distance
268	WI Trip C	Phase C trip on weak infeed	PSL (OUT) Distance
269	Power Swing	Power swing detected (3 single phase loop inside the quad & crossing the ΔR band in less than 5ms in a 50 Hz network). Power swing is present either with out of step cycle or stable swing cycle.	PSL (OUT) Distance
270	Reversal Guard	Current reversal guard logic in action (Directional switching from Rev to Fwd in parallel line application)	PSL (OUT) Distance

Ordinal	English Text	Description	Source
271	DEF Sig. Send	DEF protection schemes - Signal Send (Default PSL: Relay 05)	PSL (OUT) Aided DEF
272	DEF UNB CR	Unblocking DEF channel internal Carrier Received signal (main Directional Earth Fault unblocking signal) received.	PSL (OUT) Unblocking logic
273	DEF Rev	Channel Aided DEF: reverse fault	PSL (OUT) Aided DEF
274	DEF Fwd	Channel Aided DEF: forward fault	PSL (OUT) Aided DEF
275	DEF Start A	Channel Aided DEF: start phase A	PSL (OUT) Aided DEF
276	DEF Start B	Channel Aided DEF: start phase B	PSL (OUT) Aided DEF
277	DEF Start C	Channel Aided DEF: start phase C	PSL (OUT) Aided DEF
278	DEF Trip A	Channel Aided DEF: trip phase A Default PSL: Relay 09	PSL (OUT) Aided DEF
279	DEF Trip B	Channel Aided DEF: trip phase B Default PSL: Relay 09	PSL (OUT) Aided DEF
280	DEF Trip C	Channel Aided DEF: trip phase C Default PSL: Relay 09	PSL (OUT) Aided DEF
281	IN>1 Trip	Earth fault stage 1 trip – 3-pole trip command issued when the associated time-delay has elapsed	PSL (OUT) Earth Fault 1
282	IN>2 Trip	Earth fault stage 2 trip – 3-pole trip command issued when the associated time-delay has elapsed Default PSL: Relay 09.	PSL (OUT) Earth Fault 2
283	IN>1 Start	Earth fault stage 1 start – Start function (the associated time-delay picks up) Directional or not - with DT or IDMT curves Negative or positive sequence polarization Set to 0: Reset with IN below the threshold IN>1 Hysteresis	PSL (OUT) Earth Fault 1
284	IN>2 Start	Earth fault stage 2 start – Start function (the associated time-delay picks up) Directional or not - with DT or IDMT curves Negative or positive sequence polarization Set to 0: Reset with IN below the threshold IN>2 Hysteresis	PSL (OUT) Earth Fault 2
285	V< Start Any A	Any undervoltage start detected on phase A	PSL (OUT) Undervoltage
286	V< Start Any B	Any undervoltage start detected on phase B	PSL (OUT) Undervoltage
287	V< Start Any C	Any undervoltage start detected on phase C	PSL (OUT) Undervoltage
288	V<1 Start	Undervoltage 1st stage start (any phase)	PSL (OUT) Undervoltage
289	V<2 Start	Undervoltage 2nd stage start (any phase)	PSL (OUT) Undervoltage
290	V<1 Trip	Undervoltage 1st stage – 3-phase trip	PSL (OUT) Undervoltage
291	V<2 Trip	Undervoltage stage 2nd stage – 3-phase trip	PSL (OUT) Undervoltage
292	V> Start Any A	Any overvoltage start detected on phase A	PSl (OUT) Overvoltage
293	V> Start Any B	Any overvoltage start detected on phase B	PSl (OUT) Overvoltage
294	V> Start Any C	Any overvoltage start detected on phase C	PSl (OUT) Overvoltage

Ordinal	English Text	Description	Source
295	V>1 Start	Overvoltage function 1st stage start for any phase	PSI (OUT) Overvoltage
296	V>2 Start	Overvoltage function 2nd stage start for any phase	PSI (OUT) Overvoltage
297	V>1 Trip	Overvoltage 1st stage 3-phase trip	PSI (OUT) Overvoltage
298	V>2 Trip	Overvoltage 2nd stage 3-phase 2 trip	PSI (OUT) Overvoltage
299	I2> Start	Negative Sequence Current Detection – Start function (the associated time-delay picks up) Directional or not - with DT curves Negative-sequence polarization	PSL (OUT) Neg Seq. O/C
300	I2> Trip	Negative Sequence Current Trip – 3P trip command issued when the associated time-delay has elapsed	PSL (OUT) Neg Seq. O/C
301	I> Start Any A	Any overcurrent start for phase A	PSL (OUT) Phase Overc.
302	I> Start Any B	Any overcurrent start for phase B	PSL (OUT) Phase Overc.
303	I> Start Any C	Any overcurrent start for phase C	PSL (OUT) Phase Overc.
304	I>1 Start	Overcurrent stage 1 start Directional or not - with DT or IDMT curves Directional managed by Delta Algorithms VTS Block time-delay facility	PSL (OUT) Phase Overc.
305	I>2 Start	Overcurrent stage 2 start Directional or not - with DT or IDMT curves Directional managed by Delta Algorithms VTS Block time-delay facility	PSL (OUT) Phase Overc.
306	I>3 Start	Overcurrent stage 3 start Non-directional with DT curves Use without time-delay for SOTF	PSL (OUT) Phase Overc.
307	I>4 Start	Overcurrent stage 4 start Non-directional with DT curves Use without time-delay for SOTF	PSL (OUT) Phase Overc.
308	I>1 Trip	Overcurrent stage 1 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>1 Trip command	PSL (OUT) Phase Overc.
309	I>2 Trip	Overcurrent stage 2 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>2 Trip command	PSL (OUT) Phase Overc.
310	I>3 Trip	Overcurrent stage 3 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>3 Trip command	PSL (OUT) Phase Overc.
311	I>4 Trip	Overcurrent stage 4 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>4 Trip command	PSL (OUT) Phase Overc.
312	SOTF Enable	Switch On To Fault enabled: Indicates the SOTF logic is enabled in the relay Set to 1 = [SOTF not disabled (Setting 'Distance schemes / TOR-SOTF Mode')] AND [{ All poles dead AND (SOTF time-delay elapsed (110 s/default)) } OR Input Man Close] OR (CB control & Close in progress)] Reset = 500 ms time-delay elapsed after Any pole Dead OR Reset of one condition requested for SOTF enable	PSL (OUT) SOTF

Ordinal	English Text	Description	Source
313	TOR Enable	Trip On Reclose enable: indicates the TOR logic is activated in the relay Set to 1= 500 ms pulse initiated by: 'I A/R Reclaim' (internal) OR 'A/R reclaim' (External Input) OR Any pole open for more than 200 ms Reset 500 ms after Any pole dead stops	PSL (OUT) TOR
314	TOC Start A	Trip on Close start on phase A: indicates a trip order on phase A has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
315	TOC Start B	Trip on Close start on phase B: indicates a trip order on phase B has been issued by the SOTF level detectors (Pickup time-delay = 20ms)	PSL (OUT) SOTF
316	TOC Start C	Trip on Close start on phase C: indicates a trip order on phase C has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
317	Any start	Any protection start logic with any phase Default PSL: LED 4, Relay 06 (Fault record trigger in default PSL with 20 ms Dwell Timer)	PSL (OUT) All protection
318	1ph Fault	Single phase fault	PSL (OUT) Distance
319	2ph Fault	Two phase fault	PSL (OUT) Distance
320	3ph Fault	Three phase fault	PSL (OUT) Distance
321	Any Trip	Single or three pole trip or external protection trip Default PSL: Relay 07	PSL (OUT) All protection
322	Any Int. Trip A	Any internal protection A phase trip Default PSL: LED 1, Relay 02	PSL (OUT) All protection
323	Any Int. Trip B	Any internal protection B phase trip Default PSL: LED 2, Relay 03	PSL (OUT) All protection
324	Any Int. Trip C	Any internal protection C phase trip Default PSL: LED 3, Relay 04	PSL (OUT) All protection
325	Any Trip A	Any trip A (internal or external protection)	PSL (OUT) All protection
326	Any Trip B	Any trip B (internal or external protection)	PSL (OUT) All protection
327	Any Trip C	Any trip C (internal or external protection)	PSL (OUT) All protection
328	1P Trip	Single pole trip (internal or external)	PSL (OUT) All protection
329	3P Trip	Three pole trip (internal or external)	PSL (OUT) All protection
330	Brk.Conduct.Trip	Broken conductor trip	PSL (OUT) Broken Cond.
331	Loss. Load Trip	Loss of load trip (in application without communication scheme and a 3P Trip logic)	PSL (OUT) Loss of load
332	SOTF/TOR Trip	Switch on to fault trip or trip on reclose: indicates that a 3-pole trip order has been issued by the TOR or SOTF logic	PSL (OUT) SOTF
333	tBF1 Trip	Circuit Breaker failure on any trip, delayed by "CB Fail 1 Timer" (setting in "CB Fail" logic)	PSL (OUT) Breaker failure
334	tBF2 Trip	Circuit Breaker failure on any trip, delayed by "CB Fail 2 Timer" (setting in "CB Fail" logic)	PSL (OUT) Breaker failure
335	Control Trip	Control trip command from user (by internal CB control)	PSL (OUT) CB control

Ordinal	English Text	Description	Source
336	Control Close	Control close command from user (by internal CB control)	PSL (OUT) CB control
337	VTS Fast	Instantaneous unconfirmed fuse failure internal detection. Set high for internal Fuse Failure detection made with internal logic.	PSL (OUT) VTS
338	CB Aux A	CB Phase A status (from internal logic and CBAux opto inputs state: 1 = CB-Pole A is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
339	CB Aux B	CB Phase B status (from internal logic and CBAux opto inputs state: 1 = CB-Pole B is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
340	CB Aux C	CB Phase C status (from internal logic and CBAux opto inputs state: 1 = CB-Pole C is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
341	Any Pole Dead	Any circuit breaker pole dead (one or more poles open, pole status detected by CBaux or internal thresholds). If it is linked in the PSL, the DDB:'Any Pole Dead' signal indicates that one or more poles are open. Any Pole Dead = Pole Dead A OR Pole Dead B OR Pole Dead C	PSL (OUT) Poledead
342	All Pole Dead	All circuit breaker poles dead (breaker open 3 phase, pole status detected by Cbaux or internal thresholds). If it is linked in the PSL, the DDB:'All Pole Dead' signal indicates that all poles are dead (3 poles are open). All Pole Dead = Pole Dead A AND Pole Dead B AND Pole Dead C	PSL (OUT) Poledead
343	DIST Fwd No Filt	Distance protection: Forward fault detected not filtered (Directional Forward decision made by Distance logic without any filter by Distance Start or Zone: Picks up faster than Dist Fwd)	PSL (OUT) Distance
344	DIST Rev No Filt	Distance protection: Reverse fault detected not filtered (Directional Forward decision made by Distance logic without any filter by Distance Start or Zone: Picks up faster than Dist Fwd)	PSL (OUT) Distance
345	DIST Convergency	Distance protection: Internal characteristic Set to 1: logic with Distance Start at 1 (Minimum 1 loop has been detected in the quadrilateral characteristic) Set to 0: Reset of (R, X) (resistance, reactance) calculation made by the All pole Dead detection	PSL (OUT) Distance
346	Cross Count. Flt	Cross Country Fault Set to 1: The cross country logic is activated (1 Fault Fwd/1 Fault Rev detected)	PSL (OUT) Distance
347	ZSP Start	Zero Sequence Power - Start: The ZSP START cell at 1 indicates the Zero Sequence Power function has started - in the same time, it indicates the timer-delays associated have started and are running (fixed one first and then IDMT timer)	PSL (OUT) ZSP
348	ZSP Trip	Zero Sequence Power - Trip: The ZSP TRIP cell at 1 indicates the Zero Sequence Power function has performed a trip command (after the start and when associated timers are issued)	PSL (OUT) ZSP
349	Z1 Not Filtrated	Z1 decision not filtered by phase selection	PSL (OUT)
350	Out Of Step	Start of an Out of Step Detection (1st cycle), The first out of step cycle has been detected (Zlocus in/out with the opposite R sign) & the « Out Of Step start » picks-up	PSL (OUT)
351	S. Swing	Start of Stable Swing (1st cycle): The first stable swing cycle has been detected (Zlocus in/out with the same R sign) & the « Stable Swing start » picks-up	PSL (OUT)

Ordinal	English Text	Description	Source
352	Out Of Step Conf	Out of Step Confirmed (number of cycles reached)	PSL (OUT)
353	S. Swing Conf	Stable Swing confirmed (number of cycles reached)	PSL (OUT)
354	Dist Start N	Start of distance protection for phase to ground fault	PSL (OUT)
355	IN>3 Trip	Trip decision from IN>3 function (timer issued) Default PSL: Relay 09	PSL (OUT)
356	IN>4 Trip	Trip decision from IN>4 function (timer issued)	PSL (OUT)
357	IN>3 Start	Start of IN>3 function (timer initiated)	PSL (OUT)
358	IN>4 Start	Start of IN>4 function (timer initiated)	PSL (OUT)
359	PAP Trip A	Trip A Phase decision from PAP (specific application) function	PSL (OUT)
360	PAP Trip B	Trip B Phase decision from PAP (specific application) function	PSL (OUT)
361	PAP Trip C	Trip C Phase decision from PAP (specific application) function	PSL (OUT)
362	PAP Trip IN	Trip decision from PAP (specific application) function (Ground Fault detected)	PSL (OUT)
363	PAP Start A	Phase A Start with PAP (specific application) function	PSL (OUT)
364	PAP Start B	Phase B Start with PAP (specific application) function	PSL (OUT)
365	PAP Start C	Phase C Start with PAP (specific application) function	PSL (OUT)
366	PAP Pres IN	Residual current detected by PAP (specific application) function	PSL (OUT)
367	PAP Pre Start	PAP (specific application) Picks up by voltage detectors (timer initiated)	PSL (OUT)
368	Trace Trig OK	Triggering trace has operated correctly	PSL (OUT)
369	Thermal Alarm	Alarm from Thermal Overload function picks up	PSL (OUT)
370	Trip Thermal	Trip with Thermal Overload fucntion (timer issued)	PSL (OUT)
371	V<1 Start A	Undervoltage stage 1 pick up on phase A	PSL
372	V<1 Start B	Undervoltage stage 1 pick up on phase B	PSL
373	V<1 Start C	Undervoltage stage 1 pick up on phase C	PSL
374	V<2 Start A	Undervoltage stage 2 pick up on phase A	PSL
375	V<2 Start B	Undervoltage stage 2 pick up on phase B	PSL
376	V<2 Start C	Undervoltage stage 2 pick up on phase C	PSL
377	V>1 Start A	Overvoltage stage 1 pick up on phase A	PSL
378	V>1 Start B	Overvoltage stage 1 pick up on phase B	PSL
379	V>1 Start C	Overvoltage stage 1 pick up on phase C	PSL
380	V>2 Start A	Overvoltage stage 2 pick up on phase A	PSL
381	V>2 Start B	Overvoltage stage 2 pick up on phase B	PSL
382	V>2 Start C	Overvoltage stage 2 pick up on phase C	PSL
383	I2>2 Start	Negative overcurrent stage 2 pick-up	PSL
384	I2>3 Start	Negative overcurrent stage 3 pick-up	PSL
385	I2>4 Start	Negative overcurrent stage 4 pick-up	PSL
386	I2>2 Trip	Negative overcurrent stage 2 trip	PSL
387	I2>3 Trip	Negative overcurrent stage 3 trip	PSL
388	I2>4 Trip	Negative overcurrent stage 4 trip	PSL
389	VN>1 Start	Neutral overvoltage stage 1 pick up	PSL
390	VN>2 Start	Neutral overvoltage stage 2 pick up	PSL
391	VN>1 Trip	Neutral overvoltage stage 1 trip	PSL
392	VN>2 Trip	Neutral overvoltage stage 2 trip	PSL
393	Any Int. Trip	Any Internal trip	PSL
394	Zq	Fault in zone Q	PSL
395	Tzq	Timer in zone Q elapsed (at 1 = end of timer)	PSL

Ordinal	English Text	Description	Source
396	V<3 Start	Undervoltage stage 3 start	PSL
397	V<4 Start	Undervoltage stage 4 start	PSL
398	V<3 Start A	Undervoltage phase A stage 3 start	PSL
399	V<3 Start B	Undervoltage phase B stage 3 start	PSL
400	V<3 Start C	Undervoltage phase C stage 3 start	PSL
401	V<4 Start A	Undervoltage phase A stage 4 start	PSL
402	V<4 Start B	Undervoltage phase B stage 4 start	PSL
403	V<4 Start C	Undervoltage phase C stage 4 start	PSL
404	V<3 Trip	Undervoltage stage 3 trip	PSL
405	V<4 Trip	Undervoltage stage 4 trip	PSL
406	V>3 Start	Overvoltage stage 3 start	PSL
407	V>4 Start	Overvoltage stage 4 start	PSL
408	V>3 Start A	Overvoltage phase A stage 3 start	PSL
409	V>3 Start B	Overvoltage phase B stage 3 start	PSL
410	V>3 Start C	Overvoltage phase C stage 3 start	PSL
411	V>4 Start A	Overvoltage phase A stage 4 start	PSL
412	V>4 Start B	Overvoltage phase B stage 4 start	PSL
413	V>4 Start C	Overvoltage phase C stage 4 start	PSL
414	V>3 Trip	Overvoltage stage 3 trip	PSL
415	V>4 Trip	Overvoltage stage 4 trip	PSL
416	F<1 Start	Underfrequency stage 1 start	PSL
417	F<2 Start	Underfrequency stage 2 start	PSL
418	F<3 Start	Underfrequency stage 3 start	PSL
419	F<4 Start	Underfrequency stage 4 start	PSL
420	F>1 Start	Overfrequency stage 1 start	PSL
421	F>2 Start	Overfrequency stage 2 start	PSL
422	F<1 Trip	Underfrequency stage 1 trip	PSL
423	F<2 Trip	Underfrequency stage 2 trip	PSL
424	F<3 Trip	Underfrequency stage 3 trip	PSL
425	F<4 Trip	Underfrequency stage 4 trip	PSL
426	F>1 Trip	Overfrequency stage 1 trip	PSL
427	F>2 Trip	Overfrequency stage 2 trip	PSL
428	F Inhib	Frequency Inhibition	PSL
429	I<1 Start	Undercurrent stage 1 start	PSL
430	I<2 Start	Undercurrent stage 2 start	PSL
431	I<1 Trip	Undercurrent stage 1 trip	PSL
432	I<2 Trip	Undercurrent stage 1 trip	PSL
433	SBO Open Org 1	Select Before Operate (SBO) opening function for organ 1 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
434	SBO Open Org 2	Select Before Operate (SBO) opening function for organ 2 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
435	SBO Open Org 3	Select Before Operate (SBO) opening function for organ 3 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
436	SBO Open Org 4	Select Before Operate (SBO) opening function for organ 4 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
437	SBO Closed Org 1	Select Before Operate (SBO) closing function for organ 1 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
438	SBO Closed Org 2	Select Before Operate (SBO) closing function for organ 2 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
439	SBO Closed Org 3	Select Before Operate (SBO) closing function for organ 3 (interlocking facility in the IEC 60870-5-103 protocol)	PSL

Ordinal	English Text	Description	Source
440	SBO Closed Org 4	Select Before Operate (SBO) closing function for organ 4 (interlocking facility in the IEC60870-5-103 protocol)	PSL
468	Fault_REC_TRIG	Trigger for Fault Recorder	FRT
469	Battery Fail	Alarm battery fail	PSL(OUT)
470	Field Volt Fail	Field voltage failure (the internal 48 Vdc delivered by the relay can be used for opto input polarisation)	PSL(OUT)
471	Comm2 H/W FAIL	Alarm second rear port	PSL(OUT)
472	GOOSE IED Absent	Absence of GOOSE message from dedicated IED	PSL(OUT)
473	NIC Not Fitted	Ethernet (board not fitted) alarm	PSL(OUT)
474	NIC No Response	No response from Ethernet Board alarm.	PSL(OUT)
475	NIC Fatal Error	Fatal Error from Ethernet Board alarm	PSL(OUT)
476	NIC Soft. Reload	Ethernet Board (Configuration in progress) alarm	PSL(OUT)
477	Bad TCP/IP Cfg.	Bad configuration TCP/IP Address alarm	PSL(OUT)
478	Bad OSI Config.	Ethernet alarm	PSL(OUT)
479	NIC Link Fail	Ethernet Link Fail alarm	PSL(OUT)
480	NIC SW Mis-Match	Not compatible Ethernet version alarm	PSL(OUT)
481	IP Addr Conflict	Ethernet IP Address Conflict alarm	PSL(OUT)
482	IM Loopback	InterMiCOM indication that loopback testing is in progress	PSL(OUT)
483	IM Message Fail	InterMiCOM message failure alarm	PSL(OUT)
484	IM Data CD Fail	InterMiCOM data channel detect fail	PSL(OUT)
485	IM Channel Fail	InterMiCOM message channel fail	PSL(OUT)
486	Back Up Setting	Back up setting alarm	PSL(OUT)
487 to 511	--	Unused	PSL
512	Virtual output 1	Goose output n° 1 - Allows user to control a binary signal which can be mapped via SCADA protocol output to other devices	PSL
513 to 543	Virtual output 2 Virtual output 32	Goose output n° 2 to Goose output n° 32	PSL
576	InterMiCOM in 1	InterMiCOM IM1 Signal Input - is driven by a message from the remote line end	SW
577 to 583	InterMiCOM in 2 to InterMiCOM in 8	InterMiCOM IM2 Signal Input to InterMiCOM IM8 Signal Input	SW
584	InterMiCOM out 1	InterMiCOM IM1 Signal output - mapping what will be sent to the remote line end	PSL
585 to 591	InterMiCOM out 2 to InterMiCOM out 8	InterMiCOM IM2 Signal output to InterMiCOM IM8 Signal output	PSL
592 to 607	--	Unused	PSL
608	Control input 1	Control Input 1 - for SCADA and menu commands into PSL	SW
609 to 639	Control input 2 to Control input 32	Control input 2 to Control input 32	SW
640	LED 1 Red	Hardware version K - Programmable Red LED n° 1 is energized. ANY TRIP A in the default PSL	SW
640	LED 1	Hardware version J - Programmable LED n° 1 is energized.	SW
641	LED 1 Grn	Hardware version K - Programmable Green LED n° 1 is energized ANY TRIP A in the default PSL	SW

Ordinal	English Text	Description	Source
641	LED 2	Hardware version J - Programmable LED n° 2 is energized.	SW
642	LED 2 Red	Hardware version K - Programmable Red LED n° 2 is energized ANY TRIP B in the default PSL	SW
642	LED 3	Hardware version J - Programmable LED n° 3 is energized.	SW
643	LED 2 Grn	Hardware version K - Programmable Green LED n° 2 is energized ANY TRIP B in the default PSL	SW
643	LED 4	Hardware version J - Programmable LED n° 4 is energized.	SW
644	LED 3 Red	Hardware version K - Programmable Red LED n° 3 ANY TRIP C in the default PSL	SW
644	LED 5	Hardware version J - Programmable LED n° 5 is energized.	SW
645	LED 3 Grn	Hardware version K - Programmable Green LED n° 3 ANY TRIP C in the default PSL	SW
645	LED 6	Hardware version J - Programmable LED n° 6 is energized.	SW
646	LED 4 Red	Hardware version K - Programmable Red LED n° 4 General Start in the default PSL	SW
646	LED 7	Hardware version J - Programmable LED n° 7 is energized.	SW
647	LED 4 Grn	Hardware version K - Programmable Green LED n° 4 General Start in the default PSL	SW
647	LED 8	Hardware version J - Programmable LED n° 8 is energized.	PSL
648	LED 5 Red	Hardware version K - Programmable Red LED n° 5 Z1+Aided Trip in the default PSL	SW
648 to 655	--	Hardware version J – Unused	
649	LED 5 Grn	Hardware version K - Programmable Green LED n° 5 Z1+Aided Trip in the default PSL	SW
650	LED 6 Red	Hardware version K - Programmable Red LED n° 6 Dist Fwd in the default PSL	SW
651	LED 6 Grn	Hardware version K - Programmable Green LED n° 6 Dist Fwd in the default PSL	SW
652	LED 7 Red	Hardware version K - Programmable Red LED n° 7 Dist Rev in the default PSL	SW
653	LED 7 Grn	Hardware version K - Programmable Green LED n° 7 Dist Rev in the default PSL	SW
654	LED 8 Red	Hardware version K - Programmable Red LED n° 8 Autoreclose Enable in the default PSL	SW
655	LED 8 Grn	Hardware version K - Programmable Green LED n° 8 Autoreclose Enable in the default PSL	SW
656	LED 9 Red	Hardware version K - Programmable Red LED n° 9	SW
656	LED Cond IN 1	Hardware version J - Assignment of signal to drive output Function Key LED 1	PSL
657	LED 9 Grn	Hardware version K - Programmable Green LED n° 9	SW
657	LED Cond IN 2	Hardware version J - Assignment of signal to drive output Function Key LED 2	PSL
658	LED 10 Red	Hardware version K - Programmable Red LED n° 10	SW
658	LED Cond IN 3	Hardware version J - Assignment of signal to drive output Function Key LED 3	PSL
659	LED 10 Grn	Hardware version K - Programmable Green LED n° 10	SW

Ordinal	English Text	Description	Source
659	LED Cond IN 4	Hardware version J - Assignment of signal to drive output Function Key LED 4	PSL
660	LED 11 Red	Hardware version K - Programmable Red LED n° 11	SW
660	LED Cond IN 5	Hardware version J - Assignment of signal to drive output Function Key LED 5	PSL
661	LED 11 Grn	Hardware version K - Programmable Green LED n° 11	SW
661	LED Cond IN 6	Hardware version J - Assignment of signal to drive output Function Key LED 6	PSL
662	LED 12 Red	Hardware version K - Programmable Red LED n° 12	SW
662	LED Cond IN 7	Hardware version J - Assignment of signal to drive output Function Key LED 6	PSL
663	LED 12 Grn	Hardware version K - Programmable Green LED n° 12	SW
663	LED Cond IN 8	Hardware version J - Assignment of signal to drive output Function Key LED 7	PSL
664	LED 13 Red	Hardware version K - Programmable Red LED n° 13	SW
664 to 685	--	Hardware version J – Unused	
665	LED 13 Grn	Hardware version K - Programmable Green LED n° 13	SW
666	LED 14 Red	Hardware version K - Programmable Red LED n° 14	SW
667	LED 14 Grn	Hardware version K - Programmable Green LED n° 14	SW
668	LED 15 Red	Hardware version K - Programmable Red LED n° 15	SW
669	LED 15 Grn	Hardware version K - Programmable Green LED n° 15	SW
670	LED 16 Red	Hardware version K - Programmable Red LED n° 16	SW
671	LED 16 Grn	Hardware version K - Programmable Green LED n° 16	SW
672	LED 17 Red	Hardware version K - Programmable Red LED n° 17	SW
673	LED 17 Grn	Hardware version K - Programmable Green LED n° 17	SW
674	LED 18 Red	Hardware version K - Programmable Red LED n° 18	SW
675	LED 18 Grn	Hardware version K - Programmable Green LED n° 18	SW
676	Function Key 1	Hardware version K - Programmable Function key n° 1. In ‘Normal’ mode it is high on key press and in ‘Toggle’ mode remains high/low on single key press	SW
677 to 685	Function Key 2 to Function Key 10	Hardware version K - Function key n° 2 to Function key n° 10	SW
686 to 699	--	Unused	PSL
700 to 763	Output cond. 1 to Output cond. 64	Input to Relay Output Conditioner	PSL
764 to 799	--	Hardware version J – Unused	
764	LED 1 Red Condit	Hardware version K - Assignment of signal to drive output LED 1 red - To drive LED1 Yellow DDB 764 and DDB 765 must be driven at the same time	PSL
765	LED 1 Grn Condit	Hardware version K - Assignment of signal to drive output LED 1 green	PSL
766	LED 2 Red Condit	Hardware version K - Assignment of signal to drive output LED 2 red	PSL
767	LED 2 Grn Condit	Hardware version K - Assignment of signal to drive output LED 2 green	PSL
768	LED 3 Red Condit	Hardware version K - Assignment of signal to drive output LED 3 red	PSL
769	LED 3 Grn Condit	Hardware version K - Assignment of signal to drive output LED 3 green	PSL
770	LED 4 Red Condit	Hardware version K - Assignment of signal to drive output LED 4 red	PSL

Ordinal	English Text	Description	Source
771	LED 4 Grn Condit	Hardware version K - Assignment of signal to drive output LED 4 green	PSL
772	LED 5 Red Condit	Hardware version K - Assignment of signal to drive output LED 5 red	PSL
773	LED 5 Grn Condit	Hardware version K - Assignment of signal to drive output LED 5 green	PSL
774	LED 6 Red Condit	Hardware version K - Assignment of signal to drive output LED 6 red	PSL
775	LED 6 Grn Condit	Hardware version K - Assignment of signal to drive output LED 6 green	PSL
776	LED 7 Red Condit	Hardware version K - Assignment of signal to drive output LED 7 red	PSL
777	LED 7 Grn Condit	Hardware version K - Assignment of signal to drive output LED 7 green	PSL
778	LED 8 Red Condit	Hardware version K - Assignment of signal to drive output LED 8 red	PSL
779	LED 8 Grn Condit	Hardware version K - Assignment of signal to drive output LED 8 green	PSL
780	FnKey LED 1 Red	Hardware version K - Assignment of signal to drive output Function Key LED 1 Red - This LED is associated with Function Key 1	PSL
781	FnKey LED 1 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 1 Green - This LED is associated with Function Key 1 - To drive function key LED, yellow DDB 780 and DDB 782 must be active at the same time	PSL
782	FnKey LED 2 Red	Hardware version K - Assignment of signal to drive output Function Key LED 2 Red	PSL
783	FnKey LED 2 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 2 Green	PSL
784	FnKey LED 3 Red	Hardware version K - Assignment of signal to drive output Function Key LED 3 Red	PSL
785	FnKey LED 3 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 3 Green	PSL
786	FnKey LED 4 Red	Hardware version K - Assignment of signal to drive output Function Key LED 4 Red	PSL
787	FnKey LED 4 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 4 Green	PSL
788	FnKey LED 5 Red	Hardware version K - Assignment of signal to drive output Function Key LED 5 Red	PSL
789	FnKey LED 5 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 5 Green	PSL
790	FnKey LED 6 Red	Hardware version K - Assignment of signal to drive output Function Key LED 6 Red	PSL
791	FnKey LED 6 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 6 Green	PSL
792	FnKey LED 7 Red	Hardware version K - Assignment of signal to drive output Function Key LED 7 Red	PSL
793	FnKey LED 7 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 7 Green	PSL
794	FnKey LED 8 Red	Hardware version K - Assignment of signal to drive output Function Key LED 8 Red	PSL
795	FnKey LED 8 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 8 Green	PSL
796	FnKey LED 9 Red	Hardware version K - Assignment of signal to drive output Function Key LED 9 Red	PSL
797	FnKey LED 9 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 9 Green	PSL

Ordinal	English Text	Description	Source
798	FnKey LED 10 Red	Hardware version K - Assignment of signal to drive output Function Key LED 10 Red	PSL
799	FnKey LED 10 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 10 Green	PSL
800 to 829	--	Unused	PSL
830 to 845	Timer in 1 to Timer in 16	Hardware version K - PSL Input to Auxiliary Timer 1 to PSL Input to Auxiliary Timer 16	Auxiliary Timer
830 to 861	Timer in 1 to Timer in 16	Hardware version J - PSL Input to Auxiliary Timer 1 to PSL Input to Auxiliary Timer 32	Auxiliary Timer
846 to 861	Timer out 1 to Timer out 16	Hardware version K - PSL Ouput from Auxiliary Timer 1 PSL Ouput from Auxiliary Timer 16	Auxiliary Timer
862 to 893	Timer in 1 to Timer in 16	Hardware version J - PSL Output from Auxiliary Timer 1 to PSL Output from Auxiliary Timer 32	Auxiliary Timer
862 to 893	--	Hardware version K - Unused	PSL
894 to 922	--	Unused	PSL
923 to 1023		Can be created automatically by the PSL	PSL
1024	Trip LED	LED trip	
1025	CB Aux A (52-A)	Circuit breaker pole A closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1026	CB Aux A (52-B)	Circuit breaker pole A open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
1027	CB Aux B (52-A)	Circuit breaker pole B closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1028	CB Aux B (52-B)	Circuit breaker pole B open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
1029	CB Aux C (52-A)	Circuit breaker pole C closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1030	CB Aux C (52-B)	Circuit breaker pole C open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
1031	SPAR Enable	Enable internal single pole autorecloser. Set with Opto input (if linked by PSL) is energized (> 1s). At 1: 1P AR internal is enabled in the AR logic At 0: AR 1P internal is disabled (even if set in MiCOM S1 Agile). AR logic becomes 3P only with AR 3P cycle - if TPAR =1	PSL (IN) Autorecloser
1032	TPAR Enable	Enable internal three pole autorecloser Set with Opto input (if linked by PSL) is energized (> 1s). At 1: 3P AR internal is enabled in the AR logic At 0: AR 3P internal is disabled (even if set in MiCOM S1 Agile). 1P cycle available if SPAR =1	PSL (IN) Autorecloser
1033	A/R Internal	Give internal autorecloser present (visible): If it is assigned to an opto input in the PSL and energised, the DDB:'A/R Internal' will enable the internal AR logic. This opto input could be connected to an external condition such as the Watchdog of the Main1 protection – this activates the internal AR of Main 2 (P44x) in the case of an internal failure of the Main1.	PSL (IN) Autorecloser
1034	I A/R 1p In Prog	One-pole external autoreclose cycle in progress: If it is assigned to an opto input in the PSL and energised, The DDB:'A/R 1P in Prog' will block the internal DEF protection as it indicates that an external single-pole autoreclose cycle is in progress.	PSL (IN) Autorecloser

Ordinal	English Text	Description	Source
1035	I A/R 3p In Pr.	Three-pole external autoreclose cycle in progress: If it is assigned to an opto input in the PSL and energised, the DDB:'A/R 3P in Prog' will inform the P44x about the presence of an external 3P cycle. The data is useful in the case of an evolving fault.	PSL (IN) Autorecloser
1036	I A/R Close	Circuit Breaker closing order from external autoreclose: If it is assigned to an opto input in the PSL and energised, the DDB:'A/R Close' can be linked with the internal check synchronism condition to verify the external CB close command.	PSL (IN) Autorecloser
1037	I A/R Reclaim	External (opto input) autorecloser in progress: the DDB:'I A/R Reclaim' signal will inform the protection that an external reclaim time is in progress and will initiate the internal TOR logic (it is possible to create a dedicated PSL which would make it possible to use this information extension in Zone 1 extension schemes).	PSL (IN) Autorecloser
1038	BAR	Block internal autoreclose: Block Autoreclose (via an opto input or in the PSL). The DDB:'BAR' input will block the autoreclosure and lockout the autoreclose if a cycle is in progress. If a single-pole cycle is in progress a three-pole trip will be issued and the autorecloser will lock out. It can be used when protection operation is required without autoreclose. A typical example is for a transformer feeder, where autoreclosing may be initiated by the feeder's protection relay but blocked by the transformer's protection relay. Similarly, where a circuit breaker low gas pressure or loss of vacuum alarm occurs during the dead time, autoreclosure should be blocked – and BAR can be used to perform this blocking logic.	PSL (IN) Autorecloser
1039	Ext Chk Synch OK	Autorisation signal from external check Synchroniser (via opto input, with a dedicated PSL) for reclosing with internal autoreclose (indicates that Check Sync conditions are met by an external device – The DDB cell should be assigned afterwards an internal AR logic), If an opto input is assigned in the PSL, the autoreclose close command will be verified by an external check synchronism device. The input is energised when the Check Sync conditions are met.	PSL (IN) Autorecloser
1040	CB Healthy	Circuit breaker operational (gas pressure, mechanical state) Must be at 1 inside the time window (setting: group1/ Autoreclose mode/ AR Inhibit Wind) during an AR cycle ('A/R close' and 'A/R Reclaim' pick up when 'CB healthy' is detected during the 'A/R Inhibit Wind' time-delay')	PSL (IN) CB STATUS
1041	BLK Protection	Block all protection functions (21/67N/50/51/…)	PSL (IN) All protection
1042	Force 3P Trip	Three pole tripping only: If it is assigned to an opto input in the PSL and energised, the DDB:'Force 3P Trip' signal will force the internal single-phase protection to trip three-poles (external order from Main1 to Main2 (P44x)) – the next trip will be three-pole.	PSL (IN)

Ordinal	English Text	Description	Source
1043	Man. Close CB	Circuit breaker manual close - order received. 'If it is assigned to an opto input in the PSL and energised the DDB:'Man Close CB' signal will enable the internal 'SOTF Enable' logic without CB control activation. If CB control is activated, SOTF will be enabled by internal detection ('CB close' order managed by CB control). Manual closure of the circuit breaker will force the autorecloser in a lockout logic, if selected in the 'Distance schemes / TOR-SOTF Mode') menu. Any fault detected within 500 ms of a manual closure will cause an instantaneous three pole tripping, without autoreclose (see Block Autoreclose (BAR) logic) When autoreclose lockout (BAR) is activated, the autorecloser does not initiate any additional reclosing cycle. If autoreclose lockout picks up during a cycle, the A/R close is blocked. This prevents excessive circuit breaker operations, which could result in increased circuit breaker and system damage, when closing onto a fault.	PSL (IN) CB Status
1044	Man. Trip CB	Circuit breaker manual trip - order received. If it is assigned to an opto input in the PSL and energised, the DDB:'Man Trip CB' signal will inform the protection of an external CB trip command by the CB control function (if activated).	PSL (IN) CB Status
1045	CB Discrepancy	CB Discrepancy (one pole open). If it is assigned to an opto input in the PSL and energised, the DDB:'CB Discrepancy' signal will inform the protection of a pole discrepancy status (one pole opened and the other two poles closed). It must be set to high logical level before Dead time 1 has elapsed – it can also be generated internally (see Cbaux logic).	PSL (IN) CB Status
1046	External Trip A	Phase A trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip A (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1047	External Trip B	Phase B trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip B (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1048	External Trip C	Phase C trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip C (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1049	DIST. Chan Recv	Signal (carrier sent by zone) received on main channel for distance scheme logic (depending on the ‘Distance scheme’ setting: Program mode / Standard mode)	PSL (IN) Un-blocking logic
1050	DEF. Chan Recv	Signal received on main channel for DEF scheme logic (depending on settings: Aided DEF/Scheme logic) Selected as shared by default – Can operate as an independent scheme with a separate opto input from Dist Default PSL: Opto Label 1	PSL (IN) Un-blocking logic

Ordinal	English Text	Description	Source
1051	DIST. COS	Distance scheme channel out of service / Loss of Guard (Carrier out of service)	PSL (IN) Un-blocking logic
1052	DEF. COS	DEF scheme channel out of service / Loss of Guard Selected shared by default – Can operate as an independent scheme with a different opto input from Dist Default PSL: Opto Label 2	PSL (IN) Un-blocking logic
1053	Z1X Extension	Zone 1 Extension Input Opto input energized if linked by PSL OR any internal DDB by dedicated PSL At 1: Signal will initiate Z1 extension logic if selected (setting). This DDB can be assigned to any external/Internal condition for starting Z1X logic	PSL (IN)
1054	MCB/VTS Synchro	Fuse failure on busbar VT or MCB open (blocks voltage dependant functions), If it is linked to an opto input in the PSL and energised, the DDB signal informs the P44x about an internal maloperation from the VT used for synchronisation check (see Check Synchronism logic section).	PSL (IN) VTS
1055	MCB/VTS Main	Fuse failure on line VT or MCB open (blocks voltage dependant functions). If it is linked to an opto input in the PSL energised, the DDB informs the P44x about an internal maloperation from the VT used for the impedance measurement reference (line in this case means Main VT ref measurement, even if the main VT is on the bus side and the Synchronism check VT is on the line side).	PSL (IN) VTS
1056	IN>1 Timer Block	Block earth fault stage 1 time delay Set to 1: 'IN>1 Time Delay' will be blocked & IN>1 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
1057	IN>2 Timer Block	Block earth fault stage 2 time delay Set to 1: 'IN>2 Time Delay' will be blocked & IN>2 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
1058	IN>3 Timer Block	Block earth fault stage 3 time delay Set to 1: 'IN>3 Time Delay' will be blocked & IN>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
1059	IN>4 Timer Block	Block earth fault stage 4 time delay Set to 1: The IN>4 time-delay will be blocked & IN>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
1060	DEF Timer Block	Block aided DEF time delay The DEF time-delay will be blocked & DEF will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) DEF
1061	I>1 Timer Block	Block phase overcurrent stage 1 time delay Set to 1: 'I>1 Time Delay' will be blocked & I>1 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>1
1062	I>2 Timer Block	Block phase overcurrent stage 2 time delay Set to 1: 'I>2 Time Delay' will be blocked & I>2 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>2

Ordinal	English Text	Description	Source
1063	I>3 Timer Block	Block phase overcurrent stage 3 time delay Set to 1: 'I>3 Time Delay' will be blocked & I>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>3
1064	I>4 Timer Block	Block phase overcurrent stage 4 time delay Set to 1: 'I>4 Time Delay' will be blocked & I>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>4
1065	I2>1 Timer Block	Block negative sequence overcurrent stage 1 time delay	PSL (IN) I>4
1066	I2>2 Timer Block	Block negative sequence overcurrent stage 2 time delay	PSL (IN) I>5
1067	I2>3 Timer Block	Block negative sequence overcurrent stage 3 time delay	PSL (IN) I>6
1068	I2>4 Timer Block	Block negative sequence overcurrent stage 4 time delay	PSL (IN) I>7
1069	V<1 Timer Block	Block phase undervoltage stage 1 time delay Set to 1: 'V<1 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<1
1070	V<2 Timer Block	Block phase undervoltage stage 2 time delay Set to 1: 'V<2 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<2
1071	V<3 Timer Block	Block phase undervoltage stage 3 time delay Set to 1: 'V<3 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<3
1072	V<4 Timer Block	Block phase undervoltage stage 4 time delay Set to 1: 'V<4 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<4
1073	V>1 Timer Block	Block phase overvoltage stage 1 time delay Set to 1: 'V>1 Time Delay will be blocked and V>1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>1
1074	V>2 Timer Block	Block phase overvoltage stage 2 time delay Set to 1: 'V>2 Time Delay' will be blocked and V>2 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>2
1075	V>3 Timer Block	Block phase overvoltage stage 3 time delay Set to 1: 'V>3 Time Delay' will be blocked and V>3 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>3
1076	V>4 Timer Block	Block phase overvoltage stage 4 time delay Set to 1: 'V>4 Time Delay' will be blocked and V>4 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>4
1077	VN>1 Timer Block	Block earth overvoltage stage 1 time delay	PSL (IN) VN>1
1078	VN>2 Timer Block	Block earth overvoltage stage 2 time delay	PSL (IN) VN>2

Ordinal	English Text	Description	Source
1079	DIST. Tim. Block	Block distance element time delay At 1: The distance timer will be blocked & DIST will start but will not perform a Trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Distance
1080	Reset Lockout	Reset all CB monitoring lockout (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1081	Reset All values	Reset all values of CB monitoring (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1082	Reset Latches	Reset all permanent alarms + LEDs and relays are lached	PSI (IN)
1083	Stub Bus Enable	Enable I>4 Element for stub bus protection (isolator of HV line open - status isolator must be connected to an opto input)	PSL (IN)
1084	User Trip A	Internal input for trip logic A Set to 1: Trip A Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1085	User Trip B	Internal input for trip logic B Set to 1: Trip B Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1086	User Trip C	Internal input for trip logic C Set to 1: Trip C Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1087	ZSP Timer Block	Zero Sequence Power - Timer Block: If assigned to an opto input in a dedicated PSL, Zero Sequence Power function will start, but will not perform a trip command - the associated time-delay (adjusted with 'K Time Delay Factor ' setting, will be blocked	PSL (IN) ZSP
1088	PAP TeleTrip CR	PAP (specific application) Carrier Receive for teletransmission	PSL(IN)
1089	PAP TeleT. Heath	PAP (specific application) Carrier Out of Service (DT trip decision)	PSL(IN)
1090	PAP Timer Block	Timer Block for frosen every timer initiated with PAP (specific application) function	PSL(IN)
1091	Reset Thermal	Reset Thermal Overload Protection	PSL(IN)
1092	Time Synch	External time synchronisation input	PSL(IN)
1093	Select CS(NCIT)	Select Check synchro for NCIT	PSL
1094	T1 Timer Block	Timer block T1 input	PSL
1095	T2 Timer Block	Timer block T2 input	PSL
1096	TZp Timer Block	Timer block TZp input	PSL
1097	TZq Timer Block	Timer block TZq input	PSL
1098	T3 Timer Block	Timer block T3 input	PSL
1099	T4 Timer Block	Timer block T4 input	PSL
1100	F<1 Timer Block	Timer block underfrequency stage 1	PSL (IN)
1101	F<2 Timer Block	Timer block underfrequency stage 2	PSL (IN)
1102	F<3 Timer Block	Timer block underfrequency stage 3	PSL (IN)
1103	F<4 Timer Block	Timer block underfrequency stage 4	PSL (IN)
1104	F>1 Timer Block	Timer block overfrequency stage 1	PSL (IN)
1105	F>2 Timer Block	Timer block overfrequency stage 2	PSL (IN)
1106	I<1 Block	Block phase undercurrent stage 1	PSL (IN)
1107	I<2 Block	Block phase undercurrent stage 2	PSL (IN)
1108	I<1 Timer Block	Timer block phase undercurrent stage 1	PSL (IN)

Ordinal	English Text	Description	Source
1109	I<2 Timer Block	Timer block phase undercurrent stage 2	PSL (IN)
1110	103 MontorBlock	For IEC-870-5-103 protocol only, used for "Monitor Blocking" (relay is quiet - issues no messages via SCADA port)	PSL
1111	103 CommandBlock	For IEC-870-5-103 protocol only, used for "Command Blocking" (relay ignores SCADA commands)	PSL
1112	RP1 Read Only	All setting changes and most command/control actions blocked for Rear Port 1.	PSL
1113	RP2 Read Only	All setting changes and most command/control actions blocked for Rear Port 2.	PSL
1114	NIC Read Only	All setting changes and most command/control actions blocked for the Ethernet port (when option available).	PSL
1115	SBO InterLock 1	SBO support for IEC 61850-8-1 control function with interlocking facilities 1	PSL
1116	SBO DPI1 Org1	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 1	PSL
1117	SBO DPI2 Org1	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 1	PSL
1118	SBO Command1	SBO support for IEC 61850-8-1 function command 1	PSL
1119	SBO InterLock 2	SBO support for IEC 61850-8-1 control function with interlocking facilities 2	PSL
1120	SBO DPI1 Org2	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 2	PSL
1121	SBO DPI2 Org2	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 2	PSL
1122	SBO Command2	SBO support for IEC 61850-8-1 function command 2.	PSL
1123	SBO InterLock 3	SBO support for IEC 61850-8-1 control function with interlocking facilities 3	PSL
1124	SBO DPI1 Org3	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 3	PSL
1125	SBO DPI2 Org3	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 3	PSL
1126	SBO Command3	SBO support for IEC 61850-8-1 function command 3	PSL
1127	SBO InterLock 4	SBO support for IEC 61850-8-1 control function with interlocking facilities 4	PSL
1128	SBO DPI1 Org4	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 4	PSL
1129	SBO DPI2 Org4	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 4	PSL
1130	SBO Command4	SBO support for IEC 61850-8-1 function command 4.	PSL
1131 to 1223	--	Unused	PSL
1224	Virtual Input 1	Goose input n° 1 - Allows binary signals that are mapped to virtual inputs to interface into PSL	SW
1225 to 1287	Virtual Input 2 to Virtual Input 64	Goose input n° 2 to Goose input n° 32	SW
1288 to 1352	--	Unused	PSL
1353 to 1415	Quality VIP 1 to Quality VIP 64	Validation of the virtual input 1 (to 64) (signal correct).	PSL
1416 to 1479	--	Unused	PSL
1480 to 1543	PubPres VIP 1 to PubPres VIP 64	Publishing presence of virtual input 1 (to 64): indicates virtual input 1 (to 64) presence.	PSL

Ordinal	English Text	Description	Source
1544 to 2047	--	Unused (except next DDBs for specific options)	PSL
1672 to 1677	LN1 Analog Alarm to LN6 Analog Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL
1680 to 1685	LN1 Test Mode to LN6 Test Mode	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is in “Test Mode”	PSL
1688 to 1693	LN1 Async to LN6 Async	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is synchronized with Internal (local) synchronization	PSL
1696 to 1701	LN1 Val Quest to LN6 Val Quest	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “questionable”	PSL
1704 to 1709	LN1 Val Fail to LN6 Val Fail	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “failed”	PSL

1.1.2 Sorted by name

Ordinal	English Text	Description	Source
1111	103 CommandBlock	For IEC-870-5-103 protocol only, used for "Command Blocking" (relay ignores SCADA commands)	PSL
1110	103 MontorBlock	For IEC-870-5-103 protocol only, used for "Monitor Blocking" (relay is quiet - issues no messages via SCADA port)	PSL
328	1P Trip	Single pole trip (internal or external)	PSL (OUT) All protection
318	1ph Fault	Single phase fault	PSL (OUT) Distance
319	2ph Fault	Two phase fault	PSL (OUT) Distance
329	3P Trip	Three pole trip (internal or external)	PSL (OUT) All protection
320	3ph Fault	Three phase fault	PSL (OUT) Distance
224	A/R 1P In Prog	One-pole autoreclose cycle in progress: A single pole autoreclose cycle is in progress. This output will remain activated from the initial protection trip until the circuit breaker is closed successfully or the autoreclose function is Locked Out, indicating that a dead time timeout is in progress. This signal may be useful during relay commissioning to check the operation of the autoreclose cycle.	PSL (OUT) Autorecloser
226	A/R 1st In Prog	First high speed autoreclose cycle in progress: Used to indicate the autorecloser is timing out its first dead time, either a high-speed single-pole shot or a high speed three-pole shot.	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
227	A/R 234 In Prog	Further autoreclose cycles in progress: Used to indicate the autorecloser is timing out delayed autoreclose dead times for shots 2, 3 or 4. Where some protection elements should not initiate autoreclosure for Delayed Autoreclose (DAR) shots, the protection element operation is combined with 'A/R 234 in Prog' as a logic AND operation in the Programmable Scheme Logic, and then set to assert the DDB:'BAR' input, forcing lockout.	PSL (OUT) Autorecloser
225	A/R 3P In Prog	Three-pole autoreclose cycle in progress: A three phase autoreclose cycle is in progress. This output will remain activated from the initial protection trip until the circuit breaker is closed successfully or the AR function is Locked Out, indicating that a dead time timeout is in progress. This signal may be useful during relay commissioning to check the operation of the autoreclose cycle.	PSL (OUT) Autorecloser
223	A/R Close	Autorecloser Close command to CB: Initiates the reclose command pulse to the circuit breaker. This output feeds a signal to the Reclose time-delay, which maintains the linked reclose contact closed for a time sufficient to ensure reliable CB mechanism operation. This DDB signal may also be useful during relay commissioning to check the operation of the autoreclose cycle. Where three single pole circuit breakers are used, the AR Close contact will need to energise the closing circuits for all three breaker poles (or alternatively assign three CB Close contacts).	PSL (OUT) Autorecloser
231	A/R Enable	Indicates the autoreclose function is in service 1 = [If 'A/R SPAR Enable' OR 'A/R TPAR Enable'] AND "Internal A/R' = enabled (setting) Reset to 0: If 'A/R SPAR Enable'=0 AND 'A/R TPAR Enable'=0 (if assigned in PSL) + "Internal A/R' = disabled (setting)	PSL (OUT) Autorecloser
196	A/R Fail	No check sync / autorecloser failed: If the check sync conditions are not met prior to reclosing within the time window, the 'A/R Fail' alarm will be raised.	PSL (OUT) Autorecloser
235	A/R Force Sync.	Force synchronism check to be made (simulate the CheckSync control and forces the DDB:'CheckSync OK' (logic output) to 1 during a 1-pole or 3-pole high speed autoreclose cycle) The signal is reset with A/R reclaim	PSL (OUT) Autorecloser
1033	A/R Internal	Give internal autorecloser present (visible): If it is assigned to an opto input in the PSL and energised, the DDB:'A/R Internal' will enable the internal AR logic. This opto input could be connected to an external condition such as the Watchdog of the Main1 protection – this activates the internal AR of Main 2 (P44x) in the case of an internal failure of the Main1.	PSL (IN) Autorecloser

Ordinal	English Text	Description	Source
234	A/R Lockout	Autorecloser locked-out (no autoreclosure possible until reset), If protection operates during the reclaim time, after the final reclose attempt, the relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition is reset. This will produce an alarm: A/R Lockout. Then, the DDB:'BAR' input will block the autorecloser and cause a lockout if a reclose cycle is in progress. Lockout will also occur if the CB energy is low and the CB fails to close. Once the autorecloser is locked out, it will not function until a Reset Lockout or CB Manual Close command is received (depending on the Reset Lockout method chosen in CB Monitor Setup). NOTE: Lockout can also be caused by the CB condition monitoring functions maintenance lockout, excessive fault frequency lockout, broken current lockout, CB failed to trip and CB failed to close, manual close no check synchronism and CB unhealthy. Set to 1 = 'A/R Enable' AND [('BAR' =1 (see internal logic) OR ' A/R lockout shot> (AR lockout by number of shots) OR (No CB Healthy at the end of Inhibit Window (setting)) OR (No 'CB discrepancy' (opto input or internal by CBAux if present in PSL) at the end of 1P Dead time1) OR Trip 1P or3P maintained / still present at the end of the1P or 3P Dead time) or after discrimination time-delay if a 3-pole trip occurs during a 1-Pole AR Cycle] At 0: AR activated Reset to 0 = ('Reset 1P Trip' OR 'Reset 3P Trip') AND (End of reclaim time) AND Reset (BAR) AND Reset (A/R lockout shot>) AND Reset (No CB Healthy) AND Reset (No Discrepancy)	PSL (OUT) Autorecloser
229	A/R Reclaim	Internal autoreclose reclaim in progress (reclaim time timeout in progress). If it is assigned to an opto input in the PSL and when energised, the DDB:‘A/R Reclaim’ signal will start the internal logic TOR enable (External AR logic applied). The DDB indicates the reclaim time following a particular autoreclose shot is timing out. The DDB:'AR Reclaim' output would be energised at the same instant as any Cycle outputs are reset. ‘A/R Reclaim’ may be used to block low-set instantaneous protection on autoreclosure, when it has not been time-graded with a downstream protection. This technique is commonly used when the downstream devices are fuses, and fuse saving is implemented. This avoids fuse blowing for transient faults. ‘A/R reclaim’ can be connected to Main2 for cycle in progress external information. It initiates the internal TOR logic	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
232	A/R SPAR Enable	Single pole autorecloser (SPAR) activated: If it is assigned to an opto input in the PSL (by default PSL is inverted and linked to opto 8) and energized, The DDB:'A/R SPAR Enable' will enable the 1-pole autoreclose logic (the priority of this input is higher than the 'CB Control/A/R single pole' setting) - this means the 1-pole autoreclose logic can be disabled even if it has been activated; if the relevant opto input is not energized (to be valid, the opto must be energised for over 1.2 s). NOTE: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the “A/R enable” logic state). Set to 1: 1P AR activated (copy of 'SPAR Enable' opto input OR 'CB Control/ A/R Single pole' enabled) Reset to 0: if 'SPAR Enable' = 0 OR (A/R Single pole' disabled)	PSL (OUT) Autorecloser
233	A/R TPAR Enable	Three pole autorecloser (TPAR) activated: If it is assigned to an opto input in the PSL (by default, the PSL is inverted and linked to opto 8) and energized, the DDB:'A/R TPAR Enable' will enable the 3-pole autoreclose logic (the priority is higher than the 'CB Control / A/R three pole' setting) - this means the 3-pole autoreclose logic can be disabled even if it has been activated; if the relevant opto input is not energised (to be valid, the opto input must be energised for over 1.2 s). NOTE: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the “AR enable” logic sate). Set to 1: 3P AR activated (copy of 'TPAR enable' opto input OR 'CB Control/ A/R Three pole' enabled) Reset to 0: if 'TPAR enable' = 0 OR ('A/R Three pole' disabled)	PSL (OUT) Autorecloser
228	A/R Trip 3P	Autorecloser signal to force all trips to be 3 Ph: This is an internal logic signal used to condition any protection trip command to the circuit breaker(s). Where single-pole tripping is enabled, a fixed logic converts single-phase trips for faults on autoreclosure to three-pole trips. A/R Trip 3P can be connected to Main2 as an external "Force 3-pole" 1 = ('Internal A/R' setting enabled) AND (No 'A/R SPAR Enable') 0 = 'A/R SPAR Enable' AND ('Internal A/R' setting enabled)+ ('Inhibit Window' at 0)	PSL (OUT) Autorecloser
208	alarm user 1	Alarm user for dedicated PSL	PSL(IN)
209	alarm user 2	Alarm user for dedicated PSL	PSL(IN)
210	alarm user 3	Alarm user for dedicated PSL	PSL(IN)
211	alarm user 4	Alarm user for dedicated PSL	PSL(IN)
212	alarm user 5	Alarm user for dedicated PSL	PSL(IN)
342	All Pole Dead	All circuit breaker poles dead (breaker open 3 phase, pole status detected by Cbaux or internal thresholds). If it is linked in the PSL, the DDB:'All Pole Dead' signal indicates that all poles are dead (3 poles are open). All Pole Dead = Pole Dead A AND Pole Dead B AND Pole Dead C	PSL (OUT) Poledead
393	Any Int. Trip	Any Internal trip	PSL

Ordinal	English Text	Description	Source
322	Any Int. Trip A	Any internal protection A phase trip Default PSL: LED 1, Relay 02	PSL (OUT) All protection
323	Any Int. Trip B	Any internal protection B phase trip Default PSL: LED 2, Relay 03	PSL (OUT) All protection
324	Any Int. Trip C	Any internal protection C phase trip Default PSL: LED 3, Relay 04	PSL (OUT) All protection
341	Any Pole Dead	Any circuit breaker pole dead (one or more poles open, pole status detected by CBaux or internal thresholds). If it is linked in the PSL, the DDB:'Any Pole Dead' signal indicates that one or more poles are open. Any Pole Dead = Pole Dead A OR Pole Dead B OR Pole Dead C	PSL (OUT) Poledead
317	Any start	Any protection start logic with any phase Default PSL: LED 4, Relay 06 (Fault record trigger in default PSL with 20 ms Dwell Timer)	PSL (OUT) All protection
321	Any Trip	Single or three pole trip or external protection trip Default PSL: Relay 07	PSL (OUT) All protection
325	Any Trip A	Any trip A (internal or external protection)	PSL (OUT) All protection
326	Any Trip B	Any trip B (internal or external protection)	PSL (OUT) All protection
327	Any Trip C	Any trip C (internal or external protection)	PSL (OUT) All protection
230	AR Discrim.	'Discrimination time' window in progress (starts with the trip command). When a single pole trip is issued by the relay, a 1-pole AR cycle is initiated. The 'Dead time 1' and 'Discrimination time' are started. If the autoreclose logic detects a single pole or three-pole trip (internal or external) during the discrimination time-delay, the single pole high speed autoreclose cycle is disabled and replaced by a three pole high speed autoreclose cycle, if enabled. If no three-pole autoreclose is enabled, the relay trips 3-pole and the autoreclose is blocked. If the autoreclose logic detects a 3-pole trip (internal or external) when the Discrimination time-delay has elapsed and during the 1-pole dead time; the single pole AR cycle is stopped and the relay trips 3-pole and blocks the autoreclose.	PSL (OUT) Autorecloser
194	AR Lockout Shot>	Autoreclose lockout following final programmed attempt: Indicates a failed autoreclose (definitive trip following the last reclosing shot). The relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition has been reset. An alarm, "AR Lockout Shots>" (along with AR Lockout) will be raised. 1 = 'A/R Enable' & [('1Ptrip & No 'SPAR Enable') + (3P Trip & No 'TPAR enable) + ('1P Trip' + '3P Trip') & (Number of shots=setting)]	PSL (OUT) Autorecloser
486	Back Up Setting	Back up setting alarm	PSL(OUT)
478	Bad OSI Config.	Ethernet alarm	PSL(OUT)
477	Bad TCP/IP Cfg.	Bad configuration TCP/IP Address alarm	PSL(OUT)

Ordinal	English Text	Description	Source
1038	BAR	Block internal autoreclose: Block Autoreclose (via an opto input or in the PSL). The DDB:'BAR' input will block the autoreclosure and lockout the autoreclose if a cycle is in progress. If a single-pole cycle is in progress a three-pole trip will be issued and the autorecloser will lock out. It can be used when protection operation is required without autoreclose. A typical example is for a transformer feeder, where autoreclosing may be initiated by the feeder's protection relay but blocked by the transformer's protection relay. Similarly, where a circuit breaker low gas pressure or loss of vacuum alarm occurs during the dead time, autoreclosure should be blocked – and BAR can be used to perform this blocking logic.	PSL (IN) Autorecloser
469	Battery Fail	Alarm battery fail	PSL(OUT)
1041	BLK Protection	Block all protection functions (21/67N/50/51/…)	PSL (IN) All protection
330	Brk.Conduct.Trip	Broken conductor trip	PSL (OUT) Broken Cond.
202	Brok. Cond. Alarm	Broken Conductor Alarm	PSL(OUT) Broken conductor
338	CB Aux A	CB Phase A status (from internal logic and CBAux opto inputs state: 1 = CB-Pole A is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
1025	CB Aux A (52-A)	Circuit breaker pole A closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1026	CB Aux A (52-B)	Circuit breaker pole A open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
339	CB Aux B	CB Phase B status (from internal logic and CBAux opto inputs state: 1 = CB-Pole B is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
1027	CB Aux B (52-A)	Circuit breaker pole B closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1028	CB Aux B (52-B)	Circuit breaker pole B open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
340	CB Aux C	CB Phase C status (from internal logic and CBAux opto inputs state: 1 = CB-Pole C is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
1029	CB Aux C (52-A)	Circuit breaker pole C closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1030	CB Aux C (52-B)	Circuit breaker pole C open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
1045	CB Discrepancy	CB Discrepancy (one pole open). If it is assigned to an opto input in the PSL and energised, the DDB:'CB Discrepancy' signal will inform the protection of a pole discrepancy status (one pole opened and the other two poles closed). It must be set to high logical level before Dead time 1 has elapsed – it can also be generated internally (see Cbaux logic).	PSL (IN) CB Status
179	CB Fail Alarm	Circuit breaker failure on any trip	PSL (OUT) Breaker Fail

Ordinal	English Text	Description	Source
1040	CB Healthy	Circuit breaker operational (gas pressure, mechanical state) Must be at 1 inside the time window (setting: group1/ Autoreclose mode/ AR Inhibit Wind) during an AR cycle ('A/R close' and 'A/R Reclaim' pick up when 'CB healthy' is detected during the 'A/R Inhibit Wind' time-delay')	PSL (IN) CB STATUS
185	CB Op Time Lock	CB locked out, due to excessive operating time: An alarm is issued when the operating tripping time on any phase pass over the 'CB monitor setup / CB Time Lockout' setting (slowest pole detection calculated by I< from CB Fail logic)	PSL (OUT) CB monitoring
184	CB Op Time Maint	CB excessive operating time alarm: An alarm is issued when the operating tripping time on any phase pass over the 'CB monitor setup / CB Time Maint' setting (slowest pole detection calculated by I< from CB Fail logic)	PSL (OUT) CB monitoring
183	CB Ops Lockout	Circuit breaker operation number lockout (2nd level alarm): An alarm is issued when the maximum of CB operations is reached [initiated by internal or external trip, see setting: 'CB Monitor Setup\N° CB Ops Lockt.] Set to 0: Until number of operations is below the 'N° CB Ops Lockt." setting. The DDB:'Reset all values' resets this counter.	PSL (OUT) CB monitoring
182	CB Ops Maint	Circuit breaker operations number alarm (1st level): An alarm is issued when the maximum of CB operations is reached. This alarm is initiated by internal (any protection function) or external trip (via opto input). The Alarm can be set with 'CB Monitor Setup / N° CB Ops Maint.' setting. Set to 0: Until number of operations is below the 'N° CB 0ps Maint.' setting. The DDB:'Reset all values' resets this counter.	PSL (OUT) CB monitoring
189	CB Status Alam	Circuit Breaker Alarm Displayed when a CB Failure or CB State unknown condition is detected (the 'System data / Plant Status' two last digits = 00 or 11). The CB discrepancy status is detected after CBA time-delay issued by opto input or internally by CBAux logic – Alarm issued after 5 s	PSL (OUT)
236	Check Synch. OK	If linked to an opto input in a dedicated PSL and energised, it indicates that external synchronism conditions are met – This can be linked afterwards to an internal autoreclose logic	PSL (OUT) Synchro Check
471	Comm2 H/W FAIL	Alarm second rear port	PSL(OUT)
336	Control Close	Control close command from user (by internal CB control)	PSL (OUT) CB control
608	Control input 1	Control Input 1 - for SCADA and menu commands into PSL	SW
609 to 639	Control input 2 to Control input 32	Control input 2 to Control input 32	SW
193	Control No C/S	Autoreclosed works without check synchronism (high when the internal Check Synchronism conditions are not met).	PSL (OUT)
335	Control Trip	Control trip command from user (by internal CB control)	PSL (OUT) CB control
201	COS Alarm	HF carrier anomaly alarm (Carrier out of service)	PSL(OUT) Unblocking logic
346	Cross Count. Flt	Cross Country Fault Set to 1: The cross country logic is activated (1 Fault Fwd/1 Fault Rev detected)	PSL (OUT) Distance

Ordinal	English Text	Description	Source
178	CT Fail Alarm	Current transformers supervision indication: Indicates a CT Fail detected after time delay has elapsed is issued	PSL (OUT) CT Supervision
241	Ctrl Cls In Prog	Manual (control) close in progress - using CB control (time-delay manual closing delay in progress).	PSL (OUT) CB Control
203	CVT Alarm	Alarm for capacitive voltage Transformer: Indicates the residual voltage is greater than the threshold adjusted in the settings, during a time-delay greater than the adjustment. That alarm is also included in the general alarm.	PSL (OUT)
274	DEF Fwd	Channel Aided DEF: forward fault	PSL (OUT) Aided DEF
273	DEF Rev	Channel Aided DEF: reverse fault	PSL (OUT) Aided DEF
271	DEF Sig. Send	DEF protection schemes - Signal Send (Default PSL: Relay 05)	PSL (OUT) Aided DEF
275	DEF Start A	Channel Aided DEF: start phase A	PSL (OUT) Aided DEF
276	DEF Start B	Channel Aided DEF: start phase B	PSL (OUT) Aided DEF
277	DEF Start C	Channel Aided DEF: start phase C	PSL (OUT) Aided DEF
1060	DEF Timer Block	Block aided DEF time delay The DEF time-delay will be blocked & DEF will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) DEF
278	DEF Trip A	Channel Aided DEF: trip phase A Default PSL: Relay 09	PSL (OUT) Aided DEF
279	DEF Trip B	Channel Aided DEF: trip phase B Default PSL: Relay 09	PSL (OUT) Aided DEF
280	DEF Trip C	Channel Aided DEF: trip phase C Default PSL: Relay 09	PSL (OUT) Aided DEF
272	DEF UNB CR	Unblocking DEF channel internal Carrier Received signal (main Directional Earth Fault unblocking signal) received.	PSL (OUT) Unblocking logic
1050	DEF. Chan Recv	Signal received on main channel for DEF scheme logic (depending on settings: Aided DEF/Scheme logic) Selected as shared by default – Can operate as an independent scheme with a separate opto input from Dist Default PSL: Opto Label 1	PSL (IN) Un-blocking logic
1052	DEF. COS	DEF scheme channel out of service / Loss of Guard Selected shared by default – Can operate as an independent scheme with a different opto input from Dist Default PSL: Opto Label 2	PSL (IN) Un-blocking logic
345	DIST Convergency	Distance protection: Internal characteristic Set to 1: logic with Distance Start at 1 (Minimum 1 loop has been detected in the quadrilateral characteristic) Set to 0: Reset of (R, X) (resistance, reactance) calculation made by the All pole Dead detection	PSL (OUT) Distance
244	DIST Fwd	Distance protection: Forward fault detected (default PSL: LED6) Set to 1: Directional Forward detected in distance algorithms (Deltas or Conventional) AND (Distance Start) Set to 0: With reset of Any Start/Dist Start	PSL (OUT) Distance

Ordinal	English Text	Description	Source
343	DIST Fwd No Filt	Distance protection: Forward fault detected not filtered (Directional Forward decision made by Distance logic without any filter by Distance Start or Zone: Picks up faster than Dist Fwd)	PSL (OUT) Distance
245	DIST Rev	Distance protection: Reverse fault detected (default PSL: LED7) Set to 1: Directional Reverse detected in distance algorithms (Deltas or Conventional) AND (Distance Start) Set to 0: With reset of Any Start/Dist Start	PSL (OUT) Distance
344	DIST Rev No Filt	Distance protection: Reverse fault detected not filtered (Directional Forward decision made by Distance logic without any filter by Distance Start or Zone: Picks up faster than Dist Fwd)	PSL (OUT) Distance
252	DIST Sch. Accel.	Distance scheme Accelerating	PSL (OUT) Distance
254	DIST Sch. Block.	Distance scheme Blocking	PSL (OUT) Distance
253	DIST Sch. Perm.	Distance scheme Permissive	PSL (OUT) Distance
242	DIST Sig. Send	Distance protection schemes - Signal Send (default PSL: Relay 05)	PSL (OUT) Distance
249	DIST Start A	Distance protection started on phase A Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
250	DIST Start B	Distance protection started on phase B Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
251	DIST Start C	Distance protection started on phase C Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
354	Dist Start N	Start of distance protection for phase to ground fault	PSL (OUT)
246	DIST Trip A	Distance protection: Phase A trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80ms)	PSL (OUT) Distance
247	DIST Trip B	Distance protection: Phase B trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80ms)	PSL (OUT) Distance
248	DIST Trip C	Distance protection: Phase C trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80ms)	PSL (OUT) Distance
243	DIST UNB CR	Unblock main channel received Internal Carrier Received signal (main Distance unblocking signal) received.	PSL(OUT) Unblocking Logic
1049	DIST. Chan Recv	Signal (carrier sent by zone) received on main channel for distance scheme logic (depending on the 'Distance scheme' setting: Program mode / Standard mode)	PSL (IN) Un-blocking logic
1051	DIST. COS	Distance scheme channel out of service / Loss of Guard (Carrier out of service)	PSL (IN) Un-blocking logic

Ordinal	English Text	Description	Source
1079	DIST. Tim. Block	Block distance element time delay At 1: The distance timer will be blocked & DIST will start but will not perform a Trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Distance
1039	Ext Chk Synch OK	Authorization signal from external check Synchroniser (via opto input, with a dedicated PSL) for reclosing with internal autoreclose (indicates that Check Sync conditions are met by an external device – The DDB cell should be assigned afterwards an internal AR logic), If an opto input is assigned in the PSL, the autoreclose close command will be verified by an external check synchronism device. The input is energised when the Check Sync conditions are met.	PSL (IN) Autorecloser
1046	External Trip A	Phase A trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip A (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1047	External Trip B	Phase B trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip B (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1048	External Trip C	Phase C trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip C (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
428	F Inhib	Frequency Inhibition	PSL
176	F out of Range	Frequency tracking does not work correctly (provides a Frequency Out-of-Range indication)	PSL (OUT)
187	F.F. Lock	Excessive Fault Frequency CB Trip pre lockout Alarm (maximum number of fault): An alarm is issued at (n) value in the counters of Main lock out or Fault frequency	PSL (OUT) CB monitoring
186	F.F. Pre Lockout	Excessive Fault Frequency CB Trip lockout Alarm (maximum number of fault): An alarm is issued at (n-1) value in the counters of Main lock out or Fault frequency	PSL (OUT) CB monitoring
416	F<1 Start	Underfrequency stage 1 start	PSL
1100	F<1 Timer Block	Timer block underfrequency stage 1	PSL (IN)
422	F<1 Trip	Underfrequency stage 1 trip	PSL
417	F<2 Start	Underfrequency stage 2 start	PSL
1101	F<2 Timer Block	Timer block underfrequency stage 2	PSL (IN)
423	F<2 Trip	Underfrequency stage 2 trip	PSL
418	F<3 Start	Underfrequency stage 3 start	PSL
1102	F<3 Timer Block	Timer block underfrequency stage 3	PSL (IN)
424	F<3 Trip	Underfrequency stage 3 trip	PSL
419	F<4 Start	Underfrequency stage 4 start	PSL
1103	F<4 Timer Block	Timer block underfrequency stage 4	PSL (IN)

Ordinal	English Text	Description	Source
425	F<4 Trip	Underfrequency stage 4 trip	PSL
420	F>1 Start	Overfrequency stage 1 start	PSL
1104	F>1 Timer Block	Timer block overfrequency stage 1	PSL (IN)
426	F>1 Trip	Overfrequency stage 1 trip	PSL
421	F>2 Start	Overfrequency stage 2 start	PSL
1105	F>2 Timer Block	Timer block overfrequency stage 2	PSL (IN)
427	F>2 Trip	Overfrequency stage 2 trip	PSL
468	Fault_REC_TRIG	Trigger for Fault Recorder	FRT
470	Field Volt Fail	Field voltage failure (the internal 48 Vdc delivered by the relay can be used for opto input polarisation)	PSL(OUT)
781	FnKey LED 1 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 1 Green - This LED is associated with Function Key 1 - To drive function key LED, yellow DDB 780 and DDB 782 must be active at the same time	PSL
780	FnKey LED 1 Red	Hardware version K - Assignment of signal to drive output Function Key LED 1 Red - This LED is associated with Function Key 1	PSL
799	FnKey LED 10 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 10 Green	PSL
798	FnKey LED 10 Red	Hardware version K - Assignment of signal to drive output Function Key LED 10 Red	PSL
783	FnKey LED 2 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 2 Green	PSL
782	FnKey LED 2 Red	Hardware version K - Assignment of signal to drive output Function Key LED 2 Red	PSL
785	FnKey LED 3 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 3 Green	PSL
784	FnKey LED 3 Red	Hardware version K - Assignment of signal to drive output Function Key LED 3 Red	PSL
787	FnKey LED 4 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 4 Green	PSL
786	FnKey LED 4 Red	Hardware version K - Assignment of signal to drive output Function Key LED 4 Red	PSL
789	FnKey LED 5 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 5 Green	PSL
788	FnKey LED 5 Red	Hardware version K - Assignment of signal to drive output Function Key LED 5 Red	PSL
791	FnKey LED 6 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 6 Green	PSL
790	FnKey LED 6 Red	Hardware version K - Assignment of signal to drive output Function Key LED 6 Red	PSL
793	FnKey LED 7 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 7 Green	PSL
792	FnKey LED 7 Red	Hardware version K - Assignment of signal to drive output Function Key LED 7 Red	PSL
795	FnKey LED 8 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 8 Green	PSL
794	FnKey LED 8 Red	Hardware version K - Assignment of signal to drive output Function Key LED 8 Red	PSL
797	FnKey LED 9 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 9 Green	PSL
796	FnKey LED 9 Red	Hardware version K - Assignment of signal to drive output Function Key LED 9 Red	PSL

Ordinal	English Text	Description	Source
1042	Force 3P Trip	Three pole tripping only: If it is assigned to an opto input in the PSL and energised, the DDB:'Force 3P Trip' signal will force the internal single-phase protection to trip three-poles (external order from Main1 to Main2 (P44x)) – the next trip will be three-pole.	PSL (IN)
676	Function Key 1	Hardware version K - Programmable Function key n° 1. In 'Normal' mode it is high on key press and in 'Toggle' mode remains high/low on single key press	SW
677 to 685	Function Key 2 to Function Key 10	Hardware version K - Function key n° 2 to Function key n° 10	SW
174	General Alarm	Groupment of all alarms	PSL (OUT)
472	GOOSE IED Absent	Absence of GOOSE message from dedicated IED	PSL(OUT)
1034	I A/R 1p In Prog	One-pole external autoreclose cycle in progress: If it is assigned to an opto input in the PSL and energised, The DDB:'A/R 1P in Prog' will block the internal DEF protection as it indicates that an external single-pole autoreclose cycle is in progress.	PSL (IN) Autorecloser
1035	I A/R 3p In Pr.	Three-pole external autoreclose cycle in progress: If it is assigned to an opto input in the PSL and energised, the DDB:'A/R 3P in Prog' will inform the P44x about the presence of an external 3P cycle. The data is useful in the case of an evolving fault.	PSL (IN) Autorecloser
1036	I A/R Close	Circuit Breaker closing order from external autoreclose: If it is assigned to an opto input in the PSL and energised, the DDB:'A/R Close' can be linked with the internal check synchronism condition to verify the external CB close command.	PSL (IN) Autorecloser
1037	I A/R Reclaim	External (opto input) autorecloser in progress: the DDB:'I A/R Reclaim' signal will inform the protection that an external reclaim time is in progress and will initiate the internal TOR logic (it is possible to create a dedicated PSL which would make it possible to use this information extension in Zone 1 extension schemes).	PSL (IN) Autorecloser
181	I^ Lockout Alarm	Broken current lockout alarm (2nd level): An alarm Lock Out is issued when the maximum broken current (2nd level) calculated by the monitoring function is reached	PSL (OUT) CB monitoring
180	I^ Maint Alarm	Broken current maintenance alarm (1st level): An alarm maintenance is issued when the maximum broken current (1st level) calculated by the CB monitoring function is reached (see setting: 'CB monitor setup / I^ Maintenance')	PSL (OUT) CB monitoring
1106	I<1 Block	Block phase undercurrent stage 1	PSL (IN)
429	I<1 Start	Undercurrent stage 1 start	PSL
1108	I<1 Timer Block	Timer block phase undercurrent stage 1	PSL (IN)
431	I<1 Trip	Undercurrent stage 1 trip	PSL
1107	I<2 Block	Block phase undercurrent stage 2	PSL (IN)
430	I<2 Start	Undercurrent stage 2 start	PSL
1109	I<2 Timer Block	Timer block phase undercurrent stage 2	PSL (IN)
432	I<2 Trip	Undercurrent stage 1 trip	PSL
301	I> Start Any A	Any overcurrent start for phase A	PSL (OUT) Phase Overc.
302	I> Start Any B	Any overcurrent start for phase B	PSL (OUT) Phase Overc.
303	I> Start Any C	Any overcurrent start for phase C	PSL (OUT) Phase Overc.

Ordinal	English Text	Description	Source
304	I>1 Start	Overcurrent stage 1 start Directional or not - with DT or IDMT curves Directional managed by Delta Algorithms VTS Block time-delay facility	PSL (OUT) Phase Overc.
1061	I>1 Timer Block	Block phase overcurrent stage 1 time delay Set to 1: 'I>1 Time Delay' will be blocked & I>1 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>1
308	I>1 Trip	Overcurrent stage 1 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>1 Trip command	PSL (OUT) Phase Overc.
305	I>2 Start	Overcurrent stage 2 start Directional or not - with DT or IDMT curves Directional managed by Delta Algorithms VTS Block time-delay facility	PSL (OUT) Phase Overc.
1062	I>2 Timer Block	Block phase overcurrent stage 2 time delay Set to 1: 'I>2 Time Delay' will be blocked & I>2 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>2
309	I>2 Trip	Overcurrent stage 2 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>2 Trip command	PSL (OUT) Phase Overc.
306	I>3 Start	Overcurrent stage 3 start Non-directional with DT curves Use without time-delay for SOTF	PSL (OUT) Phase Overc.
1063	I>3 Timer Block	Block phase overcurrent stage 3 time delay Set to 1: 'I>3 Time Delay' will be blocked & I>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>3
310	I>3 Trip	Overcurrent stage 3 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>3 Trip command	PSL (OUT) Phase Overc.
307	I>4 Start	Overcurrent stage 4 start Non-directional with DT curves Use without time-delay for SOTF	PSL (OUT) Phase Overc.
1064	I>4 Timer Block	Block phase overcurrent stage 4 time delay Set to 1: 'I>4 Time Delay' will be blocked & I>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>4
311	I>4 Trip	Overcurrent stage 4 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>4 Trip command	PSL (OUT) Phase Overc.
299	I2> Start	Negative Sequence Current Detection – Start function (the associated time-delay picks up) Directional or not - with DT curves Negative-sequence polarisation	PSL (OUT) Neg Seq. O/C
300	I2> Trip	Negative Sequence Current Trip – 3P trip command issued when the associated time-delay has elapsed	PSL (OUT) Neg Seq. O/C
1065	I2>1 Timer Block	Block negative sequence overcurrent stage 1 time delay	PSL (IN) I>4
383	I2>2 Start	Negative overcurrent stage 2 pick-up	PSL
1066	I2>2 Timer Block	Block negative sequence overcurrent stage 2 time delay	PSL (IN) I>5

Ordinal	English Text	Description	Source
386	I2>2 Trip	Negative overcurrent stage 2 trip	PSL
384	I2>3 Start	Negative overcurrent stage 3 pick-up	PSL
1067	I2>3 Timer Block	Block negative sequence overcurrent stage 3 time delay	PSL (IN) I>6
387	I2>3 Trip	Negative overcurrent stage 3 trip	PSL
385	I2>4 Start	Negative overcurrent stage 4 pick-up	PSL
1068	I2>4 Timer Block	Block negative sequence overcurrent stage 4 time delay	PSL (IN) I>7
388	I2>4 Trip	Negative overcurrent stage 4 trip	PSL
485	IM Channel Fail	InterMiCOM message channel fail	PSL(OUT)
484	IM Data CD Fail	InterMiCOM data channel detect fail	PSL(OUT)
482	IM Loopback	InterMiCOM indication that loopback testing is in progress	PSL(OUT)
483	IM Message Fail	InterMiCOM message failure alarm	PSL(OUT)
283	IN>1 Start	Earth fault stage 1 start – Start function (the associated time-delay picks up) Directional or not - with DT or IDMT curves Negative or positive sequence polarization Set to 0: Reset with IN below the threshold IN>1 Hysteresis	PSL (OUT) Earth Fault 1
1056	IN>1 Timer Block	Block earth fault stage 1 time delay Set to 1: 'IN>1 Time Delay' will be blocked & IN>1 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
281	IN>1 Trip	Earth fault stage 1 trip – 3-pole trip command issued when the associated time-delay has elapsed	PSL (OUT) Earth Fault 1
284	IN>2 Start	Earth fault stage 2 start – Start function (the associated time-delay picks up) Directional or not - with DT or IDMT curves Negative or positive sequence polarization Set to 0: Reset with IN below the threshold IN>2 Hysteresis	PSL (OUT) Earth Fault 2
1057	IN>2 Timer Block	Block earth fault stage 2 time delay Set to 1: 'IN>2 Time Delay' will be blocked & IN>2 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
282	IN>2 Trip	Earth fault stage 2 trip – 3-pole trip command issued when the associated time-delay has elapsed Default PSL: Relay 09.	PSL (OUT) Earth Fault 2
357	IN>3 Start	Start of IN>3 function (timer initiated)	PSL (OUT)
1058	IN>3 Timer Block	Block earth fault stage 3 time delay Set to 1: 'IN>3 Time Delay' will be blocked & IN>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
355	IN>3 Trip	Trip decision from IN>3 function (timer issued) Default PSL: Relay 09	PSL (OUT)
358	IN>4 Start	Start of IN>4 function (timer initiated)	PSL (OUT)
1059	IN>4 Timer Block	Block earth fault stage 4 time delay Set to 1: The IN>4 time-delay will be blocked & IN>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
356	IN>4 Trip	Trip decision from IN>4 function (timer issued)	PSL (OUT)

Ordinal	English Text	Description	Source
576	InterMiCOM in 1	InterMiCOM IM1 Signal Input - is driven by a message from the remote line end	SW
577 to 583	InterMiCOM in 2 to InterMiCOM in 8	InterMiCOM IM2 Signal Input to InterMiCOM IM8 Signal Input	SW
584	InterMiCOM out 1	InterMiCOM IM1 Signal output - mapping what will be sent to the remote line end	PSL
585 to 591	InterMiCOM out 2 to InterMiCOM out 8	InterMiCOM IM2 Signal output to InterMiCOM IM8 Signal output	PSL
481	IP Addr Conflict	Ethernet IP Address Conflict alarm	PSL(OUT)
640	LED 1	Hardware version J - Programmable LED n° 1 is energized.	SW
641	LED 1 Grn	Hardware version K - Programmable Green LED n° 1 is energized ANY TRIP A in the default PSL	SW
765	LED 1 Grn Condit	Hardware version K - Assignment of signal to drive output LED 1 green	PSL
640	LED 1 Red	Hardware version K - Programmable Red LED n° 1 is energized. ANY TRIP A in the default PSL	SW
764	LED 1 Red Condit	Hardware version K - Assignment of signal to drive output LED 1 red - To drive LED1 Yellow DDB 764 and DDB 765 must be driven at the same time	PSL
659	LED 10 Grn	Hardware version K - Programmable Green LED n° 10	SW
658	LED 10 Red	Hardware version K - Programmable Red LED n° 10	SW
661	LED 11 Grn	Hardware version K - Programmable Green LED n° 11	SW
660	LED 11 Red	Hardware version K - Programmable Red LED n° 11	SW
663	LED 12 Grn	Hardware version K - Programmable Green LED n° 12	SW
662	LED 12 Red	Hardware version K - Programmable Red LED n° 12	SW
665	LED 13 Grn	Hardware version K - Programmable Green LED n° 13	SW
664	LED 13 Red	Hardware version K - Programmable Red LED n° 13	SW
667	LED 14 Grn	Hardware version K - Programmable Green LED n° 14	SW
666	LED 14 Red	Hardware version K - Programmable Red LED n° 14	SW
669	LED 15 Grn	Hardware version K - Programmable Green LED n° 15	SW
668	LED 15 Red	Hardware version K - Programmable Red LED n° 15	SW
671	LED 16 Grn	Hardware version K - Programmable Green LED n° 16	SW
670	LED 16 Red	Hardware version K - Programmable Red LED n° 16	SW
673	LED 17 Grn	Hardware version K - Programmable Green LED n° 17	SW
672	LED 17 Red	Hardware version K - Programmable Red LED n° 17	SW
675	LED 18 Grn	Hardware version K - Programmable Green LED n° 18	SW
674	LED 18 Red	Hardware version K - Programmable Red LED n° 18	SW
641	LED 2	Hardware version J - Programmable LED n° 2 is energized.	SW
643	LED 2 Grn	Hardware version K - Programmable Green LED n° 2 is energized ANY TRIP B in the default PSL	SW
767	LED 2 Grn Condit	Hardware version K - Assignment of signal to drive output LED 2 green	PSL
642	LED 2 Red	Hardware version K - Programmable Red LED n° 2 is energized ANY TRIP B in the default PSL	SW
766	LED 2 Red Condit	Hardware version K - Assignment of signal to drive output LED 2 red	PSL
642	LED 3	Hardware version J - Programmable LED n° 3 is energized.	SW

Ordinal	English Text	Description	Source
645	LED 3 Grn	Hardware version K - Programmable Green LED n° 3 ANY TRIP C in the default PSL	SW
769	LED 3 Grn Condit	Hardware version K - Assignment of signal to drive output LED 3 green	PSL
644	LED 3 Red	Hardware version K - Programmable Red LED n° 3 ANY TRIP C in the default PSL	SW
768	LED 3 Red Condit	Hardware version K - Assignment of signal to drive output LED 3 red	PSL
643	LED 4	Hardware version J - Programmable LED n° 4 is energized.	SW
647	LED 4 Grn	Hardware version K - Programmable Green LED n° 4 General Start in the default PSL	SW
771	LED 4 Grn Condit	Hardware version K - Assignment of signal to drive output LED 4 green	PSL
646	LED 4 Red	Hardware version K - Programmable Red LED n° 4 General Start in the default PSL	SW
770	LED 4 Red Condit	Hardware version K - Assignment of signal to drive output LED 4 red	PSL
644	LED 5	Hardware version J - Programmable LED n° 5 is energized.	SW
649	LED 5 Grn	Hardware version K - Programmable Green LED n° 5 Z1+Aided Trip in the default PSL	SW
773	LED 5 Grn Condit	Hardware version K - Assignment of signal to drive output LED 5 green	PSL
648	LED 5 Red	Hardware version K - Programmable Red LED n° 5 Z1+Aided Trip in the default PSL	SW
772	LED 5 Red Condit	Hardware version K - Assignment of signal to drive output LED 5 red	PSL
645	LED 6	Hardware version J - Programmable LED n° 6 is energized.	SW
651	LED 6 Grn	Hardware version K - Programmable Green LED n° 6 Dist Fwd in the default PSL	SW
775	LED 6 Grn Condit	Hardware version K - Assignment of signal to drive output LED 6 green	PSL
650	LED 6 Red	Hardware version K - Programmable Red LED n° 6 Dist Fwd in the default PSL	SW
774	LED 6 Red Condit	Hardware version K - Assignment of signal to drive output LED 6 red	PSL
646	LED 7	Hardware version J - Programmable LED n° 7 is energized.	SW
653	LED 7 Grn	Hardware version K - Programmable Green LED n° 7 Dist Rev in the default PSL	SW
777	LED 7 Grn Condit	Hardware version K - Assignment of signal to drive output LED 7 green	PSL
652	LED 7 Red	Hardware version K - Programmable Red LED n° 7 Dist Rev in the default PSL	SW
776	LED 7 Red Condit	Hardware version K - Assignment of signal to drive output LED 7 red	PSL
647	LED 8	Hardware version J - Programmable LED n° 8 is energized.	PSL
655	LED 8 Grn	Hardware version K - Programmable Green LED n° 8 Autoreclose Enable in the default PSL	SW
779	LED 8 Grn Condit	Hardware version K - Assignment of signal to drive output LED 8 green	PSL
654	LED 8 Red	Hardware version K - Programmable Red LED n° 8 Autoreclose Enable in the default PSL	SW

Ordinal	English Text	Description	Source
778	LED 8 Red Condit	Hardware version K - Assignment of signal to drive output LED 8 red	PSL
657	LED 9 Grn	Hardware version K - Programmable Green LED n° 9	SW
656	LED 9 Red	Hardware version K - Programmable Red LED n° 9	SW
656	LED Cond IN 1	Hardware version J - Assignment of signal to drive output Function Key LED 1	PSL
657	LED Cond IN 2	Hardware version J - Assignment of signal to drive output Function Key LED 2	PSL
658	LED Cond IN 3	Hardware version J - Assignment of signal to drive output Function Key LED 3	PSL
659	LED Cond IN 4	Hardware version J - Assignment of signal to drive output Function Key LED 4	PSL
660	LED Cond IN 5	Hardware version J - Assignment of signal to drive output Function Key LED 5	PSL
661	LED Cond IN 6	Hardware version J - Assignment of signal to drive output Function Key LED 6	PSL
662	LED Cond IN 7	Hardware version J - Assignment of signal to drive output Function Key LED 6	PSL
663	LED Cond IN 8	Hardware version J - Assignment of signal to drive output Function Key LED 7	PSL
1672 to 1677	LN1 Analog Alarm to LN6 Analog Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL
1688 to 1693	LN1 Async to LN6 Async	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is synchronized with Internal (local) synchronization	PSL
1680 to 1685	LN1 Test Mode to LN6 Test Mode	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is in “Test Mode”	PSL
1704 to 1709	LN1 Val Fail to LN6 Val Fail	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “failed”	PSL
1696 to 1701	LN1 Val Quest to LN6 Val Quest	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “questionable”	PSL
188	Lockout Alarm	Lockout alarm: An alarm is issued with: ‘Man CB Unhealthy’or no 'Check Sync OK' (CB conditioning) or ‘Man CB Cls Fail’ or ‘Man CB Fail Trip’ or 'F.F. Lock' or 'CB Op Time Lock' or 'CB Ops Lockout'	PSL (OUT)
331	Loss. Load Trip	Loss of load trip (in application without communication scheme and a 3P Trip logic)	PSL (OUT) Loss of load
191	Man CB Cls Fail	Alarm CB fail for manual closing command	PSL (OUT)
190	Man CB Trip Fail	Alarm CB Fail for manual trip command	PSL (OUT)
192	Man CB Unhealthy	Alarm CB performed by unhealthy condition	PSL (OUT)

Ordinal	English Text	Description	Source
1043	Man. Close CB	Circuit breaker manual close - order received. 'If it is assigned to an opto input in the PSL and energised the DDB:'Man Close CB' signal will enable the internal 'SOTF Enable' logic without CB control activation. If CB control is activated, SOTF will be enabled by internal detection ('CB close' order managed by CB control). Manual closure of the circuit breaker will force the autorecloser in a lockout logic, if selected in the 'Distance schemes / TOR-SOTF Mode') menu. Any fault detected within 500ms of a manual closure will cause an instantaneous three pole tripping, without autoreclose (see Block Autoreclose (BAR) logic) When autoreclose lockout (BAR) is activated, the autorecloser does not initiate any additional reclosing cycle. If autoreclose lockout picks up during a cycle, the A/R close is blocked. This prevents excessive circuit breaker operations, which could result in increased circuit breaker and system damage, when closing onto a fault.	PSL (IN) CB Status
1044	Man. Trip CB	Circuit breaker manual trip - order received. If it is assigned to an opto input in the PSL and energised, the DDB:'Man Trip CB' signal will inform the protection of an external CB trip command by the CB control function (if activated).	PSL (IN) CB Status
1055	MCB/VTS Main	Fuse failure on line VT or MCB open (blocks voltage dependant functions). If it is linked to an opto input in the PSL energised, the DDB informs the P44x about an internal maloperation from the VT used for the impedance measurement reference (line in this case means Main VT ref measurement, even if the main VT is on the bus side and the Synchronism check VT is on the line side).	PSL (IN) VTS
1054	MCB/VTS Synchro	Fuse failure on busbar VT or MCB open (blocks voltage dependant functions), If it is linked to an opto input in the PSL and energised, the DDB signal informs the P44x about an internal maloperation from the VT used for synchronisation check (see Check Synchronism logic section).	PSL (IN) VTS
204	NCIT Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) IEC 61850 9-2 Alarm - Frame from Merge Units missing. If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL (OUT)
475	NIC Fatal Error	Fatal Error from Ethernet Board alarm	PSL(OUT)
479	NIC Link Fail	Ethernet Link Fail alarm	PSL(OUT)
474	NIC No Response	No response from Ethernet Board alarm.	PSL(OUT)
473	NIC Not Fitted	Ethernet (board not fitted) alarm	PSL(OUT)
1114	NIC Read Only	All setting changes and most command/control actions blocked for the Ethernet port (when option available).	PSL
476	NIC Soft. Reload	Ethernet Board (Configuration in progress) alarm	PSL(OUT)
480	NIC SW Mis-Match	Not compatible Ethernet version alarm	PSL(OUT)

Ordinal	English Text	Description	Source
64	Opto Label 01	OPTO ISOLATOR 1 Set to 1 when the opto input is energised for a minimum time: 7ms (48Vdc), 10ms (universal) to be validated by internal logic To enable the selection of a setting group by state change of the opto isolated logic inputs 1 and 2, disconnect Opto inputs 01 and 02 in the PSL (Opto inputs 01 and 02 must not be connected to any output signal)	OPTO
65	Opto Label 02	OPTO ISOLATOR 2 Set to 1 when the opto input is energised for a minimum time: 7ms (48Vdc), 10ms (universal) to be validated by internal logic To enable the selection of a setting group by state change of the opto isolated logic inputs 1 and 2, disconnect Opto inputs 01 and 02 in the PSL (Opto inputs 01 and 02 must not be connected to any output signal)	OPTO
66 to 95	Opto Label 03 to Opto Label 32	OPTO ISOLATOR 3 to OPTO ISOLATOR 32 Set to 1 when the opto input is energised for a minimum time:7ms (48Vdc), 10ms (universal) to be validated by internal logic	OPTO
350	Out Of Step	Start of an Out of Step Detection (1st cycle), The first out of step cycle has been detected (Zlocus in/out with the opposite R sign) & the « Out Of Step start » picks-up	PSL (OUT)
352	Out Of Step Conf	Out of Step Confirmed (number of cycles reached)	PSL (OUT)
700 to 763	Output cond. 1 to Output cond. 64	Input to Relay Output Conditioner	PSL
367	PAP Pre Start	PAP (specific application) Picks up by voltage detectors (timer initiated)	PSL (OUT)
366	PAP Pres IN	Residual current detected by PAP (specific application) function	PSL (OUT)
363	PAP Start A	Phase A Start with PAP (specific application) function	PSL (OUT)
364	PAP Start B	Phase B Start with PAP (specific application) function	PSL (OUT)
365	PAP Start C	Phase C Start with PAP (specific application) function	PSL (OUT)
1089	PAP TeleT. Heath	PAP (specific application) Carrier Out of Service (DT trip decision)	PSL(IN)
1088	PAP TeleTrip CR	PAP (specific application) Carrier Receive for teletransmission	PSL(IN)
1090	PAP Timer Block	Timer Block for frozen every timer initiated with PAP (specific application) function	PSL(IN)
359	PAP Trip A	Trip A Phase decision from PAP (specific application) function	PSL (OUT)
360	PAP Trip B	Trip B Phase decision from PAP (specific application) function	PSL (OUT)
361	PAP Trip C	Trip C Phase decision from PAP (specific application) function	PSL (OUT)
362	PAP Trip IN	Trip decision from PAP (specific application) function (Ground Fault detected)	PSL (OUT)
269	Power Swing	Power swing detected (3 single phase loop inside the quad & crossing the ΔR band in less than 5ms in a 50 Hz network). Power swing is present either with out of step cycle or stable swing cycle.	PSL (OUT) Distance
175	Prot'n Disabled	Protection is disabled and test mode enabled	PSL (OUT)
1480 to 1543	PubPres VIP 1 to PubPres VIP 64	Publishing presence of virtual input 1 (to 64): indicates virtual input 1 (to 64) presence.	PSL
1353 to 1415	Quality VIP 1 to Quality VIP 64	Validation of the virtual input 1 (to 64) (signal correct).	PSL

Ordinal	English Text	Description	Source
0 to 63	Relay Label 01 to Relay Label 64	OUTPUT RELAY 1 to OUTPUT RELAY 64 High level when a DDB cell (linked by PSL logic) is at 1. State depends on the logic set in the PSL (MiCOM S1 Agile) These programmable relays are assigned in the default PSL, with the following logic conditions (see section 1.8.2): - Pulse time-delay - Pick Up/Drop Off Time-delay - Dwell Time-delay - Pick Up Time-delay - Drop Off Time-delay - Latching - Straight (used in default PSL)	RELAY
1081	Reset All values	Reset all values of CB monitoring (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1082	Reset Latches	Reset all permanent alarms + LEDs and relays are latched	PSl (IN)
1080	Reset Lockout	Reset all CB monitoring lockout (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1091	Reset Thermal	Reset Thermal Overload Protection	PSL(IN)
270	Reversal Guard	Current reversal guard logic in action (Directional switching from Rev to Fwd in parallel line application)	PSL (OUT) Distance
1112	RP1 Read Only	All setting changes and most command/control actions blocked for Rear Port 1.	PSL
1113	RP2 Read Only	All setting changes and most command/control actions blocked for Rear Port 2.	PSL
351	S. Swing	Start of Stable Swing (1st cycle): The first stable swing cycle has been detected (Zlocus in/out with the same R sign) & the « Stable Swing start » picks-up	PSL (OUT)
353	S. Swing Conf	Stable Swing confirmed (number of cycles reached)	PSL (OUT)
437	SBO Closed Org 1	Select Before Operate (SBO) closing function for organ 1 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
438	SBO Closed Org 2	Select Before Operate (SBO) closing function for organ 2 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
439	SBO Closed Org 3	Select Before Operate (SBO) closing function for organ 3 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
440	SBO Closed Org 4	Select Before Operate (SBO) closing function for organ 4 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
1118	SBO Command1	SBO support for IEC 61850-8-1 function command 1	PSL
1122	SBO Command2	SBO support for IEC 61850-8-1 function command 2.	PSL
1126	SBO Command3	SBO support for IEC 61850-8-1 function command 3	PSL
1130	SBO Command4	SBO support for IEC 61850-8-1 function command 4.	PSL
1116	SBO DPI1 Org1	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 1	PSL
1120	SBO DPI1 Org2	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 2	PSL
1124	SBO DPI1 Org3	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 3	PSL
1128	SBO DPI1 Org4	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 4	PSL
1117	SBO DPI2 Org1	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 1	PSL
1121	SBO DPI2 Org2	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 2	PSL

Ordinal	English Text	Description	Source
1125	SBO DPI2 Org3	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 3	PSL
1129	SBO DPI2 Org4	SBO support for IEC61850-8-1 function SBO Double Point Information 2 Organe 4	PSL
1115	SBO InterLock 1	SBO support for IEC 61850-8-1 control function with interlocking facilities 1	PSL
1119	SBO InterLock 2	SBO support for IEC 61850-8-1 control function with interlocking facilities 2	PSL
1123	SBO InterLock 3	SBO support for IEC 61850-8-1 control function with interlocking facilities 3	PSL
1127	SBO InterLock 4	SBO support for IEC61850-8-1 control function with interlocking facilities 4	PSL
433	SBO Open Org 1	Select Before Operate (SBO) opening function for organ 1 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
434	SBO Open Org 2	Select Before Operate (SBO) opening function for organ 2 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
435	SBO Open Org 3	Select Before Operate (SBO) opening function for organ 3 (interlocking facility in the IEC60870-5-103 protocol)	PSL
436	SBO Open Org 4	Select Before Operate (SBO) opening function for organ 4 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
1093	Select CS(NCIT)	Select Check synchro for NCIT	PSL
195	SG-opto Invalid	Setting group (selected via opto inputs 1 & 2) invalid	PSL (OUT)
312	SOTF Enable	Switch On To Fault enabled: Indicates the SOTF logic is enabled in the relay Set to 1 = [SOTF not disabled (Setting 'Distance schemes / TOR-SOTF Mode')] AND [{ All poles dead AND (SOTF time-delay elapsed (110 s/default)) } OR Input Man Close] OR (CB control & Close in progress)] Reset = 500ms time-delay elapsed after Any pole Dead OR Reset of one condition requested for SOTF enable	PSL (OUT) SOTF
332	SOTF/TOR Trip	Switch on to fault trip or trip on reclose: indicates that a 3-pole trip order has been issued by the TOR or SOTF logic	PSL (OUT) SOTF
1031	SPAR Enable	Enable internal single pole autorecloser. Set with Opto input (if linked by PSL) is energized (> 1s). At 1: 1P AR internal is enabled in the AR logic At 0: AR 1P internal is disabled (even if set in MiCOM S1 Agile). AR logic becomes 3P only with AR 3P cycle -if TPAR =1	PSL (IN) Autorecloser
1083	Stub Bus Enable	Enable I>4 Element for stub bus protection (isolator of HV line open - status isolator must be connected to an opto input)	PSL (IN)
207	Synchro Acq Al.	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x - Any Logical Node is synchronized with external (global) synchronization	PSL (OUT)
261	T1	Distance time-delay in zone 1 tZ1 elapsed (1 = end of timer) If T1=0 picks up when the relay starts (Distance Start or preset)	PSL (OUT) Distance
1094	T1 Timer Block	Timer block T1 input	PSL

Ordinal	English Text	Description	Source
262	T2	Distance time-delay in zone 2 tZ2 elapsed (1 = end of timer)	PSL (OUT) Distance
1095	T2 Timer Block	Timer block T2 input	PSL
263	T3	Distance time-delay in zone 3 tZ3elapsed (1 = end of timer)	PSL (OUT) Distance
1098	T3 Timer Block	Timer block T3 input	PSL
264	T4	Distance time-delay in zone 4 tZ4 elapsed (1 = end of timer)	PSL (OUT) Distance
1099	T4 Timer Block	Timer block T4 input	PSL
333	tBF1 Trip	Circuit Breaker failure on any trip, delayed by "CB Fail 1 Timer" (setting in "CB Fail" logic)	PSL (OUT) Breaker failure
334	tBF2 Trip	Circuit Breaker failure on any trip, delayed by "CB Fail 2 Timer" (setting in "CB Fail" logic)	PSL (OUT) Breaker failure
206	Test Mode Acq	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x - Any Logical Node is in “Test Mode”	PSL (OUT)
369	Thermal Alarm	Alarm from Thermal Overload function picks up	PSL (OUT)
1092	Time Synch	External time synchronisation input	PSL(IN)
830 to 845	Timer in 1 to Timer in 16	Hardware version K - PSL Input to Auxiliary Timer 1 to PSL Input to Auxiliary Timer 16	Auxiliary Timer
830 to 861	Timer in 1 to Timer in 16	Hardware version J - PSL Input to Auxiliary Timer 1 to PSL Input to Auxiliary Timer 32	Auxiliary Timer
862 to 893	Timer in 1 to Timer in 16	Hardware version J - PSL Output from Auxiliary Timer 1 to PSL Output from Auxiliary Timer 32	Auxiliary Timer
846 to 861	Timer out 1 to Timer out 16	Hardware version K - PSL Ouput from Auxiliary Timer 1 PSL Ouput from Auxiliary Timer 16	Auxiliary Timer
314	TOC Start A	Trip on Close start on phase A: indicates a trip order on phase A has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
315	TOC Start B	Trip on Close start on phase B: indicates a trip order on phase B has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
316	TOC Start C	Trip on Close start on phase C: indicates a trip order on phase C has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
313	TOR Enable	Trip On Reclose enable: indicates the TOR logic is activated in the relay Set to 1= 500 ms pulse initiated by: 'I A/R Reclaim' (internal) OR 'A/R reclaim' (External Input) OR Any pole open for more than 200 ms Reset 500 ms after Any pole dead stops	PSL (OUT) TOR
1032	TPAR Enable	Enable internal three pole autorecloser Set with Opto input (if linked by PSL) is energized (> 1s). At 1: 3P AR internal is enabled in the AR logic At 0: AR 3P internal is disabled (even if set in MiCOM S1 Agile). 1P cycle available if SPAR =1	PSL (IN) Autorecloser
368	Trace Trig OK	Triggering trace has operated correctly	PSL (OUT)
1024	Trip LED	LED trip	
370	Trip Thermal	Trip with Thermal Overload fucntion (timer issued)	PSL (OUT)
265	Tzp	Distance time-delay in zone p tZp elapsed (1 = end of timer)	PSL (OUT) Distance
1096	TZp Timer Block	Timer block TZp input	PSL

Ordinal	English Text	Description	Source
395	Tzq	Timer in zone Q elapsed (at 1 = end of timer)	PSL
1097	TZq Timer Block	Timer block TZq input	PSL
1084	User Trip A	Internal input for trip logic A Set to 1: Trip A Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1085	User Trip B	Internal input for trip logic B Set to 1: Trip B Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1086	User Trip C	Internal input for trip logic C Set to 1: Trip C Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
239	V< Dead Bus	Dead Bus: high when the Dead Bus condition is met (voltage below the V<Dead Bus threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
237	V< Dead Line	Dead Line: high when the Dead Line condition is met (voltage below the 'V< Dead Line' threshold value (setting) – The measured voltage is always calculated as a single phase voltage	PSL (OUT) Synchro Check
285	V< Start Any A	Any undervoltage start detected on phase A	PSL (OUT) Undervoltage
286	V< Start Any B	Any undervoltage start detected on phase B	PSL (OUT) Undervoltage
287	V< Start Any C	Any undervoltage start detected on phase C	PSL (OUT) Undervoltage
197	V<1 Alarm	1st stage undervoltage alarm picks up when V<1 starts	PSL (OUT) V<1
288	V<1 Start	Undervoltage 1st stage start (any phase)	PSL (OUT) Undervoltage
371	V<1 Start A	Undervoltage stage 1 pick up on phase A	PSL
372	V<1 Start B	Undervoltage stage 1 pick up on phase B	PSL
373	V<1 Start C	Undervoltage stage 1 pick up on phase C	PSL
1069	V<1 Timer Block	Block phase undervoltage stage 1 time delay Set to 1: 'V<1 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<1
290	V<1 Trip	Undervoltage 1st stage – 3-phase trip	PSL (OUT) Undervoltage
198	V<2 Alarm	2nd stage undervoltage alarm picks up when V<21 starts	PSL (OUT) V<2
289	V<2 Start	Undervoltage 2nd stage start (any phase)	PSL (OUT) Undervoltage
374	V<2 Start A	Undervoltage stage 2 pick up on phase A	PSL
375	V<2 Start B	Undervoltage stage 2 pick up on phase B	PSL
376	V<2 Start C	Undervoltage stage 2 pick up on phase C	PSL
1070	V<2 Timer Block	Block phase undervoltage stage 2 time delay Set to 1: 'V<2 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<2
291	V<2 Trip	Undervoltage stage 2nd stage – 3-phase trip	PSL (OUT) Undervoltage
396	V<3 Start	Undervoltage stage 3 start	PSL

Ordinal	English Text	Description	Source
398	V<3 Start A	Undervoltage phase A stage 3 start	PSL
399	V<3 Start B	Undervoltage phase B stage 3 start	PSL
400	V<3 Start C	Undervoltage phase C stage 3 start	PSL
1071	V<3 Timer Block	Block phase undervoltage stage 3 time delay Set to 1: 'V<3 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<3
404	V<3 Trip	Undervoltage stage 3 trip	PSL
397	V<4 Start	Undervoltage stage 4 start	PSL
401	V<4 Start A	Undervoltage phase A stage 4 start	PSL
402	V<4 Start B	Undervoltage phase B stage 4 start	PSL
403	V<4 Start C	Undervoltage phase C stage 4 start	PSL
1072	V<4 Timer Block	Block phase undervoltage stage 4 time delay Set to 1: 'V<4 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<4
405	V<4 Trip	Undervoltage stage 4 trip	PSL
240	V> Live Bus	Live Bus: high when the Live Bus condition is met (voltage above the V>Live Bus threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
238	V> Live Line	Live Line: high when the Live line condition is met (voltage above the 'V> Live Line' threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
292	V> Start Any A	Any overvoltage start detected on phase A	PSl (OUT) Overvoltage
293	V> Start Any B	Any overvoltage start detected on phase B	PSl (OUT) Overvoltage
294	V> Start Any C	Any overvoltage start detected on phase C	PSl (OUT) Overvoltage
199	V>1 Alarm	1st stage overvoltage alarm picks up when V>1 starts	PSL (OUT) V>1
295	V>1 Start	Overvoltage function 1st stage start for any phase	PSl (OUT) Overvoltage
377	V>1 Start A	Overvoltage stage 1 pick up on phase A	PSL
378	V>1 Start B	Overvoltage stage 1 pick up on phase B	PSL
379	V>1 Start C	Overvoltage stage 1 pick up on phase C	PSL
1073	V>1 Timer Block	Block phase overvoltage stage 1 time delay Set to 1: 'V>1 Time Delay will be blocked and V>1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>1
297	V>1 Trip	Overvoltage 1st stage 3-phase trip	PSl (OUT) Overvoltage
200	V>2 Alarm	2nd stage overvoltage alarm picks up when V>2 starts	PSL (OUT) V>2
296	V>2 Start	Overvoltage function 2nd stage start for any phase	PSl (OUT) Overvoltage
380	V>2 Start A	Overvoltage stage 2 pick up on phase A	PSL
381	V>2 Start B	Overvoltage stage 2 pick up on phase B	PSL
382	V>2 Start C	Overvoltage stage 2 pick up on phase C	PSL

Ordinal	English Text	Description	Source
1074	V>2 Timer Block	Block phase overvoltage stage 2 time delay Set to 1: 'V>2 Time Delay' will be blocked and V>2 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>2
298	V>2 Trip	Overvoltage 2nd stage 3-phase 2 trip	PSI (OUT) Overvoltage
406	V>3 Start	Overvoltage stage 3 start	PSL
408	V>3 Start A	Overvoltage phase A stage 3 start	PSL
409	V>3 Start B	Overvoltage phase B stage 3 start	PSL
410	V>3 Start C	Overvoltage phase C stage 3 start	PSL
1075	V>3 Timer Block	Block phase overvoltage stage 3 time delay Set to 1: 'V>3 Time Delay' will be blocked and V>3 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>3
414	V>3 Trip	Overvoltage stage 3 trip	PSL
407	V>4 Start	Overvoltage stage 4 start	PSL
411	V>4 Start A	Overvoltage phase A stage 4 start	PSL
412	V>4 Start B	Overvoltage phase B stage 4 start	PSL
413	V>4 Start C	Overvoltage phase C stage 4 start	PSL
1076	V>4 Timer Block	Block phase overvoltage stage 4 time delay Set to 1: 'V>4 Time Delay' will be blocked and V>4 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>4
415	V>4 Trip	Overvoltage stage 4 trip	PSL
213	V3< Alarm	Third undervoltage stage Alarm	PSL(IN)
215	V3> Alarm	Third overvoltage stage Alarm	PSL(IN)
214	V4< Alarm	Fourth undervoltage stage Alarm	PSL(IN)
216	V4> Alarm	Fourth overvoltage stage Alarm	PSL(IN)
205	Val/Fail Acq Al.	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x Alarm NCIT (9-2 Ethernet) - Frame from Merge Units failed. Any Logical Node is synchronized with Internal (local) synchronization	PSL (OUT)
1224	Virtual Input 1	Goose input n° 1 - Allows binary signals that are mapped to virtual inputs to interface into PSL	SW
1225 to 1287	Virtual Input 2 to Virtual Input 64	Goose input n° 2 to Goose input n° 32	SW
512	Virtual output 1	Goose output n° 1 - Allows user to control a binary signal which can be mapped via SCADA protocol output to other devices	PSL
513 to 543	Virtual output 2 Virtual output 32	Goose output n° 2 to Goose output n° 32	PSL
389	VN>1 Start	Neutral overvoltage stage 1 pick up	PSL
1077	VN>1 Timer Block	Block earth overvoltage stage 1 time delay	PSL (IN) VN>1
391	VN>1 Trip	Neutral overvoltage stage 1 trip	PSL
390	VN>2 Start	Neutral overvoltage stage 2 pick up	PSL
1078	VN>2 Timer Block	Block earth overvoltage stage 2 time delay	PSL (IN) VN>2
392	VN>2 Trip	Neutral overvoltage stage 2 trip	PSL

Ordinal	English Text	Description	Source
177	VT Fail Alarm	Fuse failure indication (VT alarm). High when the opto input is energised (copy of MCB) OR an internal Fuse Failure is confirmed when the VTS timer elapses.	PSL (OUT) VT Supervision
337	VTS Fast	Instantaneous unconfirmed fuse failure internal detection. Set high for internal Fuse Failure detection made with internal logic.	PSL (OUT) VTS
266	WI Trip A	Phase A trip on weak infeed	PSL (OUT) Distance
267	WI Trip B	Phase B trip on weak infeed	PSL (OUT) Distance
268	WI Trip C	Phase C trip on weak infeed	PSL (OUT) Distance
255	Z1	Fault in zone 1 (convergence of loop in Z1) Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection (default PSL: LED 5, Relays 01 / 10)	PSL (OUT) Distance
349	Z1 Not Filtrated	Z1 decision not filtered by phase selection	PSL (OUT)
256	Z1X	Fault in zone 1 extended Z1x (convergence of loop in Z1x) and filtered by blocking/unblocking Power Swing/Reversal guard logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
1053	Z1X Extension	Zone 1 Extension Input Opto input energized if linked by PSL OR any internal DDB by dedicated PSL At 1: Signal will initiate Z1 extension logic if selected (setting). This DDB can be assigned to any external/Internal condition for starting Z1X logic	PSL (IN)
257	Z2	Fault in zone 2 (convergence of loop in Z2) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
258	Z3	Fault in zone 3 (convergence of loop in Z3) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
259	Z4	Fault in zone 4 (convergence of loop in Z4) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
260	Zp	Fault in zone P Zp (convergence of loop in Zp) logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
394	Zq	Fault in zone Q	PSL
347	ZSP Start	Zero Sequence Power - Start: The ZSP START cell at 1 indicates the Zero Sequence Power function has started - in the same time, it indicates the timer-delays associated have started and are running (fixed one first and then IDMT timer)	PSL (OUT) ZSP
1087	ZSP Timer Block	Zero Sequence Power - Timer Block: If assigned to an opto input in a dedicated PSL, Zero Sequence Power function will start, but will not perform a trip command - the associated time-delay (adjusted with 'K Time Delay Factor ' setting, will be blocked	PSL (IN) ZSP
348	ZSP Trip	Zero Sequence Power - Trip: The ZSP TRIP cell at 1 indicates the Zero Sequence Power function has performed a trip command (after the start and when associated timers are issued)	PSL (OUT) ZSP
454	LBlinder DetectAN	Load Blinder Detection in Loop AN: Cell at 1 indicates the Impedance is located within the AN loop Load Blinder Region.	PSL (OUT) Distance

Ordinal	English Text	Description	Source
455	LBlinder DetectBN	Load Blinder Detection in Loop BN: Cell at 1 indicates the Impedance is located within the BN loop Load Blinder Region.	PSL (OUT) Distance
456	LBlinder DetectCN	Load Blinder Detection in Loop CN: Cell at 1 indicates the Impedance is located within the CN loop Load Blinder Region.	PSL (OUT) Distance
457	LBlinder DetectAB	Load Blinder Detection in Loop AB: Cell at 1 indicates the Impedance is located within the AB loop Load Blinder Region.	PSL (OUT) Distance
458	LBlinder DetectBC	Load Blinder Detection in Loop BC: Cell at 1 indicates the Impedance is located within the BC loop Load Blinder Region.	PSL (OUT) Distance
459	LBlinder DetectCA	Load Blinder Detection in Loop CA: Cell at 1 indicates the Impedance is located within the CA loop Load Blinder Region.	PSL (OUT) Distance
460	LB PowerSwing	Power Swing Detected within Load Blinder Region	PSL (OUT) Distance

1.2 Factory default programmable scheme logic

1.2.1 Logic input mapping

The default mappings for each of the opto-isolated inputs are as shown in the following table (PSL are equivalent for P442 and P444):

Opto Input N°	P442 Relay	P444 Relay
1	Channel Receive (Distance or DEF)	Channel Receive (Distance or DEF)
2	Channel out of Service (Distance or DEF)	Channel out of Service (Distance or DEF)
3	MCB/VTS Main (Z measurement-Dist)	MCB/VTS Main (Z measurement-Dist)
4	Block Autoreclose (BAR) (Lockout)	Block Autoreclose (BAR) (Lockout)
5	Circuit Breaker Healthy	Circuit Breaker Healthy
6	Circuit breaker Manual Close external order	Circuit breaker Manual Close external order
7	Reset Lockout	Reset Lockout
8	Disable Autoreclose (1-pole and 3-pole)	Disable Autoreclose (1-pole and 3-pole)
9	Not allocated	Not allocated
10	Not allocated	Not allocated
11	Not allocated	Not allocated
12	Not allocated	Not allocated
13	Not allocated	Not allocated
14	Not allocated	Not allocated
15	Not allocated	Not allocated
16	Not allocated	Not allocated
17		Not allocated
18		Not allocated
19		Not allocated
20		Not allocated

Opto Input N°	P442 Relay	P444 Relay
21		Not allocated
22		Not allocated
23		Not allocated
24		Not allocated

1.2.2 Relay output contact mapping

The default mappings and conditioning for each of the relay output contacts are shown in the following table (PSL are equivalent for P442/444):

Relay Contact N°	P442 Relay	P444 Relay
1	TripA+B+C & Z1 [straight]	TripA+B+C & Z1 [straight]
2	Any Trip Phase A [straight]	Any Trip Phase A [straight]
3	Any Trip Phase B [straight]	Any Trip Phase B [straight]
4	Any Trip Phase C [straight]	Any Trip Phase C [straight]
5	Signal send (Dist. or DEF) [straight]	Signal send (Dist. or DEF) [straight]
6	Any Protection Start [straight]	Any Protection Start [straight]
7	Any Trip [straight]	Any Trip [straight]
8	General Alarm [straight]	General Alarm [straight]
9	DEF A+B+C Trip + IN>2Trip + IN>3Trip [straight]	DEF A+B+C Trip + IN>2Trip + IN>3Trip [straight]
10	Dist. Trip & Any Zone & Dist Unb CR [straight]	Dist. Trip & Any Zone & Dist Unb CR [straight]
11	Autoreclose lockout [straight]	Autoreclose lockout [straight]
12	Autoreclose 1P + 3P cycle in progress [straight]	Autoreclose 1P + 3P cycle in progress [straight]
13	A/R Close [straight]	A/R Close [straight]
14	Power Swing Detected [straight]	Power Swing Detected [straight]
15	Not allocated	Not allocated
16	Not allocated	Not allocated
17	Not allocated	Not allocated
18	Not allocated	Not allocated
19	Not allocated	Not allocated
20	Not allocated	Not allocated
21	Not allocated	Not allocated
22	Not allocated	Not allocated
23		Not allocated
24		Not allocated
25		Not allocated
26		Not allocated
27		Not allocated
28		Not allocated
29		Not allocated
30		Not allocated
31		Not allocated

Relay Contact N°	P442 Relay	P444 Relay
32		Not allocated

Note: When 3-pole tripping mode is selected in the menu 'Distance Schemes / Trip mode', all the relay contacts connected to a trip (trip A, trip B, trip C, and Any Trip) close simultaneously.

The following relay logic conditions (time-delays, straight condition) can be used to set the PSL relay design:

- Pulse Timer
- Pick UP/Drop Off Timer
- Dwell Timer
- Pick Up Timer
- Drop Off Timer
- Latching
- Straight (transparent)

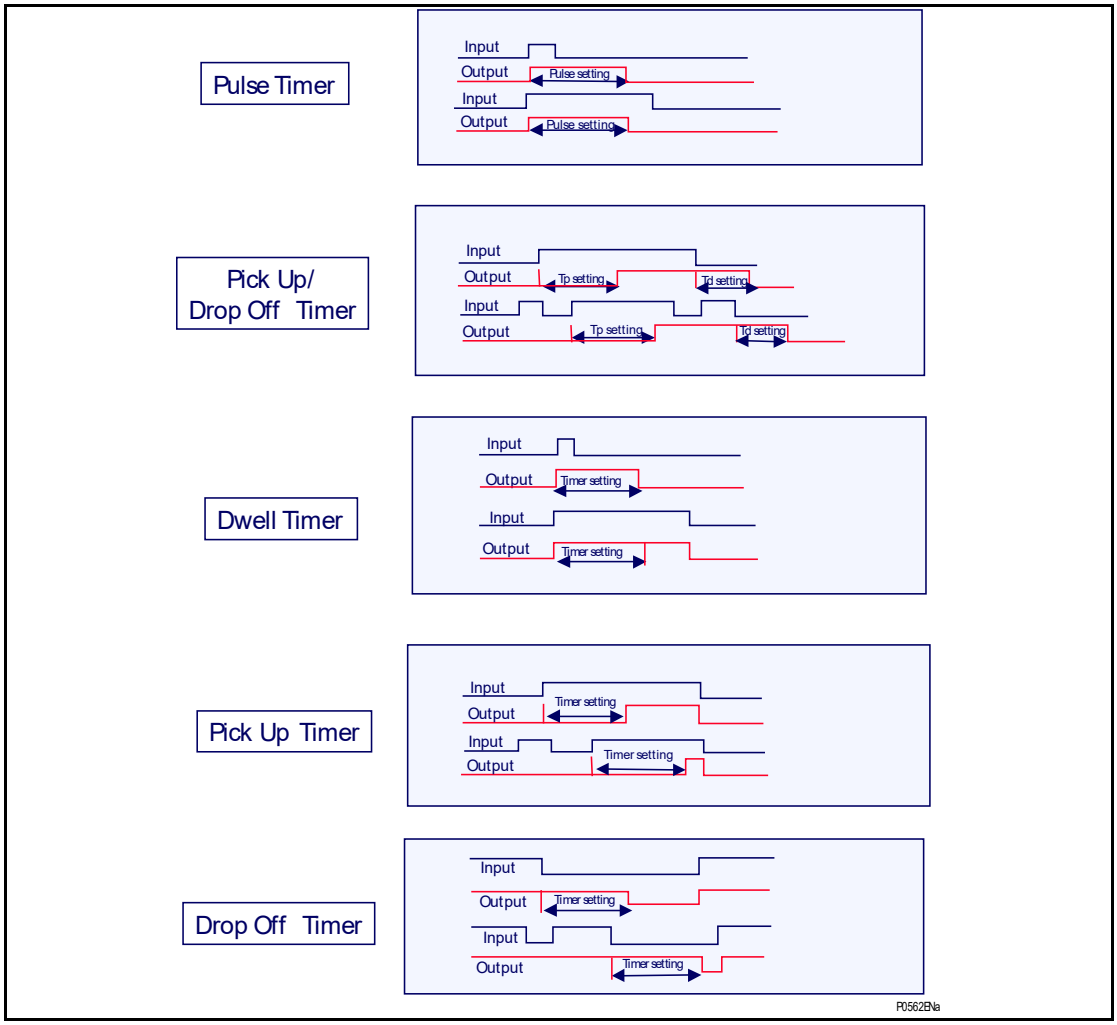


Figure 1: Time-delay definition in psl

1.2.3 Programmable LED output mapping

The default mappings for each of the programmable LEDs are as shown in the following table:

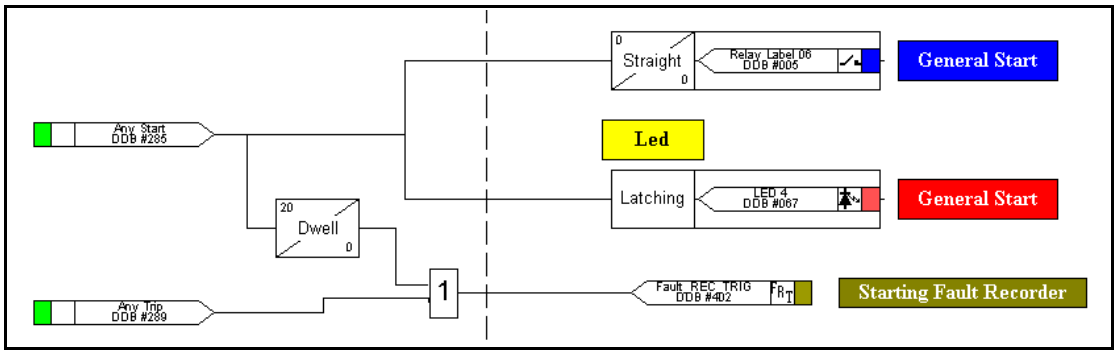
LED No.	P442 Relay	P444 Relay
1	Any Trip A	Any Trip A
2	Any Trip B	Any Trip B
3	Any Trip C	Any Trip C
4	Any Start	Any Start
5	Z1+Aided Trip	Z1+Aided Trip
6	Dist Fwd	Dist Fwd
7	Dist Rev	Dist Rev
8	A/R Enable	A/R Enable

Note: All the LEDs are latched in the default PSL.

1.2.4 Fault recorder trigger

The default PSL trigger which initiates a fault record is shown in the following table:

P442 Relay	P444 Relay
Any Start	Any Start
Any Trip	Any Trip



If the fault recorder trigger is not assigned in the PSL, no Fault recorder can be initiated and displayed in the list by the LCD front panel.

2 MICOM PX40 IEC 61850 IED CONFIGURATOR

IEC 61850 is a substation communications standard. It standardizes the way data is transferred to and from IEC 61850 compliant IEDs, making the communication independent of the manufacturer. This makes it easier to connect different manufacturers' products together and simplifies wiring and network changes.

The IEC 61850 Configurator tool is used to configure the IEC 61850 settings of MiCOM IEDs, not the protection settings. It also allows you to extract a configuration file so you can view, check and modify the IEC 61850 settings during precommissioning.

Further information is available in the Help system and in the Settings Application Software Guide P40-M&CR-UG-EN-n, where n is the latest version of the settings application software.

3 GOOSE EDITOR

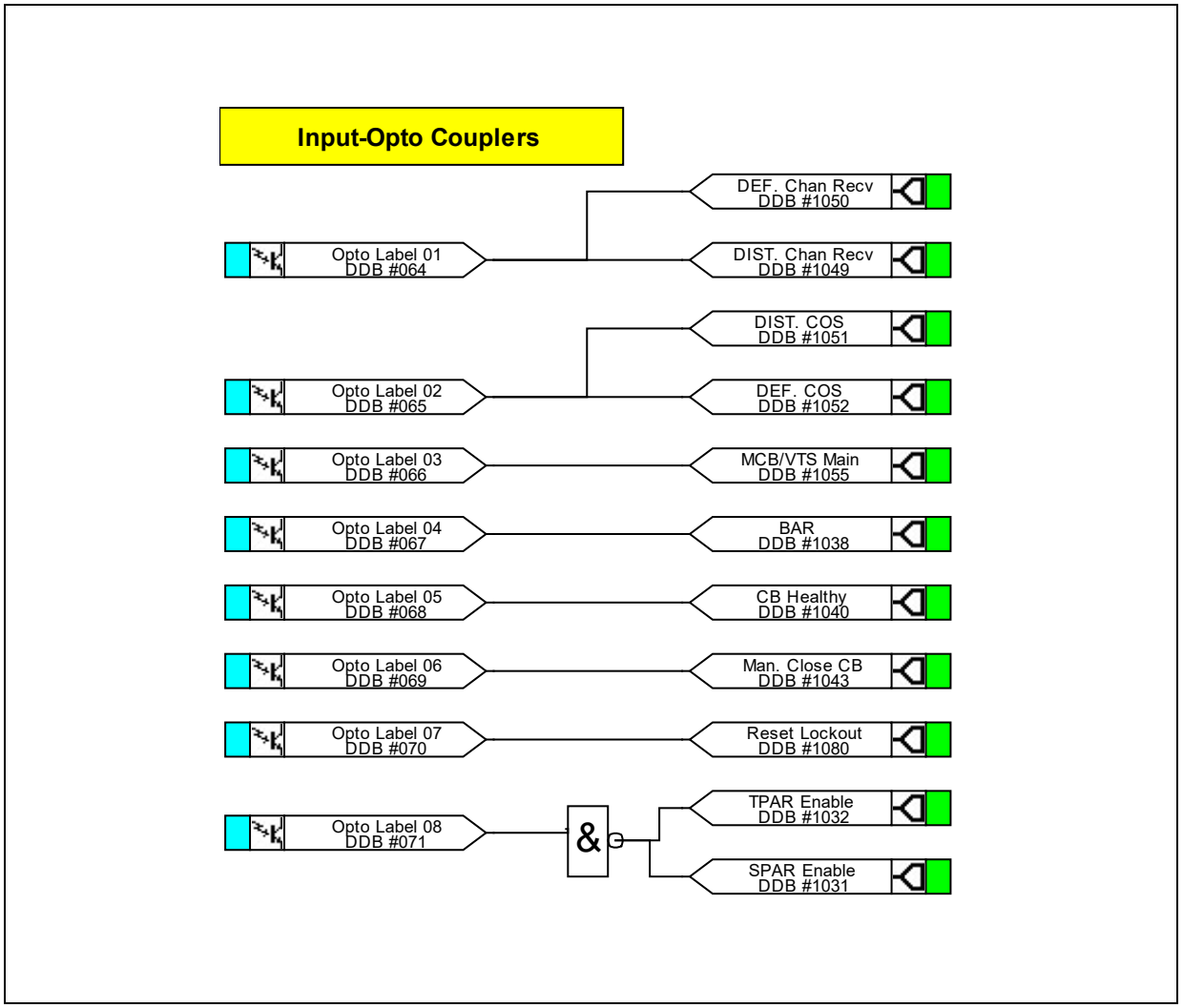
Using the GOOSE Editor you can edit the UCA2 GOOSE settings for a MiCOM Px4x series IED. You can also map GOOOSE inputs and outputs to the DDB signals of an IED.

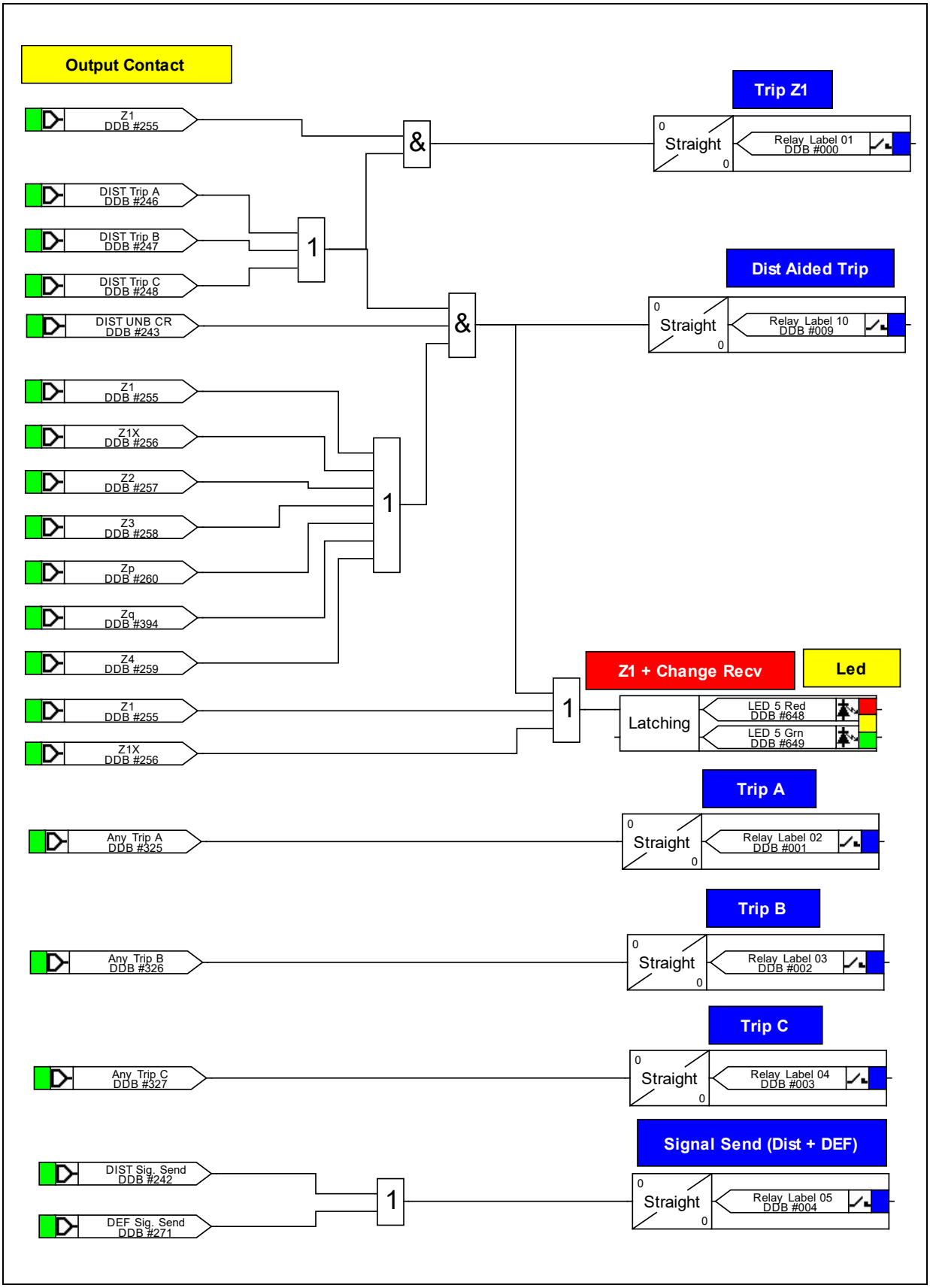
The GOOSE Editor can extract settings from and send settings to an IED using a Courier port on the IED. It can also save IED settings to a file on your PC or print them.

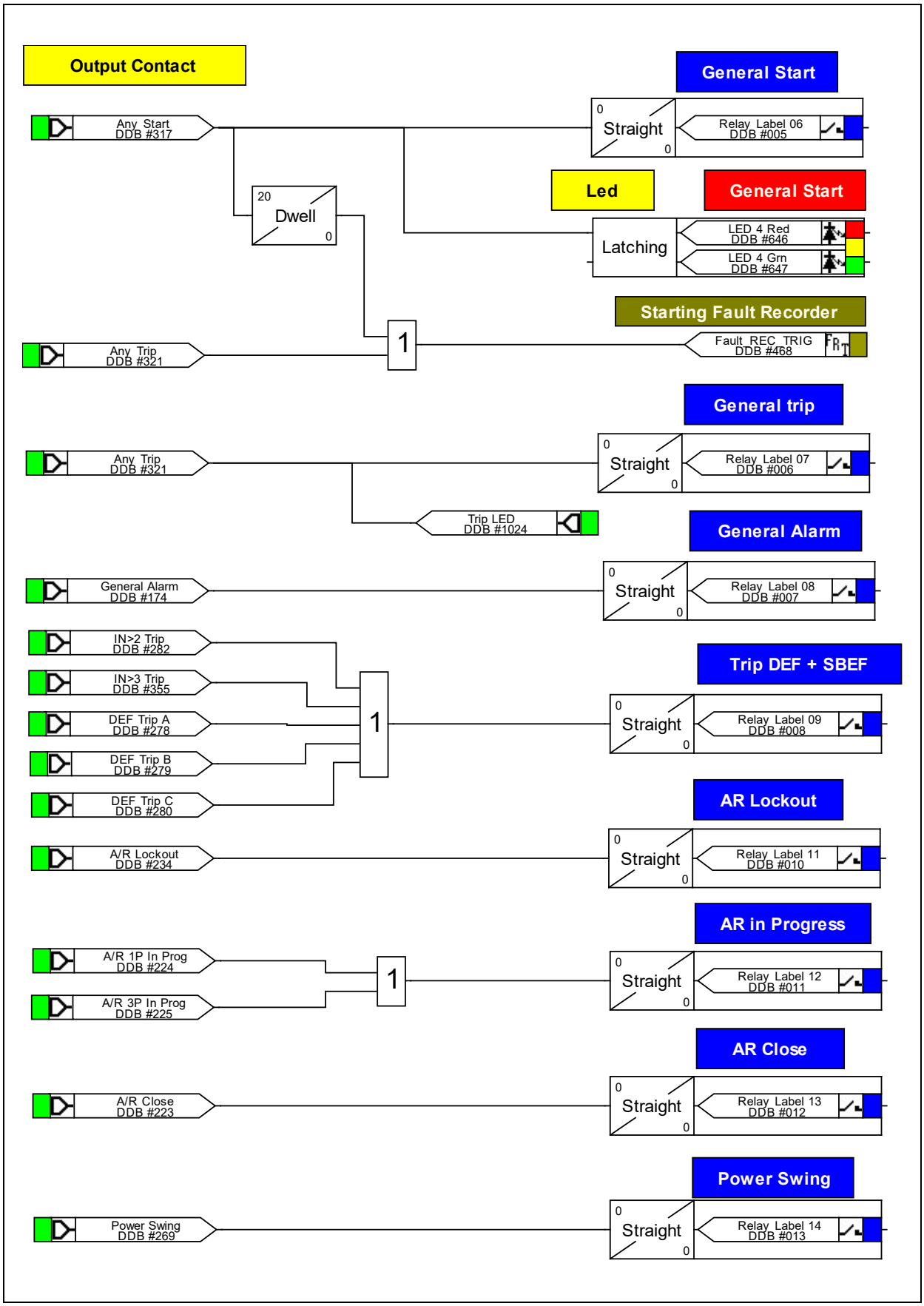
Further information is available in the Help system and in the Settings Application Software Guide P40-M&CR-UG-EN-n, where n is the latest version of the settings application software.

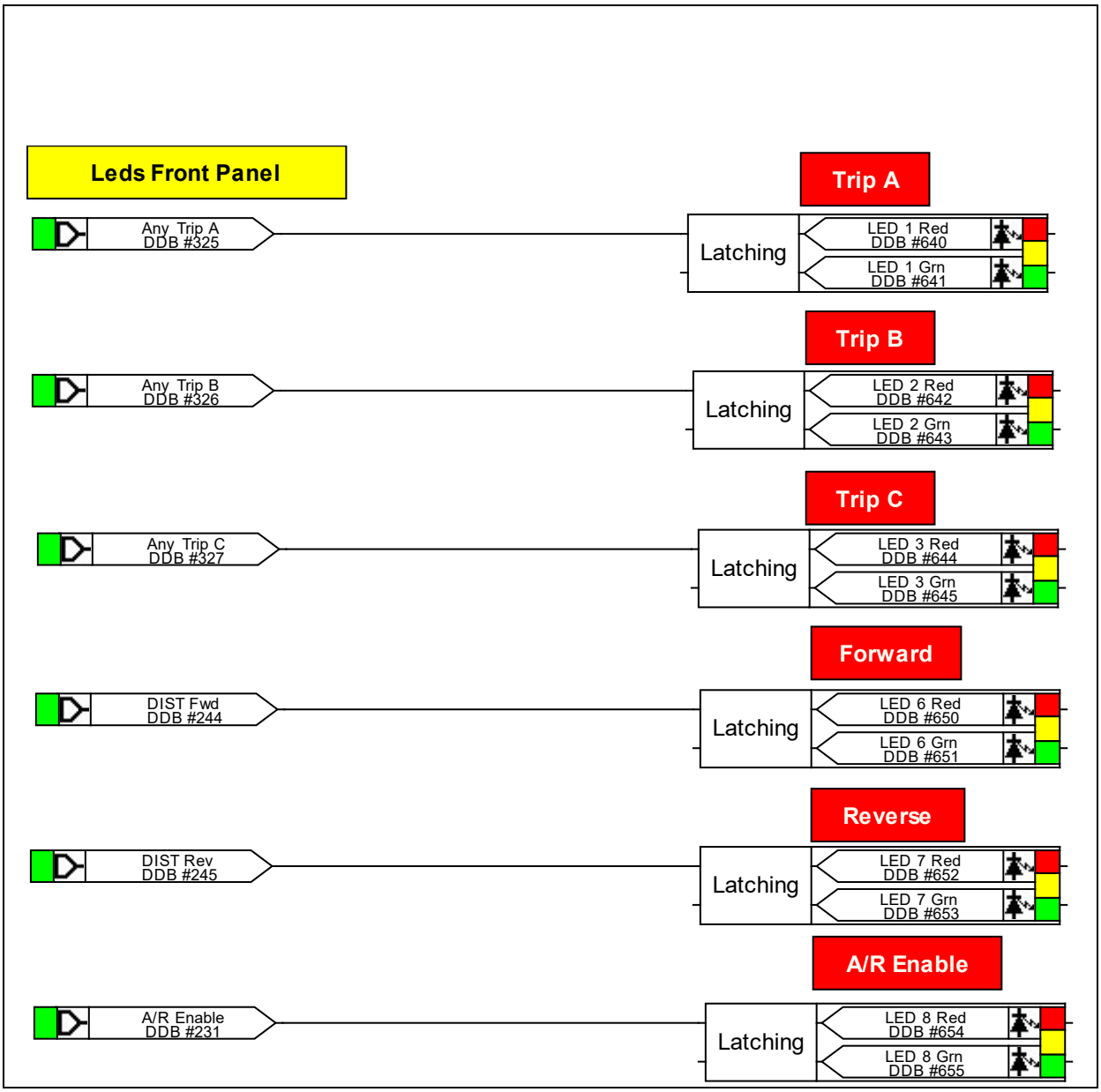
4 DEFAULT PROGRAMMABLE SCHEME LOGIC (PSL)

Example: MiCOM P444 with 46 outputs




Output Contact
Z1 DDB #255
DIST Trip A DDB #246
DIST Trip B DDB #247
DIST Trip C DDB #248
DIST UNB CR DDB #243
Z1 DDB #255
Z1X DDB #256
Z2 DDB #257
Z3 DDB #258
Zp DDB #260
Zq DDB #394
Z4 DDB #259
Z1 DDB #255
Z1X DDB #256
Any Trip A DDB #325
Any Trip B DDB #326
Any Trip C DDB #327
DIST Sig. Send DDB #242
DEF Sig. Send DDB #271
&
1
&
1
1
1
Trip Z1
0 Straight 0
Relay Label 01 DDB #000
Dist Aided Trip
0 Straight 0
Relay Label 10 DDB #009
Z1 + Change Recv
Led
Latching
LED 5 Red DDB #648
LED 5 Grn DDB #649
Trip A
0 Straight 0
Relay Label 02 DDB #001
Trip B
0 Straight 0
Relay Label 03 DDB #002
Trip C
0 Straight 0
Relay Label 04 DDB #003
Signal Send (Dist + DEF)
0 Straight 0
Relay Label 05 DDB #004


Output Contact
General Start
Any Start DDB #317
0 Straight 0
Relay Label 06 DDB #005
20 Dwell 0
Led
General Start
Latching
LED 4 Red DDB #646
LED 4 Grn DDB #647
Starting Fault Recorder
Any Trip DDB #321
1
Fault REC TRIG DDB #468
General trip
Any Trip DDB #321
0 Straight 0
Relay Label 07 DDB #006
Trip LED DDB #1024
General Alarm
General Alarm DDB #174
0 Straight 0
Relay Label 08 DDB #007
IN>2 Trip DDB #282
IN>3 Trip DDB #355
DEF Trip A DDB #278
DEF Trip B DDB #279
DEF Trip C DDB #280
1
Trip DEF + SBEF
0 Straight 0
Relay Label 09 DDB #008
AR Lockout
A/R Lockout DDB #234
0 Straight 0
Relay Label 11 DDB #010
AR in Progress
A/R 1P In Prog DDB #224
A/R 3P In Prog DDB #225
1
0 Straight 0
Relay Label 12 DDB #011
AR Close
A/R Close DDB #223
0 Straight 0
Relay Label 13 DDB #012
Power Swing
Power Swing DDB #269
0 Straight 0
Relay Label 14 DDB #013


Leds Front Panel
Trip A
Any Trip A
DDB #325
Latching
LED 1 Red
DDB #640
LED 1 Grn
DDB #641
Trip B
Any Trip B
DDB #326
Latching
LED 2 Red
DDB #642
LED 2 Grn
DDB #643
Trip C
Any Trip C
DDB #327
Latching
LED 3 Red
DDB #644
LED 3 Grn
DDB #645
Forward
DIST Fwd
DDB #244
Latching
LED 6 Red
DDB #650
LED 6 Grn
DDB #651
Reverse
DIST Rev
DDB #245
Latching
LED 7 Red
DDB #652
LED 7 Grn
DDB #653
A/R Enable
A/R Enable
DDB #231
Latching
LED 8 Red
DDB #654
LED 8 Grn
DDB #655

INSTALLATION

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1 RECEIPT OF RELAYS

Protective relays, although generally of robust construction, require careful treatment prior to installation on site. On receipt, relays should be examined immediately to ensure no external damage has been sustained in transit.

If damage has been sustained, a claim should be made to the transport contractor and GE Vernova should be promptly notified.

Relays that are supplied unmounted and not intended for immediate installation should be returned to their protective polythene bags and delivery carton.

Section 3 of this chapter gives more information about the storage of relays.

2 HANDLING OF ELECTRONIC EQUIPMENT

A person's normal movements can easily generate electrostatic potentials of several thousand volts. Discharge of these voltages into semiconductor devices when handling electronic circuits can cause serious damage which, although not always immediately apparent, will reduce the reliability of the circuit. This is particularly important to consider where the circuits use complementary metal oxide semiconductors (CMOS), as is the case with these relays.

The relay's electronic circuits are protected from electrostatic discharge when housed in the case. Do not expose them to risk by removing the front panel or printed circuit boards unnecessarily.

Each printed circuit board incorporates the highest practicable protection for its semiconductor devices. However, if it becomes necessary to remove a printed circuit board, the following precautions should be taken to preserve the high reliability and long life for which the relay has been designed and manufactured.

1. Before removing a printed circuit board, ensure that you are at the same electrostatic potential as the equipment by touching the case.
2. Handle analogue input modules by the front panel, frame or edges of the circuit boards. Printed circuit boards should only be handled by their edges.
   Avoid touching the electronic components, printed circuit tracks or connectors.
3. Do not pass the module to another person without first ensuring you are both at the same electrostatic potential. Shaking hands achieves equipotential.
4. Place the module on an anti-static surface, or on a conducting surface which is at the same potential as yourself.
5. If it is necessary to store or transport printed circuit boards removed from the case, place them individually in electrically conducting anti-static bags.

In the unlikely event that you are making measurements on the internal electronic circuitry of a relay in service, it is preferable that you are earthed to the case with a conductive wrist strap. Wrist straps should have a resistance to ground between 500 kΩ to 10 MΩ. If a wrist strap is not available you should maintain regular contact with the case to prevent a build-up of electrostatic potential. Instrumentation which may be used for making measurements should also be earthed to the case whenever possible.

More information on safe working procedures for all electronic equipment can be found in IEC 61340-5-1. It is strongly recommended that detailed investigations on electronic circuitry or modification work should be carried out in a special handling area such as described in the aforementioned Standard document.

3 STORAGE

If relays are not to be installed immediately upon receipt, they should be stored in a place free from dust and moisture in their original cartons. Where de-humidifier bags have been included in the packing they should be retained. The action of the de-humidifier crystals will be impaired if the bag is exposed to ambient conditions and may be restored by gently heating the bag for about an hour prior to replacing it in the carton.

To prevent battery drain during transportation and storage a battery isolation strip is fitted during manufacture. With the lower access cover open, presence of the battery isolation strip can be checked by a red tab protruding from the positive side.

Care should be taken on subsequent unpacking that any dust which has collected on the carton does not fall inside. In locations of high humidity the carton and packing may become impregnated with moisture and the de-humidifier crystals will lose their efficiency.

Prior to installation, relays should be stored at a temperature of between –40˚C to +70˚C.

4 UNPACKING

Care must be taken when unpacking and installing the relays so that none of the parts are damaged and additional components are not accidentally left in the packing or lost.

> *Note: With the lower access cover open, the red tab of the battery isolation strip will be seen protruding from the positive side of the battery compartment. Do not remove this strip because it prevents battery drain during transportation and storage and will be removed as part of the commissioning tests.*

Relays must only be handled by skilled persons.

The site should be well lit to facilitate inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies to installations which are being carried out at the same time as construction work.

5 RELAY MOUNTING

MiCOM relays are dispatched either individually or as part of a panel/rack assembly.

Individual relays are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres. This information can also be found in the product publication.

Secondary front covers can also be supplied as an option item to prevent unauthorised changing of settings and alarm status. They are available in sizes 40TE (GN0037 001) and 60TE (GN0038 001). Note that the 60TE cover also fits the 80TE case size of the relay.

The design of the relay is such that the fixing holes in the mounting flanges are only accessible when the access covers are open and hidden from sight when the covers are closed.

If a P991 or MMLG test block is to be included, it is recommended that, when viewed from the front, it is positioned on the right-hand side of the relay (or relays) with which it is associated. This minimises the wiring between the relay and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

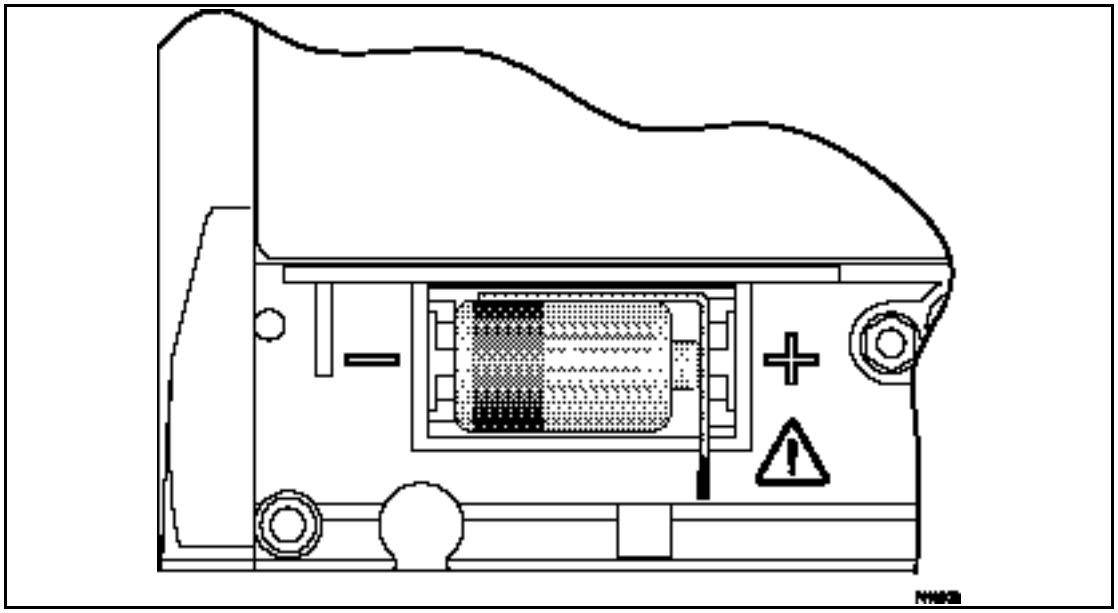


Figure 1 - Location of battery isolation strip

If it is necessary to test correct relay operation during the installation, the battery isolation strip can be removed but should be replaced if commissioning of the scheme is not imminent. This will prevent unnecessary battery drain during transportation to site and installation. The red tab of the isolation strip can be seen protruding from the positive side of the battery compartment when the lower access cover is open. To remove the isolation strip, pull the red tab whilst lightly pressing the battery to prevent it falling out of the compartment. When replacing the battery isolation strip, ensure that the strip is refitted as shown in Figure 1, ie. with the strip behind the battery with the red tab protruding.

5.1 Rack mounting

MiCOM relays may be rack mounted using single tier rack frames (our part number FX0021 001), as shown in Figure 2. These frames have been designed to have dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483mm (19") rack system this enables combinations of widths of case up to a total equivalent of size 80TE to be mounted side by side.

Relays in 80TE cases are also available as direct 19" rack mounting ordering variants, having mounted flanges similar to those shown in Figure 2.

The two horizontal rails of the rack frame have holes drilled at approximately 26mm intervals and the relays are attached via their mounting flanges using M4 Taptite self-tapping screws with captive 3mm thick washers (also known as a SEMS unit).

> *Note: Conventional self-tapping screws, including those supplied for mounting MIDOS relays, have marginally larger heads which can damage the front cover moulding if used.*

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

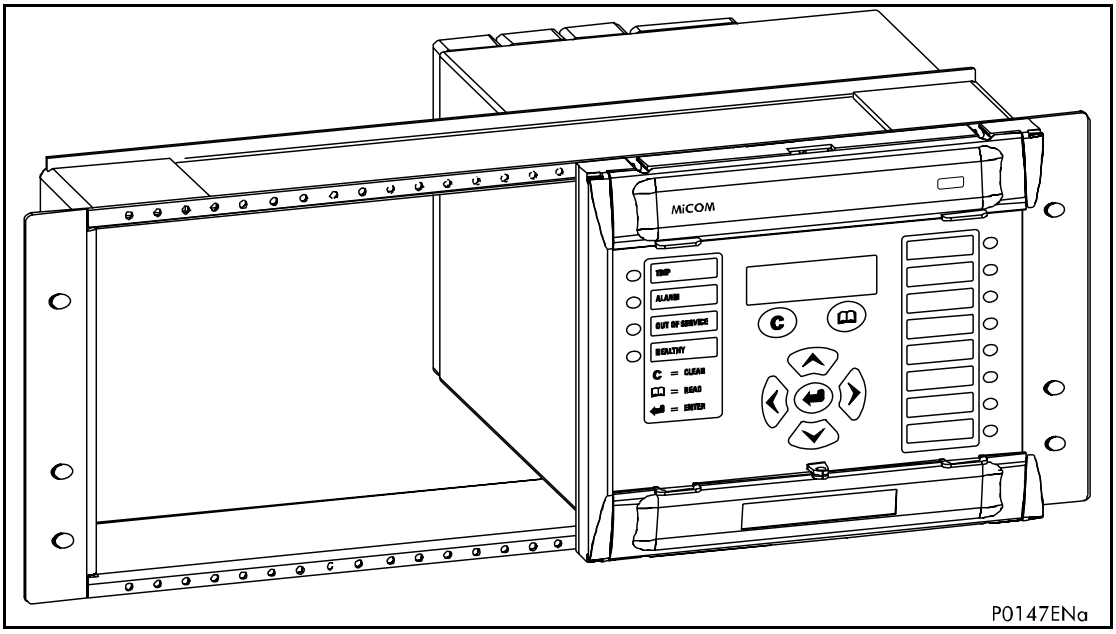


Figure 2 - Rack mounting of relays

Relays can be mechanically grouped into single tier (4U) or multi-tier arrangements by means of the rack frame. This enables schemes using products from the MiCOM and MiDOS product ranges to be pre-wired together prior to mounting.

Where the case size summation is less than 80TE on any tier, or space is to be left for installation of future relays, blanking plates may be used. These plates can also be used to mount ancillary components. Table 1 shows the sizes that can be ordered.

Further details on mounting MiDOS relays can be found in publication R7012, “MiDOS Parts Catalogue and Assembly Instructions”.

Case size summation	Blanking plate part number
5TE	GJ2028 001
10TE	GJ2028 002
15TE	GJ2028 003
20TE	GJ2028 004
25TE	GJ2028 005
30TE	GJ2028 006
35TE	GJ2028 007
40TE	GJ2028 008

Table 1 - Blanking plates

5.2 Panel mounting

The relays can be flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3mm thick washers (also known as a SEMS unit).

Note: Conventional self-tapping screws, including those supplied for mounting MIDOS relays, have marginally larger heads which can damage the front cover moulding if used.

Alternatively tapped holes can be used if the panel has a minimum thickness of 2.5mm.

For applications where relays need to be semi-projection or projection mounted, a range of collars are available.

Where several relays are to mounted in a single cut-out in the panel, it is advised that they are mechanically grouped together horizontally and/or vertically to form rigid assemblies prior to mounting in the panel.

Note: It is not advised that MiCOM relays are fastened using pop rivets as this will not allow the relay to be easily removed from the panel in the future if repair is necessary.

If it is required to mount a relay assembly on a panel complying to BS EN60529 IP52, it will be necessary to fit a metallic sealing strip between adjoining relays (Part no GN2044 001) and a sealing ring selected from Table 2 around the complete assembly.

Width	Single tier	Double tier
10TE	GJ9018 002	GJ9018 018
15TE	GJ9018 003	GJ9018 019
20TE	GJ9018 004	GJ9018 020
25TE	GJ9018 005	GJ9018 021
30TE	GJ9018 006	GJ9018 022
35TE	GJ9018 007	GJ9018 023
40TE	GJ9018 008	GJ9018 024
45TE	GJ9018 009	GJ9018 025
50TE	GJ9018 010	GJ9018 026
55TE	GJ9018 011	GJ9018 027

Width	Single tier	Double tier
60TE	GJ9018 012	GJ9018 028
65TE	GJ9018 013	GJ9018 029
70TE	GJ9018 014	GJ9018 030
75TE	GJ9018 015	GJ9018 031
80TE	GJ9018 016	GJ9018 032

Table 2 - IP52 sealing rings

Further details on mounting MiDOS relays can be found in publication R7012, “MiDOS Parts Catalogue and Assembly Instructions”.

6 RELAY WIRING

This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the MiCOM relay.

6.1 Medium and heavy duty terminal block connections

Loose relays are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per relay terminal.

If required, we can supply M4 90° crimp ring terminals in two different sizes depending on wire size (see Table 3). Each type is available in bags of 100.

Part number	Wire size	Insulation colour
ZB9124 901	0.25 – 1.65 mm^2 (22 – 16AWG)	Red
ZB9124 900	1.04 – 2.63 mm^2 (16 – 14AWG)	Blue

Table 3 - M4 90° crimp ring terminals

* To maintain the terminal block insulation requirements for safety, an insulating sleeve should be fitted over the ring terminal after crimping.

The following minimum wire sizes are recommended:

Current Transformers 2.5 mm^2

Auxiliary Supply, Vx 1.5 mm^2

RS485 Port See separate section

Other circuits 1.0 mm^2

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 using ring terminals that are not pre-insulated. Where it required to only use pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63 mm^2 per ring terminal. If a larger wire size is required, two wires should be used in parallel, each terminated in a separate ring terminal at the relay.

The wire used for all connections to the medium and heavy duty terminal blocks, except the RS485 port, should have a minimum voltage rating of 300 Vrms.

It is recommended that the auxiliary supply wiring should be protected by a 16 A high rupture capacity (HRC) fuse of type NIT or TIA. For safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

6.2 RS485 port

Connections to the RS485 port are made using ring terminals. It is recommended that a 2 core screened cable is used with a maximum total length of 1000m or 200 nF total cable capacitance. A typical cable specification would be:

Each core:	16/0.2 mm copper conductors PVC insulated
Nominal conductor area:	0.5 mm^2 per core
Screen:	Overall braid, PVC sheathed

6.3 IRIG-B connections (if applicable)

The IRIG-B input and BNC connector have a characteristic impedance of 50 Ω. It is recommended that connections between the IRIG-B equipment and the relay are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

6.4 RS232 port

Short term connections to the RS232 port, located behind the bottom access cover, can be made using a screened multi-core communication cable up to 15m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. Chapter 2, Section 3.7 of this manual details the pin allocations.

6.5 Download/monitor port

Short term connections to the download/monitor port, located behind the bottom access cover, can be made using a screened 25-core communication cable up to 4m long. The cable should be terminated at the relay end with a 25-way, metal shelled, D-type male plug. Chapter 2, Section 3.7 of this manual details the pin allocations.

6.6 Earth connection

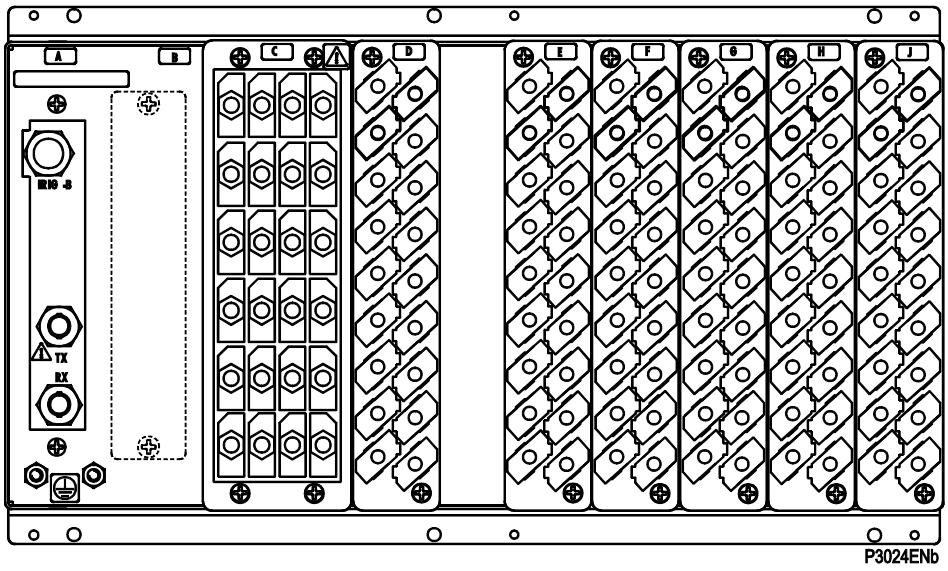
Every relay must be connected to the local earth bar using the M4 earth studs in the bottom left hand corner of the relay case. The minimum recommended wire size is 2.5 mm^2 and should have a ring terminal at the relay end. Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 per wire. If a greater cross-sectional area is required, two parallel connected wires, each terminated in a separate ring terminal at the relay, or a metal earth bar could be used.

Note:	*To prevent any possibility of electrolytic action between brass or copper earth conductors and the rear panel of the relay, precautions should be taken to isolate them from one another. This could be achieved in a number of ways, including placing a nickel-plated or insulating washer between the conductor and the relay case, or using tinned ring terminals.*



Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety and Technical Data sections and the ratings on the equipment's rating label

7 MICOM P442 – REAR VIEW (HARDWARE M)

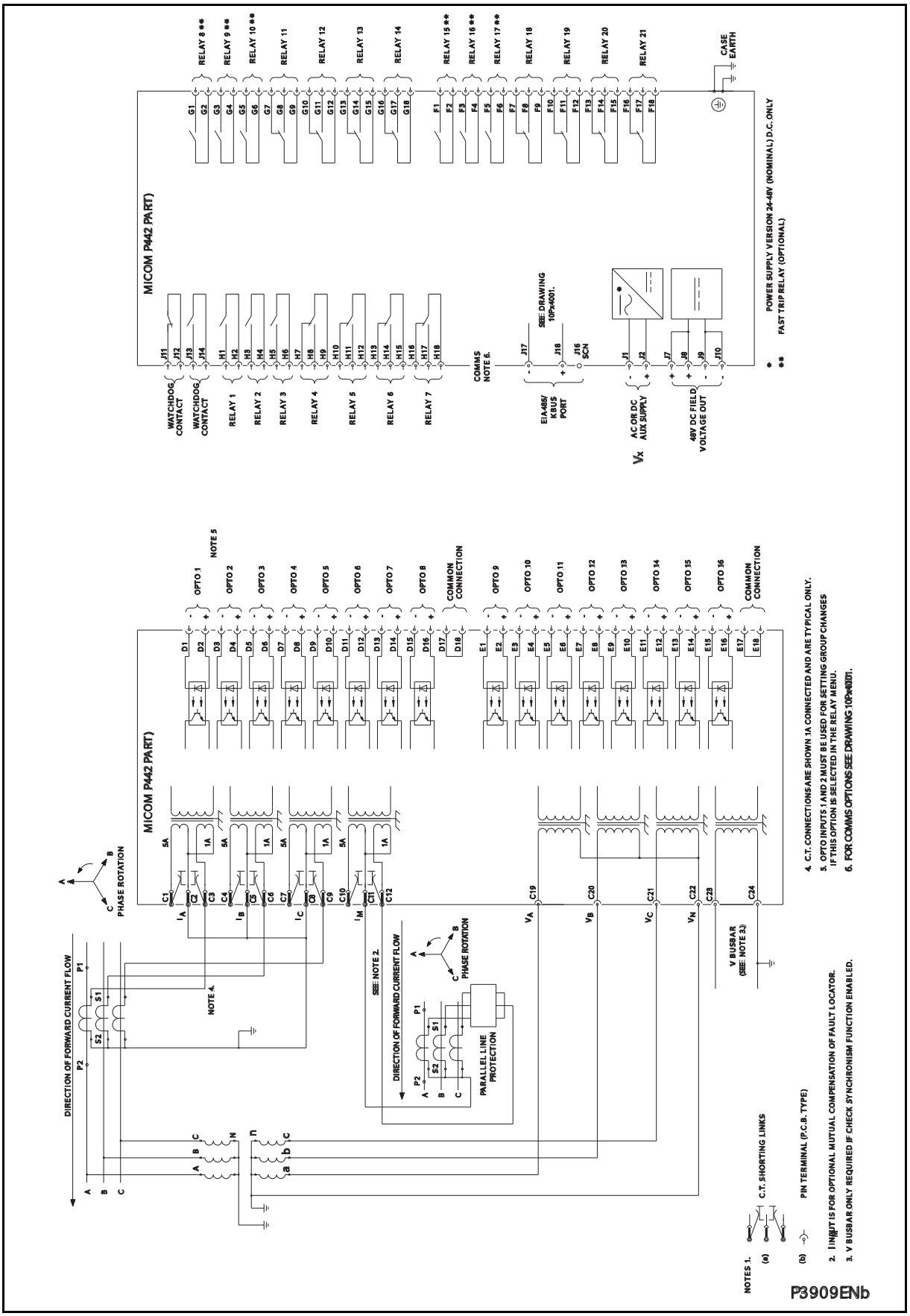


A –	Optional board (1)	F –	Output relay/High Break board (2)
B –	Optional board (1)	G –	Output relay board
C –	Current and voltage input board	F –	Power supply board
D –	Opto-input board		
E –	Opto-input board	* =	option depending on the model

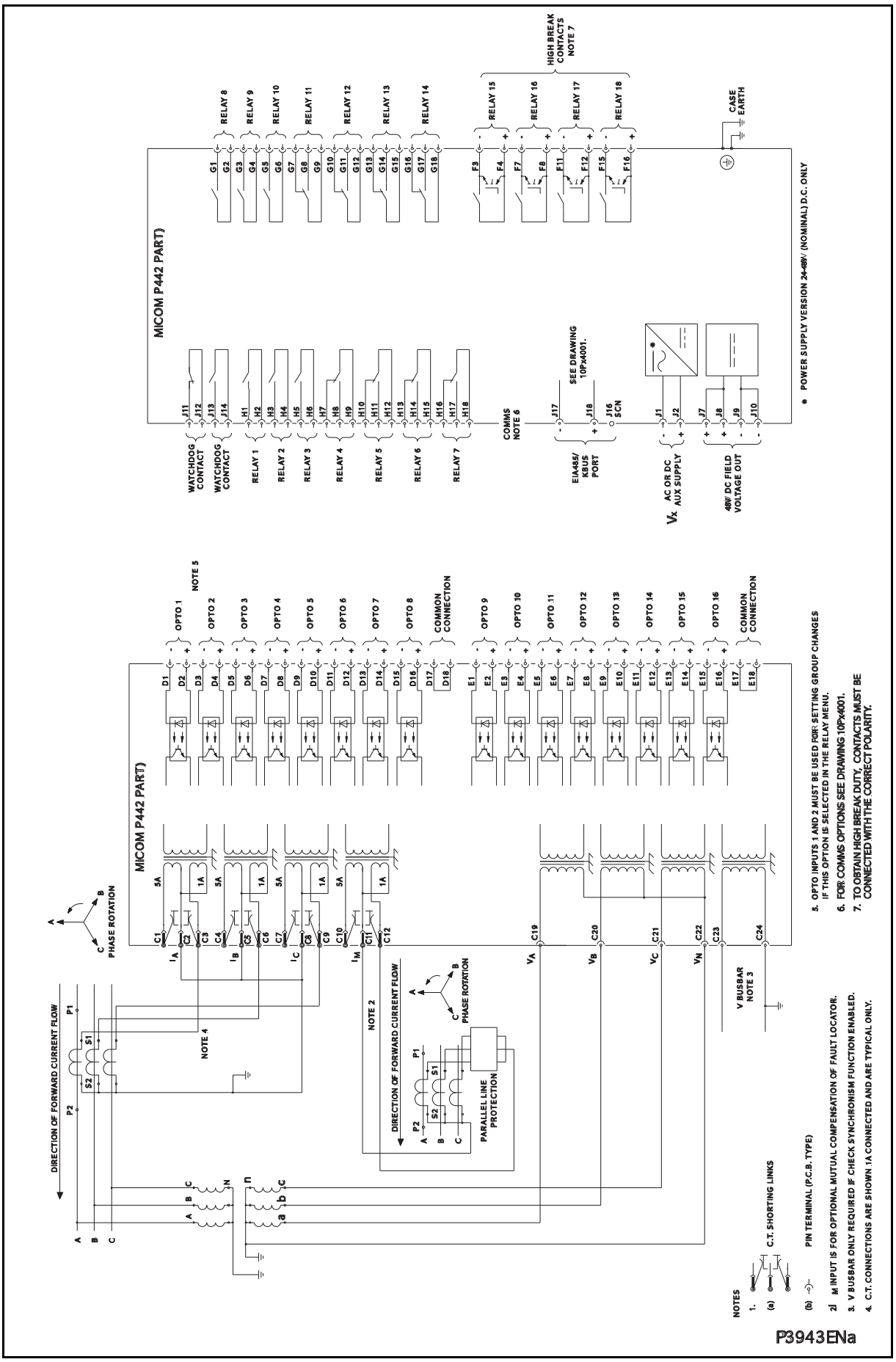
(1) Hardware options:
Refer to Introduction chapter section 3.1 Ordering Options

(2) Models:
Refer to Introduction chapter section 3.1 Ordering Options

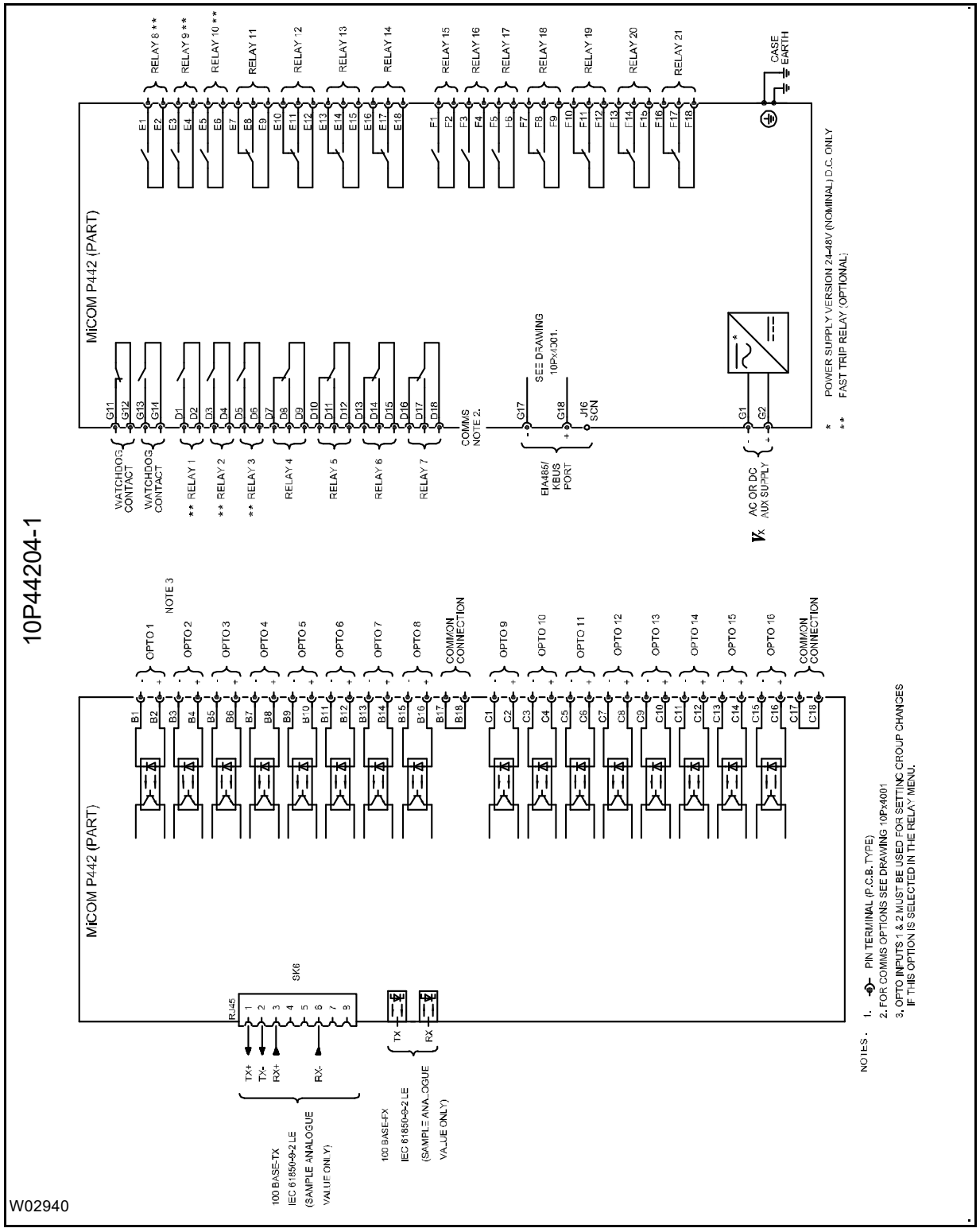
7.1 MICOM P442 with Standard contacts - Wiring Diagram (1/5)



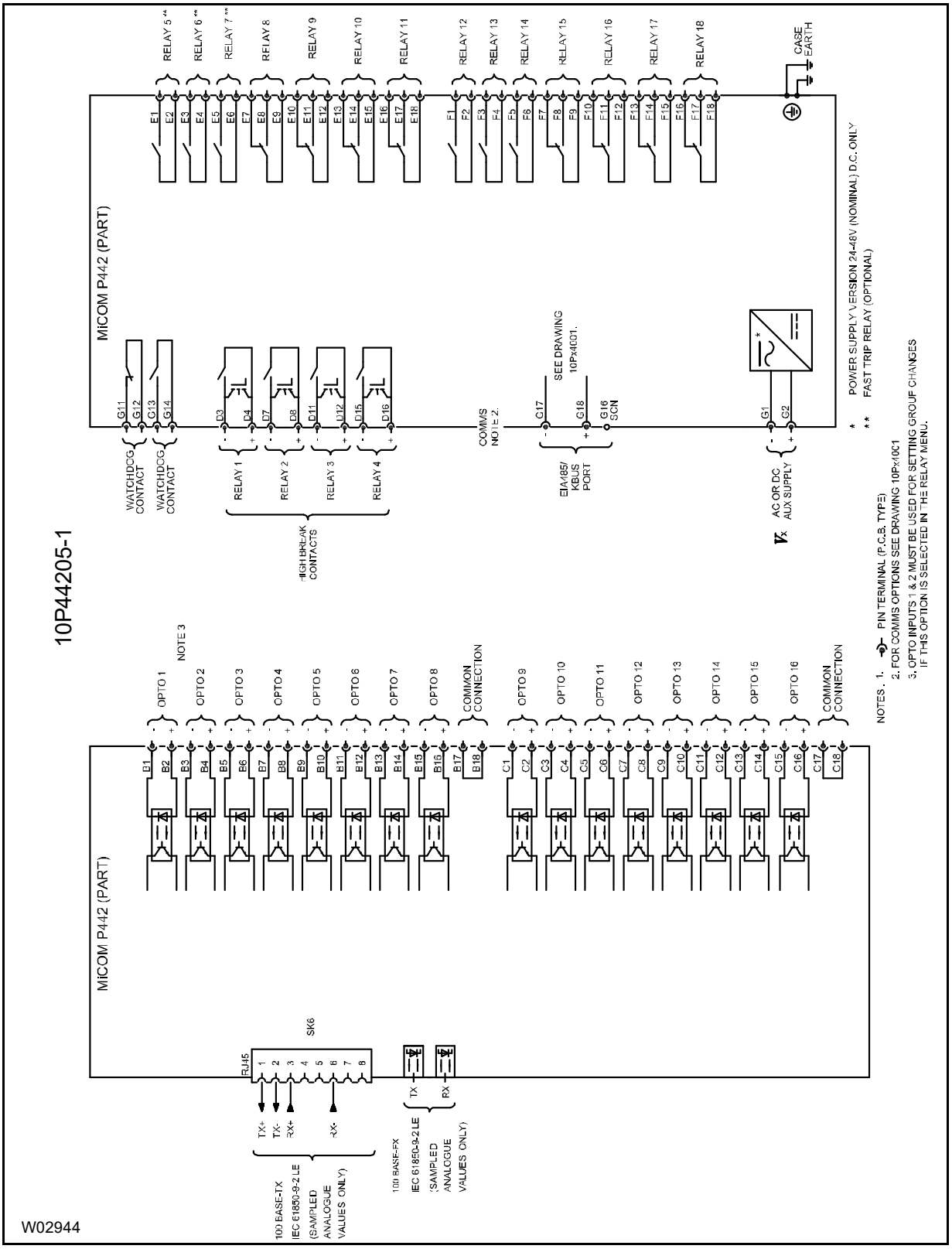
7.2 MICOM P442 with High Break contacts - Wiring Diagram (2/5)



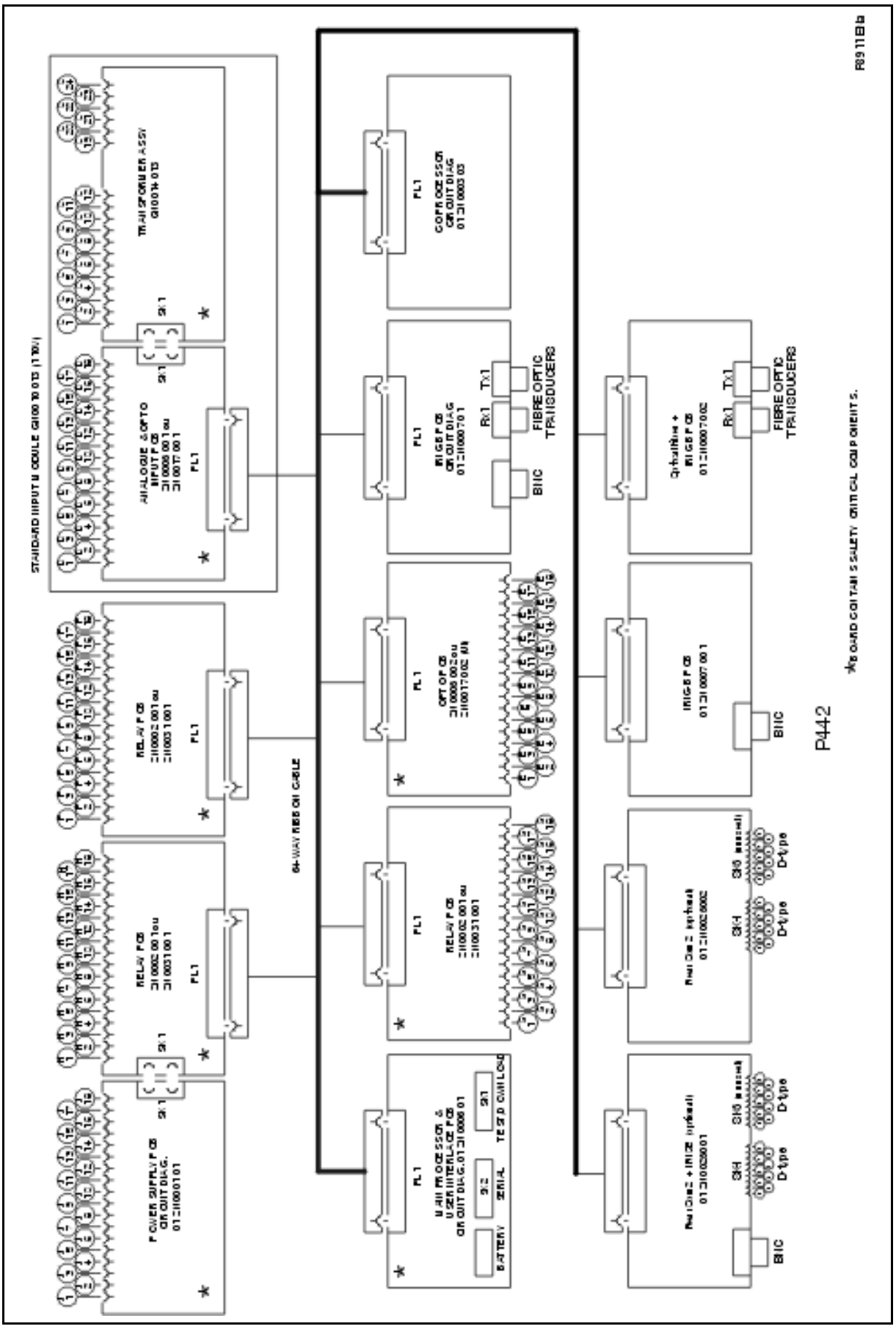
7.3 MICOM P442 with NCIT and Standard contacts - Wiring Diagram (3/5)



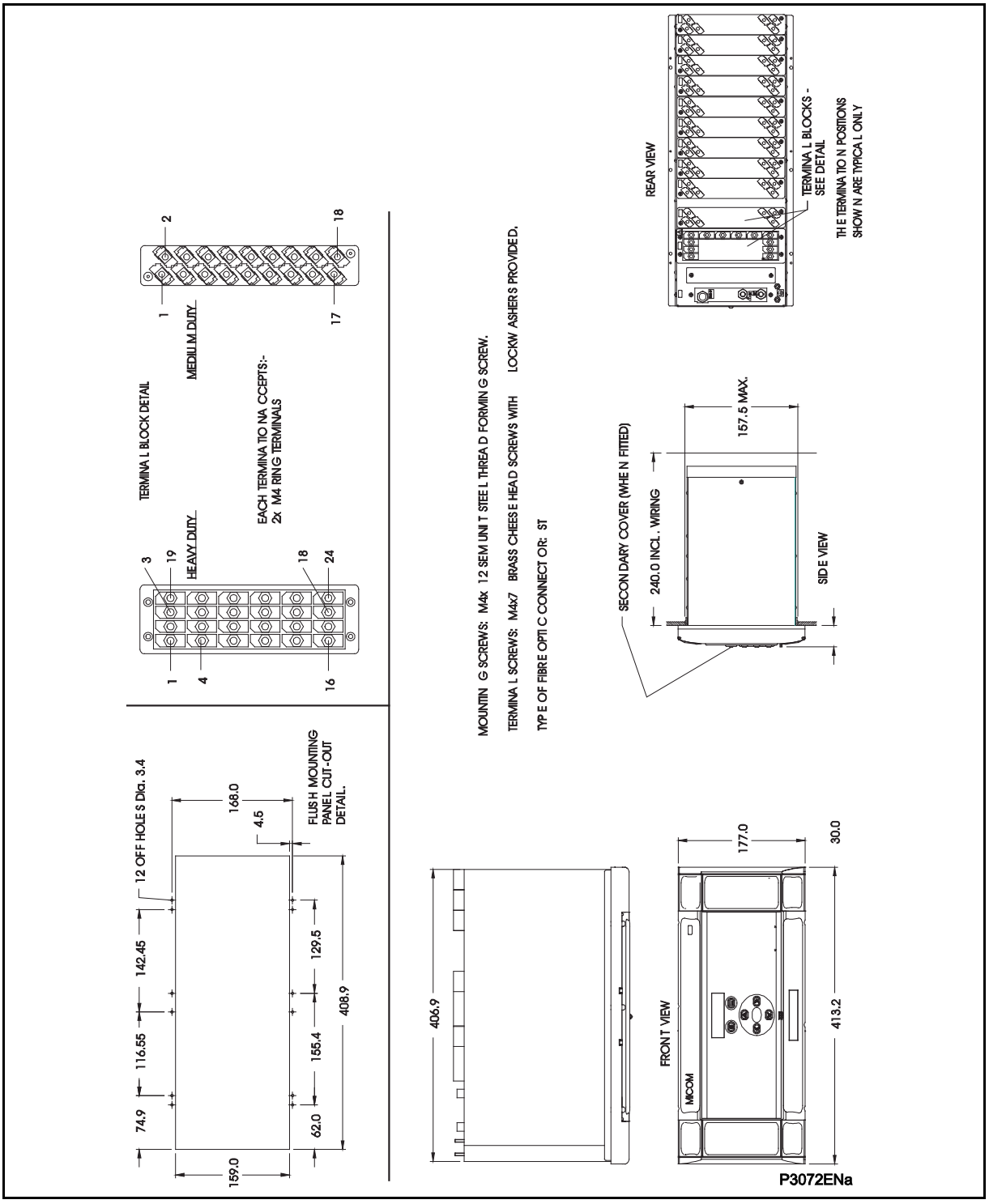
7.4 MICOM P442 with NCIT and High Break contacts - Wiring Diagram (4/5)



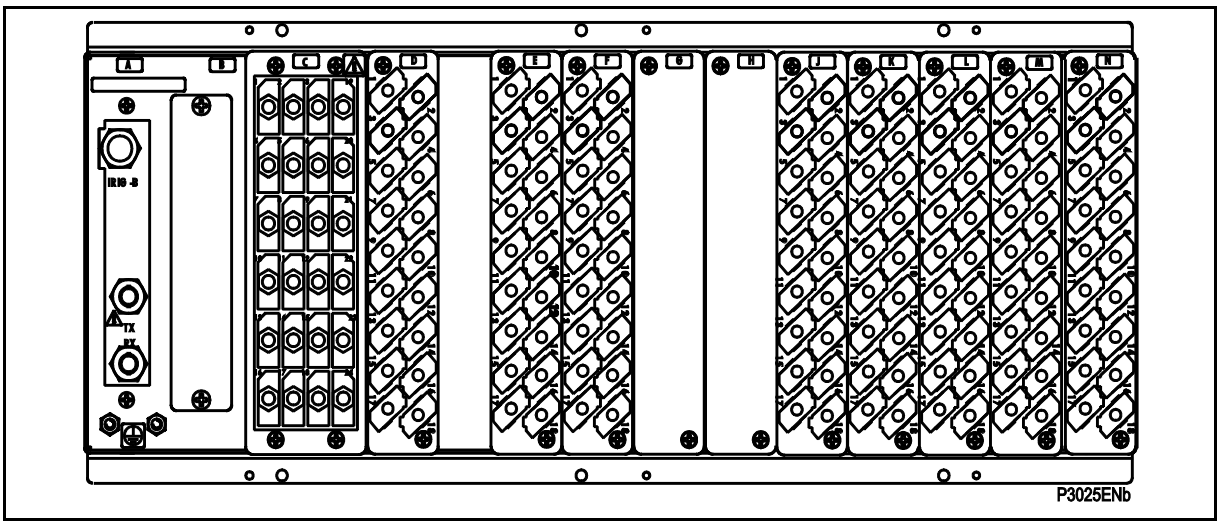
7.5 MICOM P442 – Wiring Diagram (5/5)



8 MiCOM P444 – HARDWARE DESCRIPTION (HARWARE M)



8.1 MiCOM P444 – Rear View

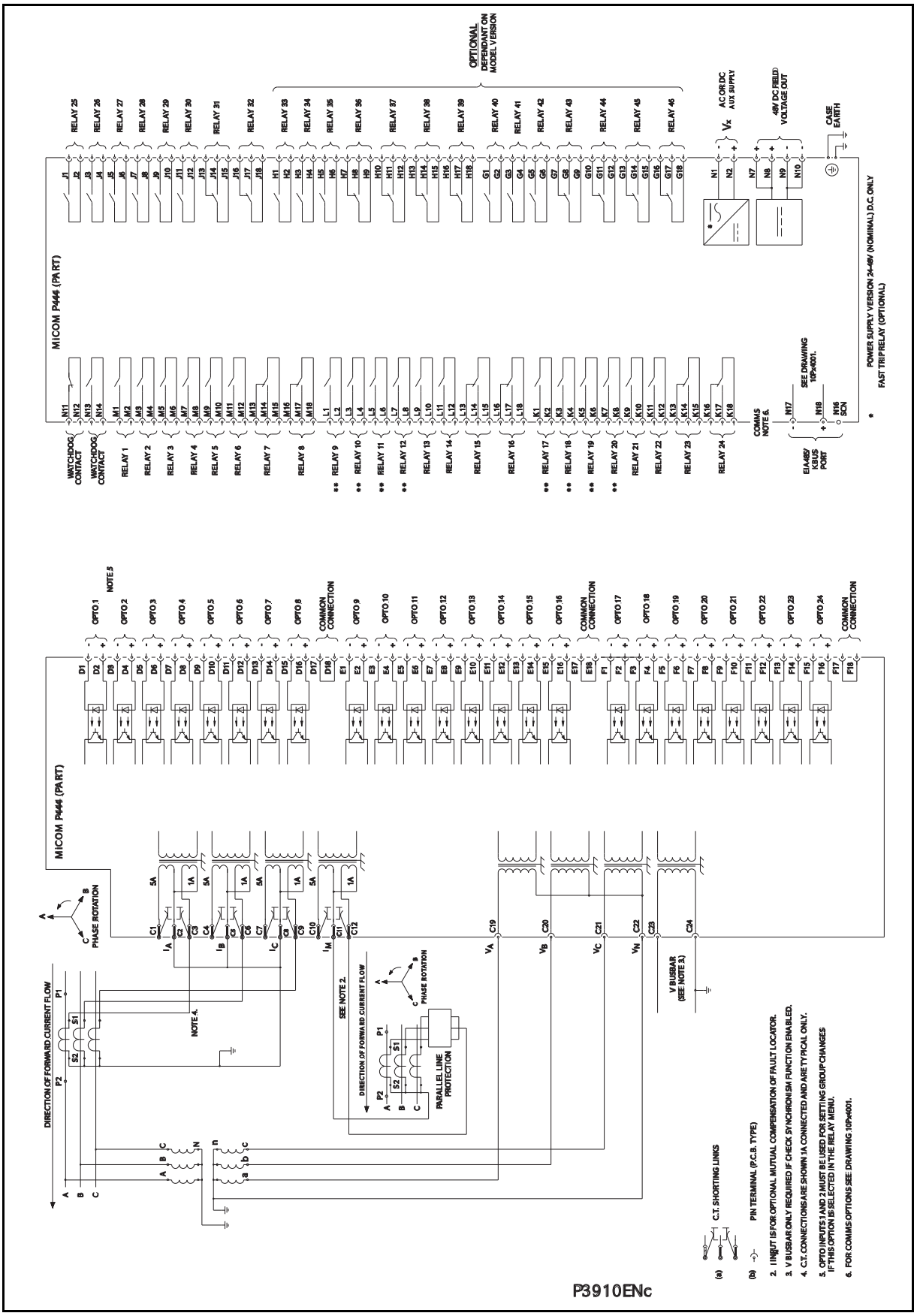


A – Optional board (1)
B – Optional board (1)
C – Current and voltage input board
D – Opto-input board
E – Opto-input board
F – Opto Input board
G – Relay board (2)
H – Relay board
J – Output relay/High Break board (2)
K – Output relay/High Break board (2)
L – Output relay/High Break board (2)
M – Relay board
N – Power supply board

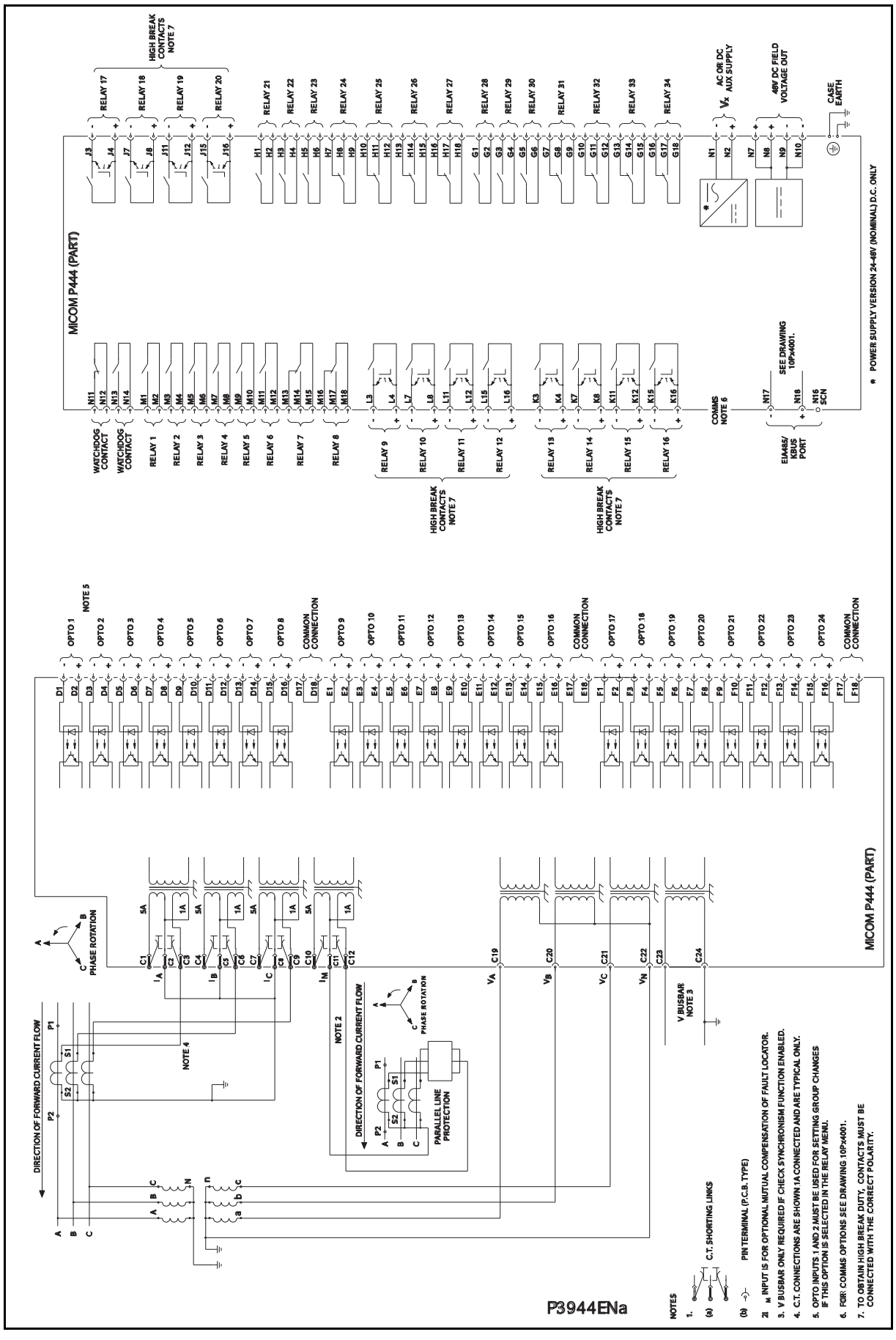
(1) Hardware options:
Refer to Introduction chapter section 3.1 Ordering Options

(2) Models:
Refer to Introduction chapter section 3.1 Ordering Options

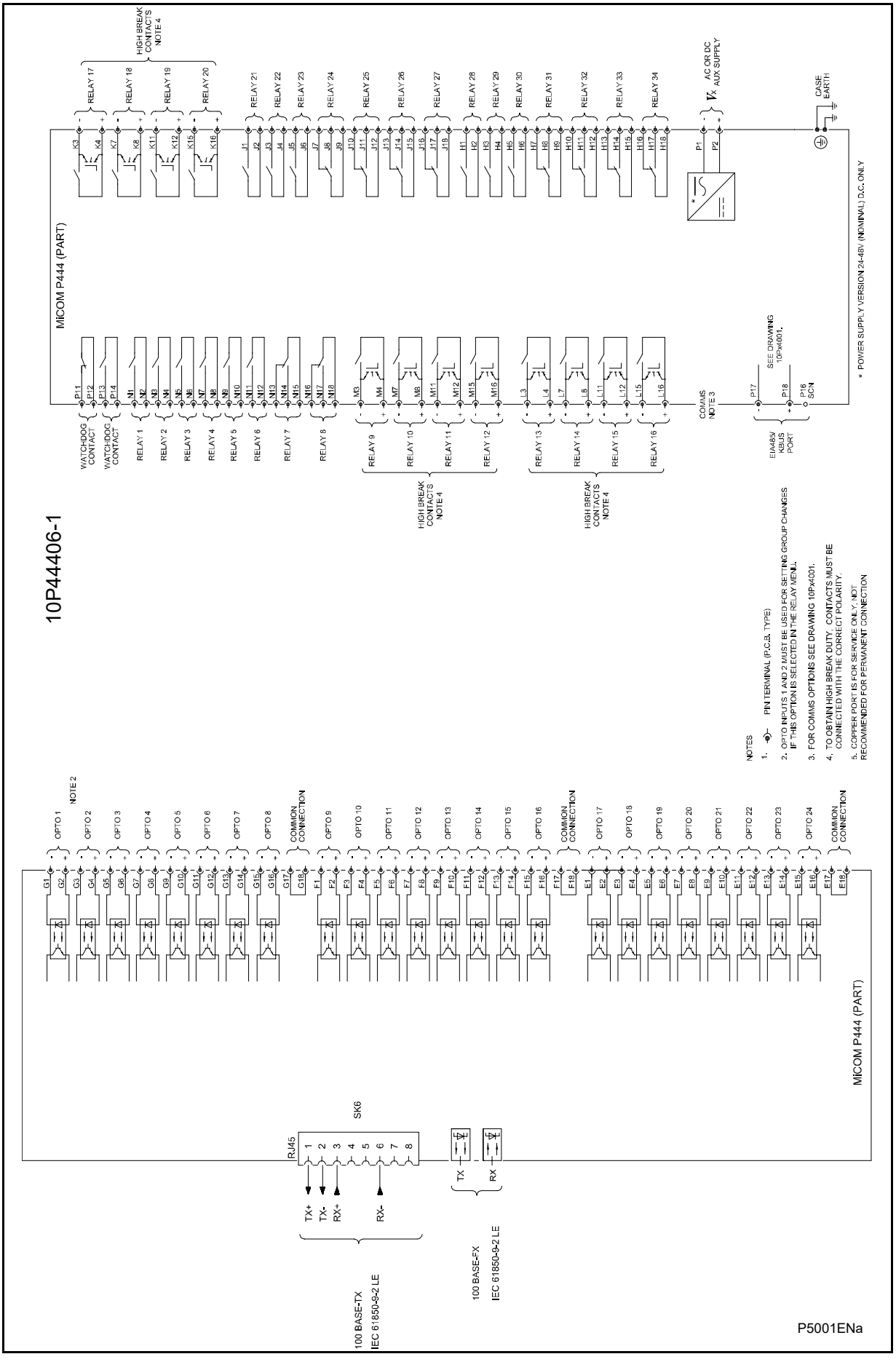
8.2 MICOM P444 with Standard contacts - Wiring Diagram (1/4)



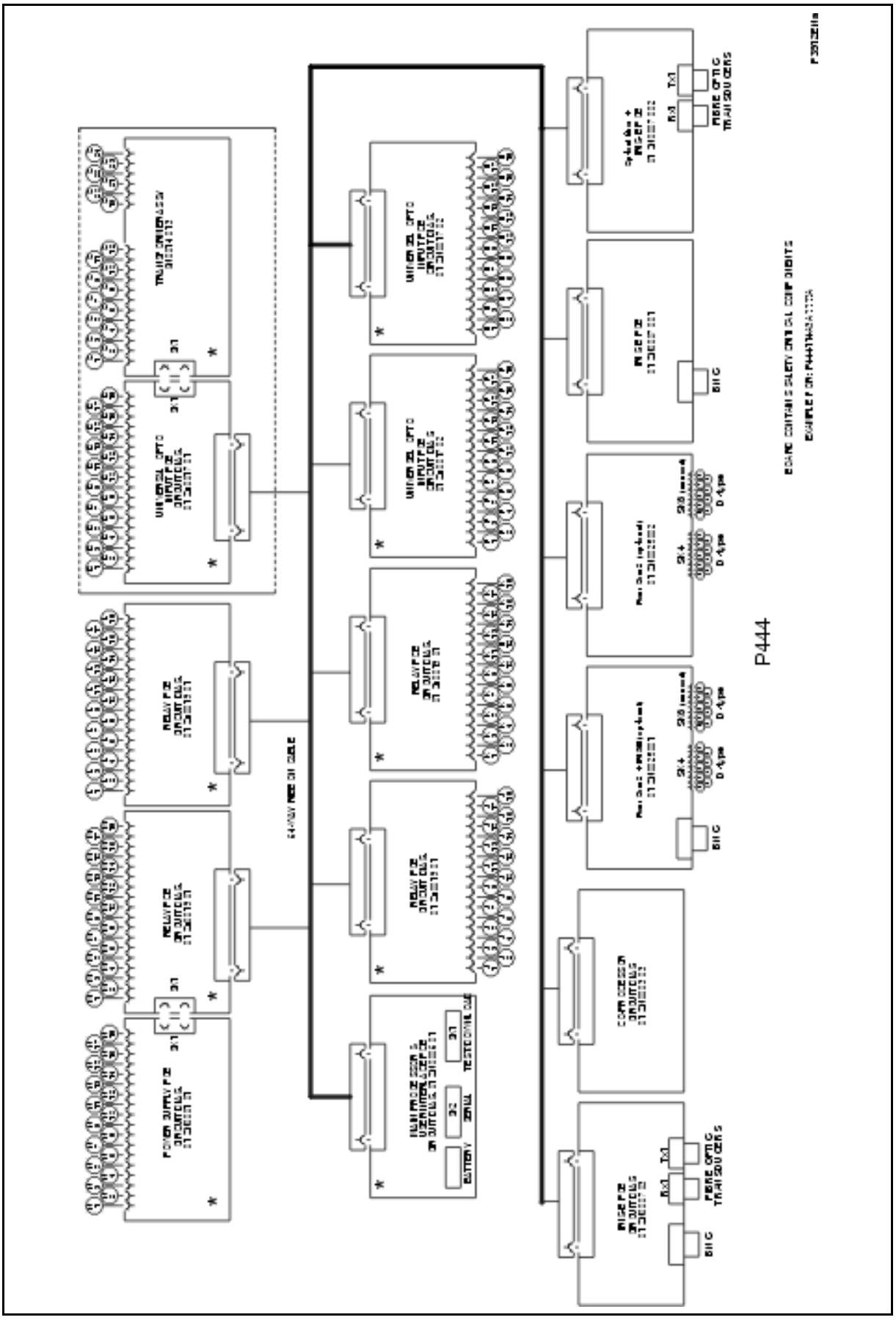
8.3 MICOM P444 with High Break contacts - Wiring Diagram (2/4)



8.4 MICOM P444 with NCIT and High Break contacts - Wiring Diagram (3/4)



8.5 MICOM P444 – Wiring Diagram (4/4)



Ordinal	English Text	Description	Source
1063	I>3 Timer Block	Block phase overcurrent stage 3 time delay Set to 1: 'I>3 Time Delay' will be blocked & I>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>3
1064	I>4 Timer Block	Block phase overcurrent stage 4 time delay Set to 1: 'I>4 Time Delay' will be blocked & I>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>4
1065	I2>1 Timer Block	Block negative sequence overcurrent stage 1 time delay	PSL (IN) I>4
1066	I2>2 Timer Block	Block negative sequence overcurrent stage 2 time delay	PSL (IN) I>5
1067	I2>3 Timer Block	Block negative sequence overcurrent stage 3 time delay	PSL (IN) I>6
1068	I2>4 Timer Block	Block negative sequence overcurrent stage 4 time delay	PSL (IN) I>7
1069	V<1 Timer Block	Block phase undervoltage stage 1 time delay Set to 1: 'V<1 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<1
1070	V<2 Timer Block	Block phase undervoltage stage 2 time delay Set to 1: 'V<2 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<2
1071	V<3 Timer Block	Block phase undervoltage stage 3 time delay Set to 1: 'V<3 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<3
1072	V<4 Timer Block	Block phase undervoltage stage 4 time delay Set to 1: 'V<4 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<4
1073	V>1 Timer Block	Block phase overvoltage stage 1 time delay Set to 1: 'V>1 Time Delay will be blocked and V>1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>1
1074	V>2 Timer Block	Block phase overvoltage stage 2 time delay Set to 1: 'V>2 Time Delay' will be blocked and V>2 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>2
1075	V>3 Timer Block	Block phase overvoltage stage 3 time delay Set to 1: 'V>3 Time Delay' will be blocked and V>3 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>3
1076	V>4 Timer Block	Block phase overvoltage stage 4 time delay Set to 1: 'V>4 Time Delay' will be blocked and V>4 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>4
1077	VN>1 Timer Block	Block earth overvoltage stage 1 time delay	PSL (IN) VN>1
1078	VN>2 Timer Block	Block earth overvoltage stage 2 time delay	PSL (IN) VN>2

Ordinal	English Text	Description	Source
1079	DIST. Tim. Block	Block distance element time delay At 1: The distance timer will be blocked & DIST will start but will not perform a Trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Distance
1080	Reset Lockout	Reset all CB monitoring lockout (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1081	Reset All values	Reset all values of CB monitoring (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1082	Reset Latches	Reset all permanent alarms + LEDs and relays are lached	PSI (IN)
1083	Stub Bus Enable	Enable I>4 Element for stub bus protection (isolator of HV line open - status isolator must be connected to an opto input)	PSL (IN)
1084	User Trip A	Internal input for trip logic A Set to 1: Trip A Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1085	User Trip B	Internal input for trip logic B Set to 1: Trip B Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1086	User Trip C	Internal input for trip logic C Set to 1: Trip C Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1087	ZSP Timer Block	Zero Sequence Power - Timer Block: If assigned to an opto input in a dedicated PSL, Zero Sequence Power function will start, but will not perform a trip command - the associated time-delay (adjusted with 'K Time Delay Factor ' setting, will be blocked	PSL (IN) ZSP
1088	PAP TeleTrip CR	PAP (specific application) Carrier Receive for teletransmission	PSL(IN)
1089	PAP TeleT. Heath	PAP (specific application) Carrier Out of Service (DT trip decision)	PSL(IN)
1090	PAP Timer Block	Timer Block for frosen every timer initiated with PAP (specific application) function	PSL(IN)
1091	Reset Thermal	Reset Thermal Overload Protection	PSL(IN)
1092	Time Synch	External time synchronisation input	PSL(IN)
1093	Select CS(NCIT)	Select Check synchro for NCIT	PSL
1094	T1 Timer Block	Timer block T1 input	PSL
1095	T2 Timer Block	Timer block T2 input	PSL
1096	TZp Timer Block	Timer block TZp input	PSL
1097	TZq Timer Block	Timer block TZq input	PSL
1098	T3 Timer Block	Timer block T3 input	PSL
1099	T4 Timer Block	Timer block T4 input	PSL
1100	F<1 Timer Block	Timer block underfrequency stage 1	PSL (IN)
1101	F<2 Timer Block	Timer block underfrequency stage 2	PSL (IN)
1102	F<3 Timer Block	Timer block underfrequency stage 3	PSL (IN)
1103	F<4 Timer Block	Timer block underfrequency stage 4	PSL (IN)
1104	F>1 Timer Block	Timer block overfrequency stage 1	PSL (IN)
1105	F>2 Timer Block	Timer block overfrequency stage 2	PSL (IN)
1106	I<1 Block	Block phase undercurrent stage 1	PSL (IN)
1107	I<2 Block	Block phase undercurrent stage 2	PSL (IN)
1108	I<1 Timer Block	Timer block phase undercurrent stage 1	PSL (IN)

Ordinal	English Text	Description	Source
1109	I<2 Timer Block	Timer block phase undercurrent stage 2	PSL (IN)
1110	103 MontorBlock	For IEC-870-5-103 protocol only, used for "Monitor Blocking" (relay is quiet - issues no messages via SCADA port)	PSL
1111	103 CommandBlock	For IEC-870-5-103 protocol only, used for "Command Blocking" (relay ignores SCADA commands)	PSL
1112	RP1 Read Only	All setting changes and most command/control actions blocked for Rear Port 1.	PSL
1113	RP2 Read Only	All setting changes and most command/control actions blocked for Rear Port 2.	PSL
1114	NIC Read Only	All setting changes and most command/control actions blocked for the Ethernet port (when option available).	PSL
1115	SBO InterLock 1	SBO support for IEC 61850-8-1 control function with interlocking facilities 1	PSL
1116	SBO DPI1 Org1	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 1	PSL
1117	SBO DPI2 Org1	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 1	PSL
1118	SBO Command1	SBO support for IEC 61850-8-1 function command 1	PSL
1119	SBO InterLock 2	SBO support for IEC 61850-8-1 control function with interlocking facilities 2	PSL
1120	SBO DPI1 Org2	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 2	PSL
1121	SBO DPI2 Org2	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 2	PSL
1122	SBO Command2	SBO support for IEC 61850-8-1 function command 2.	PSL
1123	SBO InterLock 3	SBO support for IEC 61850-8-1 control function with interlocking facilities 3	PSL
1124	SBO DPI1 Org3	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 3	PSL
1125	SBO DPI2 Org3	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 3	PSL
1126	SBO Command3	SBO support for IEC 61850-8-1 function command 3	PSL
1127	SBO InterLock 4	SBO support for IEC 61850-8-1 control function with interlocking facilities 4	PSL
1128	SBO DPI1 Org4	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 4	PSL
1129	SBO DPI2 Org4	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 4	PSL
1130	SBO Command4	SBO support for IEC 61850-8-1 function command 4.	PSL
1131 to 1223	--	Unused	PSL
1224	Virtual Input 1	Goose input n° 1 - Allows binary signals that are mapped to virtual inputs to interface into PSL	SW
1225 to 1287	Virtual Input 2 to Virtual Input 64	Goose input n° 2 to Goose input n° 32	SW
1288 to 1352	--	Unused	PSL
1353 to 1415	Quality VIP 1 to Quality VIP 64	Validation of the virtual input 1 (to 64) (signal correct).	PSL
1416 to 1479	--	Unused	PSL
1480 to 1543	PubPres VIP 1 to PubPres VIP 64	Publishing presence of virtual input 1 (to 64): indicates virtual input 1 (to 64) presence.	PSL

Ordinal	English Text	Description	Source
1544 to 2047	--	Unused (except next DDBs for specific options)	PSL
1672 to 1677	LN1 Analog Alarm to LN6 Analog Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL
1680 to 1685	LN1 Test Mode to LN6 Test Mode	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is in “Test Mode”	PSL
1688 to 1693	LN1 Async to LN6 Async	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is synchronized with Internal (local) synchronization	PSL
1696 to 1701	LN1 Val Quest to LN6 Val Quest	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “questionable”	PSL
1704 to 1709	LN1 Val Fail to LN6 Val Fail	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “failed”	PSL

1.1.2 Sorted by name

Ordinal	English Text	Description	Source
1111	103 CommandBlock	For IEC-870-5-103 protocol only, used for "Command Blocking" (relay ignores SCADA commands)	PSL
1110	103 MontorBlock	For IEC-870-5-103 protocol only, used for "Monitor Blocking" (relay is quiet - issues no messages via SCADA port)	PSL
328	1P Trip	Single pole trip (internal or external)	PSL (OUT) All protection
318	1ph Fault	Single phase fault	PSL (OUT) Distance
319	2ph Fault	Two phase fault	PSL (OUT) Distance
329	3P Trip	Three pole trip (internal or external)	PSL (OUT) All protection
320	3ph Fault	Three phase fault	PSL (OUT) Distance
224	A/R 1P In Prog	One-pole autoreclose cycle in progress: A single pole autoreclose cycle is in progress. This output will remain activated from the initial protection trip until the circuit breaker is closed successfully or the autoreclose function is Locked Out, indicating that a dead time timeout is in progress. This signal may be useful during relay commissioning to check the operation of the autoreclose cycle.	PSL (OUT) Autorecloser
226	A/R 1st In Prog	First high speed autoreclose cycle in progress: Used to indicate the autorecloser is timing out its first dead time, either a high-speed single-pole shot or a high speed three-pole shot.	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
227	A/R 234 In Prog	Further autoreclose cycles in progress: Used to indicate the autorecloser is timing out delayed autoreclose dead times for shots 2, 3 or 4. Where some protection elements should not initiate autoreclosure for Delayed Autoreclose (DAR) shots, the protection element operation is combined with 'A/R 234 in Prog' as a logic AND operation in the Programmable Scheme Logic, and then set to assert the DDB:'BAR' input, forcing lockout.	PSL (OUT) Autorecloser
225	A/R 3P In Prog	Three-pole autoreclose cycle in progress: A three phase autoreclose cycle is in progress. This output will remain activated from the initial protection trip until the circuit breaker is closed successfully or the AR function is Locked Out, indicating that a dead time timeout is in progress. This signal may be useful during relay commissioning to check the operation of the autoreclose cycle.	PSL (OUT) Autorecloser
223	A/R Close	Autorecloser Close command to CB: Initiates the reclose command pulse to the circuit breaker. This output feeds a signal to the Reclose time-delay, which maintains the linked reclose contact closed for a time sufficient to ensure reliable CB mechanism operation. This DDB signal may also be useful during relay commissioning to check the operation of the autoreclose cycle. Where three single pole circuit breakers are used, the AR Close contact will need to energise the closing circuits for all three breaker poles (or alternatively assign three CB Close contacts).	PSL (OUT) Autorecloser
231	A/R Enable	Indicates the autoreclose function is in service 1 = [If 'A/R SPAR Enable' OR 'A/R TPAR Enable'] AND "Internal A/R' = enabled (setting) Reset to 0: If 'A/R SPAR Enable'=0 AND 'A/R TPAR Enable'=0 (if assigned in PSL) + "Internal A/R' = disabled (setting)	PSL (OUT) Autorecloser
196	A/R Fail	No check sync / autorecloser failed: If the check sync conditions are not met prior to reclosing within the time window, the 'A/R Fail' alarm will be raised.	PSL (OUT) Autorecloser
235	A/R Force Sync.	Force synchronism check to be made (simulate the CheckSync control and forces the DDB:'CheckSync OK' (logic output) to 1 during a 1-pole or 3-pole high speed autoreclose cycle) The signal is reset with A/R reclaim	PSL (OUT) Autorecloser
1033	A/R Internal	Give internal autorecloser present (visible): If it is assigned to an opto input in the PSL and energised, the DDB:'A/R Internal' will enable the internal AR logic. This opto input could be connected to an external condition such as the Watchdog of the Main1 protection – this activates the internal AR of Main 2 (P44x) in the case of an internal failure of the Main1.	PSL (IN) Autorecloser

Ordinal	English Text	Description	Source
234	A/R Lockout	Autorecloser locked-out (no autoreclosure possible until reset), If protection operates during the reclaim time, after the final reclose attempt, the relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition is reset. This will produce an alarm: A/R Lockout. Then, the DDB:'BAR' input will block the autorecloser and cause a lockout if a reclose cycle is in progress. Lockout will also occur if the CB energy is low and the CB fails to close. Once the autorecloser is locked out, it will not function until a Reset Lockout or CB Manual Close command is received (depending on the Reset Lockout method chosen in CB Monitor Setup). NOTE: Lockout can also be caused by the CB condition monitoring functions maintenance lockout, excessive fault frequency lockout, broken current lockout, CB failed to trip and CB failed to close, manual close no check synchronism and CB unhealthy. Set to 1 = 'A/R Enable' AND [('BAR' =1 (see internal logic) OR ' A/R lockout shot> (AR lockout by number of shots) OR (No CB Healthy at the end of Inhibit Window (setting)) OR (No 'CB discrepancy' (opto input or internal by CBAux if present in PSL) at the end of 1P Dead time1) OR Trip 1P or3P maintained / still present at the end of the1P or 3P Dead time) or after discrimination time-delay if a 3-pole trip occurs during a 1-Pole AR Cycle] At 0: AR activated Reset to 0 = ('Reset 1P Trip' OR 'Reset 3P Trip') AND (End of reclaim time) AND Reset (BAR) AND Reset (A/R lockout shot>) AND Reset (No CB Healthy) AND Reset (No Discrepancy)	PSL (OUT) Autorecloser
229	A/R Reclaim	Internal autoreclose reclaim in progress (reclaim time timeout in progress). If it is assigned to an opto input in the PSL and when energised, the DDB:‘A/R Reclaim’ signal will start the internal logic TOR enable (External AR logic applied). The DDB indicates the reclaim time following a particular autoreclose shot is timing out. The DDB:'AR Reclaim' output would be energised at the same instant as any Cycle outputs are reset. ‘A/R Reclaim’ may be used to block low-set instantaneous protection on autoreclosure, when it has not been time-graded with a downstream protection. This technique is commonly used when the downstream devices are fuses, and fuse saving is implemented. This avoids fuse blowing for transient faults. ‘A/R reclaim’ can be connected to Main2 for cycle in progress external information. It initiates the internal TOR logic	PSL (OUT) Autorecloser

Ordinal	English Text	Description	Source
232	A/R SPAR Enable	Single pole autorecloser (SPAR) activated: If it is assigned to an opto input in the PSL (by default PSL is inverted and linked to opto 8) and energized, The DDB:'A/R SPAR Enable' will enable the 1-pole autoreclose logic (the priority of this input is higher than the 'CB Control/A/R single pole' setting) - this means the 1-pole autoreclose logic can be disabled even if it has been activated; if the relevant opto input is not energized (to be valid, the opto must be energised for over 1.2 s). NOTE: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the “A/R enable” logic state). Set to 1: 1P AR activated (copy of 'SPAR Enable' opto input OR 'CB Control/ A/R Single pole' enabled) Reset to 0: if 'SPAR Enable' = 0 OR (A/R Single pole' disabled)	PSL (OUT) Autorecloser
233	A/R TPAR Enable	Three pole autorecloser (TPAR) activated: If it is assigned to an opto input in the PSL (by default, the PSL is inverted and linked to opto 8) and energized, the DDB:'A/R TPAR Enable' will enable the 3-pole autoreclose logic (the priority is higher than the 'CB Control / A/R three pole' setting) - this means the 3-pole autoreclose logic can be disabled even if it has been activated; if the relevant opto input is not energised (to be valid, the opto input must be energised for over 1.2 s). NOTE: After a new PSL has been downloaded to the relay (including the "TPAR" or "SPAR" cells); the settings configuration must be uploaded back (from PC to relay) to update the data in the RAM and the EEPROM (otherwise discrepancies could appear in the “AR enable” logic sate). Set to 1: 3P AR activated (copy of 'TPAR enable' opto input OR 'CB Control/ A/R Three pole' enabled) Reset to 0: if 'TPAR enable' = 0 OR ('A/R Three pole' disabled)	PSL (OUT) Autorecloser
228	A/R Trip 3P	Autorecloser signal to force all trips to be 3 Ph: This is an internal logic signal used to condition any protection trip command to the circuit breaker(s). Where single-pole tripping is enabled, a fixed logic converts single-phase trips for faults on autoreclosure to three-pole trips. A/R Trip 3P can be connected to Main2 as an external "Force 3-pole" 1 = ('Internal A/R' setting enabled) AND (No 'A/R SPAR Enable') 0 = 'A/R SPAR Enable' AND ('Internal A/R' setting enabled)+ ('Inhibit Window' at 0)	PSL (OUT) Autorecloser
208	alarm user 1	Alarm user for dedicated PSL	PSL(IN)
209	alarm user 2	Alarm user for dedicated PSL	PSL(IN)
210	alarm user 3	Alarm user for dedicated PSL	PSL(IN)
211	alarm user 4	Alarm user for dedicated PSL	PSL(IN)
212	alarm user 5	Alarm user for dedicated PSL	PSL(IN)
342	All Pole Dead	All circuit breaker poles dead (breaker open 3 phase, pole status detected by Cbaux or internal thresholds). If it is linked in the PSL, the DDB:'All Pole Dead' signal indicates that all poles are dead (3 poles are open). All Pole Dead = Pole Dead A AND Pole Dead B AND Pole Dead C	PSL (OUT) Poledead
393	Any Int. Trip	Any Internal trip	PSL

Ordinal	English Text	Description	Source
322	Any Int. Trip A	Any internal protection A phase trip Default PSL: LED 1, Relay 02	PSL (OUT) All protection
323	Any Int. Trip B	Any internal protection B phase trip Default PSL: LED 2, Relay 03	PSL (OUT) All protection
324	Any Int. Trip C	Any internal protection C phase trip Default PSL: LED 3, Relay 04	PSL (OUT) All protection
341	Any Pole Dead	Any circuit breaker pole dead (one or more poles open, pole status detected by CBaux or internal thresholds). If it is linked in the PSL, the DDB:'Any Pole Dead' signal indicates that one or more poles are open. Any Pole Dead = Pole Dead A OR Pole Dead B OR Pole Dead C	PSL (OUT) Poledead
317	Any start	Any protection start logic with any phase Default PSL: LED 4, Relay 06 (Fault record trigger in default PSL with 20 ms Dwell Timer)	PSL (OUT) All protection
321	Any Trip	Single or three pole trip or external protection trip Default PSL: Relay 07	PSL (OUT) All protection
325	Any Trip A	Any trip A (internal or external protection)	PSL (OUT) All protection
326	Any Trip B	Any trip B (internal or external protection)	PSL (OUT) All protection
327	Any Trip C	Any trip C (internal or external protection)	PSL (OUT) All protection
230	AR Discrim.	'Discrimination time' window in progress (starts with the trip command). When a single pole trip is issued by the relay, a 1-pole AR cycle is initiated. The 'Dead time 1' and 'Discrimination time' are started. If the autoreclose logic detects a single pole or three-pole trip (internal or external) during the discrimination time-delay, the single pole high speed autoreclose cycle is disabled and replaced by a three pole high speed autoreclose cycle, if enabled. If no three-pole autoreclose is enabled, the relay trips 3-pole and the autoreclose is blocked. If the autoreclose logic detects a 3-pole trip (internal or external) when the Discrimination time-delay has elapsed and during the 1-pole dead time; the single pole AR cycle is stopped and the relay trips 3-pole and blocks the autoreclose.	PSL (OUT) Autorecloser
194	AR Lockout Shot>	Autoreclose lockout following final programmed attempt: Indicates a failed autoreclose (definitive trip following the last reclosing shot). The relay will be driven to lockout and the autoreclose function will be disabled until the lockout condition has been reset. An alarm, "AR Lockout Shots>" (along with AR Lockout) will be raised. 1 = 'A/R Enable' & [('1Ptrip & No 'SPAR Enable') + (3P Trip & No 'TPAR enable) + ('1P Trip' + '3P Trip') & (Number of shots=setting)]	PSL (OUT) Autorecloser
486	Back Up Setting	Back up setting alarm	PSL(OUT)
478	Bad OSI Config.	Ethernet alarm	PSL(OUT)
477	Bad TCP/IP Cfg.	Bad configuration TCP/IP Address alarm	PSL(OUT)

Ordinal	English Text	Description	Source
1038	BAR	Block internal autoreclose: Block Autoreclose (via an opto input or in the PSL). The DDB:'BAR' input will block the autoreclosure and lockout the autoreclose if a cycle is in progress. If a single-pole cycle is in progress a three-pole trip will be issued and the autorecloser will lock out. It can be used when protection operation is required without autoreclose. A typical example is for a transformer feeder, where autoreclosing may be initiated by the feeder's protection relay but blocked by the transformer's protection relay. Similarly, where a circuit breaker low gas pressure or loss of vacuum alarm occurs during the dead time, autoreclosure should be blocked – and BAR can be used to perform this blocking logic.	PSL (IN) Autorecloser
469	Battery Fail	Alarm battery fail	PSL(OUT)
1041	BLK Protection	Block all protection functions (21/67N/50/51/…)	PSL (IN) All protection
330	Brk.Conduct.Trip	Broken conductor trip	PSL (OUT) Broken Cond.
202	Brok. Cond. Alarm	Broken Conductor Alarm	PSL(OUT) Broken conductor
338	CB Aux A	CB Phase A status (from internal logic and CBAux opto inputs state: 1 = CB-Pole A is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
1025	CB Aux A (52-A)	Circuit breaker pole A closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1026	CB Aux A (52-B)	Circuit breaker pole A open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
339	CB Aux B	CB Phase B status (from internal logic and CBAux opto inputs state: 1 = CB-Pole B is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
1027	CB Aux B (52-A)	Circuit breaker pole B closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1028	CB Aux B (52-B)	Circuit breaker pole B open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
340	CB Aux C	CB Phase C status (from internal logic and CBAux opto inputs state: 1 = CB-Pole C is open. This signal is used for Any Pole Dead & All Pole Dead internal detection.	PSL (OUT) CB status
1029	CB Aux C (52-A)	Circuit breaker pole C closed (status input from CB, 52-A = normally open)	PSL (IN) CB STATUS
1030	CB Aux C (52-B)	Circuit breaker pole C open (Status input from CB, 52-B = normally closed)	PSL (IN) CB STATUS
1045	CB Discrepancy	CB Discrepancy (one pole open). If it is assigned to an opto input in the PSL and energised, the DDB:'CB Discrepancy' signal will inform the protection of a pole discrepancy status (one pole opened and the other two poles closed). It must be set to high logical level before Dead time 1 has elapsed – it can also be generated internally (see Cbaux logic).	PSL (IN) CB Status
179	CB Fail Alarm	Circuit breaker failure on any trip	PSL (OUT) Breaker Fail

Ordinal	English Text	Description	Source
1040	CB Healthy	Circuit breaker operational (gas pressure, mechanical state) Must be at 1 inside the time window (setting: group1/ Autoreclose mode/ AR Inhibit Wind) during an AR cycle ('A/R close' and 'A/R Reclaim' pick up when 'CB healthy' is detected during the 'A/R Inhibit Wind' time-delay')	PSL (IN) CB STATUS
185	CB Op Time Lock	CB locked out, due to excessive operating time: An alarm is issued when the operating tripping time on any phase pass over the 'CB monitor setup / CB Time Lockout' setting (slowest pole detection calculated by I< from CB Fail logic)	PSL (OUT) CB monitoring
184	CB Op Time Maint	CB excessive operating time alarm: An alarm is issued when the operating tripping time on any phase pass over the 'CB monitor setup / CB Time Maint' setting (slowest pole detection calculated by I< from CB Fail logic)	PSL (OUT) CB monitoring
183	CB Ops Lockout	Circuit breaker operation number lockout (2nd level alarm): An alarm is issued when the maximum of CB operations is reached [initiated by internal or external trip, see setting: 'CB Monitor Setup\N° CB Ops Lockt.] Set to 0: Until number of operations is below the 'N° CB Ops Lockt." setting. The DDB:'Reset all values' resets this counter.	PSL (OUT) CB monitoring
182	CB Ops Maint	Circuit breaker operations number alarm (1st level): An alarm is issued when the maximum of CB operations is reached. This alarm is initiated by internal (any protection function) or external trip (via opto input). The Alarm can be set with 'CB Monitor Setup / N° CB Ops Maint.' setting. Set to 0: Until number of operations is below the 'N° CB 0ps Maint.' setting. The DDB:'Reset all values' resets this counter.	PSL (OUT) CB monitoring
189	CB Status Alam	Circuit Breaker Alarm Displayed when a CB Failure or CB State unknown condition is detected (the 'System data / Plant Status' two last digits = 00 or 11). The CB discrepancy status is detected after CBA time-delay issued by opto input or internally by CBAux logic – Alarm issued after 5 s	PSL (OUT)
236	Check Synch. OK	If linked to an opto input in a dedicated PSL and energised, it indicates that external synchronism conditions are met – This can be linked afterwards to an internal autoreclose logic	PSL (OUT) Synchro Check
471	Comm2 H/W FAIL	Alarm second rear port	PSL(OUT)
336	Control Close	Control close command from user (by internal CB control)	PSL (OUT) CB control
608	Control input 1	Control Input 1 - for SCADA and menu commands into PSL	SW
609 to 639	Control input 2 to Control input 32	Control input 2 to Control input 32	SW
193	Control No C/S	Autoreclosed works without check synchronism (high when the internal Check Synchronism conditions are not met).	PSL (OUT)
335	Control Trip	Control trip command from user (by internal CB control)	PSL (OUT) CB control
201	COS Alarm	HF carrier anomaly alarm (Carrier out of service)	PSL(OUT) Unblocking logic
346	Cross Count. Flt	Cross Country Fault Set to 1: The cross country logic is activated (1 Fault Fwd/1 Fault Rev detected)	PSL (OUT) Distance

Ordinal	English Text	Description	Source
178	CT Fail Alarm	Current transformers supervision indication: Indicates a CT Fail detected after time delay has elapsed is issued	PSL (OUT) CT Supervision
241	Ctrl Cls In Prog	Manual (control) close in progress - using CB control (time-delay manual closing delay in progress).	PSL (OUT) CB Control
203	CVT Alarm	Alarm for capacitive voltage Transformer: Indicates the residual voltage is greater than the threshold adjusted in the settings, during a time-delay greater than the adjustment. That alarm is also included in the general alarm.	PSL (OUT)
274	DEF Fwd	Channel Aided DEF: forward fault	PSL (OUT) Aided DEF
273	DEF Rev	Channel Aided DEF: reverse fault	PSL (OUT) Aided DEF
271	DEF Sig. Send	DEF protection schemes - Signal Send (Default PSL: Relay 05)	PSL (OUT) Aided DEF
275	DEF Start A	Channel Aided DEF: start phase A	PSL (OUT) Aided DEF
276	DEF Start B	Channel Aided DEF: start phase B	PSL (OUT) Aided DEF
277	DEF Start C	Channel Aided DEF: start phase C	PSL (OUT) Aided DEF
1060	DEF Timer Block	Block aided DEF time delay The DEF time-delay will be blocked & DEF will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) DEF
278	DEF Trip A	Channel Aided DEF: trip phase A Default PSL: Relay 09	PSL (OUT) Aided DEF
279	DEF Trip B	Channel Aided DEF: trip phase B Default PSL: Relay 09	PSL (OUT) Aided DEF
280	DEF Trip C	Channel Aided DEF: trip phase C Default PSL: Relay 09	PSL (OUT) Aided DEF
272	DEF UNB CR	Unblocking DEF channel internal Carrier Received signal (main Directional Earth Fault unblocking signal) received.	PSL (OUT) Unblocking logic
1050	DEF. Chan Recv	Signal received on main channel for DEF scheme logic (depending on settings: Aided DEF/Scheme logic) Selected as shared by default – Can operate as an independent scheme with a separate opto input from Dist Default PSL: Opto Label 1	PSL (IN) Un-blocking logic
1052	DEF. COS	DEF scheme channel out of service / Loss of Guard Selected shared by default – Can operate as an independent scheme with a different opto input from Dist Default PSL: Opto Label 2	PSL (IN) Un-blocking logic
345	DIST Convergency	Distance protection: Internal characteristic Set to 1: logic with Distance Start at 1 (Minimum 1 loop has been detected in the quadrilateral characteristic) Set to 0: Reset of (R, X) (resistance, reactance) calculation made by the All pole Dead detection	PSL (OUT) Distance
244	DIST Fwd	Distance protection: Forward fault detected (default PSL: LED6) Set to 1: Directional Forward detected in distance algorithms (Deltas or Conventional) AND (Distance Start) Set to 0: With reset of Any Start/Dist Start	PSL (OUT) Distance

Ordinal	English Text	Description	Source
343	DIST Fwd No Filt	Distance protection: Forward fault detected not filtered (Directional Forward decision made by Distance logic without any filter by Distance Start or Zone: Picks up faster than Dist Fwd)	PSL (OUT) Distance
245	DIST Rev	Distance protection: Reverse fault detected (default PSL: LED7) Set to 1: Directional Reverse detected in distance algorithms (Deltas or Conventional) AND (Distance Start) Set to 0: With reset of Any Start/Dist Start	PSL (OUT) Distance
344	DIST Rev No Filt	Distance protection: Reverse fault detected not filtered (Directional Forward decision made by Distance logic without any filter by Distance Start or Zone: Picks up faster than Dist Fwd)	PSL (OUT) Distance
252	DIST Sch. Accel.	Distance scheme Accelerating	PSL (OUT) Distance
254	DIST Sch. Block.	Distance scheme Blocking	PSL (OUT) Distance
253	DIST Sch. Perm.	Distance scheme Permissive	PSL (OUT) Distance
242	DIST Sig. Send	Distance protection schemes - Signal Send (default PSL: Relay 05)	PSL (OUT) Distance
249	DIST Start A	Distance protection started on phase A Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
250	DIST Start B	Distance protection started on phase B Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
251	DIST Start C	Distance protection started on phase C Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection: – I Dead: Fourier algorithm calculation (3 or 4 samples requested) – V Dead calculated by CB Fail (More than 10ms requested)	PSL (OUT) Distance
354	Dist Start N	Start of distance protection for phase to ground fault	PSL (OUT)
246	DIST Trip A	Distance protection: Phase A trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80ms)	PSL (OUT) Distance
247	DIST Trip B	Distance protection: Phase B trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80ms)	PSL (OUT) Distance
248	DIST Trip C	Distance protection: Phase C trip Set to 0: Reset Dist Trip signal (fixed pulse duration is 80ms)	PSL (OUT) Distance
243	DIST UNB CR	Unblock main channel received Internal Carrier Received signal (main Distance unblocking signal) received.	PSL(OUT) Unblocking Logic
1049	DIST. Chan Recv	Signal (carrier sent by zone) received on main channel for distance scheme logic (depending on the 'Distance scheme' setting: Program mode / Standard mode)	PSL (IN) Un-blocking logic
1051	DIST. COS	Distance scheme channel out of service / Loss of Guard (Carrier out of service)	PSL (IN) Un-blocking logic

Ordinal	English Text	Description	Source
1079	DIST. Tim. Block	Block distance element time delay At 1: The distance timer will be blocked & DIST will start but will not perform a Trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Distance
1039	Ext Chk Synch OK	Authorization signal from external check Synchroniser (via opto input, with a dedicated PSL) for reclosing with internal autoreclose (indicates that Check Sync conditions are met by an external device – The DDB cell should be assigned afterwards an internal AR logic), If an opto input is assigned in the PSL, the autoreclose close command will be verified by an external check synchronism device. The input is energised when the Check Sync conditions are met.	PSL (IN) Autorecloser
1046	External Trip A	Phase A trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip A (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1047	External Trip B	Phase B trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip B (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
1048	External Trip C	Phase C trip by external protection relay. This input can be used to update the CB condition monitoring. Opto input is assigned to External Trip C (external Trip command issued by main 2 or to initiate the internal A/R backup protection). External trip is integrated in the DDB: 'Any Trip'. As for an internal trip, no dwell timer is associated to it.	PSL (IN)
428	F Inhib	Frequency Inhibition	PSL
176	F out of Range	Frequency tracking does not work correctly (provides a Frequency Out-of-Range indication)	PSL (OUT)
187	F.F. Lock	Excessive Fault Frequency CB Trip pre lockout Alarm (maximum number of fault): An alarm is issued at (n) value in the counters of Main lock out or Fault frequency	PSL (OUT) CB monitoring
186	F.F. Pre Lockout	Excessive Fault Frequency CB Trip lockout Alarm (maximum number of fault): An alarm is issued at (n-1) value in the counters of Main lock out or Fault frequency	PSL (OUT) CB monitoring
416	F<1 Start	Underfrequency stage 1 start	PSL
1100	F<1 Timer Block	Timer block underfrequency stage 1	PSL (IN)
422	F<1 Trip	Underfrequency stage 1 trip	PSL
417	F<2 Start	Underfrequency stage 2 start	PSL
1101	F<2 Timer Block	Timer block underfrequency stage 2	PSL (IN)
423	F<2 Trip	Underfrequency stage 2 trip	PSL
418	F<3 Start	Underfrequency stage 3 start	PSL
1102	F<3 Timer Block	Timer block underfrequency stage 3	PSL (IN)
424	F<3 Trip	Underfrequency stage 3 trip	PSL
419	F<4 Start	Underfrequency stage 4 start	PSL
1103	F<4 Timer Block	Timer block underfrequency stage 4	PSL (IN)

Ordinal	English Text	Description	Source
425	F<4 Trip	Underfrequency stage 4 trip	PSL
420	F>1 Start	Overfrequency stage 1 start	PSL
1104	F>1 Timer Block	Timer block overfrequency stage 1	PSL (IN)
426	F>1 Trip	Overfrequency stage 1 trip	PSL
421	F>2 Start	Overfrequency stage 2 start	PSL
1105	F>2 Timer Block	Timer block overfrequency stage 2	PSL (IN)
427	F>2 Trip	Overfrequency stage 2 trip	PSL
468	Fault_REC_TRIG	Trigger for Fault Recorder	FRT
470	Field Volt Fail	Field voltage failure (the internal 48 Vdc delivered by the relay can be used for opto input polarisation)	PSL(OUT)
781	FnKey LED 1 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 1 Green - This LED is associated with Function Key 1 - To drive function key LED, yellow DDB 780 and DDB 782 must be active at the same time	PSL
780	FnKey LED 1 Red	Hardware version K - Assignment of signal to drive output Function Key LED 1 Red - This LED is associated with Function Key 1	PSL
799	FnKey LED 10 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 10 Green	PSL
798	FnKey LED 10 Red	Hardware version K - Assignment of signal to drive output Function Key LED 10 Red	PSL
783	FnKey LED 2 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 2 Green	PSL
782	FnKey LED 2 Red	Hardware version K - Assignment of signal to drive output Function Key LED 2 Red	PSL
785	FnKey LED 3 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 3 Green	PSL
784	FnKey LED 3 Red	Hardware version K - Assignment of signal to drive output Function Key LED 3 Red	PSL
787	FnKey LED 4 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 4 Green	PSL
786	FnKey LED 4 Red	Hardware version K - Assignment of signal to drive output Function Key LED 4 Red	PSL
789	FnKey LED 5 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 5 Green	PSL
788	FnKey LED 5 Red	Hardware version K - Assignment of signal to drive output Function Key LED 5 Red	PSL
791	FnKey LED 6 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 6 Green	PSL
790	FnKey LED 6 Red	Hardware version K - Assignment of signal to drive output Function Key LED 6 Red	PSL
793	FnKey LED 7 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 7 Green	PSL
792	FnKey LED 7 Red	Hardware version K - Assignment of signal to drive output Function Key LED 7 Red	PSL
795	FnKey LED 8 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 8 Green	PSL
794	FnKey LED 8 Red	Hardware version K - Assignment of signal to drive output Function Key LED 8 Red	PSL
797	FnKey LED 9 Grn	Hardware version K - Assignment of signal to drive output Function Key LED 9 Green	PSL
796	FnKey LED 9 Red	Hardware version K - Assignment of signal to drive output Function Key LED 9 Red	PSL

Ordinal	English Text	Description	Source
1042	Force 3P Trip	Three pole tripping only: If it is assigned to an opto input in the PSL and energised, the DDB:'Force 3P Trip' signal will force the internal single-phase protection to trip three-poles (external order from Main1 to Main2 (P44x)) – the next trip will be three-pole.	PSL (IN)
676	Function Key 1	Hardware version K - Programmable Function key n° 1. In 'Normal' mode it is high on key press and in 'Toggle' mode remains high/low on single key press	SW
677 to 685	Function Key 2 to Function Key 10	Hardware version K - Function key n° 2 to Function key n° 10	SW
174	General Alarm	Groupment of all alarms	PSL (OUT)
472	GOOSE IED Absent	Absence of GOOSE message from dedicated IED	PSL(OUT)
1034	I A/R 1p In Prog	One-pole external autoreclose cycle in progress: If it is assigned to an opto input in the PSL and energised, The DDB:'A/R 1P in Prog' will block the internal DEF protection as it indicates that an external single-pole autoreclose cycle is in progress.	PSL (IN) Autorecloser
1035	I A/R 3p In Pr.	Three-pole external autoreclose cycle in progress: If it is assigned to an opto input in the PSL and energised, the DDB:'A/R 3P in Prog' will inform the P44x about the presence of an external 3P cycle. The data is useful in the case of an evolving fault.	PSL (IN) Autorecloser
1036	I A/R Close	Circuit Breaker closing order from external autoreclose: If it is assigned to an opto input in the PSL and energised, the DDB:'A/R Close' can be linked with the internal check synchronism condition to verify the external CB close command.	PSL (IN) Autorecloser
1037	I A/R Reclaim	External (opto input) autorecloser in progress: the DDB:'I A/R Reclaim' signal will inform the protection that an external reclaim time is in progress and will initiate the internal TOR logic (it is possible to create a dedicated PSL which would make it possible to use this information extension in Zone 1 extension schemes).	PSL (IN) Autorecloser
181	I^ Lockout Alarm	Broken current lockout alarm (2nd level): An alarm Lock Out is issued when the maximum broken current (2nd level) calculated by the monitoring function is reached	PSL (OUT) CB monitoring
180	I^ Maint Alarm	Broken current maintenance alarm (1st level): An alarm maintenance is issued when the maximum broken current (1st level) calculated by the CB monitoring function is reached (see setting: 'CB monitor setup / I^ Maintenance')	PSL (OUT) CB monitoring
1106	I<1 Block	Block phase undercurrent stage 1	PSL (IN)
429	I<1 Start	Undercurrent stage 1 start	PSL
1108	I<1 Timer Block	Timer block phase undercurrent stage 1	PSL (IN)
431	I<1 Trip	Undercurrent stage 1 trip	PSL
1107	I<2 Block	Block phase undercurrent stage 2	PSL (IN)
430	I<2 Start	Undercurrent stage 2 start	PSL
1109	I<2 Timer Block	Timer block phase undercurrent stage 2	PSL (IN)
432	I<2 Trip	Undercurrent stage 1 trip	PSL
301	I> Start Any A	Any overcurrent start for phase A	PSL (OUT) Phase Overc.
302	I> Start Any B	Any overcurrent start for phase B	PSL (OUT) Phase Overc.
303	I> Start Any C	Any overcurrent start for phase C	PSL (OUT) Phase Overc.

Ordinal	English Text	Description	Source
304	I>1 Start	Overcurrent stage 1 start Directional or not - with DT or IDMT curves Directional managed by Delta Algorithms VTS Block time-delay facility	PSL (OUT) Phase Overc.
1061	I>1 Timer Block	Block phase overcurrent stage 1 time delay Set to 1: 'I>1 Time Delay' will be blocked & I>1 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>1
308	I>1 Trip	Overcurrent stage 1 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>1 Trip command	PSL (OUT) Phase Overc.
305	I>2 Start	Overcurrent stage 2 start Directional or not - with DT or IDMT curves Directional managed by Delta Algorithms VTS Block time-delay facility	PSL (OUT) Phase Overc.
1062	I>2 Timer Block	Block phase overcurrent stage 2 time delay Set to 1: 'I>2 Time Delay' will be blocked & I>2 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>2
309	I>2 Trip	Overcurrent stage 2 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>2 Trip command	PSL (OUT) Phase Overc.
306	I>3 Start	Overcurrent stage 3 start Non-directional with DT curves Use without time-delay for SOTF	PSL (OUT) Phase Overc.
1063	I>3 Timer Block	Block phase overcurrent stage 3 time delay Set to 1: 'I>3 Time Delay' will be blocked & I>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>3
310	I>3 Trip	Overcurrent stage 3 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>3 Trip command	PSL (OUT) Phase Overc.
307	I>4 Start	Overcurrent stage 4 start Non-directional with DT curves Use without time-delay for SOTF	PSL (OUT) Phase Overc.
1064	I>4 Timer Block	Block phase overcurrent stage 4 time delay Set to 1: 'I>4 Time Delay' will be blocked & I>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) I>4
311	I>4 Trip	Overcurrent stage 4 trip (3P issued when the associated time-delay has elapsed). Set to 0: Reset I>4 Trip command	PSL (OUT) Phase Overc.
299	I2> Start	Negative Sequence Current Detection – Start function (the associated time-delay picks up) Directional or not - with DT curves Negative-sequence polarisation	PSL (OUT) Neg Seq. O/C
300	I2> Trip	Negative Sequence Current Trip – 3P trip command issued when the associated time-delay has elapsed	PSL (OUT) Neg Seq. O/C
1065	I2>1 Timer Block	Block negative sequence overcurrent stage 1 time delay	PSL (IN) I>4
383	I2>2 Start	Negative overcurrent stage 2 pick-up	PSL
1066	I2>2 Timer Block	Block negative sequence overcurrent stage 2 time delay	PSL (IN) I>5

Ordinal	English Text	Description	Source
386	I2>2 Trip	Negative overcurrent stage 2 trip	PSL
384	I2>3 Start	Negative overcurrent stage 3 pick-up	PSL
1067	I2>3 Timer Block	Block negative sequence overcurrent stage 3 time delay	PSL (IN) I>6
387	I2>3 Trip	Negative overcurrent stage 3 trip	PSL
385	I2>4 Start	Negative overcurrent stage 4 pick-up	PSL
1068	I2>4 Timer Block	Block negative sequence overcurrent stage 4 time delay	PSL (IN) I>7
388	I2>4 Trip	Negative overcurrent stage 4 trip	PSL
485	IM Channel Fail	InterMiCOM message channel fail	PSL(OUT)
484	IM Data CD Fail	InterMiCOM data channel detect fail	PSL(OUT)
482	IM Loopback	InterMiCOM indication that loopback testing is in progress	PSL(OUT)
483	IM Message Fail	InterMiCOM message failure alarm	PSL(OUT)
283	IN>1 Start	Earth fault stage 1 start – Start function (the associated time-delay picks up) Directional or not - with DT or IDMT curves Negative or positive sequence polarization Set to 0: Reset with IN below the threshold IN>1 Hysteresis	PSL (OUT) Earth Fault 1
1056	IN>1 Timer Block	Block earth fault stage 1 time delay Set to 1: 'IN>1 Time Delay' will be blocked & IN>1 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
281	IN>1 Trip	Earth fault stage 1 trip – 3-pole trip command issued when the associated time-delay has elapsed	PSL (OUT) Earth Fault 1
284	IN>2 Start	Earth fault stage 2 start – Start function (the associated time-delay picks up) Directional or not - with DT or IDMT curves Negative or positive sequence polarization Set to 0: Reset with IN below the threshold IN>2 Hysteresis	PSL (OUT) Earth Fault 2
1057	IN>2 Timer Block	Block earth fault stage 2 time delay Set to 1: 'IN>2 Time Delay' will be blocked & IN>2 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
282	IN>2 Trip	Earth fault stage 2 trip – 3-pole trip command issued when the associated time-delay has elapsed Default PSL: Relay 09.	PSL (OUT) Earth Fault 2
357	IN>3 Start	Start of IN>3 function (timer initiated)	PSL (OUT)
1058	IN>3 Timer Block	Block earth fault stage 3 time delay Set to 1: 'IN>3 Time Delay' will be blocked & IN>3 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
355	IN>3 Trip	Trip decision from IN>3 function (timer issued) Default PSL: Relay 09	PSL (OUT)
358	IN>4 Start	Start of IN>4 function (timer initiated)	PSL (OUT)
1059	IN>4 Timer Block	Block earth fault stage 4 time delay Set to 1: The IN>4 time-delay will be blocked & IN>4 will start but will not issue any trip command. Reset to 0: opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) Earth Fault
356	IN>4 Trip	Trip decision from IN>4 function (timer issued)	PSL (OUT)

Ordinal	English Text	Description	Source
576	InterMiCOM in 1	InterMiCOM IM1 Signal Input - is driven by a message from the remote line end	SW
577 to 583	InterMiCOM in 2 to InterMiCOM in 8	InterMiCOM IM2 Signal Input to InterMiCOM IM8 Signal Input	SW
584	InterMiCOM out 1	InterMiCOM IM1 Signal output - mapping what will be sent to the remote line end	PSL
585 to 591	InterMiCOM out 2 to InterMiCOM out 8	InterMiCOM IM2 Signal output to InterMiCOM IM8 Signal output	PSL
481	IP Addr Conflict	Ethernet IP Address Conflict alarm	PSL(OUT)
640	LED 1	Hardware version J - Programmable LED n° 1 is energized.	SW
641	LED 1 Grn	Hardware version K - Programmable Green LED n° 1 is energized ANY TRIP A in the default PSL	SW
765	LED 1 Grn Condit	Hardware version K - Assignment of signal to drive output LED 1 green	PSL
640	LED 1 Red	Hardware version K - Programmable Red LED n° 1 is energized. ANY TRIP A in the default PSL	SW
764	LED 1 Red Condit	Hardware version K - Assignment of signal to drive output LED 1 red - To drive LED1 Yellow DDB 764 and DDB 765 must be driven at the same time	PSL
659	LED 10 Grn	Hardware version K - Programmable Green LED n° 10	SW
658	LED 10 Red	Hardware version K - Programmable Red LED n° 10	SW
661	LED 11 Grn	Hardware version K - Programmable Green LED n° 11	SW
660	LED 11 Red	Hardware version K - Programmable Red LED n° 11	SW
663	LED 12 Grn	Hardware version K - Programmable Green LED n° 12	SW
662	LED 12 Red	Hardware version K - Programmable Red LED n° 12	SW
665	LED 13 Grn	Hardware version K - Programmable Green LED n° 13	SW
664	LED 13 Red	Hardware version K - Programmable Red LED n° 13	SW
667	LED 14 Grn	Hardware version K - Programmable Green LED n° 14	SW
666	LED 14 Red	Hardware version K - Programmable Red LED n° 14	SW
669	LED 15 Grn	Hardware version K - Programmable Green LED n° 15	SW
668	LED 15 Red	Hardware version K - Programmable Red LED n° 15	SW
671	LED 16 Grn	Hardware version K - Programmable Green LED n° 16	SW
670	LED 16 Red	Hardware version K - Programmable Red LED n° 16	SW
673	LED 17 Grn	Hardware version K - Programmable Green LED n° 17	SW
672	LED 17 Red	Hardware version K - Programmable Red LED n° 17	SW
675	LED 18 Grn	Hardware version K - Programmable Green LED n° 18	SW
674	LED 18 Red	Hardware version K - Programmable Red LED n° 18	SW
641	LED 2	Hardware version J - Programmable LED n° 2 is energized.	SW
643	LED 2 Grn	Hardware version K - Programmable Green LED n° 2 is energized ANY TRIP B in the default PSL	SW
767	LED 2 Grn Condit	Hardware version K - Assignment of signal to drive output LED 2 green	PSL
642	LED 2 Red	Hardware version K - Programmable Red LED n° 2 is energized ANY TRIP B in the default PSL	SW
766	LED 2 Red Condit	Hardware version K - Assignment of signal to drive output LED 2 red	PSL
642	LED 3	Hardware version J - Programmable LED n° 3 is energized.	SW

Ordinal	English Text	Description	Source
645	LED 3 Grn	Hardware version K - Programmable Green LED n° 3 ANY TRIP C in the default PSL	SW
769	LED 3 Grn Condit	Hardware version K - Assignment of signal to drive output LED 3 green	PSL
644	LED 3 Red	Hardware version K - Programmable Red LED n° 3 ANY TRIP C in the default PSL	SW
768	LED 3 Red Condit	Hardware version K - Assignment of signal to drive output LED 3 red	PSL
643	LED 4	Hardware version J - Programmable LED n° 4 is energized.	SW
647	LED 4 Grn	Hardware version K - Programmable Green LED n° 4 General Start in the default PSL	SW
771	LED 4 Grn Condit	Hardware version K - Assignment of signal to drive output LED 4 green	PSL
646	LED 4 Red	Hardware version K - Programmable Red LED n° 4 General Start in the default PSL	SW
770	LED 4 Red Condit	Hardware version K - Assignment of signal to drive output LED 4 red	PSL
644	LED 5	Hardware version J - Programmable LED n° 5 is energized.	SW
649	LED 5 Grn	Hardware version K - Programmable Green LED n° 5 Z1+Aided Trip in the default PSL	SW
773	LED 5 Grn Condit	Hardware version K - Assignment of signal to drive output LED 5 green	PSL
648	LED 5 Red	Hardware version K - Programmable Red LED n° 5 Z1+Aided Trip in the default PSL	SW
772	LED 5 Red Condit	Hardware version K - Assignment of signal to drive output LED 5 red	PSL
645	LED 6	Hardware version J - Programmable LED n° 6 is energized.	SW
651	LED 6 Grn	Hardware version K - Programmable Green LED n° 6 Dist Fwd in the default PSL	SW
775	LED 6 Grn Condit	Hardware version K - Assignment of signal to drive output LED 6 green	PSL
650	LED 6 Red	Hardware version K - Programmable Red LED n° 6 Dist Fwd in the default PSL	SW
774	LED 6 Red Condit	Hardware version K - Assignment of signal to drive output LED 6 red	PSL
646	LED 7	Hardware version J - Programmable LED n° 7 is energized.	SW
653	LED 7 Grn	Hardware version K - Programmable Green LED n° 7 Dist Rev in the default PSL	SW
777	LED 7 Grn Condit	Hardware version K - Assignment of signal to drive output LED 7 green	PSL
652	LED 7 Red	Hardware version K - Programmable Red LED n° 7 Dist Rev in the default PSL	SW
776	LED 7 Red Condit	Hardware version K - Assignment of signal to drive output LED 7 red	PSL
647	LED 8	Hardware version J - Programmable LED n° 8 is energized.	PSL
655	LED 8 Grn	Hardware version K - Programmable Green LED n° 8 Autoreclose Enable in the default PSL	SW
779	LED 8 Grn Condit	Hardware version K - Assignment of signal to drive output LED 8 green	PSL
654	LED 8 Red	Hardware version K - Programmable Red LED n° 8 Autoreclose Enable in the default PSL	SW

Ordinal	English Text	Description	Source
778	LED 8 Red Condit	Hardware version K - Assignment of signal to drive output LED 8 red	PSL
657	LED 9 Grn	Hardware version K - Programmable Green LED n° 9	SW
656	LED 9 Red	Hardware version K - Programmable Red LED n° 9	SW
656	LED Cond IN 1	Hardware version J - Assignment of signal to drive output Function Key LED 1	PSL
657	LED Cond IN 2	Hardware version J - Assignment of signal to drive output Function Key LED 2	PSL
658	LED Cond IN 3	Hardware version J - Assignment of signal to drive output Function Key LED 3	PSL
659	LED Cond IN 4	Hardware version J - Assignment of signal to drive output Function Key LED 4	PSL
660	LED Cond IN 5	Hardware version J - Assignment of signal to drive output Function Key LED 5	PSL
661	LED Cond IN 6	Hardware version J - Assignment of signal to drive output Function Key LED 6	PSL
662	LED Cond IN 7	Hardware version J - Assignment of signal to drive output Function Key LED 6	PSL
663	LED Cond IN 8	Hardware version J - Assignment of signal to drive output Function Key LED 7	PSL
1672 to 1677	LN1 Analog Alarm to LN6 Analog Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL
1688 to 1693	LN1 Async to LN6 Async	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is synchronized with Internal (local) synchronization	PSL
1680 to 1685	LN1 Test Mode to LN6 Test Mode	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) Any Logical Node is in “Test Mode”	PSL
1704 to 1709	LN1 Val Fail to LN6 Val Fail	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “failed”	PSL
1696 to 1701	LN1 Val Quest to LN6 Val Quest	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) The sample value (SV) transmitted status from the LN is “questionable”	PSL
188	Lockout Alarm	Lockout alarm: An alarm is issued with: ‘Man CB Unhealthy’or no 'Check Sync OK' (CB conditioning) or ‘Man CB Cls Fail’ or ‘Man CB Fail Trip’ or 'F.F. Lock' or 'CB Op Time Lock' or 'CB Ops Lockout'	PSL (OUT)
331	Loss. Load Trip	Loss of load trip (in application without communication scheme and a 3P Trip logic)	PSL (OUT) Loss of load
191	Man CB Cls Fail	Alarm CB fail for manual closing command	PSL (OUT)
190	Man CB Trip Fail	Alarm CB Fail for manual trip command	PSL (OUT)
192	Man CB Unhealthy	Alarm CB performed by unhealthy condition	PSL (OUT)

Ordinal	English Text	Description	Source
1043	Man. Close CB	Circuit breaker manual close - order received. 'If it is assigned to an opto input in the PSL and energised the DDB:'Man Close CB' signal will enable the internal 'SOTF Enable' logic without CB control activation. If CB control is activated, SOTF will be enabled by internal detection ('CB close' order managed by CB control). Manual closure of the circuit breaker will force the autorecloser in a lockout logic, if selected in the 'Distance schemes / TOR-SOTF Mode') menu. Any fault detected within 500ms of a manual closure will cause an instantaneous three pole tripping, without autoreclose (see Block Autoreclose (BAR) logic) When autoreclose lockout (BAR) is activated, the autorecloser does not initiate any additional reclosing cycle. If autoreclose lockout picks up during a cycle, the A/R close is blocked. This prevents excessive circuit breaker operations, which could result in increased circuit breaker and system damage, when closing onto a fault.	PSL (IN) CB Status
1044	Man. Trip CB	Circuit breaker manual trip - order received. If it is assigned to an opto input in the PSL and energised, the DDB:'Man Trip CB' signal will inform the protection of an external CB trip command by the CB control function (if activated).	PSL (IN) CB Status
1055	MCB/VTS Main	Fuse failure on line VT or MCB open (blocks voltage dependant functions). If it is linked to an opto input in the PSL energised, the DDB informs the P44x about an internal maloperation from the VT used for the impedance measurement reference (line in this case means Main VT ref measurement, even if the main VT is on the bus side and the Synchronism check VT is on the line side).	PSL (IN) VTS
1054	MCB/VTS Synchro	Fuse failure on busbar VT or MCB open (blocks voltage dependant functions), If it is linked to an opto input in the PSL and energised, the DDB signal informs the P44x about an internal maloperation from the VT used for synchronisation check (see Check Synchronism logic section).	PSL (IN) VTS
204	NCIT Alarm	Relays with IEC 61850 9-2 Ethernet board only (software version D5.x) IEC 61850 9-2 Alarm - Frame from Merge Units missing. If two consecutive of any Logical Node frames have not been received within the Merge Unit Delay set parameter (time of silence in the reception of the frame), the LN is “absent”	PSL (OUT)
475	NIC Fatal Error	Fatal Error from Ethernet Board alarm	PSL(OUT)
479	NIC Link Fail	Ethernet Link Fail alarm	PSL(OUT)
474	NIC No Response	No response from Ethernet Board alarm.	PSL(OUT)
473	NIC Not Fitted	Ethernet (board not fitted) alarm	PSL(OUT)
1114	NIC Read Only	All setting changes and most command/control actions blocked for the Ethernet port (when option available).	PSL
476	NIC Soft. Reload	Ethernet Board (Configuration in progress) alarm	PSL(OUT)
480	NIC SW Mis-Match	Not compatible Ethernet version alarm	PSL(OUT)

Ordinal	English Text	Description	Source
64	Opto Label 01	OPTO ISOLATOR 1 Set to 1 when the opto input is energised for a minimum time: 7ms (48Vdc), 10ms (universal) to be validated by internal logic To enable the selection of a setting group by state change of the opto isolated logic inputs 1 and 2, disconnect Opto inputs 01 and 02 in the PSL (Opto inputs 01 and 02 must not be connected to any output signal)	OPTO
65	Opto Label 02	OPTO ISOLATOR 2 Set to 1 when the opto input is energised for a minimum time: 7ms (48Vdc), 10ms (universal) to be validated by internal logic To enable the selection of a setting group by state change of the opto isolated logic inputs 1 and 2, disconnect Opto inputs 01 and 02 in the PSL (Opto inputs 01 and 02 must not be connected to any output signal)	OPTO
66 to 95	Opto Label 03 to Opto Label 32	OPTO ISOLATOR 3 to OPTO ISOLATOR 32 Set to 1 when the opto input is energised for a minimum time:7ms (48Vdc), 10ms (universal) to be validated by internal logic	OPTO
350	Out Of Step	Start of an Out of Step Detection (1st cycle), The first out of step cycle has been detected (Zlocus in/out with the opposite R sign) & the « Out Of Step start » picks-up	PSL (OUT)
352	Out Of Step Conf	Out of Step Confirmed (number of cycles reached)	PSL (OUT)
700 to 763	Output cond. 1 to Output cond. 64	Input to Relay Output Conditioner	PSL
367	PAP Pre Start	PAP (specific application) Picks up by voltage detectors (timer initiated)	PSL (OUT)
366	PAP Pres IN	Residual current detected by PAP (specific application) function	PSL (OUT)
363	PAP Start A	Phase A Start with PAP (specific application) function	PSL (OUT)
364	PAP Start B	Phase B Start with PAP (specific application) function	PSL (OUT)
365	PAP Start C	Phase C Start with PAP (specific application) function	PSL (OUT)
1089	PAP TeleT. Heath	PAP (specific application) Carrier Out of Service (DT trip decision)	PSL(IN)
1088	PAP TeleTrip CR	PAP (specific application) Carrier Receive for teletransmission	PSL(IN)
1090	PAP Timer Block	Timer Block for frozen every timer initiated with PAP (specific application) function	PSL(IN)
359	PAP Trip A	Trip A Phase decision from PAP (specific application) function	PSL (OUT)
360	PAP Trip B	Trip B Phase decision from PAP (specific application) function	PSL (OUT)
361	PAP Trip C	Trip C Phase decision from PAP (specific application) function	PSL (OUT)
362	PAP Trip IN	Trip decision from PAP (specific application) function (Ground Fault detected)	PSL (OUT)
269	Power Swing	Power swing detected (3 single phase loop inside the quad & crossing the ΔR band in less than 5ms in a 50 Hz network). Power swing is present either with out of step cycle or stable swing cycle.	PSL (OUT) Distance
175	Prot'n Disabled	Protection is disabled and test mode enabled	PSL (OUT)
1480 to 1543	PubPres VIP 1 to PubPres VIP 64	Publishing presence of virtual input 1 (to 64): indicates virtual input 1 (to 64) presence.	PSL
1353 to 1415	Quality VIP 1 to Quality VIP 64	Validation of the virtual input 1 (to 64) (signal correct).	PSL

Ordinal	English Text	Description	Source
0 to 63	Relay Label 01 to Relay Label 64	OUTPUT RELAY 1 to OUTPUT RELAY 64 High level when a DDB cell (linked by PSL logic) is at 1. State depends on the logic set in the PSL (MiCOM S1 Agile) These programmable relays are assigned in the default PSL, with the following logic conditions (see section 1.8.2): - Pulse time-delay - Pick Up/Drop Off Time-delay - Dwell Time-delay - Pick Up Time-delay - Drop Off Time-delay - Latching - Straight (used in default PSL)	RELAY
1081	Reset All values	Reset all values of CB monitoring (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1082	Reset Latches	Reset all permanent alarms + LEDs and relays are latched	PSl (IN)
1080	Reset Lockout	Reset all CB monitoring lockout (all counters and values are reset ('CB condition')	PSL (IN) CB Monitoring
1091	Reset Thermal	Reset Thermal Overload Protection	PSL(IN)
270	Reversal Guard	Current reversal guard logic in action (Directional switching from Rev to Fwd in parallel line application)	PSL (OUT) Distance
1112	RP1 Read Only	All setting changes and most command/control actions blocked for Rear Port 1.	PSL
1113	RP2 Read Only	All setting changes and most command/control actions blocked for Rear Port 2.	PSL
351	S. Swing	Start of Stable Swing (1st cycle): The first stable swing cycle has been detected (Zlocus in/out with the same R sign) & the « Stable Swing start » picks-up	PSL (OUT)
353	S. Swing Conf	Stable Swing confirmed (number of cycles reached)	PSL (OUT)
437	SBO Closed Org 1	Select Before Operate (SBO) closing function for organ 1 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
438	SBO Closed Org 2	Select Before Operate (SBO) closing function for organ 2 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
439	SBO Closed Org 3	Select Before Operate (SBO) closing function for organ 3 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
440	SBO Closed Org 4	Select Before Operate (SBO) closing function for organ 4 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
1118	SBO Command1	SBO support for IEC 61850-8-1 function command 1	PSL
1122	SBO Command2	SBO support for IEC 61850-8-1 function command 2.	PSL
1126	SBO Command3	SBO support for IEC 61850-8-1 function command 3	PSL
1130	SBO Command4	SBO support for IEC 61850-8-1 function command 4.	PSL
1116	SBO DPI1 Org1	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 1	PSL
1120	SBO DPI1 Org2	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 2	PSL
1124	SBO DPI1 Org3	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 3	PSL
1128	SBO DPI1 Org4	SBO support for IEC 61850-8-1 function. SBO Double Point Information 1 Organe 4	PSL
1117	SBO DPI2 Org1	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 1	PSL
1121	SBO DPI2 Org2	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 2	PSL

Ordinal	English Text	Description	Source
1125	SBO DPI2 Org3	SBO support for IEC 61850-8-1 function SBO Double Point Information 2 Organe 3	PSL
1129	SBO DPI2 Org4	SBO support for IEC61850-8-1 function SBO Double Point Information 2 Organe 4	PSL
1115	SBO InterLock 1	SBO support for IEC 61850-8-1 control function with interlocking facilities 1	PSL
1119	SBO InterLock 2	SBO support for IEC 61850-8-1 control function with interlocking facilities 2	PSL
1123	SBO InterLock 3	SBO support for IEC 61850-8-1 control function with interlocking facilities 3	PSL
1127	SBO InterLock 4	SBO support for IEC61850-8-1 control function with interlocking facilities 4	PSL
433	SBO Open Org 1	Select Before Operate (SBO) opening function for organ 1 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
434	SBO Open Org 2	Select Before Operate (SBO) opening function for organ 2 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
435	SBO Open Org 3	Select Before Operate (SBO) opening function for organ 3 (interlocking facility in the IEC60870-5-103 protocol)	PSL
436	SBO Open Org 4	Select Before Operate (SBO) opening function for organ 4 (interlocking facility in the IEC 60870-5-103 protocol)	PSL
1093	Select CS(NCIT)	Select Check synchro for NCIT	PSL
195	SG-opto Invalid	Setting group (selected via opto inputs 1 & 2) invalid	PSL (OUT)
312	SOTF Enable	Switch On To Fault enabled: Indicates the SOTF logic is enabled in the relay Set to 1 = [SOTF not disabled (Setting 'Distance schemes / TOR-SOTF Mode')] AND [{ All poles dead AND (SOTF time-delay elapsed (110 s/default)) } OR Input Man Close] OR (CB control & Close in progress)] Reset = 500ms time-delay elapsed after Any pole Dead OR Reset of one condition requested for SOTF enable	PSL (OUT) SOTF
332	SOTF/TOR Trip	Switch on to fault trip or trip on reclose: indicates that a 3-pole trip order has been issued by the TOR or SOTF logic	PSL (OUT) SOTF
1031	SPAR Enable	Enable internal single pole autorecloser. Set with Opto input (if linked by PSL) is energized (> 1s). At 1: 1P AR internal is enabled in the AR logic At 0: AR 1P internal is disabled (even if set in MiCOM S1 Agile). AR logic becomes 3P only with AR 3P cycle -if TPAR =1	PSL (IN) Autorecloser
1083	Stub Bus Enable	Enable I>4 Element for stub bus protection (isolator of HV line open - status isolator must be connected to an opto input)	PSL (IN)
207	Synchro Acq Al.	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x - Any Logical Node is synchronized with external (global) synchronization	PSL (OUT)
261	T1	Distance time-delay in zone 1 tZ1 elapsed (1 = end of timer) If T1=0 picks up when the relay starts (Distance Start or preset)	PSL (OUT) Distance
1094	T1 Timer Block	Timer block T1 input	PSL

Ordinal	English Text	Description	Source
262	T2	Distance time-delay in zone 2 tZ2 elapsed (1 = end of timer)	PSL (OUT) Distance
1095	T2 Timer Block	Timer block T2 input	PSL
263	T3	Distance time-delay in zone 3 tZ3elapsed (1 = end of timer)	PSL (OUT) Distance
1098	T3 Timer Block	Timer block T3 input	PSL
264	T4	Distance time-delay in zone 4 tZ4 elapsed (1 = end of timer)	PSL (OUT) Distance
1099	T4 Timer Block	Timer block T4 input	PSL
333	tBF1 Trip	Circuit Breaker failure on any trip, delayed by "CB Fail 1 Timer" (setting in "CB Fail" logic)	PSL (OUT) Breaker failure
334	tBF2 Trip	Circuit Breaker failure on any trip, delayed by "CB Fail 2 Timer" (setting in "CB Fail" logic)	PSL (OUT) Breaker failure
206	Test Mode Acq	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x - Any Logical Node is in “Test Mode”	PSL (OUT)
369	Thermal Alarm	Alarm from Thermal Overload function picks up	PSL (OUT)
1092	Time Synch	External time synchronisation input	PSL(IN)
830 to 845	Timer in 1 to Timer in 16	Hardware version K - PSL Input to Auxiliary Timer 1 to PSL Input to Auxiliary Timer 16	Auxiliary Timer
830 to 861	Timer in 1 to Timer in 16	Hardware version J - PSL Input to Auxiliary Timer 1 to PSL Input to Auxiliary Timer 32	Auxiliary Timer
862 to 893	Timer in 1 to Timer in 16	Hardware version J - PSL Output from Auxiliary Timer 1 to PSL Output from Auxiliary Timer 32	Auxiliary Timer
846 to 861	Timer out 1 to Timer out 16	Hardware version K - PSL Ouput from Auxiliary Timer 1 PSL Ouput from Auxiliary Timer 16	Auxiliary Timer
314	TOC Start A	Trip on Close start on phase A: indicates a trip order on phase A has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
315	TOC Start B	Trip on Close start on phase B: indicates a trip order on phase B has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
316	TOC Start C	Trip on Close start on phase C: indicates a trip order on phase C has been issued by the SOTF level detectors (Pickup time-delay = 20 ms)	PSL (OUT) SOTF
313	TOR Enable	Trip On Reclose enable: indicates the TOR logic is activated in the relay Set to 1= 500 ms pulse initiated by: 'I A/R Reclaim' (internal) OR 'A/R reclaim' (External Input) OR Any pole open for more than 200 ms Reset 500 ms after Any pole dead stops	PSL (OUT) TOR
1032	TPAR Enable	Enable internal three pole autorecloser Set with Opto input (if linked by PSL) is energized (> 1s). At 1: 3P AR internal is enabled in the AR logic At 0: AR 3P internal is disabled (even if set in MiCOM S1 Agile). 1P cycle available if SPAR =1	PSL (IN) Autorecloser
368	Trace Trig OK	Triggering trace has operated correctly	PSL (OUT)
1024	Trip LED	LED trip	
370	Trip Thermal	Trip with Thermal Overload fucntion (timer issued)	PSL (OUT)
265	Tzp	Distance time-delay in zone p tZp elapsed (1 = end of timer)	PSL (OUT) Distance
1096	TZp Timer Block	Timer block TZp input	PSL

Ordinal	English Text	Description	Source
395	Tzq	Timer in zone Q elapsed (at 1 = end of timer)	PSL
1097	TZq Timer Block	Timer block TZq input	PSL
1084	User Trip A	Internal input for trip logic A Set to 1: Trip A Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1085	User Trip B	Internal input for trip logic B Set to 1: Trip B Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
1086	User Trip C	Internal input for trip logic C Set to 1: Trip C Internal input managed with the general trip logic(with A/R / Evolving fault…) Can be assigned by external condition	PSL (IN) Trip Logic
239	V< Dead Bus	Dead Bus: high when the Dead Bus condition is met (voltage below the V<Dead Bus threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
237	V< Dead Line	Dead Line: high when the Dead Line condition is met (voltage below the 'V< Dead Line' threshold value (setting) – The measured voltage is always calculated as a single phase voltage	PSL (OUT) Synchro Check
285	V< Start Any A	Any undervoltage start detected on phase A	PSL (OUT) Undervoltage
286	V< Start Any B	Any undervoltage start detected on phase B	PSL (OUT) Undervoltage
287	V< Start Any C	Any undervoltage start detected on phase C	PSL (OUT) Undervoltage
197	V<1 Alarm	1st stage undervoltage alarm picks up when V<1 starts	PSL (OUT) V<1
288	V<1 Start	Undervoltage 1st stage start (any phase)	PSL (OUT) Undervoltage
371	V<1 Start A	Undervoltage stage 1 pick up on phase A	PSL
372	V<1 Start B	Undervoltage stage 1 pick up on phase B	PSL
373	V<1 Start C	Undervoltage stage 1 pick up on phase C	PSL
1069	V<1 Timer Block	Block phase undervoltage stage 1 time delay Set to 1: 'V<1 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<1
290	V<1 Trip	Undervoltage 1st stage – 3-phase trip	PSL (OUT) Undervoltage
198	V<2 Alarm	2nd stage undervoltage alarm picks up when V<21 starts	PSL (OUT) V<2
289	V<2 Start	Undervoltage 2nd stage start (any phase)	PSL (OUT) Undervoltage
374	V<2 Start A	Undervoltage stage 2 pick up on phase A	PSL
375	V<2 Start B	Undervoltage stage 2 pick up on phase B	PSL
376	V<2 Start C	Undervoltage stage 2 pick up on phase C	PSL
1070	V<2 Timer Block	Block phase undervoltage stage 2 time delay Set to 1: 'V<2 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<2
291	V<2 Trip	Undervoltage stage 2nd stage – 3-phase trip	PSL (OUT) Undervoltage
396	V<3 Start	Undervoltage stage 3 start	PSL

Ordinal	English Text	Description	Source
398	V<3 Start A	Undervoltage phase A stage 3 start	PSL
399	V<3 Start B	Undervoltage phase B stage 3 start	PSL
400	V<3 Start C	Undervoltage phase C stage 3 start	PSL
1071	V<3 Timer Block	Block phase undervoltage stage 3 time delay Set to 1: 'V<3 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<3
404	V<3 Trip	Undervoltage stage 3 trip	PSL
397	V<4 Start	Undervoltage stage 4 start	PSL
401	V<4 Start A	Undervoltage phase A stage 4 start	PSL
402	V<4 Start B	Undervoltage phase B stage 4 start	PSL
403	V<4 Start C	Undervoltage phase C stage 4 start	PSL
1072	V<4 Timer Block	Block phase undervoltage stage 4 time delay Set to 1: 'V<4 Time Delay' will be blocked and V<1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V<4
405	V<4 Trip	Undervoltage stage 4 trip	PSL
240	V> Live Bus	Live Bus: high when the Live Bus condition is met (voltage above the V>Live Bus threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
238	V> Live Line	Live Line: high when the Live line condition is met (voltage above the 'V> Live Line' threshold value (setting) - always calculated as a single phase voltage reference.	PSL (OUT) Synchro Check
292	V> Start Any A	Any overvoltage start detected on phase A	PSl (OUT) Overvoltage
293	V> Start Any B	Any overvoltage start detected on phase B	PSl (OUT) Overvoltage
294	V> Start Any C	Any overvoltage start detected on phase C	PSl (OUT) Overvoltage
199	V>1 Alarm	1st stage overvoltage alarm picks up when V>1 starts	PSL (OUT) V>1
295	V>1 Start	Overvoltage function 1st stage start for any phase	PSl (OUT) Overvoltage
377	V>1 Start A	Overvoltage stage 1 pick up on phase A	PSL
378	V>1 Start B	Overvoltage stage 1 pick up on phase B	PSL
379	V>1 Start C	Overvoltage stage 1 pick up on phase C	PSL
1073	V>1 Timer Block	Block phase overvoltage stage 1 time delay Set to 1: 'V>1 Time Delay will be blocked and V>1 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>1
297	V>1 Trip	Overvoltage 1st stage 3-phase trip	PSl (OUT) Overvoltage
200	V>2 Alarm	2nd stage overvoltage alarm picks up when V>2 starts	PSL (OUT) V>2
296	V>2 Start	Overvoltage function 2nd stage start for any phase	PSl (OUT) Overvoltage
380	V>2 Start A	Overvoltage stage 2 pick up on phase A	PSL
381	V>2 Start B	Overvoltage stage 2 pick up on phase B	PSL
382	V>2 Start C	Overvoltage stage 2 pick up on phase C	PSL

Ordinal	English Text	Description	Source
1074	V>2 Timer Block	Block phase overvoltage stage 2 time delay Set to 1: 'V>2 Time Delay' will be blocked and V>2 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>2
298	V>2 Trip	Overvoltage 2nd stage 3-phase 2 trip	PSI (OUT) Overvoltage
406	V>3 Start	Overvoltage stage 3 start	PSL
408	V>3 Start A	Overvoltage phase A stage 3 start	PSL
409	V>3 Start B	Overvoltage phase B stage 3 start	PSL
410	V>3 Start C	Overvoltage phase C stage 3 start	PSL
1075	V>3 Timer Block	Block phase overvoltage stage 3 time delay Set to 1: 'V>3 Time Delay' will be blocked and V>3 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>3
414	V>3 Trip	Overvoltage stage 3 trip	PSL
407	V>4 Start	Overvoltage stage 4 start	PSL
411	V>4 Start A	Overvoltage phase A stage 4 start	PSL
412	V>4 Start B	Overvoltage phase B stage 4 start	PSL
413	V>4 Start C	Overvoltage phase C stage 4 start	PSL
1076	V>4 Timer Block	Block phase overvoltage stage 4 time delay Set to 1: 'V>4 Time Delay' will be blocked and V>4 will start but will not issue any trip command. Reset to 0: Opto input power off if signal assigned to an opto input OR DDB at 0 if signal assigned to a DDB cell	PSL (IN) V>4
415	V>4 Trip	Overvoltage stage 4 trip	PSL
213	V3< Alarm	Third undervoltage stage Alarm	PSL(IN)
215	V3> Alarm	Third overvoltage stage Alarm	PSL(IN)
214	V4< Alarm	Fourth undervoltage stage Alarm	PSL(IN)
216	V4> Alarm	Fourth overvoltage stage Alarm	PSL(IN)
205	Val/Fail Acq Al.	Relays with IEC 61850 9-2 Ethernet board only with software version up to D4.x Alarm NCIT (9-2 Ethernet) - Frame from Merge Units failed. Any Logical Node is synchronized with Internal (local) synchronization	PSL (OUT)
1224	Virtual Input 1	Goose input n° 1 - Allows binary signals that are mapped to virtual inputs to interface into PSL	SW
1225 to 1287	Virtual Input 2 to Virtual Input 64	Goose input n° 2 to Goose input n° 32	SW
512	Virtual output 1	Goose output n° 1 - Allows user to control a binary signal which can be mapped via SCADA protocol output to other devices	PSL
513 to 543	Virtual output 2 Virtual output 32	Goose output n° 2 to Goose output n° 32	PSL
389	VN>1 Start	Neutral overvoltage stage 1 pick up	PSL
1077	VN>1 Timer Block	Block earth overvoltage stage 1 time delay	PSL (IN) VN>1
391	VN>1 Trip	Neutral overvoltage stage 1 trip	PSL
390	VN>2 Start	Neutral overvoltage stage 2 pick up	PSL
1078	VN>2 Timer Block	Block earth overvoltage stage 2 time delay	PSL (IN) VN>2
392	VN>2 Trip	Neutral overvoltage stage 2 trip	PSL

Ordinal	English Text	Description	Source
177	VT Fail Alarm	Fuse failure indication (VT alarm). High when the opto input is energised (copy of MCB) OR an internal Fuse Failure is confirmed when the VTS timer elapses.	PSL (OUT) VT Supervision
337	VTS Fast	Instantaneous unconfirmed fuse failure internal detection. Set high for internal Fuse Failure detection made with internal logic.	PSL (OUT) VTS
266	WI Trip A	Phase A trip on weak infeed	PSL (OUT) Distance
267	WI Trip B	Phase B trip on weak infeed	PSL (OUT) Distance
268	WI Trip C	Phase C trip on weak infeed	PSL (OUT) Distance
255	Z1	Fault in zone 1 (convergence of loop in Z1) Set to 0: Reset of (R, X) (resistance, reactance) calculation made by All pole Dead detection (default PSL: LED 5, Relays 01 / 10)	PSL (OUT) Distance
349	Z1 Not Filtrated	Z1 decision not filtered by phase selection	PSL (OUT)
256	Z1X	Fault in zone 1 extended Z1x (convergence of loop in Z1x) and filtered by blocking/unblocking Power Swing/Reversal guard logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
1053	Z1X Extension	Zone 1 Extension Input Opto input energized if linked by PSL OR any internal DDB by dedicated PSL At 1: Signal will initiate Z1 extension logic if selected (setting). This DDB can be assigned to any external/Internal condition for starting Z1X logic	PSL (IN)
257	Z2	Fault in zone 2 (convergence of loop in Z2) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
258	Z3	Fault in zone 3 (convergence of loop in Z3) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
259	Z4	Fault in zone 4 (convergence of loop in Z4) and filtered by blocking/unblocking Power Swing/Reversal guard logic logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
260	Zp	Fault in zone P Zp (convergence of loop in Zp) logic (default PSL: LED 5, Relay 10)	PSL (OUT) Distance
394	Zq	Fault in zone Q	PSL
347	ZSP Start	Zero Sequence Power - Start: The ZSP START cell at 1 indicates the Zero Sequence Power function has started - in the same time, it indicates the timer-delays associated have started and are running (fixed one first and then IDMT timer)	PSL (OUT) ZSP
1087	ZSP Timer Block	Zero Sequence Power - Timer Block: If assigned to an opto input in a dedicated PSL, Zero Sequence Power function will start, but will not perform a trip command - the associated time-delay (adjusted with 'K Time Delay Factor ' setting, will be blocked	PSL (IN) ZSP
348	ZSP Trip	Zero Sequence Power - Trip: The ZSP TRIP cell at 1 indicates the Zero Sequence Power function has performed a trip command (after the start and when associated timers are issued)	PSL (OUT) ZSP
454	LBlinder DetectAN	Load Blinder Detection in Loop AN: Cell at 1 indicates the Impedance is located within the AN loop Load Blinder Region.	PSL (OUT) Distance

Ordinal	English Text	Description	Source
455	LBlinder DetectBN	Load Blinder Detection in Loop BN: Cell at 1 indicates the Impedance is located within the BN loop Load Blinder Region.	PSL (OUT) Distance
456	LBlinder DetectCN	Load Blinder Detection in Loop CN: Cell at 1 indicates the Impedance is located within the CN loop Load Blinder Region.	PSL (OUT) Distance
457	LBlinder DetectAB	Load Blinder Detection in Loop AB: Cell at 1 indicates the Impedance is located within the AB loop Load Blinder Region.	PSL (OUT) Distance
458	LBlinder DetectBC	Load Blinder Detection in Loop BC: Cell at 1 indicates the Impedance is located within the BC loop Load Blinder Region.	PSL (OUT) Distance
459	LBlinder DetectCA	Load Blinder Detection in Loop CA: Cell at 1 indicates the Impedance is located within the CA loop Load Blinder Region.	PSL (OUT) Distance
460	LB PowerSwing	Power Swing Detected within Load Blinder Region	PSL (OUT) Distance

1.2 Factory default programmable scheme logic

1.2.1 Logic input mapping

The default mappings for each of the opto-isolated inputs are as shown in the following table (PSL are equivalent for P442 and P444):

Opto Input N°	P442 Relay	P444 Relay
1	Channel Receive (Distance or DEF)	Channel Receive (Distance or DEF)
2	Channel out of Service (Distance or DEF)	Channel out of Service (Distance or DEF)
3	MCB/VTS Main (Z measurement-Dist)	MCB/VTS Main (Z measurement-Dist)
4	Block Autoreclose (BAR) (Lockout)	Block Autoreclose (BAR) (Lockout)
5	Circuit Breaker Healthy	Circuit Breaker Healthy
6	Circuit breaker Manual Close external order	Circuit breaker Manual Close external order
7	Reset Lockout	Reset Lockout
8	Disable Autoreclose (1-pole and 3-pole)	Disable Autoreclose (1-pole and 3-pole)
9	Not allocated	Not allocated
10	Not allocated	Not allocated
11	Not allocated	Not allocated
12	Not allocated	Not allocated
13	Not allocated	Not allocated
14	Not allocated	Not allocated
15	Not allocated	Not allocated
16	Not allocated	Not allocated
17		Not allocated
18		Not allocated
19		Not allocated
20		Not allocated

Opto Input N°	P442 Relay	P444 Relay
21		Not allocated
22		Not allocated
23		Not allocated
24		Not allocated

1.2.2 Relay output contact mapping

The default mappings and conditioning for each of the relay output contacts are shown in the following table (PSL are equivalent for P442/444):

Relay Contact N°	P442 Relay	P444 Relay
1	TripA+B+C & Z1 [straight]	TripA+B+C & Z1 [straight]
2	Any Trip Phase A [straight]	Any Trip Phase A [straight]
3	Any Trip Phase B [straight]	Any Trip Phase B [straight]
4	Any Trip Phase C [straight]	Any Trip Phase C [straight]
5	Signal send (Dist. or DEF) [straight]	Signal send (Dist. or DEF) [straight]
6	Any Protection Start [straight]	Any Protection Start [straight]
7	Any Trip [straight]	Any Trip [straight]
8	General Alarm [straight]	General Alarm [straight]
9	DEF A+B+C Trip + IN>2Trip + IN>3Trip [straight]	DEF A+B+C Trip + IN>2Trip + IN>3Trip [straight]
10	Dist. Trip & Any Zone & Dist Unb CR [straight]	Dist. Trip & Any Zone & Dist Unb CR [straight]
11	Autoreclose lockout [straight]	Autoreclose lockout [straight]
12	Autoreclose 1P + 3P cycle in progress [straight]	Autoreclose 1P + 3P cycle in progress [straight]
13	A/R Close [straight]	A/R Close [straight]
14	Power Swing Detected [straight]	Power Swing Detected [straight]
15	Not allocated	Not allocated
16	Not allocated	Not allocated
17	Not allocated	Not allocated
18	Not allocated	Not allocated
19	Not allocated	Not allocated
20	Not allocated	Not allocated
21	Not allocated	Not allocated
22	Not allocated	Not allocated
23		Not allocated
24		Not allocated
25		Not allocated
26		Not allocated
27		Not allocated
28		Not allocated
29		Not allocated
30		Not allocated
31		Not allocated

Relay Contact N°	P442 Relay	P444 Relay
32		Not allocated

Note: When 3-pole tripping mode is selected in the menu 'Distance Schemes / Trip mode', all the relay contacts connected to a trip (trip A, trip B, trip C, and Any Trip) close simultaneously.

The following relay logic conditions (time-delays, straight condition) can be used to set the PSL relay design:

- Pulse Timer
- Pick UP/Drop Off Timer
- Dwell Timer
- Pick Up Timer
- Drop Off Timer
- Latching
- Straight (transparent)

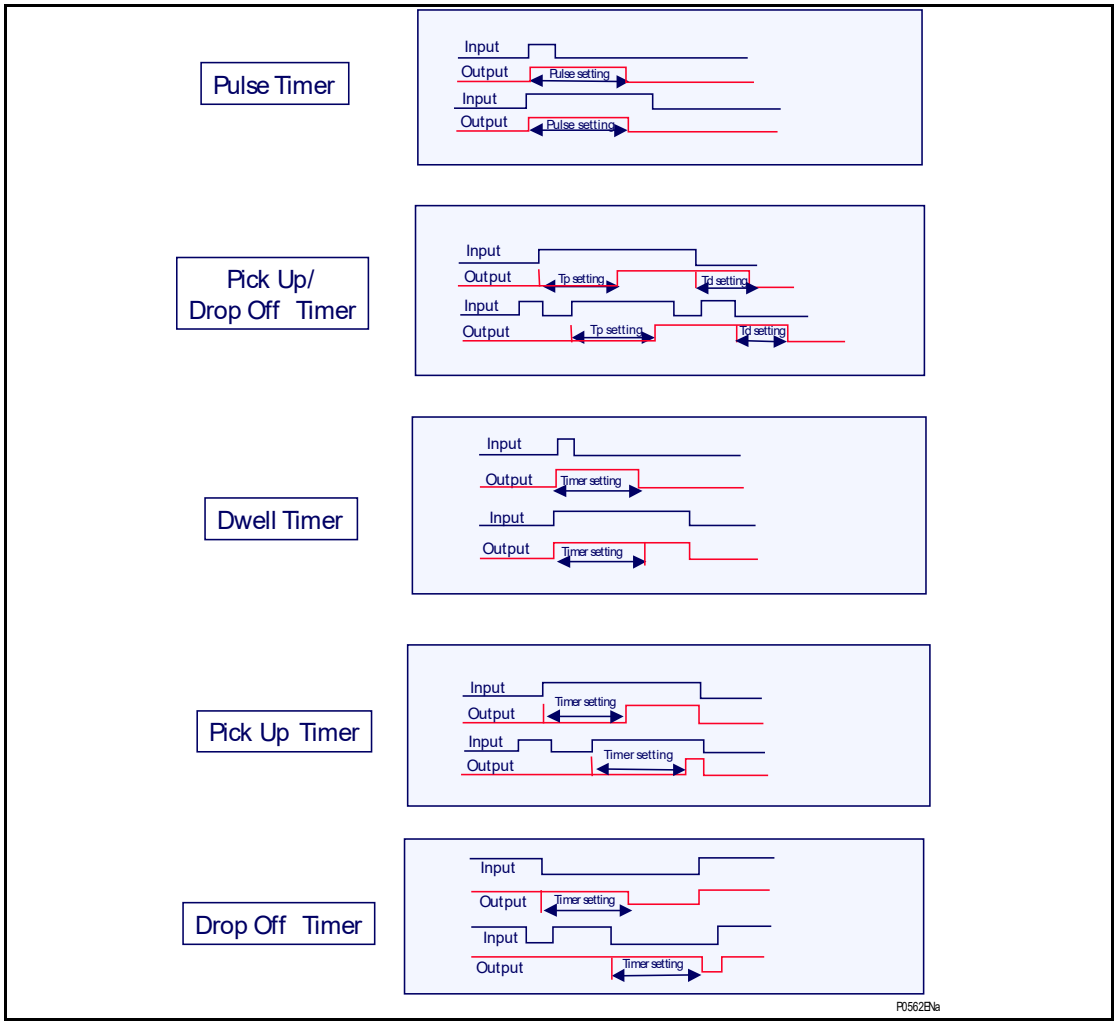


Figure 1: Time-delay definition in psl

1.2.3 Programmable LED output mapping

The default mappings for each of the programmable LEDs are as shown in the following table:

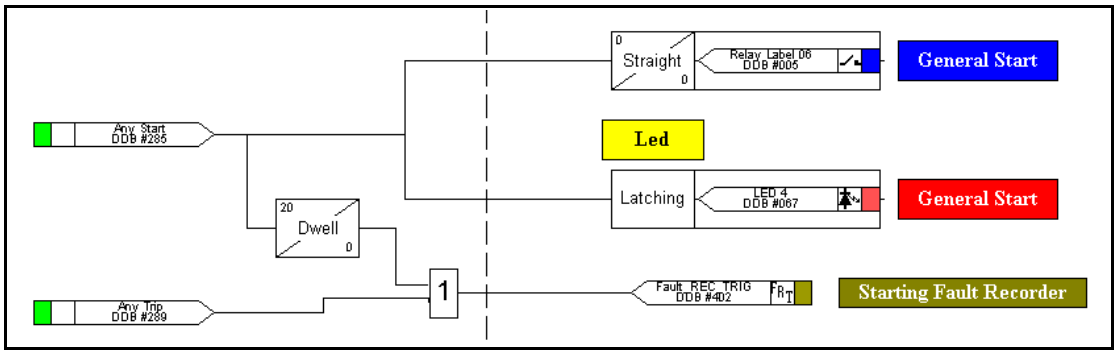
LED No.	P442 Relay	P444 Relay
1	Any Trip A	Any Trip A
2	Any Trip B	Any Trip B
3	Any Trip C	Any Trip C
4	Any Start	Any Start
5	Z1+Aided Trip	Z1+Aided Trip
6	Dist Fwd	Dist Fwd
7	Dist Rev	Dist Rev
8	A/R Enable	A/R Enable

Note: All the LEDs are latched in the default PSL.

1.2.4 Fault recorder trigger

The default PSL trigger which initiates a fault record is shown in the following table:

P442 Relay	P444 Relay
Any Start	Any Start
Any Trip	Any Trip



If the fault recorder trigger is not assigned in the PSL, no Fault recorder can be initiated and displayed in the list by the LCD front panel.

2 MICOM PX40 IEC 61850 IED CONFIGURATOR

IEC 61850 is a substation communications standard. It standardizes the way data is transferred to and from IEC 61850 compliant IEDs, making the communication independent of the manufacturer. This makes it easier to connect different manufacturers' products together and simplifies wiring and network changes.

The IEC 61850 Configurator tool is used to configure the IEC 61850 settings of MiCOM IEDs, not the protection settings. It also allows you to extract a configuration file so you can view, check and modify the IEC 61850 settings during precommissioning.

Further information is available in the Help system and in the Settings Application Software Guide P40-M&CR-UG-EN-n, where n is the latest version of the settings application software.

3 GOOSE EDITOR

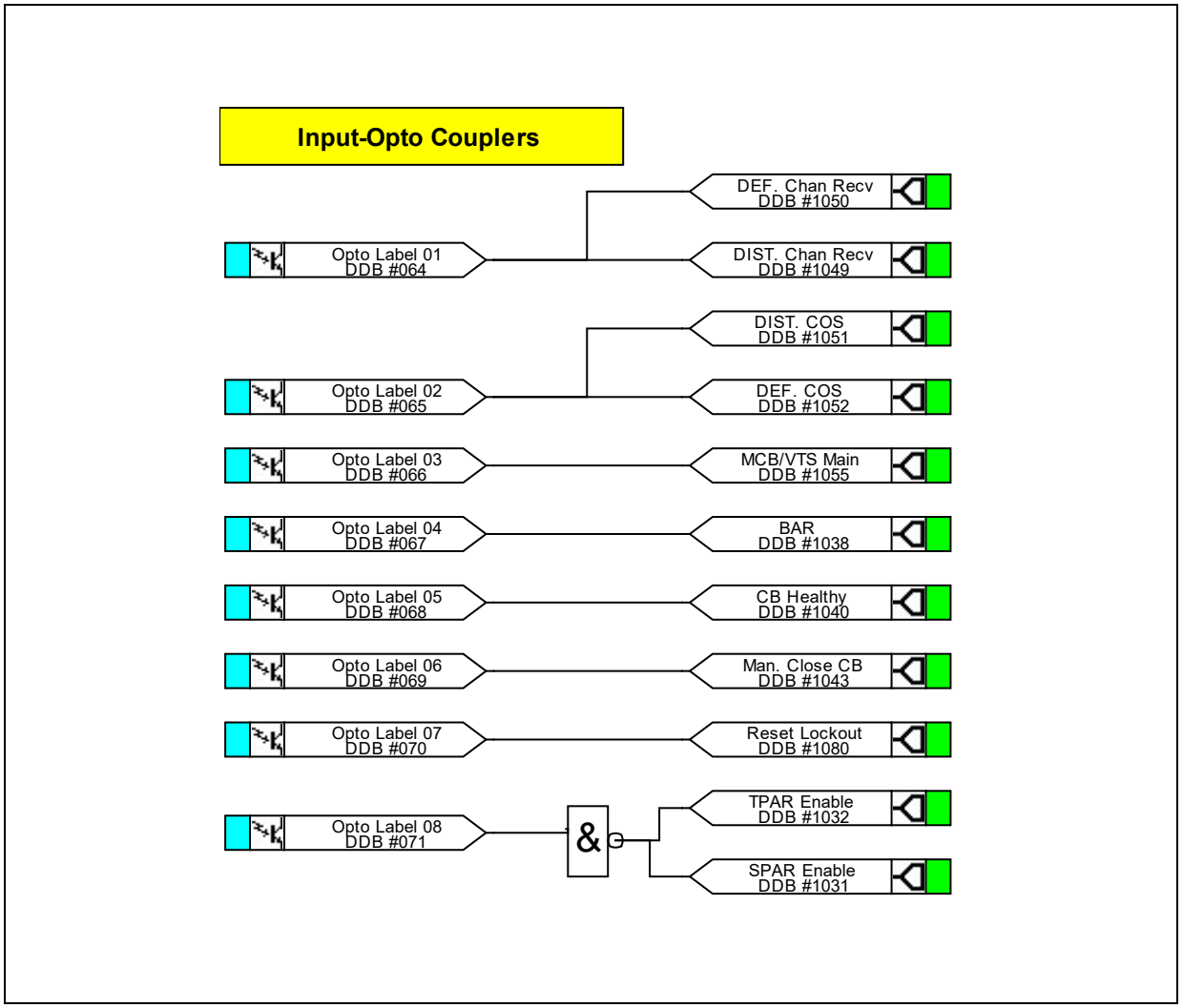
Using the GOOSE Editor you can edit the UCA2 GOOSE settings for a MiCOM Px4x series IED. You can also map GOOOSE inputs and outputs to the DDB signals of an IED.

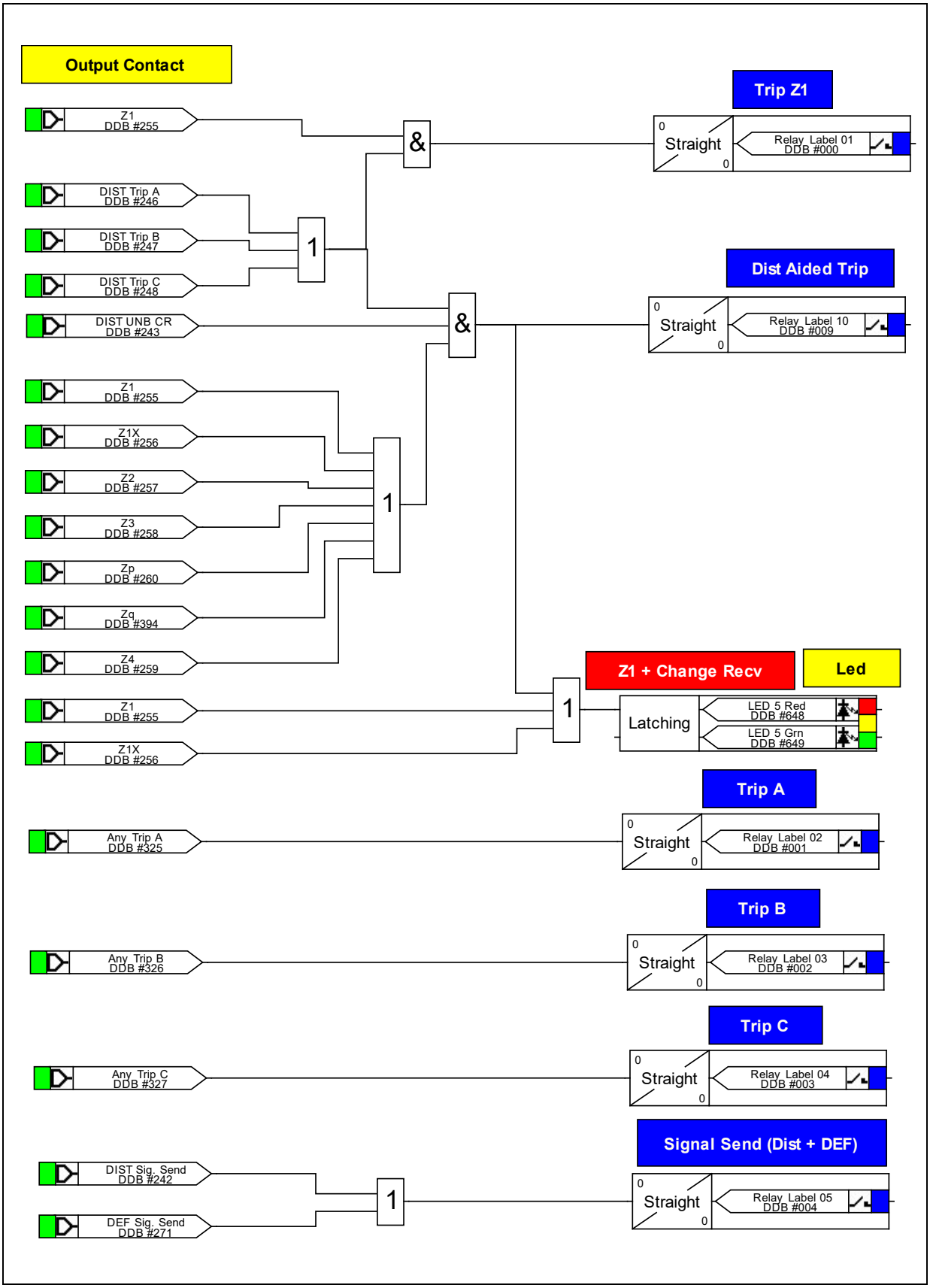
The GOOSE Editor can extract settings from and send settings to an IED using a Courier port on the IED. It can also save IED settings to a file on your PC or print them.

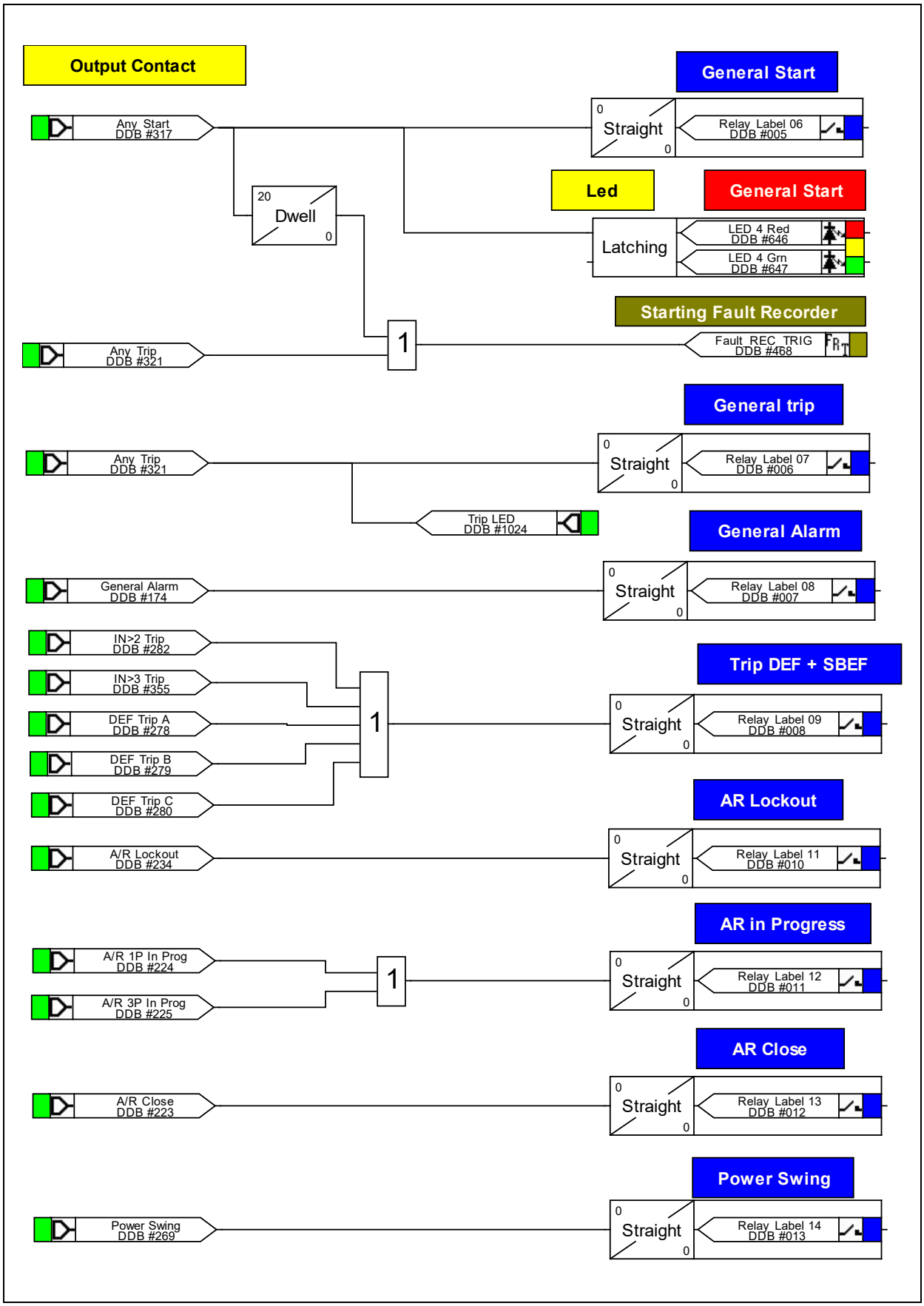
Further information is available in the Help system and in the Settings Application Software Guide P40-M&CR-UG-EN-n, where n is the latest version of the settings application software.

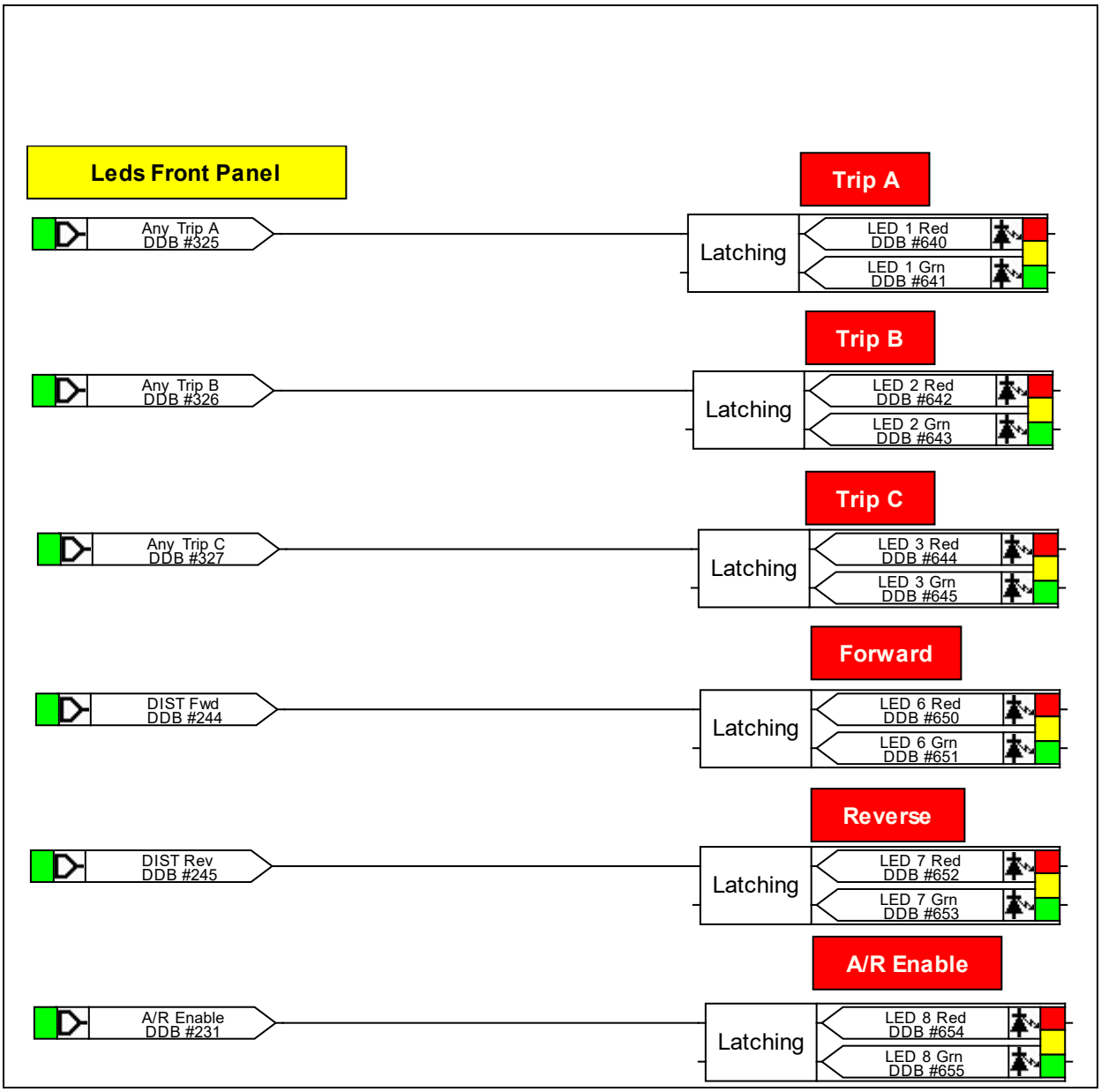
4 DEFAULT PROGRAMMABLE SCHEME LOGIC (PSL)

Example: MiCOM P444 with 46 outputs




Output Contact
Z1 DDB #255
DIST Trip A DDB #246
DIST Trip B DDB #247
DIST Trip C DDB #248
DIST UNB CR DDB #243
Z1 DDB #255
Z1X DDB #256
Z2 DDB #257
Z3 DDB #258
Zp DDB #260
Zq DDB #394
Z4 DDB #259
Z1 DDB #255
Z1X DDB #256
Any Trip A DDB #325
Any Trip B DDB #326
Any Trip C DDB #327
DIST Sig. Send DDB #242
DEF Sig. Send DDB #271
&
1
&
1
1
1
Trip Z1
0 Straight 0
Relay Label 01 DDB #000
Dist Aided Trip
0 Straight 0
Relay Label 10 DDB #009
Z1 + Change Recv
Led
Latching
LED 5 Red DDB #648
LED 5 Grn DDB #649
Trip A
0 Straight 0
Relay Label 02 DDB #001
Trip B
0 Straight 0
Relay Label 03 DDB #002
Trip C
0 Straight 0
Relay Label 04 DDB #003
Signal Send (Dist + DEF)
0 Straight 0
Relay Label 05 DDB #004


Output Contact
General Start
Any Start DDB #317
0 Straight 0
Relay Label 06 DDB #005
20 Dwell 0
Led
General Start
Latching
LED 4 Red DDB #646
LED 4 Grn DDB #647
Starting Fault Recorder
Any Trip DDB #321
1
Fault REC TRIG DDB #468
General trip
Any Trip DDB #321
0 Straight 0
Relay Label 07 DDB #006
Trip LED DDB #1024
General Alarm
General Alarm DDB #174
0 Straight 0
Relay Label 08 DDB #007
IN>2 Trip DDB #282
IN>3 Trip DDB #355
DEF Trip A DDB #278
DEF Trip B DDB #279
DEF Trip C DDB #280
1
Trip DEF + SBEF
0 Straight 0
Relay Label 09 DDB #008
AR Lockout
A/R Lockout DDB #234
0 Straight 0
Relay Label 11 DDB #010
AR in Progress
A/R 1P In Prog DDB #224
A/R 3P In Prog DDB #225
1
0 Straight 0
Relay Label 12 DDB #011
AR Close
A/R Close DDB #223
0 Straight 0
Relay Label 13 DDB #012
Power Swing
Power Swing DDB #269
0 Straight 0
Relay Label 14 DDB #013


Leds Front Panel
Trip A
Any Trip A
DDB #325
Latching
LED 1 Red
DDB #640
LED 1 Grn
DDB #641
Trip B
Any Trip B
DDB #326
Latching
LED 2 Red
DDB #642
LED 2 Grn
DDB #643
Trip C
Any Trip C
DDB #327
Latching
LED 3 Red
DDB #644
LED 3 Grn
DDB #645
Forward
DIST Fwd
DDB #244
Latching
LED 6 Red
DDB #650
LED 6 Grn
DDB #651
Reverse
DIST Rev
DDB #245
Latching
LED 7 Red
DDB #652
LED 7 Grn
DDB #653
A/R Enable
A/R Enable
DDB #231
Latching
LED 8 Red
DDB #654
LED 8 Grn
DDB #655

MEASUREMENTS AND RECORDING

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1. MEASUREMENTS AND RECORDING

1.1 Introductions

The MiCOM P442 and P444 are equipped with integral measurements, event, fault and disturbance recording facilities suitable for analysis of complex system disturbances.

The relay is flexible enough to allow for the programming of these facilities to specific user application requirements and are discussed below.

1.2 Event and fault recorder

1.2.1 Event Recorder (“View records” menu)

The relay records and time tags up to 250 events and stores them in non-volatile (battery backed up – installed behind the plastic cover in front panel of the relay)) memory. This enables the system operator to establish the sequence of events that occurred within the relay following a particular power system condition, switching sequence etc. When the available space is exhausted, the oldest event is automatically overwritten by the new one (First in first out).

The real time clock within the relay provides the time tag to each event, to a resolution of 1 ms.

The event records are available for viewing either via the frontplate LCD or remotely, via the communications ports or via MiCOM S1 Agile with a PC (connected to the relay (event extracted from relay & loaded in PC):

Local viewing on the LCD is achieved in the menu column entitled ‘VIEW RECORDS’. This column allows viewing of event, fault and maintenance records and is shown below:

VIEW RECORDS	
LCD Reference	**Description**
Select Event	Setting range from 0 to 249. This selects the required event record from the possible 250 that may be stored. A value of 0 corresponds to the latest event and so on.
Menu Cell Ref	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event
Time & Date	Time & Date Stamp for the event given by the internal Real Time Clock
Event Text	Up to 32 Character description of the Event (refer to following sections)
Event Value	Up to 32 Bit Binary Flag or integer representative of the Event (refer to following sections)
Select Fault	Setting range from 0 to 4. This selects the required fault record from the possible 5 that may be stored. A value of 0 corresponds to the latest fault and so on.
	The following cells show all the fault flags, protection starts, protection trips, fault location, measurements etc. associated with the fault, i.e. the complete fault record.
Distance	Distance protection trip: Trip Z1 aided, Trip Z1X aided, Trip Z2 aided, Trip Z3 aided, Trip Zp aided, Trip Zq aided, Trip Z5 aided,
Started Phase	A, B, C or N
Tripped phase	A, B, C or N
Overcurrent	Start I>1, Start I>2, Start I>3 or Start I>4
Overcurrent	Trip I>1, Trip I>2, Trip I>3 or Trip I>4
Neg Seq O/C	Negative sequence Overcurrent: Start I2>1, Start I2>2, Start I2>3 or Start I2>4
Neg Seq O/C	Negative sequence Overcurrent: Trip I2>1, Trip I2>2, Trip I2>3 or Trip I2>4
Broken conductor trip	

VIEW RECORDS	
LCD Reference	**Description**
Earth Fault	Start IN>1, Start IN>2, Start IN>3 or Start IN>4
Earth Fault	Trip IN>1, Trip IN>2, Trip IN>3 or Trip IN>4
Aided DEF	DEF> Start
Aided DEF	DEF> Trip
Undercurrent	Start I<1, Start I<2
Undercurrent	Trip I<1, Trip I<2
Undervoltage	Start V<1, Start V<2, Start V<3 or Start V<4
Undervoltage	Trip V<1, Trip V<2, Trip V<3 or Trip V<4
Overvoltage	Start V>1, Start V>2, Start V>3 or Start V>4
Overvoltage	Trip V>1, Trip V>2, Trip V>3 or Trip V>4
Overfrequency	Start F>1 or Start F>2
Overfrequency	Trip F>1 or Trip F>2
Underfrequency	Start F<1, Start F<2, Start F<3 or Start F<4
Underfrequency	Trip F<1, Trip F<2, Trip F<3 or Trip F<4
Res. Overvoltage	Start VN>1 or Start VN>2
Res. Overvoltage	Trip VN>1 or Trip VN>2
Breaker Fail	CB Fail 1 or CB Fail 2
Supervision	CTS, VTS or CVTS
LOL	Trip
SOTF/TOR	Trip
TOC	Start
TOC	Trip
Weak infeed	Trip
ZSP	Start
ZSP	Trip
User	Trip
Faulted Phase	Phase initiating fault recorder starts: Start A, Start B, Start C, Start N, Trip A, Trip B, Trip C, Trip N
Start Elements	General Start, Start I>1, Start I>2, Start I>3, Start I>4, Start I2>1, Start IN>1, Start IN>2, Start IN>3, Start IN>4, Start DEF, Start V<1, Start V<2, Start V>1, Start V>2, Start Broken Cond, Start LOL, Start Distance, Start TOC, Start Zero Seq. Pow., Start PAP, Thermal Alarm, Start I2>2, Start I2>3, Start I2>4, Start VN>1 or Start VN>2
Trip Elements1	Any Trip, Trip I>1, Trip I>2, Trip I>3, Trip I>4, Trip I2>1, Trip IN>1, Trip IN>2, Trip IN>3, Trip IN>4, Trip DEF, Trip V<1, Trip V<2, Trip V>1, Trip V>2, Trip Broken line, Trip Z1, Trip Z2, Trip Z3, Trip Zp, Trip Z4, Trip Z2 Aided, Trip LOL, Trip Soft Tor, Trip WI, Trip CB Fail1, Trip CB Fail2, Trip Zero Seq. Pow., Trip PAP, Trip Thermal or Trip User
Validities	“Measurements and Location are not valid” or “Measurements is valid” or “Location is valid”
Time & Date	Time & Date Stamp for the event given by the internal Real Time Clock.
Fault Alarms	VT Fail Alarm, CT Fail Alarm, CB Status Alarm, AR Lockout Shot >, V<1 Alarm, V<2 Alarm, V>1 Alarm, V>2 Alarm, COS Alarm, CVT Fail Alarm, V<3 Alarm, V<4 Alarm, V>3 Alarm or V>4 Alarm
System Frequency	50.00 Hz, 60.00 Hz
Fault duration	Duration of the fault
Relay Trip Time	Time and date of fault relay tripping

VIEW RECORDS	
LCD Reference	**Description**
Fault Location	When calculated the fault location can be found (distance in km or miles, impedance or percentage of line length, set in 'MEASUREMENT SETUP' column). See section 1.4.
IA	Magnitude of phase A current
IB	Magnitude of phase B current
IC	Magnitude of phase C current
VAN	Magnitude of phase A voltage
VBN	Magnitude of phase B voltage
VCN	Magnitude of phase C voltage
Fault Resistance	Fault resistance
Fault in Zone	None, Zone 1, Zone 2, Zone P, Zone Q, Zone 3 or Zone 4
Trip Elements 2	Trip I2>2, Trip I2>3, Trip I2>4, Trip VN>1, Trip VN>2, Trip Zq, Trip V<3, Trip V<4, Trip V>3, Trip V>4, Trip I<1, Trip I<2, Trip F<1, Trip F<2, Trip F<3, Trip F<4, Trip F>1, Trip F>2
Start Elements 2	Start V<3, Start V<4, Start V>3, Start V>4, Start I<1, Start I<2, Start F<1, Start F<2, Start F<3 ,Start F<4, Start F>1 or Start F>2
Select Report	Setting range from 0 to 4. This selects the required maintenance report from the possible 5 that may be stored. A value of 0 corresponds to the latest report and so on.
Report Text	Up to 32 Character description of the occurrence (refer to following sections)
Report Type	These cells are numbers representative of the occurrence. They form a specific error code which should be quoted in any related correspondence to AREVA T&D P&C Ltd.
Report Data	
Reset Indication	Either Yes or No. This serves to reset the trip LED indications provided that the relevant protection element has reset.

For extraction from a remote source via communications, refer to Chapter P44x/EN CM, (Commissioning) where the procedure is fully explained.

Types of Event

An event may be a change of state of a control input or output relay, an alarm condition, setting change etc. The following sections show the various items that constitute an event.

1.2.2 Change of state of opto-isolated inputs.

If one or more of the opto (logic) inputs has changed state since the last time that the protection algorithm ran, the new status is logged as an event. When this event is selected to be viewed on the LCD, three applicable cells will become visible as shown below;

Opto input Events
"LOGIC INPUTS"
"Event Value 0101010101010101"

The Event Value is an 8 or 16 bit word showing the status of the opto inputs, where the least significant bit (extreme right) corresponds to opto input 1 etc. The same information is present if the event is extracted and viewed via PC.

1.2.3 Change of state of one or more output relay contacts.

If one or more of the output relay contacts has changed state since the last time that the protection algorithm ran, then the new status is logged as an event. When this event is selected to be viewed on the LCD, three applicable cells will become visible as shown below;

Contact Events
"OUTPUT CONTACTS"
"Event Value 01010101010101010101"

The Event Value is a 7, 14 or 21 bit word showing the status of the output contacts, where the least significant bit (extreme right) corresponds to output contact 1 etc. The same information is present if the event is extracted and viewed via PC.

1.2.4 Relay Alarm conditions.

Any alarm conditions generated by the relays will also be logged as individual events. The following table shows examples of some of the alarm conditions and how they appear in the event list:

Alarm Condition	Event Text	Event Value
Battery Fail	Battery Fail ON/OFF	Bit position 0 in 32 bit field
Field Voltage Fail	Field Volt Fail ON/OFF	Bit position 1 in 32 bit field

The previous table shows the abbreviated description that is given to the various alarm conditions and also a corresponding value between 0 and 31. This value is appended to each alarm event in a similar way as for the input and output events previously described. It is used by the event extraction software, such as MiCOM S1 Agile, to identify the alarm and is therefore invisible if the event is viewed on the LCD. Either ON or OFF is shown after the description to signify whether the particular condition has become operated or has reset.

Alarm	Event Text	Explanation
Bit 0	Battery Fail	Battery Fail
Bit 1	Field Volt Fail	Field Voltage Fail
Bit 2	Prot'n Disabled	Protection Disabled
Bit 3	F out of Range	Frequency out of range
Bit 4	VT Fail Alarm	VTS Alarm
Bit 5	CT Fail Alarm	CTS Alarm
Bit 6	CB Fail Alarm	CB Trip Fail Protection
Bit 7	I^ Maint Alarm	Broken current Maintenance Alarm
Bit 8	I^ Lockout Alarm	Broken current Lockout Alarm
Bit 9	CB Ops Maint	No of CB Ops Maintenance Alarm
Bit 10	CB Ops Lockout	No of CB Ops Lockout Alarm
Bit 11	CB Op Time Maint	CB Op Time Maintenance Alarm
Bit 12	CB Op Time Lock	CB Op Time Lockout Alarm
Bit 13	F.F. Pre Lockout	Pre-alarm for lockout
Bit 14	F.F. Lock	Excessive Fault Frequency Lockout Alarm
Bit 15	CB Status Alarm	CB Status Alarm
Bit 16	Man CB Trip Fail	CB Fail Trip Control
Bit 17	Man CB Cls Fail	CB Fail Close Control
Bit 18	Man CB Unhealthy	No Healthy Control Close
Bit 19	Control No C/S	No C/S control close
Bit 20	A/R BAR Shot>	A/R Lockout max shots

Alarm	Event Text	Explanation
Bit 21	SG-opto Invalid	Setting group via optos invalid
Bit 22	A/R No Checksync	CB Fail to A/R
Bit 23	V<1 Alarm	
Bit 24	V<2 Alarm	
Bit 25	V>1 Alarm	
Bit 26	V>2 Alarm	
Bit 27	COS Alarm	
Bit 28	User Alarm 1	
Bit 29	User Alarm 2	
Bit 30	User Alarm 3	
Bit 31	User Alarm 4	

1.2.5 Protection Element Starts and Trips

Any operation of protection elements, (either a start or a trip condition), will be logged as an event record, consisting of a text string indicating the operated element and an event value. Again, this value is intended for use by the event extraction software, such as MiCOM S1 Agile, rather than for the user, and is therefore invisible when the event is viewed on the LCD.

1.2.6 General Events

A number of events come under the heading of 'General Events' - an example is shown below:

Nature of Event	Displayed Text in Event Record	Displayed Value
Level 1 Password Modified Either from User Interface, Front or Rear Port	PW1 Edited UI, F or R	0

A complete list of the 'General Events' is given in chapter P44x/EN PL.

1.2.7 Fault Records

Each time a fault record is generated, an event is also created. The event simply states that a fault record was generated, with a corresponding time stamp.

Note that viewing of the actual fault record is carried out in the '*Select Fault*' cell further down the '*VIEW RECORDS*' column, which is selectable from up to 5 records. These records consist of fault flags, fault location, fault measurements etc. Also note that the time stamp given in the fault record itself will be more accurate than the corresponding stamp given in the event record as the event is logged some time after the actual fault record is generated.

1.2.8 Maintenance Reports

Internal failures detected by the self monitoring circuitry, such as watchdog failure, field voltage failure etc. are logged into a maintenance report. The Maintenance Report holds up to 5 such 'events' and is accessed from the '*Select Report*' cell at the bottom of the '*VIEW RECORDS*' column.

Each entry consists of a self explanatory text string and a '*Type'* and '*Data'* cell, which are explained in the menu extract at the beginning of this section and in further detail in the following table (the lis is not exhaustive):

Text	Explanation
Bus Failure	Bus Check Failure
SRAM Failure	SRAM Failure
BB RAM Failure	BB RAM Failure

Text	Explanation
LCD Failure	LCD Failure
Watchdog 1 Fail	Watchdog 1 Failure (Fast)
Watchdog 2 Fail	Watchdog 2 Failure (Slow)
Field Volt Fail	Field Voltage Failure
FlashEEPROM Fail	Flash EPROM Failure
EEPROM Fail	EEPROM Failure
Cal EEPROM Fail	Cal EEPROM Failure
Invalid H/W	Incorrect Hardware Configuration
Power Up Boot	Power Up Boot
Soft Reboot	Soft Reboot

Each time a Maintenance Report is generated, an event is also created. The event simply states that a report was generated, with a corresponding time stamp.

1.2.9 Setting Changes

Changes to any setting within the relay are logged as an event. Two examples are shown in the following table:

Type of Setting Change	Displayed Text in Event Record
Control/Support Setting	C & S Changed
Group 1 / 2 / 3 or 4 Change	Group 1, 2, 3 or 4 updated
Disturbance setting	Disturbance recorder
Active group change	Active group changed

Note: Control/Support settings are communications, measurement, CT/VT ratio settings etc, which are not duplicated within the four setting groups. When any of these settings are changed, the event record is created simultaneously. However, changes to protection or disturbance recorder settings will only generate an event once the settings have been confirmed at the 'setting trap'.

1.2.10 Resetting of Event / Fault Records

If it is required to delete either the event, fault or maintenance reports, this may be done from within the '*RECORD CONTROL'* column.

1.2.11 Viewing Event Records via MiCOM S1 Agile Support Software

When the event records are extracted and viewed on a PC they look slightly different than when viewed on the LCD. The following shows an example of how various events appear when displayed using MiCOM S1 Agile:

Monday 03 November 2010 15:32:49 GMT I>1 Start ON 2147483881

MiCOM

Model Number: P441

Address: 001 Column: 00 Row: 23

Event Type: Protection operation

Monday 03 November 2010 15:32:52 GMT Fault Recorded 0

MiCOM

Model Number: P442

Address: 001 Column: 01 Row: 00

Event Type: Fault record

Monday 03 November 2010 15:33:11 GMT Logic Inputs 00000000

MiCOM

Model Number: P442

Address: 001 Column: 00 Row: 20

Event Type: Logic input changed state

Monday 03 November 2010 15:34:54 GMT Output Contacts 0010000

MiCOM

Model Number: P442

Address: 001 Column: 00 Row: 21

Event Type: relay output changed state

As can be seen, the first line gives the description and time stamp for the event, whilst the additional information that is displayed below may be collapsed via the +/- symbol.

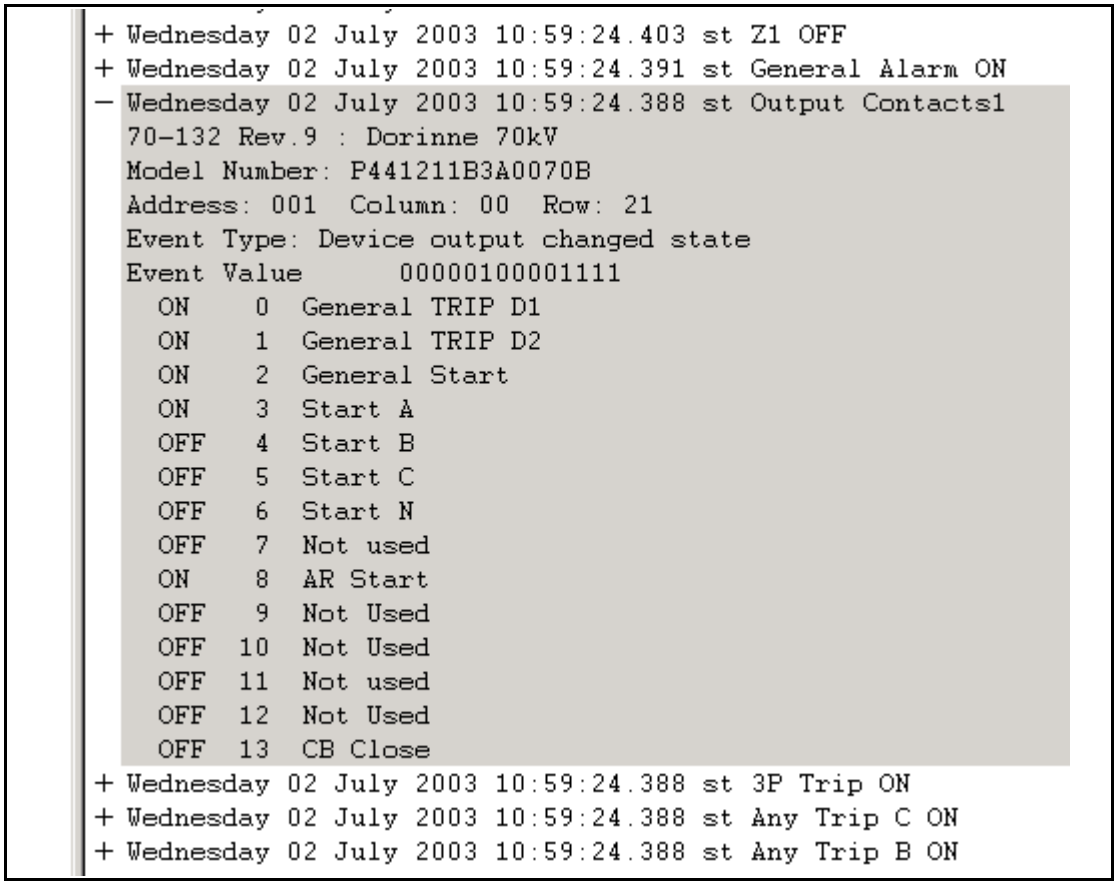


Figure 1

1.2.12 Event Filtering

It is possible to disable the reporting of events from all interfaces that supports setting changes. The settings that control the various types of events are in the “Record Control” column (see section P44x/EN ST)

1.3 Disturbance recorder

The integral disturbance recorder (“Disturb recorder” menu, P44x/EN ST) has an area of memory specifically set aside for record storage. The number of records that may be stored is dependent upon the selected recording duration but the relays typically have the capability of storing a minimum of 20 records, each of 10.5 second duration.

Note:	*1.*	*Compressed Disturbance Recorder used for Kbus/Modbus/DNP3 reach that typical size value (10.5 sec duration)*
	2.	*Uncompressed Disturbance Recorder used for IEC 60870-5/103 could be limited to 2 or 3 secondes.*

Disturbance records continue to be recorded until the available memory is exhausted, at which time the oldest record(s) are overwritten to make space for the newest one.

The recorder stores actual samples which are taken at a rate of 24 samples per cycle.

It is not possible to view the disturbance records locally via the LCD; they must be extracted using suitable software such as MiCOM S1 Agile. This process is fully explained in the SCADA Communications section (P44x/EN SC).

1.4 Fault locator

The relay has an integral fault locator that uses information from the current and voltage inputs to provide a distance to fault measurement. The sampled data from the analogue input circuits is written to a cyclic buffer until a fault condition is detected. The data in the input buffer is then held to allow the fault calculation to be made. When the fault calculation is complete the fault location information is available in the relay fault record.

When calculated the fault location can be found in the fault record under the VIEW RECORDS column in the **Fault Location** cells. Distance to fault is available in km, miles, impedance or percentage of line length. The fault locator can store data for up to five faults. This ensures that fault location can be calculated for all shots on a typical multiple reclose sequence, whilst also retaining data for at least the previous fault.

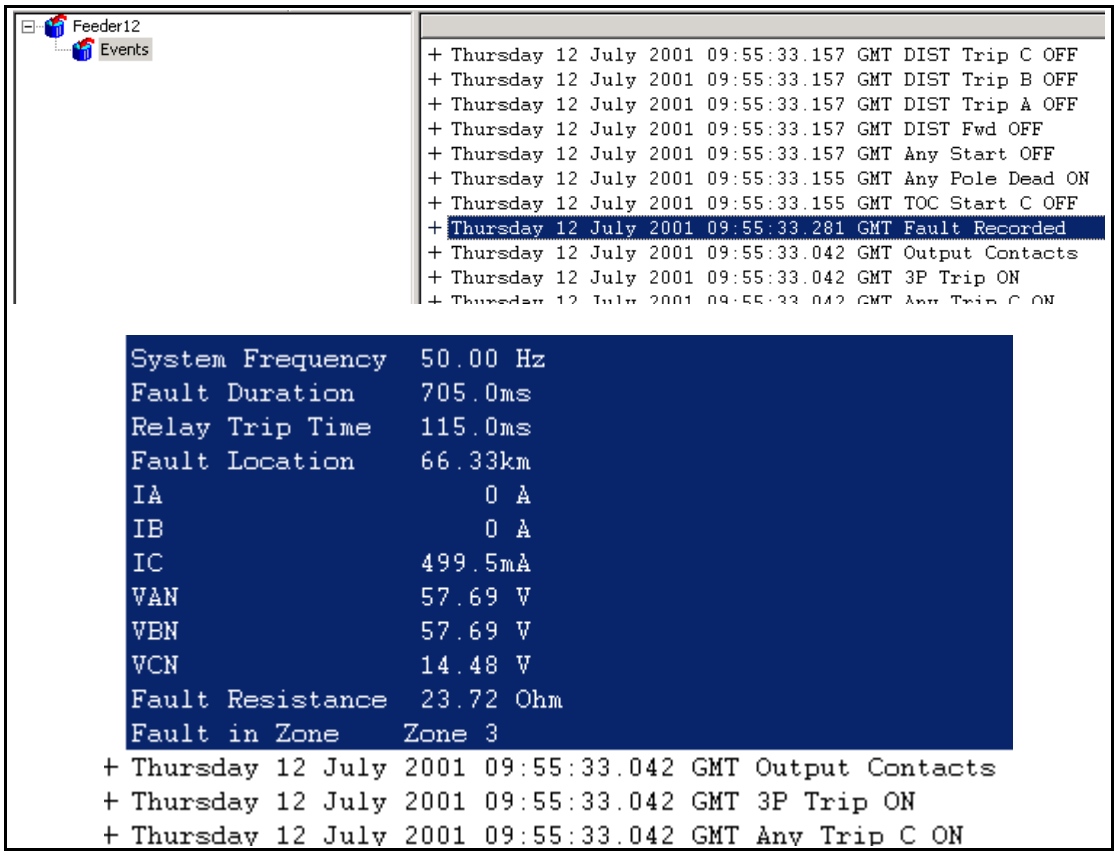


Figure 2 - Fault Location information included in an event:

2 MEASUREMENTS

The relay produces a variety of both directly measured and calculated system quantities. These measurement values are updated on a per second basis and can be viewed in the “Measurements” columns (up to three) of the relay or via MiCOM S1 Agile Measurement viewer.

The MiCOM P442 and P444 relays are able to measure and display the following quantities as summarized.

2.1 Measured currents

The MiCOM P442 and P444 relays produce current values. They are produced directly from the DFT (Discrete Fourier Transform) used by the relay protection functions and present both magnitude and phase angle measurement.

2.2 Sequence voltages and currents

Sequence quantities are produced by P442 and P444 relays from the measured Fourier values; these are displayed as magnitude and phase angle values.

2.3 Settings

The settings under the heading “Measurement setup” can be used to configure the relay measurement function: see “Settings” section P44x/EN ST for more information.

2.4 Measurement display quantities

There are three “Measurement” columns available in the relay for viewing of measurement quantities. These can also be viewed with MiCOM S1 Agile (see MiCOM Px40 – Monitoring section of the MiCOM S1 Agile User Manual) and are shown below:

P442	P444	MEASUREMENTS 1
*	*	IA Magnitude
*	*	IA phase Angle
*	*	IB Magnitude
*	*	IB Phase Angle
*	*	IV Magnitude
*	*	IC Phase Angle
*	*	IN Magnitude
*	*	IN Angle
*	*	I1 Magnitude
*	*	I2 Magnitude
*	*	I0 magnitude
*	*	VAB Magnitude
*	*	VAB Phase Angle
*	*	VBC Magnitude
*	*	VBC Phase Angle
*	*	VCA Magnitude
*	*	VCA Phase Angle
*	*	VAN Magnitude
*	*	VAN Phase Angle
*	*	VBN Magnitude
*	*	VBN Phase Angle
*	*	VCN Magnitude

P442	P444	MEASUREMENTS 1
*	*	VCN Phase Angle
*	*	VN Magnitude
*	*	VN Angle
*	*	V1 Magnitude
*	*	V2 Magnitude
*	*	V0 Magnitude
*	*	Frequency
*	*	C/S Voltage Mag
*	*	C/S Voltage Ang
*	*	IM Magnitude
*	*	IM Angle
*	*	Slip frequency
*	*	C/S Diff V

P442	P444	MEASUREMENTS 2
*	*	A Phase Watts
*	*	B Phase Watts
*	*	C Phase Watts
*	*	A Phase Vars
*	*	B Phase Vars
*	*	C Phase Vars
*	*	A Phase VA
*	*	B Phase VA
*	*	C Phase VA
*	*	3 Phase Watts
*	*	3 Phase Vars
*	*	3 Phase VA
*	*	Zero Seq power
*	*	3Ph Power Factor
*	*	Aph Power Factor
*	*	Bph Power Factor
*	*	Cph Power Factor
*	*	3 Ph W Fix Dem
*	*	3 Ph Vars Fix Dem
*	*	3Ph W Peak Dem
*	*	3Ph Vars Peak Dem
*	*	Reset Demand
*	*	3Ph Whours Fwd
*	*	3Ph Whours Rev
*	*	3Ph VArhours Fwd
*	*	3Ph VArhours Rev

P442	P444	MEASUREMENTS 3
*	*	Thermal Status
*	*	Reset Thermal

FIRMWARE DESIGN

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1 RELAY SYSTEM OVERVIEW

1.1 Hardware overview

The relay hardware is based on a modular design whereby the relay is made up of several modules which are drawn from a standard range. Some modules are essential while others are optional depending on the user's requirements.

The different modules that can be present in the relay are as follows:

1.1.1 Power supply module

The power supply module provides a power supply to all of the other modules in the relay, at three different voltage levels. The power supply board also provides the RS485 electrical connection for the rear communication port. On a second board the power supply module contains relays which provide the output contacts.

1.1.2 Main processor board

The processor board performs most of the calculations for the relay (fixed and programmable scheme logic, protection functions other than distance protection) and controls the operation of all other modules within the relay. The processor board also contains and controls the user interfaces (LCD, LEDs, keypad and communication interfaces).

1.1.3 Co-processor board

The co-processor board manages the acquisition of analogue quantities, filters them and calculates the thresholds used by the protection functions. It also processes the distance algorithms.

1.1.4 Input module

The input module converts the information contained in the analogue and digital input signals into a format suitable for the co-processor board. The standard input module consists of two boards: a transformer board to provide electrical isolation and a main input board which provides analogue to digital conversion and the isolated digital inputs.

1.1.5 Input and output boards

	P442	P444
Opto-inputs	16 x UNI(1)	24 x UNI(1)
Relay outputs	9 N/O 12 C/O	24 N/O 8 C/O (2)

(1) Universal voltage range opto inputs

N/O – normally open
C/O – change over

(1) Up to 46 outputs (in option)

1.1.6 IRIG-B modulated or unmodulated board

The modulated or unmodulated IRIG-B board, which is optional, can be used where an IRIG-B signal is available to provide an accurate time reference for the relay. There is also an option on this board to specify:

- A fibre optic rear communication port, for use with IEC 60870 communication only.
- A second rear port designed typically for dial-up modem access by protection engineers/operators (see section 1.1.7).

All modules are connected by a parallel data and address bus which allows the processor board to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sample data from the input module to the processor. Figure 1 shows the modules of the relay and the flow of information between them.

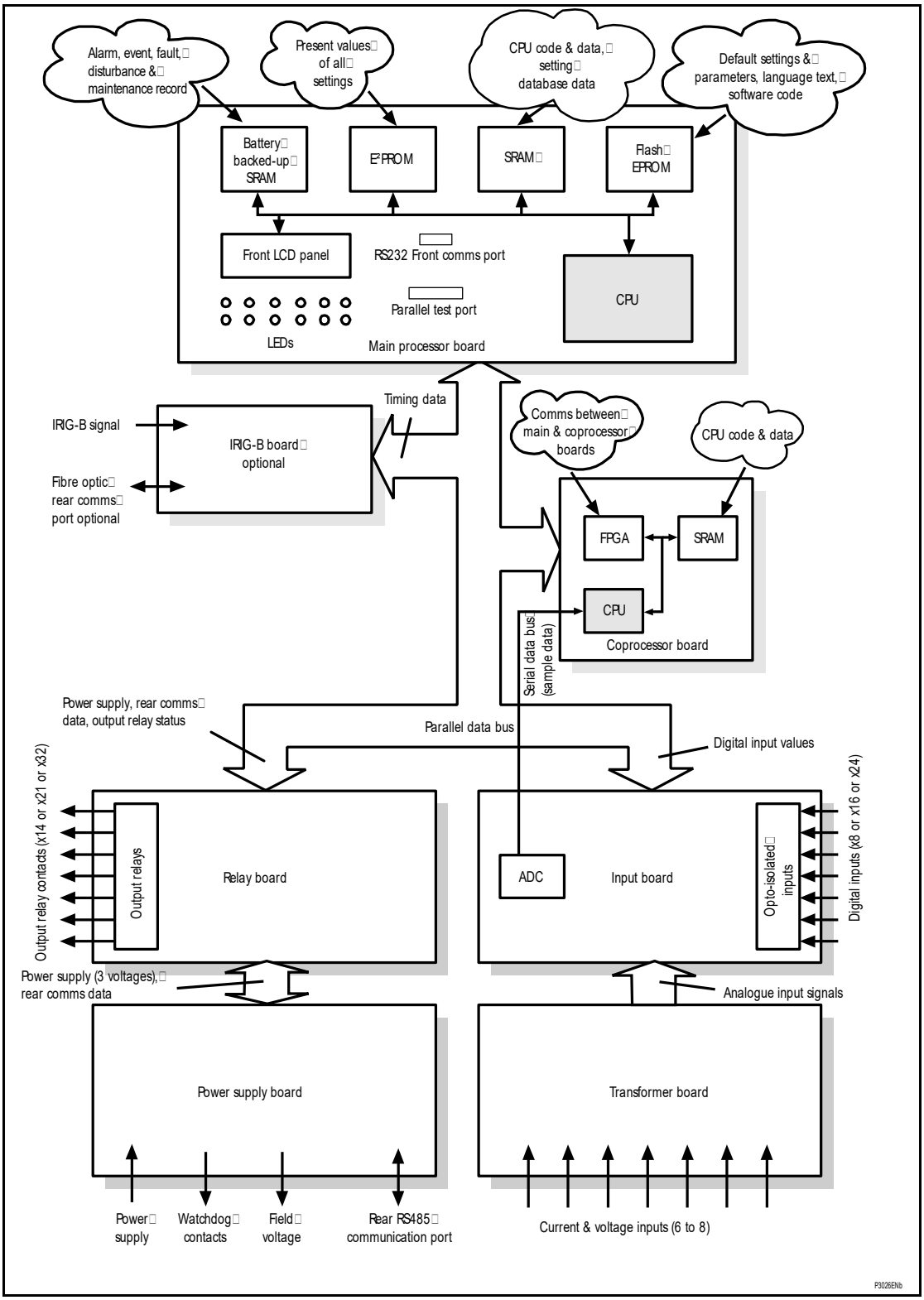


Figure 1 - Relay modules and information flow

1.1.7 Second rear comms and InterMiCOM board (optional)

The optional second rear port is designed typically for dial-up modem access by protection engineers/operators, when the main port is reserved for SCADA traffic. It is denoted “SK4”. Communication is via one of three physical links: K-Bus, EIA(RS)485 or EIA(RS)232. The port supports full local or remote protection and control access by MiCOM S1 Agile software. The second rear port is also available with an on board IRIG-B input.

The optional board also houses port “SK5”, the InterMiCOM teleprotection port. InterMiCOM permits end-to-end signalling with a remote P440 relay, for example in a distance protection channel aided scheme. Port SK5 has an EIA(RS)232 connection, allowing connection to a MODEM, or compatible multiplexers.

1.1.8 Ethernet or Redundant Ethernet board (optional)

Ethernet or dual Ethernet boards are mandatory boards for IEC 61850 enabled relays. The boards provide network connectivity through either copper or fibre media at rates of 10 Mb/s or 100 Mb/s. There is also an option on the Ethernet board to specify IRIG-B board port (modulated or un-modulated). These boards and the second rear comms board are mutually exclusive as they both utilise slot A within the relay case.

The Redundant Ethernet board (see Px4x/EN REB user guide) option provides a redundant connection, useful to safe exchanges between two relays or for specific network applications. The different options use Self Healing Protocol (SHP), Rapid Spanning Tree Protocol (RSTP) or Dual Homing Protocol (DHP).

All modules are connected by a parallel data and address bus that allows the processor board to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sample data from the input module to the processor.

Note:	*It is possible to connect to the Ethernet network any of the P44x without the embedded Ethernet board using the RS485 to Ethernet converter MiCOM I4X (Courier protocol)*

1.1.9 9-2 Ethernet board (optional)

The 9-2 Ethernet board assures appropriate communication to IEC 61850-9-2LE (Lite Edition) compliant Merging Units (MU).

The 9-2 Ethernet board is the communication interface between MiCOM protection and the network. It replaces the conventional analogue inputs (analogue module) wherever it/they stand (see Px4x/EN 9-2 user guide).

1.2 Software overview

The software for the relay can be conceptually split into four elements: the real-time operating system, the system services software, the platform software and the protection and control software. These four elements are not distinguishable to the user, and are all processed by the same processor board. The distinction between the four parts of the software is made purely for the purpose of explanation here:

1.2.1 Real-time operating system

The real time operating system is used to provide a framework for the different parts of the relay’s software to operate within. To this end the software is split into tasks. The real-time operating system is responsible for scheduling the processing of these tasks such that they are carried out in the time available and in the desired order of priority.

The operating system is also responsible for the exchange of information between tasks, in the form of messages.

1.2.2 System services software

The system services software provides the low-level control of the relay hardware. For example, the system services software controls the boot of the relay’s software from the non-

volatile flash EPROM memory at power-on, and provides driver software for the user interface via the LCD and keypad, and via the serial communication ports. The system services software provides an interface layer between the control of the relay's hardware and the rest of the relay software.

1.2.3 Platform software

The platform software deals with the management of the relay settings, the user interfaces and logging of event, alarm, fault and maintenance records. All of the relay settings are stored in a database within the relay which provides direct compatibility with Courier communications. For all other interfaces (i.e. the front panel keypad and LCD interface, Modbus and IEC 60870-5-103) the platform software converts the information from the database into the format required. The platform software notifies the protection & control software of all setting changes and logs data as specified by the protection & control software.

1.2.4 Protection & control software

The protection and control software performs the calculations for all of the protection algorithms of the relay. This includes digital signal processing such as Fourier filtering and ancillary tasks such as the measurements. The protection & control software interfaces with the platform software for settings changes and logging of records, and with the system services software for acquisition of sample data and access to output relays and digital opto-isolated inputs.

1.2.5 Disturbance Recorder

The disturbance recorder software is passed the sampled analogue values and logic signals from the protection and control software. This software compresses the data to allow a greater number of records to be stored. The platform software interfaces to the disturbance recorder to allow extraction of the stored records.

2 HARDWARE MODULES

The relay is based on a modular hardware design where each module performs a separate function within the relay operation. This section describes the functional operation of the various hardware modules.

2.1 Processor board

The relay is based around a TMS320VC33-150 MHz (peak speed) floating point, 32-bit digital signal processor (DSP) operating at a clock frequency of 75 MHz. This processor performs all of the calculations for the relay, including the protection functions, control of the data communication and user interfaces including the operation of the LCD, keypad and LEDs.

The processor board is located directly behind the relay's front panel which allows the LCD and LEDs to be mounted on the processor board along with the front panel communication ports. These comprise the 9-pin D-connector for RS232 serial communications (e.g. using MiCOM S1 Agile and Courier communications) and the 25-pin D-connector relay test port for parallel communication. All serial communication is handled using a two-channel 85C30 serial communications controller (SCC).

The memory provided on the main processor board is split into two categories, volatile and non-volatile: the volatile memory is fast access (zero wait state) SRAM which is used for the storage and execution of the processor software, and data storage as required during the processor's calculations. The non-volatile memory is sub-divided into 3 groups: 2MB of flash memory for non-volatile storage of software code and text together with default settings, 256kB of battery backed-up SRAM for the storage of disturbance, event, fault and maintenance record data and 32kB of E2PROM memory for the storage of configuration data, including the present setting values.

2.2 Co-processor board

A second processor board is used in the relay for the processing of the distance protection algorithms. The processor used on the second board is the same as that used on the main processor board. The second processor board has provision for fast access (zero wait state) SRAM for use with both program and data memory storage. This memory can be accessed by the main processor board via the parallel bus, and this route is used at power-on to download the software for the second processor from the flash memory on the main processor board. Further communication between the two processor boards is achieved via interrupts and the shared SRAM. The serial bus carrying the sample data is also connected to the co-processor board, using the processor's built-in serial port, as on the main processor board.

Coprocessor board works at 150 MHz.

2.3 Internal communication buses

The relay has two internal buses for the communication of data between different modules. The main bus is a parallel link which is part of a 64-way ribbon cable. The ribbon cable carries the data and address bus signals in addition to control signals and all power supply lines. Operation of the bus is driven by the main processor board which operates as a master while all other modules within the relay are slaves.

The second bus is a serial link which is used exclusively for communicating the digital sample values from the input module to the main processor board. The DSP processor has a built-in serial port which is used to read the sample data from the serial bus. The serial bus is also carried on the 64-way ribbon cable.

2.4 Input module

The input module provides the interface between the relay processor board and the analogue and digital signals coming into the relay. The input module consists of two PCBs; the main input board and a transformer board. The P442 and P444 relays provide three voltage inputs and four current inputs. They also provide an additional voltage input for the check sync function.

2.4.1 Transformer board

The transformer board holds up to four voltage transformers (VTs) and up to five current transformers (CTs). The current inputs will accept either 1A or 5A nominal current (menu and wiring options) and the nominal voltage input is 110 V.

The transformers are used both to step-down the currents and voltages to levels appropriate to the relay's electronic circuitry and to provide effective isolation between the relay and the power system. The connection arrangements of both the current and voltage transformer secondaries provide differential input signals to the main input board to reduce noise.

2.4.2 Input board

The main input board is shown as a block diagram in Figure 2. It provides the circuitry for the digital input signals and the analogue-to-digital conversion for the analogue signals. Hence it takes the differential analogue signals from the CTs and VTs on the transformer board(s), converts these to digital samples and transmits the samples to the processor board via the serial data bus. On the input board the analogue signals are passed through an anti-alias filter before being multiplexed into a single analogue-to-digital converter chip. The A – D converter provides 16-bit resolution and a serial data stream output. The digital input signals are opto isolated on this board to prevent excessive voltages on these inputs causing damage to the relay's internal circuitry.

2.4.3 Universal opto isolated logic inputs

The P442 and P444 relays are fitted with universal opto isolated logic inputs that can be programmed for the nominal battery voltage of the circuit of which they are a part. i.e. thereby allowing different voltages for different circuits e.g. signalling, tripping. They nominally provide a Logic 1 or On value for Voltages $\geq$80% of the set voltage and a Logic 0 or Off value for the voltages $\leq$60% of the set voltage. This lower value eliminates fleeting pickups that may occur during a battery earth fault, when stray capacitance may present up to 50% of battery voltage across an input.

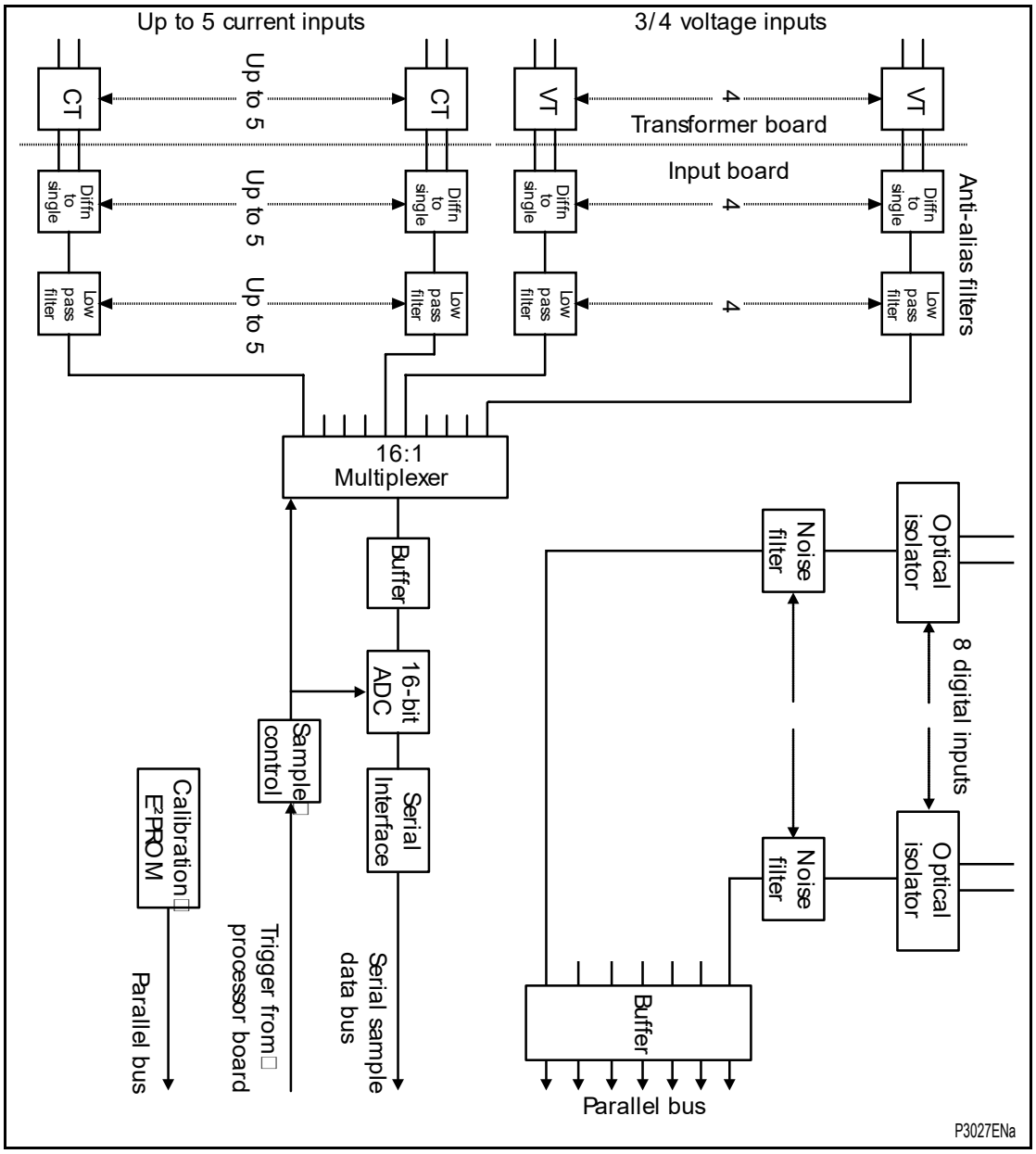


Figure 2 - Main Input Board

The other function of the input board is to read the state of the signals present on the digital inputs and present this to the parallel data bus for processing. The input board holds 8 optical isolators for the connection of up to eight digital input signals. The opto-isolators are used with the digital signals for the same reason as the transformers with the analogue signals; to isolate the relay's electronics from the power system environment. A 48 V 'field voltage' supply is provided at the back of the relay for use in driving the digital opto-inputs. The input board provides some hardware filtering of the digital signals to remove unwanted noise before buffering the signals for reading on the parallel data bus. Depending on the relay model, more than 8 digital input signals can be accepted by the relay. This is achieved by the use of an additional opto-board which contains the same provision for 8 isolated digital inputs as the main input board, but does not contain any of the circuits for analogue signals which are provided on the main input board.

Each input also has selectable filtering which can be utilised.

The P440 series relays are fitted with universal opto isolated logic inputs that can be programmed for the nominal battery voltage of the circuit of which they are a part i.e. thereby allowing different voltages for different circuits e.g. signalling, tripping. In the 'Opto Config' menu, they can also be programmed as Standard "60% – 80%" or "50% – 70%" to satisfy different operating constraints.

Threshold levels are as follows:

Nominal battery voltage (Vdc)	Standard 60% - 80%		50% - 70%	
	No Operation (logic 0) Vdc	Operation (logic 1) Vdc	No Operation (logic 0) Vdc	Operation (logic 1) Vdc
24 / 27	<16.2	>19.2	<12.0	>16.8
30 / 34	<20.4	>24.0	<15.0	>21.0
48 / 54	<32.4	>38.4	<24.0	>33.6
110 / 125	<75.0	>88.0	<55.0	>77.0
220 / 250	<150.0	>176.0	<110	>154

Table 1 – Opto inputs threshold levels

This lower value eliminates fleeting pickups that may occur during a battery earth fault, when stray capacitance may present up to 50% of battery voltage across an input.

Each input also has selectable filtering which can be utilised. This allows use of a pre-set filter of ½ cycle which renders the input immune to induced noise on the wiring: although this method is secure it can be slow, particularly for intertripping. This can be improved by switching off the ½ cycle filter in which case one of the following methods to reduce ac noise should be considered. The first method is to use double pole switching on the input, the second is to use screened twisted cable on the input circuit.

2.5 Power supply module (including output relays)

The power supply module contains two PCBs, one for the power supply unit itself and the other for the output relays. The power supply board also contains the input and output hardware for the rear communication port which provides an RS485 communication interface.

2.5.1 Power supply board (including RS485 communication interface)

One of three different configurations of the power supply board can be fitted to the relay. This will be specified at the time of order and depends on the nature of the supply voltage that will be connected to the relay. The three options are shown in Table 1 below.

Nominal dc range	Nominal ac range
24 – 48 V	dc only
48 – 110 V	30 – 100 V rms
110 – 250 V	100 – 240 V rms

Table 2 - Power supply options

The output from all versions of the power supply module are used to provide isolated power supply rails to all of the other modules within the relay. Three voltage levels are used within the relay, 5.1 V for all of the digital circuits, ±16 V for the analogue electronics, e.g. on the input board, and 22 V for driving the output relay coils. All power supply voltages including the 0 V earth line are distributed around the relay via the 64-way ribbon cable. One further voltage level is provided by the power supply board which is the 48 V field voltage. This is brought out to terminals on the back of the relay so that it can be used to drive the optically isolated digital inputs.

The two other functions provided by the power supply board are the RS485 communications interface and the watchdog contacts for the relay. The RS485 interface is used with the relay's rear communication port to provide communication using one of either Courier, Modbus or IEC 60870-5-103 protocols. The RS485 hardware supports half-duplex communication and provides optical isolation of the serial data being transmitted and received.

All internal communication of data from the power supply board is conducted via the output relay board which is connected to the parallel bus.

The watchdog facility provides two output relay contacts, one normally open and one normally closed which are driven by the processor board. These are provided to give an indication that the relay is in a healthy state.

2.5.2 Output relay board (standard)

The output relay board holds seven relays, three with normally open contacts and four with changeover contacts. The relays are driven from the 22 V power supply line. The relays' state is written to or read from using the parallel data bus. Depending on the relay model seven additional output contacts may be provided, through the use of up to three extra relay boards.

2.5.3 Output relay board (High speed / High break – Option)

The output relay board holds four relays, all normally open. The relays are driven from the 22 V power supply line. The relays' state is written to or read from using the parallel data bus.

A high speed output relay board contains a hybrid of MOSFET solid state devices (SSD) in parallel with high capacity relay output contacts. The MOSFET has a varistor across it to provide protection which is required when switching off inductive loads as the stored energy in the inductor causes a reverse high voltage which could damage the MOSFET.

When there is a control input command to operate an output contact, the miniature relay is operated at the same time as the SSD. The miniature relay contact closes in nominally 3.5 ms and is used to carry the continuous load current; the SSD operates in <0.2 ms and is switched off after 7.5 ms. When the control input resets to open the contacts, the SSD is again turned on for 7.5 ms. The miniature relay resets in nominally 3.5 ms before the SSD and so the SSD is used to break the load. The SSD absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching dc circuits only. As the SSD comes on very fast (<0.2 ms) then these high break output contacts have the added advantage of being very fast operating.

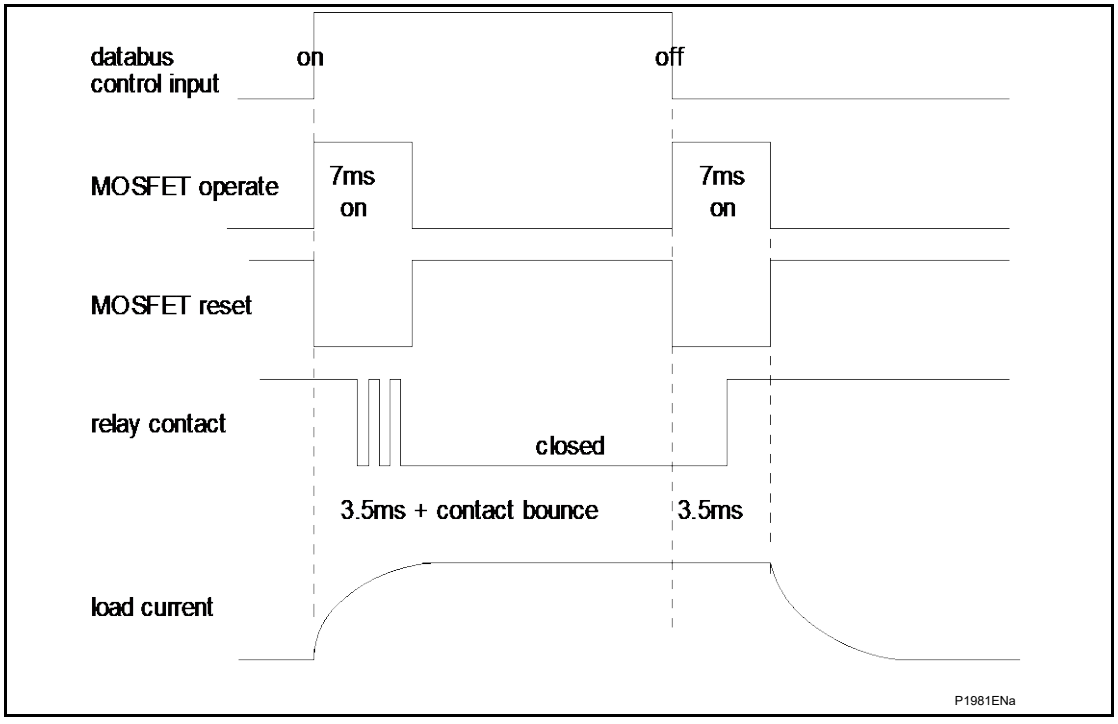


Figure 3: High break contact operation

2.6 IRIG-B board (P442 and P444 only)

The IRIG-B board is an order option which can be fitted to provide an accurate timing reference for the relay. This is available as a modulated or de-modulated option depending on the requirements. The IRIG-B signal is connected to the board via a BNC connector on the back of the relay. The timing information is used to synchronise the relay's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for the time tagging of the event, fault maintenance and disturbance records.

The IRIG-B board can also be specified with a fibre optic transmitter/receiver which can be used for the rear communication port instead of the RS485 electrical connection (IEC60870 only) and with the second rear communication board (see next section).

2.7 2nd rear communications board

For relays with Courier, Modbus, IEC 60870-5-103 or DNP3 protocol on the first rear communications port, the Courier protocol is used with an optional second rear communications port. The communication protocol network uses twisted pair K-Bus (non polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.

The second rear comms board and the IRIG-B board are mutually exclusive since they use the same hardware slot: Two versions of the second rear comms board are available; one with an IRIG-B input and one without. The physical layout of the second rear comms board is shown in Figure 4.

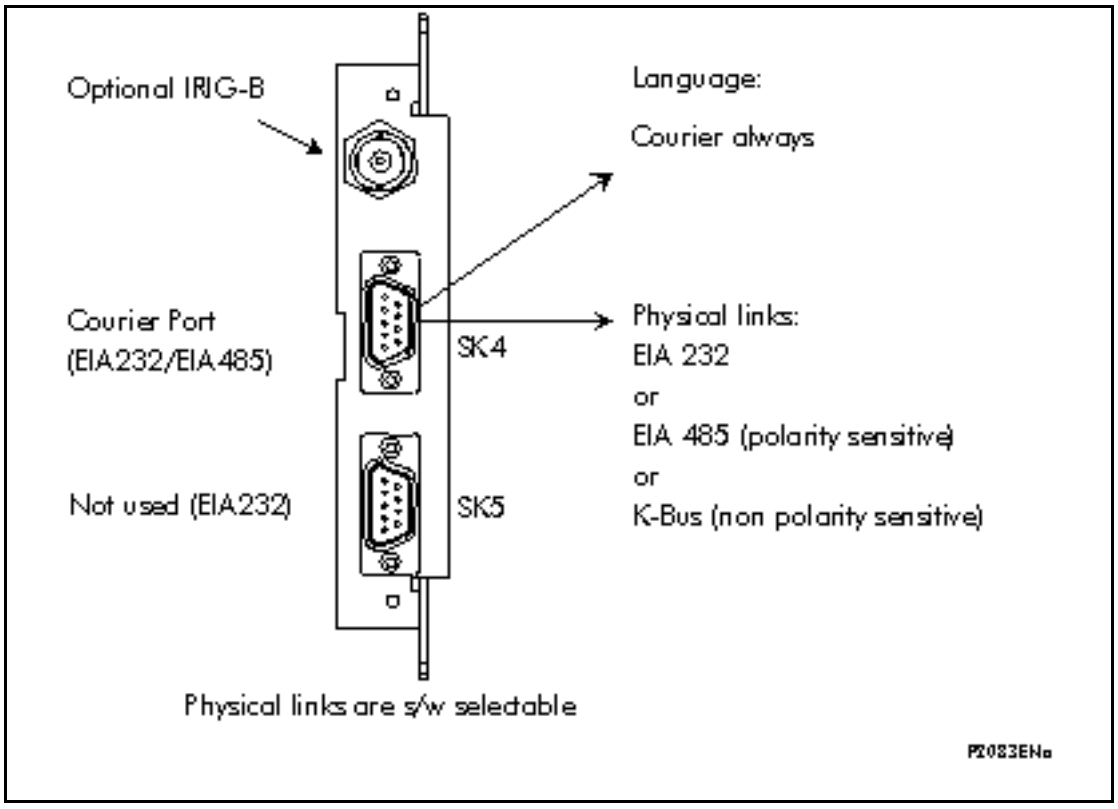


Figure 4: Rear comms. port

2.8 Ethernet and redundant boards

The Optional Ethernet board supports network connections of the following type:

- 10BASE-T
- 10BASE-FL
- 100BASE-TX
- 100BASE-FX

The optional Redundant Ethernet board (ZN0071) has 6 variants (refer to Px4x/EN REB user guide):

- redundant Ethernet (SHR protocol) with modulated or un-modulated IRIG-B,
- redundant Ethernet (RSTP protocol) with modulated or un-modulated IRIG-B,
- redundant Ethernet (DHS protocol) with modulated or un-modulated IRIG-B.

The optional 9-2 Ethernet board is the communication interface between MiCOM protection and the network. In the MiCOM Px4x protection, the 9-2 Ethernet board replaces the conventional analogue inputs (analogue module) wherever it/they stand.

For all copper based network connections an RJ45 style connector is supported. 10 Mbit/s fibre network connections use an ST style connector while 100 Mbit/s connections use the SC style fibre connection. An extra processor, a Motorola PPC, and memory block is fitted to the Ethernet card that is responsible for running all the network related functions such as TCP/IP/OSI as supplied by VxWorks and the UCA2/MMS server as supplied by Sisco inc. The extra memory block also holds the UCA2 data model supported by the relay.

2.9 Mechanical layout

The case materials of the relay are constructed from pre-finished steel which has a conductive covering of aluminium and zinc. This provides good earthing at all joints giving a low impedance path to earth which is essential for performance in the presence of external noise. The boards and modules use a multi-point earthing strategy to improve the immunity to external noise and minimise the effect of circuit noise. Ground planes are used on boards to reduce impedance paths and spring clips are used to ground the module metalwork.

Heavy duty terminal blocks are used at the rear of the relay for the current and voltage signal connections. Medium duty terminal blocks are used for the digital logic input signals, the output relay contacts, the power supply and the rear communication port. A BNC connector is used for the optional IRIG-B signal. 9-pin and 25-pin female D-connectors are used at the front of the relay for data communication.

Inside the relay the PCBs plug into the connector blocks at the rear, and can be removed from the front of the relay only. The connector blocks to the relay's CT inputs are provided with internal shorting links inside the relay which will automatically short the current transformer circuits before they are broken when the board is removed.

The front panel consists of a membrane keypad with tactile dome keys, an LCD and 12 LEDs mounted on an aluminium backing plate.

3 RELAY SOFTWARE

The relay software was introduced in the overview of the relay at the start of this section. The software can be considered to be made up of four sections:

- The real-time operating system
- The system services software
- The platform software
- The protection & control software

This section describes in detail the latter two of these, the platform software and the protection & control software, which between them control the functional behaviour of the relay. Figure 5 shows the structure of the relay software.

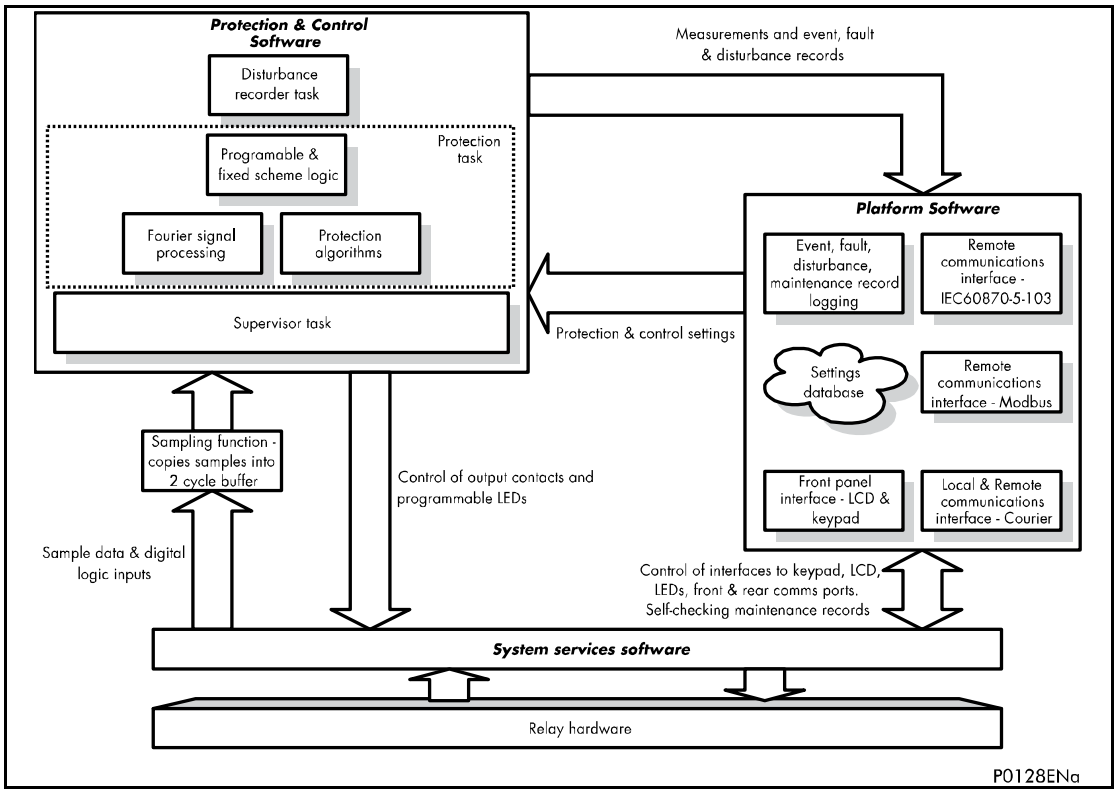


Figure 5 - Relay software structure

3.1 Real-time operating system

The software is split into tasks; the real-time operating system is used to schedule the processing of the tasks to ensure that they are processed in the time available and in the desired order of priority. The operating system is also responsible in part for controlling the communication between the software tasks through the use of operating system messages.

3.2 System services software

As shown in Figure 5, the system services software provides the interface between the relay's hardware and the higher-level functionality of the platform software and the protection & control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports, and controls the boot of the processor and downloading of the processor code into SRAM from non-volatile flash EPROM at power up.

3.3 Platform software

The platform software has three main functions:

- To control the logging of records that are generated by the protection software, including alarms and event, fault, and maintenance records.
- To store and maintain a database of all of the relay's settings in non-volatile memory.
- To provide the internal interface between the settings database and each of the relay's user interfaces, i.e. the front panel interface and the front and rear communication ports, using whichever communication protocol has been specified (Courier, Modbus, IEC 60870-5-103, DNP3).

3.3.1 Record logging

The logging function is provided to store all alarms, events, faults and maintenance records. The records for all of these incidents are logged in battery backed-up SRAM in order to provide a non-volatile log of what has happened. The relay maintains four logs: one each for up to 96 alarms (with 64 application alarms: 32 alarms in alarm status 1 and another group of 32 alarms in alarm status 2 and 32 alarms platform (see GC annex for mapping), 250 event records, 5 fault records and 5 maintenance records. The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software or the platform software is responsible for logging of a maintenance record in the event of a relay failure. This includes errors that have been detected by the platform software itself or error that are detected by either the system services or the protection software function. See also the section on supervision and diagnostics later in this section.

3.3.2 Settings database

The settings database contains all of the settings and data for the relay, including the protection, disturbance recorder and control & support settings. The settings are maintained in non-volatile E2PROM memory. The platform software's management of the settings database includes the responsibility of ensuring that only one user interface modifies the settings of the database at any one time. This feature is employed to avoid conflict between different parts of the software during a setting change. For changes to protection settings and disturbance recorder settings, the platform software operates a 'scratchpad' in SRAM memory. This allows a number of setting changes to be applied to the protection elements, disturbance recorder and saved in the database in E2PROM. (See § 3, section P44x/EN IT). If a setting change affects the protection & control task, the database advises it of the new values.

3.3.3 Database interface

The other function of the platform software is to implement the relay's internal interface between the database and each of the relay's user interfaces. The database of settings and measurements must be accessible from all of the relay's user interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each user interface.

3.4 Protection and control software

The protection and control software task is responsible for processing all of the protection elements and measurement functions of the relay. To achieve this it has to communicate with both the system services software and the platform software as well as organise its own operations. The protection software has the highest priority of any of the software tasks in the relay in order to provide the fastest possible protection response. The protection & control software has a supervisor task which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

3.4.1 Overview - protection and control scheduling

After initialisation at start-up, the protection and control task is suspended until there are sufficient samples available for it to process. The acquisition of samples is controlled by a 'sampling function' which is called by the system services software and takes each set of new samples from the input module and stores them in a two-cycle buffer. The protection and control software resumes execution when the number of unprocessed samples in the buffer reaches a certain number. For the 442-444 distance protection relay, the protection task is executed twice per cycle, i.e. after every 24 samples for the sample rate of 48 samples per power cycle used by the relay. The protection and control software is suspended again when all of its processing on a set of samples is complete. This allows operations by other software tasks to take place.

3.4.2 Signal processing

The sampling function provides filtering of the digital input signals from the opto-isolators and frequency tracking of the analogue signals. The digital inputs are checked against their previous value over a period of half a cycle. Therefore a change in the state of one of the inputs must be maintained over at least half a cycle before it is registered with the protection and control software.

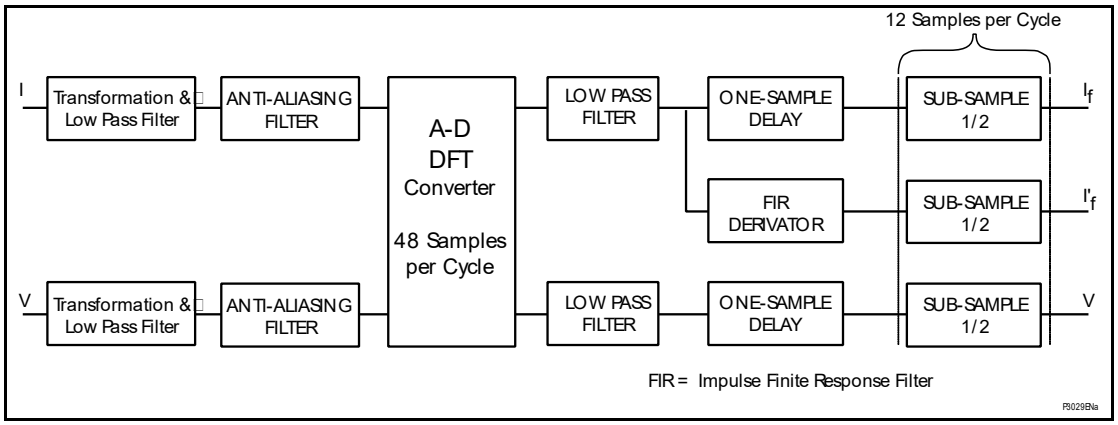


Figure 6 - Signal acquisition and processing

The frequency tracking of the analogue input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals, and works by detecting a change in the measured signal's phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module so as to achieve a constant sample rate of 48 samples per cycle of the power waveform. The value of the frequency is also stored for use by the protection and control task.

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analogue signals. The Fourier components are calculated using a one-cycle, 48-sample Discrete Fourier Transform (DFT). The DFT is always calculated using the last cycle of samples from the 2-cycle buffer, i.e. the most recent data is used. The DFT used in this way extracts the power frequency fundamental component from the signal and produces the magnitude and phase angle of the fundamental in rectangular component format. The DFT provides an accurate measurement of the fundamental frequency component, and effective filtering of harmonic frequencies and noise. This performance is achieved in conjunction with the relay input module which provides hardware anti-alias filtering to attenuate frequencies above the half sample rate, and frequency tracking to maintain a sample rate of 48 samples per cycle. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms. The samples from the input module are also used in an unprocessed form by the disturbance recorder for waveform recording and to calculate true rms values of current, voltage and power for metering purposes.

3.4.3 Programmable scheme logic

The purpose of the programmable scheme logic (PSL) is to allow the relay user to configure an individual protection scheme to suit their own particular application. This is achieved through the use of programmable logic gates and delay timers.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements, e.g. protection starts and trips, and the outputs of the fixed protection scheme logic. The fixed scheme logic provides the relay's standard protection schemes. The PSL itself consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, e.g. to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven; the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection and control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

This system provides flexibility for the user to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system, and because of this setting of the PSL is implemented through the PC support MiCOM S1 Agile.

3.4.4 Event and Fault Recording

A change in any digital input signal or protection element output signal causes an event record to be created. When this happens, the protection and control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer in SRAM which is controlled by the supervisor task. When the supervisor task receives either an event or fault record message, it instructs the platform software to create the appropriate log in battery backed-up SRAM. The operation of the record logging to battery backed-up SRAM is slower than the supervisor's buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost if the supervisor's buffer is full before the platform software is able to create a new log in battery backed-up SRAM. If this occurs then an event is logged to indicate this loss of information.

3.4.5 Disturbance recorder

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms for up to 8 analogue channels and the values of up to 64 digital signals. The recording time is user selectable up to a maximum of 10 seconds (the maximum storage capacity is 84 s). The disturbance recorder is supplied with data by the protection and control task once per cycle. The disturbance recorder collates the data that it receives into the required length disturbance record. It attempts to limit the demands on memory space by saving the analogue data in compressed format whenever possible. This is done by detecting changes in the analogue input signals and compressing the recording of the waveform when it is in a steady-state condition. The disturbance records can be extracted by MiCOM S1 Agile that can also store the data in COMTRADE format, thus allowing the use of other packages to view the recorded data.

3.4.6 Fault locator

The fault locator task is also separate from the protection and control task. The fault locator is invoked by the protection and control task when a fault is detected. The fault locator uses a 12-cycle buffer of the analogue input signals and returns the calculated location of the fault to the protection and control task which includes it in the fault record for the fault. When the fault record is complete (i.e. includes the fault location), the protection and control task can send a message to the supervisor task to log the fault record.

4 SELF TESTING & DIAGNOSTICS

The relay includes a number of self-monitoring functions to check the operation of its hardware and software when it is in service. These are included so that if an error or fault occurs within the relay's hardware or software, the relay is able to detect and report the problem and attempt to resolve it by rebooting. This involves the relay being out of service for a short period of time indicated by the 'Healthy' LED on the front of the relay being extinguished and the watchdog contact at the rear operating. If the restart fails to resolve the problem, then the relay will take itself permanently out of service. Again this will be indicated by the LED and watchdog contact.

If a problem is detected by the self-monitoring functions, the relay attempts to store a maintenance record in battery backed-up SRAM to allow the nature of the problem to be notified to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed when the relay is booted-up, e.g. at power-on, and secondly a continuous self-checking operation which checks the operation of the relay's critical functions whilst it is in service.

4.1 Start-up self-testing

The self-testing which is carried out when the relay is started takes a few seconds to complete, during which time the relay's protection is unavailable. This is signalled by the 'Healthy' LED on the front of the relay, which will illuminate when the relay has passed all of the tests and entered operation. If the testing detects a problem, the relay will remain out of service until it is manually restored to working order.

The operations that are performed at start-up are as follows:

4.1.1 System boot

The integrity of the flash EPROM memory is verified using a checksum before the program code and data stored in it is copied into SRAM to be used for execution by the processor. When the copy has been completed the data then held in SRAM is compared to that in the flash EPROM to ensure that the two are the same and that no errors have occurred in the transfer of data from flash EPROM to SRAM. The entry point of the software code in SRAM is then called which is the relay initialisation code.

4.1.2 Initialisation software

The initialisation process includes the operations of initialising the processor registers and interrupts, starting the watchdog timers (used by the hardware to determine whether the software is still running), starting the real-time operating system and creating and starting the supervisor task. In the course of the initialisation process the relay checks:

- the status of the battery.
- the integrity of the battery backed-up SRAM that is used to store event, fault and disturbance records.
- the voltage level of the field voltage supply that is used to drive the opto-isolated inputs.
- the operation of the LCD controller.
- the watchdog operation.

At the conclusion of the initialisation software the supervisor task begins the process of starting the platform software.

4.1.3 Platform software initialisation & monitoring

In starting the platform software, the relay checks the integrity of the data held in E2PROM with a checksum, the operation of the real-time clock, and the IRIG-B board if fitted. The final test that is made concerns the input and output of data; the presence and healthy condition of the input board is checked and the analogue data acquisition system is checked through sampling the reference voltage.

At the successful conclusion of all of these tests the relay is entered into service and the protection started-up.

4.2 Continuous self-testing

When the relay is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software (see section on relay software earlier in this document) and the results reported to the platform software. The functions that are checked are as follows:

- the flash EPROM containing all program code and language text is verified by a checksum.
- the code and constant data held in SRAM is checked against the corresponding data in flash EPROM to check for data corruption.
- the SRAM containing all data other than the code and constant data is verified with a checksum.
- the E2PROM containing setting values is verified by a checksum.
- the battery status.
- the level of the field voltage.
- the integrity of the digital signal I/O data from the opto-isolated inputs and the relay contacts is checked by the data acquisition function every time it is executed. The operation of the analogue data acquisition system is continuously checked by the acquisition function every time it is executed, by means of sampling the reference voltages.
- the operation of the IRIG-B board is checked, where it is fitted, by the software that reads the time and date from the board.

In the unlikely event that one of the checks detects an error within the relay's subsystems, the platform software is notified and it will attempt to log a maintenance record in battery backed-up SRAM. If the problem is with the battery status or the IRIG-B board, the relay will continue in operation. However, for problems detected in any other area the relay will initiate a shutdown and re-boot. This will result in a period of up to 5 seconds when the protection is unavailable, but the complete restart of the relay including all initialisations should clear most problems that could occur. As described above, an integral part of the start-up procedure is a thorough diagnostic self-check. If this detects the same problem that caused the relay to restart, i.e. the restart has not cleared the problem, then the relay will take itself permanently out of service. This is indicated by the 'Healthy' LED on the front of the relay, which will extinguish, and the watchdog contact which will operate.

COMMISSIONING

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1 INTRODUCTION

The MiCOM P44x distance protection relays are fully numerical in their design, implementing all protection and non-protection functions in software. The relays employ a high degree of self-checking and, in the unlikely event of a failure, will give an alarm. As a result of this, the commissioning tests do not need to be as extensive as with non-numerical electronic or electro-mechanical relays.

To commission numerical relays, it is only necessary to verify that the hardware is functioning correctly and the application-specific software settings have been applied to the relay. It is considered unnecessary to test every function of the relay if the settings have been verified by one of the following methods:

Extracting the settings applied to the relay using appropriate setting software (preferred method) using the operator interface.

To confirm the product is operating correctly once the application-specific settings have been applied, a test should be performed on a single protection element.

Unless previously agreed, the customer will be responsible for determining the application-specific settings to be applied to the relay and for testing of any scheme logic applied by external wiring and/or configuration of the relay's internal programmable scheme logic.

As the relay's menu language is user-selectable, it is acceptable for the Commissioning Engineer to change it to allow accurate testing as long as the menu is restored to the customer's preferred language on completion.

To simplify the specifying of menu cell locations in these Commissioning Instructions, they will be given in the form [Courier reference: COLUMN HEADING, Cell Text]. For example, the cell for selecting the menu language (first cell under the column heading) is located in the System Data column (column 00) so it would be given as [0001: SYSTEM DATA, Language].



Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety and Installation chapters of this manual.

2 SETTING FAMILIARISATION

When commissioning a MiCOM P44x relay for the first time, allow enough time to become familiar with the method the settings are applied.

With the secondary front cover in place all keys except the [Enter] key are accessible. All menu cells can be read. LEDs and alarms can be reset. However, no protection or configuration settings can be changed, or fault and event records cleared.

Removing the secondary front cover allows access to all keys so that settings can be changed, LEDs and alarms reset, and fault and event records cleared. However, menu cells which have access levels higher than the default level will require the appropriate password to be entered before changes can be made.

Alternatively, if a portable PC is available together with suitable setting software (such as MiCOM S1 Agile), the menu can be viewed a page at a time to display a full column of data and text. This PC software also allows settings to be entered more easily, saved to a file on disk for future reference or printed to produce a settings record. Refer to the PC software user manual for details. If the software is being used for the first time, allow sufficient time to become familiar with its operation.

3 EQUIPMENT REQUIRED FOR COMMISSIONING

3.1 Minimum Equipment Required

Overcurrent test set with interval timer

110 V ac voltage supply (if stage 1 of the overcurrent function is set directional)

Multimeter with suitable ac current range, and ac and dc voltage ranges of 0-440 V and 0-250 V respectively

Continuity tester (if not included in multimeter)

Phase angle meter

Phase rotation meter

Note: Modern test equipment may contain many of the above features in one unit.

3.2 Optional Equipment

Multi-finger test plug type MMLB01 (if test block type MMLG installed)

An electronic or brushless insulation tester with a dc output not exceeding 500 V (For insulation resistance testing when required).

A portable PC, with appropriate software (This enables the rear communications port to be tested if this is to be used and will also save considerable time during commissioning).

KITZ K-Bus to RS232 protocol converter (if RS485 K-Bus port is being tested and one is not already installed).

RS485 to RS232 converter (if RS485 Modbus port is being tested).

A printer (for printing a setting record from the portable PC).

4 PRODUCT CHECKS

These product checks cover all aspects of the relay that need to be checked to ensure that it has not been physically damaged prior to commissioning, is functioning correctly and all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the relay prior to commissioning, it is advisable to make a copy of the settings so as to allow their restoration later. This could be done by:

- Obtaining a setting file on a diskette from the customer (This requires a portable PC with appropriate setting software for transferring the settings from the PC to the relay)
- Extracting the settings from the relay itself (This again requires a portable PC with appropriate setting software)
- Manually creating a setting record. This could be done using a copy of the setting record located at the end of this chapter to record the settings as the relay's menu is sequentially stepped through via the front panel user interface.

If password protection is enabled and the customer has changed password 2 that prevents unauthorised changes to some of the settings, either the revised password 2 should be provided, or the customer should restore the original password prior to commencement of testing.

Note: If the password has been lost, a recovery password can be obtained from GE Vernova by quoting the serial number of the relay. The recovery password is unique to that relay and will not work on any other relay.

4.1 With the Relay De-energised

The following group of tests should be carried out without the auxiliary supply being applied to the relay and with the trip circuit isolated.



The current and voltage transformer connections must be isolated from the relay for these checks. If an MMLG test block is provided, the required isolation can easily be achieved by inserting test plug type MMLB01 which effectively open-circuits all wiring routed through the test block.

Before inserting the test plug, reference should be made to the scheme (wiring) diagram to ensure that this will not potentially cause damage or a safety hazard. For example, the test block may also be associated with protection current transformer circuits. It is essential that the sockets in the test plug which correspond to the current transformer secondary windings are linked before the test plug is inserted into the test block.



DANGER: NEVER OPEN-CIRCUIT THE SECONDARY CIRCUIT OF A CURRENT TRANSFORMER SINCE THE HIGH VOLTAGE PRODUCED MAY BE LETHAL AND COULD DAMAGE THE INSULATION.

If a test block is not provided, the voltage transformer supply to the relay should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the relay terminals. Where means of isolating the auxiliary supply and trip circuit (e.g. isolation links, fuses, MCB, etc.) are provided, these should be used. If this is not possible, the wiring to these circuits will have to be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

4.1.1 Visual Inspection

Carefully examine the relay to see that no physical damage has occurred since installation.

The rating information given under the top access cover on the front of the relay should be checked to ensure it is correct for the particular installation.

Ensure the case earthing connections, bottom left-hand corner at the rear of the relay case, are used to connect the relay to a local earth bar using an adequate conductor.

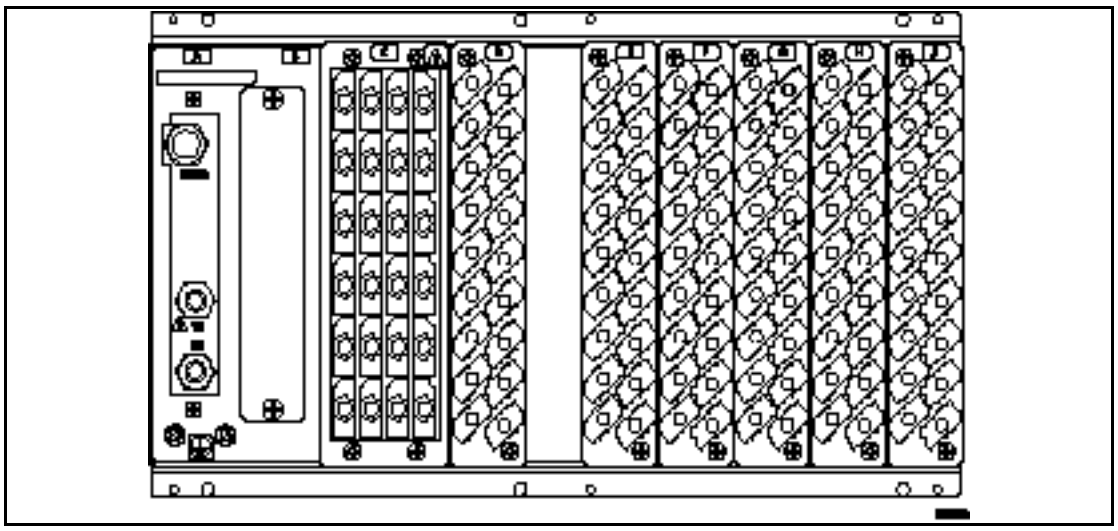


Figure 1a: Rear terminal blocks on size 60TE case (P442)

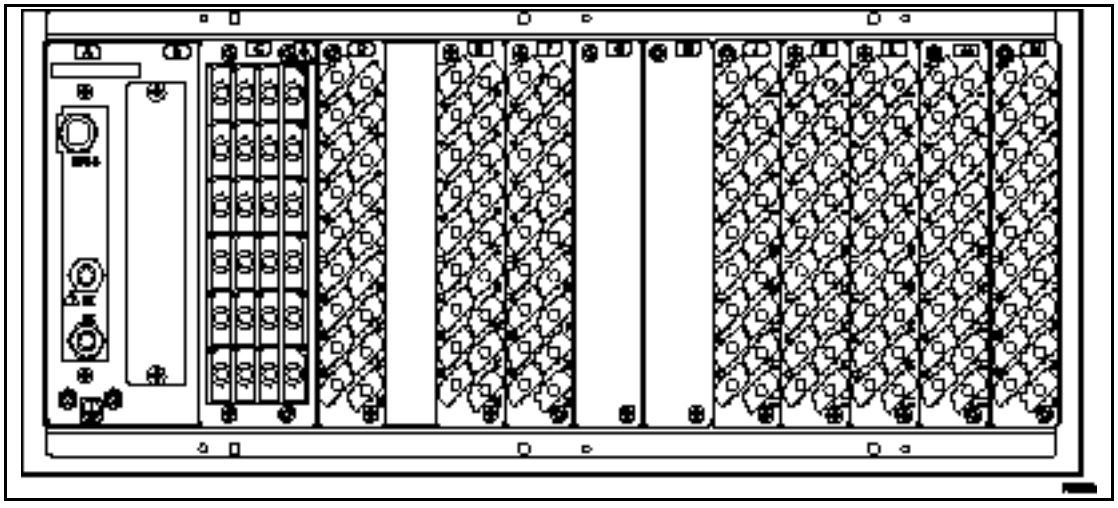


Figure 1b: Rear terminal blocks on size 80TE case (P444)

4.1.2 Current Transformer Shorting Contacts

If required, the current transformer shorting contacts can be checked to ensure they close when the heavy duty terminal block is disconnected from the current input PCB.

The heavy duty terminal block is fastened to the rear panel using four crosshead screws. These are located top and bottom between the first and second, and third and fourth, columns of terminals.

Note:	*The use of a magnetic bladed screwdriver is recommended to minimize the risk of the screws being left in the terminal block or lost.*

Pull the terminal block away from the rear of the case and check that all the shorting switches being used are closed with a continuity tester. Table 1 shows the terminals between which shorting contacts are fitted.

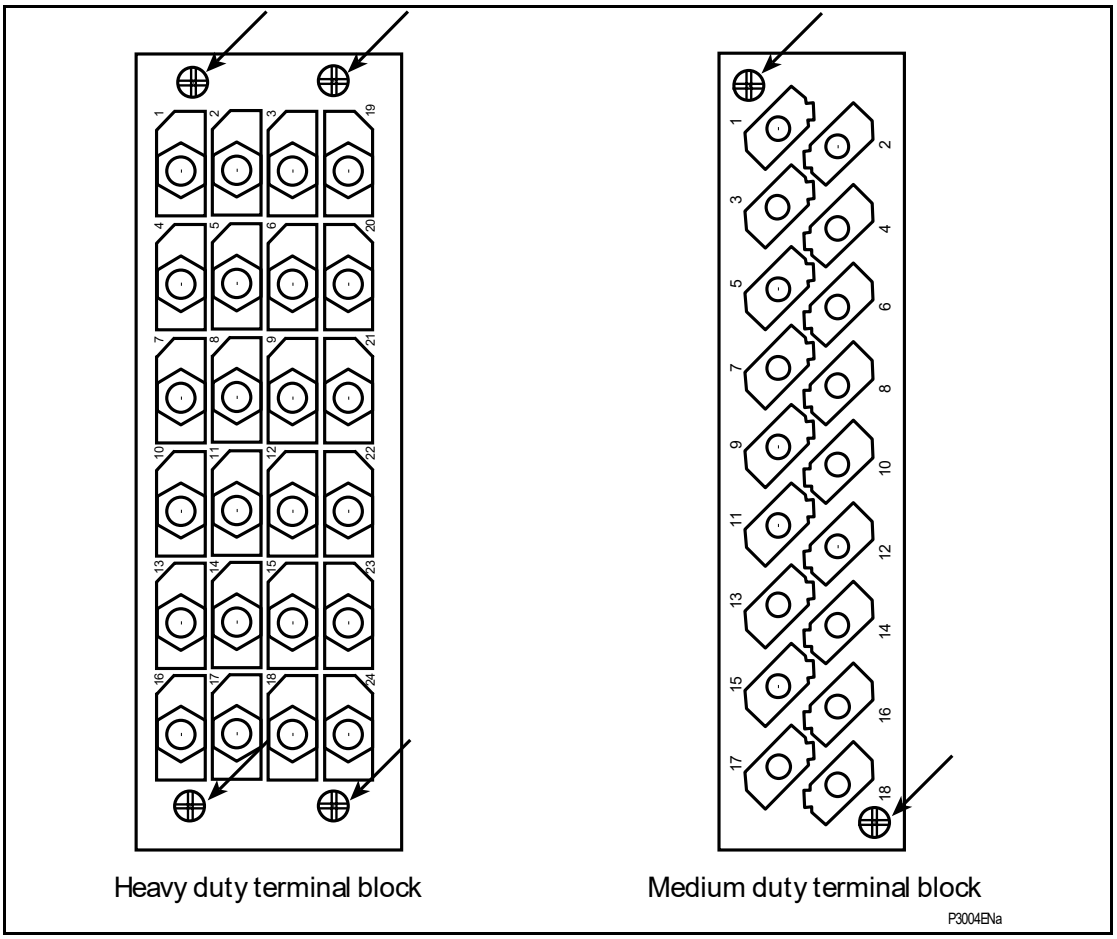


Figure 1: Location of Securing Screws for Terminal Blocks

Current Input	Shorting contact between terminals	
	1A CT's	5A CT's
IA	C3-C2	C1-C2
IB	C6-C5	C4-C5
IC	C9-C8	C7-C8
IM	C12-C11	C10-C11

Table 1 - Current Transformer Shorting Contact Locations

4.1.3 External Wiring

Check the external wiring is correct to the relevant relay diagram or scheme diagram. The relay diagram number appears on the rating label under the top access cover on the front of the relay. The corresponding connection diagram will have been supplied with the Alstom Grid order acknowledgement for the relay.

If a test block is provided, the connections should be checked against the scheme (wiring) diagram. It is recommended that the supply connections are to the live side of the test block (coloured orange with the odd numbered terminals (1, 3, 5, 7 etc.)). The auxiliary supply is normally routed via terminals 13 (supply positive) and 15 (supply negative), with terminals 14 and 16 connected to the relay's positive and negative auxiliary supply terminals respectively. However, check the wiring against the schematic diagram for the installation to ensure compliance with the customer's normal practice.

4.1.4 Insulation

Insulation resistance tests are only necessary during commissioning if it is required for them to be done and they have not been performed during installation.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a dc voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The main groups of relay terminals are:

- Voltage transformer circuits.
- Current transformer circuits
- Auxiliary voltage supply.
- Field voltage output and opto-isolated control inputs.
- Relay contacts.
- RS485 communication port.
- Case earth.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the unit.

4.1.5 Watchdog Contacts

Using a continuity tester, check that the normally closed watchdog contacts are in the states given in Table 2 for a de-energised relay.

Terminals		Contact State	
		Relay De-energised	Relay Energised
J11-J12 N11-N12	(P442) (P444)	Closed	Open
J13-J14 N13-N14	(P442) (P444)	Open	Closed

Table 2 - Watchdog Contact Status

4.1.6 Auxiliary Supply

The relay can be operated from either a dc only or an ac/dc auxiliary supply depending on the relay's nominal supply rating. The incoming voltage must be within the operating range specified in Table 3.

Without energising the relay, measure the auxiliary supply to ensure it is within the operating range.



Nominal Supply Rating DC [AC rms]		DC Operating Range	AC Operating Range
24/54 V	[-]	19 – 65 V	-
48/110 V	[30/100 V]	37 – 150 V	24 – 110 V
110/250 V	[100/240 V]	87 – 300 V	80 – 265 V

Table 3 - Operational Range of Auxiliary Supply

The relay can withstand an ac ripple of up to 12% of the upper rated voltage on the dc auxiliary supply.

Do not energise the relay using the battery charger with the battery disconnected as this can irreparably damage the relay's power supply circuitry.

Energise the relay if the auxiliary supply is within the operating range. If an MMLG test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the relay.

4.2 With the Relay Energised

The following group of tests verify that the relay hardware and software is functioning correctly and should be carried out with the auxiliary supply applied to the relay.

The current and voltage transformer connections must remain isolated from the relay for these checks.

4.2.1 Watchdog Contacts

Using a continuity tester, check the watchdog contacts are in the states given in Table 3 for an energized relay.

4.2.2 Date and Time

The date and time should now be set to the correct values. The method of setting will depend on whether accuracy is being maintained via the optional Inter-Range Instrumentation Group standard B (IRIG-B) port on the rear of the relay.

4.2.3 With an IRIG-B signal

If a satellite time clock signal conforming to IRIG-B is provided and the relay has the optional IRIG-B port fitted, the satellite clock equipment should be energised.

To allow the relay's time and date to be maintained from an external IRIG-B source cell [0804: DATE and TIME, IRIG-B Sync] must be set to 'Enabled'.

Ensure the relay is receiving the IRIG-B signal by checking that cell [0805: DATE and TIME, IRIG-B Status] reads 'Active'.

Once the IRIG-B signal is active, adjust the time offset of the universal co-ordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.

Check the time, date and month are correct in cell [0801: DATE and TIME, Date/Time]. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.

In the event of the auxiliary supply failing, with a battery fitted in the compartment behind the bottom access cover, the time and date will be maintained. Therefore, when the auxiliary supply is restored, the time and date will be correct and not need to be set again.

To test this, remove the IRIG-B signal, then remove the auxiliary supply from the relay. Leave the relay de-energized for approximately 30 seconds. On re-energisation, the time in cell [0801: DATE and TIME, Date/Time] should be correct.

Reconnect the IRIG-B signal.

4.2.4 Without an IRIG-B signal

If the time and date is not being maintained by an IRIG-B signal, ensure that cell [0804: DATE and TIME, IRIG-B Sync] is set to 'Disabled'.

Set the date and time to the correct local time and date using cell [0801: DATE and TIME, Date/Time].

In the event of the auxiliary supply failing, with a battery fitted in the compartment behind the bottom access cover, the time and date will be maintained. Therefore when the auxiliary supply is restored the time and date will be correct and not need to be set again.

To test this, remove the auxiliary supply from the relay for approximately 30 seconds. On re-energisation, the time in cell [0801: DATE and TIME, Date/Time] should be correct.

4.2.5 Light Emitting Diodes (LEDs)

On power up the green LED should have illuminated and stayed on indicating that the relay is healthy. The relay has non-volatile memory which remembers the state (on or off) of the alarm, trip and, if configured to latch, user-programmable LED indicators when the relay was last energised from an auxiliary supply. Therefore these indicators may also illuminate when the auxiliary supply is applied.



Check the PSL enabled in the internal logic.

If any of these LEDs are on then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes out), there is no testing required for that LED because it is known to be operational.

Testing the alarm and out of service LEDs

The alarm and out of service LEDs can be tested using the COMMISSIONING TESTS menu column. Set cell [0F0E: COMMISSIONING TESTS, Test Mode] to 'Enabled'. Check that the alarm and out of service LEDs illuminate.

It is not necessary to return cell [0F0E: COMMISSIONING TESTS, Test Mode] to 'Disabled' at this stage because the test mode will be required for later tests.

Testing the trip LED

The trip LED can be tested by initiating a manual circuit breaker trip from the relay. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

Testing the user-programmable LEDs

To test the user-programmable LEDs set cell [0F12: COMMISSIONING TESTS, Test LEDs] to 'Apply Test'. Check that all 8 LEDs on the right-hand side of the relay illuminate.

4.2.6 Field Voltage Supply

The relay generates a field voltage of nominally 48 V that should be used to energise the opto-isolated inputs.

Measure the field voltage across the terminals given in Table 4. Check that the field voltage is present at each positive and negative terminal and that the polarity is correct.

Repeat for terminals 8 and 10.

Supply rail	**Terminals**	
	P442	P444
+48 Vdc	J7 & J8	N7 & N8
–48 Vdc	J9 & J10	N9 & N10

Table 4 - Field Voltage Terminals

4.2.7 Input Opto-isolators

This test checks that all the opto-isolated inputs are functioning correctly. P442 relays have 16 opto-isolated inputs and P444 relays have 24 opto-isolated inputs.

The opto-isolated inputs should be energised one at a time. Ensuring correct polarity, connect the field supply voltage to the appropriate terminals for the input being tested. The opto-isolated input terminal allocations are given in Table 5.



Note: The opto-isolated inputs may be energised from an external 50 V battery in some installations. Check that this is not the case before connecting the field voltage otherwise damage to the relay may result.

The status of each opto-isolated input can be viewed using cell [0020: SYSTEM DATA, Opto I/P Status], a '1' indicating an energised input and a '0' indicating a de-energised input. When each opto-isolated input is energised one of the characters on the bottom line of the display will change to the value shown in Table 5 to indicate the new state of the inputs.

	Apply field voltage to terminals			
	P442		**P444**	
	-ve	**+ve**	**-ve**	**+ve**
Opto input 1	D1	D2	D1	D2
Opto input 2	D3	D4	D3	D4
Opto input 3	D5	D6	D5	D6
Opto input 4	D7	D8	D7	D8
Opto input 5	D9	D10	D9	D10
Opto input 6	D11	D12	D11	D12
Opto input 7	D13	D14	D13	D14

	Apply field voltage to terminals			
	P442		P444	
	-ve	+ve	-ve	+ve
Opto input 8	D15	D16	D15	D16
Opto input 9	E1	E2	E1	E2
Opto input 10	E3	E4	E3	E4
Opto input 11	E5	E6	E5	E6
Opto input 12	E7	E8	E7	E8
Opto input 13	E9	E10	E9	E10
Opto input 14	E11	E12	E11	E12
Opto input 15	E13	E14	E13	E14
Opto input 16	E15	E16	E15	E16
Opto input 17			F1	F2
Opto input 18			F3	F4
Opto input 19			F5	F6
Opto input 20			F7	F8
Opto input 21			F9	F10
Opto input 22			F11	F12
Opto input 23			F13	F14
Opto input 24			F15	F16

Table 5 - Opto-isolated Input Terminals

4.2.8 Output Relays

This test checks that all the output relays are functioning correctly. The P442 relays have 21 output relays and the P444 relays have 32 output relays.

Ensure that the relay is still in test mode by viewing cell [0F0E: COMMISSIONING TESTS, Test Mode].

The output relays should be energised one at a time. To select output relay 1 for testing, set cell [0F0F: COMMISSIONING TESTS, Test Pattern] as shown in Table 6.

Connect a continuity tester across the terminals corresponding to output relay 1 given in Table 6.

To operate the output relay set cell [0F11: COMMISSIONING TESTS, Contact Test] to 'Apply Test'. Operation will be confirmed by the continuity tester operating for a normally open contact and ceasing to operate for a normally closed contact.

Reset the output relay by setting cell [0F11: COMMISSIONING TESTS, Contact Test] to 'Remove Test'.

> *Note: Ensure that thermal ratings of anything connected to the output relays during the contact test procedure are not exceeded by the associated output relay being operated for too long. It is therefore advised that the time between application and removal of contact test be kept to the minimum.*

Repeat the test for all the other output relays (number depends on the model).

MiCOM P442						
Output	N/C	N/O		Output	N/C	N/O
Without high break relay board (all models except P442×××C)						
Relay 1	-	H1-H2		Relay 12	G10-G12	G11-G12
Relay 2	-	H3-H4		Relay 13	G13-G15	G14-G15
Relay 3	-	H5-H6		Relay 14	G16-G18	G17-G18

Relay 4	H7-H9	H8-H9		Relay 15	-	F1-F2
Relay 5	H10-H12	H11-H12		Relay 16	-	F3-F4
Relay 6	H13-H15	H14-H15		Relay 17	-	F5-F6
Relay 7	H16-H18	H17-H18		Relay 18	F7-F9	F8-F9
Relay 8	-	G1-G2		Relay 19	F10-F12	F11-F12
Relay 9	-	G3-G4		Relay 20	F13-F15	F14-F15
Relay 10	-	G5-G6		Relay 21	F16-F18	F17-F18
Relay 11	G7-G9	G8-G9				
With high break relay board (model P442×××C)						
Output	**N/C**	**N/O**		**Output**	**N/C**	**N/O**
Relay 1	-	H1-H2		Relay 10	-	G5-G6
Relay 2	-	H3-H4		Relay 11	G7-G9	G8-G9
Relay 3	-	H5-H6		Relay 12	G10-G12	G11-G12
Relay 4	H7-H9	H8-H9		Relay 13	G13-G15	G14-G15
Relay 5	H10-H12	H11-H12		Relay 14	G16-G18	G17-G18
Relay 6	H13-H15	H14-H15		HB relay 15	-	F3(–)-F4
Relay 7	H16-H18	H17-H18		HB relay 16	-	F7(–)-F8(+)
Relay 8	-	G1-G2		HB relay 17	-	F11(–)-F12(+)
Relay 9	-	G3-G4		HB relay 18	-	F15(–)-F16(+)

MiCOM P444						
Output	**N/C**	**N/O**		**Output**	**N/C**	**N/O**
Without high break relay board (all models except P444×××C)						
Relay 1	-	M1-M2		Relay 24	K16-K18	K17-K18
Relay 2	-	M3-M4		Relay 25	-	J1-J2
Relay 3	-	M5-M6		Relay 26	-	J3-J4
Relay 4	-	M7-M8		Relay 27	-	J5-J6
Relay 5	-	M9-M10		Relay 28	-	J7-J8
Relay 6	-	M11-M12		Relay 29	-	J9-J10
Relay 7	M13-M15	M14-M15		Relay 30	-	J11-J12
Relay 8	M16-M18	M17-M18		Relay 31	J13-J15	J14-J15
Relay 9	-	L1-L2		Relay 32	J16-J18	J17-J18
Relay 10	-	L3-L4		Relay 33	-	H1-H2
Relay 11	-	L5-L6		Relay 34	-	H3-H4
Relay 12	-	L7-L8		Relay 35	-	H5-H6
Relay 13	-	L9-L10		Relay 36	H7-H9	H8-H9
Relay 14	-	L11-L12		Relay 37	H10-H12	H11-H12
Relay 15	L13-L15	L14-L15		Relay 38	H13-H15	H14-H15
Relay 16	L16-L18	L17-L18		Relay 39	H16-H18	H17-H18
Relay 17	-	K1-K2		Relay 40	-	G1-G2
Relay 18	-	K3-K4		Relay 41	-	G3-G4
Relay 19	-	K5-K6		Relay 42	-	G5-G6
Relay 20	-	K7-K8		Relay 43	G7-G9	G8-G9
Relay 21	-	K9-K10		Relay 44	G10-G12	G11-G12
Relay 22	-	K11-K12		Relay 45	G13-G15	G14-G15
Relay 23	K13-K15	K14-K15		Relay 46	G16-G18	G17-G18
With high break relay board (model P444×××C)						
Relay 1	-	M1-M2		HB relay 18	-	J7(–)-J8(+)
Relay 2	-	M3-M4		HB relay 19	-	J11(–)-J12(+)

Relay 3	-	M5-M6	HB relay 20	-	J15(–)-J16(+)
Relay 4	-	M7-M8	Relay 21	-	H1-H2
Relay 5	-	M9-M10	Relay 22	-	H3-H4
Relay 6	-	M11-M12	Relay 23	-	H5-H6
Relay 7	M13-M15	M14-M15	Relay 24	H7-H9	H8-H9
Relay 8	M16-M18	M17-M18	Relay 25	H10-H12	H11-H12
HB relay 9		L3(–)-L4(+)	Relay 26	H13-H15	H14-H15
HB relay 10		L7(–)-L8(+)	Relay 27	H16-H18	H17-H18
HB relay 11		L11(–)-L12(+)	Relay 28	-	G1-G2
HB relay 12		L15(–)-L16(+)	Relay 29	-	G3-G4
HB relay 13		K3(–)-K4(+)	Relay 30	-	G5-G6
HB relay 14		K7(–)-K8(+)	Relay 31	G7-G9	G8-G9
HB relay 15		K11(–)-K12(+)	Relay 32	G10-G12	G11-G12
HB relay 16		K15(–)-K16(+)	Relay 33	G13-G15	G14-G15
HB relay 17		J3(–)-J4(+)	Relay 34	G16-G18	G17-G18

Table 6 - Relay Output Terminals and Test Pattern Settings

Return the relay to service by setting cell [0F0E: COMMISSIONING TESTS, Test Mode] to 'Disabled'.

4.2.9 Rear Communications Port

This test should only be performed where the relay is to be accessed from a remote location and will vary depending on the communications standard being adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

4.2.9.1 Courier Communications

If a K-Bus to RS232 KITZ protocol converter is installed, connect a portable PC running the appropriate software to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the type installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's K-Bus port. The terminal numbers for the relay's K-Bus port are given in Table 7. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's K-Bus port will be confirmed.

Connection		**Terminal**	
K-Bus	Modbus or VDEW	P442	P444
Screen	Screen	J16	N16
1	+ve	J17	N17
2	–ve	J18	N18

Table 7 - RS485 Terminals

Ensure the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E02: COMMUNICATIONS, Remote Address] must be set to a value between 0 and 255.

Check that communications can be established with this relay using the portable PC.

4.2.9.2 Modbus Communications

Connect a portable PC running the appropriate Modbus Master Station software to the relay's RS485 port via a RS485 to RS232 interface converter. The terminal numbers for the relay's RS485 port are given in Table 7.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E03: COMMUNICATIONS, Remote Address], [0E06: COMMUNICATIONS, Baud Rate] and [0E07: COMMUNICATIONS, Parity] of the relay.

Check that communications with this relay can be established.

4.2.9.3 IEC 60870-5-103 (VDEW) Communications

If the relay has the optional fibre optic communications port fitted, the port to be used should be selected by setting cell [0E09: COMMUNICATIONS, Physical Link] to 'Fibre Optic' or 'RS485'.

IEC 60870-5-103/VDEW communication systems are designed to have a local Master Station and this should be used to verify that the relay's fibre optic or RS485 port, as appropriate, is working.

Ensure that the relay address and baud rate settings in the application software are set the same as those in cells [0E03: COMMUNICATIONS, Remote Address] and [0E06: COMMUNICATIONS, Baud Rate] of the relay.

Check that, using the Master Station, communications with the relay can be established.

4.2.10 Current Inputs

This test verifies that the accuracy of current measurement is within the acceptable tolerances.

All relays will leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required then this must be set in cell [0009: SYSTEM DATA, Frequency].

Apply current equal to the line current transformer secondary winding rating to the each current transformer input of the corresponding rating in turn, checking its magnitude using a multimeter. Refer to Table 8 for the corresponding reading in the relay's MEASUREMENTS 1 column and record the value displayed.

Cell in MEASUREMENTS 1 column (02)		**Apply current to**	
		1A line CT	**5A line CT**
[0201: IA Magnitude]		C3-C2	C1-C2
[0203: IB Magnitude]		C6-C5	C4-C5
[0205: IC Magnitude]		C9-C8	C7-C8
[022F IM Magnitude] or [0209: IN Mag]		C12-C11	C10-C11

Table 8 - Current Input Terminals

The measured current values on the relay will either be in primary or secondary Amperes. If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Primary', the values displayed on the relay should be equal to the applied current multiplied by the corresponding current transformer ratio set in the 'VT and CT RATIOS' menu column (see Table 9). If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Secondary', the value displayed should be equal to the applied current.

The measurement accuracy of the relay is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Cell in MEASUREMENTS 1 column (02)	**Corresponding CT Ratio (in 'VT and CT RATIO column (0A) of menu)**
[0201: IA Magnitude] [0203: IB Magnitude] [0205: IC Magnitude]	**Error! Bookmark not defined.** $\frac{\text{0A07:Phase CT Primary}}{\text{0A08:Phase CT Sec'y}}$

[022F: IM Mutual Current Mag] or [0209: IN Mag]	$\frac{\text{0A0B:MComp/CT Primary}}{\text{0A0C:MComp CT Sec'y}}$

Table 9 - CT Ratio Settings

4.2.11 Voltage Inputs

This test verifies that the accuracy of voltage measurement is within the acceptable tolerances.

Apply rated voltage to each voltage transformer input in turn, checking its magnitude using a multimeter. Refer to Table 8 for the corresponding reading in the relay's MEASUREMENTS 1 column and record the value displayed.

Cell in MEASUREMENTS 1 column (02)	Voltage applied To
[021A: VAN Magnitude]	C19-C22
[021C: VBN Magnitude]	C20-C22
[021E: VCN Magnitude]	C21-C22
[022B: C/S Voltage Mag] * or [0222: VN Mag]	C23-C24

Table 10 - Voltage Input Terminals

The measured voltage values on the relay will either be in primary or secondary volts. If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Primary', the values displayed on the relay should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio set in the 'VT and CT RATIOS' menu column (see Table 11). If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Secondary', the value displayed should be equal to the applied voltage.

The measurement accuracy of the relay is ±2%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Cell in MEASUREMENTS 1 column (02)	Corresponding VT Ratio (in 'VT and CT RATIO column (0A) of menu)
[021A: VAN Magnitude] [021C: VBN Magnitude] [021E: VCN Magnitude]	**Error! Bookmark not defined.** $\frac{\text{0A01:Main VT Primary}}{\text{0A02:Main VT Sec'y}}$
[022B: C/S Voltage Mag] or [0223: VN Ang]	$\frac{\text{0A03:4th VT Primary}}{\text{0A04:4th VT Sec'y}}$

Table 11 - VT Ratio Settings

* Voltage reference for synchrocheck
Can be PGnd or PP reference with VT bus side or VT line
(see setting description in chapter AP section 4.4)

5 SETTING CHECKS

The setting checks ensure that all of the application-specific relay settings (i.e. both the relay's function and programmable scheme logic settings) for the particular installation have been correctly applied to the relay.

If the application-specific settings are not available, ignore sections 5.1 and 5.2.

5.1 Apply Application-Specific Settings

There are two methods of applying the settings:

- Transferring them from a pre-prepared setting file to the relay using a portable PC running the appropriate MiCOM S1 Agile software using the relay's front RS232 port, located under the bottom access cover, or rear communications port (with a KITZ protocol converter connected). This method is preferred for transferring function settings as it is much faster and there is less margin for error. If programmable scheme logic other than the default settings with which the relay is supplied are to be used then this is the only way of changing the settings.

If a setting file has been created for the particular application and provided on a diskette, this will further reduce the commissioning time and should always be the case where programmable scheme logic changes are to be applied to the relay.

- Enter them manually using the relay's operator interface. This method is not suitable for changing the programmable scheme logic.

5.2 Check Application-Specific Settings

The settings applied should be carefully checked against the required application-specific settings to ensure they have been entered correctly. However, this is not considered essential if a customer-prepared setting file has been transferred to the relay using a portable PC.

There are two methods of checking the settings:

- Extract the settings from the relay using a portable PC running the appropriate software via the front RS232 port, located under the bottom access cover, or rear communications port (with a KITZ protocol converter connected). Compare the settings transferred from the relay with the original written application-specific setting record. (For cases where the customer has only provided a printed copy of the required settings but a portable PC is available).
- Step through the settings using the relay's operator interface and compare them with the original application-specific setting record.

Unless previously agreed, the application-specific programmable scheme logic will not be checked as part of the commissioning tests.

Due to the versatility and possible complexity of the programmable scheme logic, it is beyond the scope of these commissioning instructions to detail suitable test procedures. Consequently, when programmable scheme logic tests must be performed, the Engineer who created the application-specific scheme logic should devise written tests that will satisfactorily demonstrate its correct operation. These should be provided to the Commissioning Engineer together with the diskette containing the programmable scheme logic settings file.

5.3 Demonstrate Correct Distance Function Operation

5.3.1 Functional Tests: Start control & Distance characteristic limits

Despite of working in 100% numerical technology some tests could be performed in order to check that the relay has the right characteristics; regarding the different choices for functions and settings (protection (with MiCOM S1 Agile / settings & records) and logic schemes (with MiCOM S1 Agile / PSL Editor) settings).

Subsection 5.3.2 explains point by point the steps to follow to perform a complete check of every distance protection functions of the relay (with the factory's settings & PSL: "P&C by default").

In the event of relay or application's failure:

WARNING: RETURN TO THE BASIC CONFIGURATION (SETTINGS & PSL) AND THEN VALIDATE THE TESTS FOLLOWING THE ENCLOSED DESCRIPTION (VIA THE LCD ON THE FRONT PANEL (CONFIGURATION/RESTORE DEFAULTS/ALL SETTINGS+VALIDATE))

The default password possibly required to confirm the settings is:

AAAA

Note: Every action performed using a laptop could also be performed using the LCD front panel (only PSL and Text Editor require a computer)

5.3.1.1 Measurements check:

Before starting the tests, perform the following injections on the secondary side of the relay:

		IA	0.2 In	0°
	Currents	IB	0.4 In	- 120°
TEST 1		IC	0.8 In	+ 120°
		VAN	30 V	0°
	Voltages	VBN	40 V	- 120°
		VCN	50 V	+ 120°

- Check the displayed values on the relay's front panel (LCD):"system/meas1"
- Secondary values in amplitude and phase
- Or primary values (control of ratios VT & CT) – If selected:

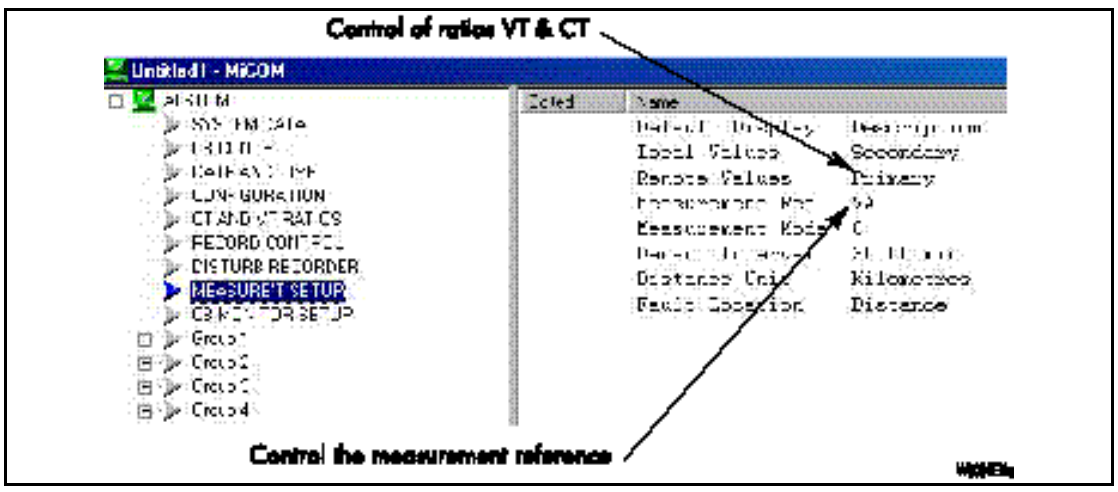


Figure 2:

Note 1:	*Check the measurement reference (ref. angle of phase shift) in: "Measurt set up/Measurement ref." (VA by default).*

Monitoring can also be selected to poll the network parameters (I/U/P/Q/f…)

Note 2:	*In LCD: IN=3I0* *After this step, the errors on the phase sequences, ratios of CT, VT and wiring (analogue input only) will be detected.*
Note 3:	*See connections drawing*
Note 4:	*See LCD structure in test tools*

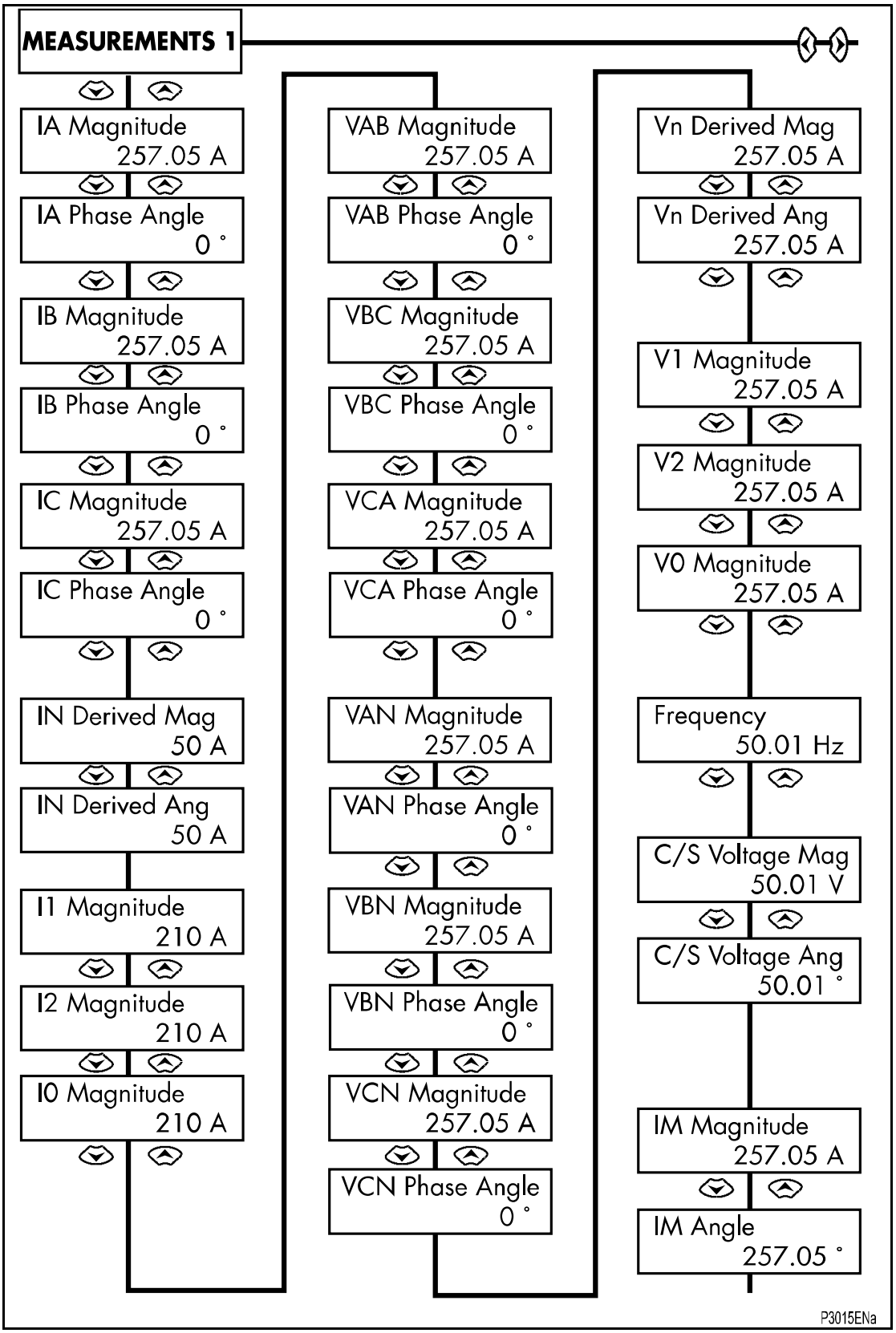


Figure 3: Measurement 1/LCD menu

Check the polarisation of the protection: inject a three-phase symmetrical load according to the following table:

TEST 2		IA	IN	20°
	Currents	IB	IN	-100°
		IC	IN	+140°
		VAN	57 V	0°
	Voltages	VBN	57 V	-120°
		VCN	57 V	+120°

- If one phase is missing the output Fuse Failure alarm will pick up & the LED general alarm on the front panel will light up (see Fuse Failure description in section P44x/EN AP)
- According to the chosen measurement mode, the following is obtained:

(MiCOM S1 Agile Measurement setup/Measurement mode):

Measurement mode	0	1	2	3
P	+	-	+	-
Q	-	-	+	+

Selected in MiCOM S1 Agile by:

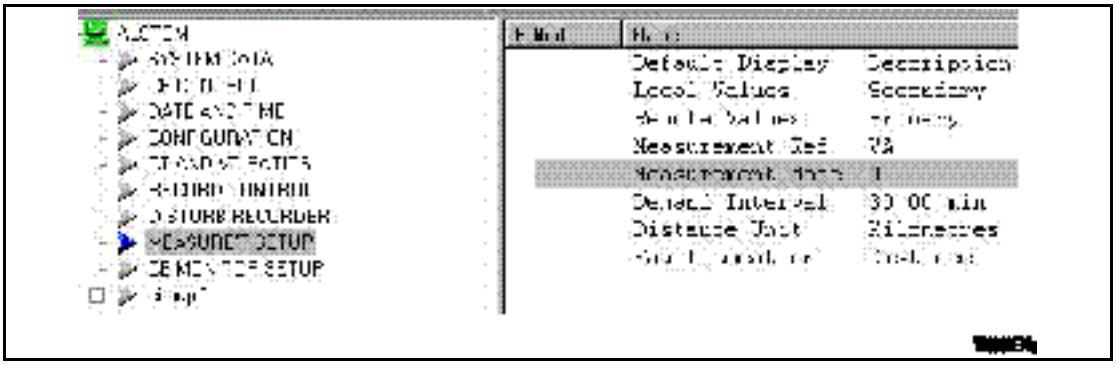


Figure 4:

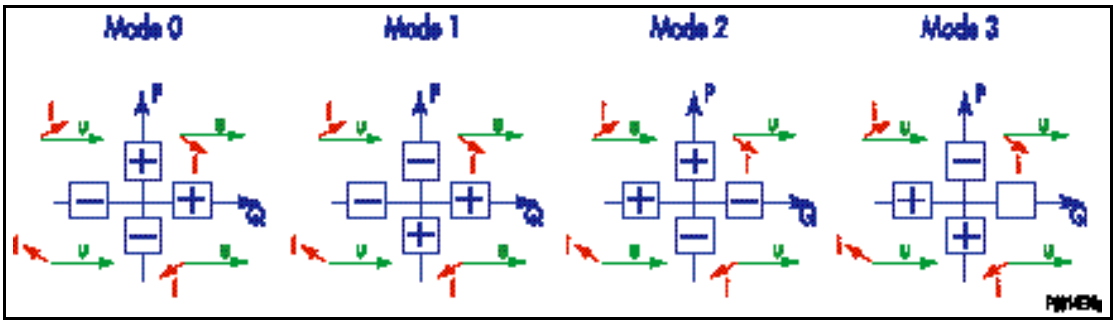


Figure 5:

- Check the signs of values P, Q to LCD ("Measurements 2") – settable with LCD (see Figure 4)

The primary side orientation remains to be achieved (repeat previously points with a primary injection)

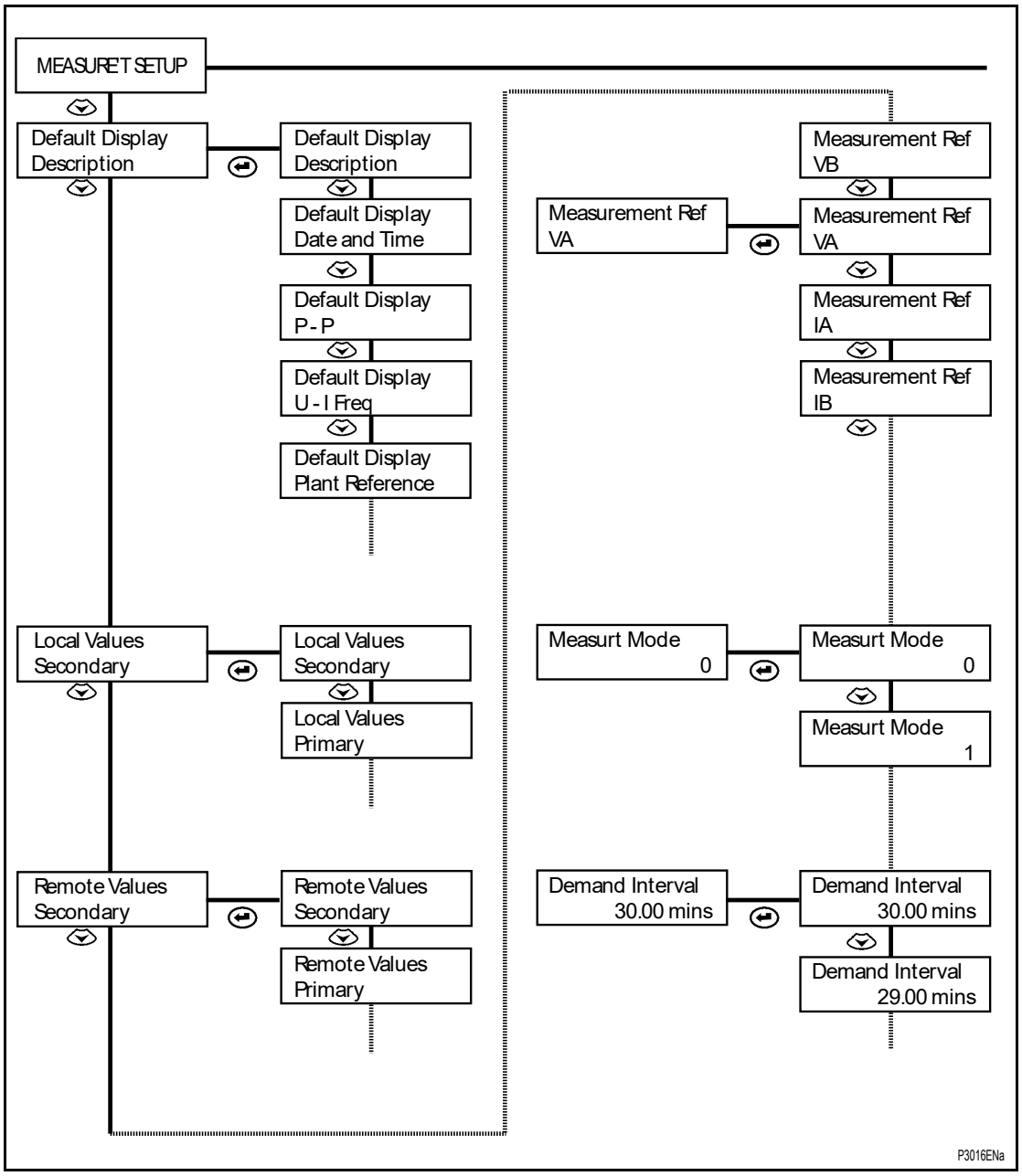


Figure 6: Measurement setup/LCD menu

5.3.1.2 Default simulation principle

To simulate a single-phase fault

The distance protection detects a single-phase default in E if the impedance and phase of this point place it inside the characteristic. The relation between the impedance and phase and the injected voltage and current is as follows:

- Fault Impedance Z = Vphase/Iphase;
- Fault Phase φ = phase-shift(Vphase, Iphase) ;
- The Vphase voltage has to remain lower than the rated voltage value

Impedance test for zone 1:

I1 = 1A

$\varphi 1$ = line angle = 76°

$\frac{V1}{I1}$ = Zfault = Zd (1 + k0) + Rfault

Rfault = R loop

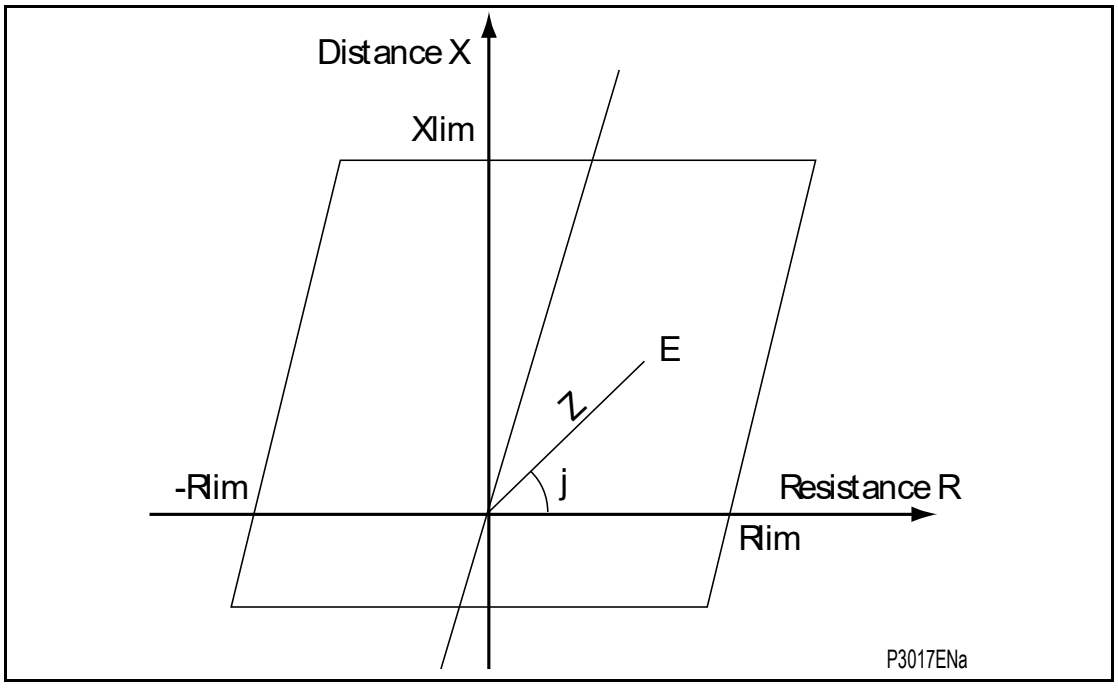


Figure 7: Characteristic point determination (Rlim two-phase & Single-phase can be different)

The characteristic angle is:

- For phase-to-phase: Argument of the positive impedance of the line (Z1)
- For phase-to-earth: Argument of 2Z1+Z0

The relay characteristic can be created and displayed with Z-Graph (MiCOM Z-Graph software is a tool delivered with the protection)

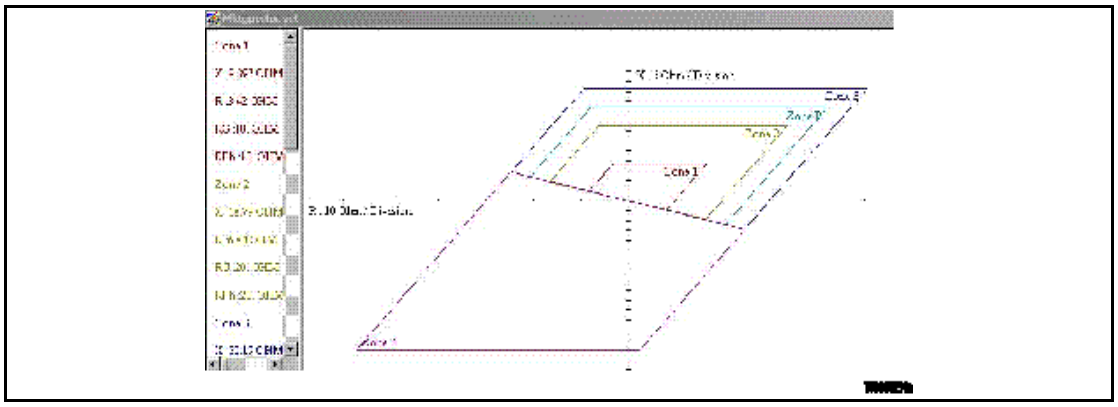


Figure 8: Example of Z-graph screen (Rio format can be created as well)

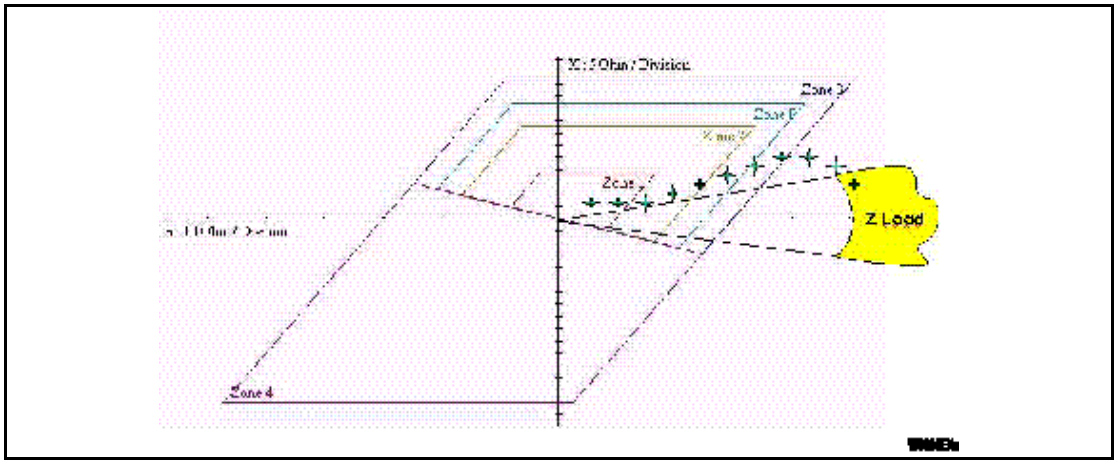


Figure 9: Evolving impedance from the load area to the final fault impedance in Zone1

To simulate a fault in a zone, it is necessary to vary the current progressively to move the point from the load area into the desired zone.

A single-phase starting characteristic with different values of K0 can be created:

(K0x = (Zx0 - Z1) /(3 Z1).

(In S1 there are up to four possibilities KZ1 & KZ2, KZp, KZ3/4)

This solution is carried out in case of an underground cable/overhead line section (KZ1 ≠ KZ2 = KZp = KZ3/4) where the Z01 & Z02 angles can be very different (HV Line at 80° and cable at 45°).

Nevertheless, the most common injection devices do not allow several values of K0 to be handled (the same for Z-Graph); therefore, for accurate control of zone limits, it will be necessary to generate several characteristic files (as many Rio files as KZ values.

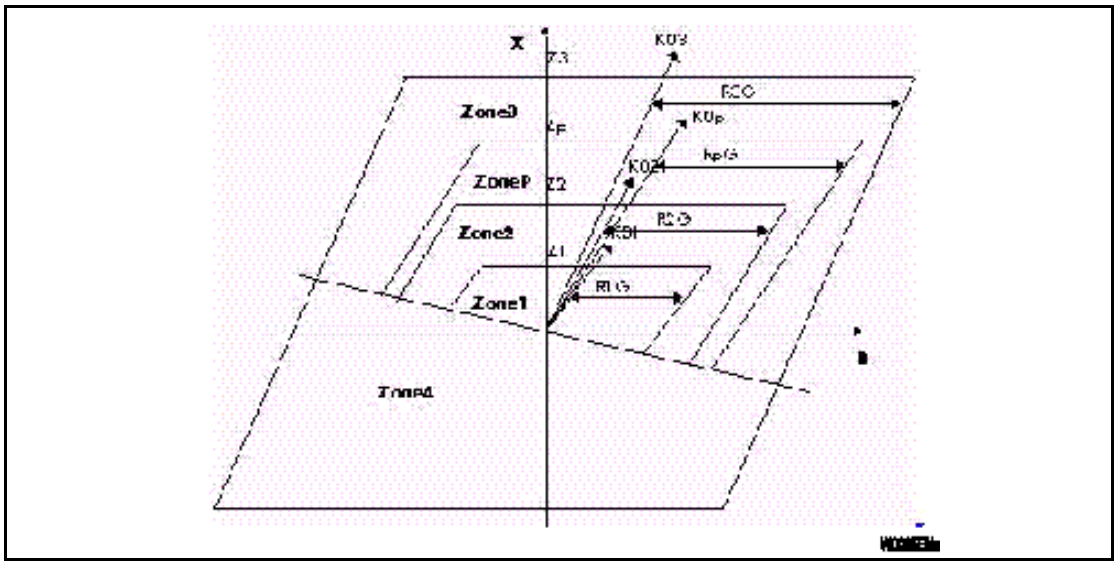


Figure 10: Single characteristic with P forward zone

Z1, Z2, Z3, Zp, Z4 : limits of zone 1, 2, 3, p, 4

R1G, R2G, R3G, RpG: resistance limits of zone 1, 2, 3, p, 4 for single-phase fault.

K01, K02, K03, K0p : residual compensation factor of zone 1, 2, 3, p

Zone 1, 2, 3 & P can have different resistance limits and residual factors. Zones 3 and 4 (start zone) have the same resistance sensitivity and residual compensation factor. The residual compensation factor depends of the line's characteristic in each zone.

Line angle: **Error! Bookmark not defined.**φpg = Arg $\frac{2xZ1+Z+0}{3}$ where Zx0 is the zero sequence impedance for zone x and Z1 is the positive impedance.

Zones coverage

Different line angles for each single-phase characteristic zone can be defined, and, depending on the configuration of each zone, some encroachment between zones could occur.

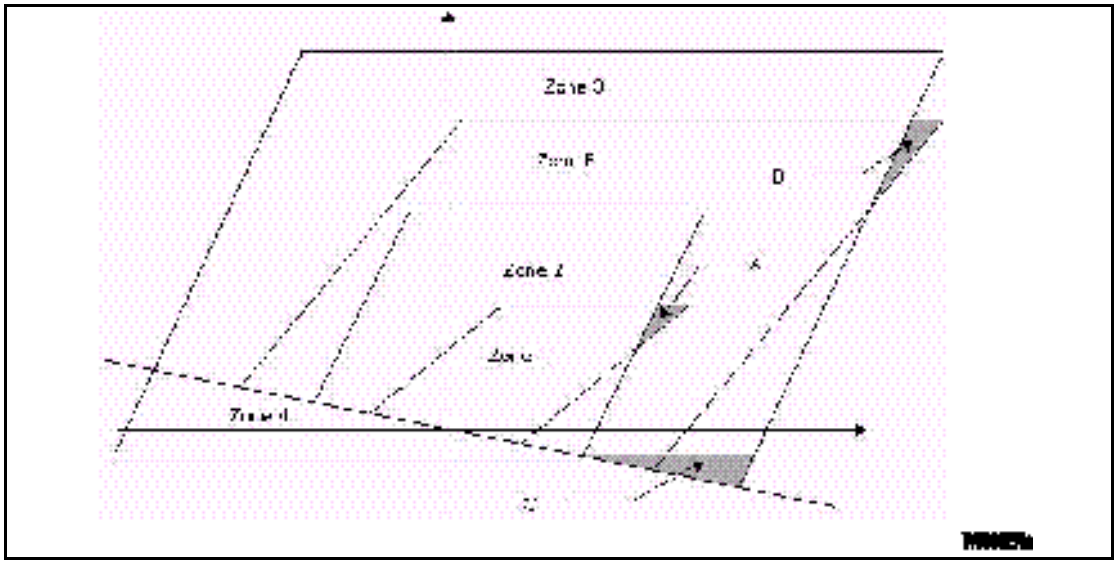


Figure 11:

In the characteristic above, the parts marked A, B and C are intersections between several zones.

- The surface A is considered as being in zone 1.
- The surface B is not a part of the characteristic (no start element).
- The surface C is not a part of the starting characteristic (up to version A4.0, a new logic is implemented to keep Z1 forward detection in area C (even with a fault negative reactance value higher than the reverse limit X4))

Plausibility:
For a characteristic to be plausible, its various parameters must comply with the following equations: (no blocking plausibility check is provided by the internal logic control of the relay)

- if zone P is set forward:
  - Z1 < Z1ext < Z2 < Zp < Z3
  - tZ1 < tZ2 < tZp < tZ3
  - R1G ≤ R2G ≤ RpG ≤ R3G
  - R1Ph ≤ R2Ph ≤ RpPh ≤ R3Ph
- if zone P is set reverse:
  - Z1 < Z1ext < Z2 < Z3
  - Zp < Z4
  - tZ1 < tZ2 < tZ3
  - tZp < tZ4
  - R1G ≤ R2G ≤ R3G
  - RpG ≤ R4G
  - R1Ph ≤ R2Ph ≤ R3Ph
  - RpPh ≤ R4Ph
- The Z minimum value measured by the relay is: 60 mohms (Z1min set in S1 is 1ohm with CT 1Amp & 200 mohms with CT 5Amp)
- There is no limit for the R/X ratio because a floating-point processor is used for the R calculation & X calculation (separated dynamic range for each calculation). In consequence the limit will be given by the angle error of the CT.

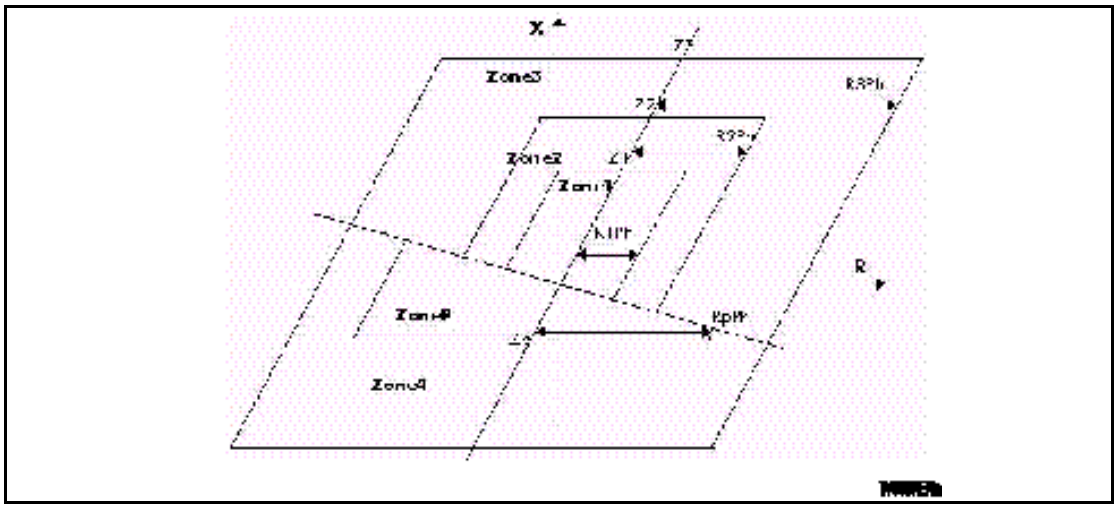
For example in PUR with CT accuracy angle at 1° (for IN), this gives a R/X = 5,7 – to keep a 10% error in the X1 measurement.

- R limit: min. 0 /max. 80 ohms (CT 5Amp) – min. 0/max. 400 ohms (CT 1Amp)
- X limit: min. 0,2/max. 100 ohms (CT 5Amp) – min.1/max. 500 ohms (CT 1Amp)

To simulate a two-phase fault
The two-phase fault simulation principle is the same as the one used to simulate a single-phase fault but:

- the voltage reference is the line to line voltage between phases, Uab for example;
- the reference current is the difference between the phase-currents, Ia - Ib for example;
  - the fault impedance Z = (Uphase-phase/(Iphase1 - Iphase2)).
  - the R1M point (single phase) is replaced by the R1ph point.(Biphase)

Two-phase characteristic with reverse zone P:



Fault simulation $\frac{U\alpha\beta}{I1}$ = 2 x Zd + Rfault

Where:

Uαβ : phase-to-phase fault voltage
I1 : fault current
φ1 : fault angle

Rfault = R loop

For a three-phase fault:

Fault simulation $\frac{V1}{I1} = Zd + \frac{Rfault}{2}$

Where:

V1 : phase-to-phase fault voltage
I1 : fault current
φ1 : fault angle

Note:	*Using the Z graph a Rio format characteristic can be created. This Rio file can be loaded onto a numerical injector that accepts this kind of files. The active settings (distance elements) can be modified by Z-graph and the relay can be upgraded with new distance parameters*

For more detail refer to section: Test tools: "Z graph user"

5.3.1.3 Check and test of the starting characteristics

In this part – tests are described with the default parameters

Open the MiCOM characteristics file If no changes have been made, the following values are obtained (Z-graph screen):

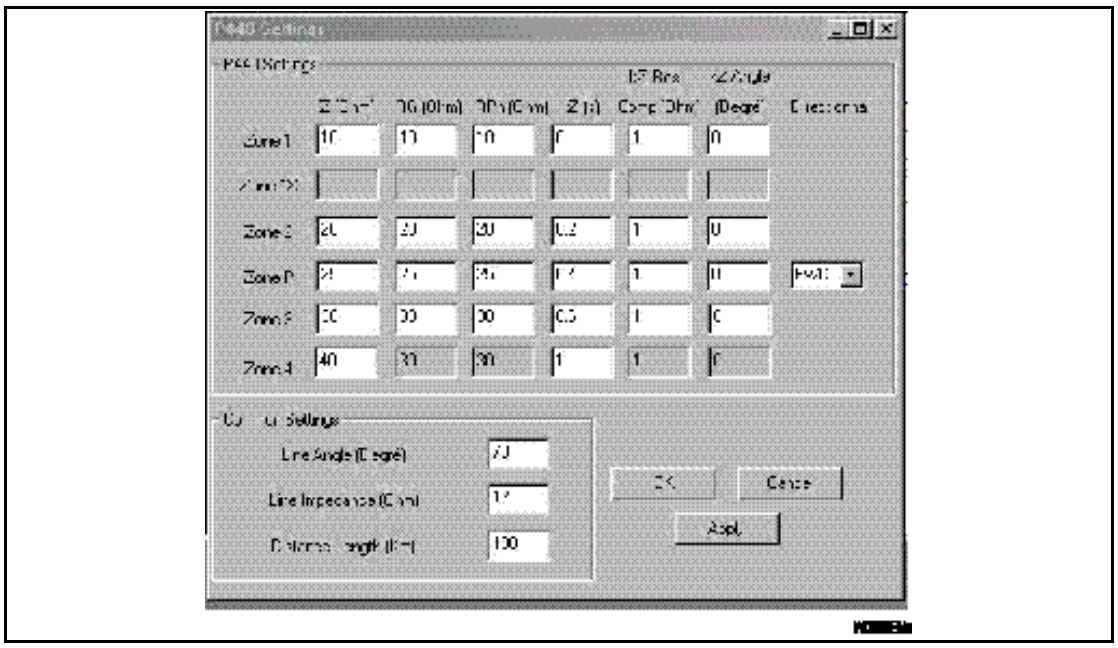


Figure 12:

Control of single-phase fault characteristic'

CAUTION: If different K0 are used – SEE SECTION 5.3.1.2

1. Energise MiCOM P44x with a healthy three-phase system (without any unbalanced condition) with a load (during a minimum time of 500 ms). This is to:
   - Enable the use of the Delta algorithms
   - Avoid the start of the SOTF logic
2. Reduce the current value to obtain a relation between V and I following the appended table (for Rlim – phase-shift at 0°, for Z limit – phase-shift corresponding to Z1 (in multiphase default) or corresponding to 2Z1+Z0 (in single fault).
3. Check that the tripping order (DDB: Any trip / Any Trip A/ Any Trip B/ Any Trip C – see DDB description) is transmitted when the concerned zone time-delay expires (for a distance scheme with transmission and all distance trip logic see the Application Notes chapter.

Note: The DDB signal any Trip A is an OR gate between
Ext Trip A
Int Trip A

4. See also the test report model (end of this section).
5. Check also in the PSL (programmable scheme logic) the trip command addresses (any Trip is linked by default to the relay 7).

By default: see the wiring diagram (for assignment of inputs/outputs).

Useful tip: - To check the logic level of internal datas (DDB cells), all or some of the 8 red LEDs on the front panel could be assigned using the PSL.

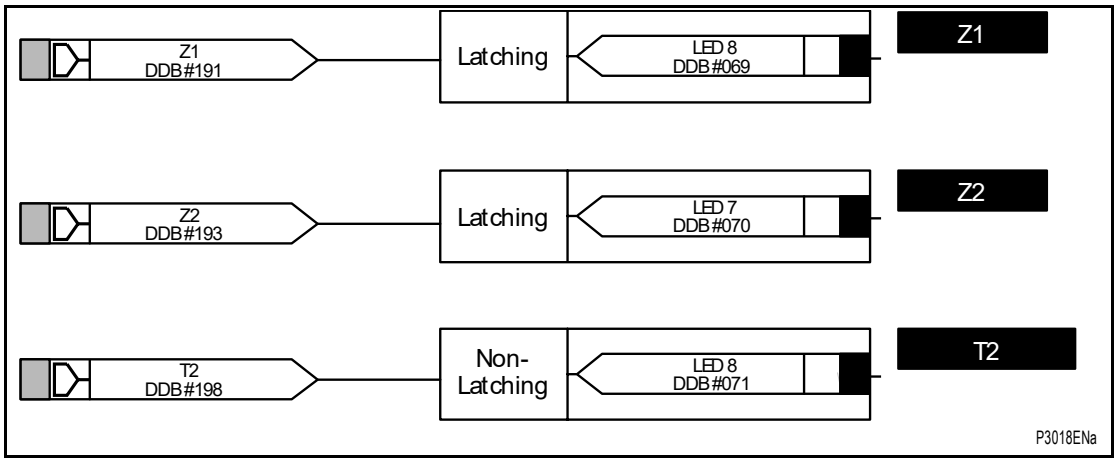


Figure 13:

If the LEDs are latched, the reset latch could be enabled by a dedicated PSL, to avoid needless keypad access during the tests:

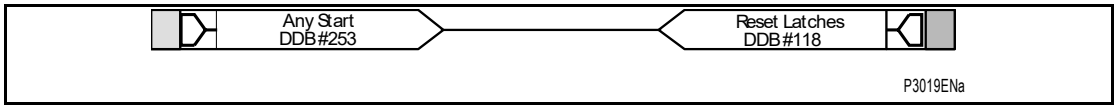


Figure 14:

Useful tip: - To check the logic level of internal data (DDB cells), monitor bit control can be used in "commissioning Test / Opto / Relay / Test port status / Led status / Monitor bit 1 to bit 8". Any cells of the DDB can be assigned and then displayed as 1 of the 8 bits (see User Tools).

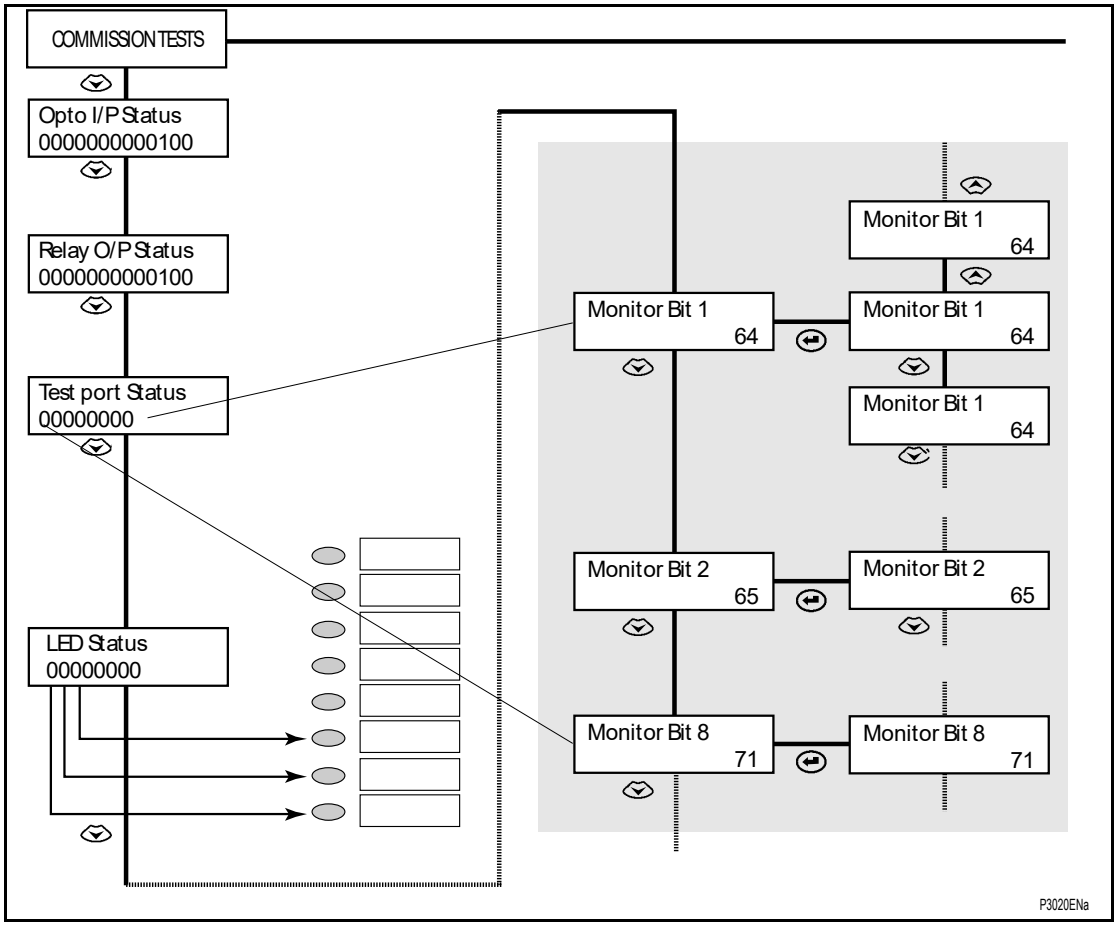
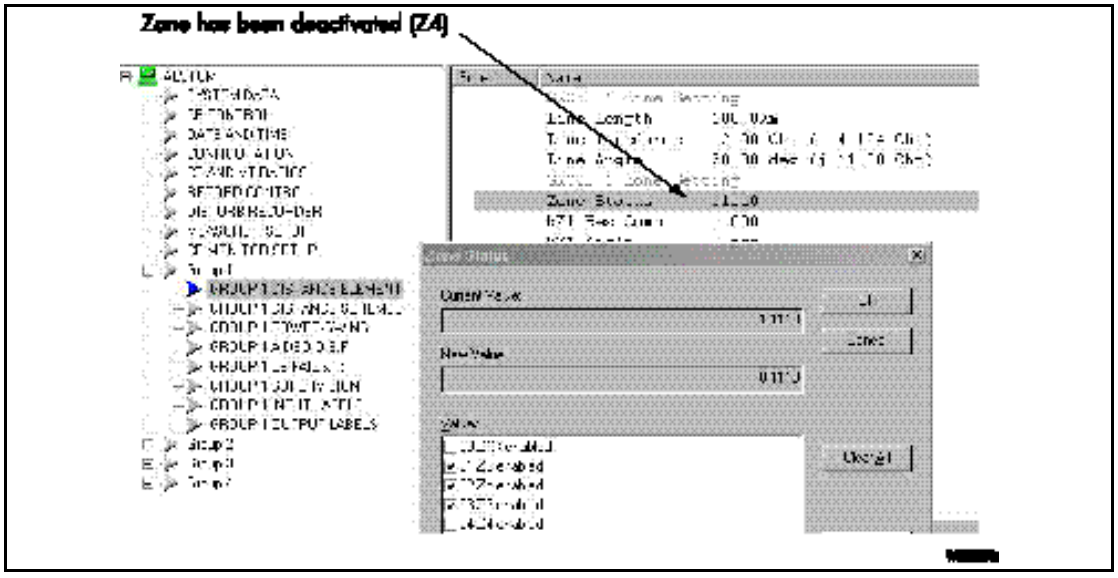


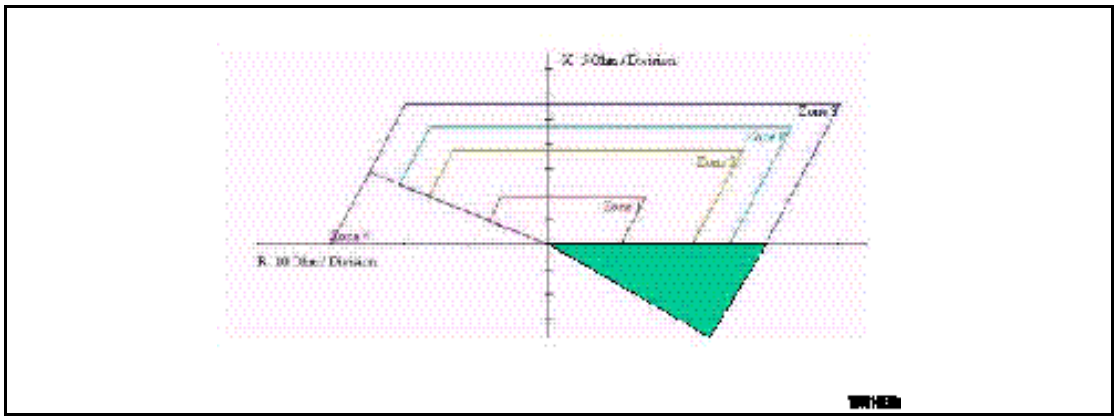
Figure 15: LCD menu for a control of an input/output / monitor bits check

Test point B:Bi M:mono	I,V phase shift (I is behind V)	Tripping time
R1 B	0°	T1
R1 M	0°	T1
R2 B	0°	T2
R2 M	0°	T2
Rp B	0°	Tp
Rp M	0°	Tp
R3 B	0°	T3
R3 M	0°	T3
- R Lim = -R3	0°	T4
Z1 B	Arg Zd	T1
Z1 M	Arg (2Zd+Z0)	T1
Z2 B	Arg Zd	T2
Z2 M	Arg (2Zd+Z0)	T2
Zp B	Arg Zd	Tp
Zp M	Arg (2Zd+Z0)	Tp
Z3 B	Arg Zd	T3
Z3 M	Arg (2Zd+Z0)	T3
Z4 B	Arg Zd	T4

Table 12 - Parameters of zone to test (Zp can be reverse or forward / each zone is enabled or disabled – Z is always enabled)

Note: R3 represents the starting limit on the R axis (detection sensitivity of resistive defaults – The starting element for phase/earth can be superior to the phase/phase). If the reverse zone has been disabled (Z4), there is still a no-trip zone (up to version A3.2 & 2.10) in the 4th quadrant below the R axis.





If Z3 is disabled, the resistance limits R3-R4 are no longer visible in MiCOM S1 Agile.

Note:	*All other characteristic points can be tested after calculating the impedance and the phase shift between U and I.* *All these examples use the default settings.*

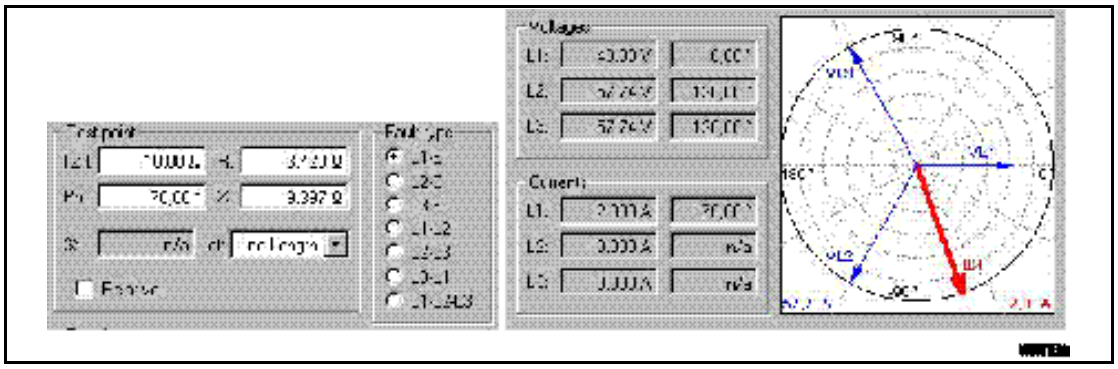


Figure 16: Example: AN - lim Z1

VAN/IA = Zf =Z1(1+K01) 40V/2A (phase shift of –70°) =20 Ω = Z1(1+1)

Lim Z1=10 Ω (if KO1=1)

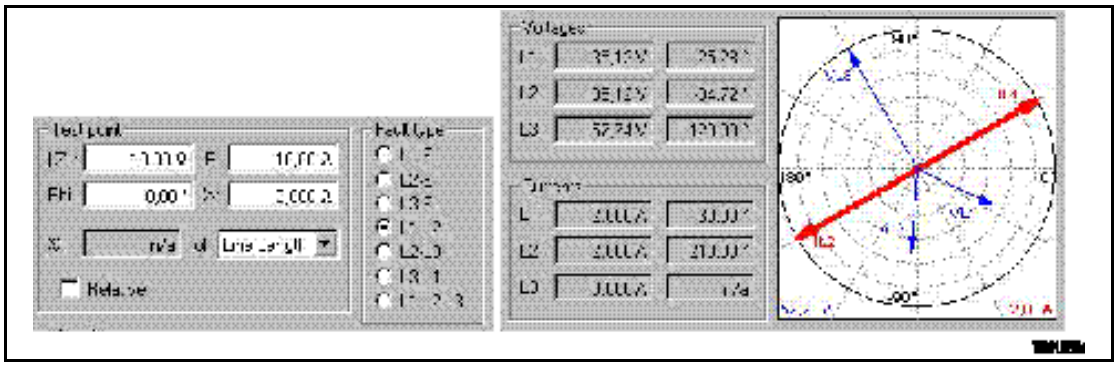


Figure 17: Example: AB - limR2

VAB = 2 sin 34,72° * 35,12=40 V / IAB=2A

UAB/IA (in phase) =Rf=20 Ω=LimR2
LimR2 (R2 value in MiCOM S1 Agile in ohms loop).

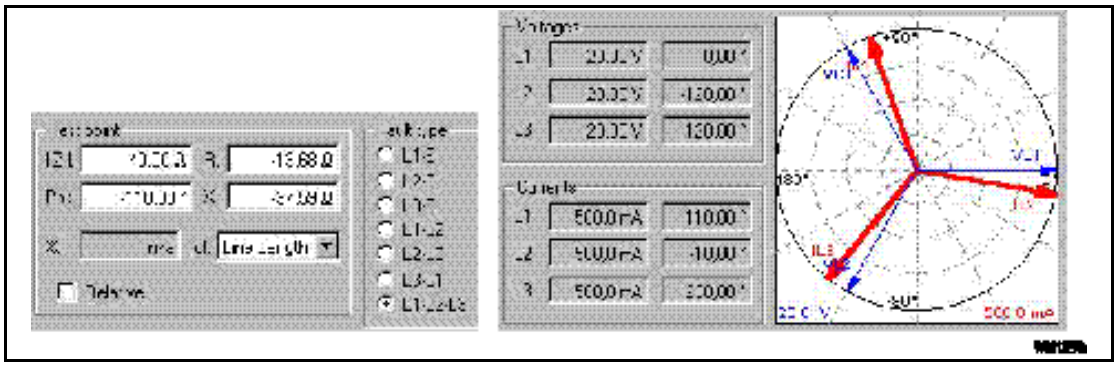


Figure 18: Example: ABC-limZ4 (Reverse)

VAN/IAN = Zf=Rf=20 V/0,500 mA=40 Ω=Lim Z4 with angle(VAN/IAN)=70°-180°=-110°

Note: Simulator use can generate transients greater than 0.2 In on currents where the generation of a fault condition can induce errors about the directional calculation with "Delta" algorithms. This error is due to the simulator boxes which do not always reflect the real conditions of fault occurrence during the transient condition. To avoid this problem during the starting zones check, we recommend inhibiting the "Delta" algorithms in the characteristics path by setting T1 to 50 ms (beyond 40 ms, algorithms "Delta" are no longer valid). It is the case for numerical injection boxes.

Check in the injection device, whether any possibility of DC component could be chosen to force the start of the faulty current at 0 (If not, the model network could be unrealistic)

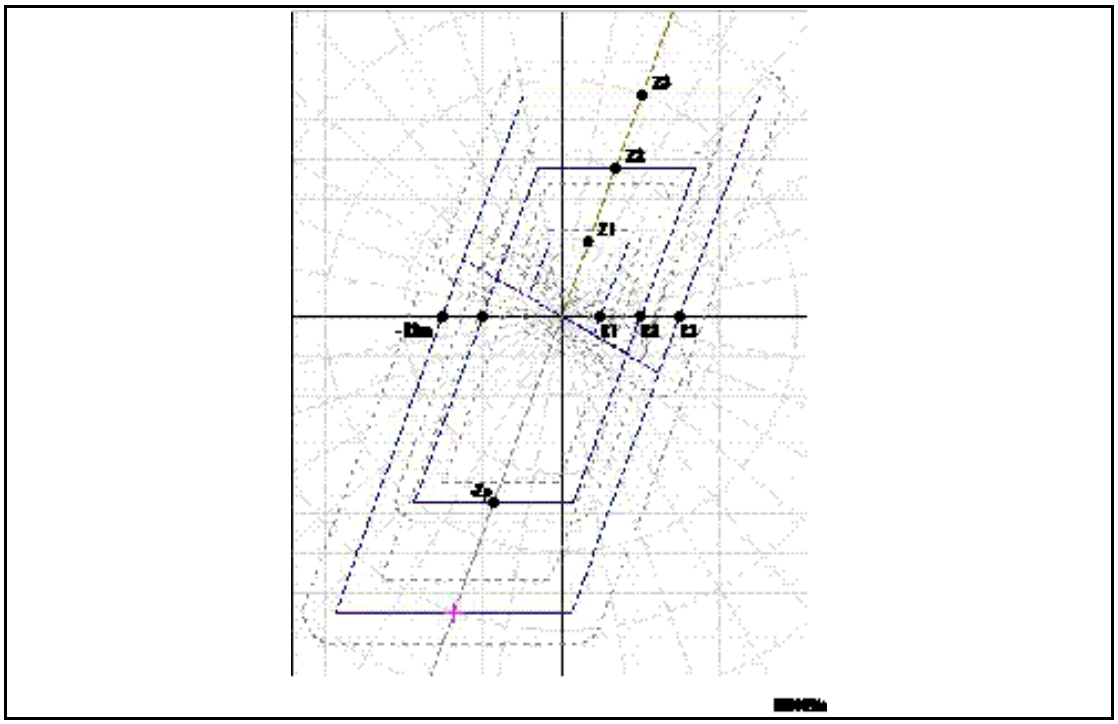


Figure 19: Points limit of the characteristic to be tested (with Zp selected as a reverse zone)

5.3.2 Distance scheme test (if activated in MiCOM S1 Agile)

5.3.2.1 Control

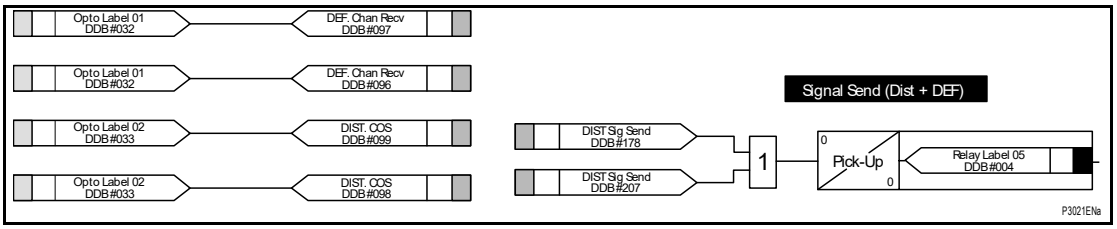
- The type of distance scheme enabled in MiCOM S1 Agile
- The DDB cells assigned for the distance scheme
- Ref to the description feature in P44x/EN AP section “Distance protection schemes”:
  - Settings in S1
  - DDB cells
  - Internal logic in A2.10 & A3.2

REMINDER: General equation to the tripping in distance protection since A2.9/A3.1 – From A2.10/A3.2 it can be found in the Chap EN AP – section 2.5

Note: Before testing, check the input presence / Output in PSL linked to the selected channel-aided scheme (DDB: DistCR/Dist CS). Also check the I/O condition change (on LCD in FAV in "system")

Input:(PSL by default "P&C ") Output: (PSL by default "P&C ")

WARNING: WHEN SWITCHING GROUPS VIA THE OPTO COUPLERS: OPTOS 1 AND 2 MUST NOT BE ASSIGNED IN THE PSL.



1. Select a mode.
2. Implement the fault indicated in the panel first column, the carrier signal input is enabled (with carrier receive).
3. Check that the trip contact have been energised at the end of the time-delay indicated in the same column (With carrier receive).
4. Repeat step 2 and 3 but without the carrier receive input and checking the indicated time-delay in the panel’s 2nd column (without carrier receive).

Repeat step 2 and 4 for the other faulted zones by checking that whatever the carrier receive input state, the time-delays associated with every zone are not modified (according to the 4th column equations)

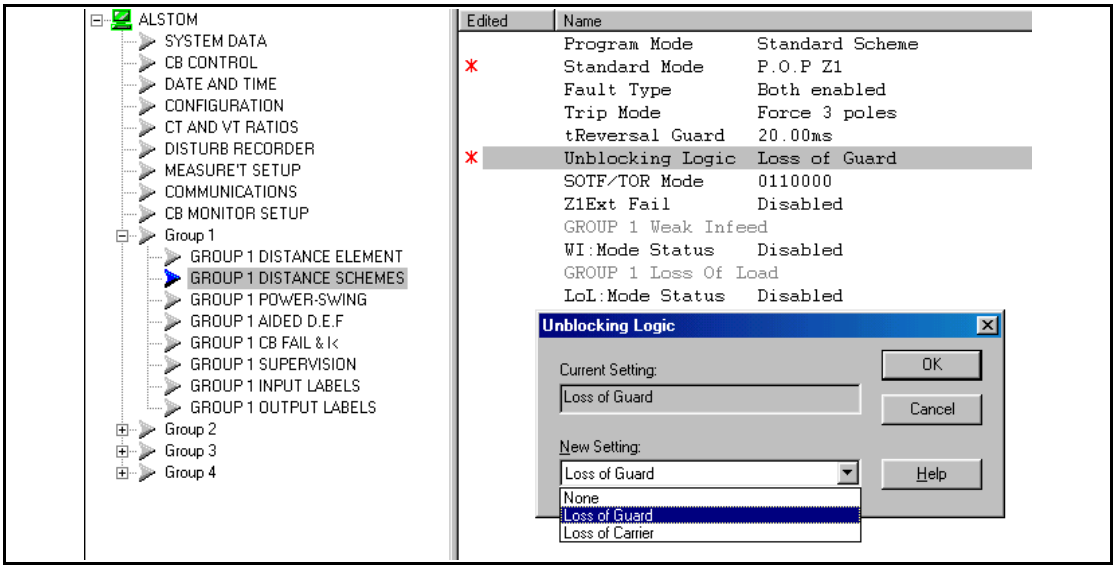
Note: Channel-aided schemes can be simulated by inverting the optos

Channel-aided schemes transmissions can also be checked by generating defaults according to the 3rd column.

To simplify the relay I/O control condition, the assignments of LEDs in the PSL can be modified. It is also possible in MiCOM S1 Agile

5.3.3 Loss of guard/loss of carrier test

Setting:



TEST: Follow the truth table (section P44x/EN AP)

Note:	*In case of channel-aided loss, the scheme Z1X (out fail) will be applied if selected in MiCOM S1 Agile*

5.3.4 Weak infeed mode test

From MiCOM S1 Agile
(If Permissive schemes are enabled in MiCOM S1 Agile: 4 possible choices):fig winf1

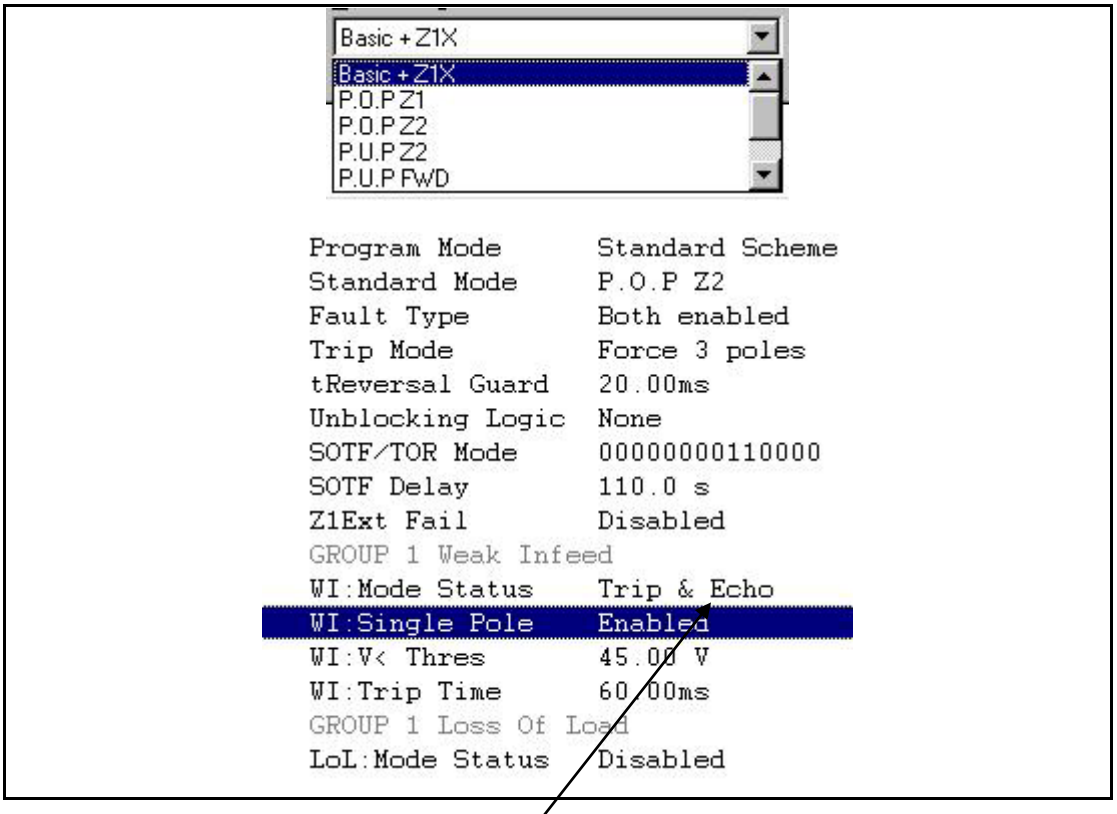


Figure 20: Winf2

Put into service the weak infeed mode (single-pole possible);

1. Inhibit tripping authorisation and phase selection.
2. Enable the carrier receive input.
3. Check that:
   - the channel-aided scheme transmission signal is enabled;
   - the trip contact is not enabled.

From MiCOM S1 Agile enable the three-phase authorization.

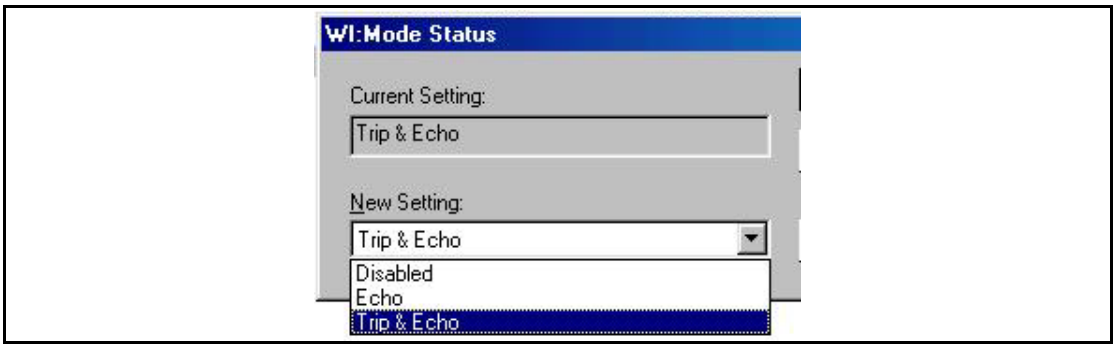


Figure 21:

4. Enable the carrier receive input.
5. Check that:
   - the channel-aided scheme signal is enabled ;
   - the trip contacts closing.

From MiCOM S1 Agile, enable the minimum voltage phase selection, set undervoltage threshold to 0.4 Vn, make VB = –VC = Vn, enable the single-phase tripping authorisation.

6. Enable the carrier receive input.
7. Check that:
   - the channel-aided scheme transmission signal is enabled;
   - the protection trips phase A.

5.3.5 Protection operation during fuse failure

See internal logic description in P44x/EN AP – “Voltage Transformer Supervision” section.

Relay blocking (loss of 1 or 2 phases)

1. Supply MiCOM P44x with a "healthy" system with load:
2. Remove the phase A supply.((V0) & (/I0) creation)
3. Check that:
   - the fuse failure signal is activated at the end of the signal time-delay sign;
   - the protection start and trip signal are not activated.

Relay unblocking

1. Keep the phase A supply cut-off and generate a fault (1- or 3-phase) which fault current (IR>3I0) is higher than the set threshold (I2 or I0).
2. Check that the trip contact is activated.

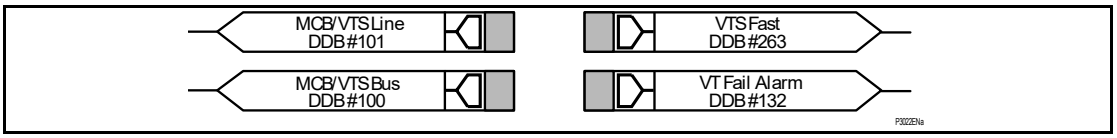
Relay locking (3 phases loss)

1. Repeat step 1 and then open the 3 voltage channels without creating a delta I. Check as in step 3

Outside sign:

1. Polarise the input: and check that the outputs change state:

Signal repercussions:
The signal (VT fail alarm) drops off if:



Fuse_Failure = 0

and

INP_FFUS_Line = 0

and

(All Poles Dead Or healthy system)

All Poles Dead:
No current AND no voltage on the line or open circuit-breaker

Healthy system:
Rated voltage on the line AND

- No zero sequence voltage and current AND
- No starting AND
- No power swing.

5.4 Demonstrate Correct Overcurrent Function Operation

This test, performed in stage 1 of the overcurrent protection function in setting group 1, demonstrates that the relay is operating correctly at the application-specific settings.

It is not considered necessary to check the boundaries of operation where cell [3502: GROUP 1 OVERCURRENT, I>1 Direction] is set to 'Directional Fwd' or 'Directional Rev' as the test detailed test already confirms the correct functionality between current and voltage inputs, processor and outputs and earlier checks confirmed that the measurement accuracy lies within the stated tolerance.

5.4.1 Connect the test circuit

Determine which output relay has been selected to operate when an I>1 trip occurs by viewing the relay's programmable scheme logic.

The programmable scheme logic can only be changed using the appropriate software. If this software has not been available then the default output relay allocations will still be applicable.

If the trip outputs are phase-segregated (i.e. a different output relay allocated for each phase), the relay assigned for tripping on 'A' phase faults should be used.

If stage 1 is not mapped directly to an output relay in the programmable scheme logic, output relay 3 should be used for the test as it operates for any trip condition.

The associated terminal numbers can be found either in the external connection diagram (P44x/EN IN) or in Table 5.

Connect the output relay so that its operation will trip the test set and stop the timer.



Connect the current output of the test set to the 'A' phase current transformer input of the relay (terminals C3 and C2 where 1A current transformers are being used and terminals C1 and C2 for 5A current transformers).

If [3502: GROUP 1 OVERCURRENT, I>1 Direction] is set to 'Directional Fwd', the current should flow out of terminal C2 but into C2 if set to 'Directional Rev'.

If cell [351D: GROUP 1 OVERCURRENT, VCO Status] is set to 'Enabled' (overcurrent function configured for voltage controlled overcurrent operation) or [3502: GROUP 1 OVERCURRENT, I>1 Direction] has been set to 'Directional Fwd' or 'Directional Rev' then rated voltage should be applied to terminals C19 and C22.

Ensure that the timer will start when the current is applied to the relay.

> *Note: If the timer does not start when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the set direction of operation set. Try again with the current connections reversed.*

5.4.2 Perform the test

Ensure that the timer is reset.

Apply a current of twice the setting in cell [3504: GROUP 1 OVERCURRENT, I>1 Current Set] to the relay and note the time displayed when the timer stops.

5.4.3 Check the operating time

Check that the operating time recorded by the timer is within the range shown in Table 13.

> *Note: Except for the definite time characteristic, the operating times given in Table 13 are for a time multiplier or time dial setting of 1. Therefore, to obtain the operating time at other time multiplier or time dial settings, the time given in Table 13 must be multiplied by the setting of cell [3507: GROUP 1 OVERCURRENT, I>1 TMS] for IEC and UK characteristics or cell [3508: GROUP 1 OVERCURRENT, Time Dial] for IEEE and US characteristics.*
>
> *In addition, for definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively that may need to be added to the relay's acceptable range of operating times.*
>
> *For all characteristics, allowance must be made for the accuracy of the test equipment being used.*

Characteristic	**Operating Time at twice current setting and time multiplier/time dial setting of 1.0**	
	Nominal (Seconds)	Range (Seconds)
DT	[3505: I>1 Time-delay] setting	Setting ±2%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	24.67 - 28.67
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	0.64	0.61 - 0.67
IEEE V Inverse	1.42	1.35 - 1.50
IEEE E Inverse	1.46	1.39 - 1.54
US Inverse	0.46	0.44 - 0.49

Table 13 - Characteristic Operating Times for I>1

5.5 Check Trip and Auto-reclose Cycle

If the autoreclose function is being used, the circuit breaker trip and autoreclose cycle can be tested automatically at the application-specific settings.

To test the first autoreclose cycle, set cell [0F13: COMMISSIONING TESTS, Autoreclose Test] to "3 Pole Test". The relay will perform a trip/reclose cycle. Repeat this operation to test the subsequent autoreclose cycles.

Check that all output relays used for circuit breaker tripping and closing, blocking other devices, etc. operate at the correct times during the trip/close cycle.

6 ON-LOAD CHECKS

Remove all test leads and temporary shorting leads, and replace any external wiring that has been removed to allow testing.

If it has been necessary to disconnect any of the external wiring from the relay in order to perform any of the foregoing tests, it should be ensured that all connections are replaced in accordance with the relevant external connection or scheme diagram.

The following on-load measuring checks ensure the external wiring to the current and voltage inputs is correct but can only be carried out if there are no restrictions preventing the energisation of the plant being protected.

6.1 Voltage Connections

Using a multimeter measure the voltage transformer secondary voltages to ensure they are correctly rated. Check that the system phase rotation is correct using a phase rotation meter.

Compare the values of the secondary phase voltages with the relay's measured values, which can be found in the MEASUREMENTS 1 menu column.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Secondary', the values displayed on the relay should be equal to the applied secondary voltage. The relay values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Primary', the values displayed on the relay should be equal to the applied secondary voltage multiplied by the corresponding voltage transformer ratio set in the 'VT & CT RATIOS' menu column (see Table 14). Again the relay values should be within 1% of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

Voltage	Cell in MEASUREMENTS 1 column (02)	Corresponding VT Ratio (in 'VT and CT RATIO column (0A) of menu)
VAB	[0214: VAB Magnitude]	$\frac{\text{0A07:Phase CT Primary}}{\text{0A08:Phase CT Sec'y}}$
VBC	[0216: VBC Magnitude]	
VCA	[0218: VCA Magnitude]	
VAN	[021A: VAN Magnitude]	
VBN	[021C: VBN Magnitude]	
VCN	[021E: VCN Magnitude]	
VCHECKSYNC	[022B: C/S Voltage Mag]	$\frac{\text{0A03:C/SVT Primary}}{\text{0A04:C/SVT Sec'y}}$
VN measured	[0222: VN Mag]	$\frac{\text{0A03:C/SVT Primary}}{\text{0A04:C/SVT Sec'y}}$

Table 14 - Measured Voltages and VT Ratio Settings

6.2 Current Connections



Measure the current transformer secondary values for each using a multimeter connected in series with the corresponding relay current input.

Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of the power flow by contacting the system control centre.

Ensure that the current flowing in the neutral circuit of the current transformers is negligible.

Compare the values of the secondary phase currents and phase angle with the relay's measured values, which can be found in the MEASUREMENTS 1 menu column.

> *Note: Under normal load conditions the earth fault function will measure little, if any, current. It is therefore necessary to simulate a phase to neutral fault. This can be achieved by temporarily disconnecting one or two of the line current transformer connections to the relay and shorting the terminals of these current transformer secondary windings.*

If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Secondary', the currents displayed on the relay should be equal to the applied secondary current. The relay values should be within 1% of the applied secondary currents. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: MEASURE'T SETUP, Local Values] is set to 'Secondary', the currents displayed on the relay should be equal to the applied secondary current multiplied by the corresponding current transformer ratio set in the 'VT & CT RATIOS' menu column. Again the relay values should be within 1% of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

7 FINAL CHECKS



The tests are now complete.

Remove all test or temporary shorting leads, etc. If it has been necessary to disconnect any of the external wiring from the relay in order to perform the wiring verification tests, it should be ensured that all connections are replaced in accordance with the relevant external connection or scheme diagram.

Ensure that the relay has been restored to service by checking that cell [0F0E: COMMISSIONING TESTS, Test Mode] is set to 'Disabled'.

If the relay is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using cell [0608: CB CONDITION, Reset All Values]. If the required access level is not active, the relay will prompt for a password to be entered so that the setting change can be made.

If an MMLG test block is installed, remove the MMLB01 test plug and replace the MMLG cover so that the protection is put into service.

Ensure that all event records, fault records, disturbance records, alarms and LEDs have been reset before leaving the relay.

If applicable, replace the secondary front cover on the relay.

MAINTENANCE

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1 MAINTENANCE

1.1 Maintenance Period

It is recommended that products supplied by GE Vernova receive regular monitoring after installation. As with all products some deterioration with time is inevitable. In view of the critical nature of protective relays and their infrequent operation, it is desirable to confirm that they are operating correctly at regular intervals.

GE Vernova protective relays are designed for a life in excess of 20 years.

MiCOM P44x distance relays are self-supervising and so require less maintenance than earlier relay designs. Most problems will result in an alarm so that remedial action can be taken. However, some periodic tests should be done to ensure that the relay is functioning correctly and the external wiring is intact.

If a Preventative Maintenance Policy exists within the customer's organisation then the recommended product checks should be included in the regular program. Maintenance periods will depend on many factors, such as:

- the operating environment
- the accessibility of the site
- the amount of available manpower
- the importance of the installation in the power system
- the consequences of a failure

1.2 Maintenance Checks

Although some functionality checks can be performed from a remote location by utilising the communications capability of the relays, these are predominantly restricted to checking that the relay is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. Therefore it is recommended that maintenance checks be performed locally (i.e. at the substation itself).



Before carrying out any work on the equipment, the user should be familiar with the Safety and Installation chapters of this manual.

1.2.1 Alarms

The alarm status LED should first be checked to identify if any alarm conditions exist. If so, press the read key 1 repeatedly to stop the alarms. Clear the alarms to extinguish the LED.

1.2.2 Opto-isolators

The opto-isolated inputs can be checked to ensure that the relay responds to their energisation by repeating the commissioning test detailed in Section P44x/EN CM.

1.2.3 Output Relays

The output relays can be checked to ensure that they operate by repeating the commissioning test detailed in P44x/EN CM.

1.2.4 Measurement accuracy

If the power system is energised, the values measured by the relay can be compared with known system values to check that they are in the approximate range that is expected. If they are, then the analogue/digital conversion and calculations are being performed correctly by the relay.

Alternatively, the values measured by the relay can be checked against known values injected into the relay via the test block, if fitted, or injected directly into the relay terminals. These tests will prove the calibration accuracy is being maintained.

1.3 Method of Repair

If the relay should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. Due to the extensive use of surface-mount components faulty PCBs must be replaced as it is not possible to perform repairs on damaged circuits. Therefore either the complete relay or just the faulty PCB, identified by the in-built diagnostic software, can be replaced. Advice about identifying the faulty PCB can be found in the Troubleshooting chapter.

The preferred method is to replace the complete relay as it ensures that the internal circuitry is protected against electrostatic discharge and physical damage at all times and overcomes the possibility of incompatibility between replacement PCBs. However, it may be difficult to remove an installed relay due to limited access in the back of the cubicle and scheme wiring rigidity.

Replacing PCBs can reduce transport costs but requires clean, dry conditions on site and higher skills from the person performing the repair. However, if the repair is not performed by an approved service centre, the warranty will be invalidated.

Before carrying out any work on the equipment, the user should be familiar with the Safety and Installation chapters of this manual. This should ensure that no damage is caused by incorrect handling of the electronic components.

1.3.1 Replacing the Complete Relay

The case and rear terminal blocks have been designed to facilitate removal of the complete relay should replacement or repair become necessary without having to disconnect the scheme wiring.

Before working at the rear of the relay, isolate all voltage and current supplies to the relay.

Note: The MiCOM range of relays have integral current transformer shorting switches that will close when the heavy duty terminal block is removed.

Disconnect the relay earth, IRIG-B (Central unit only) and fibre optic connections, as appropriate, from the rear of the relay.

Two types of terminal block used on the relay, medium and heavy duty. They are fastened to the rear panel using crosshead screws.

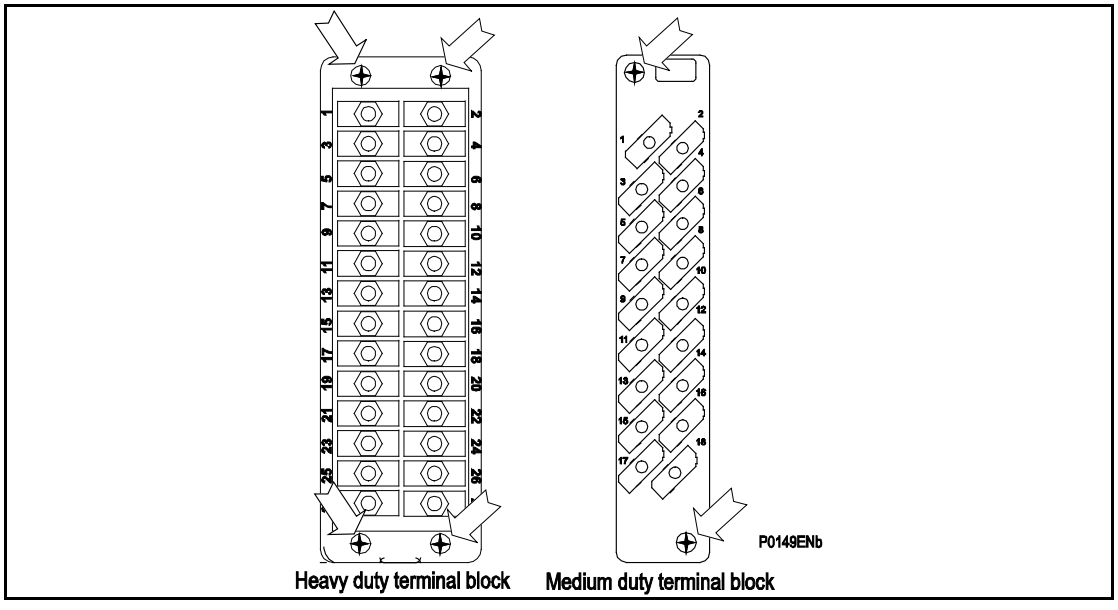


Figure 1: Location of securing screws for terminal block

Note: The use of a magnetic-bladed screwdriver is recommended to minimise the risk of the screws being left in the terminal block or lost.

Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.

Remove the screws used to fasten the relay to the panel, rack, etc. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.



If the top and bottom access covers have been removed, do not remove the screws with the smaller diameter heads that are accessible. These screws hold the front panel on the relay.

Withdraw the relay from the panel, rack, etc. carefully because it is heavy due to the internal transformers.

To reinstall the repaired or replacement relay follow the above instructions in reverse, ensuring that each terminal block is returned to its in the correct position and the case earth, IRIG-B and fibre optic connections are replaced.

Once reinstallation is complete the relay should be recommissioned using the instructions in sections 1 to 7 (inclusive) of this chapter.

1.3.2 Replacing a PCB

If the relay fails to operate correctly refer to section P44x/EN TS, 'Troubleshooting', to help determine which PCB is faulty.

To replace any of the relay's PCBs it is necessary to first remove the front panel.



Before removing the front panel to replace a PCB the auxiliary supply must be removed. It is also strongly recommended that the voltage and current transformer connections and trip circuit be isolated.

Open the top and bottom access covers. With size 60TE cases the access covers have two hinge-assistance T-pieces that clear the front panel moulding when the access covers are opened by more than 90°, therefore allowing their removal.

If fitted, remove the transparent secondary front cover. A description of how to do this is given in the Introduction chapter.

By slightly bending the access covers at one end, the end pivot can be removed from its socket and the access cover removed to give access to the screws that fasten the front panel to the case.

The size 40TE case has four crosshead screws fastening the front panel to the case, one in each corner, in recessed holes. The size 60TE case has two additional screws, one midway along each of the top and bottom edges of the front plate. Undo and remove the screws.



Do not remove the screws with the larger diameter heads that are accessible when the access covers are fitted and open. These screws hold the relay in its mounting (panel or cubicle).

When the screws have been removed, the complete front panel can be pulled forward and separated from the metal case. Caution should be observed at this stage because the front panel is connected to the rest of the relay circuitry by a 64-way ribbon cable.

Additionally, from here on, the internal circuitry of the relay is exposed and not protected against electrostatic discharges, dust ingress, etc. Therefore ESD precautions and clean working conditions should be maintained at all times.

The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable itself and a plug with locking latches on the front panel. Gently push the two locking latches outwards this will eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.

P442

J	H	G	F	E	D	C	B	A
Power supply	Relay board	Relay board	Relay Board (or optional high break	Opto-input board	Opto-input board	Transformer board	Optional board	Optional board

P444

N	M	L	K	J	H	G	F	E	D	C	B	A
Power supply	Relay Board	Relay Board (or optional high break	Relay Board (or optional high break	Relay Board (or optional high break	Relay board (option)	Relay board (option)	Opto-input board	Opto-input board	Opto-input board	Transformer board	Optional board	Optional board

Figure 2 - P44x PCB/Module Locations (Viewed from front)

The PCBs within the relay are now accessible, Figure 2 show the PCB locations for the distance relays in size 60TE (P442).

The 64-way ribbon cable to the front panel also provides the electrical connections between PCBs with the connections being via IDC connectors.

The slots inside the case to hold the PCBs securely in place each correspond to a rear terminal block. Looking from the front of the relay these terminal blocks are labelled from right to left.

> *Note: To ensure compatibility, always replace a faulty PCB with one of an identical part number. Table 1 lists the part numbers of each PCB type.*

REF		PCB	Part Number
P442	P444		
--	--	Main processor and user interface board	ZN0006-001
--	--	Co-processor board	ZN0003 003
J	N	Power Supply Board (24/54V dc) (48/125V dc) (110/250V dc)	ZN0001 001 ZN0001 002 ZN0001 003
FGH F		Relay outputs PCB High-break relay outputs PCB	ZN0002 001 ZN0031-001
	GHJKLM JKL	Relay outputs PCB High-break relay outputs PCB	ZN0019 001 ZN0031-001
DE	DEF	Opto Input PCB	ZN0005-001 or ZN0005-002 ZN0017 001
C	C	Transformer PCB	GN0014-013
AB	AB	Assy IRIG-B modulated PCB Optical Fibre + IRIG-B PCB Assy IRIG-B demodulated PCB Assy Ethernet (100Mbps) PCB Assy Ethernet (100Mbps) + IRIG-B (mod) PCB Assy Ethernet (100Mbps) IRIG-B (demod) PCB Assy 2nd rear port + IRIG-B (mod) PCB Assy 2nd rear port only PCB Assy Redundant Ethernet (SHR) Modulated IRIG-B PCB Assy Redundant Ethernet (SHR) non Modulated IRIG-B PCB Assy Redundant Ethernet (RSTP) Modulated IRIG-B PCB Assy Redundant Ethernet (RSTP) non Modulated IRIG-B PCB Assy Redundant Ethernet (DHS) Modulated IRIG-B PCB Assy Redundant Ethernet (DHS) non Modulated IRIG-B PCB	ZN0007 001 ZN0007-002 ZN0007 003 ZN0049 001 ZN0049 002 ZN0049 003 ZN0025 001 ZN0025 002 ZN0071 001 ZN0071 002 ZN0071 005 ZN0071 006 ZN0071 007 ZN0071 008

Table 1 - PCB Part Numbers

1.3.2.1 Replacement of the main processor board

The main processor board is located in the front panel, not within the case as with all the other PCBs.

Place the front panel with the user interface face-down and remove the six screws from the metallic screen, as shown in Figure 3. Remove the metal plate.

There are two further screws, one each side of the rear of the battery compartment moulding, that hold the main processor PCB in position. Remove these screws.

The user interface keypad is connected to the main processor board via a flex-strip ribbon cable. Carefully disconnect the ribbon cable at the PCB-mounted connector as it could easily be damaged by excessive twisting.

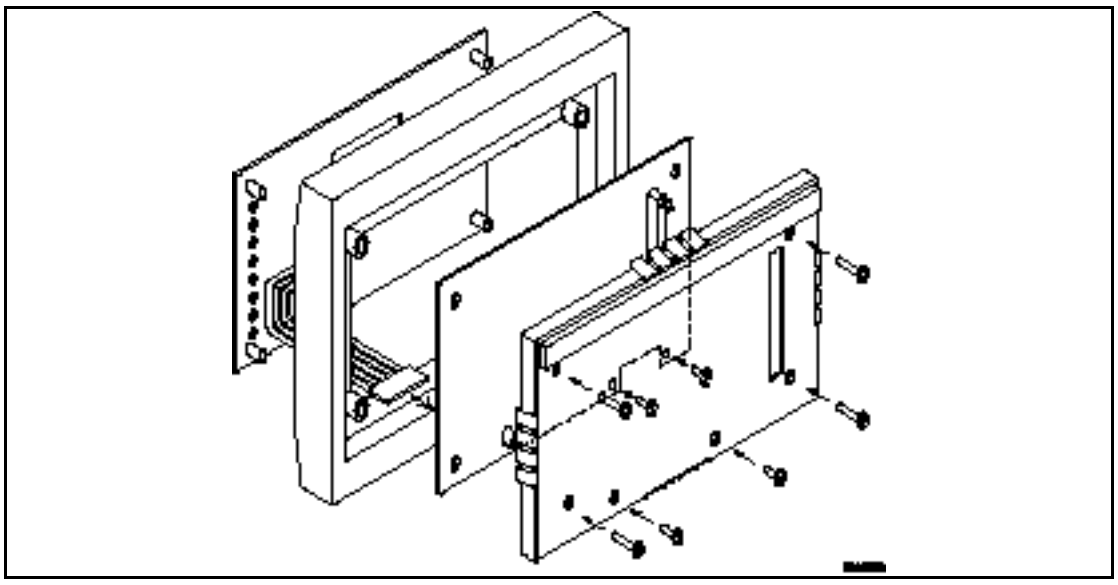


Figure 3 - Front Panel Assembly

The front panel can then be re-assembled with a replacement PCB using the reverse procedure, ensuring that the ribbon cable is reconnected to the main processor board and all eight screws are re-fitted.

Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on case sizes 60TE, press on the location of the hinge-assistance T-pieces so that they click back into the front panel moulding.

After replacement of the main processor board, all the settings required for the application will need to be re-entered. It is therefore useful to have an electronic copy of the application-specific settings is available on disk. Although this is not essential, it can reduce the time taken to re-enter the settings and hence the time the protection is out of service.

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 7 (inclusive) of this document.

1.3.2.2 Replacement of an optional (IRIG-B, Ethernet…) board

To replace a faulty board, disconnect all connections at the rear of the relay.

Depending on the model number of the relay, the optional board may have connections for IRIG-B signals, IEC 60870-5-103 (VDEW) communications, etc.

To replace a faulty board, disconnect all connections at the rear of the relay.

The module is secured in the case by two screws accessible from the rear of the relay, one at the top and another at the bottom, as shown in Figure 4. Remove these screws carefully as they are not captive in the rear panel of the relay.

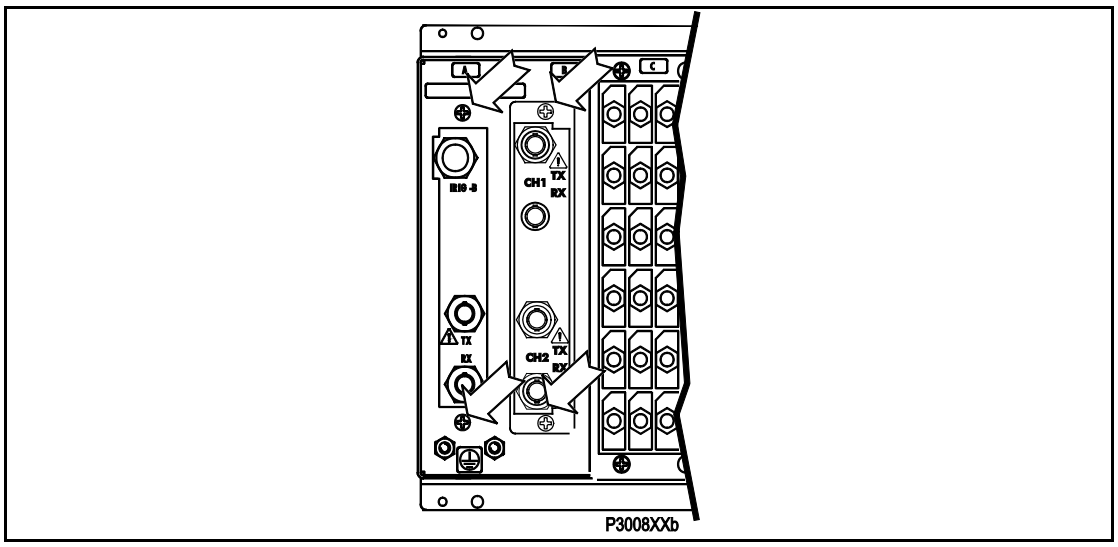


Figure 4 - Location of Securing Screws for optional Boards

Gently pull the board forward and out of the case.

To help identify that the correct board has been removed, Figure 5 shows the layout of the IRIG-B board with both IRIG-B and IEC 60870-5-103 options fitted (ZN0007 003). The other versions (ZN0007 001 and ZN0007 002) use the same PCB layout but with less components fitted.

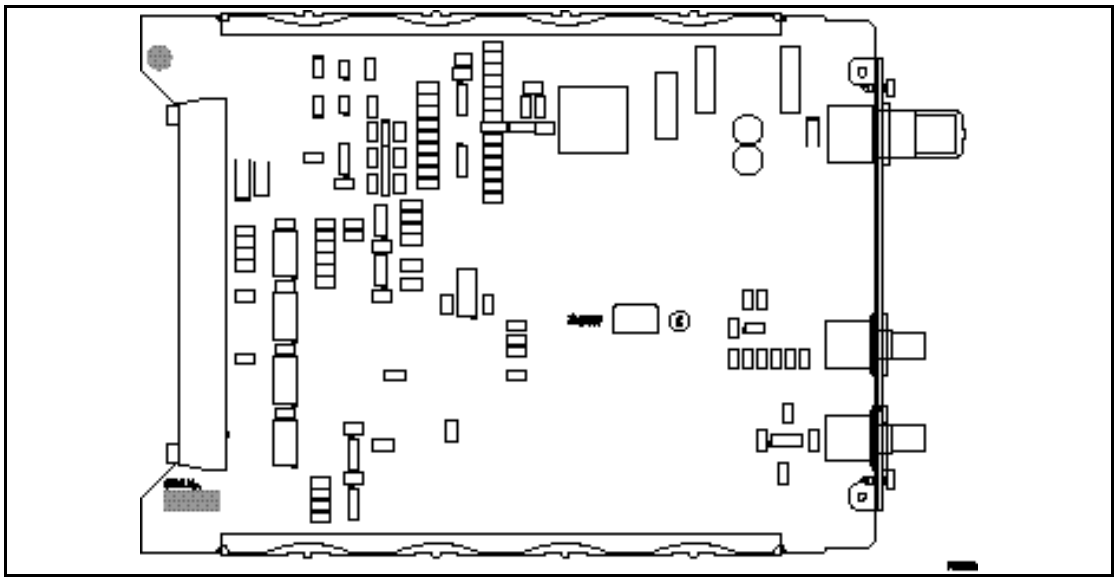


Figure 5 - Typical IRIG-B Board

The replacement PCB should be carefully fitted into the appropriate slot, ensuring that it is pushed fully back on to the rear terminal blocks and the securing screws are re-fitted.

Reconnect all connections at the rear of the relay.

Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on case sizes 60TE, press on the location of the hinge-assistance T-pieces so that they click back into the front panel moulding.

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 7 (inclusive) of this document.

1.3.2.3 Replacement of the input module

The input module comprises of two boards fastened together, the transformer board and the input board.

The module is secured in the case by two screws on its right-hand side, accessible from the front of the relay, as shown in Figure 6. Remove these screws carefully as they are not captive in the front plate of the module.

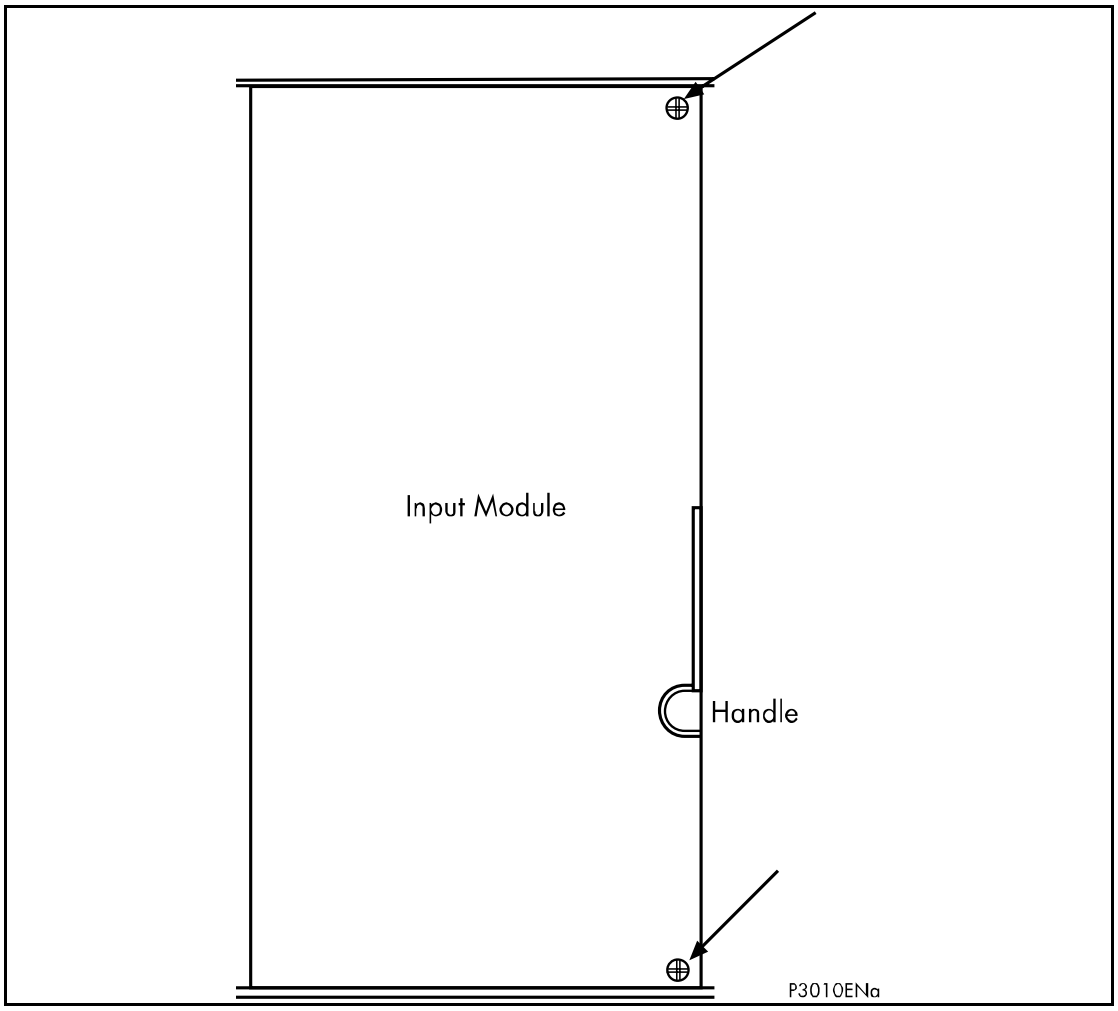


Figure 6 - Location of Securing Screws for Input Module

On the right-hand side of the analogue input module there is a small metal tab that brings out a handle. Grasping this handle firmly, pull the module forward, away from the rear terminal blocks. A reasonable amount of force will be required to achieve this due to the friction between the contacts of two terminal blocks, one medium duty and one heavy duty.

Note:	*Care should be taken when withdrawing the input module as it will suddenly come loose once the friction of the terminal blocks has been overcome. This is particularly important with loose relays as the metal case will need to be held firmly whilst the module is withdrawn.*

Remove the module from the case, taking care as it is heavy because it contains all the relay's input voltage and current transformers.

The replacement module can be slotted in using the reverse procedure, ensuring that it is pushed fully back on to the rear terminal blocks and the securing screws are re-fitted.

> *Note: The transformer and input boards within the module are calibrated together with the calibration data being stored on the input board. Therefore it is recommended that the complete module is replaced to avoid having to perform an on-site recalibration.*

Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on case sizes 60TE, press on the location of the hinge-assistance T-pieces so that they click back into the front panel moulding.

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 7 (inclusive) of this document.

1.3.2.4 Replacement of the power supply board

The power supply board is fastened to a relay board to form the power supply module and is located on the extreme left-hand side of all MiCOM distance relays.

Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force will be required to achieve this due to the friction between the contacts of the two medium duty terminal blocks.

The two boards are held together with push-fit nylon pillars and can be separated by pulling them apart. Care should be taken when separating the boards to avoid damaging the inter-board connectors located near the lower edge of the PCBs towards the front of the power supply module.

The power supply board is the one with two large electrolytic capacitors on it that protrude through the other board that forms the power supply module. To help identify that the correct board has been removed, Figure 7 shows the layout of the power supply board for all voltage ratings.

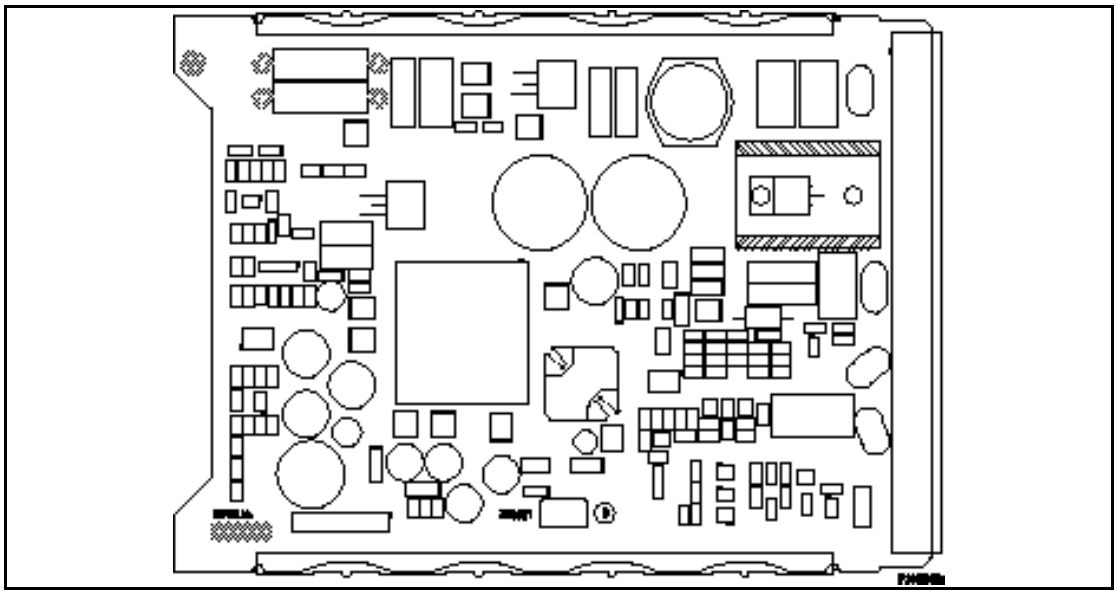


Figure 7 - Typical Power Supply Board

Re-assemble the module with a replacement board ensuring the inter-board connectors are firmly pushed together and the four push-fit nylon pillars are securely located in their respective holes in each PCB.

Slot the power supply module back into the relay case, ensuring that it is pushed fully back on to the rear terminal blocks.

Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on case sizes 60TE, press on the location of the hinge-assistance T-pieces so that they click back into the front panel moulding.

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 7 (inclusive) of this document.

1.3.2.5 Replacement of the relay board in the power supply module

Remove and replace the relay board in the power supply module as described in 8.3.2.4 above.

The relay board is the one with the board with holes cut in it to allow the transformer and two large electrolytic capacitors to protrude through. To help identify that the correct board has been removed, Figure 8 shows the layout of the relay board.

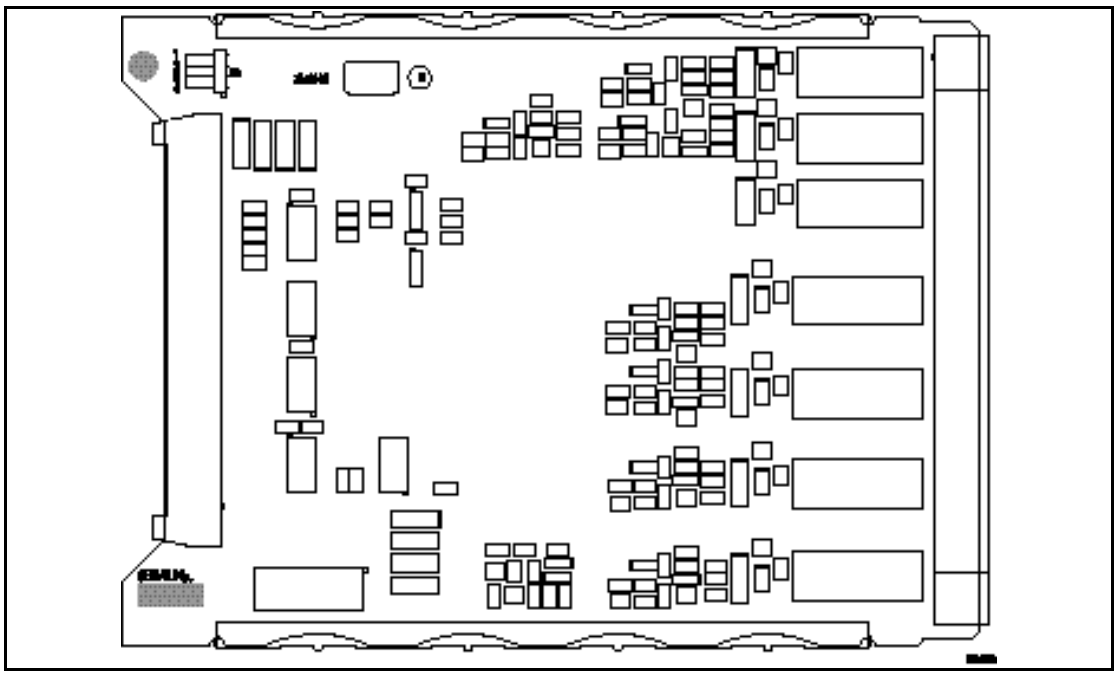


Figure 8 - Typical Relay Board

Ensure the setting of the link (located above IDC connector) on the replacement relay board is the same as the one being replaced before replacing the module in the relay case.

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 7 (inclusive) of this document.

1.3.2.6 Replacement of the extra relay board (P442 and P444 only)

The P442 distance relay has two additional boards compared to the P441 and the P444 four additional boards compared to the P441. Some of these boards provides extra output relays and optically-isolated inputs.

To remove a faulty PCB, gently pull it forward and out of the case.

If the relay board is being replaced, ensure the setting of the link (located above IDC connector) on the replacement relay board is the same as the one being replaced. To help identify that the correct board has been removed, Figure 8 and Figure 9 illustrate the layout of the relay and Opto boards respectively.

The replacement PCB should be carefully fitted into the appropriate slot, ensuring that it is pushed fully back on to the rear terminal blocks.

Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on case sizes 60TE, press on the location of the hinge-assistance T-pieces so that they click back into the front panel moulding.

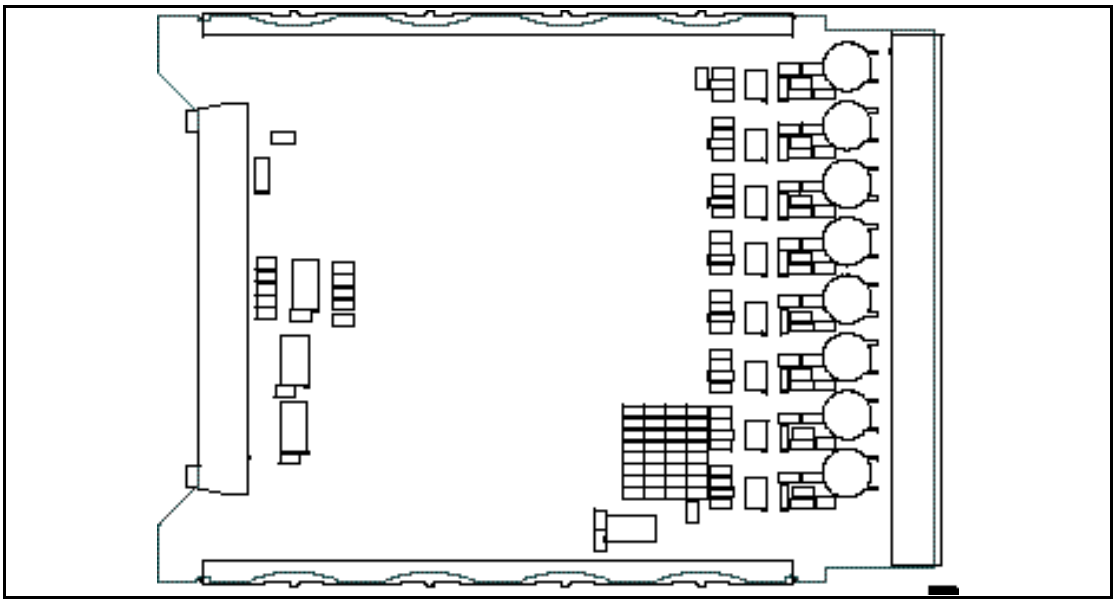


Figure 9 – Typical Opto Board

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 7 (inclusive) of this document.

1.3.2.7 Replacement of the opto and separate relay boards

To remove either, gently pull the faulty PCB forward and out of the case.

If the relay board is being replaced, ensure the setting of the link (located above IDC connector) on the replacement relay board is the same as the one being replaced. To help identify that the correct board has been removed, Figure 10 shows the layout of the opto board.

Before fitting the replacement PCB check that the number on the round label adjacent to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect write the correct slot number on the label.

The replacement PCB should be carefully slid into the appropriate slot, ensuring that it is pushed fully back on to the rear terminal blocks.

Refit the front panel using the reverse procedure to that given in section 1.3.2. After refitting and closing the access covers on size 80TE cases, press at the location of the hinge-assistance T-pieces so that they click back into the front panel moulding.

Once the relay has been reassembled after repair, it should be recommissioned in accordance with the instructions in sections 1 to 8 inclusive (see commissioning and maintenance section in P44x/EN CM).

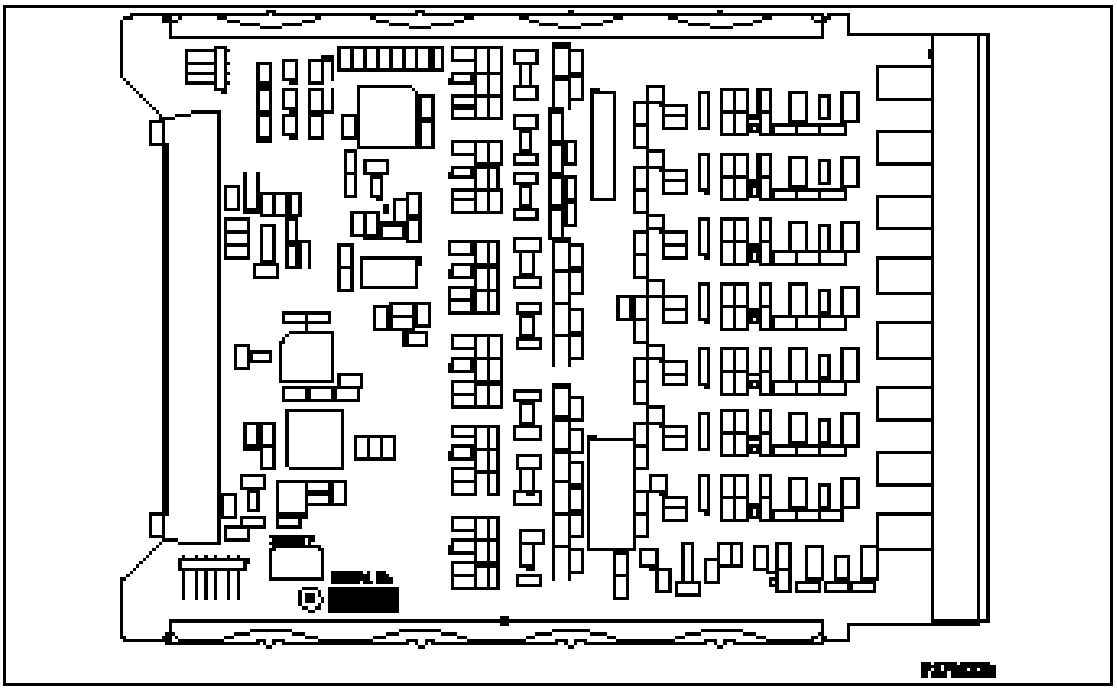


Figure 10: Typical opto board

1.4 Recalibration

Recalibration is not usually required when a PCB is replaced unless it happens to be one of the two boards in the input module, the replacement of which directly affect the calibration.

Although it is possible to carry out an on-site recalibration, this requires test equipment with suitable accuracy and a special calibration program to run on a PC. It is therefore recommended that the work be carried out by the manufacturer, or entrusted to an approved service centre.

1.5 Changing the battery

Each relay has a battery to maintain status data and the correct time when the auxiliary supply voltage fails. The data maintained includes event, fault and disturbance records and the thermal state at the time of failure.

This battery will periodically need changing, although an alarm will be given as part of the relay's continuous self-monitoring in the event of a low battery condition.

If the battery-backed facilities are not required to be maintained during an interruption of the auxiliary supply, the steps below can be followed to remove the battery, but do not replace with a new battery.

1.5.1 Instructions for Replacing The Battery

Open the bottom access cover on the front of the relay.

Gently extract the battery from its socket. If necessary, use a small screwdriver to prise the battery free.

Ensure that the metal terminals in the battery socket are free from corrosion, grease and dust.

The replacement battery should be removed from its packaging and placed into the battery holder, taking care to ensure that the polarity markings on the battery agree with those adjacent to the socket.



Note: Only use a type ½AA Lithium battery with a nominal voltage of 3.6 V.

Ensure that the battery is securely held in its socket and that the battery terminals are making good contact with the metal terminals of the socket.

Close the bottom access cover.

1.5.2 Post Modification Tests

To ensure that the replacement battery will maintain the time and status data if the auxiliary supply fails, check cell [0806: DATE and TIME, Battery Status] reads ‘Healthy’.

1.5.3 Battery Disposal

The battery that has been removed should be disposed of in accordance with the disposal procedure for Lithium batteries in the country in which the relay is installed.

TROUBLESHOOTING

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1 INTRODUCTION



Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Section/Safety Guide Pxxx-SG-4L-2 or later issue, the Technical Data chapter and the ratings on the equipment rating label.

The purpose of this chapter is to allow an error condition on the relay to be identified so that appropriate corrective action can be taken.

Should the relay have developed a fault, it should be possible in most cases to identify which relay module requires attention. The Maintenance chapter (P44x/EN MT) advises on the recommended method of repair where faulty modules need replacing. It is not possible to perform an on-site repair to a faulted module.

In cases where a faulty relay/module is being returned to the manufacturer or one of their approved service centres, the Repair/Modification Return Authorization should be included.

2 INITIAL PROBLEM IDENTIFICATION

Consult the table below to find the description that best matches the problem experienced, then consult the section referenced to perform a more detailed analysis of the problem.

Symptom	Refer To
Relay fails to power up	Section 4
Relay powers up - but indicates error and halts during power-up sequence	Section 5
Relay Powers up but Out of Service LED is illuminated	Section 6
Error during normal operation	Section 7
Mal-operation of the relay during testing	Section 8

Table 1: Problem identification

3 POWER UP ERRORS

If the relay does not appear to power up then the following procedure can be used to determine whether the fault is in the external wiring, auxiliary fuse, power supply module of the relay or the relay front panel.

Test	Check	Action
1	Measure auxiliary voltage on terminals 1 and 2; verify voltage level and polarity against rating the label on front. Terminal 1 is –dc, 2 is +dc	If auxiliary voltage is present and correct, then proceed to test 2. Otherwise the wiring/fuses in auxiliary supply should be checked.
2	Do LEDs/and LCD backlight illuminate on power-up, also check the N/O watchdog contact for closing.	If they illuminate or the contact closes and no error code is displayed then error is probably in the main processor board (front panel). If they do not illuminate and the contact does not close then proceed to test 3.
3	Check Field voltage output (nominally 48 V DC)	If field voltage is not present then the fault is probably in the relay power supply module.

Table 2: Failure of relay to power up

4 ERROR MESSAGE/CODE ON POWER-UP

During the power-up sequence of the relay self-testing is performed as indicated by the messages displayed on the LCD. If an error is detected by the relay during these self-tests then an error message will be displayed and the power-up sequence will be halted. If the error occurs when the relay application software is executing then a maintenance record will be created and the relay will reboot.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If relay locks up and displays an error code permanently then proceed to test 2. If the relay prompts for input by the user proceed to test 4. If the relay re-boots automatically then proceed to test 5
2	Record displayed error, then remove and re-apply relay auxiliary supply.	Record whether the same error code is displayed when the relay is rebooted. If no error code is displayed then contact the local service centre stating the error code and relay information. If the same code is displayed proceed to test 3.
3	Error code Identification Following text messages (in English) will be displayed if a fundamental problem is detected preventing the system from booting: Bus Fail – address lines SRAM Fail – data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail The following hex error codes relate to errors detected in specific relay modules:	These messages indicate that a problem has been detected on the main processor board of the relay (located in the front panel).
	0c140005/0c0d0000	Input Module (inc. Opto-isolated inputs)
	0c140006/0c0e0000	Output Relay Cards
	Last 4 digits provide details on the actual error.	Other error codes relate to problems within the main processor board hardware or software. It will be necessary to contact GE Vernova with details of the problem for a full analysis.
4	Relay displays message for corrupt settings and prompts for restoration of defaults to the affected settings.	The power up tests have detected corrupted relay settings, it is possible to restore defaults to allow the power-up to be completed. It will then be necessary to re-apply the application-specific settings.
5	Relay resets on completion of power up - record error code displayed	Error 0x0E080000, programmable scheme logic error due to excessive execution time. If the relay powers up successfully, check programmable logic for feedback paths. Other error codes will relate to software errors on the main processor board, contact GE Vernova.

Table 3: Power-up self-test error

5 OUT OF SERVICE LED ILLUMINATED ON POWER UP

Test	Check	Action
1	Using the relay menu confirm whether the Commission Test/Test Mode setting is Enabled. Otherwise proceed to test 2.	If the setting is Enabled then disable the test mode and, verify that the Out of Service LED is extinguished.
2	Select and view the last maintenance record from the menu (in the View Records).	Check for H/W Verify Fail this indicates a discrepancy between the relay model number and the hardware; examine the “Maint. Data”, this indicates the causes of the failure using bit fields: Bit Meaning 0 The application type field in the model number does not match the software ID 1 The application field in the model number does not match the software ID 2 The variant 1 field in the model number does not match the software ID 3 The variant 2 field in the model number does not match the software ID 4 The protocol field in the model number does not match the software ID 5 The language field in the model number does not match the software ID 6 The VT type field in the model number is incorrect (110 V VTs fitted) 7 The VT type field in the model number is incorrect (440 V VTs fitted) 8 The VT type field in the model number is incorrect (no VTs fitted)

Table 4: Out of service LED illuminated

6 ERROR CODE DURING OPERATION

The relay performs continuous self-checking, if an error is detected then an error message will be displayed, a maintenance record will be logged and the relay will reset (after a 1.6 second delay). A permanent problem (for example due to a hardware fault) will generally be detected on the power up sequence, following which the relay will display an error code and halt. If the problem was transient in nature then the relay should reboot correctly and continue in operation. The nature of the detected fault can be determined by examination of the maintenance record logged.

There are also two cases where a maintenance record will be logged due to a detected error where the relay will not reset. These are detection of a failure of either the field voltage or the lithium battery, in these cases the failure is indicated by an alarm message, however the relay will continue to operate.

If the field voltage is detected to have failed (the voltage level has dropped below threshold), then a scheme logic signal is also set. This allows the scheme logic to be adapted in the case of this failure (for example if a blocking scheme is being used).

In the case of a battery failure it is possible to prevent the relay from issuing an alarm using the setting under the Date and Time section of the menu. This setting ‘Battery Alarm’ can be set to 'Disabled' to allow the relay to be used without a battery, without an alarm message being displayed.

Error codes (as reported by the relay via the front panel or in the Maintenance Records) can offer a considerable amount of information about the source of the error.

The Hex Code is reported on the front user interface of the relay immediately prior to a reboot sequence. If this code could not be observed, use the Maintenance Records section of the View Records column to display the corresponding Decimal Code.

Hex Code	Decimal Code	Meaning
0x0C0D0000	202178560	An error has been found in the acquisition process. Check the input boards and opto-input boards
0x0C1600C0	202768576	An error has been found in the output relay board. Check the output relay boards.
0x0C140001	202637313	The serial driver failed to initialise properly. Check the serial port hardware on the power supply board and the main processor board.
0x0C140002	202637314	The LCD driver failed to initialise properly. Check the LCD on the main processor board.
0x0C140003	202637315	The Flash memory driver failed to initialise properly. Check the Flash memory on the main processor board.
0x0C140004	202637316	The date and time driver failed to initialise properly. Check the real-time clock and battery-backed SRAM on the main processor board.
0x0C140005	202637317	The acquisition software failed to initialise properly. Check the input boards and opto-input boards
0x0C140006	202637318	The relay software failed to initialise properly. Check the input boards and opto-input boards
0x0C140007	202637319	The recorder software failed to initialise properly. Check the SRAM memory backup on the main processor board
0x0C140008	202637320	The database failed to initialise properly. Check the EEPROM on the main processor board.
0x0C140009	202637321	The database took too long to commit a change. Check the EEPROM on the main processor board.
0x0C14000A	202637322	The IRIG-B driver failed to initialise properly. Check the IRIG-B interface hardware on the IRIG-B board.
0x0C160010	202768400	The continuous self-checks have found an error in the RAM bus. Check the RAM on the main processor board.
0x0C160011	202768401	The continuous self-checks have found an error in the RAM block. Check the RAM on the main processor board.

Hex Code	Decimal Code	Meaning
0x0C160012	202768402	The continuous self-checks have found an error in the Flash EPROM checksum. Check the Flash EPROM on the main processor board, and then try downloading a new program.
0x0C160013	202768403	The continuous self-checks have found an error in the code comparison. Check the Flash EPROM on the main processor board, and then try downloading a new program.
0x0C160014	202768404	The continuous self-checks have found an error in the battery backed SRAM. Check the battery, then the RAM on the main processor board.
0x0C160015	202768405	The continuous self-checks have found an error in the EEPROM. Check the EEPROM on the main processor board.
0x0C1600A0	202768544	The continuous self-checks have found an error on the acquisition board. Check the input board.
0x0C1600B0	202768560	The continuous self-checks have found an error on the relay board. Check the relay board.
0x0C1600C0	202768576	The continuous self-checks have found an error on an opto-imput board. Check the opto-input board.
0x0C170016	202833942	Secondary initialisation tests detected a fast watchdog failure. Check the Flash EPROM on the main processor board.
0x0C170017	202833943	Secondary initialisation tests detected a battery backed SRAM failure. Check the battery backed SRAM on the main processor board.
0x0C170018	202833944	Secondary initialisation tests detected a bus reset test failure. Check the main processor board.
0x0C170019	202833945	Secondary initialisation tests detected a slow watchdog failure.
0x0E020000	235012096	The number of logic gates in the PSL exceeds allowed number. Check and correct the PSL.
0x0E080000	235405312	The execution of the PSL logic exceeds available time. Check and correct the PSL.
0x8182xxxx	2122252288 to 2122186753	Error code in the commissioning test module. Check the processor board.
0x93830000	1820131328	Software in
0x93840000	1820065792	The check of the SRAM has failed. Check the differential current board.
0x93860000	1819934720	The program does not start. Check the opto-input board.
0x93870000	1819869184	Bad number of opto-inputs. Check the Opto-input board and model number.
0xAC810000	1400832000	Opto-input software stopped

Table 5: Error Codes

Other error codes relate to problems within the main processor board software. Contact the GE Vernova Contact Centre at GA.support@gevernova.com with details of the problem for a full analysis.

7 MAL-OPERATION OF THE RELAY DURING TESTING

7.1 Failure of output contacts

An apparent failure of the relay output contacts may be caused by the relay configuration; the following tests should be performed to identify the real cause of the failure. Note that the relay self-tests verify that the coil of the contact has been energized, an error will be displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED illuminated?	Illumination of this LED may indicate that the relay is in test mode or that the protection has been disabled due to a hardware verify error (see Table 4).
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated then proceed to test 4, if not proceed to test 3.
3	Verify by examination of the fault record or by using the test port whether the protection element is operating correctly.	If the protection element does not operate verify whether the test is being correctly applied. If the protection element does operate then it will be necessary to check the programmable logic, to ensure that the mapping of the protection element to the contacts is correct.
4	Using the Commissioning/Test mode function apply a test pattern to the relevant relay output contacts and verify whether they operate (note the correct external connection diagram should be consulted). A continuity tester can be used at the rear of the relay for this purpose.	If the output relay does operate then the problem must be in the external wiring to the relay. If the output relay does not operate this could indicate a failure of the output relay contacts (note that the self-tests verify that the relay coil is being energized). Ensure that the closed resistance is not too high for the continuity tester to detect.

Table 6: Failure of output contacts

7.2 Failure of opto-isolated inputs

The opto-isolated inputs are mapped onto the relay internal signals using the programmable scheme logic. If an input does not appear to be recognized by the relay scheme logic the Commission Tests/Opto Status menu option can be used to verify whether the problem is in the opto-isolated input itself or the mapping of its signal to the scheme logic functions. If the opto-isolated input does appear to be read correctly then it will be necessary to examine its mapping within the programmable logic.

Ensure the voltage rating for the opto inputs has been configured correctly with applied voltage. If the opto-isolated input state is not being correctly read by the relay the applied signal should be tested. Verify the connections to the opto-isolated input using the correct wiring diagram. Next, using a voltmeter verify that 80% opto setting voltage is present on the terminals of the opto-isolated input in the energized state. If the signal is being correctly applied to the relay then the failure may be on the input card itself. Depending on which opto-isolated input has failed this may require replacement of either the complete analog input module (the board within this module cannot be individually replaced without re-calibration of the relay) or a separate opto board.

7.3 Incorrect analog signals

The measurements may be configured in primary or secondary to assist. If it is suspected that the analog quantities being measured by the relay are not correct then the measurement function of the relay can be used to verify the nature of the problem. The measured values displayed by the relay should be compared with the actual magnitudes at the relay terminals. Verify that the correct terminals are being used (in particular the dual rated CT inputs) and that the CT and VT ratios set on the relay are correct. The correct 120 degree displacement of the phase measurements should be used to confirm that the inputs have been correctly connected.

7.4 PSL editor troubleshooting

A failure to open a connection could be because of one or more of the following:

- The relay address is not valid (note: this address is always 1 for the front port)
- Password in not valid
- Communication Set-up - COM port, Baud rate, or Framing - is not correct
- Transaction values are not suitable for the relay and/or the type of connection
- Modem configuration is not valid. Changes may be necessary when using a modem
- The connection cable is not wired correctly or broken. See MiCOM S1 Agile connection configurations

7.4.1 Diagram reconstruction after recover from relay

Although the extraction of a scheme from a relay is supported, the facility is provided as a way of recovering a scheme in the event that the original file is unobtainable.

The recovered scheme will be logically correct, but much of the original graphical information is lost. Many signals will be drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B.

Any annotation added to the original diagram (titles, notes, etc.) are lost.

Sometimes a gate type may not be what was expected, e.g. a 1-input AND gate in the original scheme will appear as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 will also appear as OR gates.

7.4.2 PSL version check

The PSL is saved with a version reference, time stamp and CRC check. This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

SCADA COMMUNICATIONS

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1 SCADA COMMUNICATIONS

1.1 Introduction

This section outlines the remote communications interfaces of the MiCOM relay. The relay supports a choice of one of five protocols via the rear communication interface, selected via the model number when ordering. This is in addition to the front serial interface and 2nd rear communications port, which supports the Courier protocol only.

The rear EIA(RS)485 interface is isolated and is suitable for permanent connection whichever protocol is selected. The advantage of this type of connection is that up to 32 relays can be 'daisy chained' together using a simple twisted pair electrical connection.

The descriptions in this section do not detail the protocol itself. The relevant documentation for the protocol should be referred to for this information. This section serves to describe the specific implementation of the protocol in the relay.

1.2 Rear port information and connection advice – EIA(RS)485 protocols

1.2.1 Rear communication port EIA(RS)485 interface

The rear EIA(RS)485 communication port is provided by a 3-terminal screw connector located on the back of the relay. See section P44x/EN IN for details of the connection terminals. The rear port provides K-Bus/EIA(RS)485 serial data communication and is intended for use with a permanently wired connection to a remote control centre. Of the three connections, two are for the signal connection, and the other is for the earth shield of the cable. When the K-Bus option is selected for the rear port, the two signal connections are not polarity conscious, however for MODBUS, IEC 60870-5-103 and DNP3.0 care must be taken to observe the correct polarity.

The protocol provided by the relay is indicated in the relay menu in the 'Communications' column. Using the keypad and LCD, firstly check that the 'Comms. settings' cell in the 'Configuration' column is set to 'Visible', then move to the 'Communications' column. The first cell down the column shows the communication protocol being used by the rear port.

1.2.1.1 EIA(RS)485 bus

The EIA(RS)485 two-wire connection provides a half-duplex fully isolated serial connection to the product. The connection is polarized and whilst the product's connection diagrams indicate the polarization of the connection terminals it should be borne in mind that there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

1.2.1.2 Bus termination

The EIA(RS)485 bus must have 120 Ω (Ohm) ½ Watt terminating resistors fitted at either end across the signal wires – see Figure 1. Some devices may be able to provide the bus terminating resistors by different connection or configuration arrangements, in which case separate external components will not be required. However, this product does not provide such a facility, so if it is located at the bus terminus then an external termination resistor will be required.

1.2.1.3 Bus connections & topologies

The EIA(RS)485 standard requires that each device be directly connected to the physical cable that is the communications bus. Stubs and tees are expressly forbidden, as are star topologies. Loop bus topologies are not part of the EIA(RS)485 standard and are forbidden by it.

Two-core screened cable is recommended. The specification of the cable will be dependent on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. Total cable length must not exceed 1000m. The screen must be continuous and connected to ground at one end, normally at the master connection point; it is important to avoid circulating currents, especially when the cable runs between buildings, for both safety and noise reasons.

This product does not provide a signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored, although it must have continuity for the benefit of other devices connected to the bus. At no stage must the signal ground be connected to the cables screen or to the product's chassis. This is for both safety and noise reasons.

1.2.1.4 Biasing

It may also be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master purposefully waits in receive mode, or even in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequentially not responding. Symptoms of this are poor response times (due to retries), increasing message error counters, erratic communications, and even a complete failure to communicate.

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean; otherwise noise will be injected.

Note: Some devices may (optionally) be able to provide the bus bias, in which case external components will not be required.

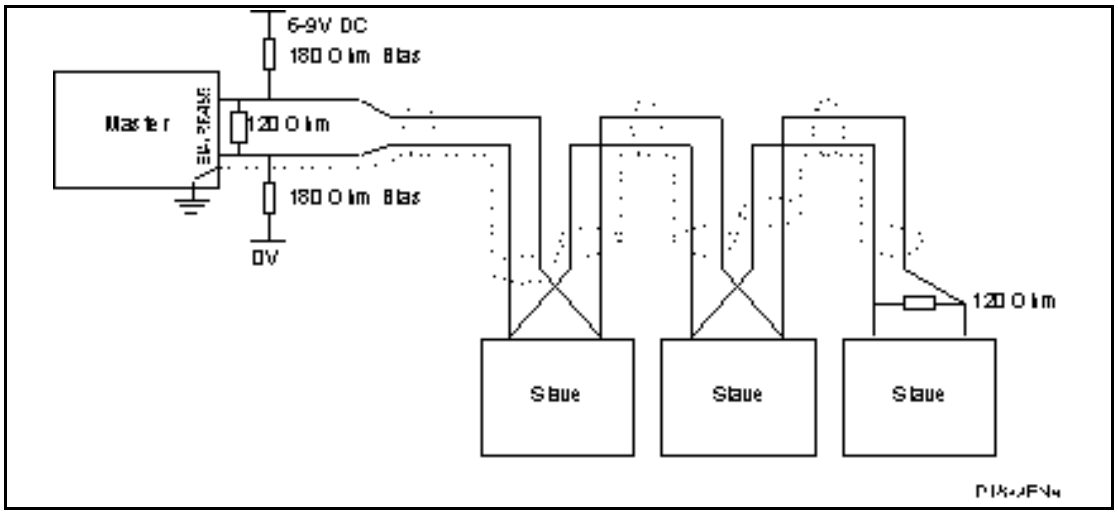


Figure 1: EIA(RS)485 Bus connection arrangements

It is possible to use the products field voltage output (48 V DC) to bias the bus using values of 2.2 kΩ (½W) as bias resistors instead of the 180 Ω resistors shown in the above diagram.

The following warnings apply:

- It is extremely important that the 120 Ω termination resistors are fitted. Failure to do so will result in an excessive bias voltage that may damage the devices connected to the bus.
- As the field voltage is much higher than that required, Alstom Grid cannot assume responsibility for any damage that may occur to a device connected to the network as a result of incorrect application of this voltage.
- Ensure that the field voltage is not being used for other purposes (i.e. powering logic inputs) as this may cause noise to be passed to the communication network.

1.2.2 Courier communication

Courier works on a master/slave basis where the slave units contain information in the form of a database, and respond with information from the database when it is requested by a master unit.

The relay is a slave unit that is designed to be used with a Courier master unit such as MiCOM S1 Agile, MiCOM S1,PAS&T or a SCADA system.

To use the K-Bus rear port to communicate with a PC-based master station using Courier, a KITZ K-Bus to EIA(RS)232 protocol converter is required. This unit is available from GE Vernova. A typical connection arrangement is shown in Figure 2. For more detailed information on other possible connection arrangements refer to the manual for the Courier master station software and the manual for the KITZ protocol converter. Each spur of the K-Bus twisted pair wiring can be up to 1000m in length and have up to 32 relays connected to it.

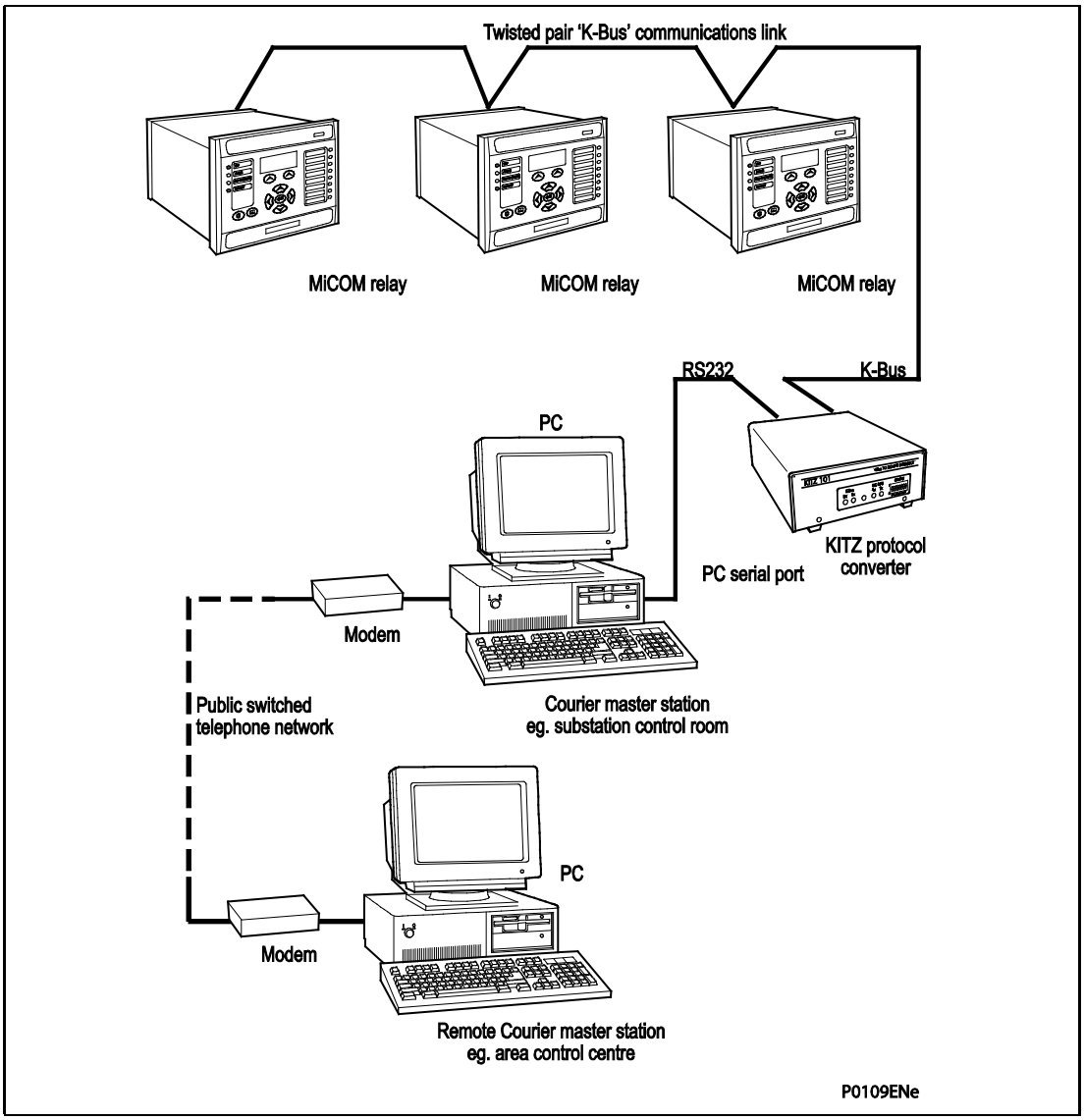


Figure 2: Remote communication connection arrangements

Having made the physical connection to the relay, the relay's communication settings must be configured. To do this use the keypad and LCD user interface. In the relay menu firstly check that the 'Comms. settings' cell in the 'Configuration' column is set to 'Visible', then move to the 'Communications' column. Only two settings apply to the rear port using Courier, the relay's address and the inactivity timer. Synchronous communication is used at a fixed baud rate of 64 kbits/s.

Move down the 'Communications' column from the column heading to the first cell down which indicates the communication protocol:

Protocol
Courier

The next cell down the column controls the address of the relay:

Remote address
1

Since up to 32 relays can be connected to one K-bus spur, as indicated in Figure 2, it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. Courier uses an integer number between 0 and 254

for the relay address, which is set with this cell. It is important that no two relays have the same Courier address. The Courier address is then used by the master station to communicate with the relay. Default value of remote address is 255 and must be changed.

The next cell down controls the inactivity timer:

Inactivity timer
10.00 min.

The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

Note that protection and disturbance recorder settings that are modified using an on-line editor such as PAS&T must be confirmed with a write to the 'Save changes' cell of the 'Configuration' column. Off-line editors such as MiCOM S1 Agile do not require this action for the setting changes to take effect.

1.2.3 MODBUS communication

MODBUS is a master/slave communication protocol, which can be used for network control. In a similar fashion to Courier, the system works by the master device initiating all actions and the slave devices, (the relays), responding to the master by supplying the requested data or by taking the requested action. MODBUS communication is achieved via a twisted pair EIA(RS)485 connection to the rear port and can be used over a distance of 1000m with up to 32 slave devices.

1.2.4 IEC 60870-5 CS 103 communication

The IEC specification IEC 60870-5-103: Telecontrol Equipment and Systems, Part 5: Transmission Protocols Section 103 defines the use of standards IEC 60870-5-1 to IEC 60870-5-5 to perform communication with protection equipment. The standard configuration for the IEC 60870-5-103 protocol is to use a twisted pair EIA(RS)485 connection over distances up to 1000m. The relay operates as a slave in the system, responding to commands from a master station.

1.2.5 DNP3.0 communication

The DNP 3.0 protocol is defined and administered by the DNP User Group. Information about the user group, DNP 3.0 in general and protocol specifications can be found on their website: www.dnp.org

1.3 Second rear communication port (SK4)

There is a hardware option of a second rear communications port, which will run the Courier language. This can be used over one of three physical links: twisted pair K-Bus (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.

The settings for this port are located immediately below the ones for the first port as described in previous sections of P44x/EN IT. Move down the settings until the following sub heading is displayed.

REAR PORT2 (RP2)

The next cell down indicates the language, which is fixed at Courier for RP2.

RP2 protocol Courier

The next cell down indicates the status of the hardware, e.g.

RP2 card status EIA(RS)232 OK

The next cell allows for selection of the port configuration.

RP2 port config. EIA(RS)232

The port can be configured for EIA(RS)232, EIA(RS)485 or K-Bus.

In the case of EIA(RS)232 and EIA(RS)485 the next cell selects the communication mode.

RP2 comms. mode IEC60870 FT1.2

The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.

The next cell down controls the comms. port address.

RP2 address
255

Since up to 32 relays can be connected to one K-bus spur, as indicated in Figure 2, it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. Courier uses an integer number between 0 and 254 for the relay address that is set with this cell. It is important that no two relays have the same Courier address. The Courier address is then used by the master station to communicate with the relay. The default value is 255 and must be changed in the range 0 to 254 before use.

The next cell down controls the inactivity timer.

RP2 inactivity timer
15 mins.

The inactivity timer controls how long the relay will wait without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

In the case of EIA(RS)232 and EIA(RS)485 the next cell down controls the baud rate. For K-Bus the baud rate is fixed at 64kbit/second between the relay and the KITZ interface at the end of the relay spur.

RP2 baud rate
19200

Courier communications is asynchronous. Three baud rates are supported by the relay, ‘9600 bits/s’, ‘19200 bits/s’ and ‘38400 bits/s’.

1.4 Ethernet communication

1.4.1 Legacy Protocols

It is possible to communicate through an Ethernet network using an Alstom Grid I4XS4UE (refer to Px4x/EN REB user guide for Redundant Ethernet board connections).

1.4.2 Hot-standby Ethernet failover

This is used for products which do not have Ethernet redundancy and applies only to those using single Ethernet boards. This board has one fibre and one copper interface. If there is a fault on the fibre channel it can switch to the copper channel, or vice versa. Px4x products which use the Parallel Redundancy Protocol (PRP) do not need this function.

When this function detects a link failure, it generates the NIC Fail Alarm. The failover timer then starts, which has a settable timeout of 2 to 60 secs in 100 ms steps. During this time, the Hot Standby Failover function continues to check the status of the other channel. If the link failure recovers before the failover timer timesout, the channels are not swapped over. If there is still a fail when the failover timer times out and the other channel status is ok, the channels are swapped over. The Ethernet controller is then reconfigured and the link is renegotiated.

1.4.2.1 Hot-standby Ethernet failover settings

To set the function:

1. Start S1 Agile.
2. Click the Ethernet Configuration tile.
3. Start the IEC 61850 IED Configurator.

Working offline:

1. Click the icon New MiCOM Configuration from an Installed ICD File.
2. Double-click the product variant.
3. Double-click the Communications item.

Or working online:

1. Select Device > Manage IED.
2. Select the IED type device number.
3. Select the IED address and click Next. The IED 61850 Configurator tool reads information from the IED and shows them in the Summary view.
4. Click the Communications tab to read and edit the settings.

Then:

1. The Media setting defines the default interface used to communicate between clients and peers, and the MiCOM IED. The value is taken from the ConnectedAP/PhysConn section of the configured SCL file and is editable in Manual Editing Mode. The single Ethernet board has one fibre and one copper interface. If you are using fibre, select Single Fibre. If you are using copper, select Single Copper or Redundant Fibre. If you are using a Redundant Ethernet board, select Single Copper or Redundant Fibre.
2. Set the Ethernet Failover to Enable and adjust the Failover Timeout as required. This does not appear if the product does not have Ethernet Failover.

2 COURIER INTERFACE

2.1 Courier protocol

K-Bus is based on EIA(RS)485 voltage levels with HDLC FM0 encoded synchronous signalling and its own frame format. The K-Bus twisted pair connection is unpolarized, whereas the EIA(RS)485 and EIA(RS)232 interfaces are polarized.

The EIA(RS)232 interface uses the IEC 60870-5 FT1.2 frame format.

The relay supports an IEC 60870-5 FT1.2 connection on the front-port. This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate, 11-bit frame, and a fixed device address.

The rear interface is used to provide a permanent connection for K-Bus and allows multi-drop connection. It should be noted that although K-Bus is based on EIA(RS)485 voltage levels it is a synchronous HDLC protocol using FM0 encoding. It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. Nor is it possible to connect K-Bus to an EIA(RS)485 computer port. A protocol converter, such as the KITZ101, should be employed for this purpose.

Alternatively for direct connections, the fibre optic converter card may be used to convert the rear EIA(RS)485 port into a fibre optic (ST) port.

2.2 Supported command set

The following Courier commands are supported by the relay:

Protocol Layer

- Reset Remote Link
- Poll Status
- Poll Buffer*

Low Level Commands

- Send Event*
- Accept Event*
- Send Block
- Store Block Identifier
- Store Block Footer

Menu Browsing

- Get Column Headings
- Get Column Text
- Get Column Values
- Get Strings
- Get Text
- Get Value
- Get Column Setting Limits

Setting Changes

Enter Setting Mode

Preload Setting

Abort Setting

Execute Setting

Reset Menu Cell

Set Value

Control Commands

Select Setting Group

Change Device Address*

Set Real Time

*Note: Commands indicated with a * are not supported via the front Courier port.*

2.3 Relay courier database

The Courier database is a two dimensional structure with each cell in the database being referenced by a row and column address. Both the column and the row can take a range from 0 to 255. Addresses in the database are specified as hexadecimal values; e.g. 0A02 is column 0A (10 decimal) row 02. Associated settings/data will be part of the same column, row zero of the column contains a text string to identify the contents of the column, i.e. a column heading.

The menu database contains the complete database definition for the relay. For each cell location the following information is stated:

- Cell text
- Cell datatype
- Cell value
- Whether the cell is settable, if so
- Minimum value
- Maximum value
- Step size
- Password level required to allow setting changes
- String information (for Indexed String or Binary flag cells)

2.4 Setting changes

(See R6512, Courier User Guide - Chapter 9)

There are three categories of settings within the relay database:

- Control and support
- Disturbance recorder
- Protection settings group

Setting changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to either the disturbance recorder settings or the protection settings groups are stored in a 'scratchpad' memory and are not immediately implemented by the relay.

To action setting changes stored in the scratchpad the save changes cell in the configuration column must be written to. This allows the changes to either be confirmed and stored in non-volatile memory, or the setting changes to be aborted.

2.4.1 Setting transfer mode

If it is necessary to transfer all of the relay settings to or from the relay a cell within the communication system data column can be used. This cell (location BF03) when set to 1 makes all of the relay settings visible. Any setting changes made, with the relay set in this mode, are stored in scratchpad memory (including control and support settings). When the value of BF03 is set back to 0 any setting changes are verified and stored in non-volatile memory.

2.5 Event extraction

Events can be extracted either automatically (rear port only) or manually (either Courier port). For automatic extraction all events are extracted in sequential order using the standard Courier event mechanism, this includes fault/maintenance data if appropriate. The manual approach allows the user to select events, faults, or maintenance data at random from the stored records.

2.5.1 Automatic event extraction

(See Chapter 7 Courier User Guide, publication R6512)

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported via the rear Courier port.

When new event information is created the event bit is set within the status byte, this indicates to the master device that event information is available. The oldest, unextracted event can be extracted from the relay using the send event command. The relay will respond with the event data, which will be either a Courier Type 0 or Type 3 event. The Type 3 event is used for fault records and maintenance records.

Once an event has been extracted from the relay, the accept event can be used to confirm that the event has been successfully extracted. If all events have been extracted then the event bit will reset, if there are more events still to be extracted the next event can be accessed using the send event command as before.

2.5.2 Event types

Events will be created by the relay under the following circumstances:

- Change of state of output contact
- Change of state of opto input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out
- Fault record (Type 3 Courier Event)
- Maintenance record (Type 3 Courier Event)

2.5.3 Event format

The send event command results in the following fields being returned by the relay:

- Cell reference
- Timestamp
- Cell text
- Cell value

The menu database contains a table of the events created by the relay and indicates how the contents of the above fields are interpreted. Fault records and maintenance records will return a Courier Type 3 event, which contains the above fields together with two additional fields:

- Event extraction column
- Event number

These events contain additional information that is extracted from the relay using the referenced extraction column. Row 01 of the extraction column contains a setting that allows the fault/maintenance record to be selected. This setting should be set to the event number value returned within the record; the extended data can be extracted from the relay by uploading the text and data from the column.

2.5.4 Manual event record extraction

Column 01 of the database can be used for manual viewing of event, fault, and maintenance records. The contents of this column will depend on the nature of the record selected. It is possible to select events by event number and to directly select a fault record or maintenance record by number.

Event Record Selection (Row 01) - This cell can be set to a value between 0 to 511 to select which of the 512 stored events is selected, 0 will select the most recent record; 511 the oldest stored record. For simple event records, (Type 0) cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3) then the remainder of the column will contain the additional information.

Fault Record Selection (Row 05) – This cell can be used to directly select a fault record using a value between 0 and 4 to select one of up to five stored fault records. (0 will be the most recent fault and 4 will be the oldest). The column will then contain the details of the fault record selected.

Maintenance Record Selection (Row F0) – This cell can be used to select a maintenance record using a value between 0 and 4 and operates in a similar way to the fault record selection.

If this column is used to extract event information from the relay the number associated with a particular record will change when a new event or fault occurs.

2.6 Disturbance record extraction

Select Record Number (Row 01) - This cell can be used to select the record to be extracted. Record 0 will be the oldest unextracted record, already extracted older records will be assigned positive values, and negative values will be used for more recent records. To facilitate automatic extraction via the rear port the disturbance bit of the status byte is set by the relay whenever there are unextracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from cell 02. The disturbance record itself can be extracted using the block transfer mechanism from cell B00B.

As has been stated, the rear Courier port can be used to automatically extract disturbance records as they occur. This operates using the standard Courier mechanism defined in Chapter 8 of the Courier User Guide. The front Courier port does not support automatic extraction although disturbance record data can be extracted manually from this port.

2.7 Programmable scheme logic settings

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the relay using the block transfer mechanism.

The following cells are used to perform the extraction:

- B204 Domain: Used to select either PSL settings (Upload or download) or PSL configuration data (Upload only)
- B208 Sub-Domain: Used to select the Protection Setting Group to be uploaded/downloaded.
- B20C Version: Used on a download to check the compatibility of the file to be downloaded with the relay.
- B21C Transfer Mode: Used to set-up the transfer process.
- B120 Data Transfer Cell: Used to perform upload/download.

The programmable scheme logic settings can be uploaded and downloaded to and from the relay using this mechanism. If it is necessary to edit the settings MiCOM S1 Agile must be used as the data format is compressed. MiCOM S1 Agile also performs checks on the validity of the settings before they are downloaded to the relay.

3 MODBUS INTERFACE

The MODBUS interface is a master/slave protocol and it is defined by MODBUS.org: See

www.modbus.org

MODBUS Serial Protocol Reference Guide: PI-MBUS-300 Rev. E

3.1 Communication link

This interface also uses the rear EIA(RS)485 port (or converted fiber optic port) for communication using 'RTU' mode communication rather than 'ASCII' mode as this provides more efficient use of the communication bandwidth. This mode of communication is defined by the MODBUS standard.

In summary, the character framing is 1 start bit, 8 bit data, either 1 parity bit and 1 stop bit, or two stop bits. This gives 11 bits per character.

The following parameters can be configured for this port using either the front panel interface or the front Courier port:

- Baud rate
- Device address
- Parity
- Inactivity time

3.2 MODBUS functions

The following MODBUS function codes are supported by the relay:

01 Read Coil Status

02 Read Input Status

03 Read Holding Registers

04 Read Input Registers

06 Preset Single Register

08 Diagnostics

11 Fetch Communication Event Counter

12 Fetch Communication Event Log

16 Preset Multiple Registers 127 max

These are interpreted by the MiCOM relay in the following way:

01 Read status of output contacts (0xxxx addresses)

02 Read status of opto inputs (1xxxx addresses)

03 Read setting values (4xxxx addresses)

04 Read measured values (3xxxx addresses

06 Write single setting value (4xxxx addresses)

16 Write multiple setting values (4xxxx addresses)

3.3 Response codes

Code	MODBUS Description	MiCOM Interpretation
01	Illegal Function Code	The function code transmitted is not supported by the slave.
02	Illegal Data Address	The start data address in the request is not an allowable value. If any of the addresses in the

Code	MODBUS Description	MiCOM Interpretation
		range cannot be accessed due to password protection then all changes within the request are discarded and this error response will be returned. Note: If the start address is correct but the range includes non–implemented addresses this response is not produced.
03	Illegal Value	A value referenced in the data field transmitted by the master is not within range. Other values transmitted within the same packet will be executed if inside range.
06	Slave Device Busy	The write command cannot be implemented due to the database being locked by another interface. This response is also produced if the relay software is busy executing a previous request.

3.4 Register mapping

The relay supports the following memory page references:

Memory Page	Interpretation
0xxxx	Read and write access of the output relays
1xxxx	Read only access of the opto inputs
3xxxx	Read only access of data
4xxxx	Read and write access of settings

Where xxxx represents the addresses available in the page (0 to 9999).

Note: The "extended memory file" (6xxxx) is not supported.

A complete map of the MODBUS addresses supported by the relay is shown in the Menu Database.

MODBUS convention is to document register addresses as ordinal values whereas the actual protocol addresses are literal values. The MiCOM relays begin their register addresses at zero. Therefore, the first register in a memory page is register address zero. The second register is register address 1 and so on. Note that the page number notation is not part of the address.

3.5 Event extraction

The relay supports two methods of event extraction providing either automatic or manual extraction of the stored event, fault, and maintenance records.

3.5.1 Manual selection

There are three registers available to manually select stored records, there are also three read only registers allowing the number of stored records to be determined.

40100 - Select Event, 0 to 249

40101 - Select Fault, 0 to 4

40102 - Select Maintenance Record, 0 to 4

For each of the above registers a value of 0 represents the most recent stored record. The following registers can be read to indicate the numbers of the various types of record stored.

30100 - Number of stored records

30101 - Number of stored fault records

30102 - Number of stored maintenance records

Each fault or maintenance record logged causes an event record to be created by the relay. If this event record is selected the additional registers allowing the fault or maintenance record details will also become populated.

3.5.2 Automatic extraction

The automatic extraction facilities allow all types of record to be extracted as they occur. Event records are extracted in sequential order including any fault or maintenance data that may be associated with the event.

The MODBUS master can determine whether the relay has any events stored that have not yet been extracted. This is performed by reading the relay status register 30001 (G26 data type). If the event bit of this register is set then the relay has unextracted events available. To select the next event for sequential extraction the master station writes a value of 1 to the record selection register 40400 (G18 data type). The event data together with any fault/maintenance data can be read from the registers specified below. Once the data has been read the event record can be marked as having been read by writing a value of 2 to register 40400.

3.5.3 Record data

The location and format of the registers used to access the record data is the same whether they have been selected using either of the two mechanisms detailed above.

Event Description	MODBUS Address	Length	Comments
Time and Date	30103	4	See G12 data type description in section 3.8.
Event Type	30107	1	See G13 data type. Indicates type of event.
Event Value	30108	2	Nature of value depends on event type. This will contain the status as a binary flag for contact, opto, alarm, and protection events.
MODBUS Address	30110	1	This indicates the MODBUS register address where the change occurred. Alarm 30011 Relays 30723 Optos 30725 Protection events – like the relay and opto addresses this will map onto the MODBUS address of the appropriate DDB status register depending on which bit of the DDB the change occurred. These will range from 30727 to 30785. For platform events, fault events and maintenance events the default is 0.
Event Index	30111	1	This register will contain the DDB ordinal for protection events or the bit number for alarm events. The direction of the change will be indicated by the most significant bit; 1 for 0 – 1 change and 0 for 1 – 0 change.
Additional Data Present	30112	1	0 means that there is no additional data. 1 means fault record data can be read from 30113 to 30199 (number of registers depends on the product). 2 means maintenance record data can be read from 30036 to 30039.

If a fault record or maintenance record is directly selected using the manual mechanism then the data can be read from the register ranges specified above. The event record data in registers 30103 to 30111 will not be available.

It is possible using register 40401(G6 data type) to clear independently the stored relay event/fault and maintenance records. This register also provides an option to reset the relay indications, which has the same effect on the relay as pressing the clear key within the alarm viewer using the front panel menu.

3.6 Disturbance record extraction

The relay provides facilities for both manual and automatic extraction of disturbance records. The extraction mechanisms are explained below:

3.6.1 Extraction mechanism

Records extracted over MODBUS from Px40 platform relays will be presented in COMTRADE format. This involves extracting an ASCII text configuration file and then extracting a binary data file.

Each file is extracted by reading a series of data pages from the relay. The data page is made up of 127 registers, giving a maximum transfer of 254 bytes per page.

3.6.1.1 Interface registers

The following set of registers is presented to the master station to support the extraction of uncompressed disturbance records:

MODBUS Register	Name	Description
3x00001	Status register	Provides the status of the relay as bit flags: b0 – Out of service b1 – Minor self test failure b2 – Event b3 – Time synchronization b4 – Disturbance b5 – Fault b6 – Trip b7 – Alarm b8 to b15 – Unused A '1' on b4 indicates the presence of a disturbance.
3x00800	Nº of stored disturbances	Indicates the total number of disturbance records currently stored in the relay, both extracted and unextracted.
3x00801	Unique identifier of the oldest disturbance record	Indicates the unique identifier value for the oldest disturbance record stored in the relay. This is an integer value used in conjunction with the 'Nº of stored disturbances' value to calculate a value for manually selecting records.
4x00250	Manual disturbance record selection register	This register is used to manually select disturbance records. The values written to this cell are an offset of the unique identifier value for the oldest record. The offset value, which ranges from 0 to the Nº of stored disturbances – 1, is added to the identifier of the oldest record to generate the identifier of the required record.
4x00400	Record selection command register	This register is used during the extraction process and has a number of commands. These are: b0 – Select next event b1 – Accept event b2 – Select next disturbance record b3 – Accept disturbance record b4 – Select next page of disturbance data b5 – Select data file
3x00930 – 3x00933	Record time stamp	These registers return the timestamp of the disturbance record.

MODBUS Register	Name	Description
3x00802	Nº of registers in data page	This register informs the master station of the number of registers in the data page that are populated.
3x00803 – 3x00929	Data page registers	These 127 registers are used to transfer data from the relay to the master station. They are 16-bit unsigned integers.
3x00934	Disturbance record status register	The disturbance record status register is used during the extraction process to indicate to the master station when data is ready for extraction. See next table.
4x00251	Data file format selection	This is used to select the required data file format. This is reserved for future use.

Note: Register addresses are provided in reference code + address format. E.g. 4x00001 is reference code 4x, address 1 (which is specified as function code 03, address 0x0000 in the MODBUS specification).

The disturbance record status register will report one of the following values:

State	Description
Idle	This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
Busy	The relay is currently processing data.
Page ready	The data page has been populated and the master station can now safely read the data.
Configuration complete	All of the configuration data has been read without error.
Record complete	All of the disturbance data has been extracted.
Disturbance overwritten	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.
No unextracted disturbances	An attempt was made by the master station to automatically select the next oldest unextracted disturbance when all records have been extracted.
Not a valid disturbance	An attempt was made by the master station to manually select a record that did not exist in the relay.
Command out of sequence	The master station issued a command to the relay that was not expected during the extraction process.

3.6.2 Extraction procedure

The following procedure will be used to extract disturbances from the relay. The procedure is split into four sections:

1. Selection of a disturbance – either manually or automatically
2. Extraction of the configuration file
3. Extraction of the data file
4. Accepting the extracted record (automatic extraction only)

3.6.2.1 Manual extraction procedure

The procedure used to extract a disturbance manually is shown in the following figure. The manual method of extraction does not allow for the acceptance of disturbance records.

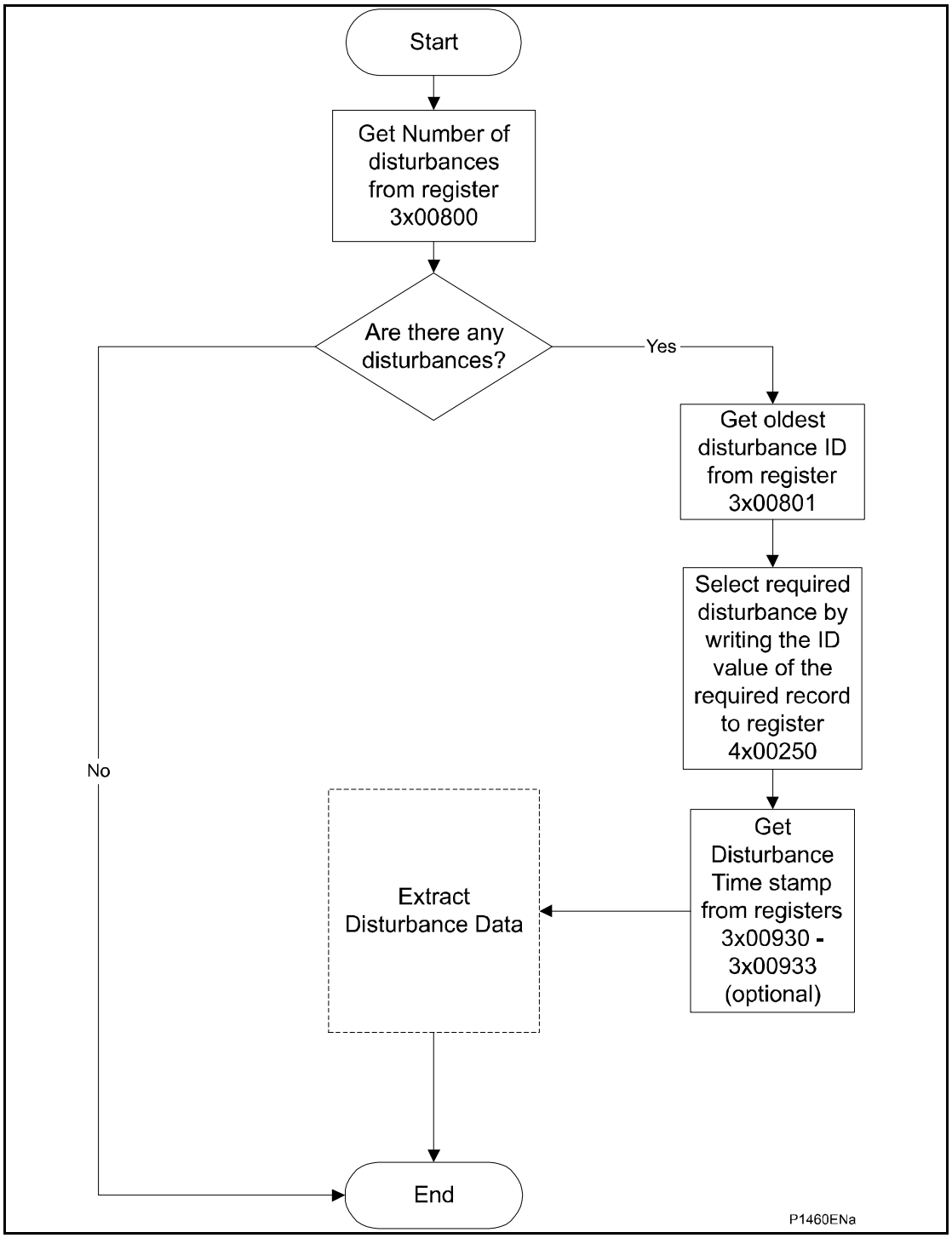


Figure 3: Manual selection of a disturbance record

3.6.2.2 Automatic extraction procedure

There are two methods that can be used for automatically extracting disturbances. Option 1 is simpler and is better at extracting single disturbance records, i.e. when the disturbance recorder is polled regularly. Option 2, however, is more complex to implement but is more efficient at extracting large quantities of disturbance records. This may be useful when the disturbance recorder is polled only occasionally and hence may have many stored records.

3.6.2.3 Automatic extraction procedure – option 1

The procedure for the first method is shown in the following figure. This also shows the acceptance of the disturbance record once the extraction is complete.

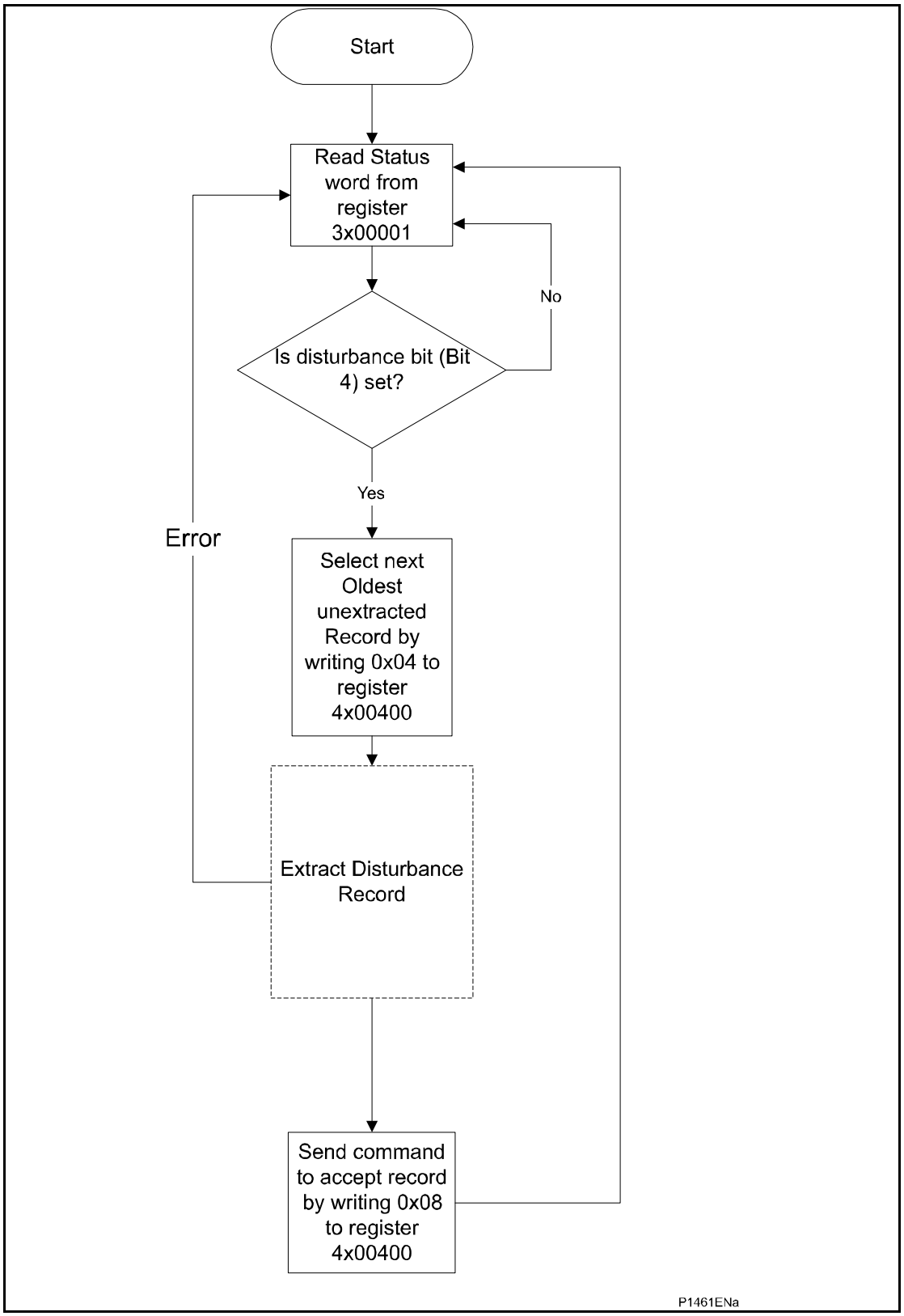


Figure 4: Automatic selection of a disturbance – option 1

3.6.2.4 Automatic extraction procedure – option 2

The second method used for automatic extraction is shown in the following figure. This also shows the acceptance of the disturbance record once the extraction is complete:

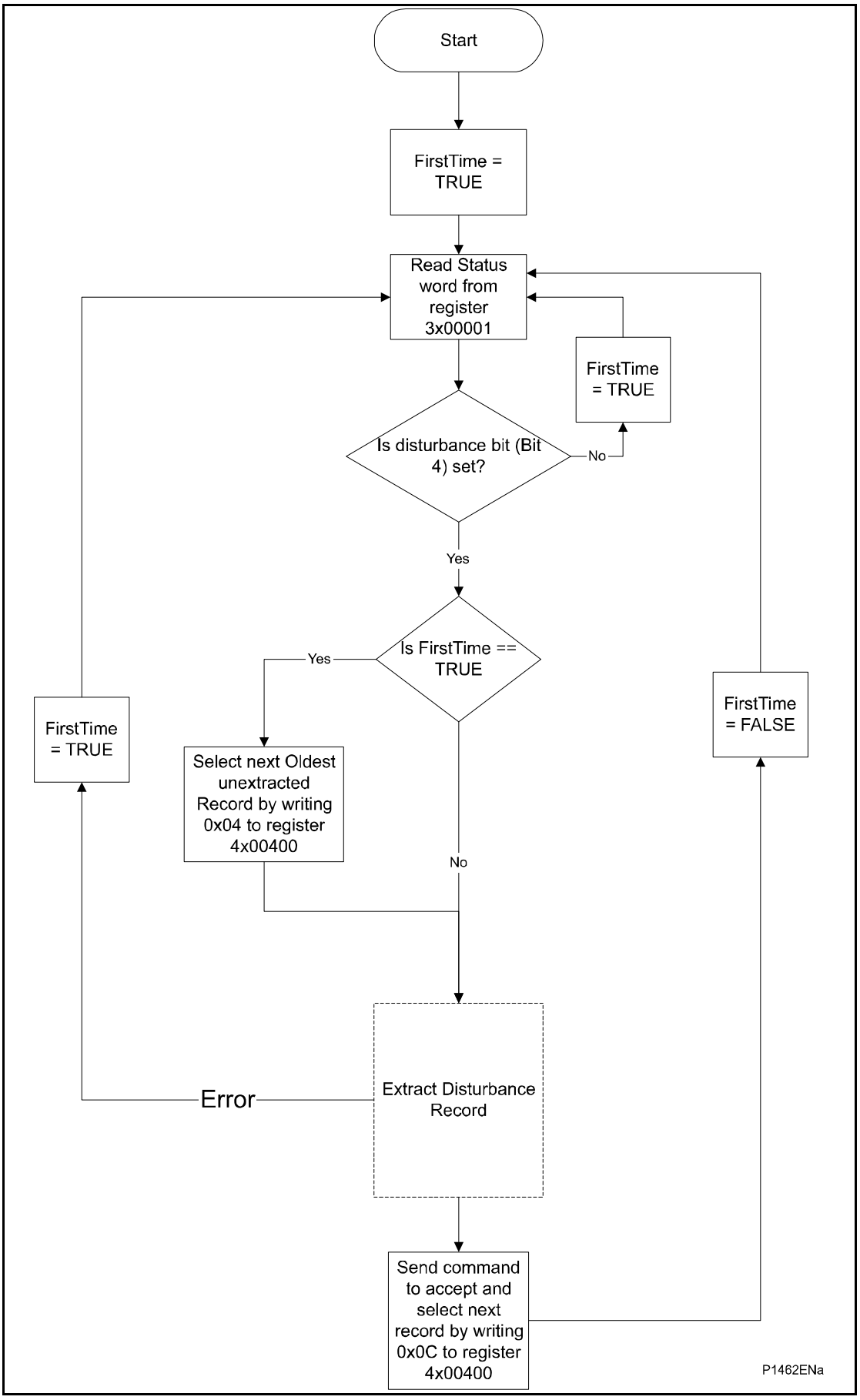


Figure 5: Automatic selection of a disturbance – option 2

3.6.3 Extracting the disturbance data

The extraction of the disturbance record, as shown in the three figures above, is a two-stage process that involves extracting the configuration file first and then the data file.

The following figure shows how the configuration file is extracted from the relay:

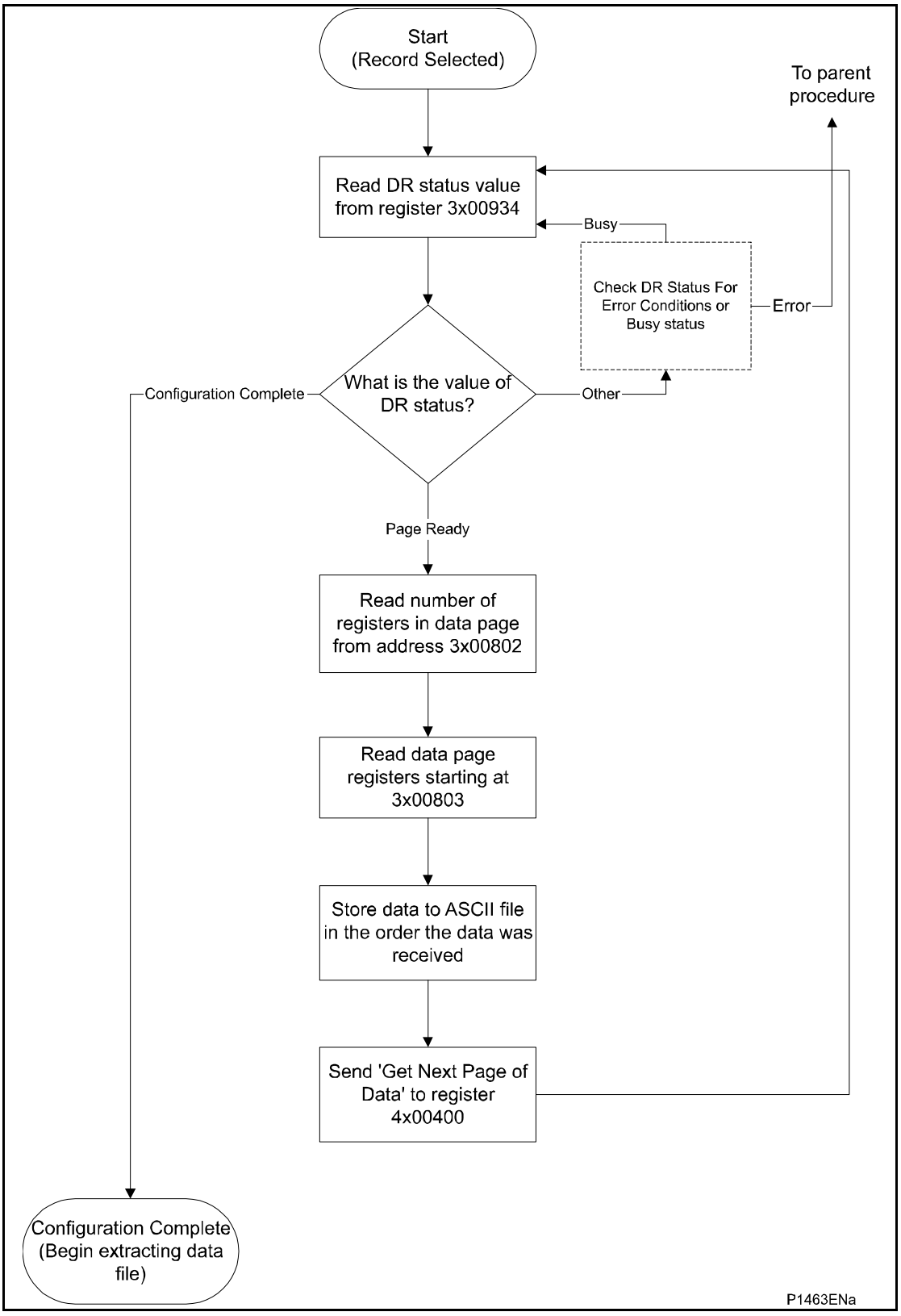


Figure 6: Extracting the comtrade configuration file

The following figure shows how the data file is extracted:

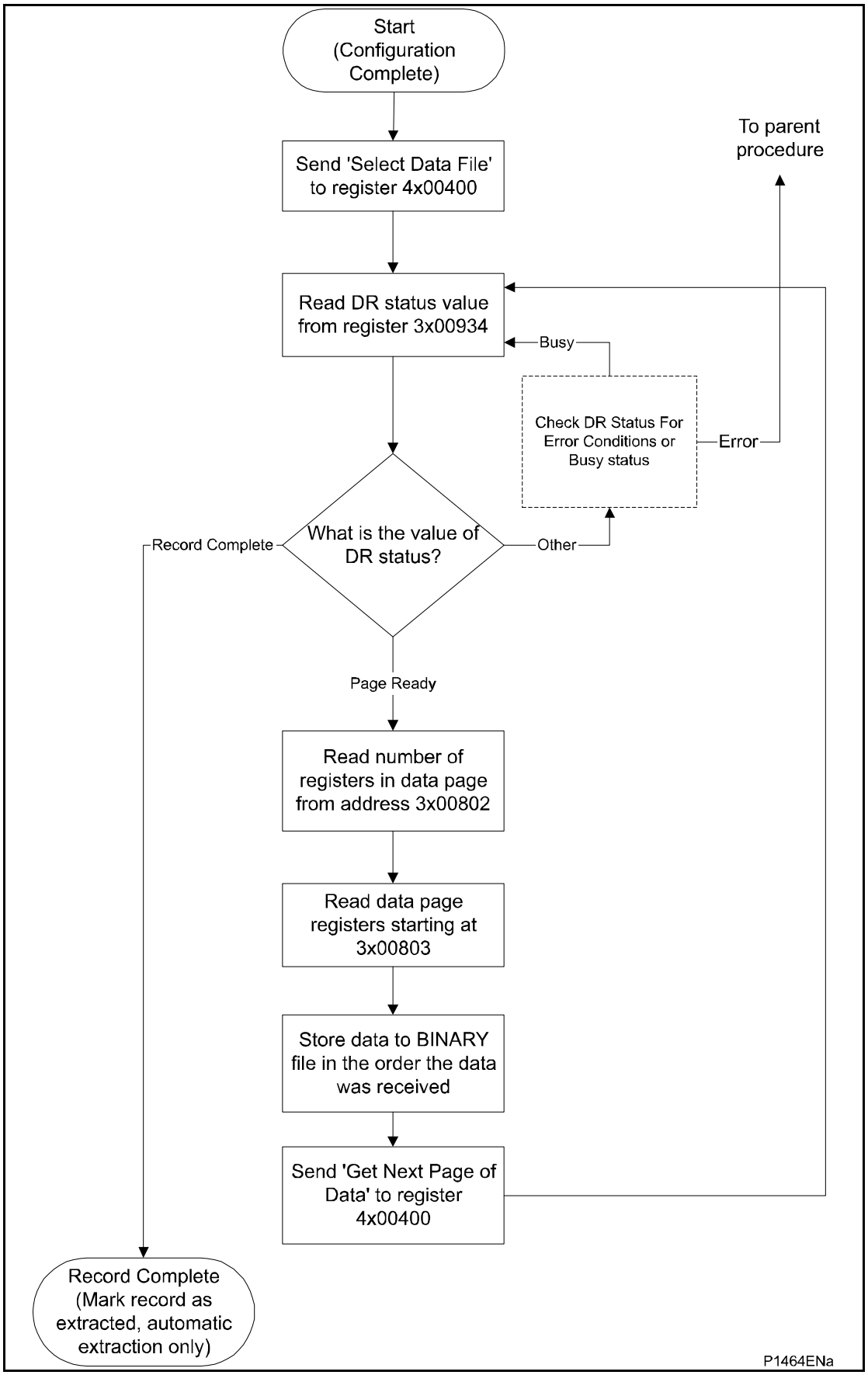


Figure 7: Extracting the comtrade binary data file

During the extraction of the COMTRADE files, an error may occur that will be reported on the DR Status register 3x00934. This can be caused by the relay overwriting the record being extracted or due to the master station issuing a command that is not within the bounds of the extraction procedure.

3.7 Setting changes

The relay settings can be split into two categories:

- Control and support settings
- Disturbance record settings and protection setting groups

Changes to settings within the control and support area are executed immediately. Changes to the protection setting groups or the disturbance recorder settings are stored in a temporary 'scratchpad' area and must be confirmed before they are implemented. All the relay settings are 4xxxx page addresses. The following points should be noted when changing settings:

- Settings implemented using multiple registers must be written to using a multi-register write operation.
- The first address for a multi-register write must be a valid address, if there are unmapped addresses within the range being written to then the data associated with these addresses will be discarded.
- If a write operation is performed with values that are out of range then the illegal data response will be produced. Valid setting values within the same write operation will be executed.
- If a write operation is performed attempting to change registers that require a higher level of password access than is currently enabled then all setting changes in the write operation will be discarded.

3.7.1 Password protection

As described in the introduction to this service manual, the relay settings can be subject to password protection. The level of password protection required to change a setting is indicated in the relay setting database. Level 2 or 3 (relays with cyber security features) is the highest level of password access, level 0 indicates that no password is required.

The following registers are available to control password protection:

a) Models without Cyber Security

40001 & 40002 Password entry

40022 Default password level

40023 & 40024 Setting to change password level 1

40025 & 40026 Setting to change password level 2

30010Can be read to indicate current access level

b) Models with Cyber Security

420008 - 420011 Setting to change password level 1

420016 - 420019 Setting to change password level 2

420024 - 420027 Setting to change password level 1

3.7.2 Control and support settings

Control and support settings are executed immediately on the write operation.

3.7.3 Protection and disturbance recorder settings

Setting changes to either of these areas are stored in a scratchpad area and will not be used by the relay unless a confirm or an abort operation is performed. Register 40405 can be used either to confirm or abort the setting changes within the scratchpad area. The relay supports four groups of protection settings. The MODBUS addresses for each of the four groups are repeated within the following address ranges:

Group 1 41000 - 42999

Group 2 43000 - 44999

Group 3 45000 - 46999

Group 4 47000 - 48999

In addition to the basic editing of the protection setting groups, the following functions are provided:

- Default values can be restored to a setting group or to all of the relay settings by writing to register 40402.
- It is possible to copy the contents of one setting group to another by writing the source group to register 40406 and the target group to 40407.

The setting changes performed by either of the two operations defined above are made to the scratchpad area. These changes must be confirmed by writing to register 40405.

The active protection setting groups can be selected by writing to register 40404. An illegal data response will be returned if an attempt is made to set the active group to one that has been disabled.

3.8 Date and time format (data type G12)

The date-time data type G12 allows *real* date and time information to be conveyed down to a resolution of 1ms. The structure of the data type is shown in

Table 3-1 and is compliant with the IEC60870-5-4 “Binary Time 2a” format.

The seven bytes of the structure are packed into four 16-bit registers, such that byte 1 is transmitted first, followed by byte 2 through to byte 7, followed by a null (zero) byte to make eight bytes in total. Since register data is usually transmitted in big-endian format (high order byte followed by low order byte), byte 1 will be in the high-order byte position followed by byte 2 in the low-order position for the first register. The last register will contain just byte 7 in the high order position and the low order byte will have a value of zero.

Byte	Bit Position							
	7	6	5	4	3	2	1	0
1	m^7	m^6	m^5	m^4	m^3	m^2	m^1	m^0
2	m^{15}	m^{14}	m^{13}	m^{12}	m^{11}	m^{10}	m^9	m^8
3	IV	R	I^5	I^4	I^3	I^2	I^1	I^0
4	SU	R	R	H^4	H^3	H^2	H^1	H^0
5	W^2	W^1	W^0	D^4	D^3	D^2	D^1	D^0
6	R	R	R	R	M^3	M^2	M^1	M^0
7	R	Y^6	Y^5	Y^4	Y^3	Y^2	Y^1	Y^0

Table 3-1 G12 date & time data type structure

Where:

m = 0…59,999ms

I = 0…59 minutes

H = 0…23 Hours

W = 1…7 Day of week; Monday to Sunday, 0 for not calculated

D = 1…31 Day of Month

M = 1…12 Month of year; January to December

Y = 0…99 Years (year of century)

R = Reserved bit = 0

SU = summertime: 0 = standard time, 1 = summer time

IV = invalid value: 0 = valid, 1 = invalid

range = 0ms…99 years

Since the range of the data type is only 100 years, the century must be deduced. The century is calculated as the one that will produce the nearest time value to the current date. For example: 30-12-99 is 30-12-1999 when received in 1999 & 2000, but is 30-12-2099 when received in 2050. This technique allows 2 digit years to be accurately converted to 4 digits in a ±50 year window around the current datum.

The invalid bit has two applications:

1. It can indicate that the date-time information is considered inaccurate, but is the best information available.
2. Date-time information is not available.

The summertime bit is used to indicate that summertime (day light saving) is being used and, more importantly, to resolve the alias and time discontinuity which occurs when summertime starts and ends. This is important for the correct time correlation of time stamped records.

The day of the week field is optional and if not calculated will be set to zero.

The concept of time zone is not catered for by this data type and hence by the relay. It is up to the end user to determine the time zone utilized by the relay. Normal practice is to use UTC (universal coordinated time), which avoids the complications with day light saving time-stamp correlation's.

3.9 Power & energy measurement data formats (G29 & G125)

The power and energy measurements are available in two data formats; G29 integer format and G125 IEEE754 floating point format. For historical reasons the registers listed in the main part of the "Measurements 2" column of the menu database are of the G29 format. The floating point, G125, versions appear at the end of the column.

3.9.1 Data type G29

Data type G29 consists of three registers. The first register is the per unit power or energy measurement and is of type G28, which is a signed 16 bit quantity. The second and third registers contain a multiplier to convert the per unit value to a real value. The multiplier is of type G27, which is an unsigned 32-bit quantity. Thus, the overall value conveyed by the G29 data type must be calculated as G29 = G28×G27.

The relay calculates the G28 per unit power or energy value as G28 = ((measured secondary quantity)/(CT secondary) × (110V/(VT secondary)). Since data type G28 is a signed 16-bit integer, its dynamic range is constrained to ±32768. This limitation should be borne in mind for the energy measurements, as the G29 value will saturate a long time before the equivalent G125 does.

The associated G27 multiplier is calculated as G27 = (CT primary) × (VT primary/110V) when primary value measurements are selected, and as G27 = (CT secondary) × (VT secondary/110V) when secondary value measurements are selected.

Due to the required truncations from floating point values to integer values in the calculations of the G29 component parts and its limited dynamic range, the use of the G29 values is only recommended when the MODBUS master cannot deal with the G125 IEEE754 floating point equivalents.

> *Note: The G29 values must be read in whole multiples of three registers. It is not possible to read the G28 and G27 parts with separate read commands.*

Example:

For A-Phase Power (Watts) (registers 30300 - 30302) for a 110 V relay, In = 1A, VT ratio = 110 V:110 V and CT ratio = 1A:1A.

Applying A-phase 1A @ 63.51V

A-phase Watts = ((63.51 V × 1A)/In = 1A) × (110/Vn = 110 V) = 63.51 Watts

The G28 part of the value is the truncated per unit quantity, which will be equal to 64 (40h).

The multiplier is derived from the VT and CT ratios set in the relay, with the equation ((CT Primary) × (VT Primary)/110 V). Therefore, the G27 part of the value will equal 1. Hence the overall value of the G29 register set is 64×1 = 64 W

The registers would contain:

30300 - 0040h

30301 - 0000h

30302 - 0001h

Using the previous example with a VT ratio = 110,000V; 110V and CT ratio = 10,000A:1A the G27 multiplier would be 10,000A × 110,000 V/110 = 10,000,000. The overall value of the G29 register set is 64 × 10,000,000 = 640 MW. (Note that there is an actual error of 49 MW in this calculation due to loss of resolution.)

The registers would contain:

30300 - 0040h

30301 - 0098h

30302 - 9680h

3.9.2 Data type G125

Data type G125 is a short float IEEE754 floating point format, which occupies 32 bits in two consecutive registers. The high order byte of the format is in the first (low order) register and the low order byte in the second register.

The value of the G125 measurement is as accurate as the relay's ability to resolve the measurement after it has applied the secondary or primary scaling factors as require. It does not suffer from the truncation errors or dynamic range limitations associated with the G29 data format.

4 IEC 60870-5-103 INTERFACE

The IEC 60870-5-103 interface is a master/slave interface with the relay as the slave device. The relay conforms to compatibility level 2; compatibility level 3 is not supported.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (reset)
- Time synchronization
- Event record extraction
- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

4.1 Physical connection and link layer

Two connection options are available for IEC 60870-5-103, either the rear EIA(RS)485 port or an optional rear fiber optic port. Should the fiber optic port be fitted the selection of the active port can be made via the front panel menu or the front Courier port, however the selection will only be effective following the next relay power up.

For either of the two modes of connection it is possible to select both the relay address and baud rate using the front panel menu/front Courier. Following a change to either of these two settings a reset command is required to re-establish communications, see reset command description below.

4.2 Initialization

Whenever the relay has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The relay will respond to either of the two reset commands (Reset CU or Reset FCB), the difference being that the Reset CU will clear any unsent messages in the relay's transmit buffer.

The relay will respond to the reset command with an identification message ASDU 5, the Cause Of Transmission COT of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the menu database.

In addition to the above identification message, if the relay has been powered up it will also produce a power up event.

4.3 Time synchronization

The relay time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The relay will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send/confirm message then the relay will respond with a confirm. Whether the time-synchronization message is sent as a send confirm or a broadcast (send/no reply) message, a time synchronization Class 1 event will be generated/produced.

If the relay clock is being synchronized using the IRIG-B input then it will not be possible to set the relay time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the relay to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

4.4 Spontaneous events

Events are categorized using the following information:

- Function type
- Information number

The IEC 60870-5-103 profile in the menu database contains a complete listing of all events produced by the relay.

4.5 General interrogation

The GI request can be used to read the status of the relay, the function numbers, and information numbers that will be returned during the GI cycle are indicated in the IEC 60870-5-103 profile in the menu database.

4.6 Cyclic measurements

The relay will produce measured values using ASDU 9 on a cyclical basis, this can be read from the relay using a Class 2 poll (note ADSU 3 is not used). The rate at which the relay produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu/front Courier port and is active immediately following a change.

The measurands transmitted by the relay are sent as a proportion of 2.4 times the rated value of the analog value.

4.7 Commands

A list of the supported commands is contained in the menu database. The relay will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating 'negative acknowledgement'.

4.8 Test mode

It is possible using either the front panel menu or the front Courier port to disable the relay output contacts to allow secondary injection testing to be performed. This is interpreted as 'test mode' by the IEC 60870-5-103 standard. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the relay is in test mode will have a COT of 'test mode'.

4.9 Disturbance records

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

> *Note: IEC 60870-5-103 only supports up to 8 records.*

4.10 Blocking of monitor direction

The relay supports a facility to block messages in the monitor direction and also in the command direction. Messages can be blocked in the monitor and command directions using the menu commands, Communications – CS103 Blocking – Disabled/Monitor Blocking/Command Blocking or DDB signals Monitor Blocked and Command Blocked.

5 DNP3.0 INTERFACE

5.1 DNP3.0 protocol

The descriptions given here are intended to accompany the device profile document that is included in the menu database. The DNP3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP3.0 implementation for the relay. This is the standard format DNP3.0 document that specifies which objects, variations and qualifiers are supported. The device profile document also specifies what data is available from the relay via DNP3.0. The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol, plus some of the features from level 3.

DNP3.0 communication uses the EIA(RS)485 or fiber optic communication port at the rear of the relay. The data format is 1 start bit, 8 data bits, an optional parity bit and 1 stop bit. Parity is configurable (see menu settings below).

5.2 DNP3.0 menu setting

The settings shown below are available in the menu for DNP3.0 in the 'Communications' column.

Setting	Range	Description
Remote Address	0 – 65534	DNP3.0 address of relay (decimal)
Baud Rate	1200, 2400, 4800, 9600, 19200, 38400	Selectable baud rate for DNP3.0 communication
Parity	None, Odd, Even	Parity setting
Time Sync.	Enabled, Disabled	Enables or disables the relay requesting time sync. from the master via IIN bit 4 word 1

5.3 Object 1 binary inputs

Object 1, binary inputs, contains information describing the state of signals within the relay which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and input optos, alarm signals and protection start and trip signals. The 'DDB number' column in the device profile document provides the DDB numbers for the DNP3.0 point data. These can be used to cross-reference to the DDB definition list that is also found in the menu database. The binary input points can also be read as change events via object 2 and object 60 for class 1-3 event data.

5.4 Object 10 binary outputs

Object 10, binary outputs, contains commands that can be operated via DNP3.0. As such the points accept commands of type pulse on [null, trip, close] and latch on/off as detailed in the device profile in the menu database and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

Due to that fact that many of the relay's functions are configurable, it may be the case that some of the object 10 commands described below are not available for operation. In the case of a read from object 10 this will result in the point being reported as off-line and an operate command to object 12 will generate an error response.

Examples of object 10 points that maybe reported as off-line are:

- Activate setting groups - Ensure setting groups are enabled
- CB trip/close - Ensure remote CB control is enabled
- Reset NPS thermal - Ensure NPS thermal protection is enabled
- Reset thermal O/L - Ensure thermal overload protection is enabled
- Reset RTD flags - Ensure RTD Inputs is enabled
- Control Inputs - Ensure control inputs are enabled

5.5 Object 20 binary counters

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from object 20, or as a 'frozen' value from object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding object 21 frozen counter. The freeze and clear function resets the object 20 running counter to zero after freezing its value.

5.6 Object 30 analog input

Object 30, analog inputs, contains information from the relay's measurements columns in the menu. All object 30 points are reported as fixed-point values although they are stored inside the relay in a floating-point format. The conversion to fixed-point format requires the use of a scaling factor, which differs for the various types of data within the relay e.g. current, voltage, phase angle etc. The data types supported are listed at the end of the device profile document with each type allocated a 'D number', i.e. D1, D2, etc. In the object 30 point list each data point has a D number data type assigned to it which defines the scaling factor, default deadband setting and the range and resolution of the deadband setting. The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read via object 32 or object 60 and will be generated for any point whose value has changed by more than the deadband setting since the last time the data value was reported.

Any analog measurement that is unavailable at the time it is read will be reported as offline, e.g. the frequency when the current and voltage frequency is outside the tracking range of the relay or the thermal state when the thermal protection is disabled in the configuration column. Note that all object 30 points are reported as secondary values in DNP3.0 (with respect to CT and VT ratios).

5.7 DNP3.0 configuration using MiCOM S1 Agile

A PC support package for DNP3.0 is available as part of the settings and records module of MiCOM S1 Agile . The S1 module allows configuration of the relay's DNP3.0 response. The PC is connected to the relay via a serial cable to the 9-pin front part of the relay – see Introduction (P44X/EN IT). The configuration data is uploaded from the relay to the PC in a block of compressed format data and downloaded to the relay in a similar manner after modification. The new DNP3.0 configuration takes effect in the relay after the download is complete. The default configuration can be restored at any time by choosing 'All Settings' from the 'Restore Defaults' cell in the menu 'Configuration' column. In S1, the DNP3.0 data is displayed on a three-tabbed screen, one screen each for object 1, 20 and 30. Object 10 is not configurable.

5.7.1 Object 1

For every point included in the device profile document there is a check box for membership of class 0 and radio buttons for class 1, 2 or 3 membership. Any point that is in class 0 must be a member of one of the change event classes 1, 2 or 3.

Points that are configured out of class 0 are by default not capable of generating change events. Furthermore, points that are not part of class 0 are effectively removed from the DNP3.0 response by renumbering the points that are in class 0 into a contiguous list starting at point number 0. The renumbered point numbers are shown at the left-hand side of the screen in S1 and can be printed out to form a revised device profile for the relay. This mechanism allows best use of available bandwidth by only reporting the data points required by the user when a poll for all points is made.

5.7.2 Object 20

The running counter value of object 20 points can be configured to be in or out of class 0. Any running counter that is in class 0 can have its frozen value selected to be in or out of the DNP3.0 response, but a frozen counter cannot be included without the corresponding running counter. As with object 1, the class 0 response will be renumbered into a contiguous list of points based on the selection of running counters. The frozen counters will also be renumbered based on the selection; note that if some of the counters that are selected as running are not also selected as frozen then the renumbering will result in the frozen

counters having different point numbers to their running counterparts. For example, object 20 point 3 (running counter) might have its frozen value reported as object 21 point 1.

5.7.3 Object 30

For the analog inputs, object 30, the same selection options for classes 0, 1, 2 and 3 are available as for object 1. In addition to these options, which behave in exactly the same way as for object 1, it is possible to change the deadband setting for each point. The minimum and maximum values and the resolution of the deadband settings are defined in the device profile document; MiCOM S1 Agile will allow the deadband to be set to any value within these constraints.

6 IEC 61850 ETHERNET INTERFACE

6.1 Introduction

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security which is essential in substations today.

The MiCOM protection relays can integrate with the PACiS substation control systems, to complete Alstom Grid offers of a full IEC 61850 solution for the substation. The majority of MiCOM Px4x relay types can be supplied with Ethernet, in addition to traditional serial protocols. Relays which have already been delivered with UCA2.0 on Ethernet can be easily upgraded to IEC 61850.

6.2 What is IEC 61850?

IEC 61850 is an international standard, comprising 14 parts, which defines a communication architecture for substations.

The standard defines and offers much more than just a protocol. It provides:

- Standardized models for IEDs and other equipment within the substation
- Standardized communication services (the methods used to access and exchange data)
- Standardized formats for configuration files
- Peer-to-peer (e.g. relay to relay) communication

The standard includes mapping of data onto Ethernet. Using Ethernet in the substation offers many advantages, most significantly including:

- High-speed data rates (currently 100 Mbits/s, rather than 10’s of kbits/s or less used by most serial protocols)
- Multiple masters (called “clients”)
- Ethernet is an open standard in every-day use

Alstom Grid has been involved in the Working Groups which formed the standard, building on experience gained with UCA2.0, the predecessor of IEC 61850.

6.2.1 Interoperability

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs. This responds to the utilities’ desire of having easier integration for different vendors’ products, i.e. interoperability. It means that data is accessed in the same manner in different IEDs from either the same or different IED vendors, even though, for example, the protection algorithms of different vendors’ relay types remain different.

When a device is described as IEC 61850-compliant, this does not mean that it is interchangeable, but does mean that it is interoperable. You cannot simply replace one product with another, however the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able very quickly integrate a new device without the need for mapping of all of the new data. IEC 61850 will inevitably bring improved substation communications and interoperability, at a lower cost to the end user.

6.2.2 The data model

To ease understanding, the data model of any IEC 61850 IED can be viewed as a hierarchy of information. The categories and naming of this information is standardized in the IEC 61850 specification.

The levels of this hierarchy can be described as follows:

– Physical Device	– Identifies the actual IED within a system. Typically t the device's name or IP address can be used (for e example **Feeder_1** or **10.0.0.2**).
– Logical Device	– Identifies groups of related Logical Nodes within t the Physical Device. For the MiCOM relays, 5 Logi Logical Devices exist: **Control, Measurements, Protection, Records, System**.
– Wrapper/Logical Node Instance	– Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
– Data Object	– This next layer is used to identify the type of data you will be presented with. For example, **Pos** (position) of Logical Node type **XCBR**.
– Data Attribute	– This is the actual data (measurement value, status, description, etc.). For example, **stVal** (status value) indicating actual position of circuit breaker for Data Object type **Pos** of Logical Node type **XCBR**.

6.3 IEC 61850 in MiCOM relays

IEC 61850 is implemented in MiCOM relays by use of a separate Ethernet card. This card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection.

In order to communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 "client" (or master), for example a PACiS computer (MiCOM C264) or HMI, or
- An "MMS browser", with which the full data model can be retrieved from the IED, without any prior knowledge

6.3.1 Capability

The IEC 61850 interface provides the following capabilities:

1. Read access to measurements

   All measurands are presented using the measurement Logical Nodes, in the 'Measurements' Logical Device. Reported measurement values are refreshed by the relay once per second, in line with the relay user interface.

2. Generation of unbuffered reports on change of status/measurement

   Unbuffered reports, when enabled, report any change of state in statuses and/or measurements (according to deadband settings).

3. Support for time synchronization over an Ethernet link

   Time synchronization is supported using SNTP (Simple Network Time Protocol); this protocol is used to synchronize the internal real time clock of the relays.

4. GOOSE peer-to-peer communication

   GOOSE communications of statuses are included as part of the IEC 61850 implementation.Please see section 6.6 for more details.

5. Disturbance record extraction

   Extraction of disturbance records, by file transfer, is supported by the MiCOM relays.

The record is extracted as an ASCII format COMTRADE file.

Setting changes (e.g. of protection settings) are not supported in the current IEC 61850 implementation. In order to keep this process as simple as possible, such setting changes are done using MiCOM S1 Agile Settings & Records program. This can be done as previously using the front port serial connection of the relay, or now optionally over the Ethernet link if preferred (this is known as “tunneling”).

6.3.2 IEC 61850 Configuration

One of the main objectives of IEC 61850 is to allow IEDs to be directly configured from a configuration file generated at system configuration time. At the system configuration level, the capabilities of the IED are determined from an IED capability description file (ICD) which is provided with the product. Using a collection of these ICD files from varying products, the entire protection of a substation can be designed, configured and tested (using simulation tools) before the product is even installed into the substation.

To aid in this process, the MiCOM S1 Agile Support Software provides an IED Configurator tool which allows the pre-configured IEC 61850 configuration file (an SCD file or CID file) to be imported and transferred to the IED. Alongside this, the requirements of manual configuration are satisfied by allowing the manual creation of configuration files for MiCOM relays based on their original IED capability description (ICD file).

Other features include the extraction of configuration data for viewing and editing, and a sophisticated error checking sequence which ensures that the configuration data is valid for sending to the IED and that the IED will function within the context of the substation.

To aid the user, some configuration data is available in the ‘IED CONFIGURATOR’ column of the relay user interface, allowing read-only access to basic configuration data.

6.3.2.1 Configuration Banks

To promote version management and minimize down-time during system upgrades and maintenance, the MiCOM relays have incorporated a mechanism consisting of multiple configuration banks. These configuration banks are categorized as:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the relay is automatically stored into the inactive configuration bank, therefore not immediately affecting the current configuration. Both active and inactive configuration banks can be extracted at anytime.

When the upgrade or maintenance stage is complete, the IED Configurator tool can be used to transmit a command (to a single IED) authorizing the activation of the new configuration contained in the inactive configuration bank, by switching the active and inactive configuration banks. This technique ensures that the system down-time is minimized to the start-up time of the new configuration. The capability to switch the configuration banks is also available via the ‘IED CONFIGURATOR’ column.

For version management, data is available in the ‘IED CONFIGURATOR’ column in the relay user interface, displaying the SCL Name and Revision attributes of both configuration banks.

6.3.2.2 Network connectivity

Note:	*This section presumes a prior knowledge of IP addressing and related topics. Further details on this topic may be found on the Internet (search for IP Configuration) and in numerous relevant books.*

Configuration of the relay IP parameters (IP Address, Subnet Mask, Gateway) and SNTP time synchronization parameters (SNTP Server 1, SNTP Server 2) is performed by the IED Configurator tool, so if these parameters are not available via an SCL file, they must be configured manually.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications will operate in an indeterminate way. However, the relay will check for a

conflict on every IP configuration change and at power up. An alarm will be raised if an IP conflict is detected.

The relay can be configured to accept data from networks other than the local network by using the 'Gateway' setting.

6.4 The data model of MiCOM relays

The data model naming adopted in Px40 relays has been standardized for consistency. Hence the Logical Nodes are allocated to one of the five Logical Devices, as appropriate, and the wrapper names used to instantiate Logical Nodes are consistent between Px40 relays.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available separately. The MICS document provides lists of Logical Device definitions, Logical Node definitions, Common Data Class and Attribute definitions, Enumeration definitions, and MMS data type conversions. It generally follows the format used in Parts 7-3 and 7-4 of the IEC 61850 standard.

6.5 The communication services of MiCOM relays

The IEC 61850 communication services which are implemented in Px40 relays are described in the Protocol Implementation Conformance Statement (PICS) document, which is available separately. The PICS document provides the Abstract Communication Service Interface (ACSI) conformance statements as defined in Annex A of Part 7-2 of the IEC 61850 standard.

6.6 Peer-to-peer (GSE) communications

The implementation of IEC 61850 Generic Substation Event (GSE) sets the way for cheaper and faster inter-relay communications. The generic substation event model provides the possibility for a fast and reliable system-wide distribution of input and output data values. The generic substation event model is based on the concept of an autonomous decentralization, providing an efficient method allowing the simultaneous delivery of the same generic substation event information to more than one physical device through the use of multicast services.

The use of multicast messaging means that IEC 61850 GOOSE uses a publisher-subscriber system to transfer information around the network*. When a device detects a change in one of its monitored status points it publishes (i.e. sends) a new message. Any device that is interested in the information subscribes (i.e. listens) to the data it contains.

*Note: * Multicast messages cannot be routed across networks without specialized equipment.*

Each new message is re-transmitted at user-configurable intervals until the maximum interval is reached, in order to overcome possible corruption due to interference, and collisions. In practice, the parameters which control the message transmission cannot be calculated. Time must be allocated to the testing of GSE schemes before or during commissioning, in just the same way a hardwired scheme must be tested.

6.6.1 Scope

A maximum of 32 virtual inputs are available within the PSL which can be mapped directly to a published dataset in a GOOSE message (only 1 fixed dataset is supported). All published GOOSE signals are BOOLEAN values.

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the 32 virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

The MiCOM relay can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2

- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

6.6.2 IEC 61850 GOOSE configuration

All GOOSE configuration is performed via the IED Configurator tool available within the MiCOM S1 Agile Support Software.

All GOOSE publishing configuration can be found under the 'GOOSE Publishing' tab in the configuration editor window. All GOOSE subscription configuration can be found under the 'External Binding' tab in the configuration editor window. Care should be taken to ensure that the configuration is correct, to ensure efficient GOOSE scheme operation.

Settings to enable GOOSE signalling and to apply Test Mode are available via the relay user interface.

6.7 Ethernet functionality

Settings relating to a failed Ethernet link are available in the 'COMMUNICATIONS' column of the relay user interface.

6.7.1 Ethernet disconnection

IEC 61850 'associations' are unique and made to the relay between the client (master) and server (IEC 61850 device). In the event that the Ethernet is disconnected, such associations are lost, and will need to be re-established by the client. The TCP_KEEPALIVE function is implemented in the relay to monitor each association, and terminate any which are no longer active.

6.7.2 Loss of power

The relay allows the re-establishment of associations by the client without a negative impact on the relay's operation after having its power removed. As the relay acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset and must be re-enabled by the client when it next creates the new association to the relay.

SYMBOLS AND GLOSSARY

Logic Symbols used

Symbols	Explanation
&	Logical “AND”: Used in logic diagrams to show an AND-gate function.
Σ	“Sigma”: Used to indicate a summation, such as cumulative current interrupted.
τ	“Tau”: Used to indicate a time constant, often associated with thermal characteristics.
<	Less than: Used to indicate an “under” threshold, such as undercurrent (current dropout).
>	Greater than: Used to indicate an “over” threshold, such as overcurrent (current overload).
Δ	Delta
∠	Angle
1	Logical “OR”: Used in logic diagrams to show an OR-gate function.
1P / 3P	One-pole trip / three-pole trip
21G/21P	Phase and Earth Distance Protection
79/25	Autoreclosure with Check Synchronism
50N/51N	Instantaneous and time-delayed neutral overcurrent protection
27	Undervoltage protection
46BC	Broken conductor detection
49	Thermal overload protection
50BF	Circuit Breaker Failure detection
59	Overvoltage protection
52a/52b	A circuit breaker closed / open auxiliary contact
89a	An Isolator closed auxiliary contact: The contact is in the same state as the breaker primary contacts.
89b	An Isolator open auxiliary contact: The contact is in the opposite state to the breaker primary contacts.
A/R	Abbreviation of “Autoreclose”
ACSI	Abstract Communication Service Interface: In IEC 61850, the ACSI provides abstract definitions of a hierarchical data model and the services that operate on the data.
BAR	Block auto-reclose signal.
BN>	Neutral over susceptance protection element: Reactive component of admittance calculation from neutral current and residual voltage.
BU	Backup: Typically a back-up protection element.
C/O	A changeover contact having normally closed and normally open connections: Often called a “form C” contact.
CB	Circuit breaker.
CB Aux.	Circuit breaker auxiliary contacts: Indication of the breaker open/closed status.
CBF	Circuit breaker failure protection.
CLP	Cold load pick-up.
CR	Carrier Received
CS	Carrier Send
CS	Check synchronism

Symbols	Explanation
CsZ1	Carrier sent by Z1
CT	Current transformer.
CTRL.	Abbreviation of “Control”: As used for the Control Inputs function.
CTS	Current transformer supervision (to detect CT input failure.)
CVMR	Start and Convergency
CVT	Capacitive Voltage Transformer supervision (Voltage dividers capacitors failure.)
CZ	Abbreviation of “Check Zone”: Zone taking into account only the feeders.
DDB	Digital data bus within the programmable scheme logic: A logic point that has a zero or 1 status. DDB signals are mapped in logic to customize the relay’s operation.
DEF	Directional earth fault protection: A directionalised ground fault aided scheme.
Df/dt	Rate of change of frequency protection (ROCOF).
Dly	Time delay.
DNP	Distributed Network Protocol
DR	Abbreviation of “Disturbance Record”
DT	Abbreviation of “Definite Time”: An element which always responds with the same constant time delay on operation.
DZ	Abbreviation of “Dead Zone”: Area between a CT and an open breaker or an open isolator.
E/F	Earth fault: Directly equivalent to ground fault.
F<	An underfrequency element: Could be labelled 81U in ANSI terminology.
F>	An overfrequency element: Could be labelled 81O in ANSI terminology.
FLC	Full load current: The nominal rated current for the circuit.
Flt.	Abbreviation of “Fault”: Typically used to indicate faulted phase selection.
FN	Function.
FSK	Frequency Shift Keyed
Fwd.	Indicates an element responding to a flow in the “Forward” direction.
GN>	Neutral over conductance protection element: Real component of admittance calculation from neutral current and residual voltage.
Gnd.	Abbreviation of “Ground”: Used in distance settings to identify settings that relate to ground (earth) faults.
GOOSE	Generic Object Oriented Substation Event: In IEC 61850, a specific definition of a type of generic substation event, for peer-peer communication.
GRP.	Abbreviation of “Group”: Typically an alternative setting group.
GSE	Generic Substation Event: In IEC 61850, the generic substation event model provides the possibility for a fast and reliable system-wide distribution of input and output data values (peer-peer communication).
HMI	Human Machine Interface: The graphical user interface of the control system.
I	Current.

Symbols	Explanation
I^	Current raised to a power: Such as when breaker statistics monitor the square of ruptured current squared (^ power = 2).
I/O	Abbreviation of “Inputs and Outputs”: Used in connection with the number of optocoupled inputs and output contacts within the relay.
I/P	Abbreviation of “Input”.
I<	An undercurrent element: Responds to current dropout.
I>	An overcurrent element: Detects phase faults; Optionally used by the 50BF protection.
I>1	First stage of phase overcurrent protection: Could be labelled 51-1 in ANSI terminology.
I>2	Second stage of phase overcurrent protection: Could be labelled 51-2 in ANSI terminology.
I>3	Third stage of phase overcurrent protection: Could be labelled 51-3 in ANSI terminology.
I>4	Fourth stage of phase overcurrent protection: Could be labelled 51-4 in ANSI terminology.
I>BB	Minimum pick-up phase threshold for the local trip order confirmation.
I>DZ	Minimum pick-up phase threshold for the Dead Zone protection.
I_0	Zero sequence current: Equals one third of the measured neutral/residual current.
I_1	Positive sequence current.
I_2	Negative sequence current.
I2>	Negative sequence overcurrent protection (NPS element).
I2pol	Negative sequence polarizing current.
IA	Phase A current: Might be phase L1, red phase. or other, in customer terminology.
IB	Phase B current: Might be phase L2, yellow phase. or other, in customer terminology.
IbiasPh> Cur.	SDEF blocking bias current threshold.
IC	Phase C current: Might be phase L3, blue phase. or other, in customer terminology.
ID	Abbreviation of “Identifier”: Often a label used to track a software version installed.
ID>1	Minimum pick-up phase circuitry fault threshold.
ID>2	Minimum pick-up differential phase element for all the zones.
IDCZ>2	Minimum pick-up differential phase element for the Check Zone.
IDMT	Inverse definite minimum time: A characteristic whose trip time depends on the measured input (e.g. current) according to an inverse-time curve.
IDN>1	Minimum pick-up neutral circuitry fault threshold.
IDN>2	Minimum pick-up differential neutral element for all the zones.
IDNCZ>2	Minimum pick-up differential neutral element for the Check Zone.
IDZ	Minimum pick-up differential neutral element for the Check Zone.
IEC	International Electrotechnical Commission (organization that prepares and publishes International Standards for all electrical, electronic and related technologies)

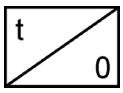
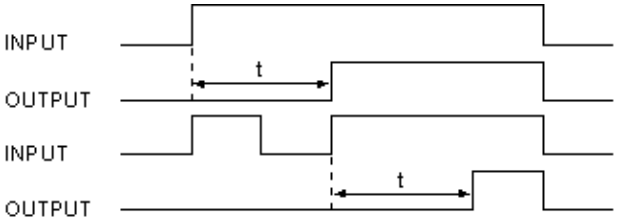
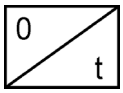
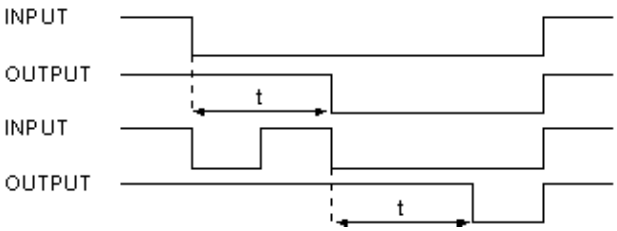
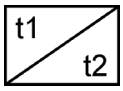
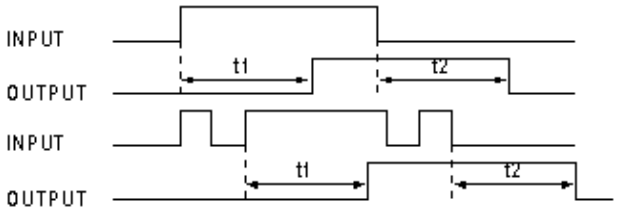
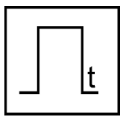
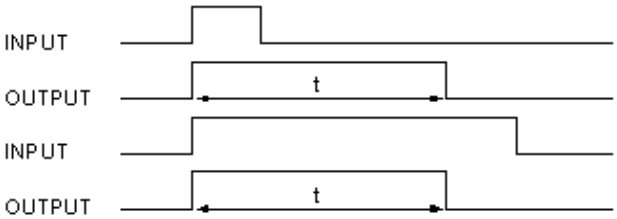
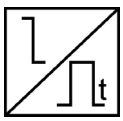
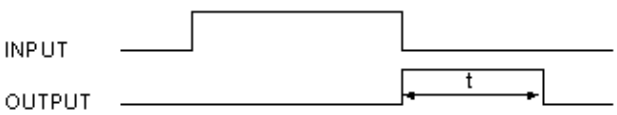
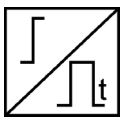
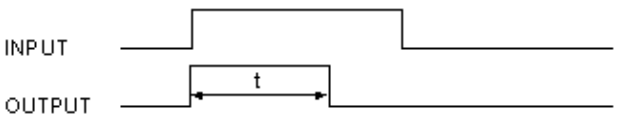
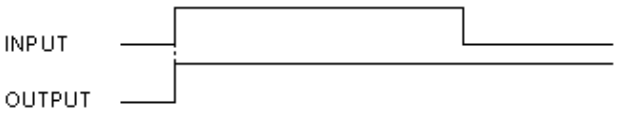
Symbols	Explanation
IED	Intelligent Electronic Device: For example a MiCOM relay
In	The rated nominal current of the relay: Software selectable as 1 amp or 5 amps to match the line CT input.
IN	Neutral current, or residual current: This results from an internal summation of the three measured phase currents.
IN>	A neutral (residual) overcurrent element: Detects earth/ground faults.
IN>1	First stage of ground overcurrent protection: Could be labelled 51N-1 in ANSI terminology.
IN>2	Second stage of ground overcurrent protection: Could be labelled 51N-2 in ANSI terminology.
IN>BB	Minimum pick-up neutral threshold for the local trip order confirmation.
IN>DZ	Minimum pick-up neutral threshold for the Dead Zone protection.
Inh	An inhibit signal.
Inst.	An element with “instantaneous” operation: i.e. having no deliberate time delay.
IRIG-B	IRIG-B Standard (Inter-Range Instrumentation Group)
ISEF>	Sensitive earth fault overcurrent element.
K1	Slope of the phase circuitry fault function.
K2	Slope of the differential phase element for all the zones.
KCZ	Slope of the differential phase element for the Check Zone.
KN1	Slope of the neutral circuitry fault function.
KN2	Slope of the differential neutral element for all the zones.
KNCZ	Slope of the differential neutral element for the Check Zone.
KZ	Residual compensation factor: Ensuring correct reach for ground distance elements. kZ1 (for Z1 and Zone X), kZ2 (for zone 2), kZ3/Z4 (shared by zones 3 and 4), kZp (Zone P), ZQ (for zone Q).
LCD	Liquid crystal display: The front-panel text display on the relay.
LD	Abbreviation of “Level Detector”: An element responding to a current or voltage below its set threshold.
LED	Light emitting diode: Bicolour: Red/black or green/black or orange/black indicator on the relay front-panel. Tricolour: Red/orange/green/black indicator on the relay front-panel.
LN	Logical Nodes Measured voltages and currents converted into digital sampled values and grouped (used with Ethernet NCIT board)
MCB	A “miniature circuit breaker”: Used instead of a fuse to protect VT secondary circuits.
MICS	Model Implementation Conformance Specification: Defines the IEC 61850 data model implemented in an IED.
MMS	Manufacturing Message Specification: A protocol used to transport the data of IEC 61850 across an Ethernet network.
N	Indication of “Neutral” involvement in a fault: i.e. a ground (earth) fault.
N/A	Not applicable.
N/C	A normally closed or “break” contact: Often called a “form B” contact.

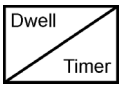
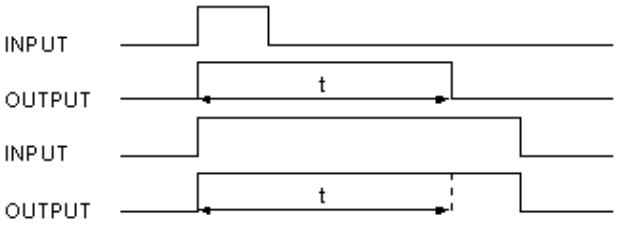
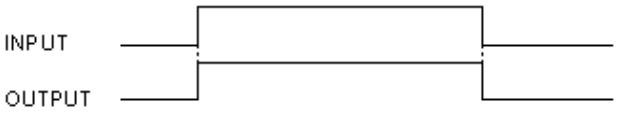
Symbols	Explanation
N/O	A normally open or “make” contact: Often called a “form A” contact.
NCIT	Non Conventional Instrument Transformer
NIC	Network Interface Card: i.e. the Ethernet card of the IED
NPS	Negative phase sequence.
NVD	Neutral voltage displacement: Equivalent to residual overvoltage protection.
NXT	Abbreviation of “Next”: In connection with hotkey menu navigation.
o	A small circle on the input or output of a logic gate: Indicates a NOT (invert) function.
O/C	Abbreviation of “Overcurrent”.
O/P	Abbreviation of “output”.
O/V	Abbreviation of “Overvoltage”
Opto	An optocoupled logic input: Alternative terminology: binary input.
P1	Used in IEC terminology to identify the primary CT terminal polarity: Replace by a dot when using ANSI standards.
P2	Used in IEC terminology to identify the primary CT terminal polarity: The non-dot terminal.
PCB	Printed circuit board.
Ph	Abbreviation of “Phase”: Used in distance settings to identify settings that relate to phase-phase faults.
PICS	Protocol Implementation Conformance Specification: Defines the IEC 61850 services implemented in an IED, with reference to the ACSI.
PLC	Power Line Carrier or Power Line Communication
PN>	Wattmetric earth fault protection: Calculated using residual voltage and current quantities.
Pol	Abbreviation of “Polarizing”: Typically the polarizing voltage used in making directional decisions.
POP	Permissive Overreach Protection
PUP	Permissive Underreach Protection
BOP	Blocking Overreach Protection
PCB	Printed Circuit Board
PSL	Programmable Scheme Logic: The part of the relay’s logic configuration that can be modified by the user, using the graphical editor within MiCOM S1 Studio software.
Qx	Isolator number x (from 1 to 6).
R	A resistance.
R Gnd.	A distance zone resistive reach setting: Used for ground (earth) faults.
RBN	Lead burden for the neutral.
RBPh	Lead burden for the phases.
RCA	Abbreviation of “Relay Characteristic Angle”: The centre of the directional characteristic.
RCT	Current Transformer secondary resistance.
REF	Restricted earth fault protection.
Rev.	Indicates an element responding to a flow in the “reverse” direction.

Symbols	Explanation
RMS	The equivalent a.c. current: Taking into account the fundamental, plus the equivalent heating effect of any harmonics. Abbreviation of “root mean square”.
RP	Abbreviation of “Rear Port”: The communication ports on the rear of the relay.
Rx	Abbreviation of “Receive”: Typically used to indicate a communication receive line/pin.
S1	Used in IEC terminology to identify the secondary CT terminal polarity: Replace by a dot when using ANSI standards.
S2	Used in IEC terminology to identify the secondary CT terminal polarity: The non-dot terminal.
SCADA	Supervisory Control and Data Acquisition remote communications interfaces of the MiCOM relay
SCL	Substation Configuration Language: In IEC 61850, the definition of the configuration files.
SCSM	Specific Communication Service Mappings: In IEC 61850, the SCSMs define the actual information exchange mechanisms currently used (e.g. MMS).
SDEF	Sensitive Differential Earth Fault Protection.
SEF	Sensitive Earth Fault Protection.
SNTP	Simple Network Time Protocol used to synchronize the internal real time clock of the relays
SOTF	Switch On To Fault
SSD	Solid State Device
SV	Sample Value Digital values obtained from the analog to digital conversion of a measured voltages and currents (used with Ethernet NCIT board)
T	A time delay.
TCS	Trip circuit supervision.
TD	The time dial multiplier setting: Applied to inverse-time curves (ANSI/IEEE).
TE	A standard for measuring the width of a relay case: One inch = 5TE units.
TMS	The Time Multiplier Setting applied to inverse-time curves (IEC).
TOR	Trip On Reclose
tZ	
Tx	Abbreviation of “Transmit”: Typically used to indicate a communication transmit line/pin.
V	Voltage.
V<	An undervoltage element.
V<1	First stage of undervoltage protection: Could be labelled 27-1 in ANSI terminology.
V<2	Second stage of undervoltage protection: Could be labelled 27-2 in ANSI terminology.
V>	An overvoltage element.
V>1	First stage of overvoltage protection: Could be labelled 59-1 in ANSI terminology.
V>2	Second stage of overvoltage protection: Could be labelled 59-2 in ANSI terminology.

Symbols	Explanation
V_0	Zero sequence voltage: Equals one third of the measured neutral/residual voltage.
V_1	Positive sequence voltage.
V_2	Negative sequence voltage.
V2pol	Negative sequence polarizing voltage.
VA	Phase A voltage: Might be phase L1, red phase. or other, in customer terminology.
VB	Phase B voltage: Might be phase L2, yellow phase. or other, in customer terminology.
VC	Phase C voltage: Might be phase L3, blue phase. or other, in customer terminology.
VCO	Voltage controlled overcurrent element.
Vk	IEC knee point voltage of a current transformer.
Vn	The rated nominal voltage of the relay: To match the line VT input.
VN	Neutral voltage displacement or residual voltage.
VN>1	First stage of residual (neutral) overvoltage protection.
VN>2	Second stage of residual (neutral) overvoltage protection.
Vres.	Neutral voltage displacement or residual voltage.
VT	Voltage transformer.
VTS	Voltage transformer supervision (to detect VT input failure).
Vx	An auxiliary supply voltage: Typically the substation battery voltage used to power the relay.
WI	Weak Infeed
YN>	Neutral overadmittance protection element: Non-directional neutral admittance protection calculated from neutral current and residual voltage.
Z1…ZQ	Zone 1, 2, 3, 4, P or Q.
Z1X	Zone 1 Extended
Z_0	Zero sequence impedance.
Z_1	Positive sequence impedance.
Z_2	Negative sequence impedance.
ZSP	Zero Sequence Power (Earth Fault Protection)

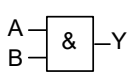
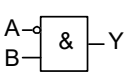
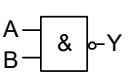
Logic Timers

Logic Symbols	Explanation	Time Chart
	Delay on pick-up timer, t	
	Delay on drop-off timer, t	
	Delay on pick-up/drop-off timer	
	Pulse timer	
	Pulse pick-up falling edge	
	Pulse pick-up raising edge	
	Latch	

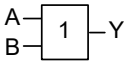
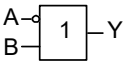
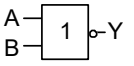
Logic Symbols	Explanation	Time Chart
	Dwell timer	
	**Straight (non latching):** Hold value until input reset signal	

Logic Gates

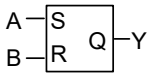
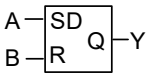
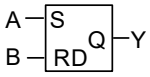
AND GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN A B / OUT Y: 0 0 0; 0 1 0; 1 0 0; 1 1 1		IN A B / OUT Y: 0 0 0; 0 1 1; 1 0 0; 1 1 0		IN A B / OUT Y: 0 0 1; 0 1 1; 1 0 1; 1 1 0

OR GATE

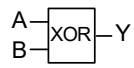
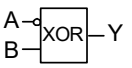
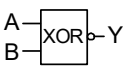
Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN A B / OUT Y: 0 0 0; 0 1 1; 1 0 1; 1 1 1		IN A B / OUT Y: 0 0 1; 0 1 1; 1 0 0; 1 1 1		IN A B / OUT Y: 0 0 1; 0 1 0; 1 0 0; 1 1 0

S – R FLIP-FLOP

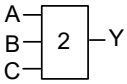
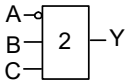
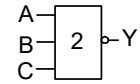
Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
 Standard S-R gate	A B Q_0 Q_1: 0 0 0 0; 0 0 1 1; 0 1 0 0; 0 1 1 0; 1 0 0 1; 1 0 1 1; 1 1 0 0; 1 1 1 1	 SD = Set Dominant	A B Q_0 Q_1: 0 0 0 0; 0 0 1 1; 0 1 0 0; 0 1 1 0; 1 0 0 1; 1 0 1 1; 1 1 0 1; 1 1 1 1	 RD = Reset Dominant	A B Q_0 Q_1: 0 0 0 0; 0 0 1 1; 0 1 0 0; 0 1 1 0; 1 0 0 1; 1 0 1 1; 1 1 0 0; 1 1 1 0

Warning: To avoid ambiguity, do not use the standard S-R gate unless specifically required

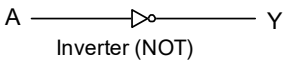
EXCLUSIVE OR GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN A B / OUT Y: 0 0 0; 0 1 1; 1 0 1; 1 1 0		IN A B / OUT Y: 0 0 1; 0 1 1; 1 0 0; 1 1 1		IN A B / OUT Y: 0 0 1; 0 1 0; 1 0 0; 1 1 1

PROGRAMMABLE GATE

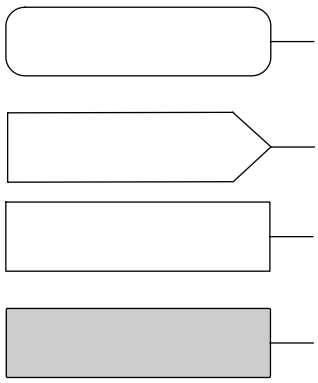
Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
	IN A B C / OUT Y: 0 0 0 0; 0 0 1 0; 0 1 0 0; 0 1 1 1; 1 0 0 0; 1 0 1 1; 1 1 0 1; 1 1 1 1		IN A B C / OUT Y: 0 0 0 0; 0 0 1 1; 0 1 0 1; 0 1 1 1; 1 0 0 0; 1 0 1 0; 1 1 0 0; 1 1 1 1		IN A B C / OUT Y: 0 0 0 1; 0 0 1 1; 0 1 0 1; 0 1 1 0; 1 0 0 1; 1 0 1 0; 1 1 0 0; 1 1 1 0

NOT GATE

Symbol	Truth Table
 Inverter (NOT)	IN A / OUT Y: 0 1; 1 0

P4424ENa

Specific inputs or outputs in this manual:



Internal logic status from the logic of the protection (« the line is dead » or « the pole is dead »)

User setting, adjustment or selection (IHM or MiCOM S1)

Command / logical external status linked to an opto input from the protection, or logical output.

Digital Data Bus (DDB) within the Programmable Scheme Logic (PSL) corresponding to a command, a logical external status or a logical output.

INSTALLATION

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1 RECEIPT OF RELAYS

Protective relays, although generally of robust construction, require careful treatment prior to installation on site. On receipt, relays should be examined immediately to ensure no external damage has been sustained in transit.

If damage has been sustained, a claim should be made to the transport contractor and GE Vernova should be promptly notified.

Relays that are supplied unmounted and not intended for immediate installation should be returned to their protective polythene bags and delivery carton.

Section 3 of this chapter gives more information about the storage of relays.

2 HANDLING OF ELECTRONIC EQUIPMENT

A person's normal movements can easily generate electrostatic potentials of several thousand volts. Discharge of these voltages into semiconductor devices when handling electronic circuits can cause serious damage which, although not always immediately apparent, will reduce the reliability of the circuit. This is particularly important to consider where the circuits use complementary metal oxide semiconductors (CMOS), as is the case with these relays.

The relay's electronic circuits are protected from electrostatic discharge when housed in the case. Do not expose them to risk by removing the front panel or printed circuit boards unnecessarily.

Each printed circuit board incorporates the highest practicable protection for its semiconductor devices. However, if it becomes necessary to remove a printed circuit board, the following precautions should be taken to preserve the high reliability and long life for which the relay has been designed and manufactured.

1. Before removing a printed circuit board, ensure that you are at the same electrostatic potential as the equipment by touching the case.
2. Handle analogue input modules by the front panel, frame or edges of the circuit boards. Printed circuit boards should only be handled by their edges.
   Avoid touching the electronic components, printed circuit tracks or connectors.
3. Do not pass the module to another person without first ensuring you are both at the same electrostatic potential. Shaking hands achieves equipotential.
4. Place the module on an anti-static surface, or on a conducting surface which is at the same potential as yourself.
5. If it is necessary to store or transport printed circuit boards removed from the case, place them individually in electrically conducting anti-static bags.

In the unlikely event that you are making measurements on the internal electronic circuitry of a relay in service, it is preferable that you are earthed to the case with a conductive wrist strap. Wrist straps should have a resistance to ground between 500 kΩ to 10 MΩ. If a wrist strap is not available you should maintain regular contact with the case to prevent a build-up of electrostatic potential. Instrumentation which may be used for making measurements should also be earthed to the case whenever possible.

More information on safe working procedures for all electronic equipment can be found in IEC 61340-5-1. It is strongly recommended that detailed investigations on electronic circuitry or modification work should be carried out in a special handling area such as described in the aforementioned Standard document.

3 STORAGE

If relays are not to be installed immediately upon receipt, they should be stored in a place free from dust and moisture in their original cartons. Where de-humidifier bags have been included in the packing they should be retained. The action of the de-humidifier crystals will be impaired if the bag is exposed to ambient conditions and may be restored by gently heating the bag for about an hour prior to replacing it in the carton.

To prevent battery drain during transportation and storage a battery isolation strip is fitted during manufacture. With the lower access cover open, presence of the battery isolation strip can be checked by a red tab protruding from the positive side.

Care should be taken on subsequent unpacking that any dust which has collected on the carton does not fall inside. In locations of high humidity the carton and packing may become impregnated with moisture and the de-humidifier crystals will lose their efficiency.

Prior to installation, relays should be stored at a temperature of between –40˚C to +70˚C.

4 UNPACKING

Care must be taken when unpacking and installing the relays so that none of the parts are damaged and additional components are not accidentally left in the packing or lost.

> *Note: With the lower access cover open, the red tab of the battery isolation strip will be seen protruding from the positive side of the battery compartment. Do not remove this strip because it prevents battery drain during transportation and storage and will be removed as part of the commissioning tests.*

Relays must only be handled by skilled persons.

The site should be well lit to facilitate inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies to installations which are being carried out at the same time as construction work.

5 RELAY MOUNTING

MiCOM relays are dispatched either individually or as part of a panel/rack assembly.

Individual relays are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres. This information can also be found in the product publication.

Secondary front covers can also be supplied as an option item to prevent unauthorised changing of settings and alarm status. They are available in sizes 40TE (GN0037 001) and 60TE (GN0038 001). Note that the 60TE cover also fits the 80TE case size of the relay.

The design of the relay is such that the fixing holes in the mounting flanges are only accessible when the access covers are open and hidden from sight when the covers are closed.

If a P991 or MMLG test block is to be included, it is recommended that, when viewed from the front, it is positioned on the right-hand side of the relay (or relays) with which it is associated. This minimises the wiring between the relay and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

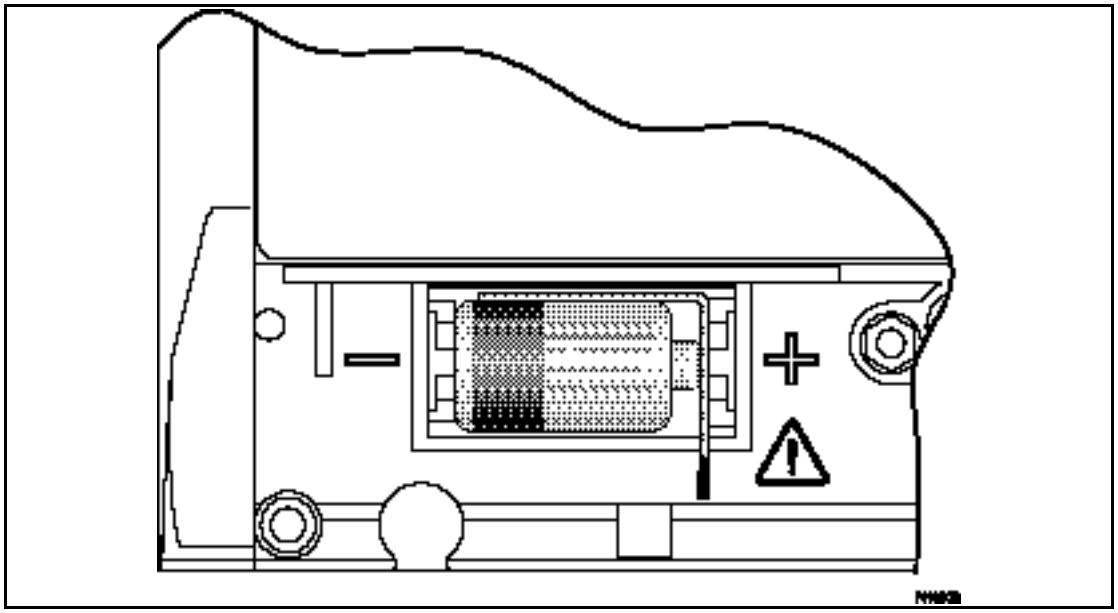


Figure 1 - Location of battery isolation strip

If it is necessary to test correct relay operation during the installation, the battery isolation strip can be removed but should be replaced if commissioning of the scheme is not imminent. This will prevent unnecessary battery drain during transportation to site and installation. The red tab of the isolation strip can be seen protruding from the positive side of the battery compartment when the lower access cover is open. To remove the isolation strip, pull the red tab whilst lightly pressing the battery to prevent it falling out of the compartment. When replacing the battery isolation strip, ensure that the strip is refitted as shown in Figure 1, ie. with the strip behind the battery with the red tab protruding.

5.1 Rack mounting

MiCOM relays may be rack mounted using single tier rack frames (our part number FX0021 001), as shown in Figure 2. These frames have been designed to have dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483mm (19") rack system this enables combinations of widths of case up to a total equivalent of size 80TE to be mounted side by side.

Relays in 80TE cases are also available as direct 19" rack mounting ordering variants, having mounted flanges similar to those shown in Figure 2.

The two horizontal rails of the rack frame have holes drilled at approximately 26mm intervals and the relays are attached via their mounting flanges using M4 Taptite self-tapping screws with captive 3mm thick washers (also known as a SEMS unit).

> *Note: Conventional self-tapping screws, including those supplied for mounting MIDOS relays, have marginally larger heads which can damage the front cover moulding if used.*

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

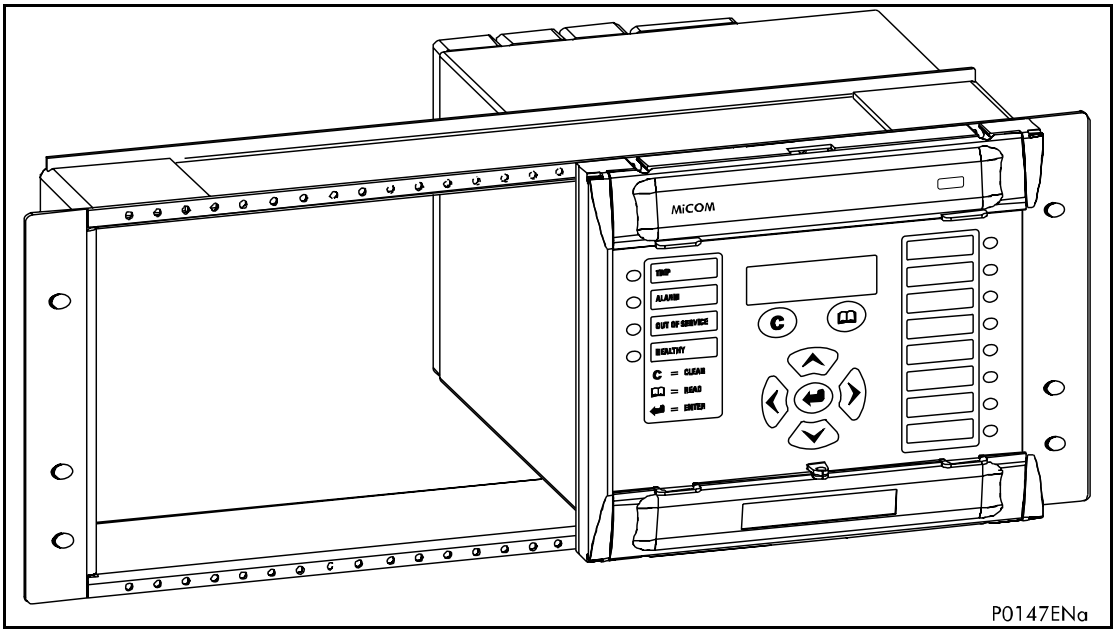


Figure 2 - Rack mounting of relays

Relays can be mechanically grouped into single tier (4U) or multi-tier arrangements by means of the rack frame. This enables schemes using products from the MiCOM and MiDOS product ranges to be pre-wired together prior to mounting.

Where the case size summation is less than 80TE on any tier, or space is to be left for installation of future relays, blanking plates may be used. These plates can also be used to mount ancillary components. Table 1 shows the sizes that can be ordered.

Further details on mounting MiDOS relays can be found in publication R7012, “MiDOS Parts Catalogue and Assembly Instructions”.

Case size summation	Blanking plate part number
5TE	GJ2028 001
10TE	GJ2028 002
15TE	GJ2028 003
20TE	GJ2028 004
25TE	GJ2028 005
30TE	GJ2028 006
35TE	GJ2028 007
40TE	GJ2028 008

Table 1 - Blanking plates

5.2 Panel mounting

The relays can be flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3mm thick washers (also known as a SEMS unit).

Note: Conventional self-tapping screws, including those supplied for mounting MIDOS relays, have marginally larger heads which can damage the front cover moulding if used.

Alternatively tapped holes can be used if the panel has a minimum thickness of 2.5mm.

For applications where relays need to be semi-projection or projection mounted, a range of collars are available.

Where several relays are to mounted in a single cut-out in the panel, it is advised that they are mechanically grouped together horizontally and/or vertically to form rigid assemblies prior to mounting in the panel.

Note: It is not advised that MiCOM relays are fastened using pop rivets as this will not allow the relay to be easily removed from the panel in the future if repair is necessary.

If it is required to mount a relay assembly on a panel complying to BS EN60529 IP52, it will be necessary to fit a metallic sealing strip between adjoining relays (Part no GN2044 001) and a sealing ring selected from Table 2 around the complete assembly.

Width	Single tier	Double tier
10TE	GJ9018 002	GJ9018 018
15TE	GJ9018 003	GJ9018 019
20TE	GJ9018 004	GJ9018 020
25TE	GJ9018 005	GJ9018 021
30TE	GJ9018 006	GJ9018 022
35TE	GJ9018 007	GJ9018 023
40TE	GJ9018 008	GJ9018 024
45TE	GJ9018 009	GJ9018 025
50TE	GJ9018 010	GJ9018 026
55TE	GJ9018 011	GJ9018 027

Width	Single tier	Double tier
60TE	GJ9018 012	GJ9018 028
65TE	GJ9018 013	GJ9018 029
70TE	GJ9018 014	GJ9018 030
75TE	GJ9018 015	GJ9018 031
80TE	GJ9018 016	GJ9018 032

Table 2 - IP52 sealing rings

Further details on mounting MiDOS relays can be found in publication R7012, “MiDOS Parts Catalogue and Assembly Instructions”.

6 RELAY WIRING

This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the MiCOM relay.

6.1 Medium and heavy duty terminal block connections

Loose relays are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per relay terminal.

If required, we can supply M4 90° crimp ring terminals in two different sizes depending on wire size (see Table 3). Each type is available in bags of 100.

Part number	Wire size	Insulation colour
ZB9124 901	0.25 – 1.65 mm^2 (22 – 16AWG)	Red
ZB9124 900	1.04 – 2.63 mm^2 (16 – 14AWG)	Blue

Table 3 - M4 90° crimp ring terminals

* To maintain the terminal block insulation requirements for safety, an insulating sleeve should be fitted over the ring terminal after crimping.

The following minimum wire sizes are recommended:

Current Transformers 2.5 mm^2

Auxiliary Supply, Vx 1.5 mm^2

RS485 Port See separate section

Other circuits 1.0 mm^2

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 using ring terminals that are not pre-insulated. Where it required to only use pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63 mm^2 per ring terminal. If a larger wire size is required, two wires should be used in parallel, each terminated in a separate ring terminal at the relay.

The wire used for all connections to the medium and heavy duty terminal blocks, except the RS485 port, should have a minimum voltage rating of 300 Vrms.

It is recommended that the auxiliary supply wiring should be protected by a 16 A high rupture capacity (HRC) fuse of type NIT or TIA. For safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

6.2 RS485 port

Connections to the RS485 port are made using ring terminals. It is recommended that a 2 core screened cable is used with a maximum total length of 1000m or 200 nF total cable capacitance. A typical cable specification would be:

Each core:	16/0.2 mm copper conductors PVC insulated
Nominal conductor area:	0.5 mm^2 per core
Screen:	Overall braid, PVC sheathed

6.3 IRIG-B connections (if applicable)

The IRIG-B input and BNC connector have a characteristic impedance of 50 Ω. It is recommended that connections between the IRIG-B equipment and the relay are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

6.4 RS232 port

Short term connections to the RS232 port, located behind the bottom access cover, can be made using a screened multi-core communication cable up to 15m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled, D-type male plug. Chapter 2, Section 3.7 of this manual details the pin allocations.

6.5 Download/monitor port

Short term connections to the download/monitor port, located behind the bottom access cover, can be made using a screened 25-core communication cable up to 4m long. The cable should be terminated at the relay end with a 25-way, metal shelled, D-type male plug. Chapter 2, Section 3.7 of this manual details the pin allocations.

6.6 Earth connection

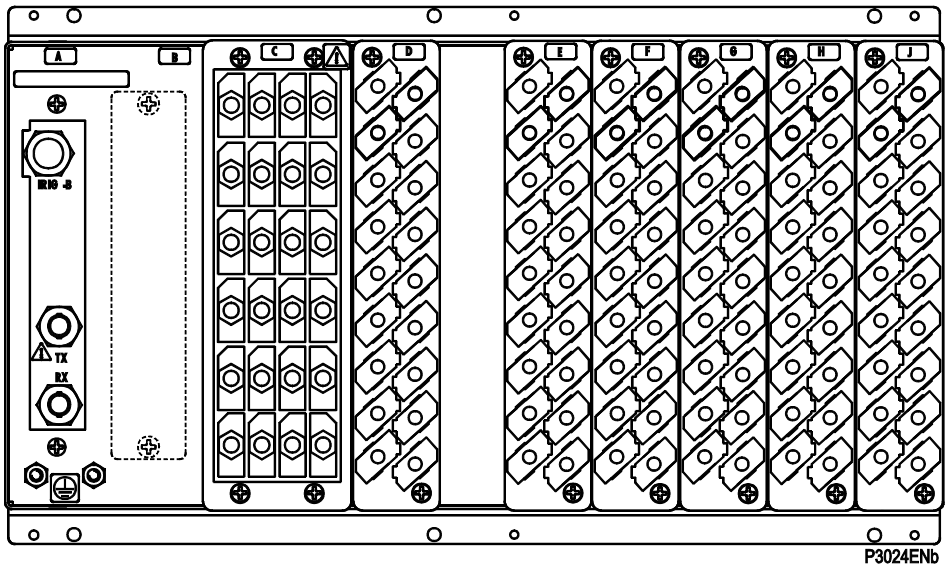
Every relay must be connected to the local earth bar using the M4 earth studs in the bottom left hand corner of the relay case. The minimum recommended wire size is 2.5 mm^2 and should have a ring terminal at the relay end. Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 per wire. If a greater cross-sectional area is required, two parallel connected wires, each terminated in a separate ring terminal at the relay, or a metal earth bar could be used.

Note:	*To prevent any possibility of electrolytic action between brass or copper earth conductors and the rear panel of the relay, precautions should be taken to isolate them from one another. This could be achieved in a number of ways, including placing a nickel-plated or insulating washer between the conductor and the relay case, or using tinned ring terminals.*



Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety and Technical Data sections and the ratings on the equipment's rating label

7 MICOM P442 – REAR VIEW (HARDWARE M)

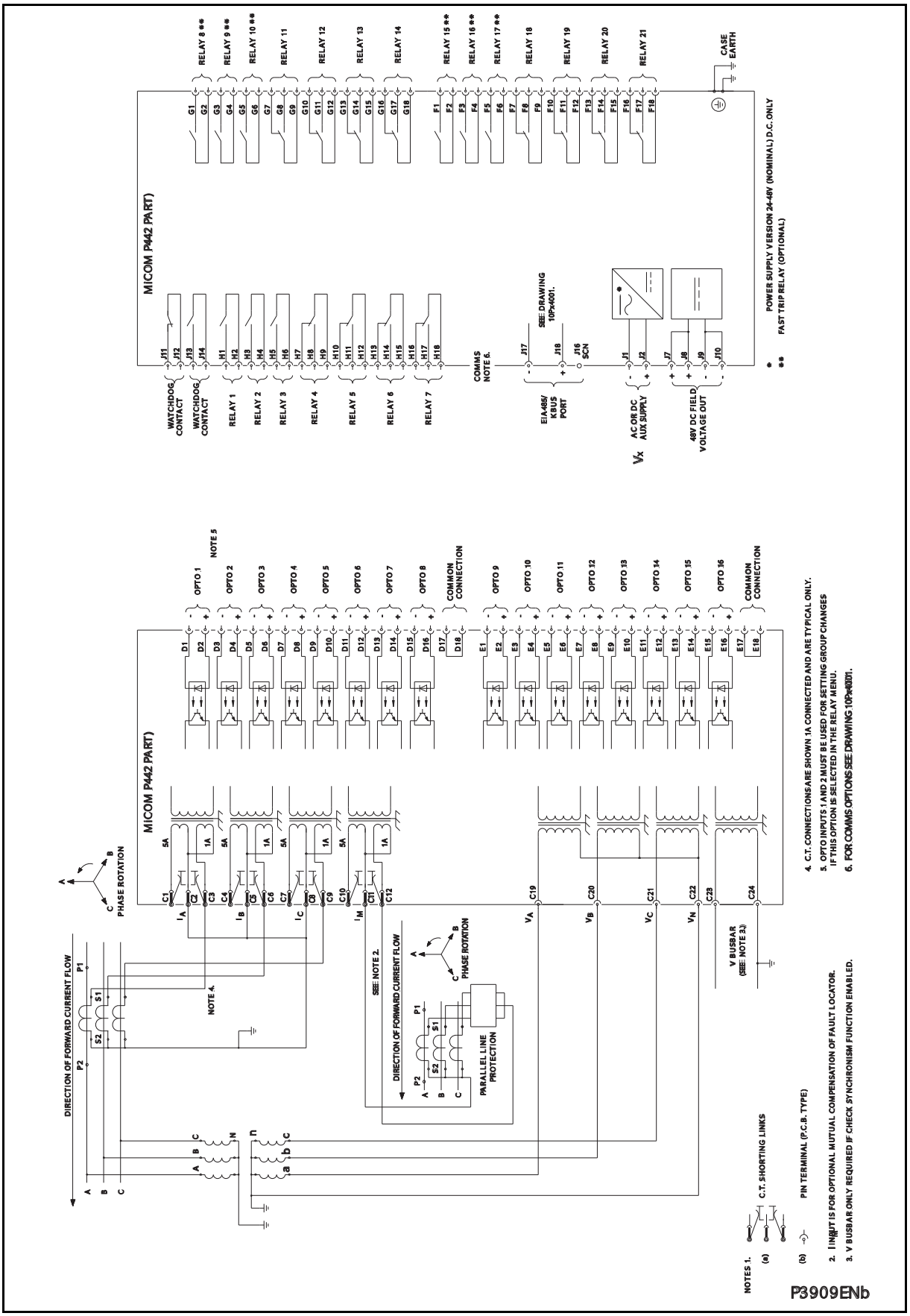


A –	Optional board (1)	F –	Output relay/High Break board (2)
B –	Optional board (1)	G –	Output relay board
C –	Current and voltage input board	F –	Power supply board
D –	Opto-input board		
E –	Opto-input board	* =	option depending on the model

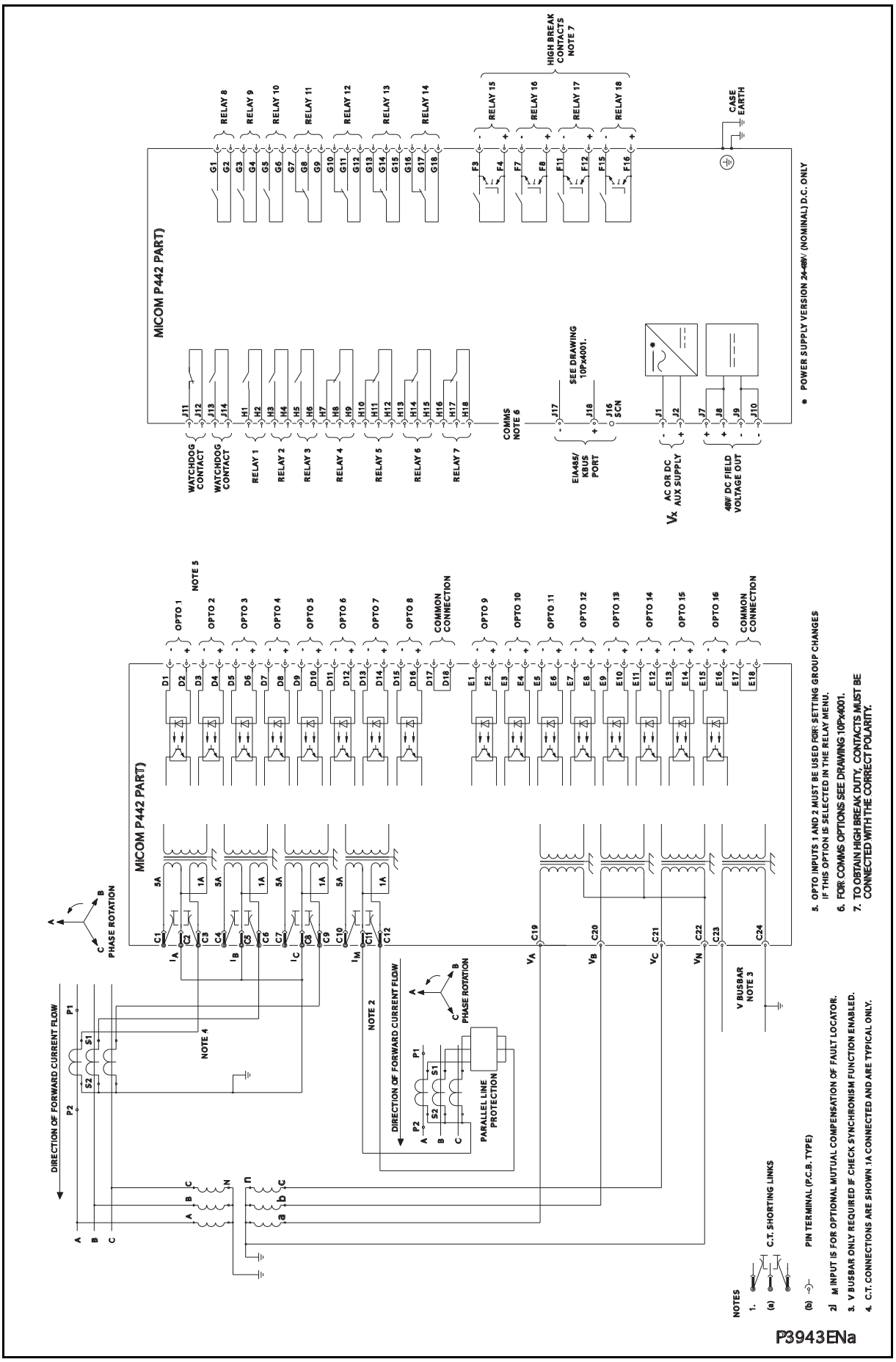
(1) Hardware options:
Refer to Introduction chapter section 3.1 Ordering Options

(2) Models:
Refer to Introduction chapter section 3.1 Ordering Options

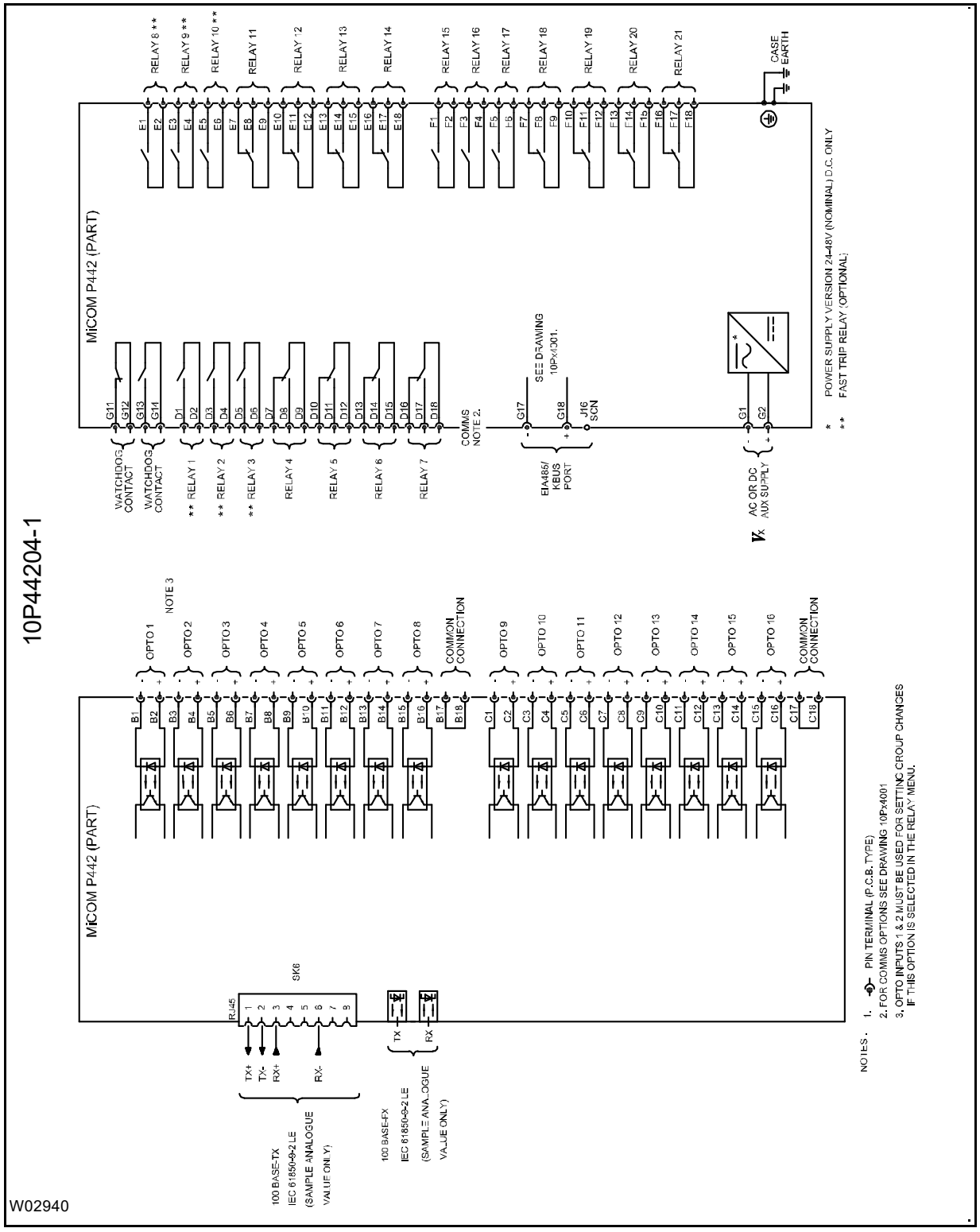
7.1 MICOM P442 with Standard contacts - Wiring Diagram (1/5)



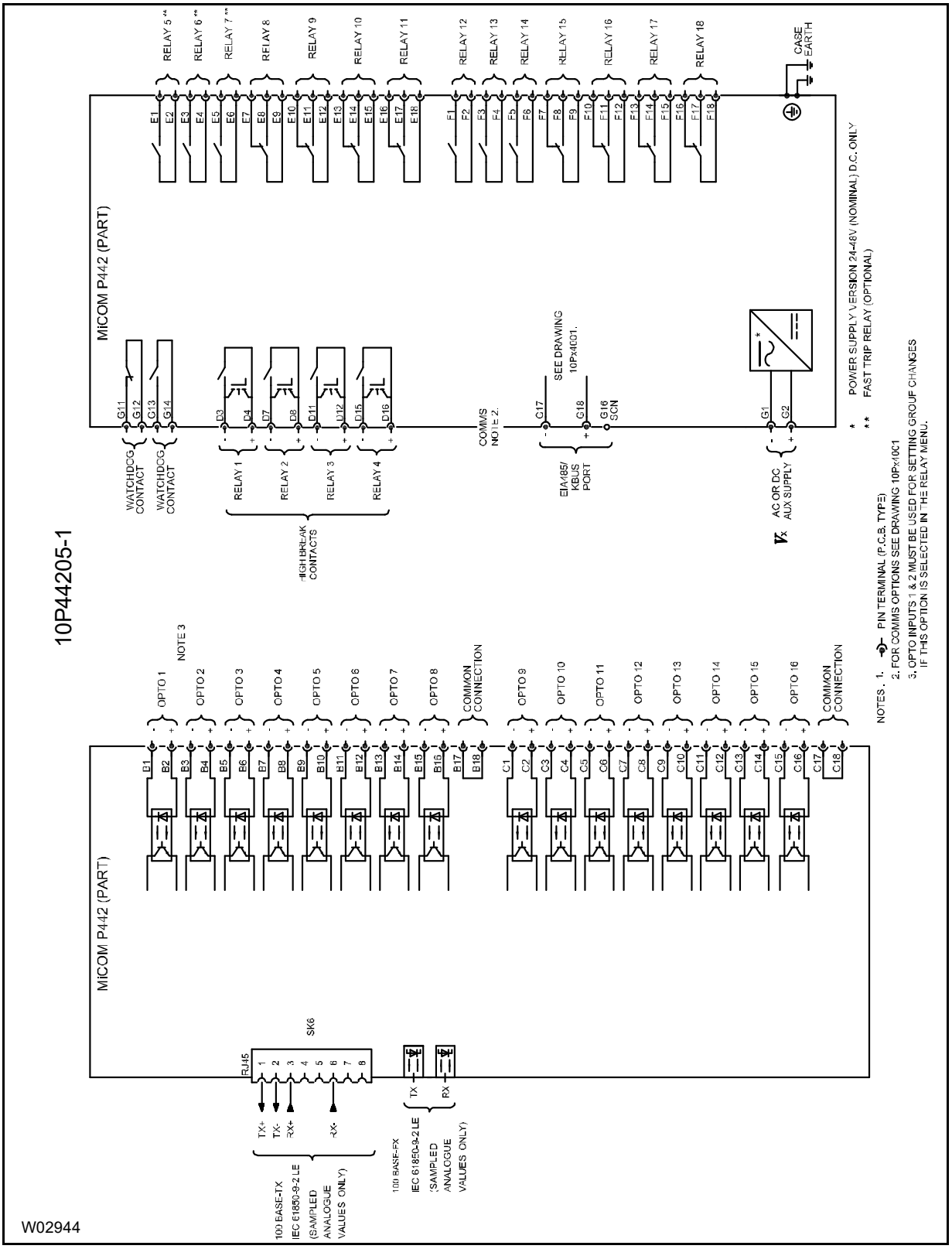
7.2 MICOM P442 with High Break contacts - Wiring Diagram (2/5)



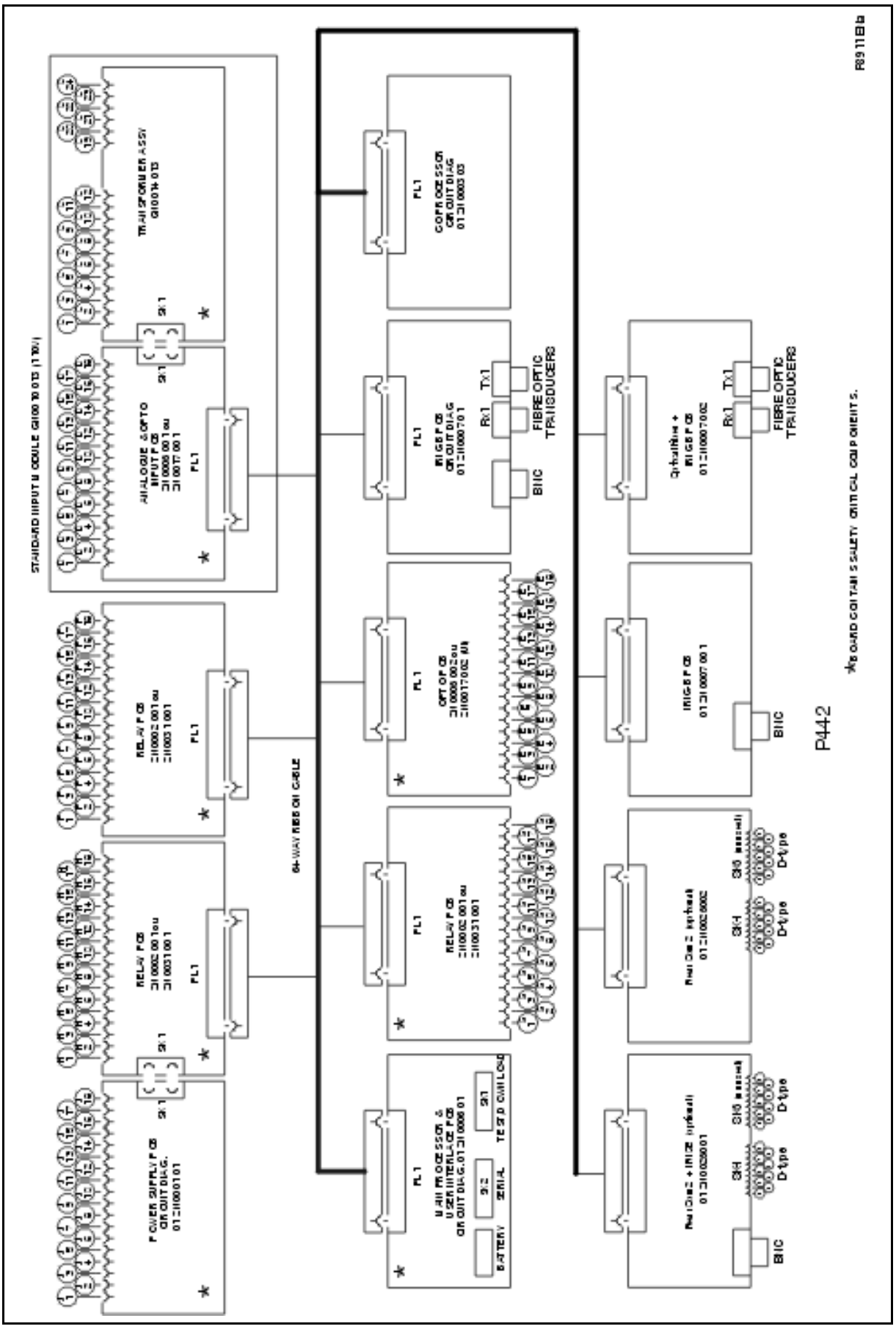
7.3 MICOM P442 with NCIT and Standard contacts - Wiring Diagram (3/5)



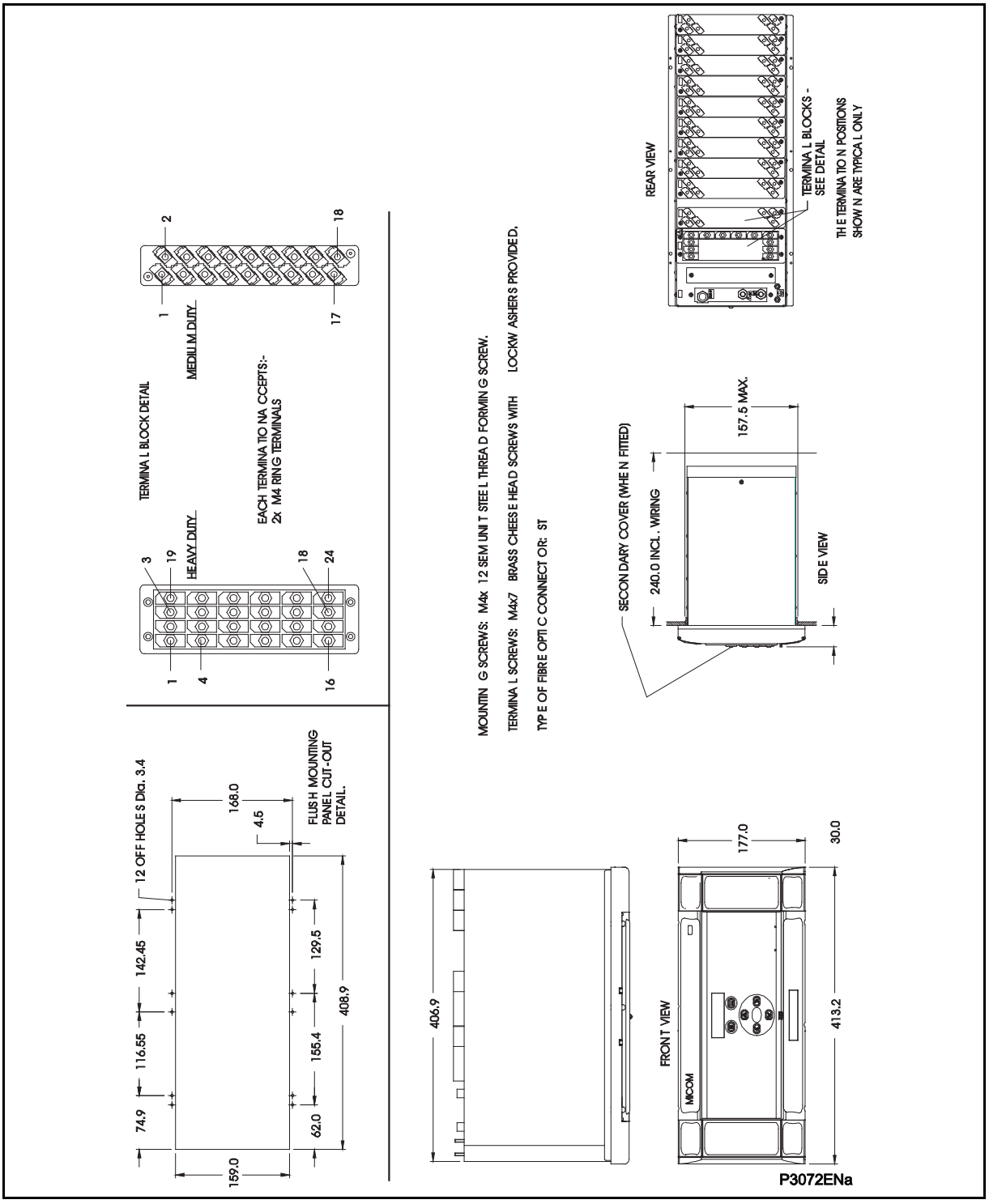
7.4 MICOM P442 with NCIT and High Break contacts - Wiring Diagram (4/5)



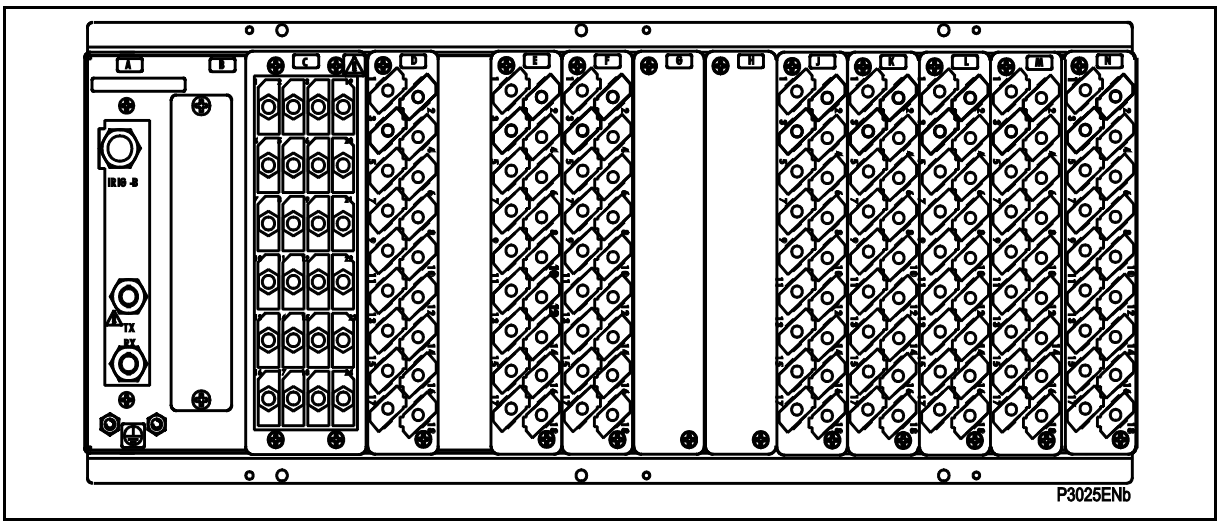
7.5 MICOM P442 – Wiring Diagram (5/5)



8 MiCOM P444 – HARDWARE DESCRIPTION (HARWARE M)



8.1 MiCOM P444 – Rear View

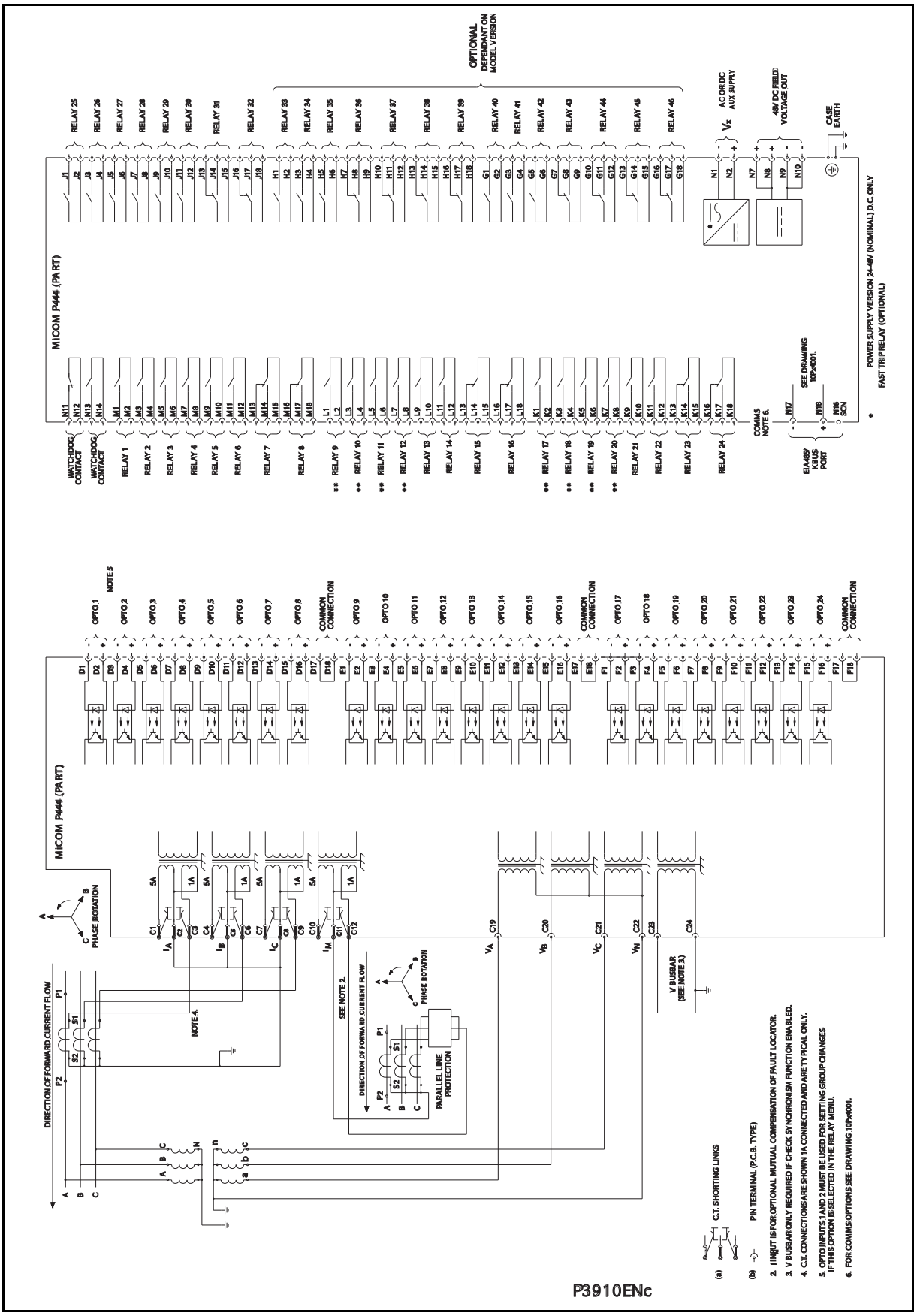


A – Optional board (1)
B – Optional board (1)
C – Current and voltage input board
D – Opto-input board
E – Opto-input board
F – Opto Input board
G – Relay board (2)
H – Relay board
J – Output relay/High Break board (2)
K – Output relay/High Break board (2)
L – Output relay/High Break board (2)
M – Relay board
N – Power supply board

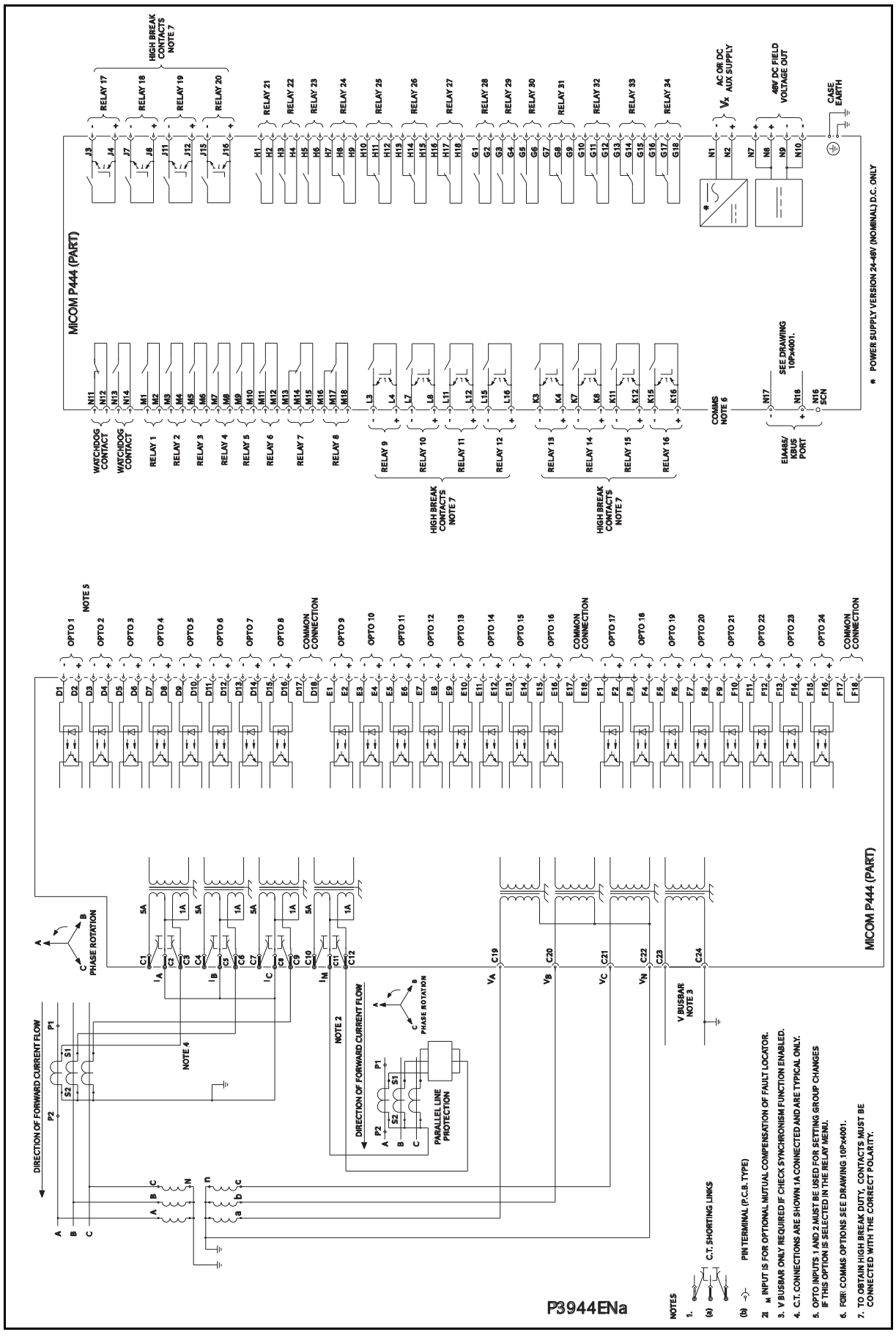
(1) Hardware options:
Refer to Introduction chapter section 3.1 Ordering Options

(2) Models:
Refer to Introduction chapter section 3.1 Ordering Options

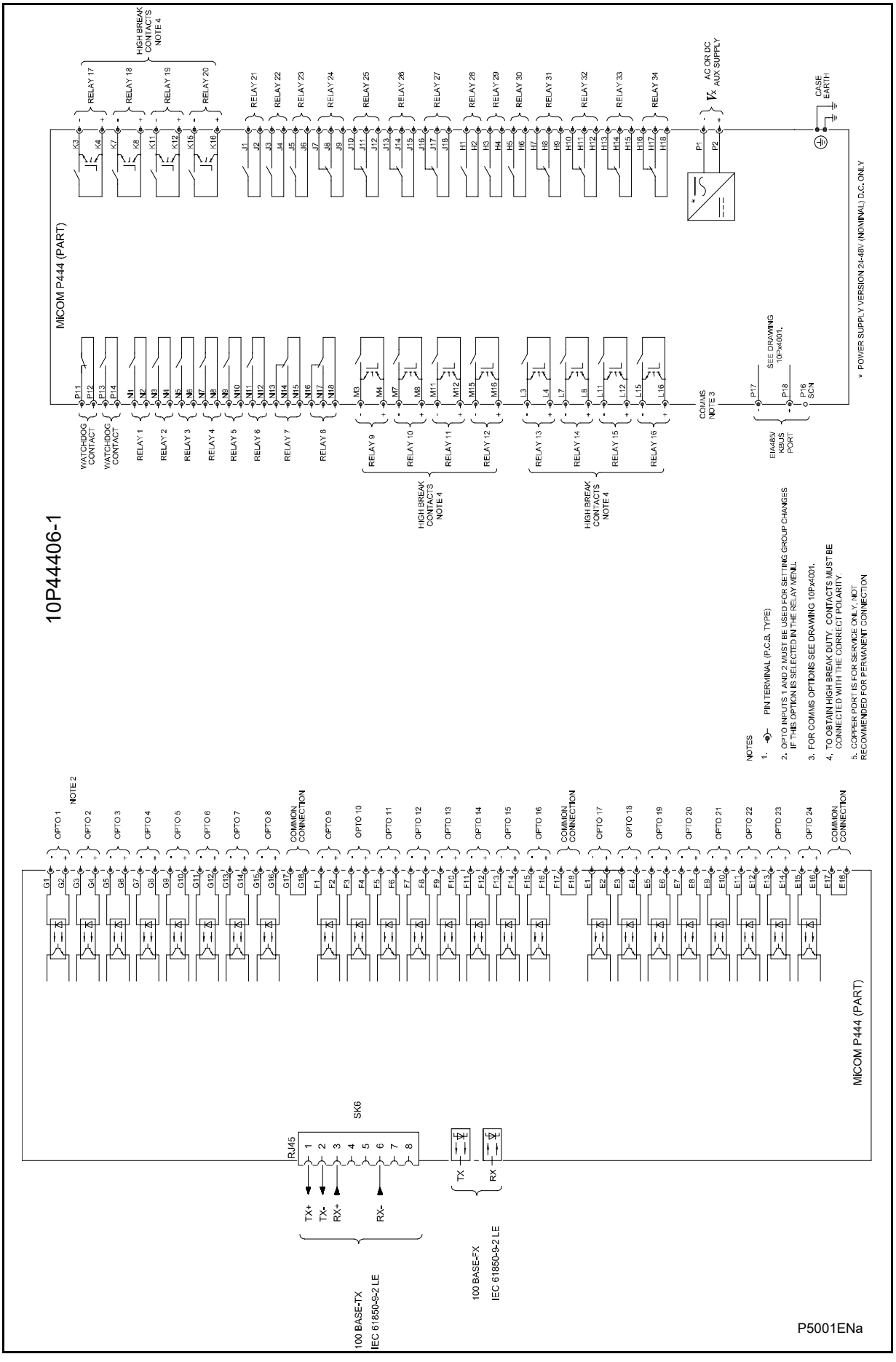
8.2 MICOM P444 with Standard contacts - Wiring Diagram (1/4)



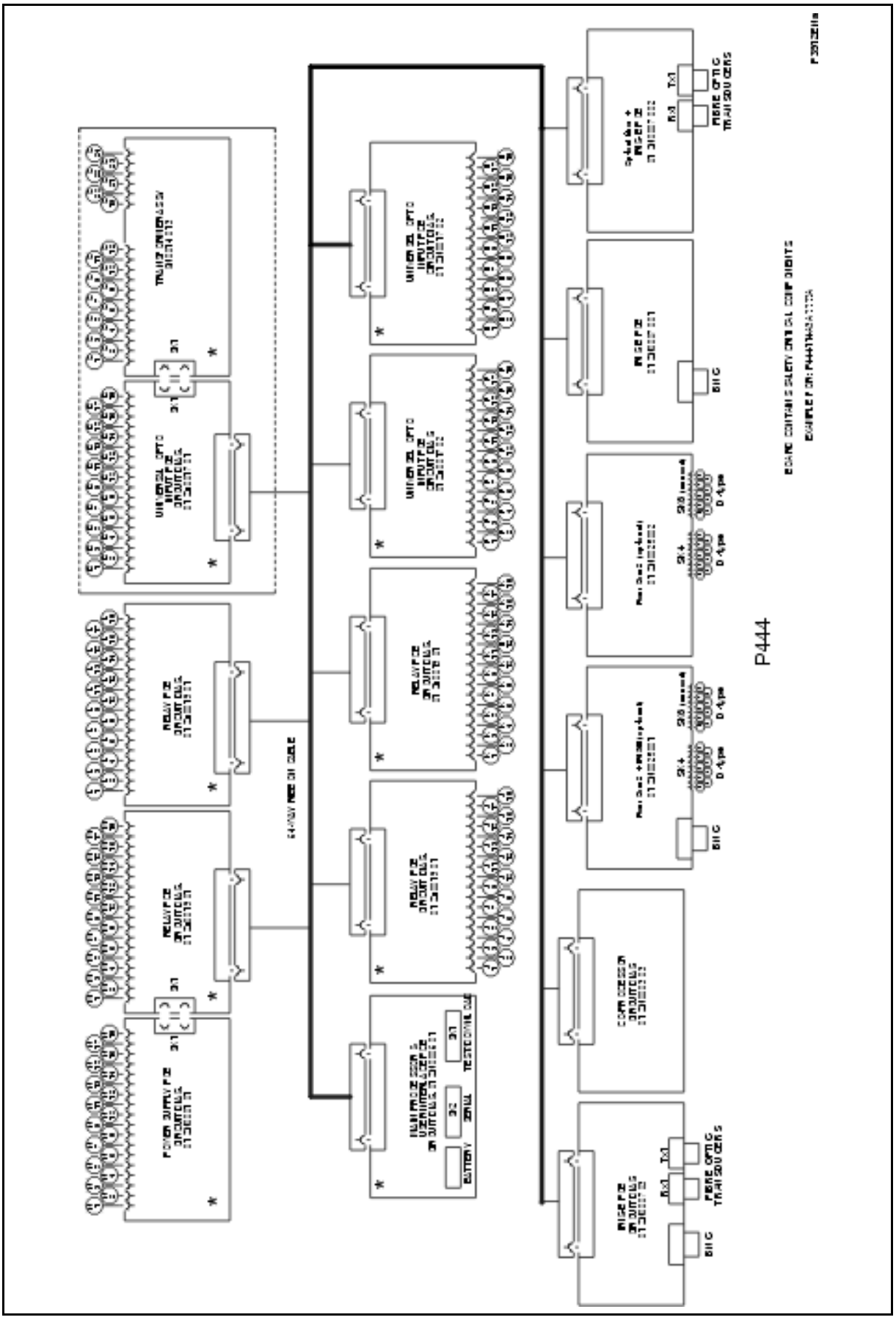
8.3 MICOM P444 with High Break contacts - Wiring Diagram (2/4)



8.4 MICOM P444 with NCIT and High Break contacts - Wiring Diagram (3/4)



8.5 MICOM P444 – Wiring Diagram (4/4)



CYBER SECURITY

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1. OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were more often than not proprietary.

For these reasons, the substation environment was very secure against cyber attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it can't be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult, to interpret them.

The increasing sophistication of protection schemes coupled with the advancement of technology and the desire for vendor interoperability has resulted in standardization of networks and data interchange within substations. Today, devices within substations use standardized protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardized protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for GE Vernova's range of Intelligent Electronic Devices (IEDs).

2. THE NEED FOR CYBER SECURITY

Cyber-security provides protection against unauthorized disclosure, transfer, modification, or destruction of information and/or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorized access to information)
- Integrity (preventing unauthorized modification)
- Availability / Authentication (preventing the denial of service and assuring authorized access to information)
- Non-Repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyze incidents)

The threats to cyber security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber attacks by hackers).

Good cyber security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (e.g. users keep passwords on their computer)
- Bypassing of controls (e.g. users turn off security measures)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Inadequate technology (e.g. substation is not firewalled)
- Examples of availability issues are:
- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate prevents access to equipment.

To help tackle these issues, standards organizations have produced various standards, by which compliance significantly reduces the threats associated with lack of cyber security.

3. STANDARDS

There are several standards, which apply to substation cyber security (see Table 1).

	Country	
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for Electric Power Utility by completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber security capabilities
IEC 62351	International	Power system data and Comm. protocol
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

Table 1: Standards applicable to cyber security

The standards currently applicable to Alstom Grid IEDs is NERC and IEEE1686.

3.1 NERC Compliance

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of Critical Cyber Assets, which control or have an influence on the reliability of North America's bulk electric systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

The group of CIP standards is listed in Table 2.

CIP standard	Description
CIP-002-1 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003-1 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004-1 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005-1 Electronic Security	Define and document logical security perimeter where Critical Cyber Assets reside and measures to control access points and monitor electronic access
CIP-006-1 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside
CIP-007-1 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets
CIP-008-1 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber Security Incidents relating to Critical Cyber Assets are identified
CIP-009-1 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

Table 2: NERC CIP standards

The following sections provide further details about each of these standards, describing the associated responsibilities of the utility company and where the IED manufacturer can help the utilities with the necessary compliance to these standards.

3.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up.

Power utility responsibilities:	Contribution:
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

3.1.2 CIP 003

CIP 003 requires the implementation of a cyber security policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained

Power utility responsibilities:	Contribution:
To create a Cyber Security Policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

3.1.3 CIP 004

CIP 004 requires that personnel having authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power utility responsibilities:	Contribution:
To provide appropriate training of its personnel	We can provide cyber security training

3.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power utility responsibilities:	Contribution:
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED the access at all access points of the ESP

3.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power utility responsibilities:	Contribution:
Provide physical security controls and perimeter monitoring. Ensure that people who have access to critical cyber assets don't have criminal records.	GE Vernova cannot provide additional help with this aspect.

3.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus

- Account management
- Monitoring
- An annual vulnerability assessment should be performed

Power utility responsibilities:	Contribution:
To provide an incident response team and have appropriate processes in place	Test procedures; We can provide advice and help on testing. Ports and services; Our devices can disable unused ports and services Security patch management; We can provide assistance Antivirus; We can provide advise and assistance Account management; We can provide advice and assistance Monitoring; Our equipment monitors and logs access

3.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power utility responsibilities:	Contribution:
To provide an incident response team and have appropriate processes in place.	GE Vernova cannot provide additional help with this aspect.

3.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power utility responsibilities:	Contribution:
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

3.2 IEEE 1686-2007

IEEE 1686-2007 is an IEEE Standard for substation IEDs cyber security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply to GE Vernova Px40 relays:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.
- Record of an audit trail listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

4. PX40 CYBER SECURITY IMPLEMENTATION

GE Vernova IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

This section describes the current implementation of cyber security, valid for the release of platform software to which this manual pertains. This current cyber security implementation is known as Cyber Security Phase 1.

At the IED level, these cyber security measures have been implemented:

- Four-level Access
- Password strengthening
- Disabling of unused application and physical ports
- Inactivity timer
- Storage of security events (logs) in the IED
- NERC-compliant default display

External to the IEDs, the following cyber security measures have been implemented:

- Antivirus
- Security patch management

4.1 Four-level Access

The menu structure contains four levels of access three of which are password protected. These are summarized in Table 3.

Level	Meaning	Read Operation	Write Operation
0	Read Some Write Minimal	SYSTEM DATA column: - Description - Plant Reference - Model Number - Serial Number - S/W Ref. - Access Level - Security Feature SECURITY CONFIG column: - User Banner - Attempts Remain - Blk Time Remain - Fallback PW level - Security Code (user interface only)	Password Entry LCD Contrast (user interface only)
1	Read All Write Few	All data and settings are readable. Poll Measurements	All items writeable at level 0. Level 1 Password setting Select Event, Main and Fault (upload) Extract Events (e.g. via MiCOM S1 Agile)

Level	Meaning	Read Operation	Write Operation
2	Read All Write Some	All data and settings are readable. Poll Measurements	All items writeable at level 1. Setting Cells that change visibility (Visible/Invisible). Setting Values (Primary/Secondary) selector Commands: - Reset Indication - Reset Demand - Reset Statistics - Reset CB Data / counters - Level 2 Password setting
3	Read All Write All	All data and settings are readable. Poll Measurements	All items writeable at level 2. Change all Setting cells Operations: - Extract and download Setting file. - Extract and download PSL - Extract and download MCL61850 (IED Config – IEC 61850) - Extraction of Disturbance Recorder - Courier/Modbus Accept Event (auto event extraction, e.g. via A2R) Commands: - Change Active Group setting - Close / Open CB - Change Comms device address. - Set Date & Time - Switch MCL banks / Switch Conf. Bank in user interface (IED Config – IEC 61850) - Enable / Disable Device ports (in SECURITY CONFIG column) - Level 3 password setting

Table 3: Password levels

4.1.1 Default Passwords

Default passwords are blank for Level 1, BBBB for level 2 and AAAA for Level 3.

4.1.2 Password Rules

- Passwords may be any length between 0 and 8 characters long
- Passwords may or may not be NERC compliant
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- Only one password is required for all the IED interfaces

4.1.3 Access Level DDBs

In additional to having the 'Access level' cell in the 'System data' column (address 00D0), the current level of access for each interface is also available for use in the Programming Scheme Logic (PSL) by mapping to these Digital Data Bus (DDB) signals:

- HMI Access Lvl 1
- HMI Access Lvl 2
- FPort AccessLvl1

- FPort AccessLvl2
- RPrt1 AccessLvl1
- RPrt1 AccessLvl2
- RPrt2 AccessLvl1
- RPrt2 AccessLvl2

Where HMI is the Human Machine Interface.

Each pair of DDB signals indicates the access level as follows:

- Lvl 1 off, Lvl 2 off = 0
- Lvl 1 on, Lvl 2 off = 1
- Lvl 1 off, Lvl 2 on = 2
- Lvl 1 on, Lvl 2 on = 3

4.2 Password Strengthening

NERC compliant passwords result in a minimum level of complexity, and include these requirements:

- At least one upper-case alpha character
- At least one lower-case alpha character
- At least one numeric character
- At least one special character (%,$...)
- At least six characters long

4.3 Password validation

The IED checks for NERC compliance. If the password is entered through the front panel then this is reflected on the panel Liquid Crystal Display (LCD) display.

If the entered password is NERC compliant, the following text is displayed

```
NERC COMPLIANT
P/WORD WAS SAVED
```

The IED does not enforce NERC compliance. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary. In the case that the password entered is not NERC-compliant, the user is required to actively confirm this, in which case the non-compliance is logged.

If the entered password is not NERC compliant, the following text is displayed:

```
NERC COMPLIANCE
NOT MET CONFIRM?
```

On confirmation, the non-compliant password is stored and the following acknowledgement message is displayed for 2 seconds.

```
NON-NERC P/WORD
SAVED OK
```

If the action is cancelled, the password is rejected and the following message displayed for 2 seconds.

```
NON-NERC P/WORD
NOT SAVE
```

If the password is entered through a communications port using Courier or Modbus protocols the IED will store the password, irrespective of whether it is or isn't NERC-compliant, and

then uses appropriate response codes to inform the client that the password was NERC-compliant or not. The client then can choose if he/she wishes to enter a new password that is NERC-compliant or leave the entered one in place.

4.3.1 Blank passwords

A blank password is effectively a zero-length password. Through the front panel it is entered by confirming the password entry without actually entering any password characters. Through a communications port the Courier and Modbus protocols each have a means of writing a blank password to the IED. A blank password disables the need for a password at the level that this password applied.

Blank passwords have a slightly different validation procedure. If a blank password is entered through the front panel, the following text is displayed, after which the procedure is the same as already described:

```
BLANK PASSWORD
ENTERED CONFIRM
```

Blank Passwords cannot be configured if the lower level password is not blank.

Blank Passwords affect fall back level after inactivity timeout or logout.

The ‘fallback level’ is the password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest level password that is blank, or level 0 if no passwords are blank.

4.4 Password Management

The user is locked out temporarily, after a defined number of failed password entry attempts. The number of password entry attempts, and the blocking periods are configurable. These settings are shown in Table 4.

The first invalid password entry sets the attempts count (actual text here) to 1 and initiates an 'attempts timer'. Further invalid passwords during the timed period increments the attempts count. When the maximum number of attempts has been reached, access is blocked. If the attempts timer expires, or the correct password is entered before the 'attempt count' reaches the maximum number, then the 'attempts count' is reset to 0.

Once the password entry is blocked, a 'blocking timer' is initiated. Attempts to access the interface whilst the 'blocking timer' is running results in an error message, irrespective of whether the correct password is entered or not. Only after the 'blocking timer' has expired will access to the interface be unblocked, whereupon the attempts counter is reset to zero.

Attempts to write to the password entry whilst it is blocked results in the following message, which is displayed for 2 seconds.

```
NOT ACCEPTED
ENTRY IS BLOCKED
```

Appropriate responses achieve the same result if the password is written through a communications port.

The attempts count, attempts timer and blocking timer can be configured, as shown in Table 4.

Setting	Cell col row	Units	Default Setting	Available Setting
Attempts Limit	25 02		3	0 to 3 step 1
Attempts Timer	25 03	Minutes	2	1 to 3 step 1
Blocking Timer	25 04	Minutes	5	1 to 30 step 1

Table 4: Password blocking configuration

4.5 Password Recovery

Password recovery is the means by which the passwords can be recovered on a device if the customer should mislay the configured passwords. To obtain the recovery password the customer must contact the GE Vernova Customer Care Center and supply two pieces of information from the IED – namely the Serial Number and its Security Code. The Customer Care Centre will use these items to generate a Recovery Password which is then provided to the customer.

The security code is a 16-character string of upper case characters. It is a read-only parameter. The IED generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

As soon as the security code is displayed on the LCD display, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the Customer Care Centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the Customer Care Centre over weekends and bank holidays.

To prevent accidental reading of the IED security code the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

The security code will be displayed on confirmation, whereupon the validity timer will be started. Note that the security code can only be read from the front panel.

4.5.1 Entry of the Recovery Password

The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.

Entry of the recovery password causes the IED to reset all passwords back to default. This is all it is designed to do. After the passwords have been set back to default, it is up to the user to enter new passwords appropriate for the function for which they are intended, ensuring NERC compliance, if required.

On this action, the following message is displayed:

```
PASSWORDS HAVE
BEEN SET TO DEFAULT
```

The recovery password can be applied through any interface, local or remote. It will achieve the same result irrespective of which interface it is applied through.

4.5.2 Password Encryption

The IED supports encryption for passwords entered remotely. The encryption key can be read from the IED through a specific cell available only through communication interfaces, not the front panel. Each time the key is read the IED generates a new key that is valid only for the next password encryption write. Once used, the key is invalidated and a new key must be read for the next encrypted password write. The encryption mechanism is otherwise transparent to the user.

4.6 Port Disablement

4.6.1 Disabling Physical Ports

It is possible to disable unused physical ports. A level 3 password is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example if rear port 1 is to be disabled, the following message appears:

```
REAR PORT 1 TO BE
DISABLED.CONFIRM
```

There are between two and four ports eligible for disablement:

- Front port
- Rear port 1
- Rear port 2 (not implemented on all models)
- Ethernet port (not implemented on all models)

Note: It is not possible to disable a port from which the disabling port command originates.

4.6.2 Disabling Logical Ports

It is possible to disable unused logical ports. A level 3 password is needed to perform this action.

Note: The port disabling setting cells are not provided in the settings file.



Caution **Disabling the Ethernet port will disable all Ethernet based communications.**

If it is not desirable to disable the Ethernet port, it is possible to disable selected protocols on the Ethernet card and leave others functioning.

Three protocols can be disabled:

- IEC 61850
- DNP3 Over Ethernet
- Courier Tunnelling

Note: If any of these protocols are enabled or disabled, the Ethernet card will reboot.

4.7 Logging out

If you have been configuring the IED, you should 'log out'. You do this by going up to the top of the menu tree. When you are at the Column Heading level and you press the Up button, you may be prompted to log out with the following display:

```
DO YOU WANT TO
LOG OUT?
```

You will only be asked this question if your password level is higher than the fallback level.

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT
Access Level <x>
```

Where x is the current fallback level.

If you decide not to log out (i.e. you cancel), the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
Access Level <x>
```

Where x is the current access level.

4.8 Events

The implementation of NERC-compliant cyber security necessitates the generation of a range of Event records, which log security issues such as the entry of a non-NERC-compliant password, or the selection of a non-NERC-compliant default display. Table 6 lists all Security events.

Event Value	Display
PASSWORD LEVEL UNLOCKED	USER LOGGED IN ON <int> LEVEL <n>
PASSWORD LEVEL RESET	USER LOGGED OUT ON <int> LEVEL <n>
PASSWORD SET BLANK	P/WORD SET BLANK BY <int> LEVEL <p>
PASSWORD SET NON-COMPLIANT	P/WORD NOT-NERC BY <int> LEVEL <p>
PASSWORD MODIFIED	PASSWORD CHANGED BY <int> LEVEL <p>
PASSWORD ENTRY BLOCKED	PASSWORD BLOCKED ON <int>
PASSWORD ENTRY UNBLOCKED	P/WORD UNBLOCKED ON <int>
INVALID PASSWORD ENTERED	INV P/W ENTERED ON <int>
PASSWORD EXPIRED	P/WORD EXPIRED ON <int>
PASSWORD ENTERED WHILE BLOCKED	P/W ENT WHEN BLK ON <int>
RECOVERY PASSWORD ENTERED	RCVY P/W ENTERED ON <int>
IED SECURITY CODE READ	IED SEC CODE RD ON <int>
IED SECURITY CODE TIMER EXPIRED	IED SEC CODE EXP -
PORT DISABLED	PORT DISABLED BY <int> PORT <prt>
PORT ENABLED	PORT ENABLED BY <int> PORT <prt>
DEF. DISPLAY NOT NERC COMPLIANT	DEF DSP NOT-NERC
PSL SETTINGS DOWNLOADED	PSL STNG D/LOAD BY <int> GROUP <grp>

Event Value	Display
DNP SETTINGS DOWNLOADED	DNP STNG D/LOAD BY <int>
TRACE DATA DOWNLOADED	TRACE DAT D/LOAD BY <int>
IEC61850 CONFIG DOWNLOADED	IED CONFG D/LOAD BY <int>
USER CURVES DOWNLOADED	USER CRV D/LOAD BY <int> GROUP <crv>
PSL CONFIG DOWNLOADED	PSL CONFG D/LOAD BY <int> GROUP <grp>
SETTINGS DOWNLOADED	SETTINGS D/LOAD BY <int> GROUP <grp>
PSL SETTINGS UPLOADED	PSL STNG UPLOAD BY <int> GROUP <grp>
DNP SETTINGS UPLOADED	DNP STNG UPLOAD BY <int>
TRACE DATA UPLOADED	TRACE DAT UPLOAD BY <int>
IEC61850 CONFIG UPLOADED	IED CONFG UPLOAD BY <int>
USER CURVES UPLOADED	USER CRV UPLOAD BY <int> GROUP <crv>
PSL CONFIG UPLOADED	PSL CONFG UPLOAD BY <int> GROUP <grp>
SETTINGS UPLOADED	SETTINGS UPLOAD BY <int> GROUP <grp>
EVENTS HAVE BEEN EXTRACTED	EVENTS EXTRACTED BY <int> <nov> EVNTS
ACTIVE GROUP CHANGED	ACTIVE GRP CHNGE BY <int> GROUP <grp>
CS SETTINGS CHANGED	C & S CHANGED BY <int>
DR SETTINGS CHANGED	DR CHANGED BY <int>
SETTING GROUP CHANGED	SETTINGS CHANGED BY <int> GROUP <grp>
POWER ON	POWER ON -
SOFTWARE_DOWNLOADED	S/W DOWNLOADED -

Table 5: Security event values

Where:

int is the interface definition (UI, FP, RP1, RP2, TNL, TCP)

prt is the port ID (FP, RP1, RP2, TNL, DNP3, IEC, ETHR)

grp is the group number (1, 2, 3, 4)

crv is the Curve group number (1, 2, 3, 4)

n is the new access level (0, 1, 2, 3)

p is the password level (1, 2, 3)

nov is the number of events (1 – nnn)

Each event is identified with a unique number that is incremented for each new event so that it is possible to detect missing events as there will be a 'gap' in the sequence of unique identifiers. The unique identifier forms part of the event record that is read or uploaded from the IED.

Note: It is no longer possible to clear Event, Fault, Maintenance, and Disturbance Records

4.9 Cyber Security Settings

Cyber Security is important enough to warrant its own IED column called SECURITY CONFIGURATION, located at column number 25. In addition to this new group, settings are affected in the SYSTEM DATA, COMMS SYS DATA and VIEW RECORDS columns.

A summary of the relevant columns is shown in Table 6. A complete listing of the settings criteria is described in the Settings and Records chapter.

Parameter	Cell col row	Default Setting	Available Setting	Interface Applicability	In Setting file?
Password	00 02		ASCII 33 to 122	All	Yes, ~~~~~~~~
Access Level	00 D0		0 = Read Some, 1 = Read All, 2 = Read All + Write Some, 3 = Read All + Write All	All	Yes, Not Settable
Password Level 1	00 D2		ASCII 33 to 122	All	Yes
Password Level 2	00 D3		ASCII 33 to 122	All	Yes
Password Level 3	00 D4		ASCII 33 to 122	All	Yes
Security Feature	00 DF		1	All	Yes, Not Settable
SECURITY CONFIG	25 00			All	Yes
Use Banner	25 01	ACCESS ONLY FOR AUTHORISED USERS	ASCII 32 to 163	All	Yes
Attempts Limit	25 02	3	0 to 3 step 1	All	Yes
Attempts Timer	25 03	2	1 to 3 step 1	All	Yes
Blocking Timer	25 04	5	1 to 30 step 1	All	Yes
Front Port	25 05	Enabled	0 = Disabled or 1 = Enabled	All	No
Rear Port 1	25 06	Enabled	0 = Disabled or 1 = Enabled	All	No
Rear Port 2	25 07	Enabled	0 = Disabled or 1 = Enabled	All	No
Ethernet Port*	25 08	Enabled	0 = Disabled or 1 = Enabled	All	No
Courier Tunnel*†	25 09	Enabled	0 = Disabled or 1 = Enabled	All	No
IEC61850*†	25 0A	Enabled	0 = Disabled or 1 = Enabled	All	No

Parameter	Cell col row	Default Setting	Available Setting	Interface Applicability	In Setting file?
DNP3 OE*†	25 0B	Enabled	0 = Disabled or 1 = Enabled	All	No
Attempts Remain	25 11			All	Yes, Not Settable
Blk Time Remain	25 12			All	Yes, Not Settable
Fallbck PW Level	25 20	0	0 = Password Level 0, 1 = Password Level 1, 2 = Password Level 2, 3 = Password Level 3	All	Yes, Not Settable
Security Code	25 FF			User interface Only	No
Evt Unique Id (Normal Extraction)	01 FE			All	No
Evt Iface Source ± (Bits 0 – 7 of Event State)	01 FA			All	No
Evt Access Level ± (Bits 15 – 8 of Event State)	01 FB			All	No
Evt Extra Info 1 ± (Bits 23 – 16 of Event State)	01 FC			All	No
Evt Extra Info 2 ±Ω (Bits 31 – 24 of Event State)	01 FD			All	No

Table 6: Security Cells Summary

Where:

* - These cells will not be present in a non-Ethernet product

†- These cells will be invisible if the Ethernet port is disabled.

± - These cells invisible if event is not a Security event

Ω – This cell is invisible in current phase as it does not contain any data. Reserved for future use.

HARDWARE/SOFTWARE VERSION HISTORY AND COMPATIBILITY

(Note: Includes versions released and supplied to customers only)

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch A2.x: First Model – P441/P442 (P444 not available) – Modbus/Kbus/IEC103 – 4 languages – Optos 48Vcc (Hardware=A) **Documentation:** *TG 1.1671-C & OG 1.1671-B*					
A2.6	**A**	**03**	10/2000	VDEW-ModBus-Kbus cells/CBaux/IRIGB/WeakInfeed/Reset IDMT/SyncCheck/AR Led	V1.09
		04	10/2000	VDEW-ModBus-Kbus cells/CBaux/IRIGB/ WeakInfeed/Reset IDMT/ SyncCheck/AR Led **New S1 version**	V2.0
A2.7		**03**	04/2001	Freq out of range (major correction)- 1/3 pole AR logic - VTS	V1.10
		04	04/2001	Frequency out of range (major correction)- 1/3 pole AR logic **New S1 version**	V2.0
A2.8		**04**	07/2001	Communication improvement / Floc with 5Amp / IrigB	V2.0
A2.9		**04**	01/ 2002	3P fault in Power Swing/SOTF logic/CB Fail/Ext. Trip + 5 ms/Z1-Z2 measure for small characteristic /SOTF-TOR / U-I prim sec	V2.0
A2.10		**04**	05/2002	EEPROM correction/RCA angle/DEF correction/New general distance Trip equation (Block scheme) / Fault Locator	V2.0
A2.11		**04**	09/2003	Last A2.x branch version: Retrip CB/Ffailure/31th December for DRec/Disturbance compressed function and communication correction/Voltage memory/DEF/Ext Csync/P.Phase ref Csync/Sync live-live/2UN Vref Sync/Z1 & Arg<55°	V2.0

Note: Software version / hardware version / model number can be found by setting in "system data" with MiCOM S1 or LCD front panel.

Note 2: Version A2.x not distributed (mandatory upgrade)

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch A3.x : P444 model with 24 optos/32 outputs (Omron) – Universal optos – Italian Language – DNP3					
A3.0	**A or B for P441/442** **A for P444**	**05**	05/2001	P444/DNP3/NCIT/universal input/5 languages Italian model 4050A for P444 P441/P442 models 050A (48Vcc) or 050B (Universal optos) DDB with 1022 cells/Discrimination timer in AR/New DDB distance cells/DEFlogic/SOTF timer/Broken Conductor/Com.	V2.02 + patch
A3.1		**06**	12/2001	SOTF-TOR/Z4 block Pswing/CB Fail/IEC103 disturbance/U-I Prim-sec / kms-Miles / 3P fault in Power Swing/Z1-Z2 measurement for a small characteristic / Ext Trip+5msec/New settings	V2.02 + patch
A3.2		**06**	05/2002	EEPROM correction/New general distance Trip equation (Block scheme)/RCA angle/IEC 103 correction/Fault Loc/DEF P selec	V2.02 + patch
A3.3		**06**	09/2003	Retrip CB/Ffailure/31st December for Drec/Disturbance (compressed or not compressed) and communication correction / Voltage memory / DEF/ Ext Chksync/P.Phase ref Chksync / Sync live-live / I broken Cond./ Px4X with Px3x in IEC103/2UN Vref Sync/Z1 & Ang<55°	V2.02 + patch
A3.4		**06**	10/2003	Last A3.x branch version: Time sync cell in ModBus/ Optos tagging in event/ CB close DNP3/ Status opto with setting group/ Im displayed in Measurement mode/ IEC 103	V2.02 + patch

Note: The software version / hardware version / model number can be found through the setting in "system data" viaMiCOM S1 or LCD front panel.

Note 2: Version A3.0, A3.1 and A3.3 not distributed (mandatory upgrade). Version A3.3: Recommanded upgrade.

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch A4.x : Second Rear Port - more alarms - new application feature					
A4.0	**A or B for P441/442** **A for P444**	**07**	09/2002	Second rear port/Slip frequency/Retrip CB/VTS phase selec/PPGround phase selection/Extraction PSL/Serial Cmp Line/New DDB cells/Overlap Z/ Rev with X4 limit/Winfeed/Floc in IEC /Dead time2/I Bk conduct.	V2.05 + patch
A4.1		**07**	12/ 2002	Bi phase ground & phase selection/Synchro VT bus side	V2.07
A4.3		**07**	04/ 2003	Voltage memory improvement/compliant IEC103 with Px3x /DEF/Pswing & glitchZ	V2.07
A4.4		**07**	08/2003	Synchro check function improvement/Tripping time stability for Z2 fault/Problem of battery alarm when IEC103 communication resolved	V2.07
A4.5		**07**	09/2003	Disturbance (compressed or not compressed) and communication correction / DEF/ Ext Csync/P.Phase ref Csync / Sync live-live / I broken Cond./ Px4X with Px3x in IEC103/Battery Alarm IEC 103/31th December for Drec/2UN Vref Sync/Z1 & Arg<55°/Zn-Zn+1 with +30msec	V2.07
A4.8		**07**	09/2004	Timesync cell in ModBus/Synchro TP bus/Optos taging in event/Dynamic management Bus-Line for checksync /ModBus correction /DNP3/Frequency tracking/Directionnal with Deltas&Classical are computed in parallel (No delay between the algorithms)	V2.07
A4.9		**07**	05/2005	DNP3 with S1/ ModBus/ CB close DNP3/ Floc with evolving fault/ Status opto with setting group/ Im displayed in Measurement mode/ VTS alarm using V2	V2.07

Note 1: The software version / hardware version / model number can be found through the setting in "system data" viat MiCOM S1 or LCD front panel.

Note 2: Version A4.0, A4.1, A4.3, A4.4 and A4.5 not distributed (mandatory upgrade). Version A4.8 and A4.9 (up to A4.9H): Recommanded upgrade.

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch B1.x : New Hardware Platform (150 MHz coprocessor Board -2nd rear port-Triptime= 1,1 Cycle - **48 samples/T**) & New functions (**32N & 59N**)					
B1.0	**C**	**08**	12/2002	New platform/model 080C/coprocessor board at 150 MHz/**PW (32N)/CVTS (59N**) new functions/ Px4X with Px3x in IEC103 / Retrip CB/Ffu/31st December for Drec/I Brok.cond./DEF polar.	V2.09
B1.1		**09**	07/2003	Synchrocheck ext correction & PPhase ref & L-Live / 32N correction / Line angle<55° / Voltage memory / Power swing & Z glitch	V2.09 + patch*
B1.2		**09**	09/2003	Disturbance compressed & not compressed function and communication correction/2UN Vref Sync/Zn-Zn+1 with +30msec	V2.09 + patch*
B1.3		**09**	07/2004	Synchro TP bus/Optos taging in event/ZSP angle/Dynamic management Bus-Line for checksync	V2.09 + patch*
B1.4		**09**	09/2004	New plateform /Timesync cell in ModBus /DNP3	V2.09 + patch*
B1.5		**09**	11/2004	CB close command is applied 2 time from DNP3 Fault location-Settings group by opto-DNP3 & model N°	V2.09 + patch*
B1.6		**09**	04/2005	32N corrected (5Amp) - Primary measurement & Im	V2.09 + patch*
B1.7		09	06/2005	ModBus/ VTS alarm using V2	V2.09 + patch*

Note: The software version / hardware version / model number can be found through the setting in "system data" via MiCOM S1 or LCD front panel.
Patch 09 is included with MiCOM S1 version V2.11

Note 2: Version B1.0, to B1.3 not distributed (mandatory upgrade). Version B1.4 to B1.7: Recommanded upgrade.

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch C1.x : New Hardware Platform (**New CPU Board 150MHz + Coprocessor Board 150MHz**-2nd rear port-Triptime= 1,1Cycle - 48 samples/T) & Functions as B1.4+ New Distance Features					
C1.0	**G for P441/442** **G - H for P444**	**20**	04/2004	**New platform**/model 20G or 20H/**Cpu board at 150 MHz**/Fast trip board/46 output-P444 model 20H/Pswing for China Distance feature: timer from Zn to Zn-1/Tilt settable in Z1Z2Zp/Output "Phaseground detection"/**PAP** (Winfeed for RTE France)/Drec not compressed with 24 samples by cycle/Control input/InterMicom/Tp in DEF/DEF timer from 2 to 100msec/3rd&4th IN>/Internal trace by Zgraph Relay-opto event log/Z4Zp indication/	V2.09 + patch* or V2.10
C1.1		**20**	12/2004	Last C1.x branch version:UCA2 / InterMicom with UCA2/Timesync cell in ModBus/Synchro TP bus/Optos taging in event/Dynamic management Bus-Line for checksync	V2.09 + patch* or V2.10

Note 1 : Version C1.0 and C1.1 not distributed (mandatory upgrade).

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch C2.x : Idem C1.x with **UCA2 (Ethernet optical support) & new function (49+NCIT)**					
C2.0	**G - J for P441/442** **G - J - H for P444**	**30**	08/2004	New platform- **NCIT**/ **Thermal Overload** as P540/ Synchro TP bus/ Optos tagging in event/ ZSP angle/ Dynamic management Bus-Line for checksync/ DEF Reverse sensitivity/ Time sync input/ ZSP start/ Ethernet module **NCIT 61850-9-2**	V2.10 + patch* or V2.11
C2.1		**30**	09/2004	Timer 0/DNP3 correction	
C2.2		**30**	10/2004	InterMicom/ DEF primary scale/ AREVA name in UCA2	
C2.5		**30**	11/2004	Phase select. PPground/ Reset IN dead/ DNP3 & CB Close/ Floc/ Opto& setting group selection/ DNP3	
C2.6		**30**	05/2005	Primary measurement & Im - Error during flash with optical fiber/ Floc&Broken currents new cells in DNP3-E2.0 official platform with NCIT	
C2.7		**30**	07/2005	UCA2 no longer supported (from that version onwards)/ Add phase voltage inversion detection in Voltage Transformer Supervision (V2 presence without I0 and I2)./ Add IEC61870-5-103 Generic Services	
C2.8		**30**	02/2006	P0 time delay/ NCIT sampling/Extended mode with DRec/ OpticFiber with KBus model/ Tilt angle & K0/ Reset latch DDB& LEDs	V2.12 + patch
C2.9		**30**	03/2006	DNP3/ PreTrigger in DRec/ Tilt angle & K0/ C264 compatibility in DNP3/ Reset VTS 3phases	
C2.10c		**30**	05/2006	Add Chinese HMI (First implementation, will become standard in next version)	
C2.11 to C2.16		**30**	052007	Zone reset&overlap/ WeakInfeed Echo+DEF/ Control Inp/ Z1ext+Tilt/ Selfcheck Output board/ DRec & 5Amp/ Start D & Phase Selection/ Timer&Thermal Protec 5Amp	V2.14
C2.17-S		**30**	2011	New Alstom Grid	

Note 1: Software version / hardware version / model number can be found by setting in “system data” with MiCOM S1 or LCD front panel.

Note 2: Version C2.0 and C2.1, 2.10c – C2.11 not distributed (mandatory upgrade). Versions C2.2 to C2.8 and C2.12 to C2.15: Recommended upgrade.

Note 3: Patch 20 & 30 are included with MiCOM S1 version V2.11

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch C3.x : Idem C2.x with **new communication protocol (IEC 61850-8-1) / UCA2 not supported – Model J only (Dual optos managed by default)**					
C3.7	**J for P441 for P442 for P444**	**31**	12/2006	Add IEC 61850-8-1 protocol / Zone reset&overlap/ WeakInfeed Echo+DEF/ Control Inp/ 2nd Sync +NCIT/ 21-67N activated separately/ 67N&Blocking Scheme/ Floc&measurement with high harmonic/ Hysteresis at 2% for V> &V<	V2.12 + Patch
C3.8		**31**	02/2007	Z1ext+Tilt/ Selfcheck Output board/ NCIT acquisition	V2.14 + Patch
C3.9		**31**	06/2007	Start Δ & Phase Selection/ Timer&Thermal Protec 5Amp/ KEMA & Floc for 61850-8-1	
C3.10		**31**	02/2008	State change & Time stamping	
C3.11 to **C3.16**		**31**	03/2008	Last C3.x branch version: Phase select & PPGnd fault /DEF & Negative polarisation/ 61850-8-1	
C3.18_A		**31**		New Brand Alstom Grid. IEC 61850 Phase 1: GOOSE, Non buffered Reports IEC 61850 9.2 First HW (A) Improved too early directional decision and Inhibit AR logic	

Note 1: Version C3.7 not distributed (mandatory upgrade). Versions C3.8 to C3.10: Recommended upgrade.

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch C4.x : Idem C3.x with **new features (cells and DDB)**					
C4.0	**J for P441 for P442 for P444**	**35**	04/2007	Start Δ & Phase Selection/ Add new DDB (Dist. Block/V>-V<)	V2.14 + Patch
C4.1		**35**	10/2007	Last C4.x branch version: Timer&Thermal Protec 5Amp/ KEMA & Floc for 61850-8-1	V2.14 + Patch
C4.1.A		**35**		New Brand Alstom Grid. Function Protection Update	

Note 1: Version C4.0 not distributed (mandatory upgrade).

Relay type: P441, P442, P444					
Branch C5.x : Idem C4.x with **new features (cells and DDB)**					
C5.0	**J for P441 for P442 for P444**	**36**	05/2007	Phase selec & PPGnd fault/ DEF & Negative polarisation/ Conventional algo & 1PGnd fault/ Fault report/ Cont Input label/ RGuard/ IN> 2nd stage/ IDMT TMS steps/ New DDB: Internal trip+trip LED/ DRec default settings/ SOTF-TOR/ I>4&StubB/ VMemory settable/ CT polarity/ I2>/ VR>/ DNP3/ **New Zone Q**/ PSwing RLim/ Channel aided scheme/ I0 setting/ PSL graphic improved	V2.14 + Patch
C5.5		**36**	04/2008	State&time stamp/ IEC 61850-8-1/ DNP3 over Ethernet/ Courier&Group/ I2&Dist start/ WeakInfeed TAC received extented	V2.14 + Patch V3.4 (S1 Studio)
C5.6-A		**36**	2011	New Brand Alstom Grid. Functional Protection Update (ex: Zq added)	
C5.7A		**36**	2012	Function Protection Update Improved too early directional decision and Inhibit AR logic	

Relay type: P441, P442, P444					
Branch C7.x : Idem C5.x with **Cyber security and "PSL Timers" features**					
C7.A	**J** **for P441** **for P442** **for P444**		05/2011	The following features are added: - Cyber security features - New "PSL timers" setting allowing remote time setting of timers in the PSL using HMI. - "IN> Blocking" menu, - New technical manual	V3.4 (S1 Studio)

Note 1: Version C5.0 – C5.1 not distributed (mandatory upgrade). Versions C5.2 to C5.4: Recommended upgrade.

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch D1.x : Idem C5.6S with **new HW suffix K: extended buttons, high break contacts, tri colors LEDs…**					
D1.0	**K for P442 for P444**	**40**	02/2007	HW suffix K/ Start D & Phase Selection/ New DDB cells V> &V<&independent distance scheme	V2.14 + Patch
D1.1 to **D1.3**		**40**	04/2008	Timer&Thermal Protec 5Amp/ KEMA & Floc for 61850-8-1	V2.14 + Patch
Branch D2.x : Idem D1.x with **new features (cells and DDB)**					
D2.0 to **D2.6**	**K for P442 for P444**	**40 45**	11/2008	The following features are added: - reverse guard detection - Second stage of IN> earth overcurrent with DT or IDMT, - IDMT step size for TMS from 0.025 to 0.005 - Extension from 4 In to 10 In the maximum setting range for the 2 first stages - Labels for disturbance records modified, - “SOFT I>3 Enabled” TOR/SOTF mode creation, - “Trip LED” menu added in DDB - voltage memory validity settable from 0s to 10s (step 0.01s) - CT connection can be modified by software - Negative sequence overcurrent protection enhanced, - Residual overvoltage enhanced - DNP3 serial added - Zone Q added - resistance limits for power swing = R1, R2, RP, RQ, R3/R4) - Channel aided trip modification - Channel-aided distance schemes: **trip after receipt of signal from remote end protection and Tp instead of T1.** - New settings for I0 threshold - InterMiCom Interrupt integration	V2.14 + Patch S1 Studio
D2.6_A		**40 45**		New Brand Alstom Grid. Same feature as Model 36 with HW K	

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch D3.x : Idem D2.6 with **new features (cells and DDB)**					
D3.0 **D3.1** **D3.2**	**K** **for P442** **for P444**	**50**	06/2009	The following features are added: - New undercurrent protection features, - New Frequency protection features, - DDB with 2047 cells - Undervoltage protection: stages 3&4 (V<3, V<4) added, - Overvoltage protection: stages 3&4 (V>3, V>4) added, - new autoreclose blocking parameters	V2.14 + Patch V3.0 (S1 Studio)
D3.3_A	**K** **for P442** **for P444**	**50**	06/2009	New brand: Alstom Grid	

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
Branch D1.x : Idem D3.x with **modified or new features (cells and DDB)**					
D4.0	**K for P442 for P444**	**55**	2011	The following features are modified: - addition of trip reset for Zero sequence power (IDMT/DT) - I0 threshold and DEF algorithm operation, - delta direction decision during delta phase selection, - forward zone decision during reverse phase operation, - zone decision when a double fault occurs, - phase selection, zone decision and global convergence after a double fault, - thermal overload deactivation, - Current measurement offset with NCIT module, - synchro check calculation (with IEC61850-9-2 module) - LED reset after 1P A/R or 3P A/R, - PAP when distance protection is disabled, - improvement of phase selection with fast decision, - bit transmission in the IEC61850 model, The following features are added: - Read Only Mode compliant with the Px4x range, - Set/Reset latch gate logic compliant with the Px4x range - DNP for SSE integration note compliant with the Px4x range - IEC61850 compliance with the Px4x range - Select-Before-Operate control function interlocking facilities in the IEC 60870-5-103 protocol, - new setting time-delay in the DEF protection, - IEC61850 and RS 485 IEC60870-5-103 comms - Control input, relays and LEDs state stored in the RAM.	V3.1 (S1 Studio)
D4.1				The following features are modified: - IEC61850-8-1 phase 2.1 comms reports issues - SBO support for CS103 protocol.	
D4.2				The following features are modified: - “Latched alarm” reset DDB for IEC61850, - DNP3 group change command	

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
D4.3	**K for P442 for P444**	**55**	2011	<u>The following features are modified:</u> - V3<, V4<, V3> or V4> fault display (front panel), - V3<, V4<,n V3> and V4> added in DNP files, - hysteresis of the first threshold of residual overvoltage = 98%, - Block A/R2 address in Modbus tab, - assignation of some Logical Nodes data source - BBRAM use - New brand	V3.1 (S1 Studio)
D4.4A			06/2009	Function Protection Update IEC 61850 9.2 First HW (A) L5.6 PL P444 Protection Functions qualified. Goose delay issue to be fixed	
D4.5A				Goose performance improved Improved too early directional decision and Inhibit AR logic	
<u>Branch D5.x :</u> Idem D4.3-S with **IEC61850-9-2 communication protocol**					
D5.A	**K for P442 for P444**	**55**	2011	<u>Last D5.x branch version</u> : The following features are modified: - Compatibility with IEC61850-9-2 Ethernet communication protocol, - modification of “Ethernet NCIT” synchronization alarms - new NCIT alarm statuses - Logical nodes arrangements modified - New technical manual	V3.4 (S1 Studio)
60A	**J**	**60**	2011	- Function Protection based Model 55 - Cyber Security - PSL settings - M3.0 PL	

Relay type: P441, P442, P444					
Software version	**Hardware version**	**Model number**	**Date of issue**	**Full Description of changes**	**S1 Compatibility**
70B	**M**	**70**	2014	- 64 digitals in the DR. - V> % Hysteresis range from 0.5 to 2 and default is 2 i.e. 0.995 to 0.98 of Setting. - Vcheck Sync is not longer an alternative. This means a 4th VT is always present and can be used for VN measured or Vcheck Sync (selected via setting). - 4th CT can be used for IN measured or Imutual coupling (selected via setting). - C/S Diff V measured included in MEASUREMENT 1 - P442 model can be ordered to work with IEC62850 9-2 - Hot standby-ethernet - SNTP alarm	MiCOM S1 Agile V1.1.0
71H	**M**	**71**		-Load Blinder Included in the Distance Characteristic	MiCOM S1 Agile V1.1.0
72A	**M**	**72**	2017	- Change in overvoltage and undervoltage measurement mode - Included the ability to block the PAP scheme in case of the distance start characteristic is asserted - Included the option of negative sequence voltage check - Incremented sampling rate for the Disturbance Record to 48 samples per cycle - Modified the setting range for V> overvoltage hysteresis - Included logical node MLFR - Modified energy measurement	MiCOM S1 Agile V1.3.1

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