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5th Generation
P54

Technical Manual
Single/Dual Breaker Current Differential with Distance

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Major changes

For information on the updates included in this release of the manual, please refer to the latest release notes.

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CHAPTER 1

INTRODUCTION

1.1 CHAPTER OVERVIEW

This chapter provides some general information about the technical manual and an introduction to the device(s) described in this technical manual.

This chapter contains the following sections:

Chapter Overview 2
Foreword 3
Product Scope 5
Features and Functions 7
Logic Diagrams 10
Functional Overview 12

1.2 FOREWORD

This technical manual provides a functional and technical description of GE Vernova's 5th Generation transmission protection IED, as well as a comprehensive set of instructions for using the device. The level at which this manual is written assumes that you are already familiar with protection engineering and have experience in this discipline. The description of principles and theory is limited to that which is necessary to understand the product. For further details on general protection engineering theory, we refer you to GE Vernova's publication, Protection and Automation Application Guide, which is available online or from our Contact Centre.

We have attempted to make this manual as accurate, comprehensive and user-friendly as possible. However we cannot guarantee that it is free from errors. Nor can we state that it cannot be improved. We would therefore be very pleased to hear from you if you discover any errors, or have any suggestions for improvement. Our policy is to provide the information necessary to help you safely specify, engineer, install, commission, maintain, and eventually dispose of this product. We consider that this manual provides the necessary information, but if you consider that more details are needed, please contact us.

All feedback should be sent to our contact centre via:

GA.support@gevernova.com

1.2.1 TARGET AUDIENCE

This manual is aimed towards all professionals charged with installing, commissioning, maintaining, troubleshooting, or operating any of the products within the specified product range. This includes installation and commissioning personnel as well as engineers who will be responsible for operating the product.

The level at which this manual is written assumes that installation and commissioning engineers have knowledge of handling electronic equipment. Also, system and protection engineers have a thorough knowledge of protection systems and associated equipment.

1.2.2 TYPOGRAPHICAL CONVENTIONS

The following typographical conventions are used throughout this manual.

- The names for special keys appear in capital letters.
  For example: ENTER
- When describing software applications, menu items, buttons, labels etc as they appear on the screen are written in bold type.
  For example: Select **Save** from the file menu.
- Filenames and paths use the courier font
  For example: `Example\File.text`
- Special terminology is written with leading capitals
  For example: Sensitive Earth Fault
- If reference is made to the IED's internal settings and signals database, the menu group heading (column) text is written in upper case italics
  For example: The *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the setting cells and DDB signals are written in bold italics
  For example: The ***Language*** cell in the *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the value of a cell's content is written in the Courier font
  For example: The ***Language*** cell in the *SYSTEM DATA* column contains the value *`English`*

1.2.3 NOMENCLATURE

Due to the technical nature of this manual, many special terms, abbreviations and acronyms are used throughout the manual. Some of these terms are well-known industry-specific terms while others may be special product-specific terms used by GE Vernova. The first instance of any acronym or term used in a particular chapter is explained. In addition, a separate glossary is available on the GE Vernova website, or from the GE Vernova contact centre.

We would like to highlight the following changes of nomenclature however:

- The word 'relay' is no longer used to describe the device itself. Instead, the device is referred to as the 'IED' (Intelligent Electronic Device), the 'device', or the 'product'. The word 'relay' is used purely to describe the electromechanical components within the device, i.e. the output relays.
- British English is used throughout this manual.
- The British term 'Earth' is used in favour of the American term 'Ground'.

1.2.4 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

1.3 PRODUCT SCOPE

The P543 and P546 devices have been designed for current differential protection of overhead line and cable applications, as well as solidly grounded systems and Petersen Coil grounded systems. The products within this range interface readily with the longitudinal (end-end) communications channel between line terminals. The P543 device applies to single circuit breaker applications and the P546 device is for dual circuit breaker applications.

The P54 includes high-speed current differential unit protection with optional high performance sub-cycle distance protection, including phase segregated aided directional earth fault protection as well as in-zone transformer differential protection (P543) and 4-shot phase-segregated autoreclose protection.

The P54 can be ordered in 40/60/80TE cases with several different digital input/output options also offered.

The P54 is available with conventional 1A/5A CT inputs and 100/120V VT inputs or with a IEC 61850-9-2LE redundant Ethernet process bus input for sampled analogue values. Unlike a conventional IED, a device with an IEC 61850-9-2 interface, or Sampled Value (SV) device accepts current and voltage measurement inputs, which have already been digitised in accordance with the IEC 61850-9-2LE standard. The IEC 61850-9-2LE version of the 5th Generation IED accepts sampled analogue values from merging units. It does not accept analogue values directly and therefore does not have any current or voltage transformers. This provides a number of advantages over conventional devices, which are discussed throughout this technical manual.

The differences between the model variants are summarised in the table below:

Feature/Variant	P543	P546
Number of CT Inputs	5	8
Number of VT inputs	4	5
Opto-coupled digital inputs	8-40	8-24
Standard relay output contacts	7-43	7-32
High speed high break output contacts	4-8	4-8

The 5 VTs model allow flexible configuration options, where one can be used to measure the residual voltage if required. To do this, you must first set all relevant residual voltage input settings to measured, then the ***VT2 Selection*** setting to `Broken Delta`.

1.3.1 PRODUCT VERSIONS

Products detailed in this manual belong to the 5th Generation of P40 protection devices.

The P54 relay software is based on 4th Generation software (SW):

- P543, P545 - 91SW
- P544, P546 - 82SW
- P546 - 84SW and 86SW (specific features)

5th Generation P543 and P546 models cover the digital input and output options of 4th Generation P543/5 single breaker and P544/6 dual breaker versions, so the P544/5 models are not needed in the P54 CORTEC. An IEC 61850-9-2LE option is included for P543/6 single and dual breaker models, which was previously only available on the P546 model. P54 models are available in 40TE/60TE/80TE case sizes, whereas previous P543-6 models only offered 60/80TE.

In the P54 CORTEC the line differential channel options and digital I/O options use separate digits to make selection of these options simpler and more flexible. A new order option is also included to select subcylce 1/3 pole tripping transmission distance protection or non subcycle subtransmission/distribution distance protection with 3 Pole tripping only. The non subcycle distance protection aligns with the distance protection in the 4th Generation P445 model. Rear communication port protocol is selectable in the settings, so there is no CORTEC option. For 4th Generation this was required as an order option.

1.3.2 ORDERING OPTIONS

All current models and variants for this product are defined in an interactive spreadsheet called the CORTEC. This is available on the company website.

Alternatively, you can obtain it via the Contact Centre at:

GA.support@gevernova.com

A copy of the CORTEC is also supplied as a static table in the Appendices of this document. However, it should only be used for guidance as it provides a snapshot of the interactive data taken at the time of publication.

1.4 FEATURES AND FUNCTIONS

1.4.1 CURRENT DIFFERENTIAL PROTECTION FUNCTIONS

Feature	IEC 61850	ANSI
Phase segregated current differential protection	DifPDIF1	87L
Neutral current differential protection (optional)	DifPDIF2	87N
2 and 3 terminal lines/cables		
Feeders with in-zone transformers (P543)		87T
Suitable for use with SDH/SONET networks (using RT430)		
GPS time synchronisation (optional)		
InterMiCOM^{64} teleprotection for direct device-to-device communication (optional)		

1.4.2 DISTANCE PROTECTION FUNCTIONS

Feature	IEC 61850	ANSI
Distance zones, full-scheme protection (9)	DisPDIS	21/21N
Phase characteristic (Mho and quadrilateral)		
Ground characteristic (Mho and quadrilateral)		
CVT transient overreach elimination		
Load blinder		
Easy setting mode		
Communication-aided schemes, PUTT, POTT, Blocking, Weak Infeed	DisPSCH	85
Accelerated tripping - loss of load and Z1 extension		
Switch on to fault and trip on reclose - elements for fast fault clearance on breaker closure	SofPSOF/ TorPSOF	50SOTF/27SOTF
Power swing blocking	PsbRPSB	68
Directional earth fault (DEF) unit protection		67N
Out of step	OstRPSB	78
Delta directional comparison - fast channel schemes operating on fault generated superimposed quantities		78DCB/78DCUB
Mutual compensation (for fault locator and distance zones)		
Cross-country fault detection		
InterMiCOM^{64} teleprotection for direct device-to-device communication (optional)		

1.4.3 PROTECTION FUNCTIONS

Feature	IEC 61850	ANSI
Tripping mode (1 & 3 pole)	PTRC	
ABC and ACB phase rotation		
Phase overcurrent, with optional directionality (4 stages)	OcpPTOC/RDIR	50/51/67

Feature	IEC 61850	ANSI
Earth/Ground overcurrent stages, with optional directionality (4 stages)	EfdPTOC/RDIR	50N/51N/ 67N
Sensitive earth fault (SEF) (4 stages)	SenPTOC/RDIR	50N/51N/67N
High impedance restricted earth fault (REF)	SenRefPDIF	64
Transient Earth Fault Detection (TEFD)	PTEF	
Negative sequence overcurrent stages, with optional directionality (4 stages)	NgcPTOC/RDIR	67/46
Broken conductor, used to detect open circuit faults		46
Thermal overload protection	ThmPTTR	49
Phase directional power (4 stages)	PdpPDOP/PDUP	32
Undervoltage protection (2 stages)	VtpPhsPTUV	27
Overvoltage protection (2 stages)	VtpPhsPTOV	59
Remote overvoltage protection (2 stages)	VtpCmpPTOV	59R
Residual voltage protection (2 stages)	VtpResPTOV	59N
Underfrequency protection (4 stages)	FrqPTUF	81
Overfrequency protection (2 stages)	FrqPTOF	81
Rate of change of frequency protection (4 stages)	DfpPFRC	81
High speed breaker fail suitable for re-tripping and back-tripping (2 stages)	RBRF	50BF
Current transformer supervision		46
Voltage transformer supervision	TVTR	47/27
Auto-reclose (4 shots)	RREC	79
Check synchronisation (2 stages)	RSYN	25

1.4.4 CONTROL FUNCTIONS

Feature	IEC 61850	ANSI
Watchdog contacts		
Read-only mode		
Function keys	FnkGGIO	
Programmable LEDs	LedGGIO	
Programmable allocation of digital inputs and outputs		
Fully customizable menu texts		
Circuit breaker control, status & condition monitoring	XCBR	52
Trip circuit and coil supervision		
Control inputs	PloGGIO1	
Power-up diagnostics and continuous self-monitoring		
Dual rated 1A and 5A CT inputs		
Alternative setting groups (4)		
Graphical programmable scheme logic (PSL)		
Fault locator	RFLO	

1.4.5 MEASUREMENT FUNCTIONS

Measurement Function	IEC 61850	ANSI
Measurement of all instantaneous & integrated values (Exact range of measurements depend on the device model)		MET
Disturbance recorder for waveform capture - specified in samples per cycle	RDRE	DFR
Fault Records		
Maintenance Records		
Event Records/Event logging		Event records
Time Stamping of Opto-inputs	Yes	Yes

1.4.6 COMMUNICATION FUNCTIONS

Feature	ANSI
NERC compliant cyber-security	
Front USB communication port for configuration	
Rear serial RS485 communication port for SCADA control--Courier/DNP 3.0/IEC 60870-5-103 protocol selectable in settings	16S
Rear serial FO communication ports for SCADA control (optional) – Courier/DNP 3.0/IEC 60870-5-103 protocol selectable in settings	16S
Ethernet communication (optional)--IEC 61850 protocol	16E
Redundant Ethernet communication (optional)--IEC 61850 protocol	16E
Rear Ethernet engineering port for configuration	16E
SNMP	16E
IRIG-B modulated and unmodulated time synchronisation (optional)	CLK
IEEE 1588 PTP	

1.5 LOGIC DIAGRAMS

This technical manual contains many logic diagrams, which should help to explain the functionality of the device. Although this manual has been designed to be as specific as possible to the chosen product, it may contain diagrams, which have elements applicable to other products. If this is the case, a qualifying note will accompany the relevant part.

The logic diagrams follow a convention for the elements used, using defined colours and shapes. A key to this convention is provided below. We recommend viewing the logic diagrams in colour rather than in black and white. The electronic version of the technical manual is in colour, but the printed version may not be. If you need coloured diagrams, they can be provided on request by calling the contact centre and quoting the diagram number.

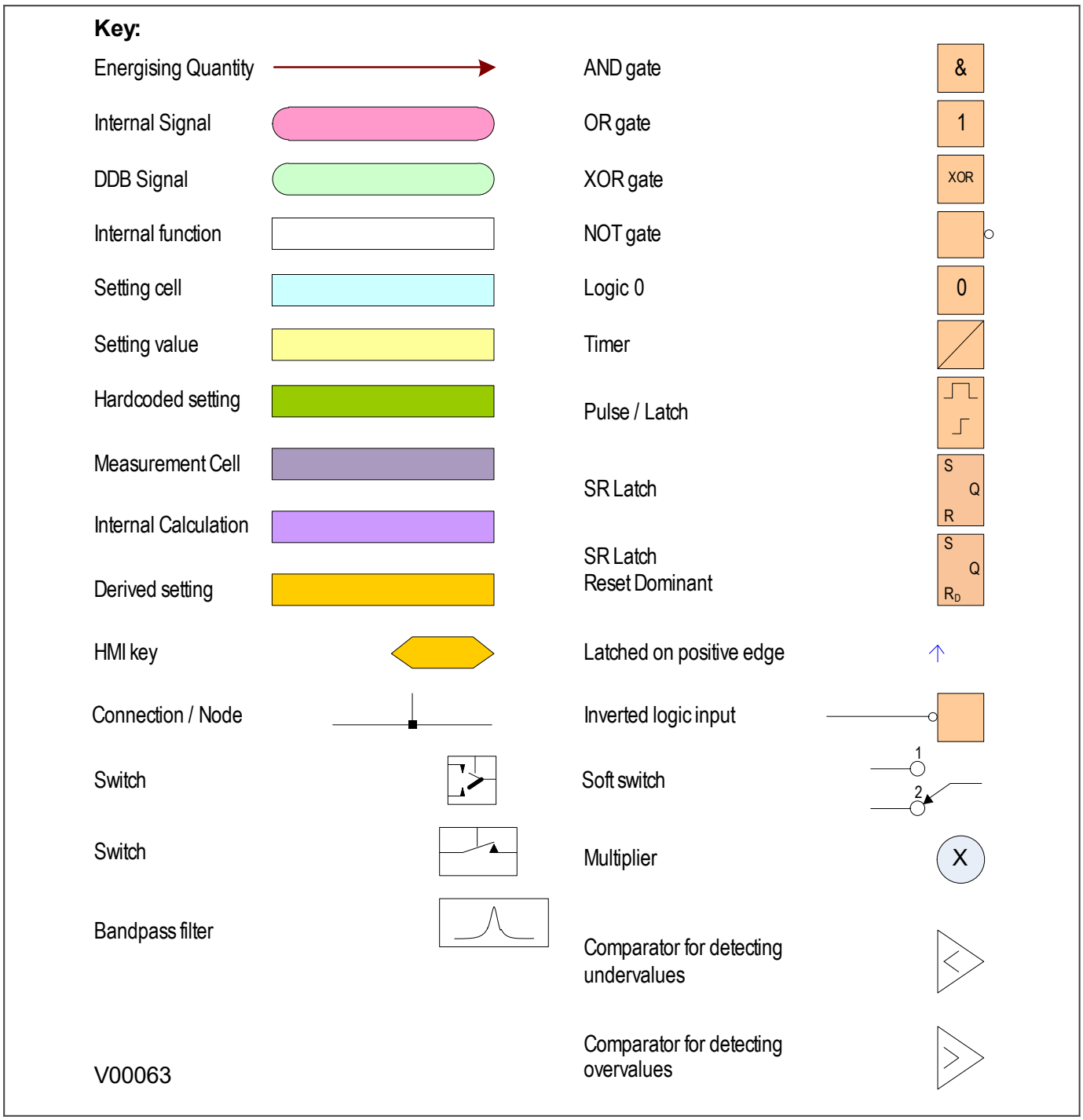


Figure 1: Key to logic diagrams

1.6 FUNCTIONAL OVERVIEW

This diagram is applicable to P54 product models. Use the key on the diagram to determine the features relevant to the product described in this technical manual.

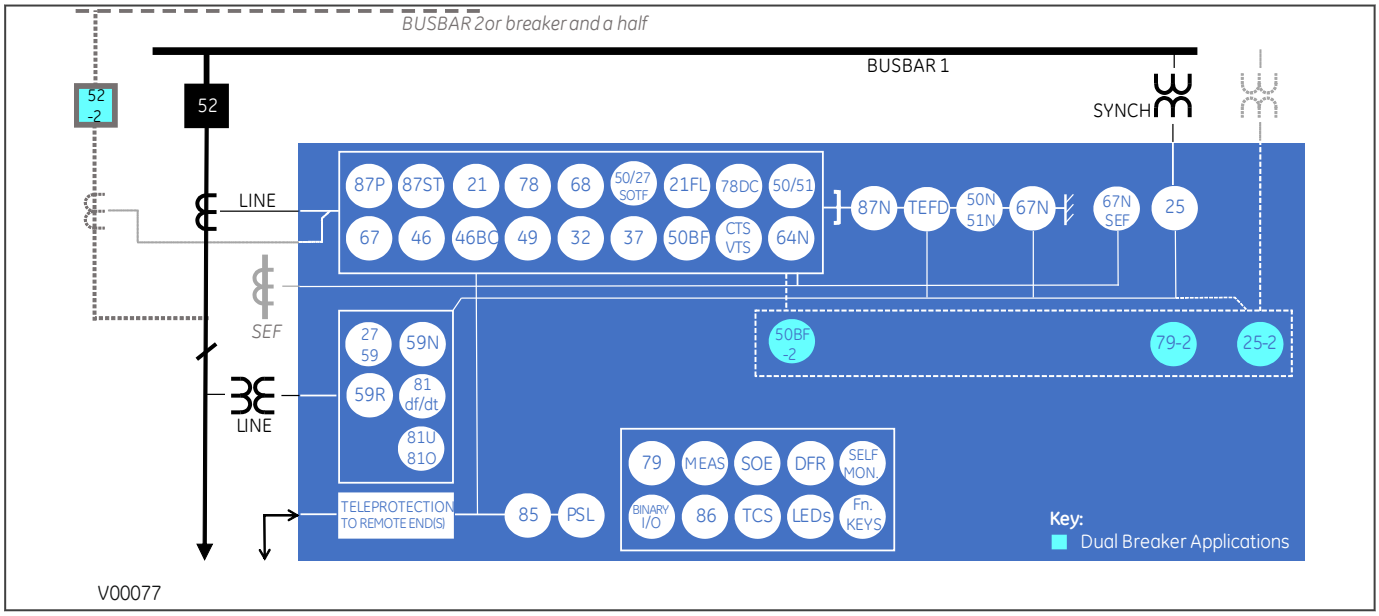


Figure 2: Functional overview

The following table lists the P54 ANSI numbers and the corresponding function descriptions:

Device Number	Function
25	Check Sychronising
27	Phase and Line Undervoltage
32	Directional Power Protection
37	Undercurrent
46	Negative Sequence Overcurrent
49	Thermal Overload
50	Phase Definite Time Overcurrent
51	Phase Inverse-Time Overcurrent
52	Circuit Breaker Control
59	Phase and Line Overvoltage
67	Directional Phase Overcurrent
68	Power Swing blocking
78	Out-of-Step Tripping
78DC	Delta (Increment) Protection
79	Autoreclose/Adaptive Autoreclose
85	Teleprotection Channel Schemes
86	Latching/Lockout Contacts
87P	Line Differential – 2 or 3 Ends

Device Number	Function
87N	Neutral Differential
87ST	Stub Bus Protection
21BL	Load Encroachment/Blinder
21FL	Fault Locator
21P/G	Phase and Ground Distance
46BC	Broken Conductor
50/27	Switch-on to Fault
50BF	CB Failure
50N	Earth Fault Definite Time Overcurrent
50ST	Stub Bus Protection
51N	Neutral/Ground IDMT Overcurrent
59N	Neutral Voltage Displacement
59R	Remote End Overvoltage
64N	Restricted Earth Fault
67N	Directional Neutral/Ground Overcurrent
81df/dt	Rate of Change of Frequency
81O	Overfrequency
81U	Underfrequency
CTS	CT Supervision
PSL	Programmable Logic
SEF	Sensitive Earth Fault
TEFD	Transient Earth Fault Detection
TCS	Trip Circuit Supervision
VTS	VT Supervision

CHAPTER 2

SAFETY INFORMATION

2.1 CHAPTER OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

This chapter contains the following sections:

Chapter Overview 15

Health and Safety 16

Symbols 17

Installation, Commissioning and Servicing 18

Decommissioning and Disposal 24

Regulatory Compliance 25

2.2 HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- Familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- Familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- Trained in the care and use of safety apparatus in accordance with safety engineering practises
- Tained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

2.3 SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.



Caution:
Refer to equipment documentation. Failure to do so could result in damage to the equipment



Warning:
Risk of electric shock



Warning:
Risk of damage to eyesight



Earth terminal. *Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.*



Protective conductor (earth) terminal



Instructions on disposal requirements

Note:
The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

2.4 INSTALLATION, COMMISSIONING AND SERVICING

2.4.1 LIFTING HAZARDS

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

2.4.2 ELECTRICAL HAZARDS



Caution:
All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.



Caution:
Consult the equipment documentation before installing, commissioning, or servicing the equipment.



Caution:
Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.



Warning:
Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.



Warning:
Isolate the equipment before working on the terminal strips.



Warning:
Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.



Caution:
Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.



Warning:
NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.



Warning:
Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.



Caution:
Operate the equipment within the specified electrical and environmental limits.



Caution:
Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.

Note:
Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

2.4.3 UL/CSA/CUL REQUIREMENTS

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.



Caution:
Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).



Caution:
To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

2.4.4 FUSING REQUIREMENTS



Caution:
Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).



Caution:
Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).
For P50 models, use a 1A maximum T-type fuse.
For P60 models, use a 4A maximum T-type fuse.



Caution:
Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.



Caution:
CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

2.4.5 EQUIPMENT CONNECTIONS



Warning:
Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.



Caution:
Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.
Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.



Caution:
Always use insulated crimp terminations for voltage and current connections.



Caution:
Always use the correct crimp terminal and tool according to the wire size.



Caution:
Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

2.4.6 PROTECTION CLASS 1 EQUIPMENT REQUIREMENTS



Caution:
Earth the equipment with the supplied PCT (Protective Conductor Terminal).



Caution:
Do not remove the PCT.



Caution:
The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.



Caution:
Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.



Caution:
The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations. For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.



Caution:
The PCT connection must have low-inductance and be as short as possible.



Caution:
All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

2.4.7 PRE-ENERGISATION CHECKLIST



Caution:
Check voltage rating/polarity (rating label/equipment documentation).



Caution:
Check CT circuit rating (rating label) and integrity of connections.



Caution:
Check protective fuse or miniature circuit breaker (MCB) rating.



Caution:
Check integrity of the PCT connection.



Caution:
Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

2.4.8 PERIPHERAL CIRCUITRY



Warning:
Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.

Note:
For most GE Vernova equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.



Caution:
Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.



Warning:
Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.



Warning:
Data communication cables with accessible screens and/or screen conductors, (including optical fibre cables with metallic elements), may create an electric shock hazard in a sub-station environment if both ends of the cable screen are not connected to the same equipotential bonded earthing system.

To reduce the risk of electric shock due to transferred potential hazards:

i. The installation shall include all necessary protection measures to ensure that no fault currents can flow in the connected cable screen conductor.

ii. The connected cable shall have its screen conductor connected to the protective conductor terminal (PCT) of the connected equipment at both ends. This connection may be inherent in the connectors provided on the equipment but, if there is any doubt, this must be confirmed by a continuity test.

iii. The protective conductor terminal (PCT) of each piece of connected equipment shall be connected directly to the same equipotential bonded earthing system.

iv. If, for any reason, both ends of the cable screen are not connected to the same equipotential bonded earth system, precautions must be taken to ensure that such screen connections are made safe before work is done to, or in proximity to, any such cables.

v. No equipment shall be connected to any download or maintenance circuits or connectors of this product except temporarily and for maintenance purposes only.

vi. Equipment temporarily connected to this product for maintenance purposes shall be protectively earthed (if the temporary equipment is required to be protectively earthed), directly to the same equipotential bonded earthing system as the product.



Warning:
Small Form-factor Pluggable (SFP) modules which provide copper Ethernet connections typically do not provide any additional safety isolation. Copper Ethernet SFP modules must only be used in connector positions intended for this type of connection.

2.4.9 UPGRADING/SERVICING



Warning:
Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.



Caution:
Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

2.5 DECOMMISSIONING AND DISPOSAL



Caution:
Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.



Caution:
Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.

2.6 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

2.6.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

2.6.3 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL US

2.6.4 UKCA COMPLIANCE

Compliance with the UK Directive on EMC and Safety is demonstrated using a technical file.

UK CA

2.6.5 EMC COMPLIANCE: ELECTROMAGNETIC COMPATIBILITY REGULATIONS 2016

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.6 SAFETY COMPLIANCE: ELECTRICAL EQUIPMENT (SAFETY) REGULATIONS 2016

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the Safety Regulations. Safety related information, such as the

installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

2.6.7 MOROCCO COMPLIANCE

Compliance with the Morocco Directive on EMC and Safety is demonstrated using a technical file.



2.6.8 EMC COMPLIANCE: NO. 2574-14 OF RAMADAN 1436

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.9 SAFETY COMPLIANCE: NO. 2573-14 OF RAMADAN 1436

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the Safety Directive. Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

CHAPTER 3

HARDWARE DESIGN

3.1 CHAPTER OVERVIEW

This chapter provides information about the product's hardware design.

This chapter contains the following sections:

Chapter Overview 28
Hardware Architecture 29
Mechanical Implementation 31
Front Panel 33
Rear Panel 37
Boards and Modules 39

3.2 HARDWARE ARCHITECTURE

The main components comprising devices based on the Px4x platform are as follows:

- The housing, consisting of a front panel and connections at the rear
- The Main processor module consisting of the main CPU (Central Processing Unit), memory and an interface to the front panel HMI (Human Machine Interface)
- A selection of plug-in boards and modules with presentation at the rear for the power supply, communication functions, digital I/O, analogue inputs, and time synchronisation connectivity

All boards and modules are connected by a parallel data and address bus, which allows the processor module to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sampled data from the input module to the CPU. These parallel and serial databuses are shown as a single interconnection module in the following figure, which shows typical modules and the flow of data between them.

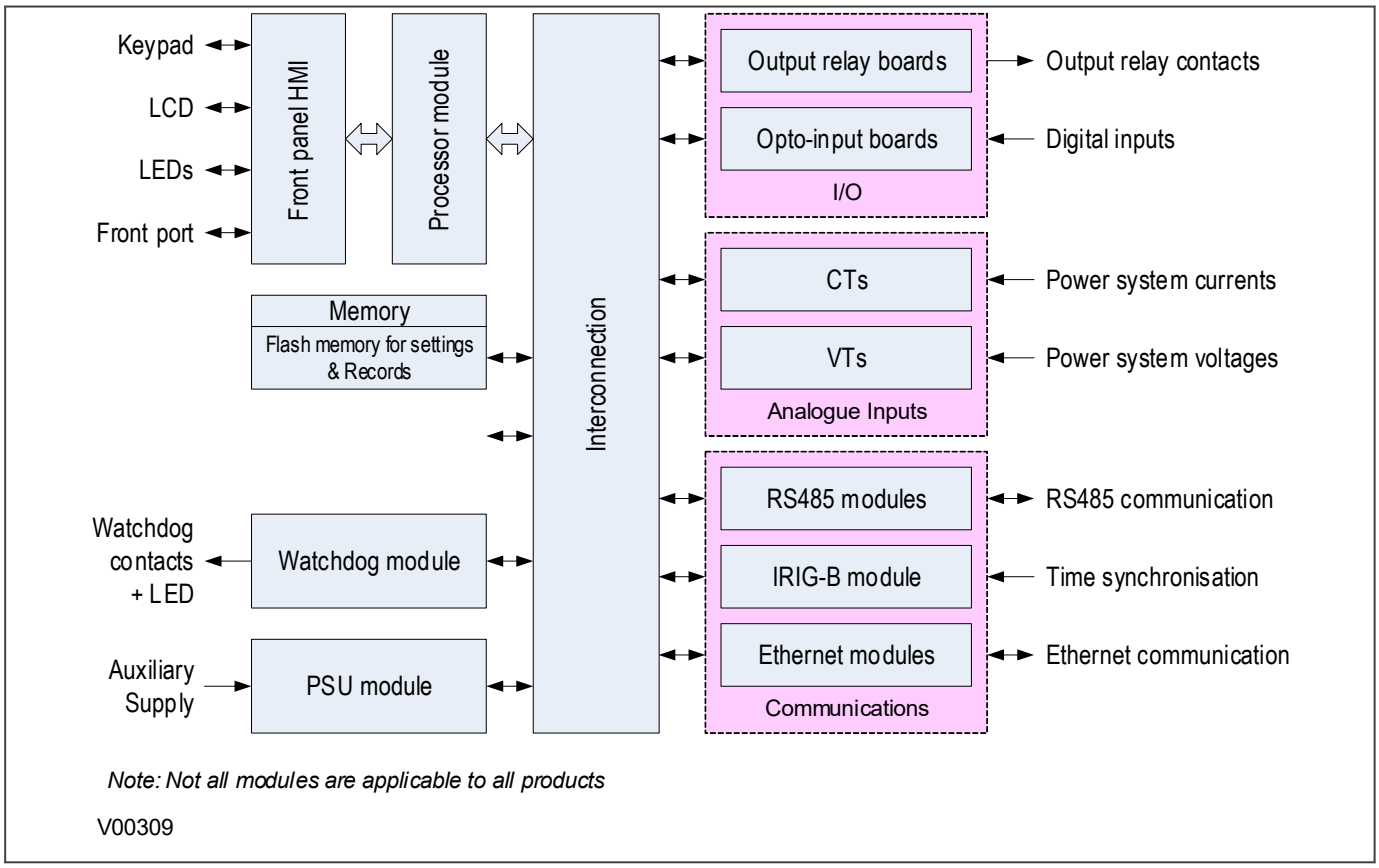


Figure 3: Hardware architecture

3.2.1 COPROCESSOR HARDWARE ARCHITECTURE

Some products are equipped with a coprocessor board for extra computing power. There are several variants of coprocessor board, depending on the required communication requirements. Some models do not need any external communication inputs, some models need inputs for current differential functionality and some models need an input for GPS time synchronisation.

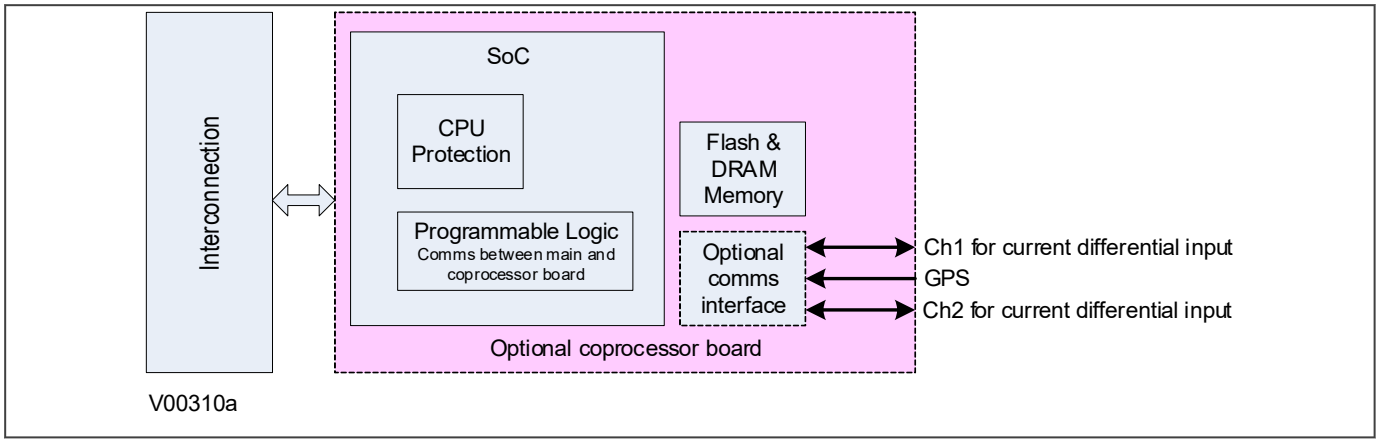


Figure 4: Coprocessor hardware architecture

3.3 MECHANICAL IMPLEMENTATION

All products based on the Px4x platform have common hardware architecture. The hardware is modular and consists of the following main parts:

- Case and terminal blocks
- Boards and modules
- Front panel

The case comprises the housing metalwork and terminal blocks at the rear. The boards fasten into the terminal blocks and are connected together by a ribbon cable. This ribbon cable connects to the processor in the front panel.

The following diagram shows an exploded view of a typical product. The diagram shown does not necessarily represent exactly the product model described in this manual.

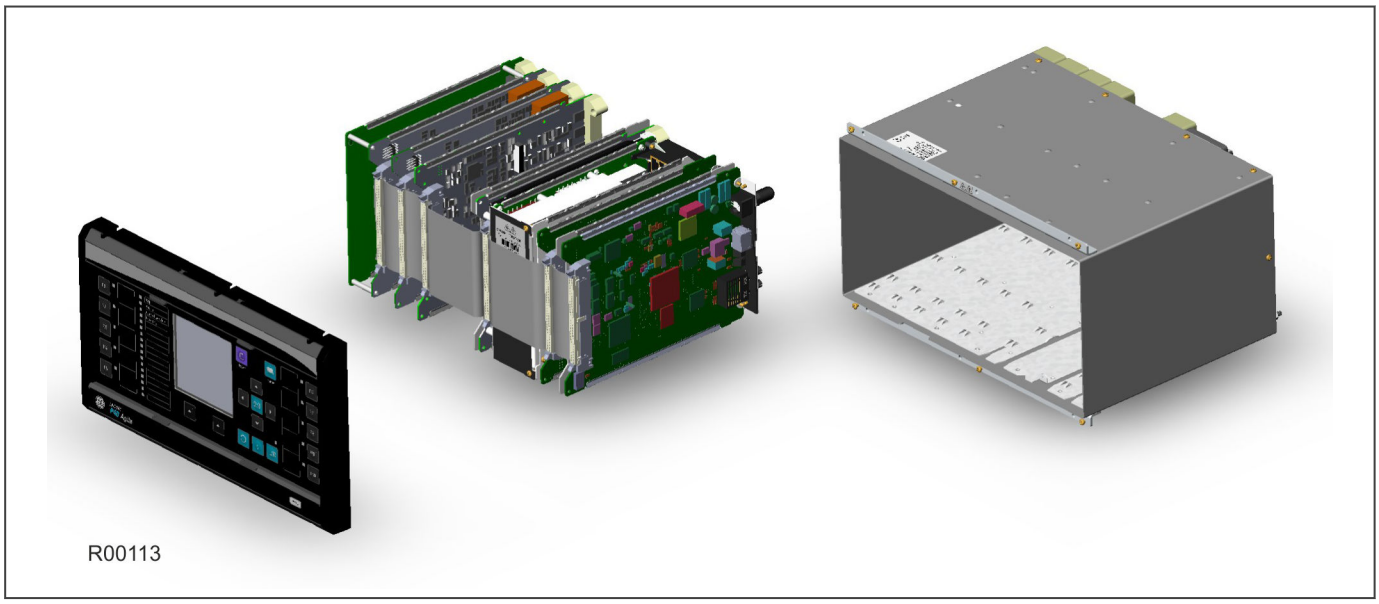


Figure 5: Exploded view of IED

3.3.1 HOUSING VARIANTS

The Px4x range of products are implemented in a range of case sizes. Case dimensions for industrial products usually follow modular measurement units based on rack sizes. These are: U for height and TE for width, where:

- 1U = 1.75 inches = 44.45 mm
- 1TE = 0.2 inches = 5.08 mm

The products are available in panel-mount or standalone versions. All products are nominally 4U high. This equates to 177.8 mm or 7 inches.

The cases are pre-finished steel with a conductive covering of aluminium and zinc. This provides good grounding at all joints, providing a low resistance path to earth that is essential for performance in the presence of external noise.

The case width depends on the product type and its hardware options. There are three different case widths for the described range of products: 40TE, 60TE and 80TE. The case dimensions and compatibility criteria are as follows:

Case width (TE)	Case width (mm)	Case width (inches)
40TE	203.2	8
60TE	304.8	12
80TE	406.4	16

3.3.2 LIST OF BOARDS

The product's hardware consists of several modules drawn from a standard range. The exact specification and number of hardware modules depends on the model number and variant. Depending on the exact model, the product in question will use a selection of the following boards.

Board	Use
Main Processor board - 40TE or smaller	Main Processor board - without support for function keys
Main Processor board - 60TE or larger	Main Processor board - with support for function keys
Power supply board - 24/54V DC	Power supply input. Accepts DC voltage between 24V and 54V
Power supply board - 48/125V DC	Power supply input. Accepts DC voltage between 48V and 125V
Power supply board - 110/250V DC	Power supply input. Accepts DC voltage between 110V and 125V
Transformer board	Contains the voltage and current transformers
Input board	Contains the A/D conversion circuitry
Input board with opto-inputs	Contains the A/D conversion circuitry + 8 digital opto-inputs
Output relay output board	Standard output relay board
High-break output relay board	Output relay board with high breaking capacity relays
Single Ethernet, universal IRIG-B, IEEE1588, maintenance port	Single LC duplex Ethernet port with universal IRIG-B and 1 RJ45 maintenance/ engineering port
IRIG-B board - modulated input	Interface board for modulated IRIG-B timing signal
Fibre board + IRIG-B	Interface board for fibre-based RS485 connection + demodulated IRIG-B
2nd rear communications board	Interface board for RS232/RS485 connections
2nd rear communications board with IRIG-B input	Interface board for RS232/RS485 + IRIG-B connections
Redundant Ethernet RSTP + PRP + HSR + Failover ports, serial fibre port, universal IRIG-B	2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with IEC 60870-5-103 serial fibre ST ports with on-board universal IRIG-B and 1 RJ45 maintenance/engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover universal IRIG-B	2 RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B and 1 RJ45 maintenance/engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover ports, universal IRIG-B	2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B and 1 RJ45 maintenance/ engineering port
Coprocessor board with dual fibre inputs	Coprocessor board with fibre connections for current differential inputs
Coprocessor board with dual fibre inputs + GPS	Coprocessor board with fibre connections for current differential inputs + GPS input.

3.4 FRONT PANEL

Depending on the exact model and chosen options, the product will be housed in either a 40TE, 60TE or 80TE case. By way of example, the following diagram shows the front panel of a typical unit. The front panels of the products based on 40TE, 60TE and 80TE cases have a lot of commonality and differ only in that the 40TE front panel does not include 10 function keys with their associated user-programmable LEDs.



Figure 6: Front panel (80TE)

The front panel consists of:

- Top and bottom compartments with hinged cover
- LCD display
- Keypad
- USB Type B port inside the bottom compartment
- Fixed function LEDs
- Function keys and LEDs (60TE and 80TE models)
- Programmable LEDs

3.4.1 FRONT PANEL COMPARTMENTS

The top compartment contains labels for the:

- Order code, Serial number and Test ID.

Note:
The Test ID on the label in the top compartment of the front panel is the serial number of the relay and consists of 6 numeric and 1 alphanumeric characters, for example 123456Z. The serial number is also shown in the System Data menu of the HMI. This serial number can be used to obtain the recovery password from the Contact Centre.
The serial number on the label in the top compartment of the front panel is the SAP manufacturing serial number and consists of 8 numeric characters, for example 37123456.

- Current and voltage ratings

The bottom compartment contains:

- USB type B port

3.4.2 HMI PANEL

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the colour LCD display.

The colour LCD display is an active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit and back-light unit. The resolution of the 4.0” TFT-LCD is 480x480 pixels and it can display up to 16.7M colours.

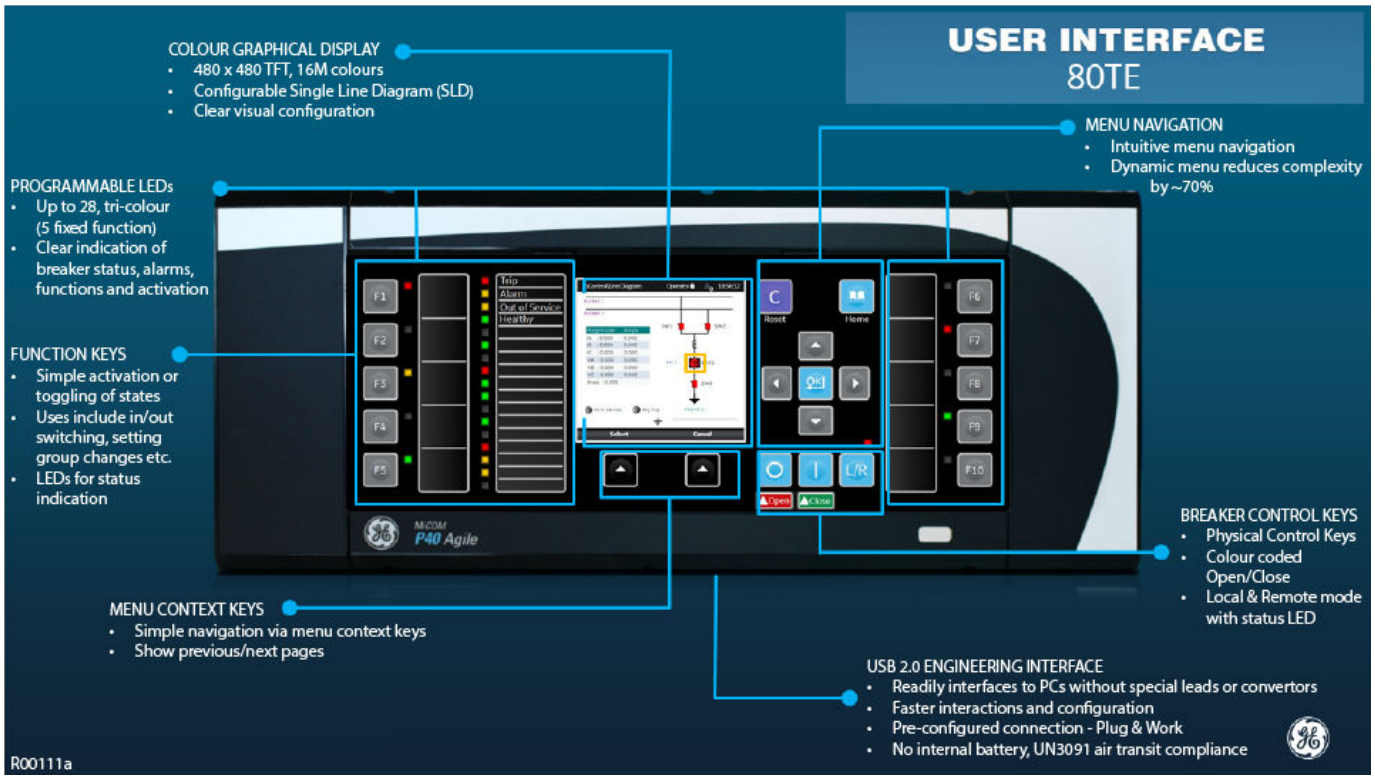
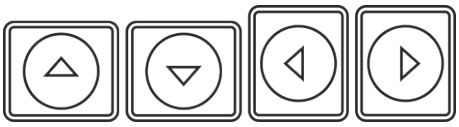
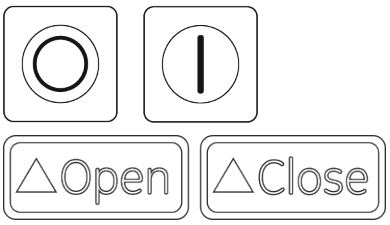


Figure 7: HMI panel

3.4.3 KEYPAD

The keypad consists of the following keys:

4 arrow keys to navigate the menus, changing values within the cell or to select the next item on the SLD (organised around the Enter key).	
An enter key for changing and executing settings. When a bottom banner menu context key label is selected, the OK key can also be used to navigate between pages.	
A clear/reset key for clearing the current setting dialogue or to navigate to the top menu.	

A home key for navigating to the default menu view.	
2 menu context keys used to navigate between pages.	
Open/Close keys (colour coded) **Note:** Colour coding is selectable via labels and configuration of PSL/ SLD.	
Local/remote key to select between local or remote modes.	

3.4.4 USB PORT

The USB port is situated inside the bottom compartment, and is used to communicate with a locally connected PC. It has two main purposes:

- To transfer settings information to/from the PC from/to the device.
- For downloading firmware updates and menu text editing.

The port is intended for temporary connection during testing, installation and commissioning. It is not intended to be used for permanent SCADA communications. This port supports the Courier communication protocol only. Courier is a proprietary communication protocol to allow communication with a range of protection equipment, and between the device and the Windows-based support software package.

You can connect the unit to a PC with a USB cable up to 5 m in length.

The inactivity timer for the front port is set to 15 minutes. This controls how long the unit maintains its level of password access on the front port. If no messages are received on the front port for 15 minutes, any password access level that has been enabled is cancelled.

Note:
The front USB port does not support automatic extraction of event and disturbance records, although this data can be accessed manually.



Caution:
When not in use, always close the cover of the USB port to prevent contamination.

3.4.5 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

3.4.6 FUNCTION KEYS

The programmable function keys are available for custom use for some models.

Factory default settings associate specific functions to these keys, but by using programmable scheme logic, you can change the default functions of these keys to fit specific needs. Adjacent to these function keys are programmable LEDs, which are usually set to be associated with their respective function keys. The device has 10 function keys in the 60TE and 80TE case size models and no function keys in the 40TE case size model.

3.4.7 PROGRAMABLE LEDS

The device has 13 of programmable LEDs, which can be associated with PSL-generated signals. The programmable LEDs are tri-colour and can be set to RED, YELLOW or GREEN.

3.5 REAR PANEL

The MiCOM Px40 series uses a modular construction. Most of the internal structure consists of boards and modules that fit into slots. Some of the boards plug into terminal blocks, which are bolted onto the rear of the unit. However, some boards such as the communications boards have their own connectors. The rear panel consists of these terminal blocks plus the rears of the communications boards.

The back panel cut-outs and slot allocations vary. This depends on the product, the type of boards and the terminal blocks needed to populate the case. The following diagram shows a typical rear view of a case populated with various boards.

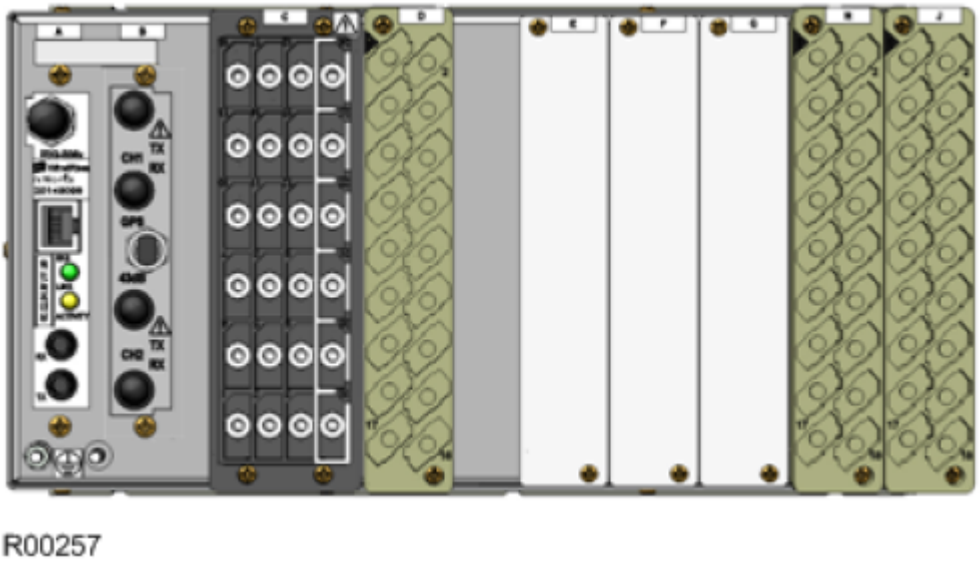


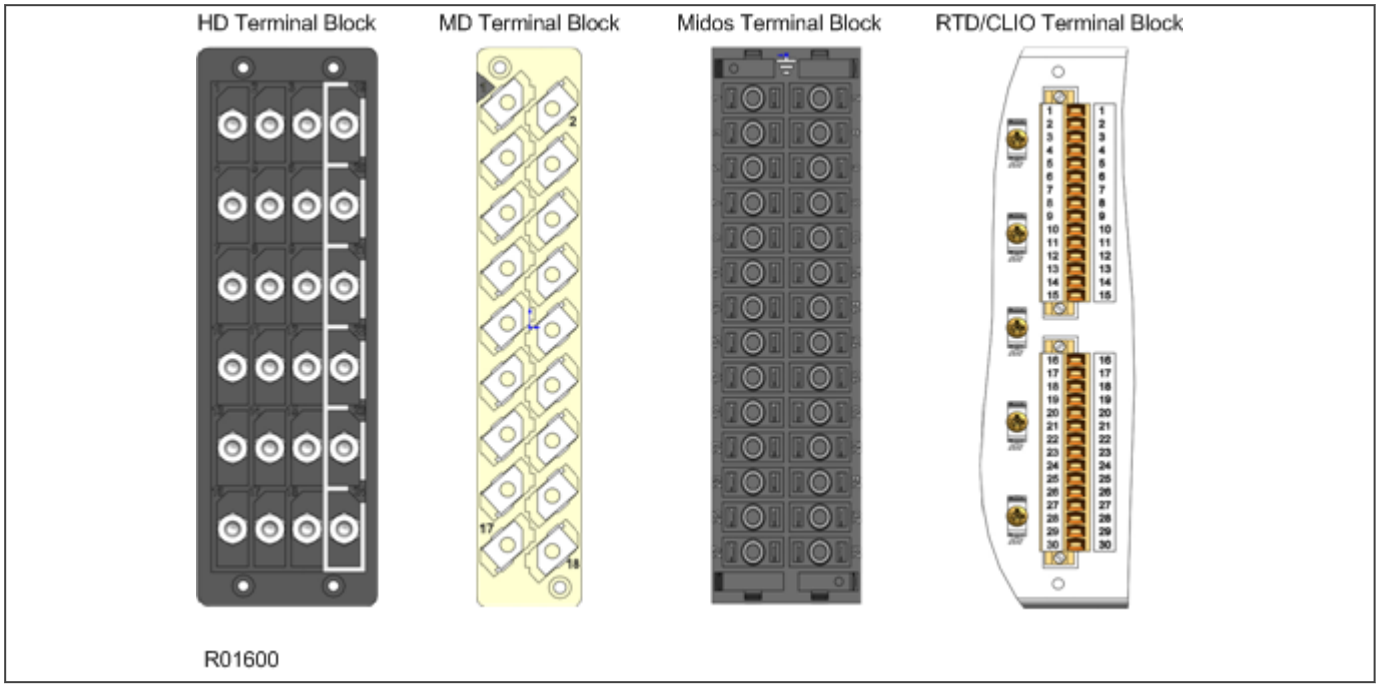
Figure 8: Rear view of populated case

Note:
This diagram is just an example and may not show the exact product described in this manual. It also does not show the full range of available boards, just a typical arrangement.

Not all slots are the same size. The slot width depends on the type of board or terminal block. For example, HD (heavy duty) terminal blocks, as required for the analogue inputs, require a wider slot size than MD (medium duty) terminal blocks. The board positions are not generally interchangeable. Each slot is designed to house a particular type of board. Again this is model-dependent.

The device may use some of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, opto-inputs, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers (refer to CORTEC options)



Note:
Not all products use all types of terminal blocks. The product described in this manual may use one or more of the above types.

3.5.1 TERMINAL BLOCK INGRESS PROTECTION

IP2x shields and side cover panels are designed to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers may be attached during installation or retrofitted to upgrade existing installations - see figure below. For more information, contact your local sales office or our worldwide Contact Centre.

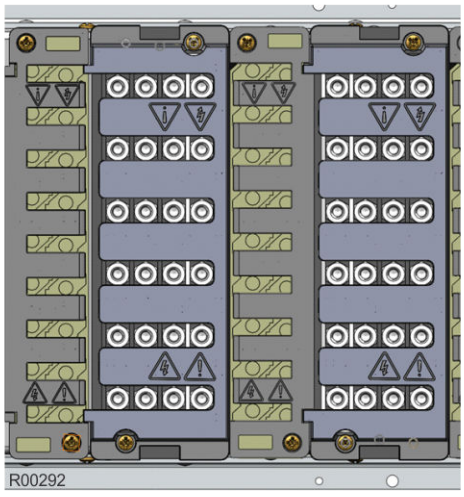


Figure 9: Example - fitted IP2x shields (cabling omitted for clarity)

3.6 BOARDS AND MODULES

Each product comprises a selection of PCBs (Printed Circuit Boards) and subassemblies, depending on the chosen configuration.

3.6.1 PCBS

A PCB typically consists of the components, a front connector for connecting into the main system parallel bus via a ribbon cable, and an interface to the rear. This rear interface may be:

- Directly presented to the outside world (as is the case for communication boards such as Ethernet Boards)
- Presented to a connector, which in turn connects into a terminal block bolted onto the rear of the case (as is the case for most of the other board types)

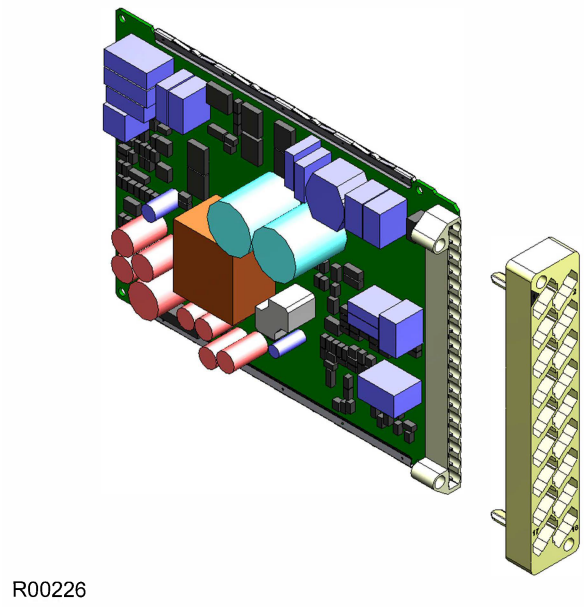


Figure 10: Rear connection to terminal block

3.6.2 SUBASSEMBLIES

A sub-assembly consists of two or more boards bolted together with spacers and connected with electrical connectors. It may also have other special requirements such as being encased in a metal housing for shielding against electromagnetic radiation.

Boards are designated by a part number beginning with ZN, whereas pre-assembled sub-assemblies are designated with a part number beginning with GN. Sub-assemblies, which are put together at the production stage, do not have a separate part number.

The products in the Px40 series typically contain two sub-assemblies:

- The power supply assembly comprising:
  - A power supply board
  - An output relay board
- The input module comprising:
  - One or more transformer boards, which contains the voltage and current transformers (partially or fully populated)
  - One or more input boards
  - Metal protective covers for EM (electromagnetic) shielding

The input module is pre-assembled and is therefore assigned a GN number, whereas the power supply module is assembled at production stage and does not therefore have an individual part number.

3.6.3 MAIN PROCESSOR BOARD

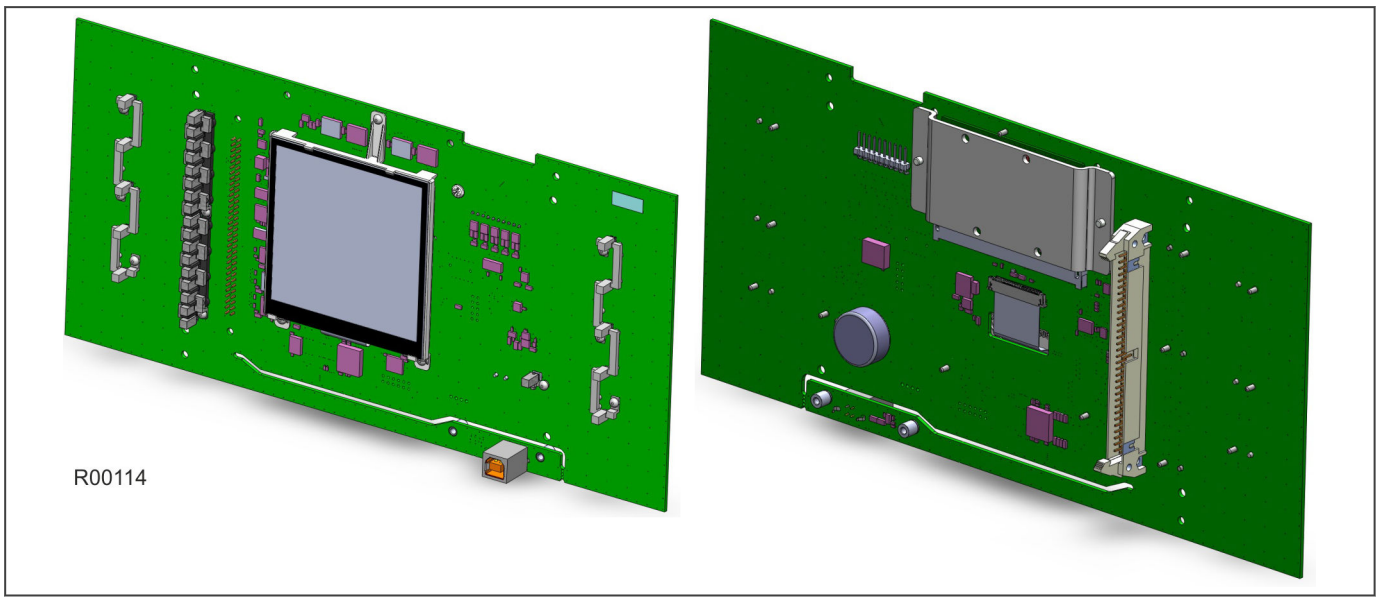


Figure 11: Main processor board

The main processor board performs all calculations and controls the operation of all other modules in the IED, including the data communication and user interfaces. This is the only board that does not fit into one of the slots. It resides in the front panel and connects to the rest of the system using an internal ribbon cable.

The LCD and LEDs are mounted on the processor board along with the front panel communication ports.

The memory on the main processor board is split into two categories: volatile and non-volatile. The volatile memory is DRAM, used by the processor to run the software and store data during calculations. The non-volatile memory is Flash memory and is used to store Product Firmware, text and configuration data including the present setting values, disturbance records, events, fault and maintenance record data.

There are two board types available depending on the size of the case:

- For models in 40TE cases
- For models in 60TE cases and larger

3.6.4 POWER SUPPLY BOARD

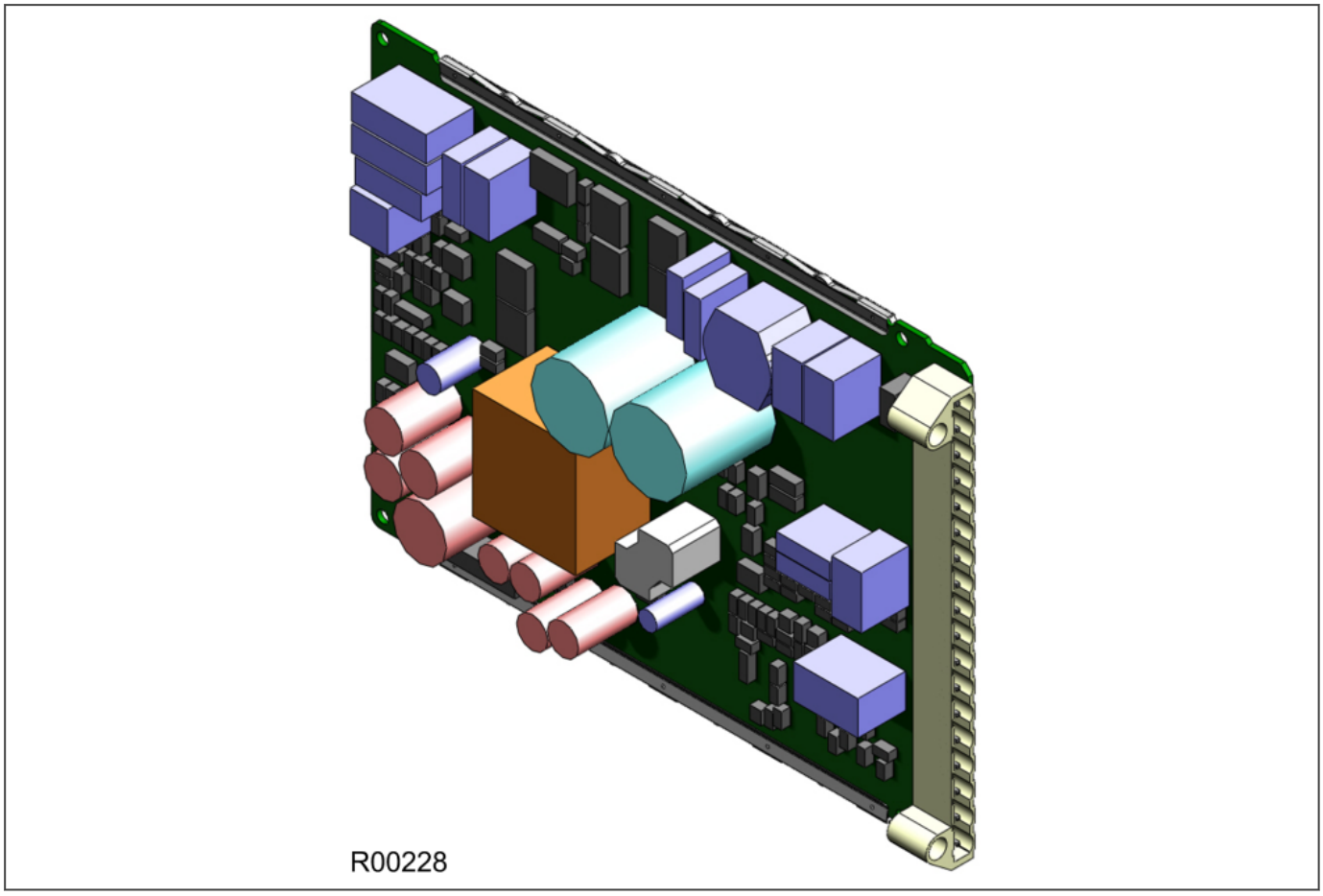


Figure 12: Power supply board

The power supply board provides power to the unit. One of three different configurations of the power supply board can be fitted to the unit. This is specified at the time of order and depends on the magnitude of the supply voltage that will be connected to it.

There are three board types, which support the following voltage ranges:

- 24/54 V DC
- 48/125 V DC or 40-100V AC
- 110/250 V DC or 100-240V AC

The power supply board connector plugs into a medium duty terminal block. This terminal block is always positioned on the right hand side of the unit looking from the rear.

The power supply board is usually assembled together with a relay output board to form a complete subassembly, as shown in the following diagram.

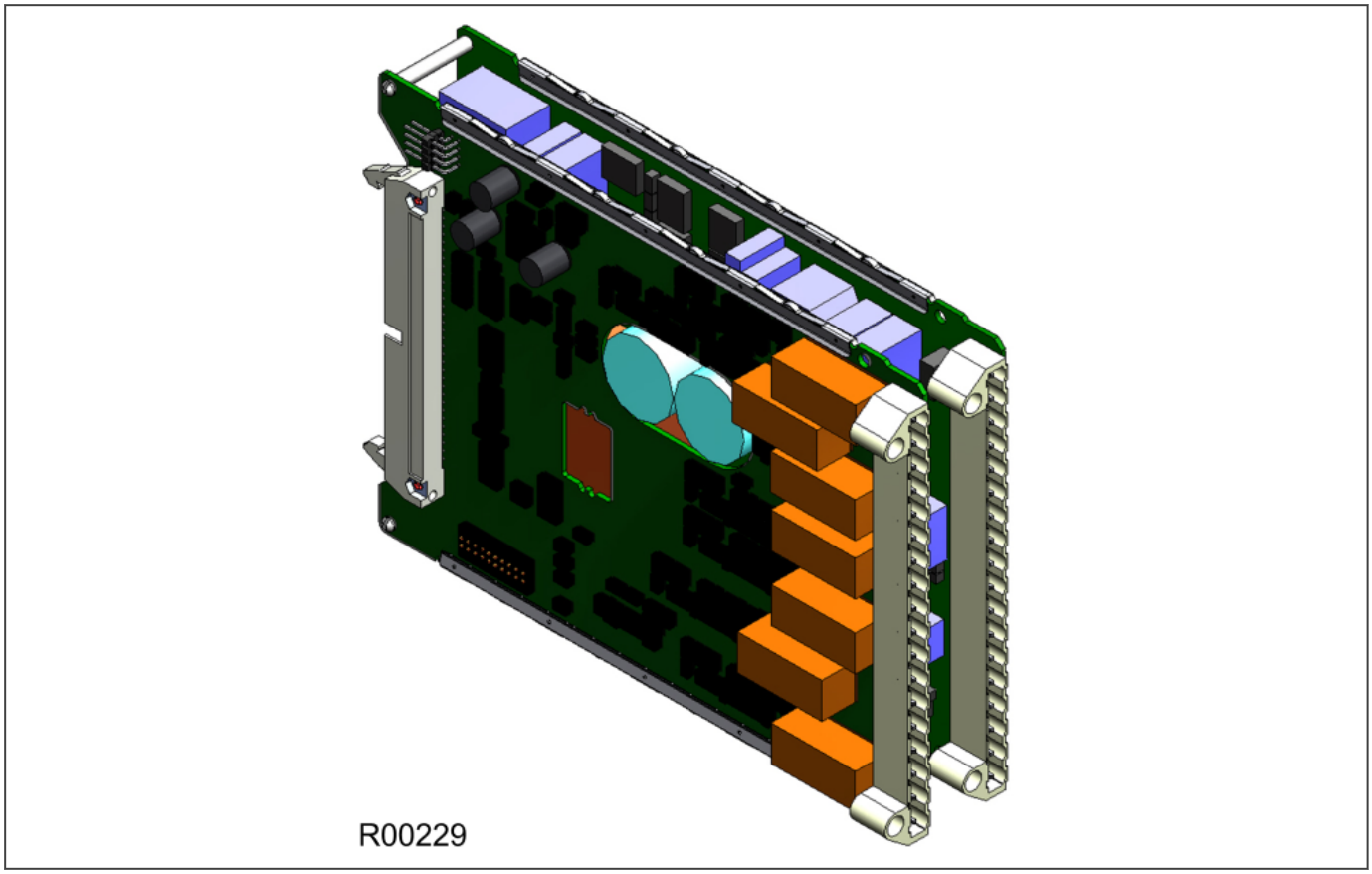


Figure 13: Power supply assembly

The power supply outputs are used to provide isolated power supply rails to the various modules within the unit. Three voltage levels are used by the unit's modules:

- 5.1 V for all of the digital circuits
- +/- 16 V for the analogue electronics such as on the input board
- 22 V for driving the output relay coils.

All power supply voltages, including the 0 V earth line, are distributed around the unit by the 64-way ribbon cable.

The power supply board incorporates inrush current limiting. This limits the peak inrush current to approximately 10 A.

Power is applied to pins 1 and 2 of the terminal block, where pin 1 is negative and pin 2 is positive. The pin numbers are clearly marked on the terminal block as shown in the following diagram.

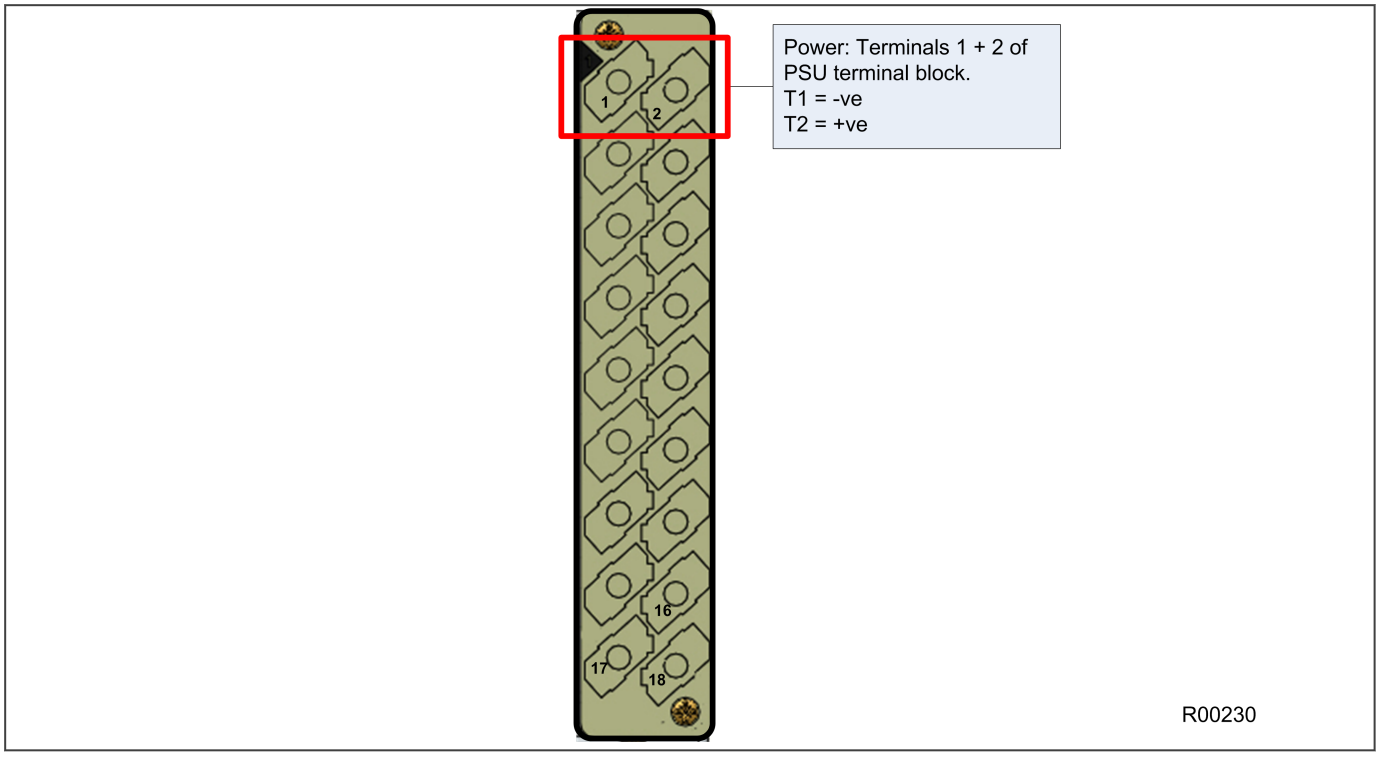


Figure 14: Power supply terminals

3.6.4.1 WATCHDOG

The Watchdog contacts are also hosted on the power supply board. The Watchdog facility provides two output relay contacts, one normally open and one normally closed. These are used to indicate the health of the device and are driven by the main processor board, which continually monitors the hardware and software when the device is in service.

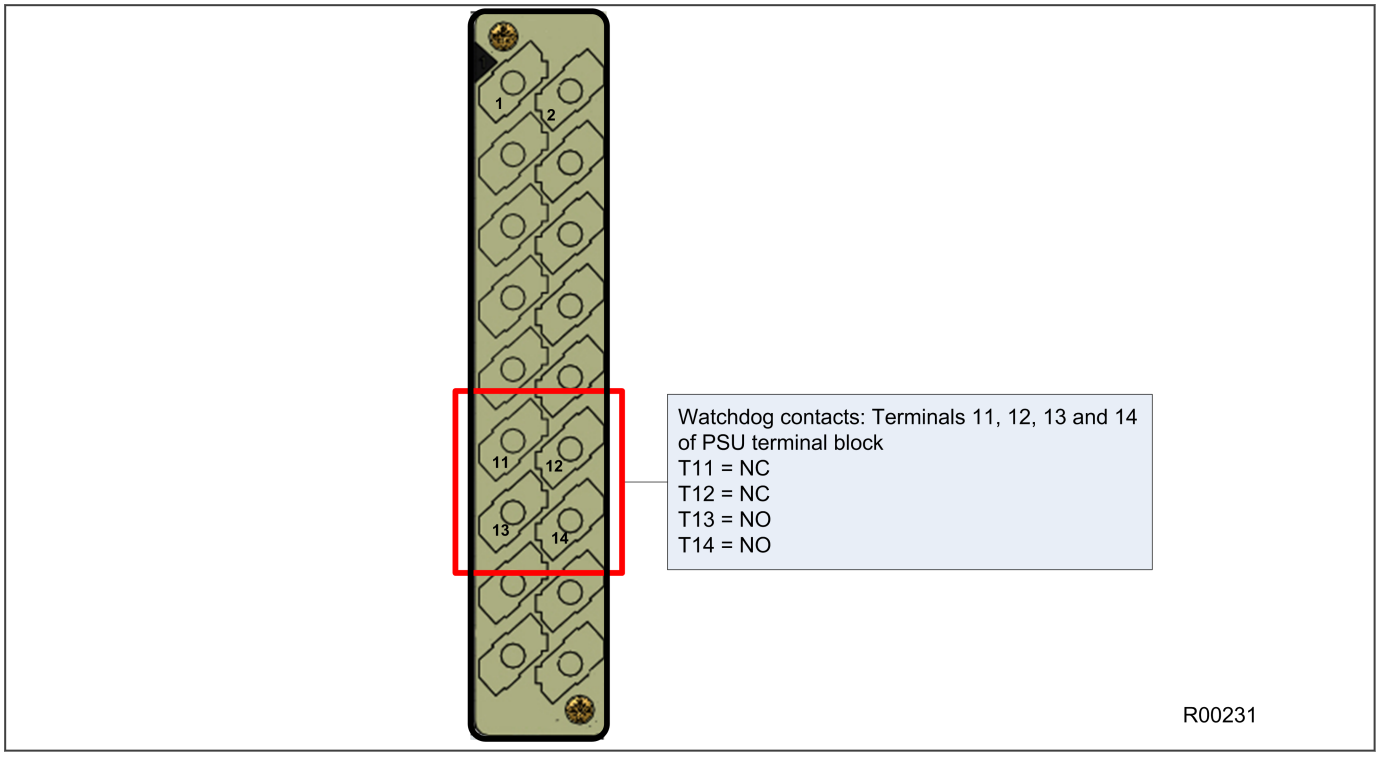


Figure 15: Watchdog contact terminals

3.6.4.2 REAR SERIAL PORT

The rear serial port (RP1) is housed on the power supply board. This is a three-terminal EIA(RS)485 serial communications port and is intended for use with a permanently wired connection to a remote control centre for SCADA communication. The interface supports half-duplex communication and provides optical isolation for the serial data being transmitted and received.

The physical connectivity is achieved using three screw terminals; two for the signal connection, and the third for the earth shield of the cable. These are located on pins 16, 17 and 18 of the power supply terminal block, which is on the far right looking from the rear. The interface can be selected between RS485 and K-bus. When the K-Bus option is selected, the two signal connections are not polarity conscious.

The polarity independent K-bus can only be used for the Courier data protocol. The polarity conscious IEC 60870-5-103 and DNP3.0 protocols need RS485.

The following diagram shows the rear serial port. The pin assignments are as follows:

- Pin 16: Earth shield
- Pin 17: Negative signal
- Pin 18: Positive signal

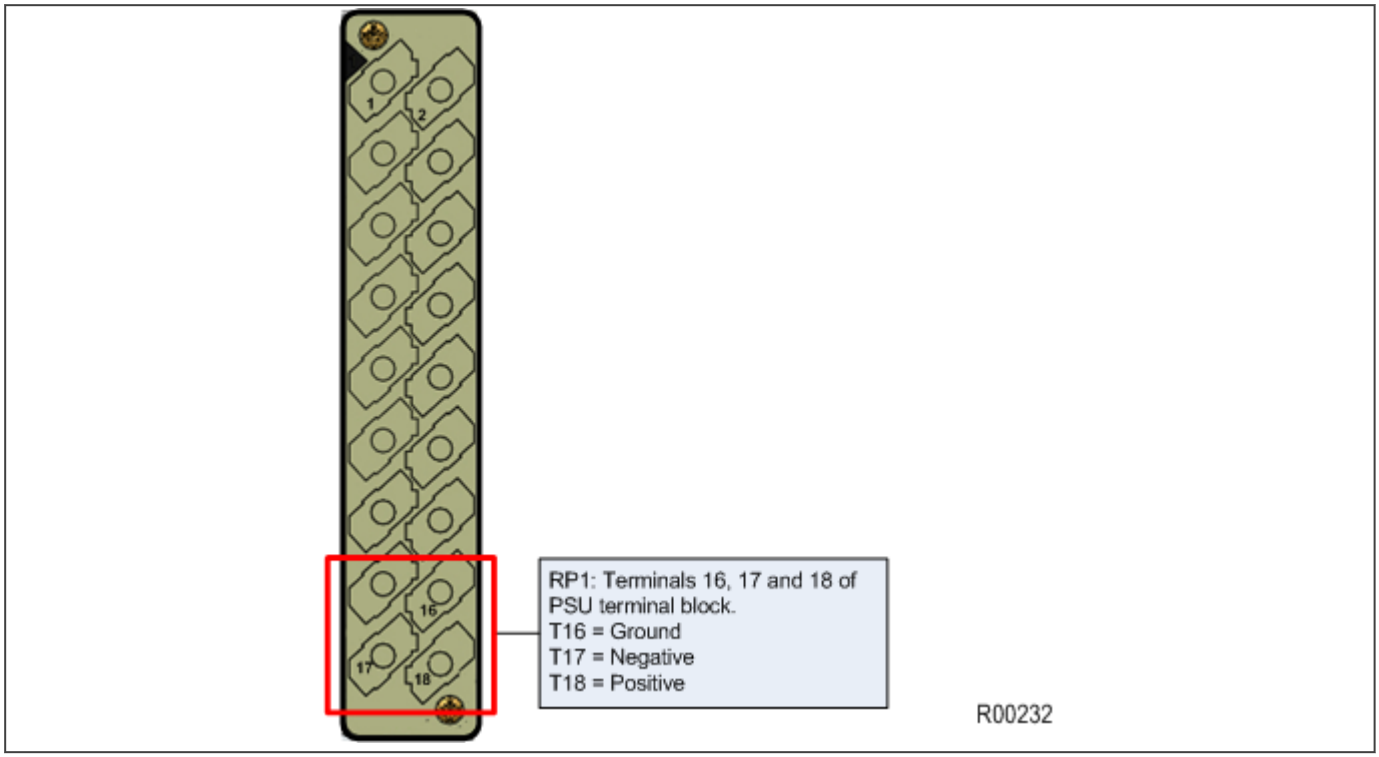


Figure 16: Rear serial port terminals

An additional serial port with D-type presentation is available as an optional board, if required.

3.6.5 INPUT MODULE - 1 TRANSFORMER BOARD

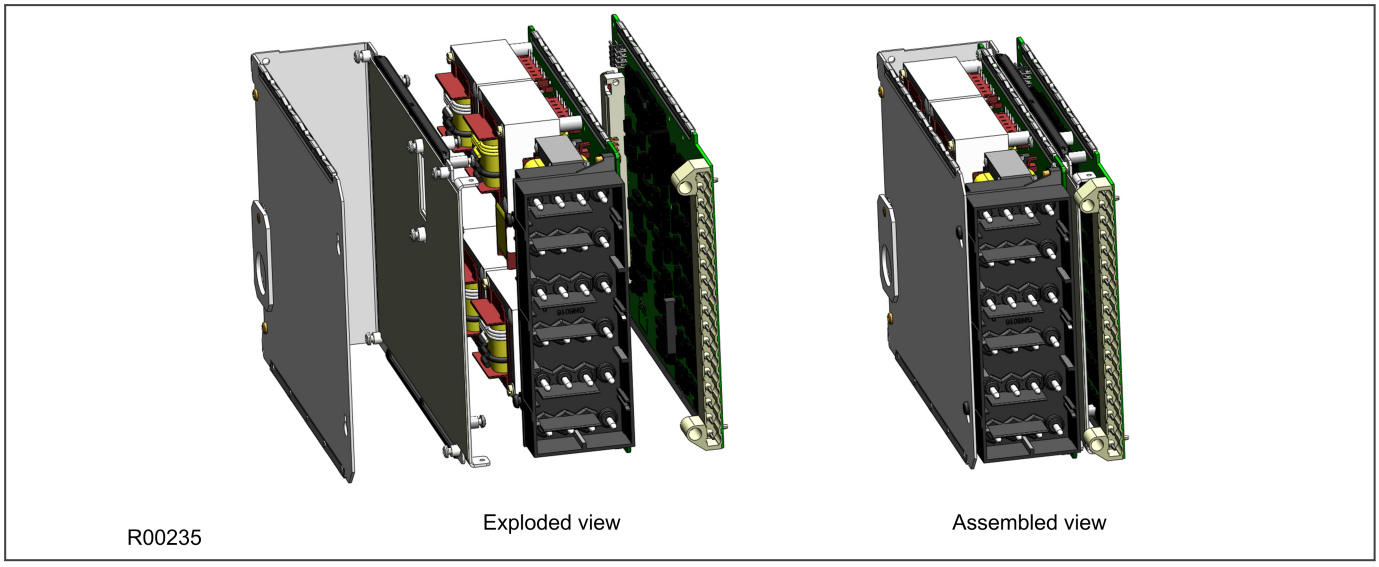


Figure 17: Input module - 1 transformer board

The input module consists of the main input board coupled together with an instrument transformer board. The instrument transformer board contains the voltage and current transformers, which isolate and scale the analogue input signals delivered by the system transformers. The input board contains the A/D conversion and digital processing circuitry, as well as eight digital isolated inputs (opto-inputs).

The boards are connected together physically and electrically. The module is encased in a metal housing for shielding against electromagnetic interference.

3.6.5.1 INPUT MODULE CIRCUIT DESCRIPTION

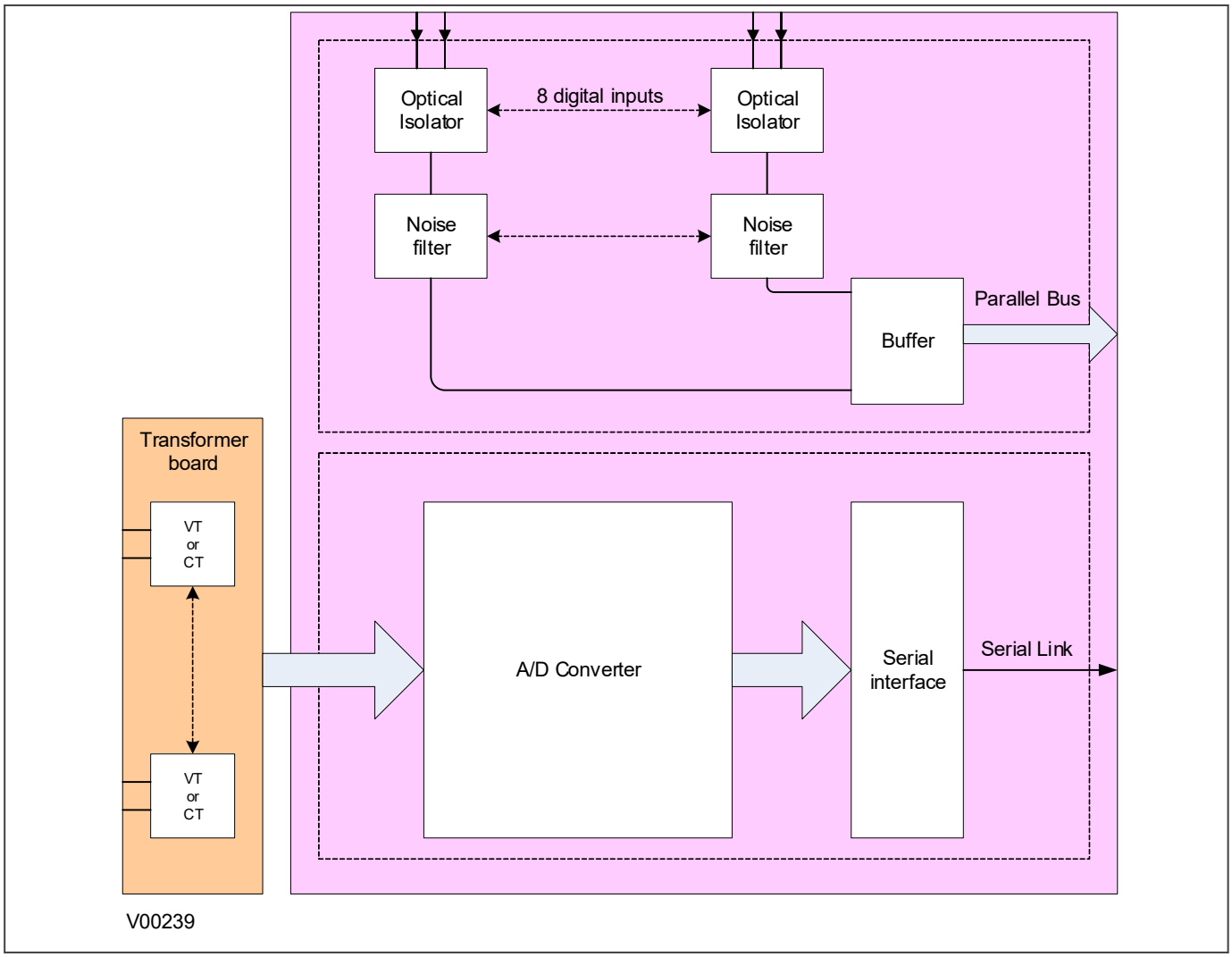


Figure 18: Input module schematic

A/D conversion

The differential analogue inputs from the CT and VT transformers are presented to the main input board as shown. Each differential input is first converted to a single input quantity referenced to the input board's earth potential. The analogue inputs are sampled and converted to digital, then filtered to remove unwanted properties. The samples are then passed through a serial interface module which outputs data on the serial sample data bus.

The calibration coefficients are stored in non-volatile memory. These are used by the processor board to correct for any amplitude or phase errors introduced by the transformers and analogue circuitry.

Opto-isolated inputs

The other function of the input board is to read in the state of the digital inputs. As with the analogue inputs, the digital inputs must be electrically isolated from the power system. This is achieved by means of the 8 on-board optical isolators for connection of up to 8 digital signals. The digital signals are passed through an optional noise filter before being buffered and presented to the unit's processing boards in the form of a parallel data bus.

This selectable filtering allows the use of a pre-set filter of ½ cycle which renders the input immune to induced power-system noise on the wiring. Although this method is secure it can be slow, particularly for inter-tripping. This

can be improved by switching off the ½ cycle filter, in which case one of the following methods to reduce ac noise should be considered.

- Use double pole switching on the input
- Use screened twisted cable on the input circuit

The opto-isolated logic inputs can be configured for the nominal battery voltage of the circuit for which they are a part, allowing different voltages for different circuits such as signalling and tripping.

Note:
The opto-input circuitry can be provided without the A/D circuitry as a separate board, which can provide supplementary opto-inputs.

3.6.5.2 TRANSFORMER BOARD

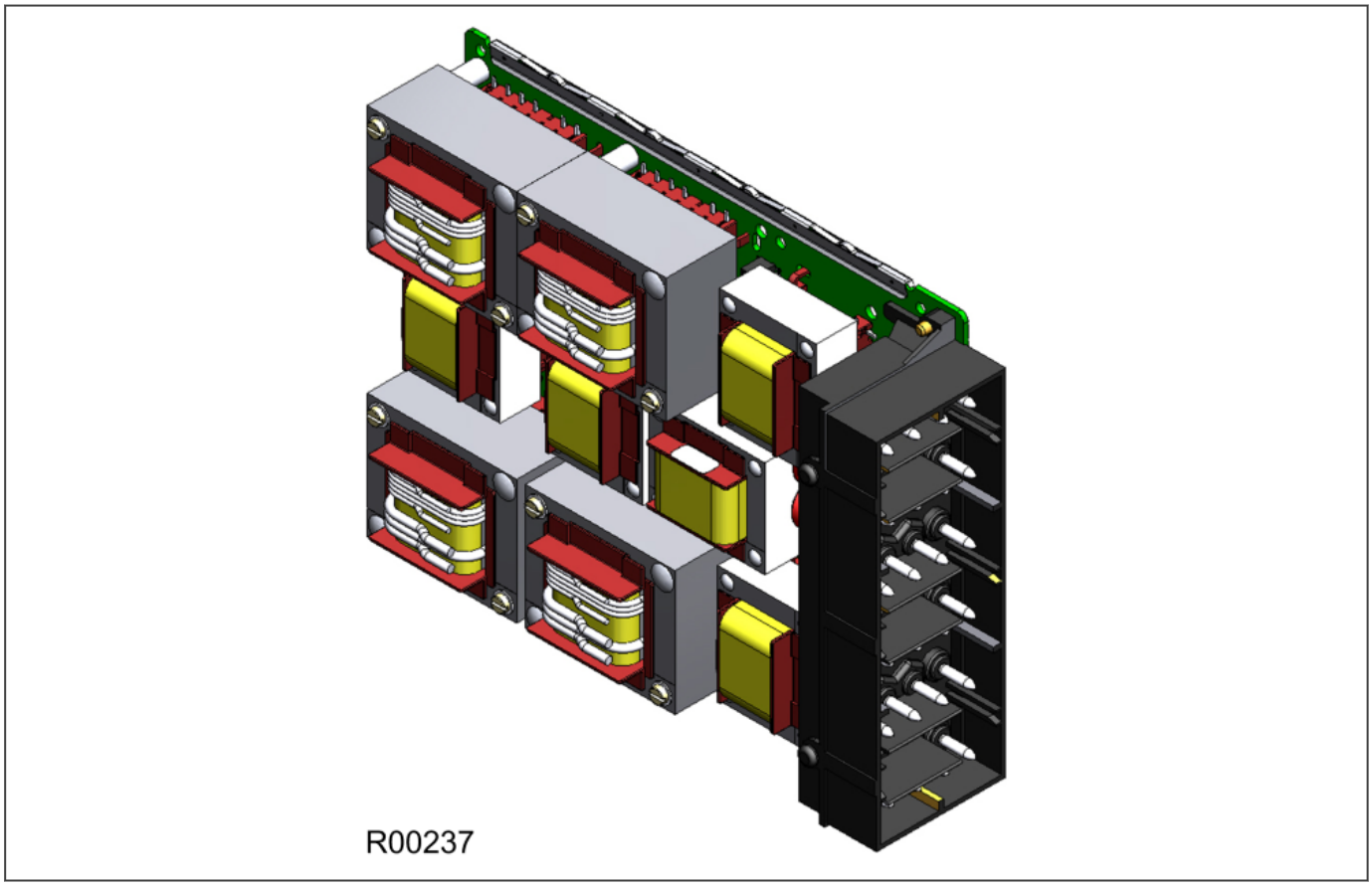


Figure 19: Transformer board

The transformer board hosts the current and voltage transformers. These are used to step down the currents and voltages originating from the power systems' current and voltage transformers to levels that can be used by the devices' electronic circuitry. In addition to this, the on-board CT and VT transformers provide electrical isolation between the unit and the power system.

The transformer board is connected physically and electrically to the input board to form a complete input module.

For terminal connections, please refer to the wiring diagrams.

3.6.5.3 INPUT BOARD

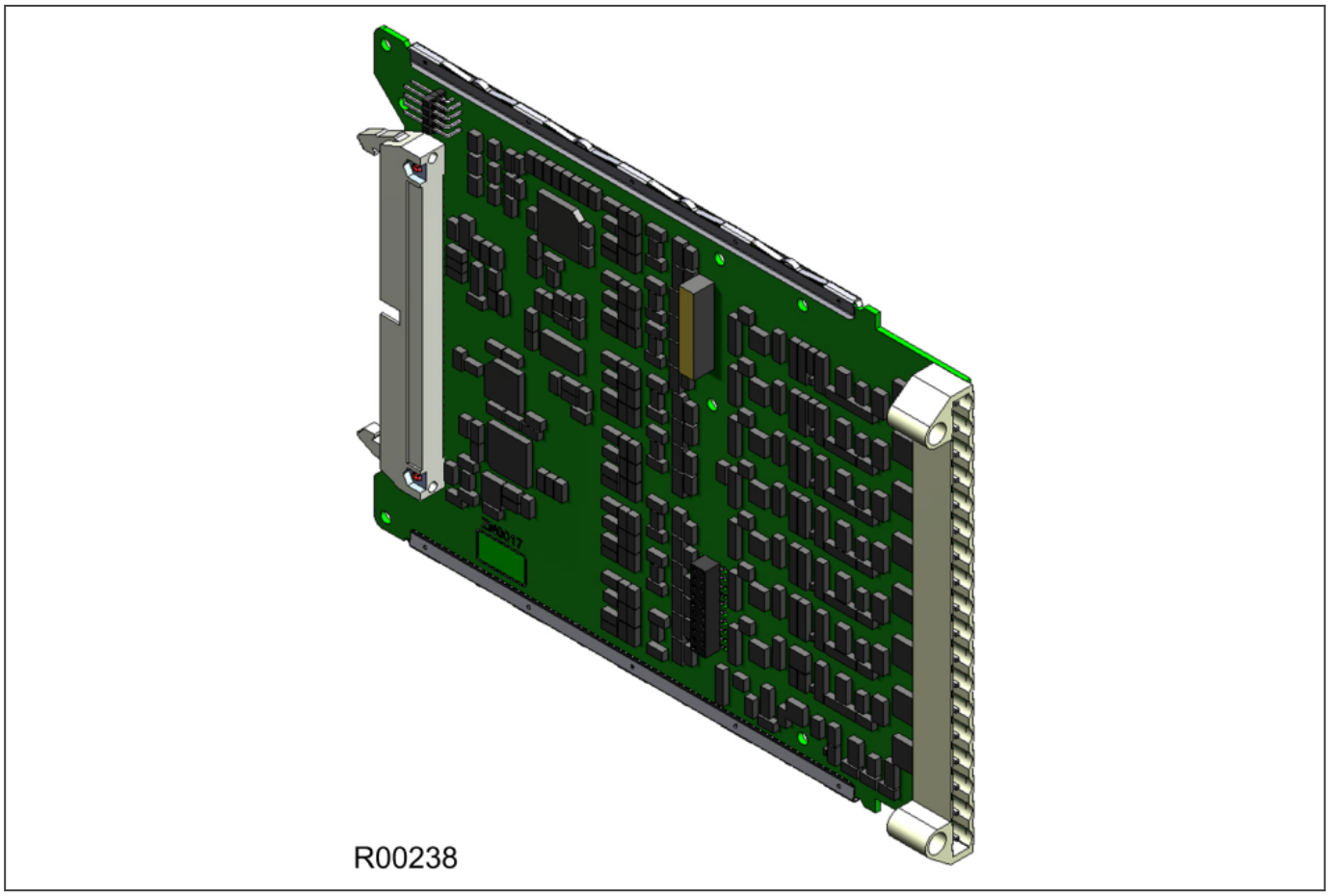


Figure 20: Input board

The input board is used to convert the analogue signals delivered by the current and voltage transformers into digital quantities used by the IED. This input board also has on-board opto-input circuitry, providing eight optically-isolated digital inputs and associated noise filtering and buffering. These opto-inputs are presented to the user by means of an MD terminal block, which sits adjacent to the analogue inputs HD terminal block.

The input board is connected physically and electrically to the transformer board to form a complete input module.

The terminal numbers of the opto-inputs are as follows:

Terminal Number	Opto-input
Terminal 1	Opto 1 -ve
Terminal 2	Opto 1 +ve
Terminal 3	Opto 2 -ve
Terminal 4	Opto 2 +ve
Terminal 5	Opto 3 -ve
Terminal 6	Opto 3 +ve
Terminal 7	Opto 4 -ve
Terminal 8	Opto 4 +ve
Terminal 9	Opto 5 -ve

Terminal Number	Opto-input
Terminal 10	Opto 5 +ve
Terminal 11	Opto 6 -ve
Terminal 12	Opto 6 +ve
Terminal 13	Opto 7 –ve
Terminal 14	Opto 7 +ve
Terminal 15	Opto 8 –ve
Terminal 16	Opto 8 +ve
Terminal 17	Common
Terminal 18	Common

3.6.6 STANDARD OUTPUT RELAY BOARD

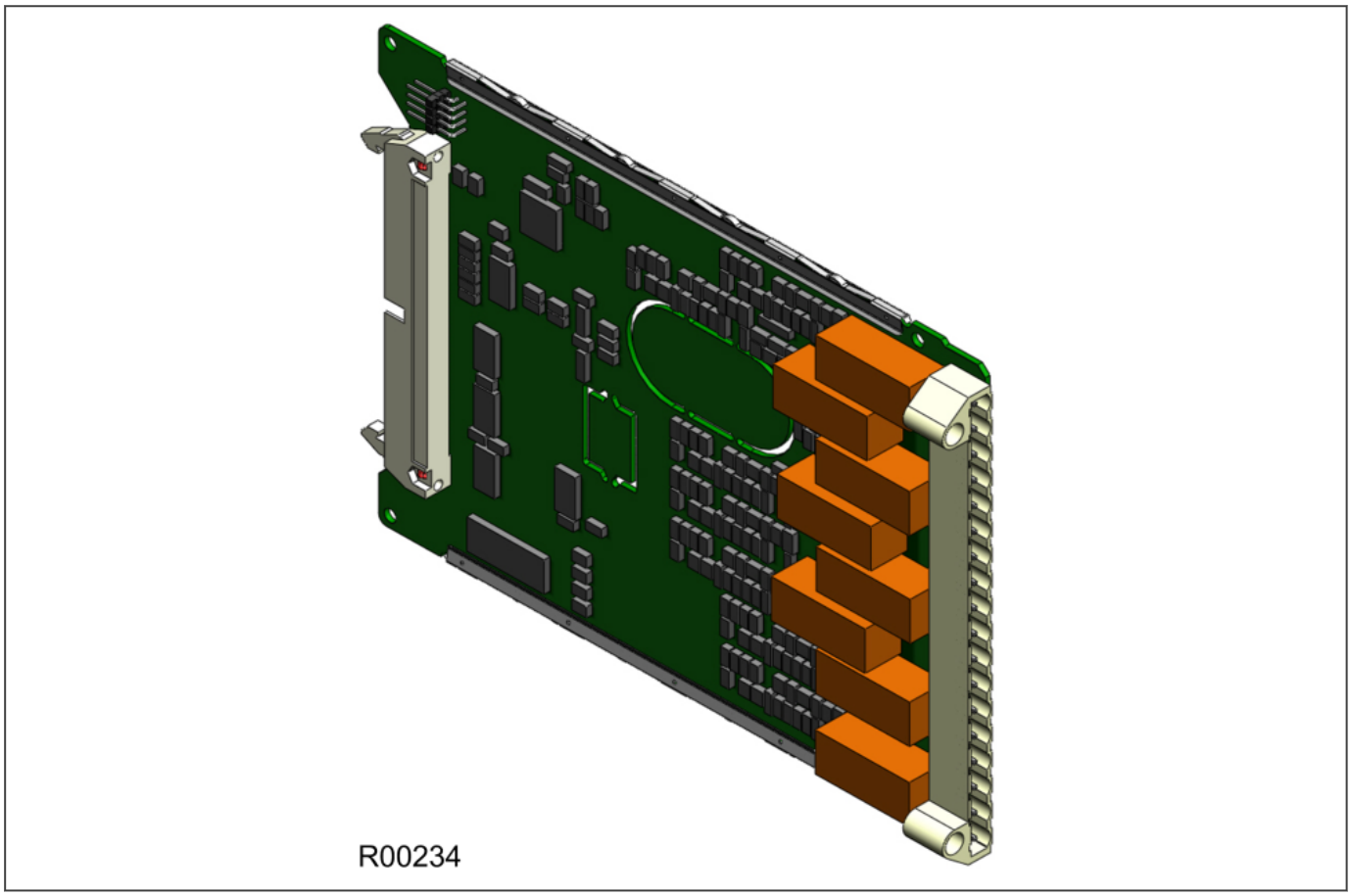


Figure 21: Standard relay output board - 8 contacts

This output relay board has 8 relays with 6 Normally Open contacts and 2 Changeover contacts.

The output relay board is provided together with the power supply board as a complete assembly, or independently for the purposes of relay output expansion.

There are two cut-out locations in the board. These can be removed to allow power supply components to protrude when coupling the output relay board to the power supply board. If the output relay board is to be used independently, these cut-out locations remain intact.

The terminal numbers are as follows:

Terminal Number	Output Relay
Terminal 1	Relay 1 NO
Terminal 2	Relay 1 NO
Terminal 3	Relay 2 NO
Terminal 4	Relay 2 NO
Terminal 5	Relay 3 NO
Terminal 6	Relay 3 NO
Terminal 7	Relay 4 NO
Terminal 8	Relay 4 NO
Terminal 9	Relay 5 NO
Terminal 10	Relay 5 NO
Terminal 11	Relay 6 NO
Terminal 12	Relay 6 NO
Terminal 13	Relay 7 changeover
Terminal 14	Relay 7 changeover
Terminal 15	Relay 7 common
Terminal 16	Relay 8 changeover
Terminal 17	Relay 8 changeover
Terminal 18	Relay 8 common

3.6.7 IRIG-B BOARD

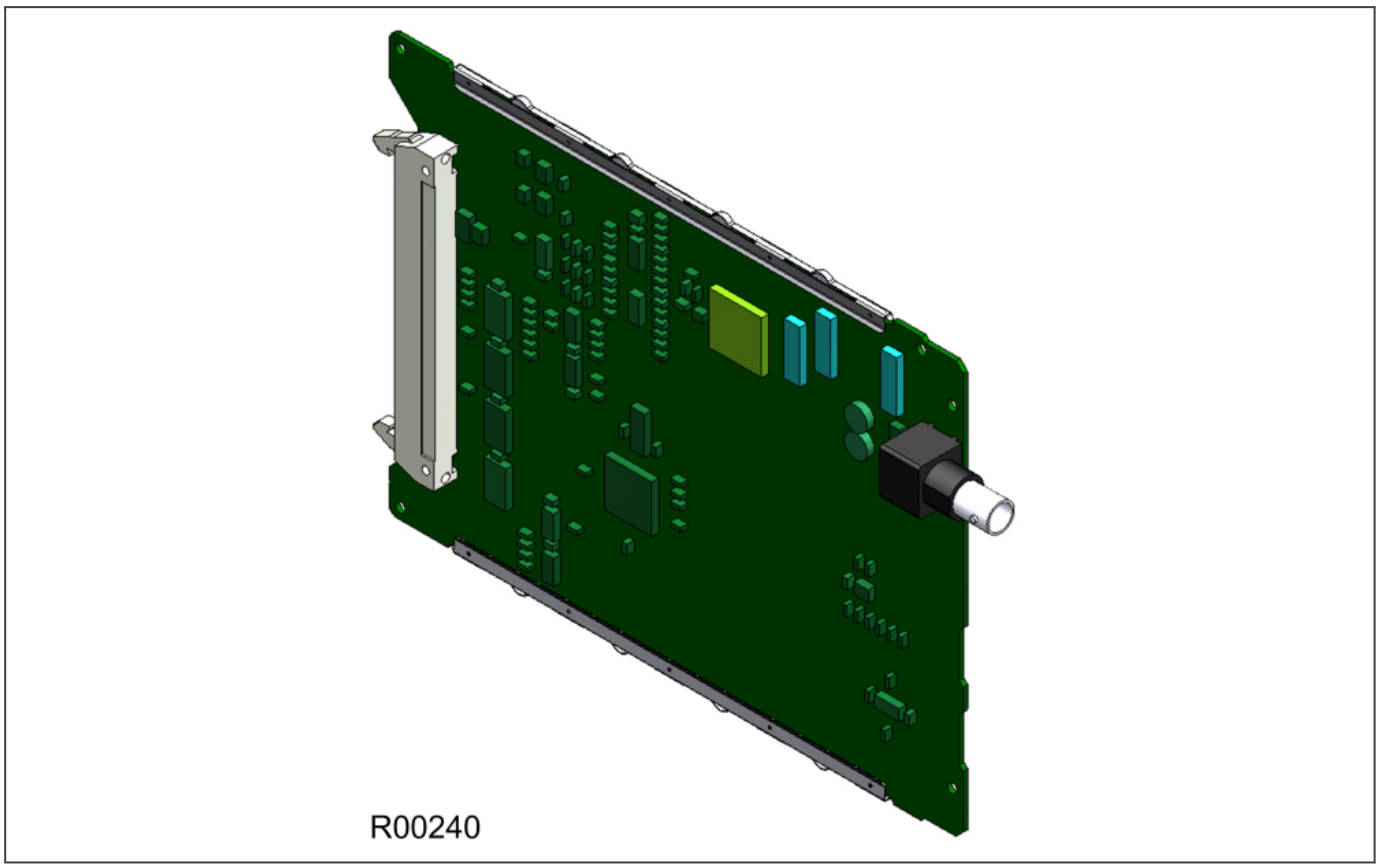


Figure 22: IRIG-B board

The IRIG-B board can be fitted to provide an accurate timing reference for the device. The IRIG-B signal is connected to the board via an BNC connector. The timing information is used to synchronise the IED's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for time tagging events, fault, maintenance and disturbance records.

IRIG-B interface is available in modulated or demodulated formats.

The IRIG-B facility is provided in combination with other functionality on a number of additional boards, such as:

- Fibre board with IRIG-B
- Second rear communications board with IRIG-B
- Ethernet board with IRIG-B
- Redundant Ethernet board with IRIG-B

There are three types of each of these boards; one type which accepts a modulated IRIG-B input, one type which accepts a demodulated IRIG-B input and one type which accepts a universal IRIG-B input. The order code will indicate which variant it supports.

3.6.8 FIBRE OPTIC BOARD

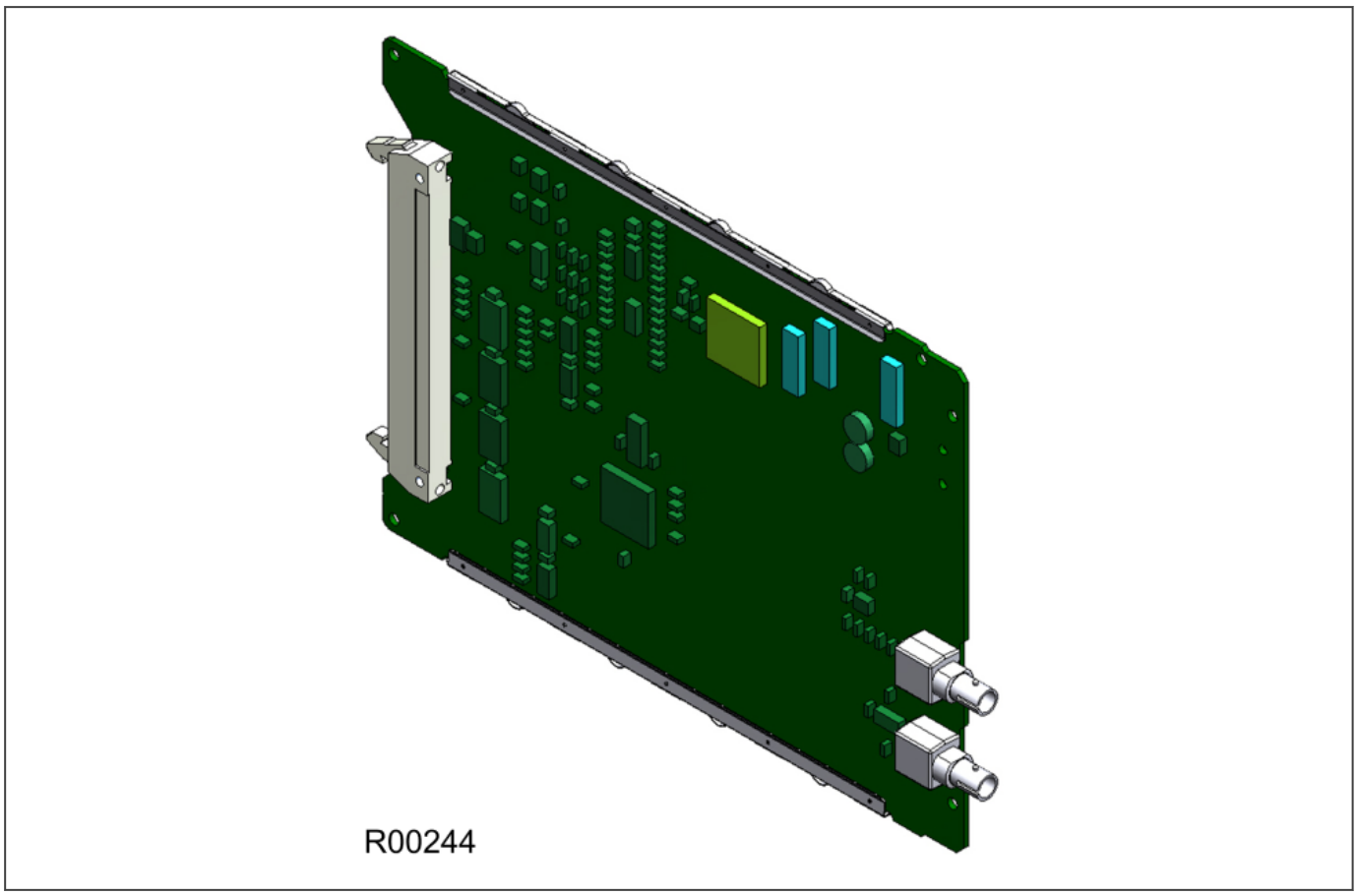


Figure 23: Fibre optic board

This board provides an interface for communicating with a master station. This communication link can use all compatible protocols (Courier, IEC 60870-5-103 and DNP 3.0). It is a fibre-optic alternative to the metallic RS485 port presented on the power supply terminal block. The metallic and fibre optic ports are mutually exclusive.

The fibre optic port uses BFOC 2.5 ST connectors.

The board comes in two varieties; one with an IRIG-B input and one without:

3.6.9 REAR COMMUNICATION BOARD

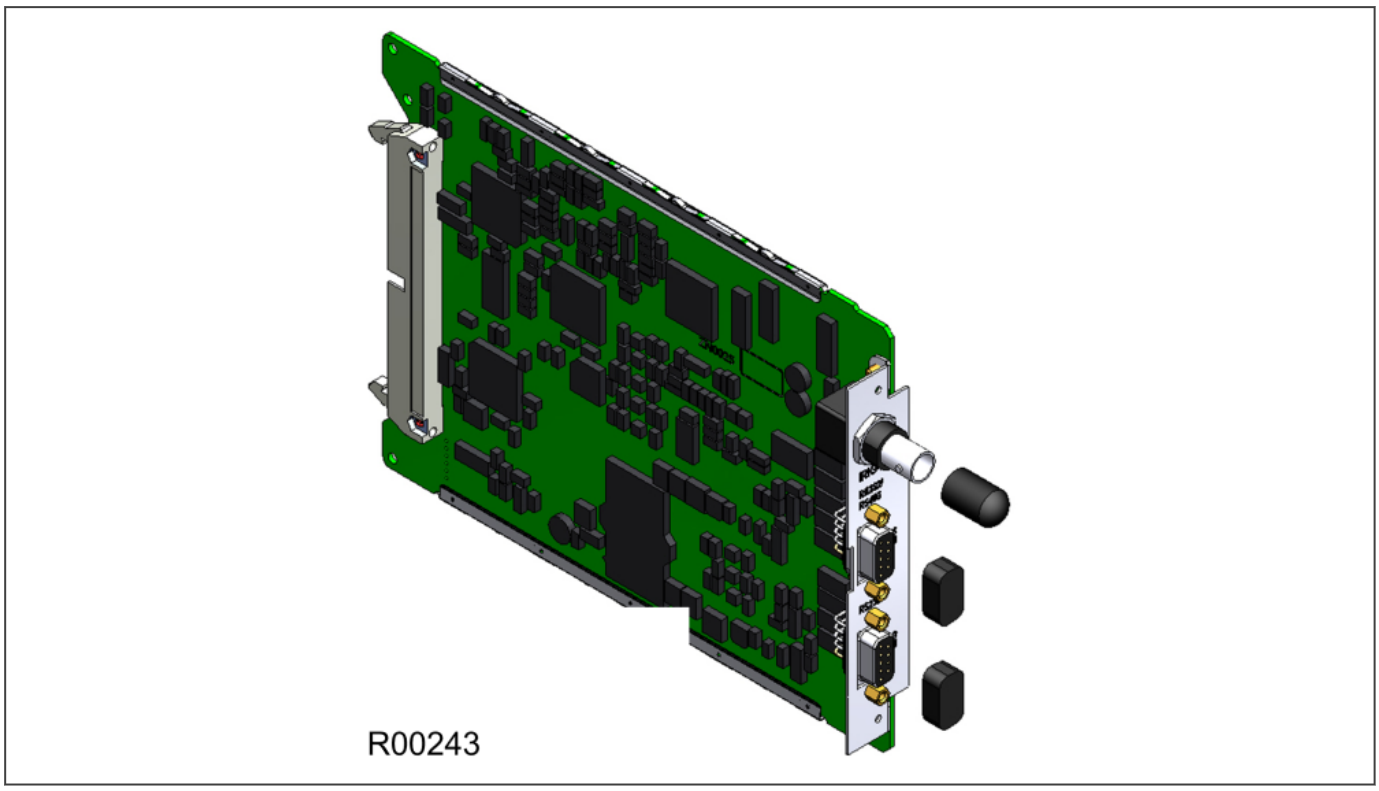


Figure 24: Rear communication board

The optional communications board containing the secondary communication ports provide two serial interfaces presented on 9 pin D-type connectors. These interfaces are known as SK4 and SK5. Both connectors are female connectors, but are configured as DTE ports. This means pin 2 is used to transmit information and pin 3 to receive.

SK4 can be used with RS232, RS485 and K-bus. SK5 can only be used with RS232 and is used for electrical teleprotection. The optional rear communications board and IRIG-B board are mutually exclusive since they use the same hardware slot. However, the board comes in two varieties; one with an IRIG-B input and one without.

3.6.10 REDUNDANT ETHERNET BOARD

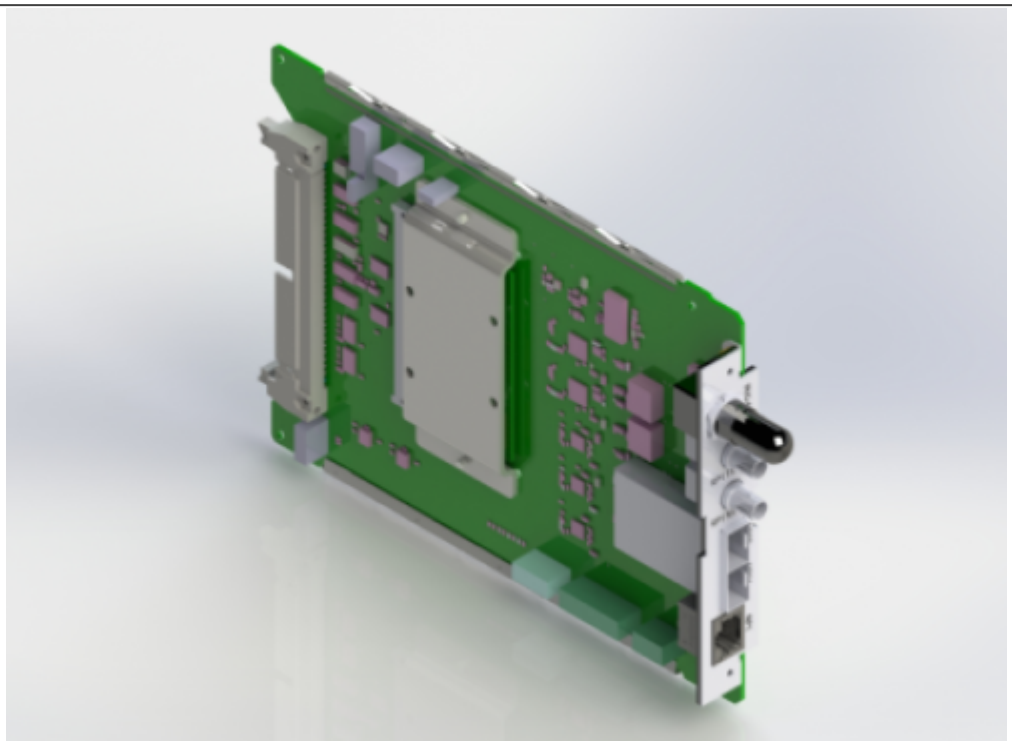




Figure 25: Redundant Ethernet board

This board provides dual redundant Ethernet (NP2A and NP2B) for station bus communications. A universal IRIG-B interface for time synchronisation and a separate Ethernet interface (NP1) for monitoring two variants. A new variant also provides serial protocol support on fiber optics (RP1).

The available redundancy protocols are:

- RSTP (Rapid Spanning Tree Protocol)
- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- Failover

There are several variants for this board as follows:

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with a serial protocol communications ST fibre port with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

Two RJ45 duplex redundant 10/100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

The Ethernet and other connection details are described below:

Universal IRIG-B connector

- Centre connection: Signal
- Outer connection: Earth

LC optical fibre connector (only for NP2A or NP2B when ordering fibre ports on station bus ports)

Connector	SFP
A	TX
B	RX

ST optical fibre connector (only for RP1 serial communications)

Connector	Communications
RP1	TX
RP2	RX

RJ45 Connector (NP1 or NP2A/NP2B when ordering two copper ports on station bus ports only)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used

Pin	Signal Name	Signal Definition
8	-	Not used

3.6.11 SINGLE ETHERNET BOARD

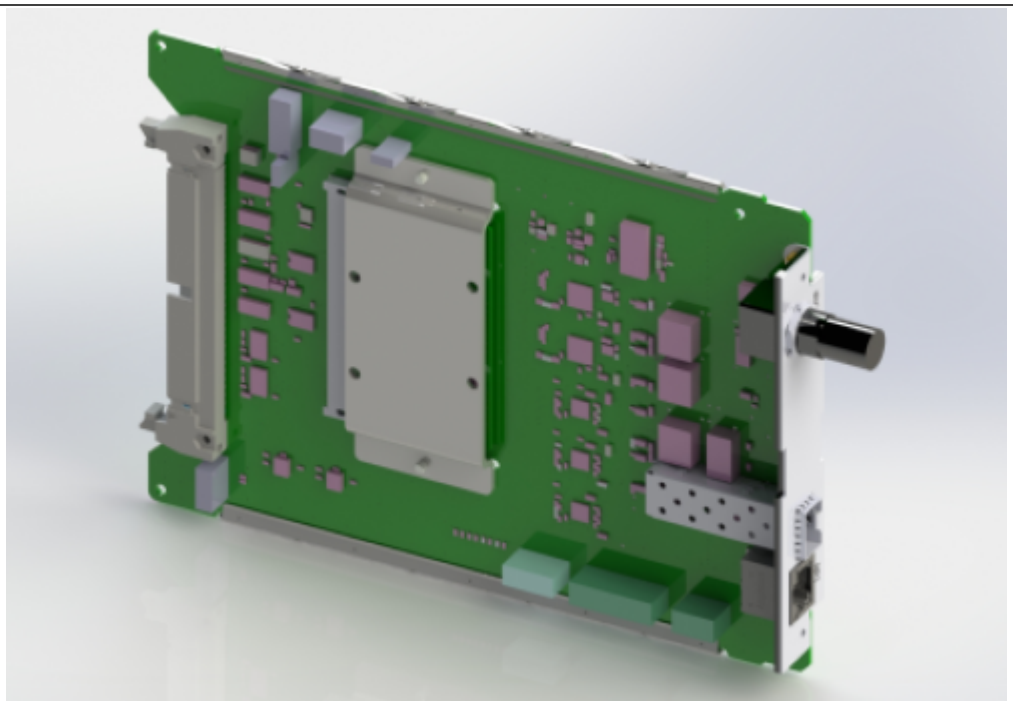




Figure 26: Ethernet board

This board provides one optical 100Mbps LC duplex Ethernet port (NP2A) for station bus communications, with a universal IRIG-B interface for time synchronisation, and a separate 10/100Mbps RJ45 Ethernet maintenance/ engineering interface (NP1) for monitoring and configuration purposes.

The Ethernet and other connection details are described below:

RJ45 connector (NP1 only)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

Universal IRIG-B connector

- Centre connection: Signal
- Outer connection: Earth

LC optical fibre connector (NP2A only)

Connector	SFP
A	TX
B	RX

3.6.12 HIGH BREAK OUTPUT RELAY BOARD

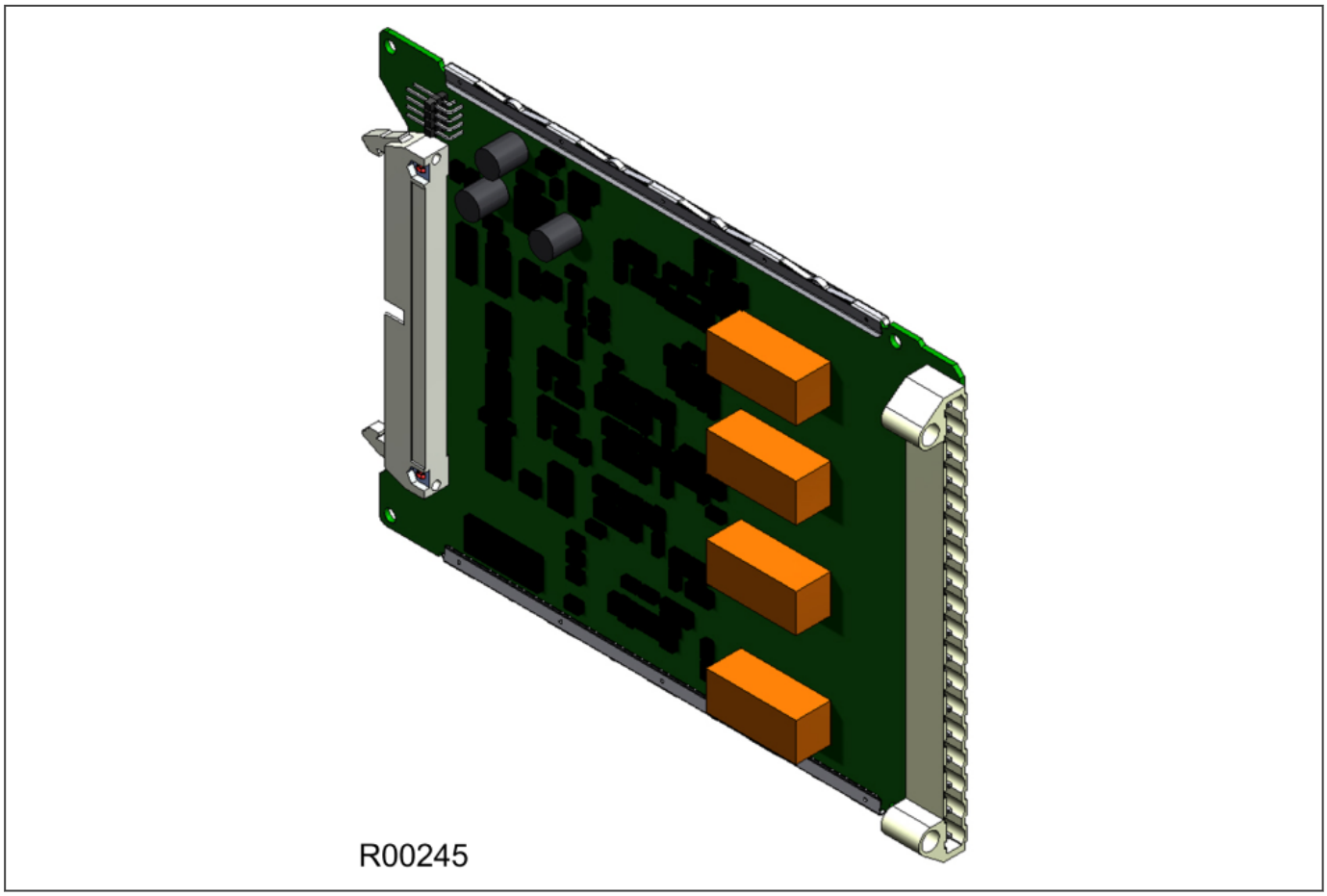


Figure 27: High break relay output board

A High Break output relay board is available as an option. It comprises four normally open output contacts, which are suitable for high breaking loads.

A High Break contact consists of a high capacity relay with a MOSFET in parallel with it. The MOSFET has a varistor placed across it to provide protection, which is required when switching off inductive loads. This is because the stored energy in the inductor causes a high reverse voltage that could damage the MOSFET, if not protected.

When there is a control input command to operate an output contact the miniature relay is operated at the same time as the MOSFET. The miniature relay contact closes in nominally 3.5 ms and is used to carry the continuous load current. The MOSFET operates in less than 0.2 ms, but is switched off after 7.5 ms.

When the control input is reset, the MOSFET is again turned on for 7.5 mS. The miniature relay resets in nominally 3.5 ms before the MOSFET. This means the MOSFET is used to break the load. The MOSFET absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching DC circuits only.

The board number is:

- ZN0042 001

High break contact operation

The following figure shows the timing diagram for High Break contact operation.

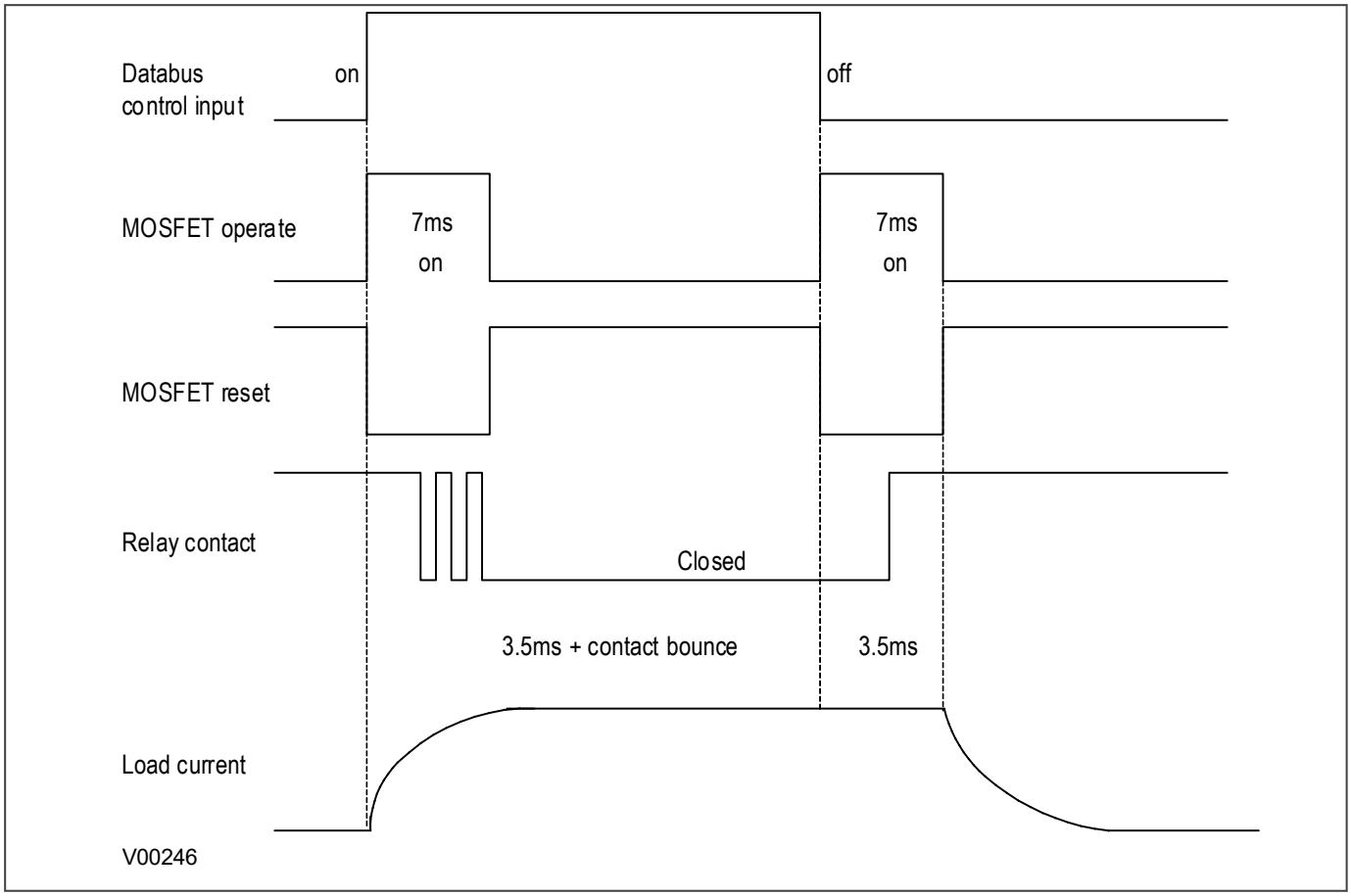


Figure 28: High break contact operation

High break contact applications

- Efficient scheme engineering

  In traditional hard wired scheme designs, High Break capability could only be achieved using external electromechanical trip relays. Instead, these internal High Break contacts can be used thus reducing space requirements.

- Accessibility of CB auxiliary contacts

  It is common practise to use circuit breaker 52a (CB Closed) auxiliary contacts to break the trip coil current on breaker opening, thereby easing the duty on the protection contacts. In some cases (such as operation of disconnectors, or retrofitting), it may be that 52a contacts are either unavailable or unreliable. In such cases, High Break contacts can be used to break the trip coil current in these applications.

- Breaker fail

  In the event of failure of the local circuit breaker (stuck breaker), or defective auxiliary contacts (stuck contacts), it is incorrect to use 52a contact action. The interrupting duty at the local breaker then falls on the relay output contacts, which may not be rated to perform this duty. High Break contacts should be used in this case to avoid the risk of burning out relay contacts.

- Initiation of teleprotection

The High Break contacts also offer fast making, which results in faster tripping. In addition, fast keying of teleprotection is a benefit. Fast keying bypasses the usual contact operation time, such that permissive, blocking and intertrip commands can be routed faster.

Warning:
These relay contacts are POLARITY SENSITIVE. External wiring must comply with the polarity requirements described in the external connection diagram to ensure correct operation.

3.6.13 COPROCESSOR BOARD

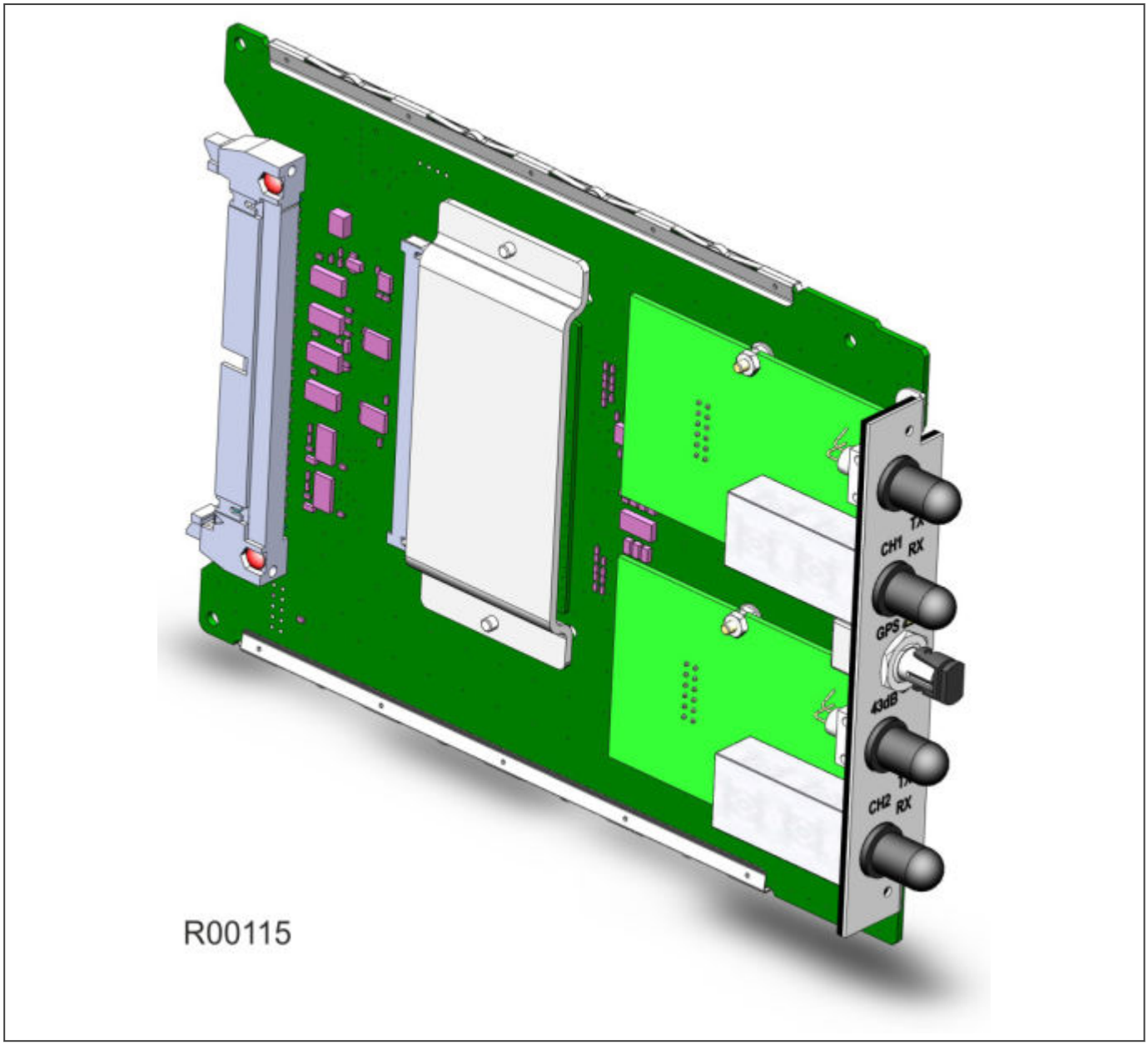


Figure 29: Fully populated coprocessor board

Note:
The above figure shows a coprocessor complete with GPS input and 2 fibre-optic serial data interfaces, and is not necessarily representative of the product and model described in this manual. These interfaces will not be present on boards that do not require them.

Where applicable, a second processor board is used to process the special algorithms associated with the device. This second processor board provides DRAM for use with both program and data memory storage. This memory can be accessed by the main processor board via the parallel bus. The Co-Processor Firmware image is stored locally in Flash Memory and the firmware is then transferred directly from the flash memory to DRAM on the Co-Pro at power up. Further communication between the two processor boards is achieved via interrupts and the shared DRAM. The serial bus carrying the sample data is also connected to the co-processor board, using the processor's built-in serial port, as on the main processor board. There are several different variants of this board, which can be chosen depending on the exact device and model. The variants are:

There are several different variants of this board, which can be chosen depending on the exact device and model. The variants are:

- Coprocessor board with current differential inputs and GPS input
- Coprocessor board with current differential inputs only
- Coprocessor board with GPS input only

3.6.13.1 CURRENT DIFFERENTIAL INPUTS

Where applicable, the coprocessor board can be equipped with up to two daughter boards, each containing a fibre-optic interface for a serial data link. BFOC 2.5 ST connectors are used for this purpose. One or two channels are provided, each channel comprising a fibre pair for transmitting and receiving (Rx Tx). These channels are labelled Ch1 and Ch2. These serial data links are used to transfer information between two or three IEDs for current differential applications.

3.6.13.2 COPROCESSOR BOARD WITH 1PPS INPUT

In some applications, where the communication links between two remote devices are provided by a third party telecommunications partner, the transmit and receive paths associated with one channel may differ considerably in length, resulting in very different transmission and receive times.

If, for example, Device A is transmitting to Device B information about the value of its measured current, the information Device A is receiving from Device B about the current measured at the same time, may reach device B at a different time. This has to be compensated for. A 1pps GPS timing signal applied to both devices will help the IEDs achieve this, because it is possible to measure the exact time taken for both transmission and receive paths.

Note:
The 1 pps signal is always supplied by a GPS receiver (such as a RT430).

Note:
This signal is used to control the sampling process, and timing calculations and is not used for time stamping or real time synchronisation.

CHAPTER 4

SOFTWARE DESIGN

4.1 CHAPTER OVERVIEW

This chapter describes the software design of the IED.

This chapter contains the following sections:

Chapter Overview 63
Software Design Overview 64
System Level Software 65
Platform Software 68
Protection and Control Functions 69

4.2 SOFTWARE DESIGN OVERVIEW

The device software can be conceptually categorised into several elements as follows:

- The system level software
- The platform software
- The protection and control software

These elements are not distinguishable to the user, and the distinction is made purely for the purposes of explanation. The following figure shows the software architecture.

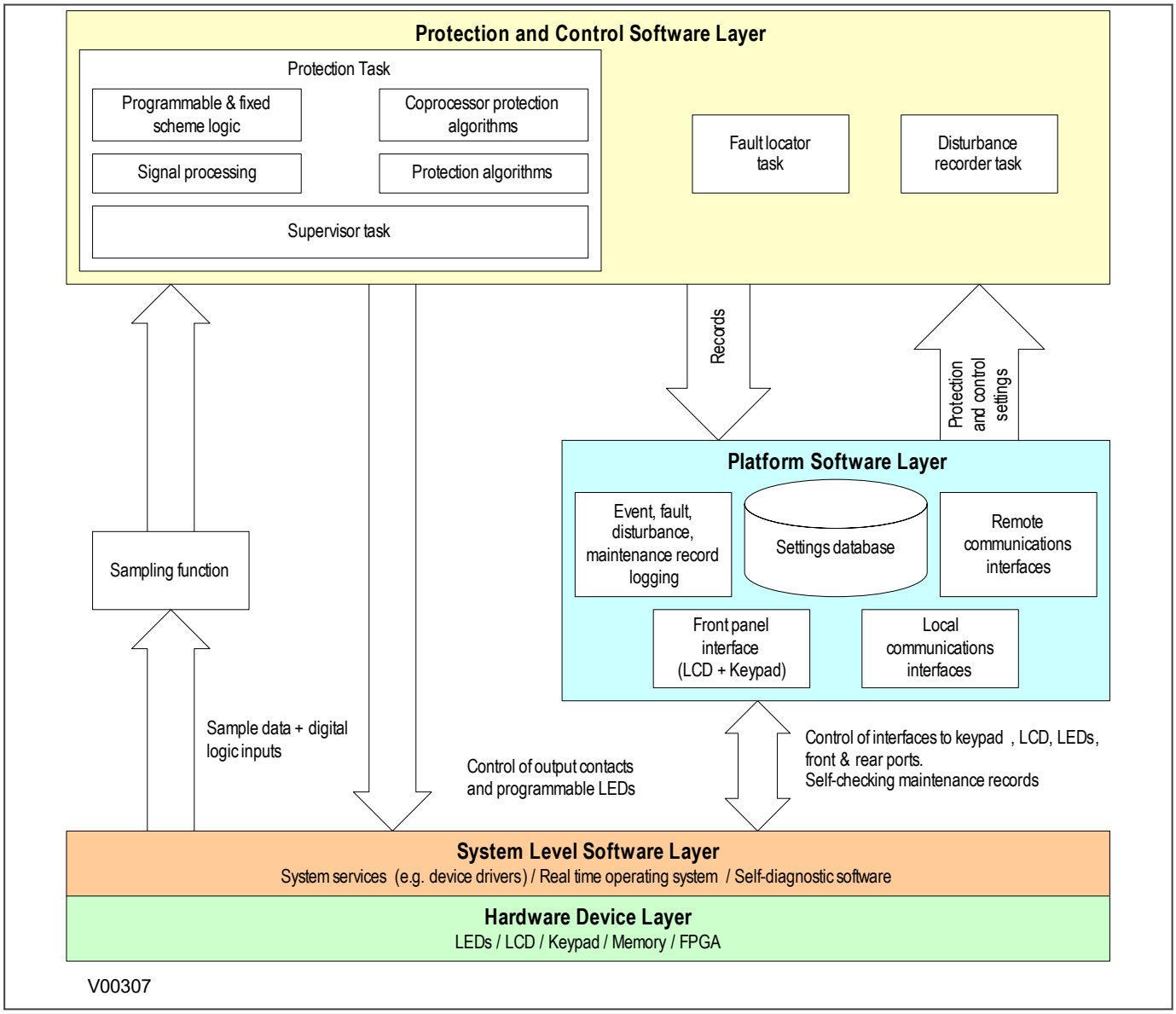


Figure 30: Software architecture

The software, which executes on the main processor, can be divided into a number of functions as illustrated above. Each function is further broken down into a number of separate tasks. These tasks are then run according to a scheduler. They are run at either a fixed rate or they are event driven. The tasks communicate with each other as and when required.

4.3 SYSTEM LEVEL SOFTWARE

4.3.1 REAL TIME OPERATING SYSTEM

The real-time operating system is used to schedule the processing of the various tasks. This ensures that they are processed in the time available and in the desired order of priority. The operating system also plays a part in controlling the communication between the software tasks, through the use of operating system messages.

4.3.2 SYSTEM SERVICES SOFTWARE

The system services software provides the layer between the hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls things like the booting of the processor and the downloading of the processor code into DRAM at startup.

4.3.3 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the ‘Healthy’ LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the ‘Healthy’ LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

4.3.4 STARTUP SELF-TESTING

The self-testing takes a few seconds to complete, during which time the IEDs measurement, recording, control, and protection functions are unavailable. On a successful start-up and self-test, the ‘Healthy' state LED on the front of the device is switched on. If a problem is detected during the start-up testing, the device remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

1. System boot
2. System software initialisation
3. Platform software initialisation and monitoring

4.3.4.1 SYSTEM BOOT

The integrity of the Flash memory is verified using a checksum before the program code and stored data is loaded into DRAM for execution by the processor. When the loading has been completed, the data held in DRAM is compared to that held in the Flash memory to ensure that no errors have occurred in the data transfer and that the two are the same. The entry point of the software code in DRAM is then called. This is the IED's initialisation code.

4.3.4.2 SYSTEM LEVEL SOFTWARE INITIALISATION

The initialisation process initialises the processor registers and interrupts, starts the watchdog timers (used by the hardware to determine whether the software is still running), starts the real-time operating system and creates and starts the supervisor task. In the initialisation process the device checks the following:

- The status of the supercapacitor to maintain the real time clock
- The operation of the LCD controller
- The watchdog operation

At the conclusion of the initialisation software the supervisor task begins the process of starting the platform software.

4.3.4.3 CO-PROCESSOR INITIALISATION

This product features a co-processor board which hosts principal protection functions and supports associated time-critical teleprotection functionality.

The co-processor is responsible for receiving sampled values of analogue inputs and performing any specific signal filtering and processing required by the hosted protection algorithms. Communications are managed using the HDLC (high-level data link control) communication protocol and enable transfer of information needed between IEDs to implement unit protection schemes.

The co-processor interface initialises and maintains appropriate time synchronisation, as well as data and command transfer with the main processor for correct protection operation.

Co-processor board initialisation checks are also made as follows:

- A check is made for the presence of the co-processor board
- The DRAM on the co-processor board is checked

If any of these checks produces an error, the co-processor board is left out of service. The other protection functions provided by the main processor board are left in service.

4.3.4.4 PLATFORM SOFTWARE INITIALISATION AND MONITORING

When starting the platform software, the IED checks the following:

- The integrity of the data held in non-volatile memory (using a checksum)
- The operation of the real-time clock
- The optional IRIG-B function (if applicable)
- The presence and condition of the input board
- The analog data acquisition system (it does this by sampling the reference voltage)

At the successful conclusion of all of these tests the unit is entered into service and the application software is started up.

4.3.5 CONTINUOUS SELF-TESTING

When the IED is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software and the results are reported to the platform software. The functions that are checked are as follows:

- The Flash memory containing all program code and language text is verified by a checksum.
- The code and constant data held in system memory is checked against the corresponding data in Flash memory to check for data corruption.
- The system memory containing all data other than the code and constant data is verified with a checksum.

- The integrity of the digital signal I/O data from the opto-inputs and the output relay coils is checked by the data acquisition function every time it is executed.
- The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed. This is done by sampling the reference voltages.
- The operation of the optional Ethernet board is checked by the software on the main processor board. If the Ethernet board fails to respond an alarm is raised and the board is reset in an attempt to resolve the problem.
- The operation of the optional IRIG-B function is checked by the software that reads the time and date from the board.

In the event that one of the checks detects an error in any of the subsystems, the platform software is notified and it attempts to log a maintenance record.

If the problem is with the IRIG-B board, the device continues in operation. For problems detected in any other area, the device initiates a shutdown and re-boot, resulting in a period of up to 10 seconds when the functionality is unavailable.

A restart should clear most problems that may occur. If, however, the diagnostic self-check detects the same problem that caused the IED to restart, it is clear that the restart has not cleared the problem, and the device takes itself permanently out of service. This is indicated by the ‘’health-state’ LED on the front of the device, which switches OFF, and the watchdog contact which switches ON.

4.4 PLATFORM SOFTWARE

The platform software has three main functions:

- To control the logging of records generated by the protection software, including alarms, events, faults, and maintenance records
- To store and maintain a database of all of the settings in non-volatile memory
- To provide the internal interface between the settings database and the user interfaces, using the front panel interface and the front and rear communication ports

4.4.1 RECORD LOGGING

The logging function is used to store all alarms, events, faults and maintenance records. The records are stored in non-volatile memory to provide a log of what has happened. The IED maintains four types of log on a first in first out basis (FIFO). These are:

- Alarms
- Event records
- Fault records
- Maintenance records

The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software. The platform software is responsible for logging a maintenance record in the event of an IED failure. This includes errors that have been detected by the platform software itself or errors that are detected by either the system services or the protection software function. See the Monitoring and Control chapter for further details on record logging.

4.4.2 SETTINGS DATABASE

The settings database contains all the settings and data, which are stored in non-volatile memory. The platform software manages the settings database and ensures that only one user interface can modify the settings at any one time. This is a necessary restriction to avoid conflict between different parts of the software during a setting change. Changes to protection settings and disturbance recorder settings, are first written to a temporary location DRAM memory. This is sometimes called 'Scratchpad' memory. These settings are not written into non-volatile memory immediately. This is because a batch of such changes should not be activated one by one, but as part of a complete scheme. Once the complete scheme has been stored in DRAM, the batch of settings can be committed to the non-volatile memory where they will become active.

4.4.3 INTERFACES

The settings and measurements database must be accessible from all of the interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each of the interfaces (LCD display, keypad and all the communications interfaces).

4.5 PROTECTION AND CONTROL FUNCTIONS

The protection and control software processes all of the protection elements and measurement functions. To achieve this it has to communicate with the system services software, the platform software as well as organise its own operations.

The protection task software has the highest priority of any of the software tasks in the main processor board. This ensures the fastest possible protection response.

The protection and control software provides a supervisory task, which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

4.5.1 ACQUSITION OF POWER SYSTEM INPUT SIGNALS

A sampling function controls the acquisition of sampled input data to the various protection and control and recording functions in this device.

Following successful initialisation from the system services software, the sampling function delivers a constant stream of input data to the Protection and Control software at a rate of 48 samples per cycle of the power system frequency. This means that on a 50Hz power system the nominal sampling rate is 2,400 Hz whereas, for a 60 Hz system, sampling will be at 2,880 Hz.

The sampled input data is consumed at different rates by the various protection, control, and recording functions according to specific application requirements and, typically, Fourier filters and/or disturbance recorders may be populated at sub-multiples of the device sampling rate (for example, 24 or 8 samples per cycle).

The following section, explains that the sampling rate is synchronised to the power system frequency by a frequency tracking algorithm. This ensures that for minor excursions in the system frequency, an exact number of samples are always acquired for every cycle, ensuring protection stability. In normal operation, the outputs from the protection elements are updated 16 times per cycle.

4.5.2 FREQUENCY TRACKING OF INPUT SIGNAL ACQUISITION

This device features a frequency tracking algorithm so that, even for small changes, its power system inputs are sampled exactly 48 times every power system cycle over the full rated frequency range. If the system frequency moves out of range, the sampling rate defaults according to the applied system frequency setting, at either 2,400 Hz for 50 Hz or 2,880 Hz for 60 Hz.

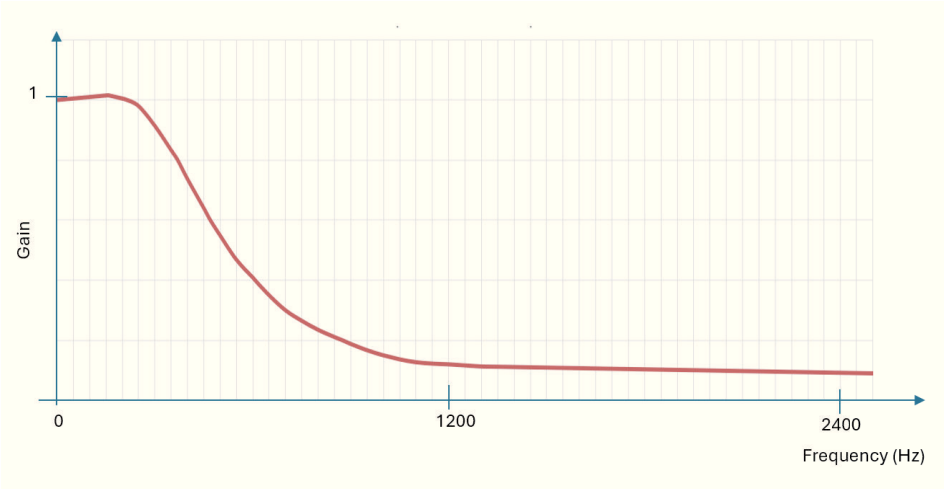
A recursive Fourier filter applied to the device’s analog inputs detects phase variations. From these changes, the precise system frequency can be determined. This is used to implement frequency tracking of the input signals acquisition, as well as to inform the protection and control and recording tasks about the measured system frequency. The frequency tracking controls the acquisition by adjusting the intervals between sampling instants to ensure that the number of samples acquired per cycle exactly matches the expected constant value. To execute, the frequency tracking requires that just one of the phase input voltage or phase input current signals is available. Availability thresholds are set as 10% Vn for voltage, and 5% In for current, and the frequency tracks off any available voltage or current input signal, prioritised in the order VA, VB, VC, IA, IB, IC.

4.5.3 INPUT SIGNAL FILTERING

Most of the protection algorithms in this product apply digital filtering to the sampled data input streams to extract useful information from power system analogue signals (phase current angles, for example). Fourier filters may be employed to provide useful information about specific frequency components, whereas other bespoke filters may facilitate the calculation of quantities such as fault impedances and distance-to-fault values.

Some of the functionality provided by this product, however, is better implemented using raw data that has not been subject to digital filtering. Un-processed raw data may be required by special (potentially very fast acting) protection functions or, more typically waveform recording and the calculation of true RMS values of current, voltage and

power for metering purposes. In these cases, the fidelity is defined by the anti-aliasing filters applied to the input signals for which the characteristics are defined by the following figure.



E80069

Figure 31: Anti-alias filter response

4.5.4 FOURIER SIGNAL FILTERING

Most protection and measurement functions in this device use single-cycle Fourier digital filtering to extract power frequency components.

The software to implement the Fourier filters acts on the sampled analogue input signals and is, along with the associated protection and control software, hosted on the main processor board.

The principal use of Fourier filters in this product is to provide measurements of fundamental components for current based protection, but Fourier filters may also be applied to extract fundamental signals for other protection functions such as voltage, as well as deriving harmonic components such as the second harmonic used to restrain current differential protection.

The magnitude and angle of fundamental frequency components of input signals are calculated using one complete cycle of the most recently acquired input data. In this case, the Fourier algorithm extracts the power frequency fundamental component from the input signal, presenting it in terms of magnitude and phase angle. This can be represented in either polar format or rectangular format, as required. Values for harmonic components can be similarly determined by appropriately varying the filters' input data streams and filter coefficients.

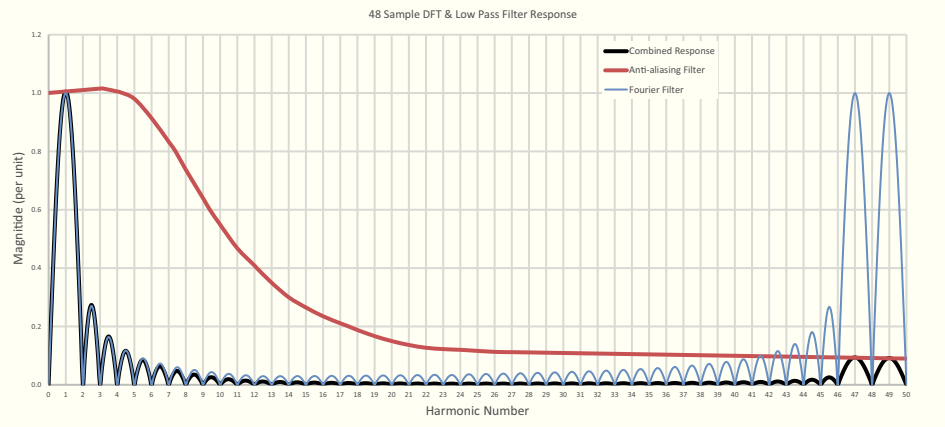
The Fourier filter acts as a function with zero gain at DC, unity gain at the fundamental, and with good harmonic rejection for all harmonic frequencies up to a value known as the Nyquist frequency (and equivalent to half the sampling frequency). Any frequency component of the input signal above this Nyquist frequency appears as an unwanted alias component causing problems. The introduction of low-pass filters to limit the input frequency spectrum to less than half that of the sampling frequency effectively prevents aliasing.

4.5.4.1 COMBINED FOURIER FILTER RESPONSE

In this product, the rate at which sampled data is made available to the protection and control software is 48 per cycle and so the required minimum cut-off frequency for the anti-aliasing filters is:

- 1200 Hz (for a 50 Hz system), or
- 1440 Hz for a 60 Hz system.

The following figure shows the frequency response of the combined anti-alias filter and 48-sample single-cycle Fourier filter implemented in this product.

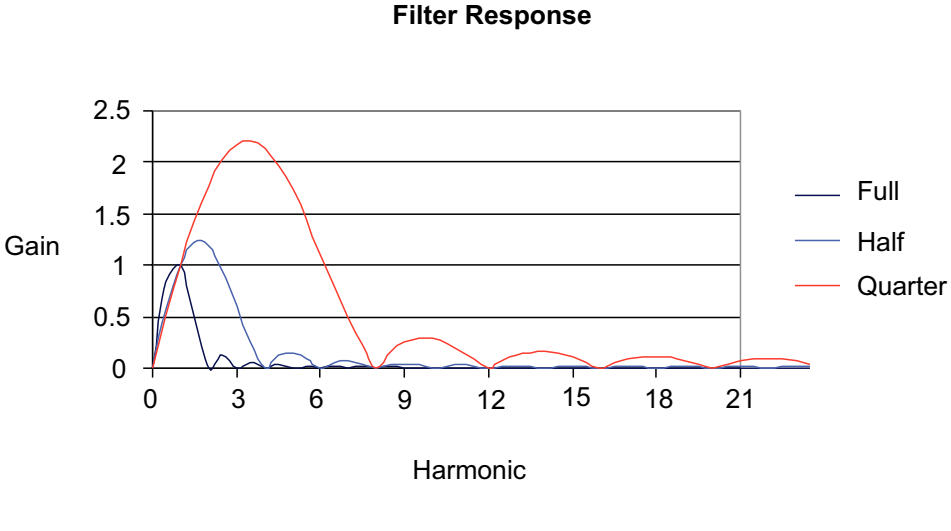


E80021

Figure 32: Combined input filter response

4.5.5 DISTANCE PROTECTION SIGNAL FILTERING

To implement distance protection in this product, the current and voltage inputs are filtered using Finite Impulse Response (FIR) digital filters. This reduces the effects of non-power frequency components in the input signals, such as DC offsets in current waveforms, and capacitor voltage transformer (CVT) transients in the voltages. The device uses a combination of a 1/4 cycle filter using 12 coefficients, a 1/2 cycle filter using 24 coefficients, and a single cycle filter using 48 coefficients. The device automatically performs intelligent switching in the application of the filters, to select the best balance of removal of transients with fast response. The protection elements themselves then perform additional filtering, implemented for example, by the trip count strategy. The following figure shows the frequency response of the 12, 24 and 48 coefficient filters, noting that all have a gain of unity at the fundamental frequency:



E00308

Figure 33: Distance protection input filter response

4.5.6 FAULT LOCATOR

The fault locator uses 12 cycles of the analog input signals to calculate the fault location. The result is returned to the protection and control task, which includes it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record. When the fault record is complete, including the fault location, the protection and control task sends a message to the supervisor task to log the fault record.

The Fault Locator is not available on all models.

4.5.7 EVENT RECORDER INTERFACE

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer controlled by the supervisor task. A background task in the platform software then converts the data into a stored non-volatile record.

Maintenance records are a special category of event record which may be created during power-up or self-testing. Similar to other events, the supervisor task instructs the platform software to log a record when it receives a maintenance record message, but the maintenance records are stored in a separate register to simplify examination.

4.5.8 SCHEME LOGIC INTERFACE

Association of the protection and control algorithms implemented in this device with external plant relies on logical allocation of software inputs and outputs with physical inputs and outputs. The functionality which implements this is known as scheme logic. The scheme logic in this device consists of fixed components and programmable components. Fixed scheme logic components are hard-coded into the protection and control algorithm software modules. They have been designed to complement the protection and control objectives and cannot be changed by the user. User control over the operation of the devices' digital inputs and output is provided by a feature know as the programmable scheme logic (PSL). Executed in response to changes of state of inputs either from external plant, or from functional inputs from the user interfaces, or from internal logic state changes emanating from execution of the protection and control software, the scheme logic allows the user to combine factory-proven application scheme logic with versatile user-designed logic processing to control outputs and led indications.

4.5.9 PROGRAMMABLE SCHEME LOGIC

The purpose of the programmable scheme logic (PSL) is to allow you to configure your own protection schemes to suit your particular application. This is done with programmable logic gates and delay timers. To allow greater flexibility, different PSL is allowed for each of the four setting groups.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic (FSL). The fixed scheme logic provides the standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the device and the output contacts at the rear.

The execution of the PSL logic is event driven. The logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

The PSL can be configured to create very complex schemes. Because of this PSL design is achieved by means of a PC support package called the PSL Editor. This is available as part of the settings application software MiCOM S1 Agile.

4.5.10 FUNCTION KEY INTERFACE

The function keys interface directly into the PSL as digital input signals. A change of state is only recognised when a key press is executed on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on

key press only (normal mode) depending on how it is programmed. It can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during device power up thus allowing the function key state to be reinstated after power-up, should power be inadvertently lost.

CHAPTER 5

CONFIGURATION

5.1 CHAPTER OVERVIEW

Each product has different configuration parameters according to the functions it has been designed to perform. There is, however, a common methodology used across the entire product series to set these parameters.

Some of the communications setup cannot be carried out using the settings applications software, it can only be carried out using the HMI. This chapter includes concise instructions on how to configure the device, as well as a description of the common methodology used to configure the device in general.

This chapter contains the following sections:

Chapter Overview 75

Settings Application Software 76

Using the HMI Panel 77

5.2 SETTINGS APPLICATION SOFTWARE

To configure this device, you will need to use the Settings Application Software. The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for setting up and managing the IEDs.

Although you can change many settings using the front panel HMI, some of the features cannot be configured without the Settings Application Software. For example, the programmable scheme logic, or the IEC 61850 communications or the SLD.

If you do not already have a copy of the Settings Application Software, you can obtain it from GE Vernova contact centre.

To configure your product, you will need a data model that matches your product. When you launch the Settings Application Software, you will be presented with a panel that allows you to invoke the “Data Model Manager”. This will close the other aspects of the software to allow an efficient import of the chosen data model. If you don’t have, or can’t find, the data model relating to your product, please call the GE Vernova contact centre.

When you have loaded all the data models you need, you should restart the Settings Application Software and start to create a model of your system using the “System Explorer” panel.

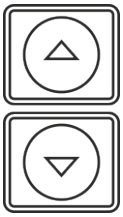
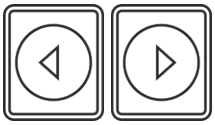
The software is designed to be intuitive, but help is available in an online help system and in the Settings Application Software user guide P40-M&CR-SAS-UG-EN-n, where 'Language' is a 2-letter code designating the language version of the user guide and 'n' is the latest version of the settings application software.

5.3 USING THE HMI PANEL

Using the Graphical HMI, you can:

- Display and modify settings
- Display measurements
- Display fault records
- Display the Single Line Diagram (SLD)
- View the digital I/O signal status
- Reset fault and alarm indications

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the screen.

Keys	Description	Function
	Up and down cursor keys	To change between settings in a particular column, changing values within a cell or to select the next item on the SLD
	Left and right cursor keys	To change between settings in a particular column, change values within a cell or to select the next item on the SLD
	ENTER/OK key	For changing and executing settings. When a bottom banner Menu context key label is selected, the OK key can also be used to navigate between pages.
	Menu context keys	Menu context keys situated directly below the graphical HMI are used to navigate between pages.
	Cancel/Reset key	To return to the menu header from any menu cell, or to cancel a setting input.
	Read/Home key	To navigate to the default Home page from anywhere in the menu.
	Function keys (not all models)	For executing user programmable functions

Keys	Description	Function
	Control key OPEN	Control key OPEN used to open the CB/Switch. **Note:** Colour coding is selectable via labels and configuration of PSL/SLD.
	Control key CLOSE	Control key CLOSE used to close the CB/Switch. **Note:** Colour coding is selectable via labels and configuration of PSL/SLD.
	Local/Remote key	To select between local and remote operating modes.

5.3.1 NAVIGATING THE HMI PANEL

The cursor keys are used to navigate the menu. To navigate between different menus, use the Menu context keys, which are located below the graphical display.

The cursor keys have an auto-repeat function if held down continuously. This can be used to speed up both setting value changes and menu navigation. The longer the key is held down, the faster the rate of change or movement.

5.3.2 GETTING STARTED

When you first start the IED, it will go through its power up procedure. After a few seconds it will settle down into the default display. If there are alarms present, the yellow Alarms LED will be flashing and the alarm counter on the top banner will show the number of alarms that are active.

The device should be in full working order when you first start it, but an alarm could still be present. For example, if there is no network connection for a device fitted with a network board. If this is the case, you can read the alarm by selecting the Alarm counter on the top banner of the display.

For the example given, if the device is fitted with an Ethernet board, you will need to connect the device to an active Ethernet network to be able to clear the alarm.

5.3.3 DEFAULT DISPLAY

The graphical HMI default display contains shortcuts to various sections of the menu, as well as a snapshot of the current device status.

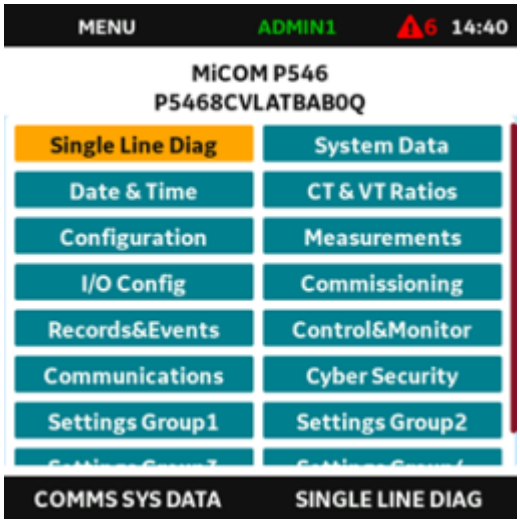


Figure 34: HMI default display

The graphical display screen consists of three main areas, which can be selected using the navigation keypad.

1. The top banner displays information left to right and includes the menu label for the current display, the user access level, the number of active alarms and the time.
2. The content area displays information related to the chosen area of navigation. For example, settings, measurements or SLD.
3. The bottom banner displays labels for the two Menu context keys, which are used for navigating between the menus.

Note:
After a period defined by the "LCD screen saver" , setting the HMI will enter rest mode. This allows the HMI to reduce power consumption and will dim the LCD backlight. The HMI may be woken from rest mode by pressing any front panel key. This mode has no effect on IED functional performance.

5.3.4 DEFAULT DISPLAY NAVIGATION

The default display provides quick and simple navigation of the complete menu database. Use the navigation keypad to change the highlighted cell. The highlighted entry can be selected using the Enter/OK Key. When the bottom of the screen is reached, the selected area moves to the Bottom Banner. From here the OK key can also be used to navigate between the pages.

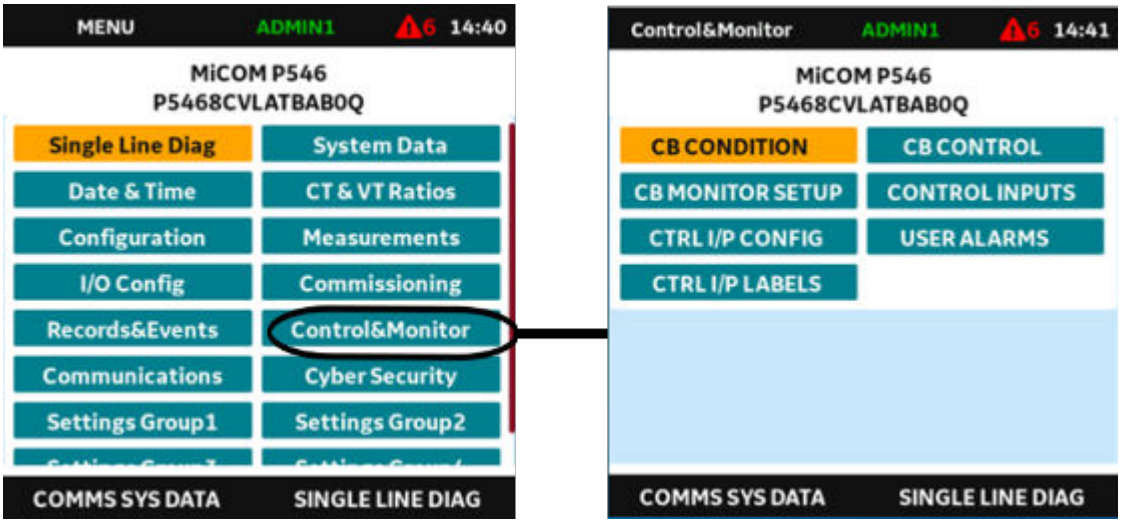
The Menu view can be directly navigated to by long pressing the "Read/Home" key.



Previous level in the navigation hierarchy may be reached by pressing the "Cancel/Reset" key.

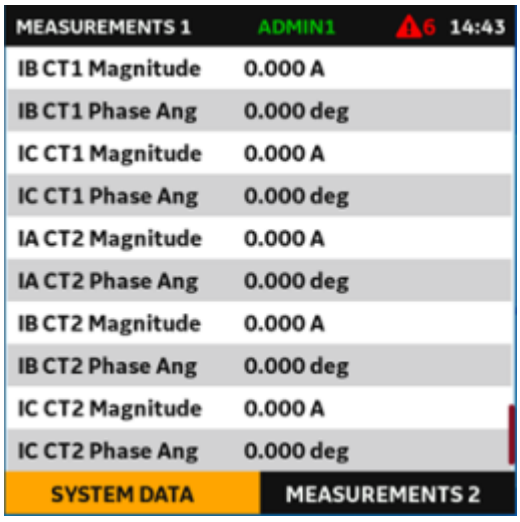


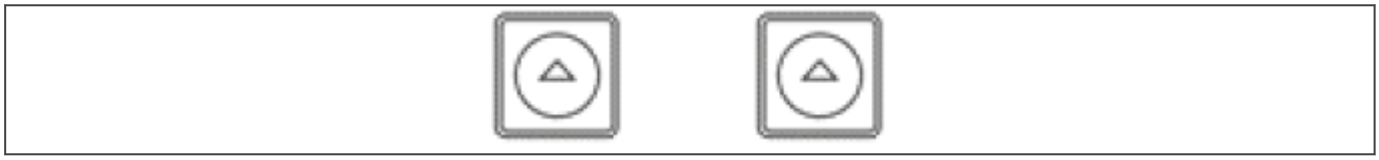
From the HMI Default Display, you can navigate to the required view or open up a Submenu using hierarchical navigation. For example, by selecting Controls & Monitor, a Submenu is opened.



As an alternative to hierarchical navigation, the views may be navigated to in sequence by using the hot keys as “Next” and “Previous” buttons, and is referred as horizontal navigation.

For example, you can move to either ***SYSTEM DATA*** or ***MEASUREMENTS 2*** Views using the horizontal navigation, menu contexts hot keys situated directly under the screen.





5.3.5 PROCESSING ALARMS AND RECORDS

While there are no alarms, the Alarm Icon on the top banner is shown as:



While there are any standing alarms, the standing alarm count will be highlighted in red in the top HMI banner and the yellow alarm LED will flash.



To launch the alarm list view, select the alarm counter in the HMI top banner and press the **OK** key. The alarm view list may be scrolled to view all alarms.

New standing and fleeting alarms may be accepted by selecting the alarm and pressing the **Ack/Clear** menu context key. Rescinded alarms may also be cleared by selecting the alarm and pressing the **Ack/Clear** menu context key.

All visible alarms may be selected by pressing the **Select All** menu context key.

The "*reset indication*" command may be issued to reset latched alarms and accept the flashing led notification. A "*reset indication*" may be issued from the "*View Records*" HMI settings view or by pressing **Ack/Clear** alarm context key.

"*Ack/Clear*" and "*reset indication*" commands are available to users with ENGINEER or OPERATOR or INSTALLER roles.

To return to the launch view from the alarm view press the **Cancel** key.

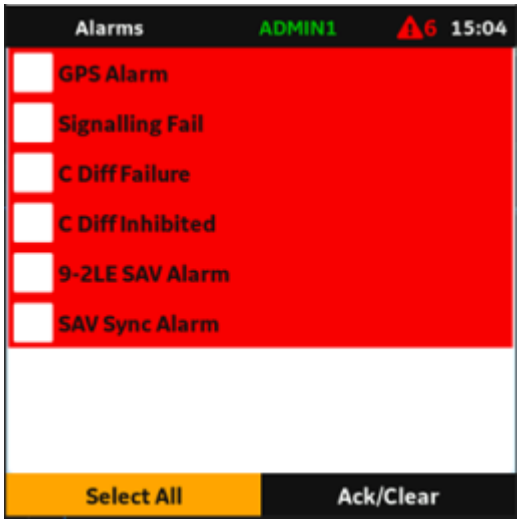


Figure 35: HMI alarms display

5.3.6 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

5.3.6.1 CIRCUIT BREAKER CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the circuit breaker selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the ***CB Control by*** setting is selected, to option 1 *Local*, option 3 *Local+Remote*, option 5 *Opto+local*, option 7 *Opto+Rem+local* or option 8 *L/R Key* in the *CB CONTROL* column users are allowed to use the Trip and Close Key on the front panel to operate the CB.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***CB control by*** setting to *L/R Key*
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is green and the Local mode is selected. When the DDB status is FALSE, the L/R

Key LED is red and the REMOTE mode is selected. ***The L/R Key Status*** DDB status is stored in non-volatile memory, so that it's status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant which you require to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the Open or Close key to operate

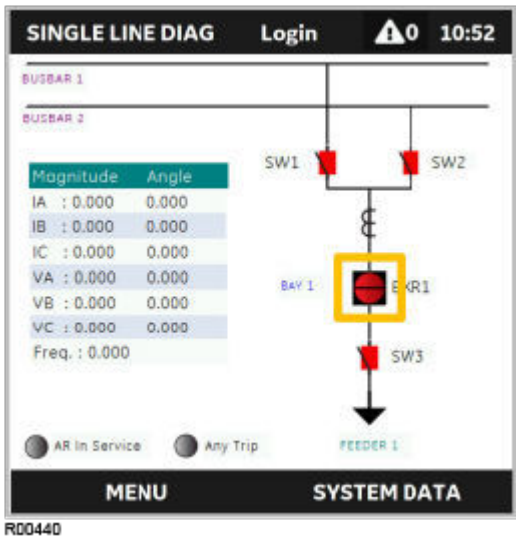


Figure 36: HMI SLD display

For the Circuit Breaker Commands from HMI, additional checks are done:

If the CB is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "Control by" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "Control by" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "Control by" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - In Remote Control".

If the associated local DDB is set to local, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

5.3.6.2 SWITCH CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the switches selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the Switch Control by setting is selected to option 1 *LOCAL*, option 3 `Local+Remote` or option 4 `L/R Key` in the SWITCH CONTROL column, users are allowed to use the Open and Close Key on the front panel to operate the SWITCH.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***Switch Control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R

Key LED is green and the REMOTE mode is selected. The **L/R Key Status** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant you want to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the OPEN or CLOSE key to operate

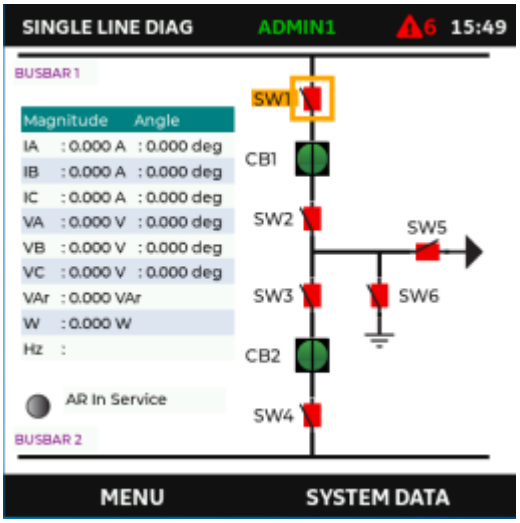


Figure 37: HMI SLD display

For the Switch Commands from HMI, these additional checks are done:

If the Switch is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "***Control by***" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - In Remote Control."

If the associated local DDB is set to local, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

5.3.7 MENU STRUCTURE

Settings, commands, records and measurements are stored in a local database inside the IED. When using the Human Machine Interface (HMI) it is convenient to visualise the menu navigation system as a table. Each item in the menu is known as a cell, which is accessed by reference to a column and row address. Each column and row is assigned 2-digit hexadecimal numbers, resulting in a unique 4-digit cell address for every cell in the database. The main menu groups are allocated columns and the items within the groups are allocated rows, meaning a particular item within a particular group is a cell.

You do not need to scroll through each of the columns horizontally to access a specific setting view. The ‘Home Page’ can be used to quickly access the required column/setting view. Each column contains all related items, for example all of the disturbance recorder settings and records are in the same column.

There are three types of cell:

- Settings: this is for parameters that can be set to different values
- Commands: this is for commands to be executed
- Data: this is for measurements and records to be viewed, which are not settable

Note:
Sometimes the term "Setting" is used generically to describe all of the three types.

The table below, provides an example of the menu structure:

SYSTEM DATA (Col 00)	VIEW RECORDS (Col 01)	MEASUREMENTS 1 (Col 02)	…
Language (Row 01)	"Select Event [0...n]" (Row 01)	IA Magnitude (Row 01)	…
Password (Row 02)	Menu Cell Ref (Row 02)	IA Phase Angle (Row 02)	…
Sys Fn Links (Row 03)	Time & Date (Row 03)	IB Magnitude (Row 03)	…
…	…	…	…

It is convenient to specify all the settings in a single column, detailing the complete Courier address for each setting. The above table may therefore be represented as follows:

Setting	Column	Row	Description
SYSTEM DATA	**00**	**00**	**First Column definition**
Language (Row 01)	00	01	First setting within first column
Password (Row 02)	00	02	Second setting within first column
Sys Fn Links (Row 03)	00	03	Third setting within first column
…	…	…	
VIEW RECORDS	**01**	**00**	**Second Column definition**
Select Event [0...n]	01	01	First setting within second column
Menu Cell Ref	01	02	Second setting within second column
Time & Date	01	03	Third setting within second column
…	…	…	
MEASUREMENTS 1	**02**	**00**	**Third Column definition**
IA Magnitude	02	01	First setting within third column
IA Phase Angle	02	02	Second setting within third column
IB Magnitude	02	03	Third setting within third column
…	…	…	

The first three column headers are common throughout much of the product ranges. However, the rows within each of these column headers may differ according to the product type. Many of the column headers are the same for all products within the series. However, there is no guarantee that the addresses will be the same for a particular column header. Therefore, you should always refer to the product settings documentation and not make any assumptions.

5.3.8 DIRECT ACCESS (MENU CONTEXT KEYS)

The IED provides a pair of menu context keys directly below the LCD display, which allows scrolling between column headings (navigation between menu screens). These keys can be pressed at any time during menu navigation to quickly access the menu label displayed in the bottom banner of the graphical HMI.

5.3.8.1 CONTROL INPUTS

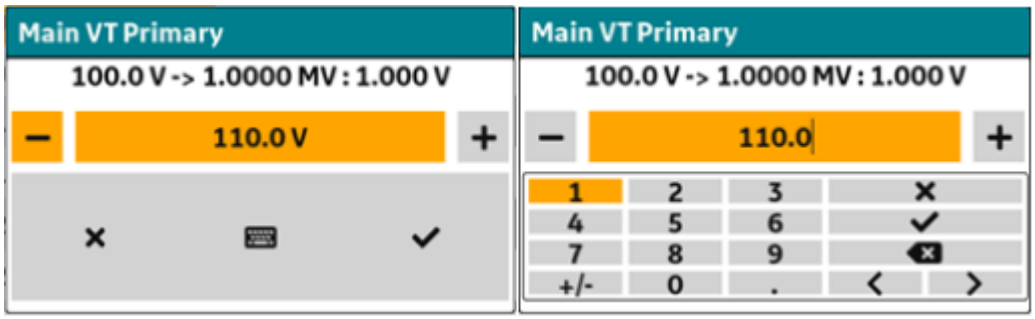
Control inputs cannot be operated through the Menu context keys. To operate control inputs, navigate to the Control Inputs settings view on the front graphical HMI screen, select the relevant control input and Set/Reset as required. RBAC is now applied to access control inputs for operation.

5.3.9 CHANGING THE SETTINGS

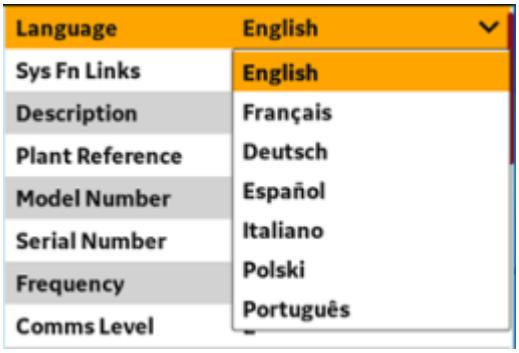
Appropriate user authority or bypass access is required to change the Settings. Please refer to the Cyber Security chapter for user authority details.

- Starting at the default display, highlight the required settings column/menu
- Use the OK key to enter the highlighted settings menu.
- To change the value of a setting, highlight the relevant cell in the menu, then press the **Enter** key to change the cell value. A settings screen will appear next to the cell. If the currently logged in user does not have the level of access required for changing the setting, a pop-up dialog box will inform the user and prevent the settings from being changed. Acknowledge the pop-up message, then navigate to the 'user accounts' section to the top of the screen (top banner) to enter the password for the required access level to change settings.
- To change the value on the settings screen, use the cursor keys to change the desired settings. When more settings are available than can fit on the screen, a scroll bar on the right-hand side appears. In some cases, a virtual keyboard is provided to enter complex characters. The IED maintains dependencies between various settings, and only the applicable settings are displayed for changing.

For Analog Value update, the new analogue value may be entered by selecting the +ve and -ve step buttons or free-form numerals entered by virtual keyboard.

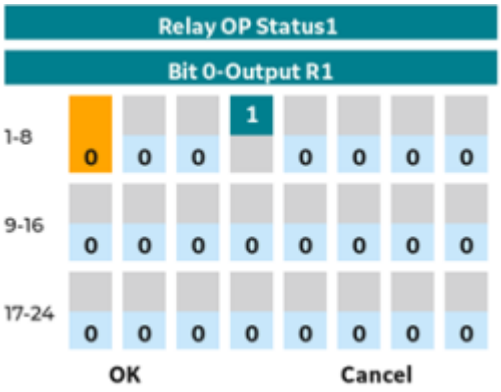


If the setting cell has the facility of drop down, the required setting can be selected from the drop down list.

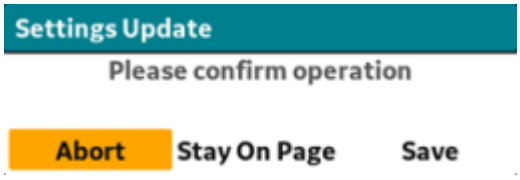


Some of the settings are in the form of Binary Data Bits update. By selecting each of the Bit position the data can be toggled.

Note:
Binary Data Bits can also be used to verify the present data of each bits for monitoring purpose.



- Press the **Enter** key to confirm the new setting value or the **Clear** key or the on-screen ‘x’ to discard it.
- To confirm the new settings, press the **Enter** key. Navigate away from the currently active group settings or press the **Home** key. A Settings update confirmation dialogue box will appear that requires choosing of one of the following options:
- Save - accept all settings including the recently changed settings
- Abort - discard recent changes and keep existing settings
- Stay on page - return to the active settings page without saving recent changes



- To return to the top of the menu, hold down the **Up** cursor key for a second or so, or press the **Clear** key once. It is possible to move across columns from anywhere in the menu by using the Menu context keys at the bottom of the display.
- To return to the default display, press the **Home** key at any time.
- Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.
- The Date and time can be adjusted by navigating to the top banner and selecting the displayed time. Press the **Enter** key to adjust the date and time using the calendar/clock widget that pops up.

Note:
For the protection group and disturbance recorder settings, the changes are not saved unless confirmed using the Settings update confirmation prompt.

Note:
All other Control and support settings (such as Communications and Control inputs), however, are updated immediately after they are entered on the front HMI without the need to confirm using the Settings update confirmation prompt.

5.3.10 FUNCTION KEYS

Most products have a number of function keys for programming control functionality using the programmable scheme logic (PSL).

Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are in the *FUNCTION KEYS* column.

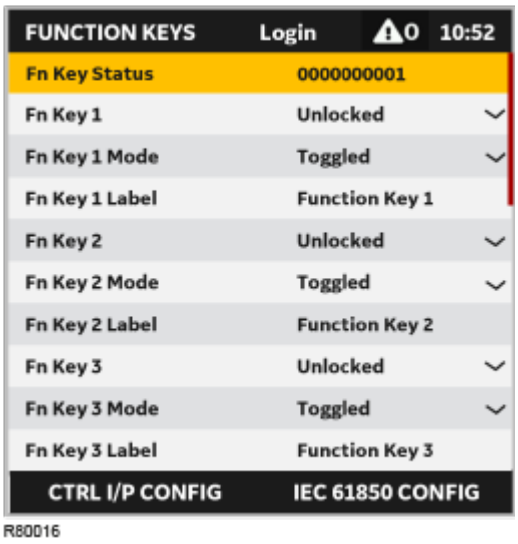


Figure 38: HMI function keys display

The first cell down in the *FUNCTION KEYS* column is the ***Fn Key Status*** cell. This contains a binary string, which represents the function key commands. Their status can be read from the binary string.

The next cell down (***Fn Key 1***) allows you to activate or disable the first function key (1). The ***Lock*** setting allows a function key to be locked. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state, preventing any further key presses from deactivating the associated function. Locking a function key that is set to the Normal mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

The next cell down (***Fn Key 1 Mode***) allows you to set the function key to `Normal` or `Toggled`. In the Toggle mode the function key DDB signal output stays in the set state until a reset command is given, by activating the function key on the next key press. In the Normal mode, the function key DDB signal stays energised for as long as the function key is pressed then resets automatically. If required, a minimum pulse width can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The next cell down (***Fn Key 1 Label***) allows you to change the label assigned to the function. The default label is `Function key 1` in this case. To change the label you need to press the enter key and then change the text on the bottom line, character by character. This text is displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

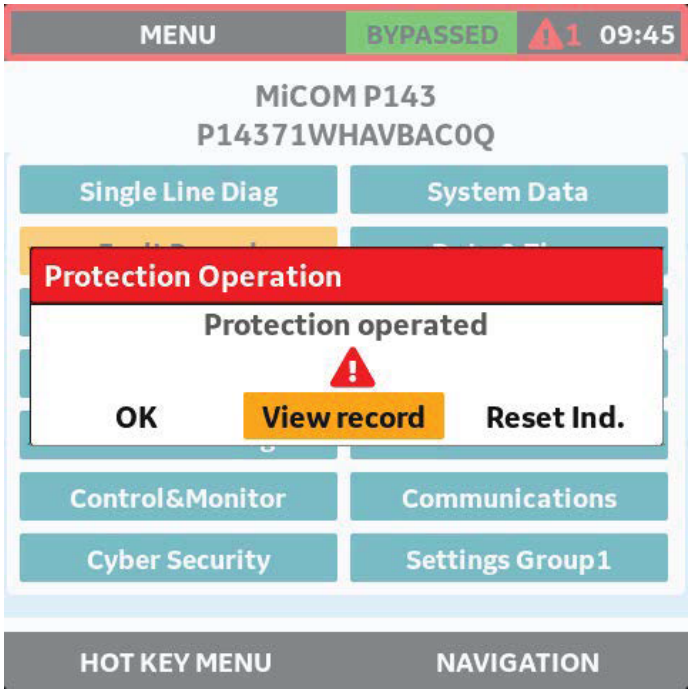
Subsequent cells allow you to carry out the same procedure as above for the other function keys.

The status of the function keys is stored in non-volatile memory. If the auxiliary supply is interrupted, the status of all the function keys is restored. The IED only recognises a single function key press at a time and a minimum key press duration of approximately 200 ms is required before the key press is recognised. This feature avoids accidental double presses.

The function keys needs operator permissions to operate. If operator permissions are not held by the present user an information dialogue is raised to inform the operation has failed.

5.3.10.1 VISUALISATION OF PROTECTION OPERATION

Where there is a protection operation/trip, in addition to the front panel LED indications, the standing trip is indicated on the LCD screen by a red trim around the top banner. Additionally, the LCD backlight becomes lit and a dialogue is presented with three options:



- “OK” - close the dialogue
- “View” - Navigate to the “record” data view and open the latest fault record
- “Reset Ind” - Attempt to reset the trip indication

CHAPTER 6

SAMPLED ANALOGUE VALUES OPERATION

6.1 CHAPTER OVERVIEW

This chapter is only applicable to Software Version AA.

This chapter contains the following sections:

Chapter Overview 90
Introduction To Sample Analogue Values 91
Data Resampling 92
Sampled Analogue Values Alignment 93

6.2 INTRODUCTION TO SAMPLE ANALOGUE VALUES

IEC 61850 Sampled Analogue Value specifications such as IEC61850-9-2 LE or 61869, define Process Bus communications between the different components of the substation automation system. MiCOM Px40 relays support IEC61850-9-2 LE. IEDs with compatible interfaces can communicate with the Process Bus and receive Sampled Analogue Values data from Merging Units. Analogue Merging Units digitise analogue values from conventional CTs and VTs, replacing analogue inputs. This simplifies the installation by replacing the analogue measurement wiring with the Process Bus Local Area Network. Using a fibre optic network instead of heavy copper cables between the measuring device and the IED provides safer and more economical cross-site cabling. It also allows IEDs to receive current and voltage sampled data through Digital Merging Units from Low Power Instrument Transformers such as optical and Rogowski devices.

IEDs, which accept digital Sampled Analogue Values (SAV) rather than analogue signals have no need for expensive and heavy on-board scaling CTs and VTs, making them smaller, lighter, safer and cheaper. A SAV IED with the same size case as a conventional IED would have more room for digital I/O, because valuable space is not taken up by the on-board CTs and VTs.

The following figure shows the difference between a conventional IED with analogue inputs and a Sampled Analogue Values IED with digital inputs:

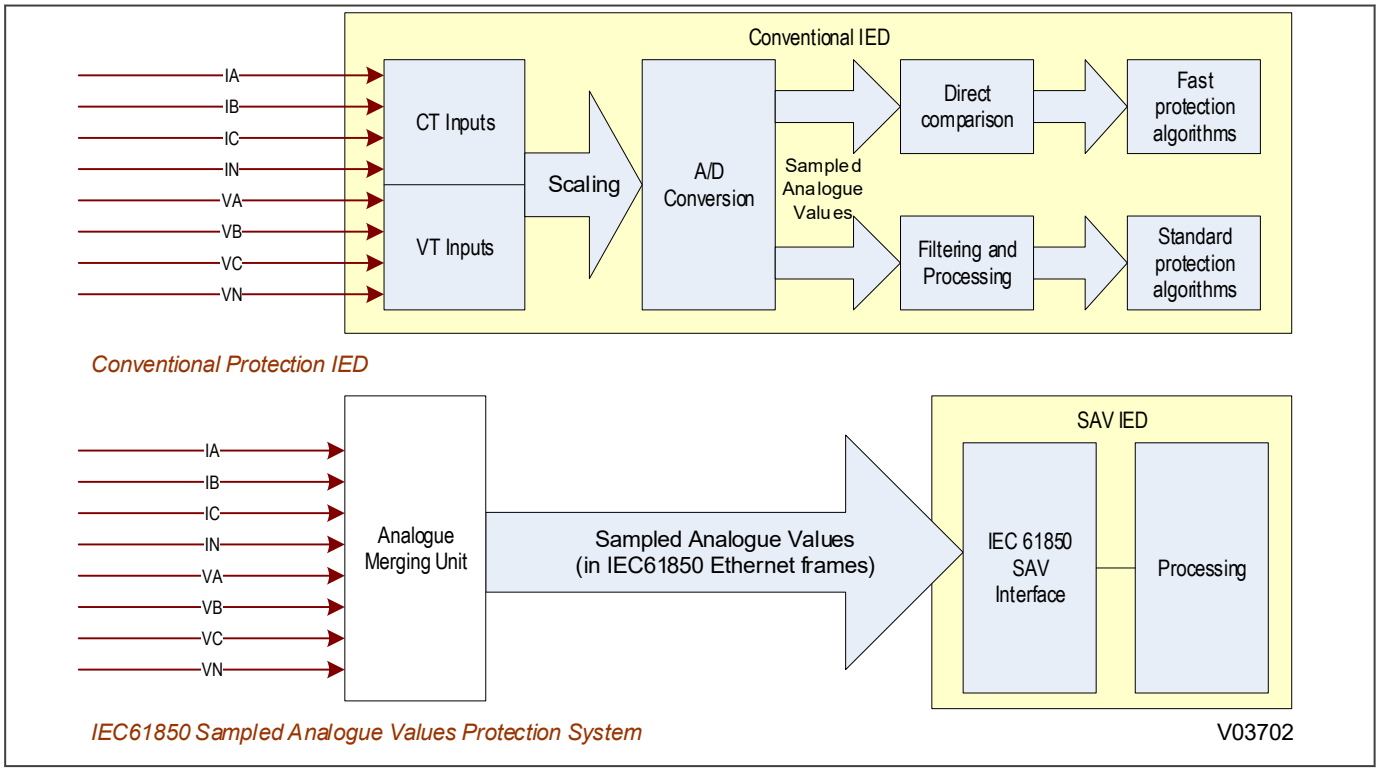


Figure 39: Comparison of conventional IED and sampled analogue values IED

6.3 DATA RESAMPLING

An IEC 61850-9-2LE SAV interface receives 80 Sampled Analogue Values per cycle from the Process Bus. This is the same for both 50 and 60 Hz. The SAV interface then resamples these Sampled Analogue Values to make the data appear the same to the IED as analogue signals would do on its normal inputs from CTs and VTs. The resampling frequency depends on the device.

The IEC 61850-9-2LE interface also tracks the supply frequency. This is because the Sample Analogue Values from the Process Bus are fixed at 4000 samples/sec for 50 Hz and 4800 samples/sec at 60 Hz.

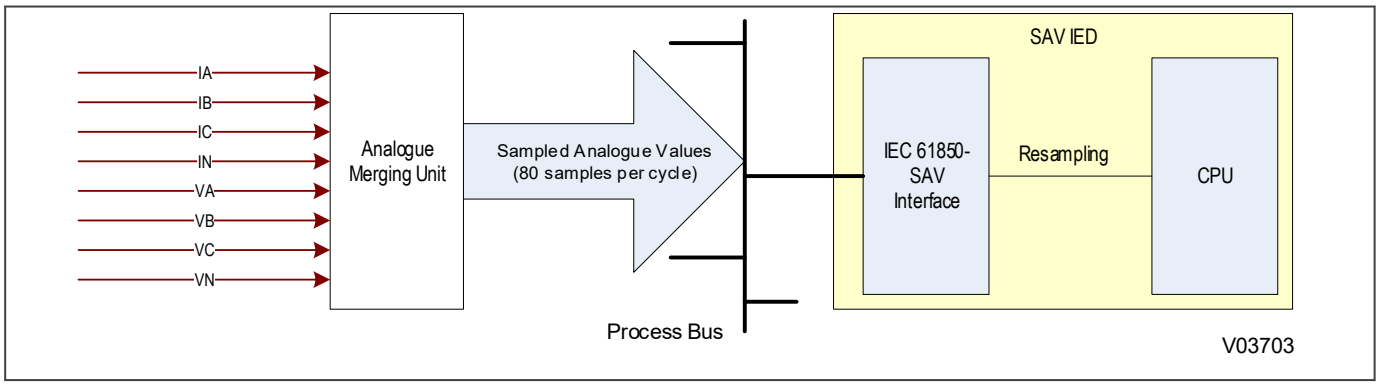


Figure 40: Data sampling using an IEC 61850-9-2LE interface

6.4 SAMPLED ANALOGUE VALUES ALIGNMENT

Sampled Analogue Value frames from different Merging Units on the Process Bus may not arrive at the same time at the IED. The transmission delay depends on the background Ethernet traffic and how many switches are used in the Process Bus network.

Transmission delays do not usually matter for functions such as three-phase overcurrent protection where current signals are all received in a single frame. However, a function such as distance protection uses voltage and current signals which may be from different merging units with different transmission delays. The SAV interface synchronises the voltage and current samples that are sent to the IED's distance protection function. The IED then uses the ***Merge Unit Delay*** setting, which is set to the maximum expected delay between the first and last Sampled Analogue Values.

The following examples show how you would need to set the delay.

- If the IED receives one Logical Node only, no delay is needed so set the merging unit delay to `0 ms`.
- If the IED receives several Logical Nodes at the same time, no delay is needed so set the merging unit delay to `0 ms`.
- If the IED receives several Logical Nodes but not at the same time, set the merging unit delay to an appropriate non-zero value.

If all the Logical Nodes configured in the IED are not received during the merging unit delay time, an alarm is raised.

To set the merging unit delay during commissioning, set ***MUs Delay Search*** to `Yes`. The IED then monitors the Sampled Analogue Value frames received for the next two seconds and displays the maximum delay between identical samples.

6.4.1 CHANNEL MAPPINGS FOR SAV TEST, SAV QUESTIONABLE, SAV INVALID

These signals correspond to the analogue channels in a conventional MiCOM IED. The channel name appears on the IED display against each bit.

P446, P546, P841B

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
VA	VB	VC	VSC1	IA1	IB1	IC1	IM	INSEN	IA2	IB2	IC2	VSC2											

P443, P543, P841A

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
VA	VB	VC	VSC1	IA1	IB1	IC1	IM	INSEN															

6.4.2 DATA QUALITY

Any degradation in the measurement or transmission of Sampled Analogue Values means that the protection function of the IED may not operate correctly. Data frames from a typical Logical Node have quality flags assigned to each of the channels. The device adapts the behaviour of protection functions according to these quality flags. The available quality flags are *Good*, *Invalid* and *Questionable*. A *Test* flag is also available for test purposes.

A protection function operates normally when all the necessary Sampled Analogue Value inputs are available and have a *Good* Quality flag. When the flag for one or more of the Sampled Analogue Value inputs changes to *Invalid,* the protection function is inhibited. When the flag for one or more of the Sampled Analogue Value inputs changes to

Questionable, the protection function can either be inhibited or not, depending on the chosen options in the ***Trus Ques Data*** setting. The options are:

- Bit 0:Out of Range
- Bit 1:Bad Reference
- Bit 2:Oscillatory
- Bit 3:Old Data
- Bit 4:Inconsistent
- Bit 5:Inaccurate

The protection function will be trusted and NOT inhibited for questionable data for the items above which have been set.

The protection function returns to the *Normal* state when the quality flags for all the necessary Sampled Analogue Value inputs are *Good*. The quality flags can change with each sample, therefore there is a one-cycle transition delay between the *Normal* and *Inhibit* states for each protection function.

6.4.2.1 IMPACT OF DATA QUALITY ON PROTECTION FUNCTIONS

The following table shows how Sampled Analogue Value errors affect protection functions in the IED.

For example, overcurrent protection can be configured as directional, in which case the voltage inputs have an impact on the function. The quality of the voltage input is not important if the overcurrent is non-directional.

X means the SAV input affects the Normal and Inhibit states of the protection function.

means the protection function is affected where configured to work with this input.

$ means that frequency protection operates if any one current or voltage phase is good quality.

	$[I_{A1}\ I_{B1}\ I_{C1}]$	$[I_{A2}\ I_{B2}\ I_{C2}]$	$[V_A\ V_B\ V_C]$	V_{SC1}	V_{SC2}	$I_{N\ SEN}$	I_M
Differential Protection	X	#	#				
Distance Protection	X	#	X				
Directional Earth Fault	X	#	X				
Overcurrent Protection	X	#	#				
Negative Sequence	X	#	#				
Broken Conductor	X	#					
Earth Fault Protection	X	#	#				
REF Protection						X	
SEF Protection						X	
Residual Overvoltage			X				
Voltage Protection			X				
Frequency Protection	$	$	$				

6.4.3 PROCESS BUS PERFORMANCE

Ethernet networks sometimes lose frames, so the IED tolerates some loss of samples to ensure availability of its protection functions. The IED calculates a ***Frame Loss Rate*** every cycle for each Merging Unit (Logical Node) with which it communicates. If the ***Frame Loss Rate*** is less than the ***Loss Rate Level*** setting (set in %), the IED tolerates network losses of up to three consecutive samples. If the ***Frame Loss Rate*** is greater than the ***Loss Rate Level*** setting (set in %), the protection functions are temporarily inhibited.

The IED display shows information about Sampled Analogue Value losses on the Process Bus for each Logical Node associated with the IED in the following cells in the *IEC 61850-9.2LE* column. This is useful during testing or commissioning to identify and resolve any network problems which could degrade the protection scheme.

The following data is provided:

LNx LossRate Sec: This is the percentage of SAV frames missing during the past second for LNx.

LNx FrmLoss Cuml: This is the number of frames lost since the last reset. The most recent reset time is listed in the IED menu.

LNx Error Second: The Frame Error Seconds is a cumulative value since the last reset. If the Frame Loss Rate exceeds 1.25% (one sample per cycle on average for one second), the IED records this as an Error Second.

where x is the number of the node (e.g. LN1)

The Sampled Analogue Values loss data can be reset manually with the ***LossRate Reset*** command in the *IEC61850-9.2LE* setting column.

6.4.4 VT SWITCHING

This function is used in the P44, P54 and P84 IEDs which have an IEC 61850-9-2LE interface. It allows the user to switch the three-phase voltage input between two independent Sampled Analogue Value frames while the IED is in service. This may correspond to two separate voltage transformers in the primary system. The VT Switch function also allows the single-phase check synchronising voltages to be selected from three independent Sampled Analogue Value frames.

The VT switching function is disabled by default. To enabled it, in the IED menu *IEC 61850-9-2LE*, select ***VT Switch Mode*** to `Enabled`.

Three-phase voltage input switching

The three-phase voltage can be switched between two Sampled Analogue Value frames. These are [VA1 VB1 VC1] and [VA2 VB2 VC2]. The switching is controlled by the status of the DDB VABC Select x. The logic is shown in the following table.

DDB VABC Select x	VA VB VC Selection
0	VA1 VB1 VC1
1	VA2 VB2 VC2

The change of VT input is accepted only if the DDB status change is effective for a minimum of 20 ms. The selected three-phase voltage is only displayed when VT Switch Mode is enabled.

Single-phase voltage input switching

There are two single-phase voltages associated with the System Check functions for CB1 and CB2. These are Vsc1 (***Sys Checks CB1***) and Vsc2 (***Sys Checks CB2***). The selection of the voltage source for Vsc1 is controlled by the combined status of two DDBs, Vsc1 Select x1 and Vsc1 Select 1x as shown in the following table.

DDB Vsc1 Select x1	DDB Vsc1 Select 1x	Vsc1 Selection
0	0	Vcs1
0	1	Vcs2
1	0	Vcs3
1	1	Unused

The selection of the voltage source for Vsc2 is controlled by the combined status of two DDBs, Vsc2 Select x1 and Vsc2 Select 1x as shown in the following table.

DDB Vsc2 Select x1	DDB Vsc2 Select 1x	Vsc2 Selection
0	0	Vcs2
0	1	Vcs3

DDB Vsc2 Select x1	DDB Vsc2 Select 1x	Vsc2 Selection
1	0	Vcs1
1	1	Unused

The selected single-phase voltages are only displayed when VT Switch Mode is enabled.

6.4.5 VIRTUAL INPUTS AND OUTPUTS

Sampled Analogue Value IEDs have virtual inputs and virtual outputs which are mapped as new DDBs in the IED's PSL and are used as triggers for GOOSE messages to and from the IED. The GOOSE Control Blocks can be configured using the IEC 61850 Configurator software tool, which is part of the Settings Application Software.

The inputs and outputs make it easier to apply the IEDs in full Digital Substations where switchgear status, controls and commands are exchanged as GOOSE messages between the IEDs and Merging Units.

6.4.5.1 VIRTUAL CT AND VT RATIO SETTINGS

The Sampled Analogue Value frames are primary measurements. These come from Merging Units (MU) connected to conventional CTs and VTs or Non-Conventional Instrument Transformers (NCITs). Alternatively they may come directly from NCITs. The IED algorithms are typically based on secondary values. If primary values are needed, they are calculated by the IED based on set CT or VT ratios.

The amplitudes for 1A CT inputs are limited to 64 A secondary. The amplitudes for 5A CT inputs are limited to 320 A secondary. The VT secondary is limited to 200 V phase-to-earth. Therefore it is necessary to set appropriate CT and VT ratios for the protection functions to operate correctly. The instrument transformer ratios are set in the IED menu *CT AND VT RATIOS*, which is common to both conventional and Sampled Analogue Value IEDs.

Measurement from a merging unit connected to a CT

As this has a real CT ratio, set the real primary CT ratio.

Direct measurement from an NCIT

There is no physical CT ratio. Set the CT ratio high enough so the maximum primary current (maximum fault level) when converted to secondary is not clamped.

For example if the maximum primary current is 50 kA:

- If the CT ratio is set to 1000:1 the converted secondary current is up to 50 A. This is less than 64 A so is acceptable.
- If the CT ratio is set to 500:1 the converted secondary current is up to 100 A. This is above 64 A so is not acceptable.

6.4.6 IED ALARMS

Sampled Analogue Value IEDs have additional alarms.

9-2 configuration alarm (9-2LE Cfg Alarm)

This alarm is raised if analogue channels in the IED are assigned incorrectly (Illegal Channel Map). For example, if you assign two current inputs to the same Logical Node.

Sampled analogue values quality alarm (9-2LE SAV Alarm)

This alarm is raised if any of the following conditions exist:

- One or more of the Sampled Analogue Value frames received are not synchronised as required by the IED configuration.
- One or more of the Sampled Analogue Value frames expected are not received.

- One or more of the Sampled Analogue Value frames received are of *Invalid* quality.
- One or more of the Sampled Analogue Value frames received are of *Questionable* quality and the IED is configured not to accept such Sampled Analogue Value frames.
- One or more of the Sampled Analogue Value frames received has a test flag, and the IED is configured to inhibit protection functions when receiving frames with a test flag.
- One or more of the Sampled Analogue Value frames received does not have a test flag, and the IED is configured to receive only frames with a test flag.
- Sampled Analogue Values received have a nominal frequency different to that set in the IED.
- The secondary current or voltage exceeds the acceptable limit.

6.4.6.1 P54 ALARMS

Sampled analogue values global synchronisation alarm (SAV Sync Alarm)

This alarm is raised if the global synchronisation for Sampled Analogue Values has failed, inhibiting the current differential function.

Inverse settings alarm (Invalid Sync Set)

This alarm is raised if ***Phase Diff*** is set to `Enabled` but ***GPS Sync*** is set to `GPS disabled`.

6.4.7 REDUNDANT CONFIGURATION

If the Sampled Values card supports redundant Ethernet all parameters related to Ethernet Network Communications must be configured using Redundant Ethernet Configurator.

> *Note:*
> *Settings related to Sampled Values are done in the settings file.*

Detecting the Ethernet card

Connect the PC to the relay using the same Ethernet network. The most reliable way to perform this configuration is to connect to the fibre optic port using a media converter or an Ethernet switch isolated from the rest of the network. This simplifies the task of spotting the correct card for the desired equipment.

Once physically connected, launch Redundant Ethernet Configurator and log in as an administrator using the default user Admin and the password Admin.

Select the Network board on the PC that is connected to the same switch as the Sampled Values card. Then click on the button, Identify Device.

All redundant cards connected on the same Ethernet network will be shown. Identify the correct card by confirming the Station bus text is shown under Board Type.

Configuring network parameters

Use the IP configuration button to set an IP address on the card. It is not possible to set a default gateway and so these cards can’t be controlled through remote networks in any way.

Use SNTP configuration to set an SNTP server. The server must be in the same Ethernet network.

Configuring redundant parameters

The card available redundant options will be displayed when selected. If the card is set to PRP, HSR or Failover select the corresponding button and perform the required settings accordingly. Use the radio buttons to switch between supported protocols, confirming your choice by pressing the Update button.

Configuring password

The default password for committing changes is AAAA. The password can be changed using the Password Configuration button. If the password is not known, it can be recovered by creating a recovery code and submitting it to the GE Vernova contact centre. Once the customer has been verified, the contact centre will provide a recovery password.

Note:
Each recovery password is unique and the relay re-rolls the recovery password every time the relay is rebooted. If the request for a recovery has been submitted to the contact centre, the relay must stay powered on until the recovery password is used or the password will be re-rolled, and it won't be usable.

MAC table

The MAC table allows the user to see the MAC address of the devices connected in the same Ethernet network as the Sampled Values card.

Filtering database

The Filtering Database allows users to filter traffic using MAC addresses. This is not recommended unless the user understands clearly the impact of filtering MAC addresses.

Update firmware

This option allows the user to change the firmware of the Sampled Valued network related firmware. Instructions on when and how to perform this as well as any required firmware files can only be obtained through After Sales.

CHAPTER 7

CURRENT DIFFERENTIAL PROTECTION

7.1 CHAPTER OVERVIEW

This product provides biased, phase-segregated, numerical Current Differential protection.

This chapter introduces the principles and theory behind Current Differential protection and describes how they are implemented in this product. Guidance for applying this protection is also provided.

The current differential protection is enabled by default, but it can be disabled if you don’t want to use it. The current differential protection needs digital communications links to exchange the values of current between the terminals in the scheme.

This chapter contains the following sections:

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Current Differential Protection Principle 101
Synchronisation of Current Signals 103
Phase Current Differential Protection 106
Neutral Current Differential Protection 109
Three-Terminal Schemes 111
Transient Bias 114
Capacitive Charging Current Compensation 115
CT Compensation 116
Feeders with In-Zone Transformers 118
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Current Differential Intertripping 128
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Stub Bus Differential Protection 131
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7.2 CURRENT DIFFERENTIAL PROTECTION PRINCIPLE

Current differential protection is based on Kirchoff's Law. It generally uses the Merz-Price principle in which the sum of the currents entering the protected zone should equal the sum of the currents leaving the protected zone. A difference between these currents is known as differential current. If the differential current exceeds a threshold, then a protection device may be required to trip. If the differential current is below the threshold then it is expected to restrain.

Errors caused by mis-match of the current transformers at the different terminals, or saturation of the current transformers during external faults could lead to false tripping under healthy conditions. For that reason a restraining quantity is normally applied so that when the magnitude of the current in the system rises, so the level of differential current necessary to cause a trip rises. The level of restraint applied is called a bias quantity and its relationship to the operate quantity is called a Biased Differential characteristic.

Current differential protection does not need voltage transformer inputs, but they can be employed to enhance capacitive charging, current compensation, protection, control, automation, and supervision features of this product for certain applications.

To provide current differential protection of transmission lines and distribution feeders, it is normal practice to have similar devices at each terminal with interconnecting communications links to exchange current signal information between terminals.

When applying numerical current differential to protection of transmission lines and distribution feeders, as well as communicating details of the local current measurements, the product also communicates timing, status, and control data to remote terminals. The current, timing, status, and control data are encapsulated into messages (sometimes referred to as telegrams) which are transmitted frequently and regularly. The timing data is used to align local and remote current measurements. The control and status data is used for purposes such as intertripping. Messages are secured by an address field as well as a cyclic redundancy check code (CRC code). The use of the address field ensures that only the intended receiving device will respond to the message. Corruption of the data in the messages could potentially cause the product to trip incorrectly. The use of the CRC code together with other error checking prevents this.

7.2.1 NUMERICAL CURRENT DIFFERENTIAL PROTECTION

At each terminal in the scheme the power system current input quantities are acquired, converted into numerical values, filtered, and compared with current input values from the other terminal(s) in the scheme.

For each phase, and at each terminal, the vector sum of the currents entering the protected zone is calculated. This is known as the Differential current and provides an operating quantity. Also calculated is the scalar sum of the same currents, of which a proportion is used as a restraining quantity. This is known as the bias current. To determine whether tripping should occur, the Differential Current is compared with a percentage of the Bias Current. If it is exceeded then a trip can be initiated.

The Differential and Bias currents are calculated on a per phase basis, and the tripping decision is made on a per phase basis. However, the Bias current used in the calculation is the same for all three phases and is based on the highest of the Bias currents calculated for each phase. This is called Maximum Bias and improves discrimination for single phase faults.

The relays also perform differential protection on the neutral current. A similar biasing principle is applied, but the characteristic is generally different.

Products are available to protect two-terminal and three-terminal lines and feeders. Models are therefore available with one or two communications channels for the Current Differential protection function. Models with two channels can be used to protect two-terminal or three-terminal feeders. In both of these cases, inherent communications redundancy assures integrity of the protection in the event of a single communication link failure. With a single communications channel, the application is restricted to the protection of two terminal lines and the protection is compromised if the communication channel fails.

The tripping characteristics for two-terminal and three-terminal applications are similar, but two-terminal applications use two current values for the evaluation of the Bias and Differential currents, whereas three-terminal applications use three current values (one from each terminal) for the evaluation of the Bias and Differential currents.

Line differential protection requires the comparison of power system quantities taken at the different line terminals. For a meaningful comparison, synchronisation of the current signals is needed so that they are related to a common time reference. Different methods are used to achieve current signal synchronisation – some requiring external time reference signals, and some using internal timing signals.

7.3 SYNCHRONISATION OF CURRENT SIGNALS

To ensure accuracy of the calculation of the differential current, the locally derived current values and the values derived from inputs at remote terminals must be aligned to a common time reference before the differential calculations are made. This process is called ‘Time Alignment’ or ‘Synchronisation’

Synchronism could be achieved by using accurate time signals from sources such as atomic clocks or the Global Positioning Satellite (GPS) system. This product can synchronise using a GPS input, and this is recommended for schemes using communications that may be subject to switching. For many applications, however, this is not necessary, and the product can self-synchronise using a technique known as “ping-pong”.

7.3.1 TIME ALIGNMENT USING PING-PONG TECHNIQUE

The following figure demonstrates the ping-pong technique for a two-terminal protection scheme. the two terminals are referred to as “End A” and “End B”.

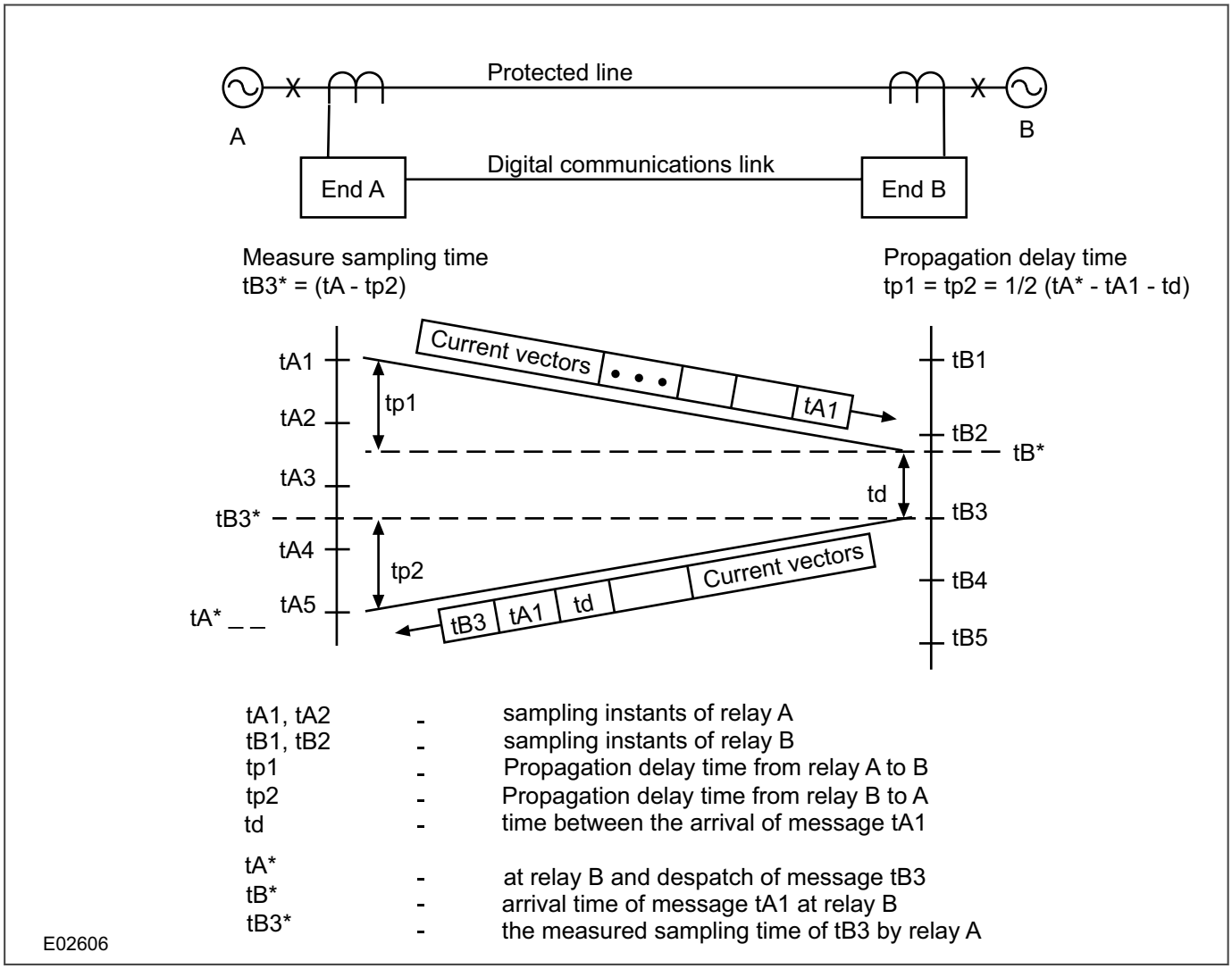


Figure 41: Ping-pong measurement for alignment of current signals

The device at End A samples its current signals at times tA1, tA2, etc. The device at End B samples its current signals at time tB1, tB2, etc. The sampling of the signals at the two ends are not synchronised, but both operate in the same way. The filtering and processing of the current inputs produces current vectors together with timing information, which are sent between devices as shown in the figure.

At time tA1, End A sends a data message to End B. The message contains a time tag, tA1, plus other timing, control, and status information as well as the calculated current values. The message arrives at End B after a channel after a propogation delay time tp1. End B registers the arrival time of the message as tB*.

Since the devices at both terminals operate in the same way, End B also sends messages to End A. In the figure, End B sends a message at tB3. The message contains the time tag tB3. It also returns the last received time tag from End A (tA1) and the delay time, td, between the time of the the message was received, tB*, and the sampling time, tB3, where td = (tB3 - tB*).

The message arrives at End A after a channel propagation delay time, tp2. The arrival time is registered by End A as tA*. From the returned time tag, tA1, End A can measure an elapsed time as (tA* - tA1). This equals the sum of the propagation delay times, tp1, and tp2, as well as the time between End B receiving the message and returning it. So:

$$(tA^* - tA1) = (td + tp1 + tp2)$$

The device assumes that the time to communicate data between two terminals is the same in each direction, and on this basis tp1 and tp2 can be calculated as:

$$tp1 = tp2 = \tfrac{1}{2}(tA^* - tA1 - td)$$

The propagation delay time is measured for each received message. This is used to monitor changes on the communication link and to manage the response of the protection. When the propagation delay time has been calculated, the sampling instant of the received data from End B (tB3*) can also be calculated. As shown in the figure, the sampling time tB3* is measured by End A as:

$$tB3^* = (tA^* - tp2)$$

In the figure, tB3* is between tA3 and tA4. To calculate the differential and bias currents, the values at each terminal must correspond to the same point in time. So the values received at tB3* must be aligned with values taken at sampling instants tA3 and tA4. This is achieved by rotating the received current vector by an angle corresponding to the time difference between tB3* and tA3 (and tA4).

After this time-alignment process, the respective differential and bias currents can be calculated.

7.3.2 GPS SYNCHRONISATION

In schemes where protection communications operate over switched communication channels, there is a possibility of asymmetry of communications channels between connected terminals. The term “asymmetry” is used to describe an application in which the time taken to communicate information between a pair of connected terminals is different in one direction to the other.

If the communication between devices is asymmetric, the ping-pong method of synchronisation may not work correctly, so the products are equipped with features designed to provide stability for asymmetric communications.

To overcome the shortcomings of the ping-pong technique, each device provides a GPS input, which can be used together with an appropriate synchronising device (RT430). GPS synchronisation works with asymmetric communications paths.

The GPS synchronisation device produces a synchronisation signal that can be connected to the protection device via optical fibre. If you have an application that needs GPS synchronisation, you must connect the GPS synchronisation input on the protection, and you must enable the function using the ***GPS Sync*** setting in the *PROT COMMS/ IM64* column.

The figure below shows the different propagation delays and how compensation is applied. The GPS synchronisation compensates for the different delays associated with the transmit and receive communication paths.

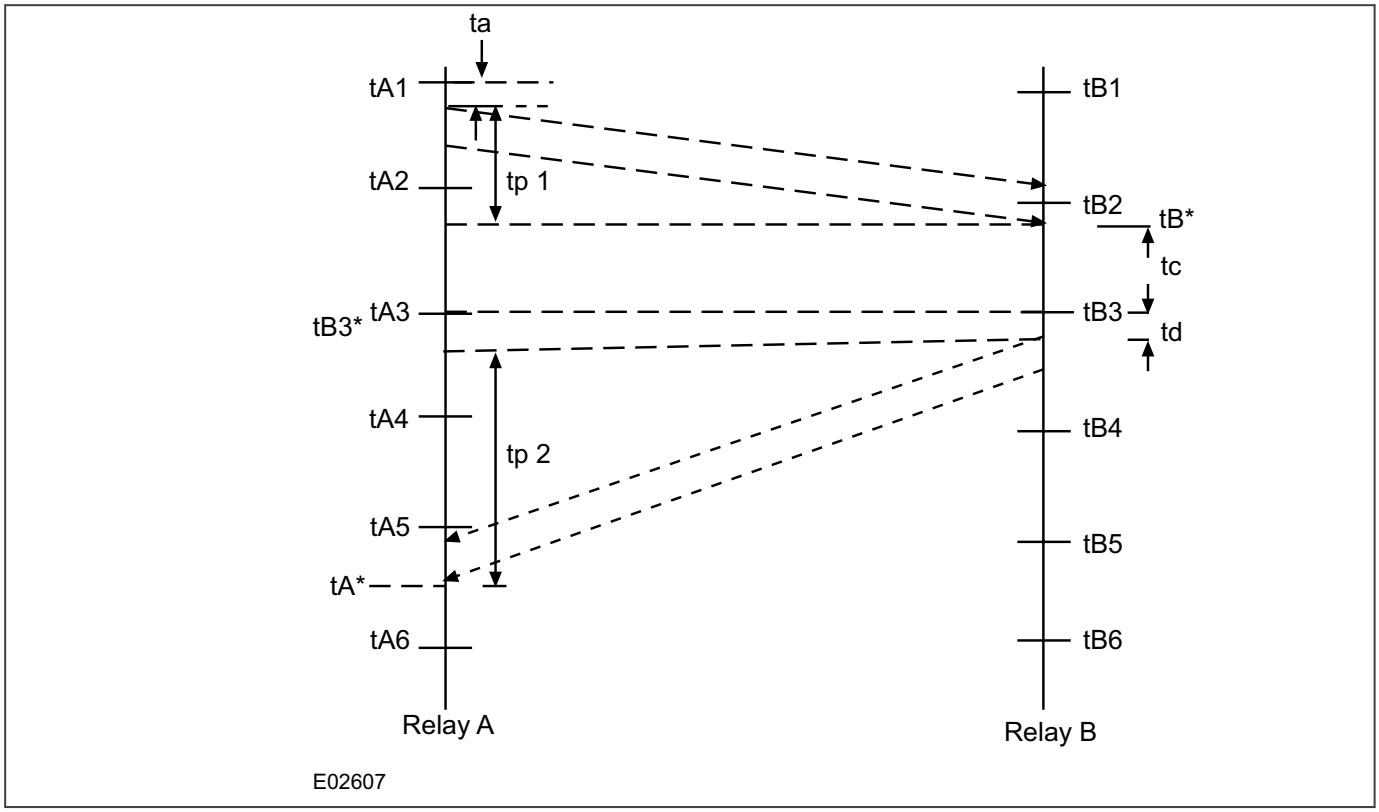


Figure 42: Asymmetric propogation delay times

The GPS synchronised values at terminal A (tA1, etc.) can be individually compared with those at terminal B (tB1, etc.) to derive the bias and differential currents. The propagation delay times are not required for the derivation of the bias and differential currents, but they can be calculated individually as tp1, and tp2, and they are stored for potential use if GPS synchronisation fails.

7.4 PHASE CURRENT DIFFERENTIAL PROTECTION

By appropriate model selection, current differential protection can be provided for two-terminal or three-terminal feeders. Products that have two protection communications channels fitted can be applied to the protection of three-terminal applications.

To uniquely identify the different terminals in a scheme, a naming convention is used in the product. It uses the terms ‘Local’ and ‘Remote’. ‘Local’ is applied to the device being described. ‘Remote’ refers to a connected device. For a two-terminal application, the remote device is referenced in the *MEASUREMENTS 3* column, etc., as ‘Remote 1’. When a third terminal is included it is referenced as ‘Remote 2’, connected to the protection communication channel 2.

So, for a three terminal scheme, the reference terminal is the Local terminal, and it connects to Remote 1 via communications channel 1, and to Remote 2 via communications channel 2.

At each device in the scheme, the remote current measurements received through the communications links are processed and compared with the local signals to derive the differential current and bias current values on a per-phase basis.

Derivation of the differential and bias currents needs to use local and remote current measurements taken at the same point in time, but the sampling of the current signals of these devices is not directly synchronised. If not corrected, this would cause errors. Correction is also needed to compensate for the delays involved in communicating measurements between terminals. This compensation process is called “time alignment”. The time-alignment process transposes remote current measurements to align them to local ones. After time alignment of the remote current measurements to the local current measurements the differential and bias currents can be calculated as:

- Differential current (IDiff) = vector summation of all currents entering the protected zone
- Bias current (IBias) = half the scalar sum of the currents entering the protected zone.

The differential and bias currents are compared against a tripping criterion which is defined by a dual-slope characteristic as shown below. The figure shows the tripping criteria for protection of a three-terminal feeder, but the principle is similar for a two-terminal feeder.

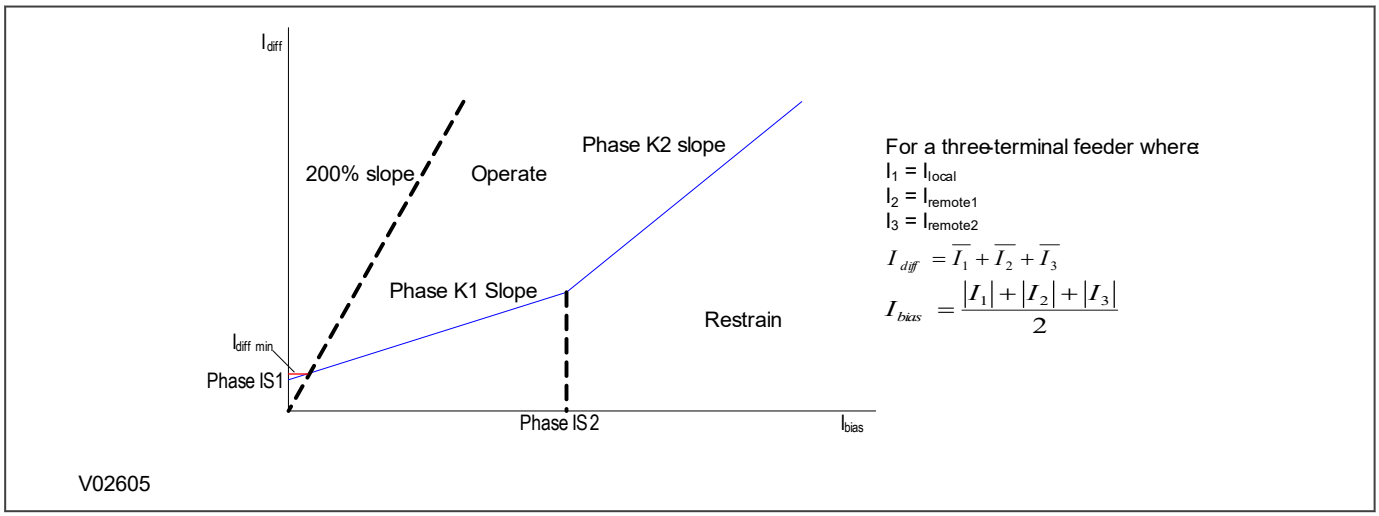


Figure 43: Dual slope current differential bias characteristic

7.4.1 PHASE CURRENT DIFFERENTIAL TRIPPING CRITERIA

The phase current differential characteristic is defined by four settings:

- ***Phase Is1***: The basic differential current setting which determines the minimum pick-up level of the protection.
- ***Phase k1***: The lower percentage bias setting used when the bias current is below the ***Phase Is2*** setting. This provides stability for small CT mismatches, while ensuring good sensitivity to resistive faults under heavy load conditions.
- ***Phase Is2***: A bias current threshold setting, above which the higher percentage bias setting ***Phase k2*** is used.
- ***Phase k2***: The higher percentage bias setting used to improve protection stability under heavy through fault current conditions.

The tripping criteria is defined by the bias characteristic graph. Basically if the differential current is above the line, the protection will trip. If it is below, the protection will restrain.

When the phase-differential protection issues a trip command, it sends a per-phase ‘differential intertrip’ signal to the remote terminals to instruct them to trip their circuit breakers. This is to ensure that all ends of the protected line trip, even for marginal fault conditions.

For grading with other protection, the phase differential protection trip signal can be time delayed using either a definite time, or an inverse time characteristic. By default, the delay characteristic is set to definite time with a zero second delay, resulting in instantaneous tripping.

Since differential and bias current calculations are made on a per-phase basis, the values vary on a per-phase basis. For optimum stability the highest value of the three-phase bias currents is used to restrain all three phases.

Minimum trip level

The minimum trip current level (Idiff min) is a function of ***Phase Is1*** and ***Phase k1*** as shown in the following calculation (note: Phase Is1 and Phase k1 have been shortened to just Is1 and k1 for clarity).

$$I_{diff} = k1(Ibias) + Is1 \ ...$$

$$I_{diff} = (k1)(0.5I_{diff}) + Is1 \ ...$$

$$Is1 = I_{diff} - k1.0.5I_{diff} = I_{diff}(1 - 0.5k1) \ ...$$

$$I_{diff} = Is1/(1 - 0.5k1)$$

if k1 has a value of 30% for example, this means that the minimum trip current is 1.176Is1.

7.4.2 PHASE CURRENT DIFFERENTIAL PROTECTION LOGIC

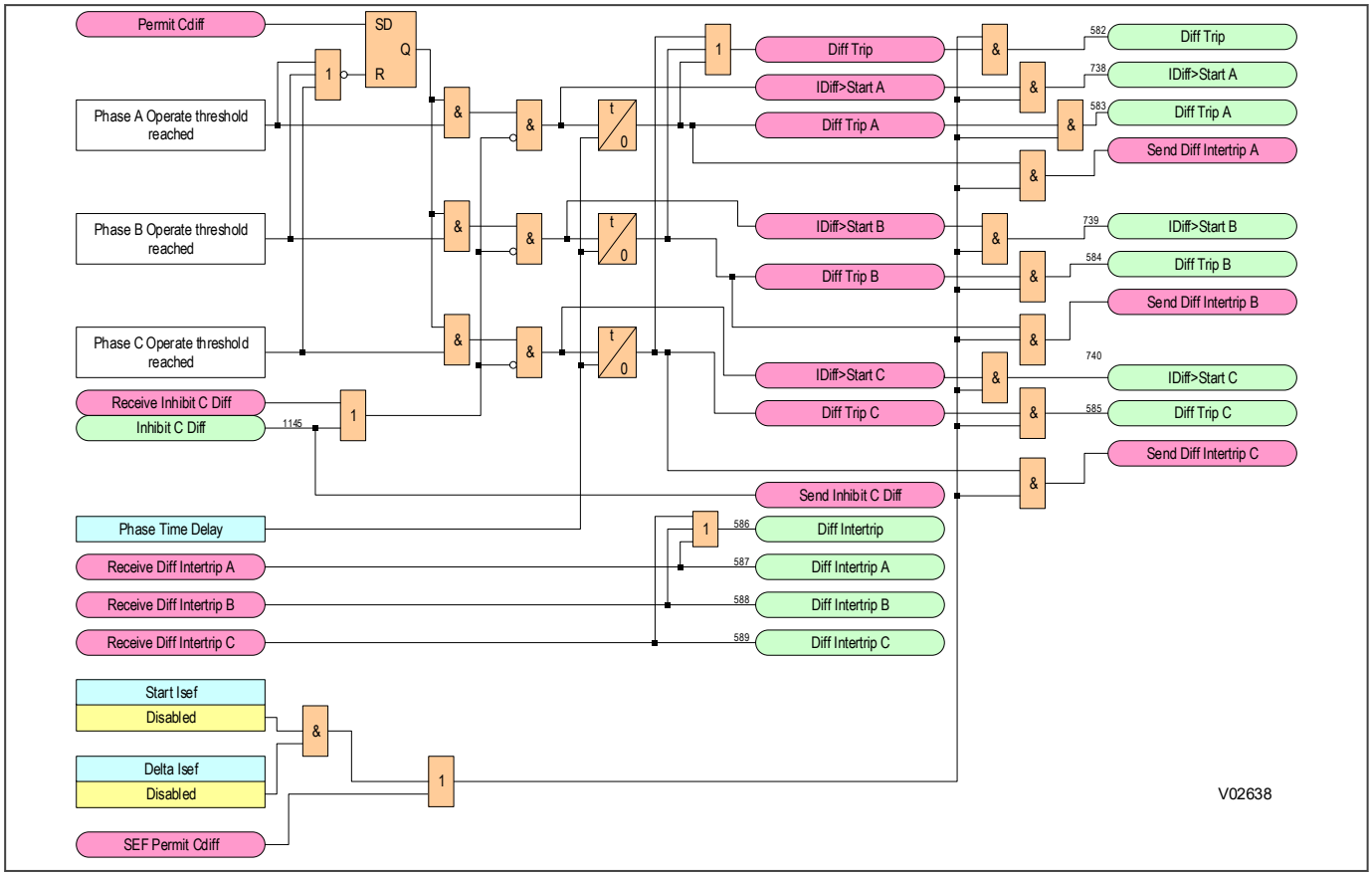


Figure 44: Phase current differential protection logic

7.5 NEUTRAL CURRENT DIFFERENTIAL PROTECTION

Neutral Current Differential protection is provided to clear high-resistive earth faults which may be below the Phase Current Differential sensitivity limit.

If you wish to use the Neutral Current Differential protection you must enable it using the ***In Diff*** setting under the *NEUTRAL DIFF* subheading of the *CURRENT DIFF* column.

The Neutral Current Differential protection can be very sensitive. Before it is allowed to operate, certain criteria must be met:

- The operation of the Neutral Current Differential is time delayed compared with the phase current differential protection to provide discrimination. Operation can be delayed further by setting the ***In Diff Time*** setting. With the ***In Diff Time*** cell set to 0 (instantaneous), the operating time for the Neutral Current Differential element will be at its minimum and typically will range between one-and-a-half and two-and-a-half cycles of power system frequency.
- Operation of the Neutral Current Differential protection is blocked or inhibited for the following cases
    - A Phase Current Differential element has started.
    - A Distance protection element has started.
    - A Current Differential CTS element has operated.
    - A Second Harmonic blocking detector has picked up
    - The device has detected that one or more of the circuit breaker (or isolator) poles are open.
- An External Inhibit condition using an opto-isolator mapped by the PSL is asserted.

The characteristic is determined by three protection settings. You can change the settings, but we strongly recommend retaining the default values, which are as follows:

- ***In Diff Is1*** = 0.1 pu
- ***In Diff Is2*** = 2.0 pu
- ***In Diff k1*** = 10%

This provides stability for small CT mismatches, while ensuring good sensitivity to resistive faults under heavy load conditions.

7.5.1 NEUTRAL CURRENT DIFFERENTIAL CHARACTERISTIC

The Neutral Current Differential characteristic is defined by three settings; ***In Diff IS1***, ***In Diff k1***, ***In Diff Is2***, as shown below:

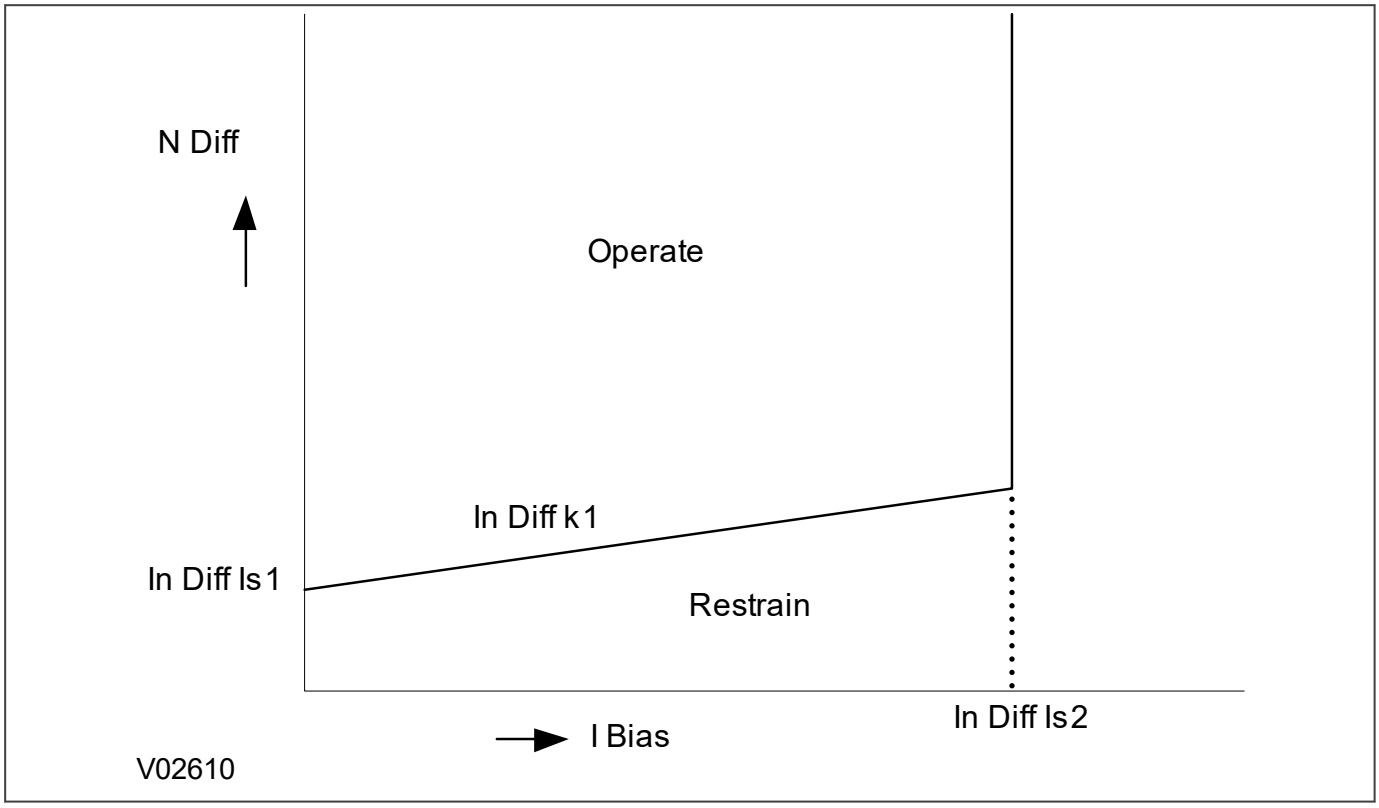


Figure 45: Neutral current differential characteristic

Note:
Ibias is calculated from the phase differential currents.

Neutral current differential calculation

The neutral current used is a derived quantity. Individual local phase current measurements are summed to produce the local neutral current. The individual remote phase current measurements are summed to produce the remote neutral current for each remote terminal in the protection scheme. The neutral differential current is calculated from the sum of the local and remote values. The value is then compared against the characteristic.

7.6 THREE-TERMINAL SCHEMES

Products that have two protection communications channels fitted can be applied to the protection of three-terminal applications.

By appropriate model selection, current differential protection can be provided for two-terminal or three-terminal feeders. A naming convention is used featuring the terms ‘Local’ and ‘Remote’. ‘Local’ is applied to the device being described. ‘Remote’ refers to a connected device. For a two-terminal application, the remote device is referenced in the *MEASUREMENTS 3* column as ‘Remote 1’. When a third terminal is included it is referenced as ‘Remote 2’.

Sometimes what is expected to be a three-terminal scheme may need to operate as a two-terminal scheme (this may be due to a line end being taken out for maintenance, or it may be that the line end has still to be added). In such a case, it is possible to reconfigure the protection devices to perform as a two-terminal application. The device that has been configured-out can be removed from the system without any alarms being raised. This reconfiguration can be done from any of the terminals in the protection scheme, but it is generally performed at the terminal being configured out, as it requires an interlock that is associated with the isolator at that terminal. If you intend to use this feature you might need to create and use customised PSL files and the product must be set up for three-terminal operation.

To reconfigure a scheme from three-terminal to two-terminal you use the ***Re-Configuration*** setting in the *PROT COMMS/IM64* column. Before you can change a configuration, two interlocking criteria need to be satisfied: The ***Inhibit C Diff*** and ***Recon Interlock*** DDB signals (455, 456 respectively) need to be asserted. The ***Inhibit C Diff*** DDB signal is mapped by default to one of the opto-isolated inputs and is used to ensure stability during the reconfiguration. According to the particular model being used, the ***Recon Interlock*** DDB signal might not be mapped by default. To reconfigure a scheme from three-terminal to two-terminal, the DDB signal must be mapped to an opto-isolated input using the PSL. This signal is intended to be connected to reflect the state of the switchgear at the terminal that is being taken out of service (The rationale being that if the line is open, current does not flow and so the scheme can be protected as a two-terminal line).

> *Note:*
> *The line end to be ‘configured out’ must be open before issuing a reconfiguration command. If this is not done, any current flowing in or out of the ‘configured out’ end will be seen as fault current and when the* ***Inhibit C Diff’****input is removed, it might cause the other devices to operate.*

Reconfiguration is only permitted if all three devices are energised and communicating correctly with each other.

Four values are available for the ***Re-Configuration*** setting:

- ***Three Ended*** (stay as three-ended)
- ***Two Ended(L&R1)*** (Local + Remote 1)
- ***Two Ended(L&R2)*** (Local + Remote 2)
- ***Two Ended(R1&R2)*** (Remote 1 + Remote 2)

If the reconfigured scheme incorporates the local device, the trip outputs of the differential protection will continue to be inhibited until the ***Inhibit C Diff*** signal at the local device is cleared. If the new reconfiguration scheme only incorporates the remote devices, the differential protection at the remote devices are not inhibited because they will ignore all commands from the local device unless it is a command for reconfiguration.

Setting the ***Re-Configuration*** setting to `Three Ended` at any terminal will restore three-terminal operation without regard to the status of the ***Inhibit C Diff*** DDB signal or the ***Recon Interlock*** DDB signal.

The operation of the change configuration logic is as follows:

- The reconfiguration setting is changed.
- The product detects the change in setting and attempts to implement the new setting.

If the current configuration is Two-Ended and the new setting is also Two-Ended, the device blocks the change and issues a configuration error alarm.

If the current configuration is Two-Ended and the new setting is Three-Ended, the device checks that all the communications are healthy and sends out the restore command to the other devices. It then checks that the scheme has stabilised as 'Three-Ended' after one second.

If any of the communications in the scheme were failed or if the scheme has not stabilised as Three-Ended, the device returns to its original Two-Ended setting and issues a configuration error alarm.

If the scheme stabilises as Three-Ended, the Reconfiguration setting is updated.

If the device configuration is Three-Ended and the new setting is Two-Ended L & R1, the device first checks that the two interlocks are energised. The differential tripping is blocked, but the backup protection can still operate the trip outputs. The device then checks that the communication with Remote 1 is healthy and sends out the command to the remote devices. It then checks that the scheme has stabilised as Two-Ended L & R1 after one second.

If the interlocks are not energised, or the communication with Remote 1 has failed, or the scheme does not stabilise as Two-Ended L & R1, the device returns to Three-Ended and issues a configuration error alarm.

If the scheme stabilises as Two-Ended L & R1, the Reconfiguration setting is updated.

If the device configuration is Three-Ended and the new setting is Two-Ended L & R2, the device reacts similarly to a Two-Ended L & R1 reconfiguration.

If the device configuration is Three-Ended and the new setting is Two-Ended R1&R2, the device reacts similarly to a Two-Ended L & R1 reconfiguration.

7.6.1 COMMUNICATION PATH FAILURE

Full line protection is provided even if one communications path should fail . For instance, in the figure below, if the A-B channel fails, C still offers line protection and will Intertrip to A and B in the event of a fault.

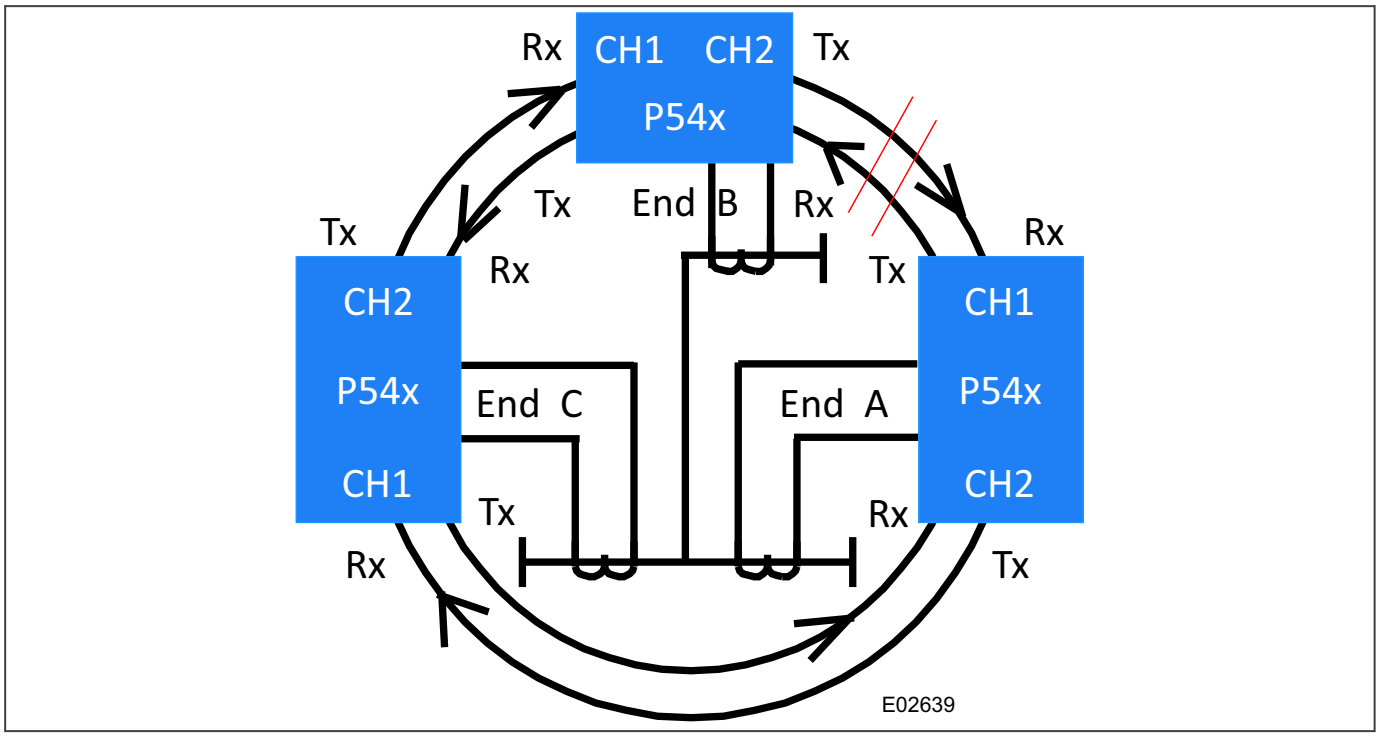


Figure 46: Line differential communications path--three-ended showing fail

7.6.2 THREE-TERMINAL SCHEME RECONFIGURATION ON ENERGISATION

This occurs when a device is energised and it tries to configure itself to be compatible with other devices in the scheme. The scheme tries to maintain the configuration set by the user. However, there are certain conditions that may prevent this from happening:

When powered on the device configuration depends on the following factors:

- The scheme currently configured on the remote devices
- The status of the communication links
- The configuration stored in non-volatile memory before power down

When the device is energised, the following events occur:

- The device checks whether any messages are being received. If so, then the configuration commands in the first messages to arrive are used to configure the device. This is subject to certain conditions. If the device receives a Two-Ended configuration instruction from one end and a Three-Ended configuration instruction from the other end, it uses the Two-Ended instruction. If both incoming commands are Three-Ended, the scheme stabilses as three-ended.
- If no messages arrive from either end, after one second the device assumes the configuration it had before power down. Once messages begin to arrive again, the device checks them for validity against the current scheme. If one device is Three-Ended and the other is Two-Ended, the configuration changes to Two-Ended. If both are Three-Ended or both are the same Two-Ended scheme, that scheme becomes the configuration. If two devices have different Two-Ended configurations, they are unable to determine which one to use and each generates a configuration error alarm and each device remains in its current configuration. This condition can be cleared by restoring the devices or by removing the supply to the device with the incorrect configuration.
- If all the devices in a scheme are energised simultaneously, the configuration reverts to Three-Ended if all the communication channels are healthy. This occurs because all the devices are waiting to be told their configuration and all default to Three-Ended. This is a very unlikely event in normal use.

If a communication channel has only half failed (for example, the receive channel has failed but not the transmit channel), there may be configuration errors on power up because the devices are not communicating correctly. If the status is available from the third device and communications are healthy using its two channels, the scheme stabilises correctly.

7.7 TRANSIENT BIAS

Phase current differential protection stability for current transformers is assisted by a feature called ***Transient Bias***. This can be enabled or disabled with the transient Bias setting in the *CURRENT DIFF* column.

Saturation of current transformers (CTs) under heavy load or external fault conditions can cause the protection to see differential current and could lead to tripping. Preventing CT saturation can impose high specifications and high costs for the CTs. The Transient Bias feature allows the CT requirements to be relaxed – typically by 25%.

The Transient Bias feature recognises the changes in bias and differential currents under different conditions and reacts as follows:

- For an internal fault, bias and differential currents start to increase together. For an external condition, bias current will start to rise, but differential current will not. If CT saturation starts to occur for an external condition, the differential current starts to increase after the bias current has increased.
- Detecting the relative changes in the bias and differential currents allows the device to detect whether the differential current is due to an internal fault or due to an external condition causing CT saturation. For external conditions, the biasing quantity is raised, transiently, to provide stability. For internal faults, sensitivity is maintained.

7.8 CAPACITIVE CHARGING CURRENT COMPENSATION

All electrical conductors, including feeders, are capacitively coupled to earth. When energised, a capacitive current flows from the feeder to earth to charge the capacitance. The capacitance is distributed along the feeder, but for analysis it can be modelled according with the following figure.

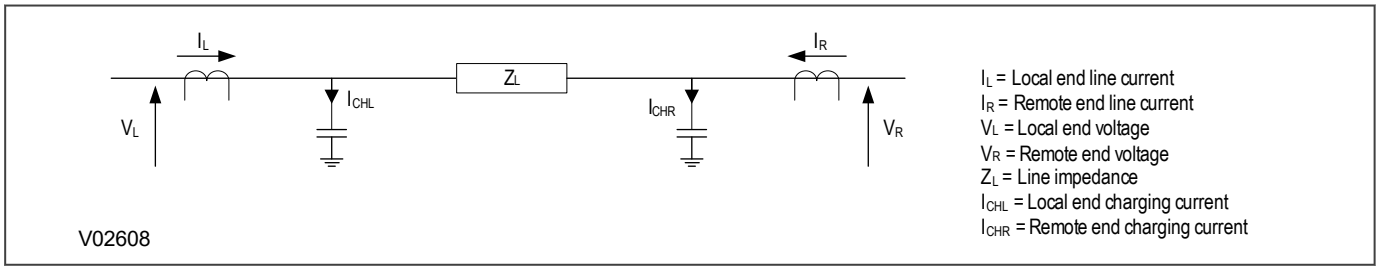


Figure 47: Capacitive charging current

Both transient capacitive and steady-state capacitive charging currents exist. Transient inrush charging current consists of predominately high-order harmonics, which are filtered out by the device. However, steady state AC charging currents flow all the time that the feeder remains energised. This capacitive charging current appears as a differential current. On long overhead lines, and on cable circuits, this capacitive charging current can be sufficiently high to cause current differential elements to trip under healthy conditions and therefore needs to be compensated.

To prevent maloperation due to capacitive charging currents, ***Phase Is1*** would normally be set to at least 2.5 times the charging current. This, however, reduces the sensitivity of the differential protection. If voltage input connections are made, more effective compensation for capacitive charging current can be applied:

Using the voltage inputs and the line positive-sequence capacitive susceptance, the devices can calculate the charging currents. These can then be taken into account before calculating the differential currents.

Referring to the figure above, we see that the line charging current at a particular location is equal to the voltage at that location multiplied by the line positive sequence capacitive susceptance (Bs). The differential current is therefore:

$$I_{diff} = I_L + I_R - (jV_{LBs}/2) - (jV_{RBs}/2) = \{I_L - (jV_{LBs}/2)\} + \{I_R - (jV_{RBs}/2)\}$$

The two terms in this equation represent one component that can be calculated at a local terminal and another that can be calculated at a remote terminal. Using these values, rather than the actual phase current measurements, will eliminate the effects caused by capacitive charging currents. So, for long line or cable applications, if voltage transformers are connected, capacitive charging current compensation can be applied. This is achieved by setting the ***Compensation*** setting in the *CURRENT DIFF* column to `Cap Charging`. This will make visible a ***Susceptance*** setting into which the line positive sequence capacitive susceptance value can be entereed.

When applied to a three-ended scheme with ends local (L), remote 1 (R1) and remote 2 (R2), the differential current is calculated as:

$$I_{diff} = I_L + I_{R1} + I_{R2} - (jV_{L\,Bs}/3) - (jV_{R1Bs}/3) - (jVR_{2Bs}/3) = \{I_L - (jV_{LBs}/3)\} + \{I_{R1} - (jV_{R1Bs}/3)\} + \{I_{R2} - (jV_{R2Bs}/3)\}$$

If the capacitive charging compensation is enabled, the current measurements in the *MEASUREMENTS 3* column display the compensated values.

7.9 CT COMPENSATION

The current differential protection provided by this product requires that the phase input currents at each terminal in the scheme are correctly measured, combined, and compared. Status of the protection is provided through internally and externally presented logic signals to indicate phase-tripping, etc. Further monitoring of the current differential protection function can be obtained through the devices measurement functions which can display the various measured and calculated current signals used within the current differential protection. Measured values may be presented in either primary or secondary values according to user preference, but the differential protection needs to use rationalised values to balance the equations. Typically, converting all currents used by a differential algorithm to per-unit (p.u.) values will achieve this. Some current differential devices are capable of protecting circuits that include additional transformers associated with the protected terminals. Where this is the case, any differences between the primary and secondary windings of these transformers will need to be compensated too. In these cases, the protection algorithms may use per-unit values which are internally compensated to account for the transformer winding mis-matches.

The primary and secondary ratios for the phase current transformers for each terminal in the scheme are set in the *CT AND VT RATIOS* column of the settings for that particular device. These settings are used to display the phase current quantities in the *MEASUREMENTS 1* column. The device can be set to display the input current either in primary values or in secondary values.

To ensure correct operation of the differential elements, it is important that under load and through fault conditions, the currents into the differential elements of the devices balance. If the CTs have different ratios this will not be the case. This product has CT ratio correction (magnitude compensation) to overcome this problem.

When calculating differential and bias current, the devices use a per-unit (p.u.) approach. Ordinarily this might be achieved by direct association with the CT secondary, but in cases where ratio matching is needed to account for additional transformers in the scheme, the per-unit values are compensated to accommodate the effect of the additional CT ratios. This compensation is applied to the current signals by upscaling them to match equivalently compensated currents from the remote terminals. The compensation is applied by setting an appropriate value in the ***Ph CT Corr'tion*** setting in the *CURRENT DIFF* column of the local device. Because of dynamic limitations, this scaled-up value is limited to 40 p.u. Values exceeding this are clipped at 40 p.u.

Similarly compensated per-unit values are used in the calculation of the differential and bias currents.

For display purposes the values presented via the *MEASUREMENTS 3* column are derived from per unit compensated values. The per-unit compensated values of local remote differential and bias currents are scaled-down by the local CT ratio correction factor, as well as being scaled by the primary or secondary rating (as appropriate) before being displayed in the *MEASUREMENTS 3* column.

The process is outlined in the following figure in which *I*' indicates a compensated per-unit value:

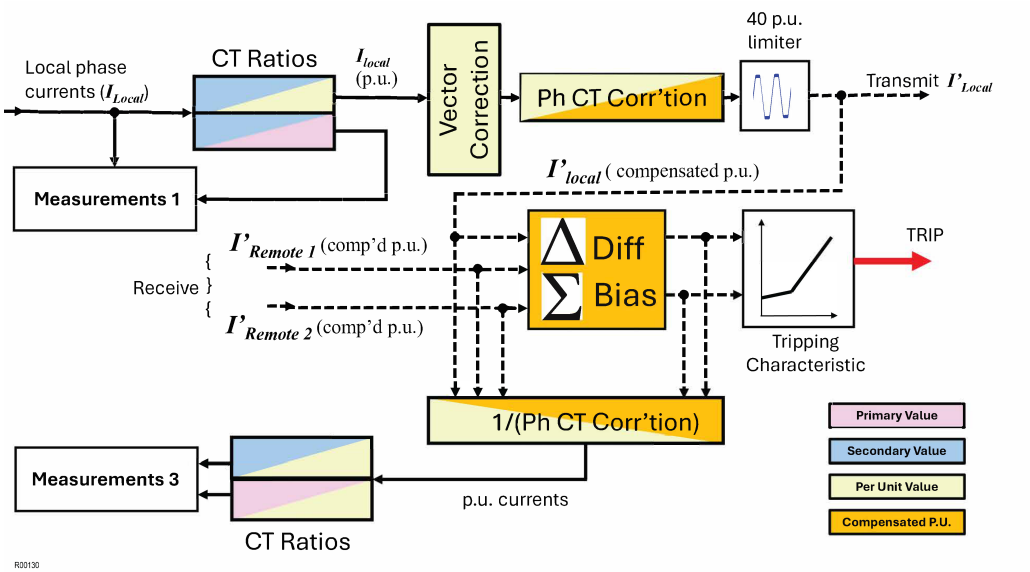


Figure 48: CT compensation with vector compensation

For products connected to two sets of current transformers with different CT ratios, then CT1 input is used as a reference. The product scales CT2 currents based on the PhaseCT1 Primary and PhaseCT2 Primary settings. So, only CT1 rated current should be considered when applying CT ratio correction.

7.10 FEEDERS WITH IN-ZONE TRANSFORMERS

A transformer feeder comprises a transformer directly connected to a transmission circuit without the intervention of switchgear. Although separate current transformer inputs may be available to allow separate overlapping zones of protection for the transformer and the feeder this is not always the case and the transformer and the feeder must be treated and protected as a single item of plant for protection. The integration of in-zone power transformers into unit feeders causes further complications for current differential protection:

- Phase shift and possible imbalance of signals across the transformer
- Transfer of earth fault current by the transformer
- Magnetising Inrush current
- Overfluxing

This (P543) product therefore provides facilities to deal with the above issues by providing:

- CT compensation for phase shifts and imbalances across the transformer
- Zero sequence compensation.
- Magnetising Inrush detection and restraint
- Second harmonic blocking.
- Overfluxing detection and restraint
- Fifth harmonic blocking.

To make these available you need to enable the differential protection for an in-zone power transformer. This is done on a per-setting group basis. The phase differential element (***Phase Diff***) for the setting group concerned must be enabled.

To enable the transformer feeder protection you set the ***Compensation*** cell in the *CURRENT DIFF* settings to ***Transformer*** (P543).

7.10.1 VECTOR GROUP COMPENSATION

To compensate for any phase shift between two windings of a transformer, it is necessary to provide correction. This is provided by specifying the vector group using the ***Vectorial comp*** setting in the *CURRENT DIFF* column.

The options are listed in the table below:

Setting	Phase Shift	Action
Yy0	0	Do nothing
Yd1	30 lag	Ia = (IA - IC)/√3 Ib = (IB - IA)/√3 Ic = (IC - IB)/√3
Yy2	60 lag	Ia = -IC Ib = -IA Ic = -IB
Yd3	90 lag	Ia = (IB - IC)/√3 Ib = (IC - IA)/√3 Ic = (IA - IB)/√3
Yy4	120 lag	Ia = IB Ib = IC Ic = IA
Yd5	150 lag	Yd11 and Invert
Yy6	180 lag	Invert currents
Yd7	150 lead	Yd1 and Invert

Setting	Phase Shift	Action
Yy8	120 lead	Ia = IC Ib = IA Ic = IB
Yd9	90 lead	Yd3 and Invert
Yy10	60 lead	Ia = -IB Ib = -IC Ic = -IA
Yd11	30 lead	Ia = (IA - IB)/√3 Ib = (IB - IC)/√3 Ic = (IC - IA)/√3
Ydy0	0	Ia = IA - (IA + IB + IC)/3 Ib = IB - (IA + IB + IC)/3 Ic = IC - (IA + IB + IC)/3
Ydy6	180 lag	Ydy0 and Invert

Where Ia, Ib, Ic are the uncorrected values and IA, IB, IC are the corrected values.

Note:
*You must set Compensation to **Transformer** before the **Vectorial Comp** setting becomes visible.*

7.10.2 ZERO SEQUENCE FILTERING

In addition to compensating for the phase shift of the protected transformer, it is also necessary to mimic the distribution of primary zero sequence current in the protection scheme. The figure below shows the need for zero sequence current filtering for differential protection across a transformer. The power transformer delta winding acts as a 'trap' to zero sequence current. This current is only seen on the star connection side of the transformer and therefore as differential current.

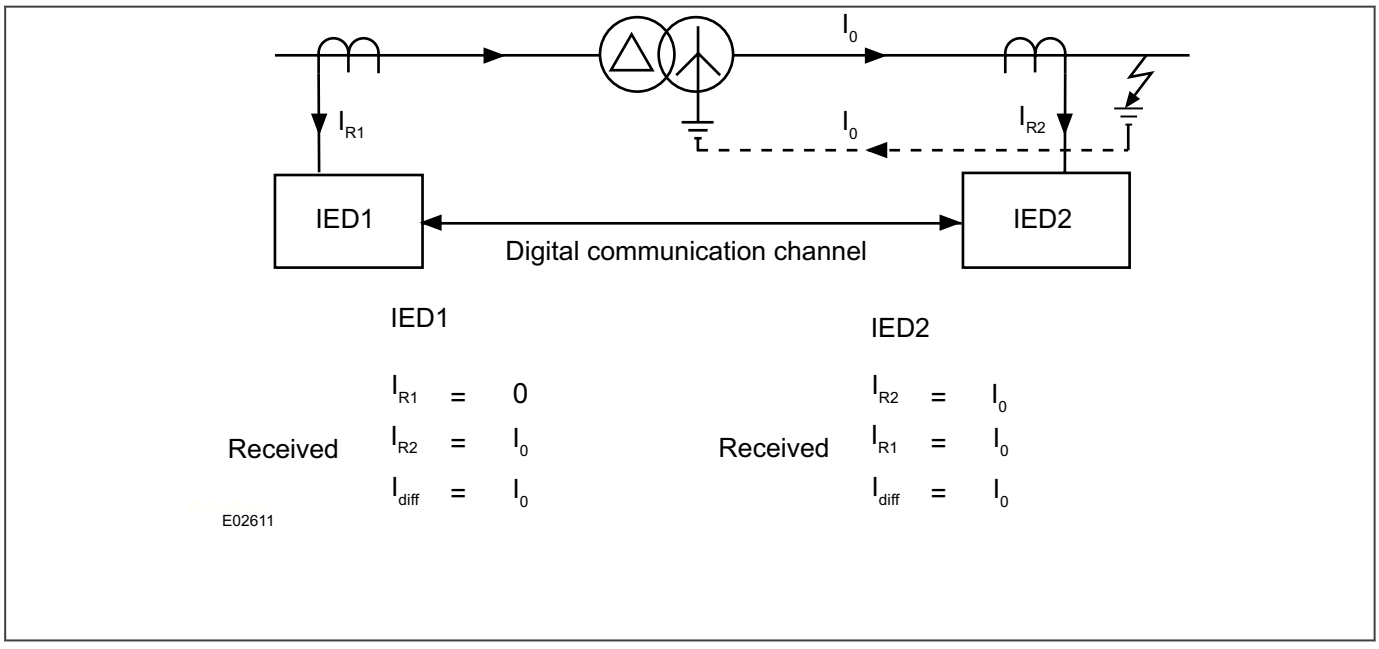


Figure 49: The need for zero-sequence current filtering

Where a transformer winding can pass zero sequence current to an external earth fault, it is essential that some form of zero sequence current filtering is used. This would also be applicable where in zone earthing transformers

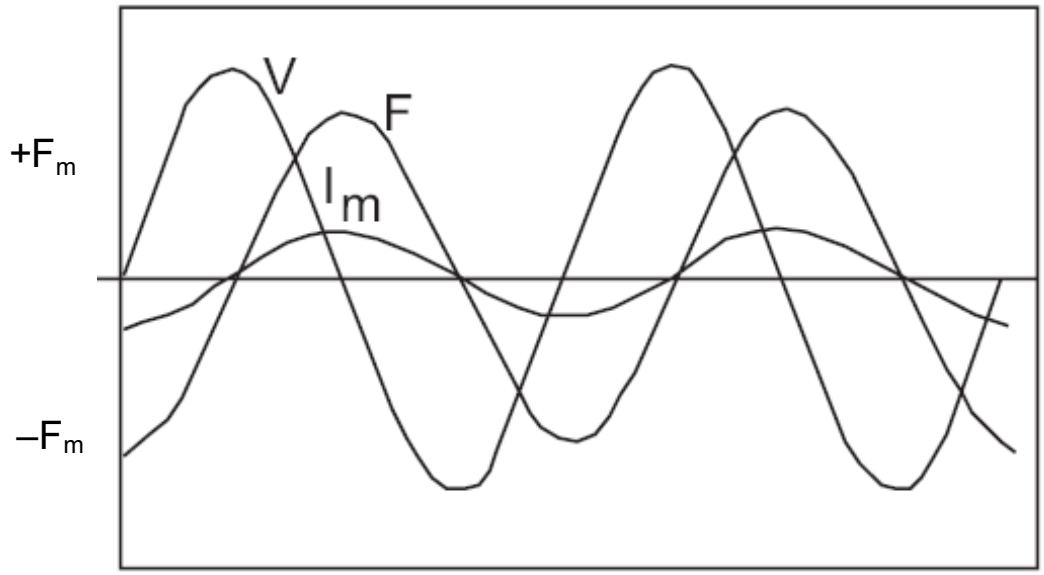
are used. In this product, zero sequence current filtering is automatically implemented in software when a delta connection is set for the vector compensation.

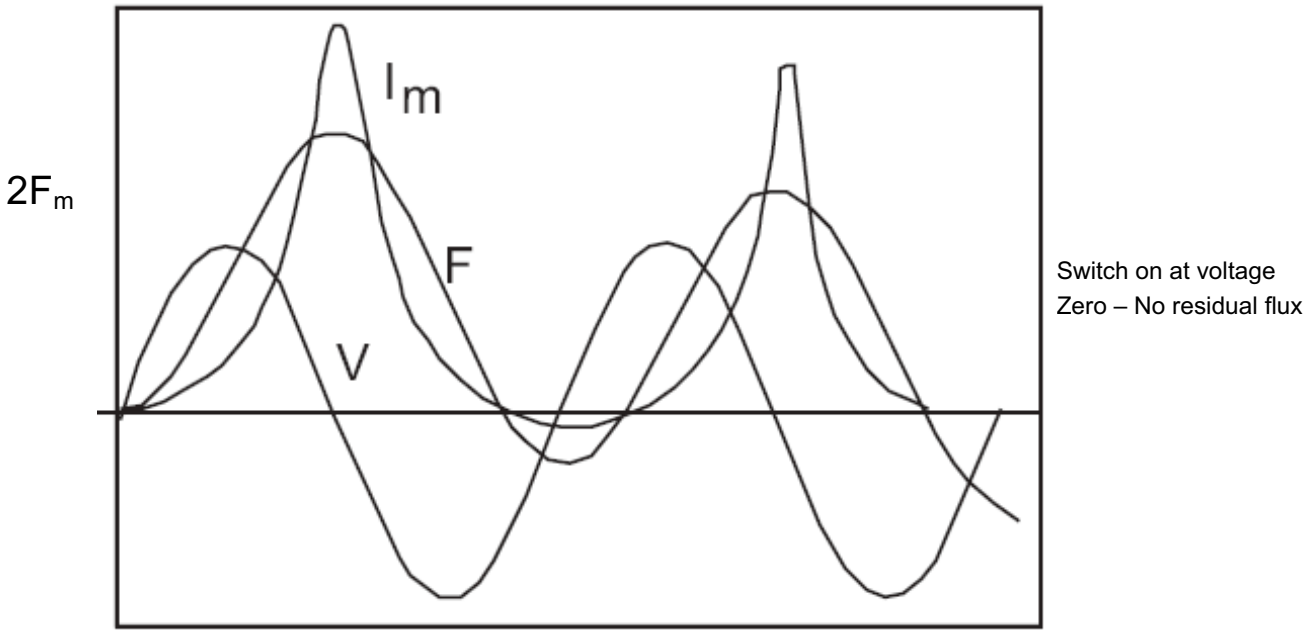
7.10.3 MAGNETISING INRUSH RESTRAINT

Whenever there is an abrupt change of magnetising voltage (e.g. when a transformer is initially connected to a source of AC voltage), there may be a substantial surge of current through the primary winding called inrush current.

In an ideal transformer, the magnetising current would rise to approximately twice its normal peak value as well, generating the necessary MMF to create this higher-than-normal flux. However, most transformers are not designed with enough of a margin between normal flux peaks and the saturation limits to avoid saturating in a condition like this, and so the core will almost certainly saturate during this first half-cycle of voltage. During saturation, disproportionate amounts of MMF are needed to generate magnetic flux. This means that winding current, which creates the MMF to cause flux in the core, could rise to a value way in excess of its steady state peak value. Furthermore, if the transformer happens to have some residual magnetism in its core at the moment of connection to the source, the problem could be further exacerbated.

The following figure shows the magnetising inrush phenomenon:





V = Voltage, F = Flux, Im = magnetising current, Fm = maximum flux

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Figure 50: Magnetising inrush phenomenon

The main characteristics of magnetising inrush currents are:

- Higher magnitude than the transformer rated current magnitude
- Containing harmonics and DC offset
- Much longer time constant than that of the DC offset component of fault current

We can see that inrush current is a regularly occurring phenomenon and should not be considered a fault, as we do not wish the protection device to issue a trip command whenever a transformer is switched on at an inconvenient point during the input voltage cycle. This presents a problem to the protection device, because it should always trip

on an internal fault. The problem is that typical internal transformer faults may produce overcurrents which are not necessarily greater than the inrush current. Furthermore, faults tend to manifest themselves on switch on, due to the high inrush currents. For this reason, we need to find a mechanism that can distinguish between fault current and inrush current. Fortunately, this is possible due to the different natures of the respective currents. An inrush current waveform is rich in harmonics, especially 2nd harmonics, whereas an internal fault current consists only of the fundamental. We can therefore develop a restraining method based on the 2nd harmonic content of the inrush current. The mechanism by which this is achieved, is called second harmonic blocking.

7.10.3.1 SECOND HARMONIC RESTRAINT

When set to protect feeders with in-zone transformers, this product measures the second harmonic components of the input currents to detect magnetising inrush, which can be used to modify operation of the current differential protection.

Using the Inrush Restraint setting you can choose what will happen to differential characteristic in the presence of second harmonic current:

- If set to `Disabled`, the characteristic will not be modified,
- If set to `Restraint`, the characteristic will be restrained if the second harmonic component is above a user set threshold.
- If set to `Blocking`, the protection will be blocked

The `Restraint` and `Blocking` modes are qualified by other settings outlined below. In both cases an unbiased high-set current differential element becomes visible.

Note:
*You must set **Compensation** to `Transformer` before the **Inrush Restraint** setting becomes visible.*

Note:
*When used, the **Inrush Restraint** function must be enabled at all ends to avoid possible maloperation.*

Note:
*There is an **Inrush Detection** setting in the SUPERVISION column of the menu. The **Inrush Detection** setting is only visible if the Inrush Blocking'in the CURRENT DIFF column is not being used. The function asserts the same DDB outputs as **Inrush Restraint** and can be used to control other protection elements during magnetising inrush conditions. The output of **Inrush Detection** does not, however, affect the Current Differential protection.*

7.10.3.1.1 SECOND HARMONIC RESTRAINT

If the ***Inrush Restraint*** setting is set to `Restraint`, then a percentage of the second harmonic component of the input signal is added to the bias quantity used in the current differential characteristic.

The amount of additional bias to be added into the calculation is defined by the following expression:

$$\text{Additional bias} = \textbf{\textit{Ih(2) Multiplier}} * 1.414 * \text{largest 2nd harmonic current}$$

You can set ***Ih(2) Multiplier*** between 1 and 20 according to your application.

Note:
*Where **Inrush Restraint** is used to restrain operation, it must be used at all terminals in the scheme to avoid possible maloperation.*

7.10.3.1.2 SECOND HARMONIC BLOCKING

If the ***Inrush Restraint*** setting is set to `Blocking`, then the operation of the current differential elements will be blocked if magnetising inrush is detected.

Magnetising inrush is considered to be present if the level of phase current is above 5% In AND the ratio of harmonic to fundamental in that phase exceeds the ***Ih(2) %>*** value which you set.

Detection of magnetising inrush forces a phase block signal to block local and remote ends.

You can choose whether to block just the affected phase, or to block all three phases using the ***Ih(2) CrossBlock*** cell. If you disable ***Ih(2) CrossBlock***, only the affected phase is blocked. If you enable ***Ih(2) CrossBlock***, all phases are blocked.

7.10.3.1.3 HIGH SET DIFFERENTIAL

It is possible for current transformers (CTs) to saturate under heavy internal fault conditions. CT saturation, like magnetising inrush, is characterised by significant second harmonic components. The protection is required to remain stable for magnetising inrush conditions, but to operate for internal faults. To discriminate between the two, an unrestrained high set differential protection is included. If ***Inrush Restraint*** is set either to `Restraint` or to `Blocking`, an unrestrained high set differential protection becomes visible. It is provided to ensure rapid clearance for heavy internal faults with saturated CTs. The element can be enabled or disabled according to the ***HighSet Status*** setting in the *CURRENT DIFF* column. The pick-up value can be set between 4 In and 32 In (RMS values) using the ***Id High Set*** cell.

> *Note:*
> *The **Id High Set** cell should be set so that it is in excess of the anticipated inrush current after ratio correction has been applied.*

7.10.4 OVERFLUXING RESTRAINT

Sometimes the protected transformer is subject to overfluxing due to temporary overloading with a voltage in excess of the nominal voltage, or a reduced voltage frequency. For example, when a load is suddenly disconnected from a power transformer, the voltage at the input terminals of the transformer may rise by 10-20% of the rated value. Since the voltage increases, the flux also increases. As a result, the transformer steady state excitation current becomes higher. The resulting excitation current flows in one winding only and therefore appears as differential current which may rise to a value high enough to operate the differential protection. A typical differential current waveform during such a condition is as follows.

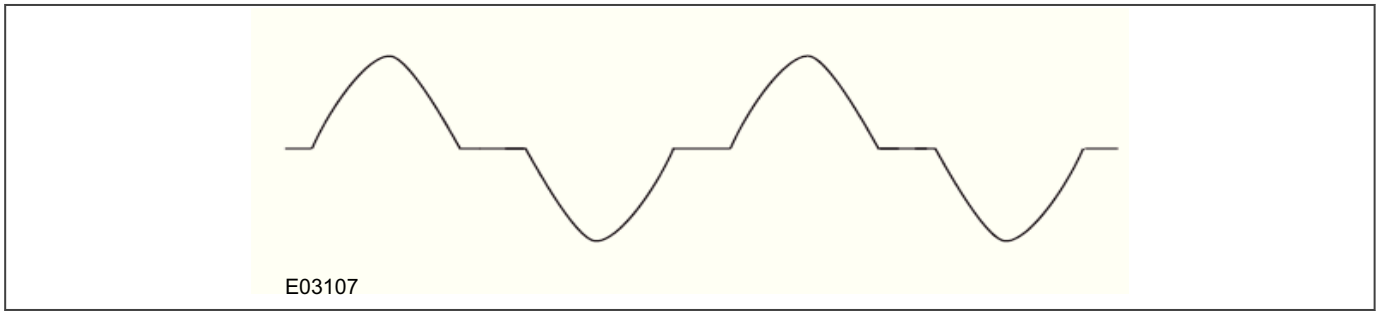


Figure 51: Typical overflux current waveform

Such waveforms have a significant 5th harmonic content. We can therefore develop a restraining method based on the 5th harmonic content of the inrush current. The mechanism by which this is achieved, is called fifth harmonic blocking.

7.10.4.1 FIFTH HARMONIC BLOCKING

A characteristic of overfluxing is that there is a strong fifth harmonic component associated.

When applied to the protection of transformer feeders, this product measures the fifth harmonic components of the input currents to detect overfluxing. This detection can be used to block operation of the current differential protection.

If the 5th Harmonic setting is enabled, then the operation of the current differential elements will be blocked if overfluxing is detected.

Overfluxing blocking is implemented on a phase-by-phase basis. Blocking is prevented if the phase current is less than 5% In. If the phase current exceeds 5% In, and the element is enabled, then if the ratio of fifth harmonic current to the fundamental component exceeds the the ***Ih(5) %>*** setting, operation of the current differential is blocked on that phase. Blocking of affected phases is applied both at local and at remote terminals.

You can choose whether to block just the affected phase, or to block all three phases using the ***Ih(5) CrossBlock*** cell. If you disable ***Ih(5) CrossBlock***, only the affected phase is blocked. If you enable ***Ih(5) CrossBlock***, all phases are blocked.

For products connected to two sets of current transformers with different CT ratios, then CT1 input is used as a reference. The product scales CT2 currents based on the PhaseCT1 Primary and PhaseCT2 Primary settings. So, only CT1 rated current should be considered when applying CT ratio correction.

7.11 LOGIC FOR FEEDERS WITH IN-ZONE TRANSFORMERS

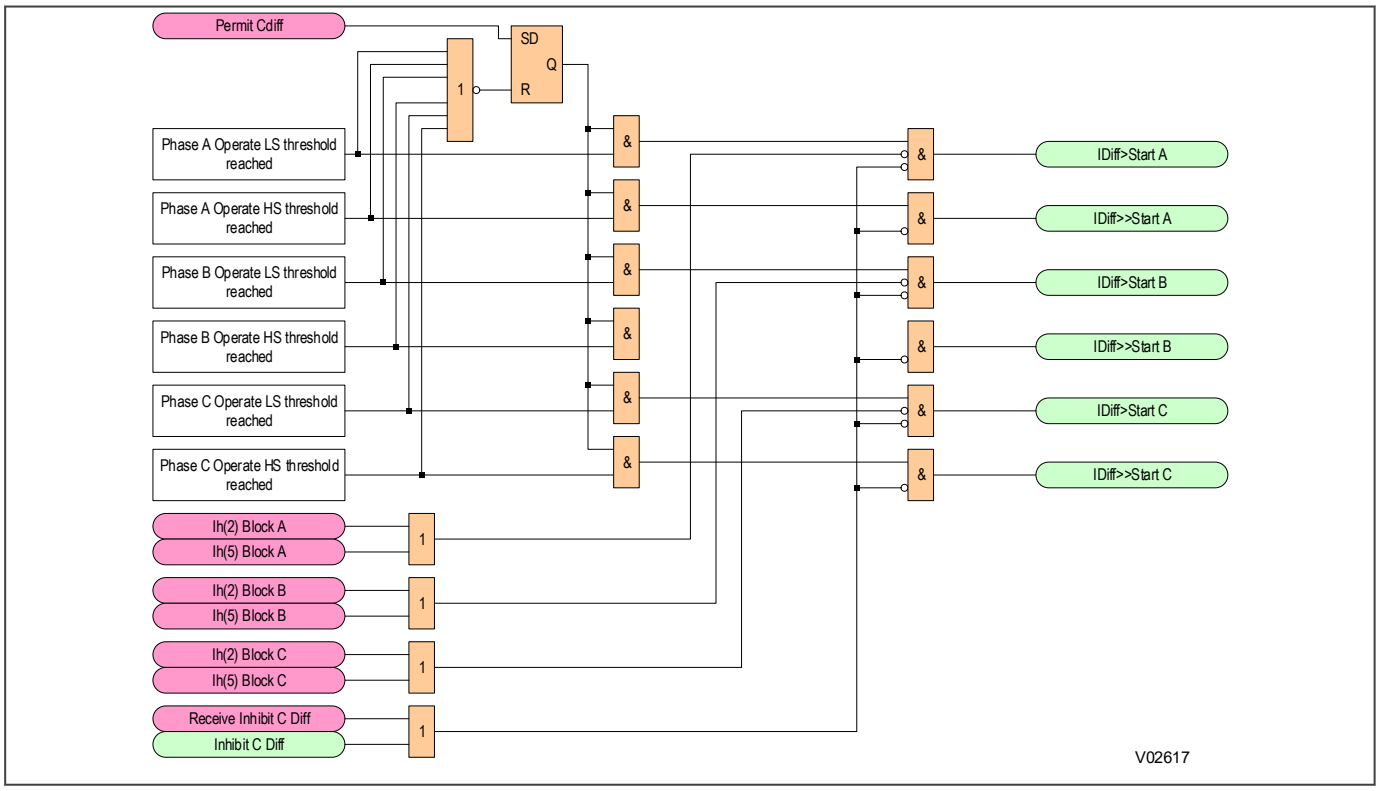


Figure 52: Phase current differential protection logic for feeders with in-zone transformers

7.12 SECOND HARMONIC BLOCKING LOGIC

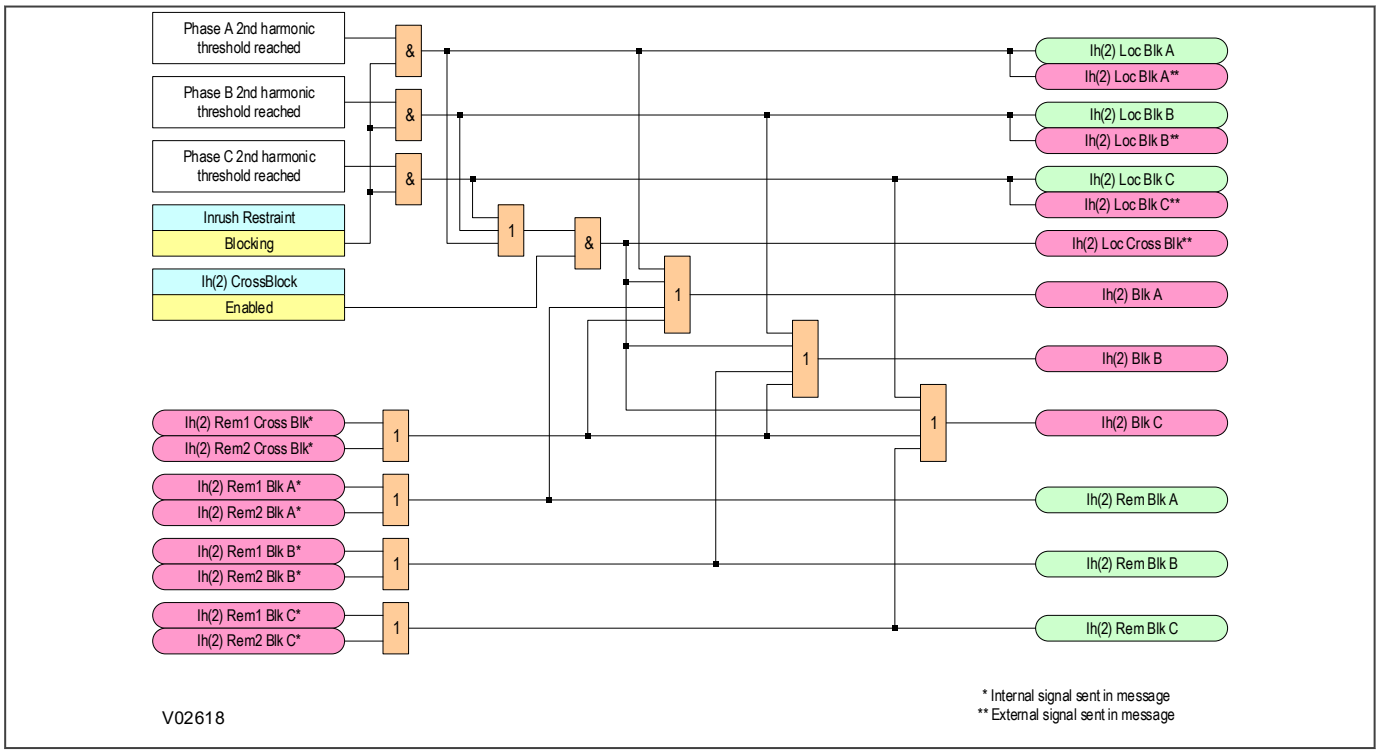


Figure 53: Second harmonic blocking logic

7.13 FIFTH HARMONIC BLOCKING LOGIC

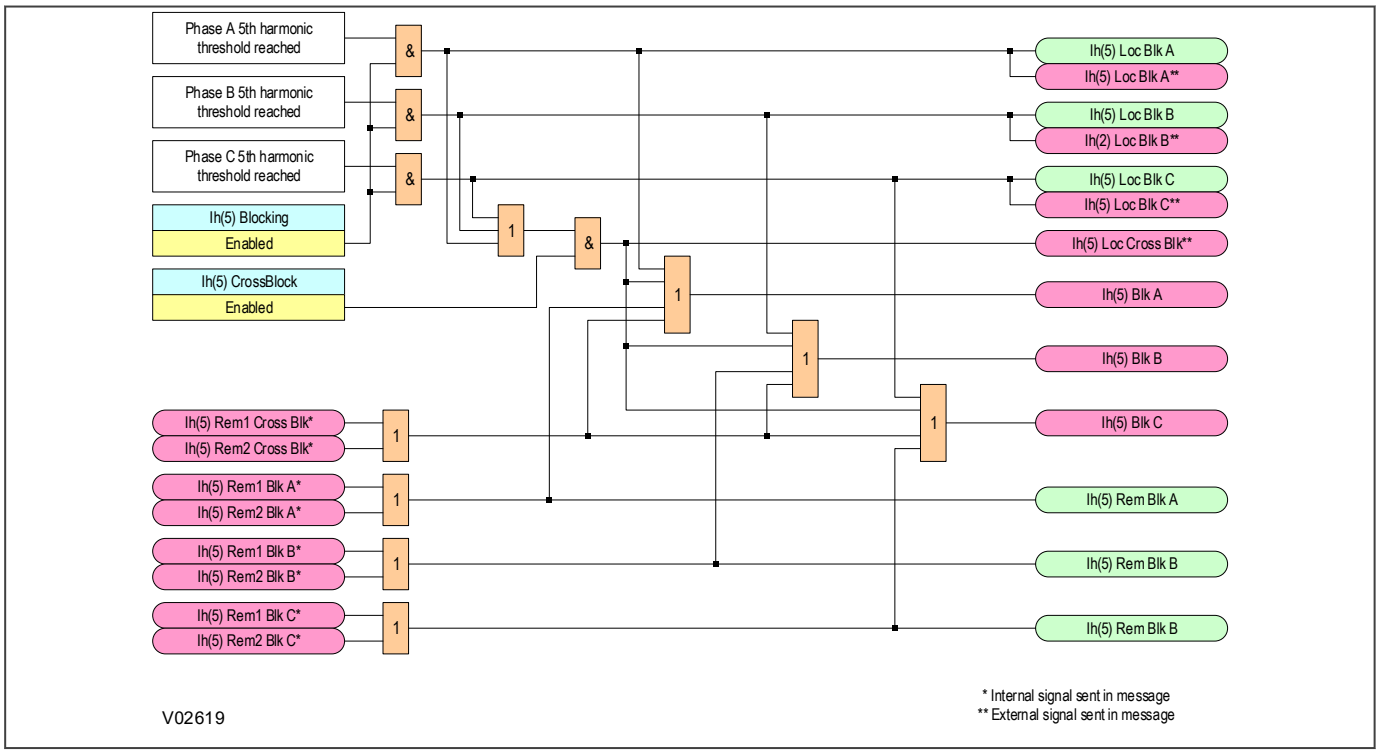


Figure 54: Fifth harmonic blocking logic

7.14 CURRENT DIFFERENTIAL INTERTRIPPING

Eight to 32 freely assignable intertripping signals are provided by a facility called InterMICOM64, which is described in the chapter on Fibre Teleprotection. In addition there are two intertripping functions associated directly with the Current Differential protection. Both are operational when the phase current differential is enabled:

The first is a differential intertripping function whereby if one terminal sees a differential fault, as well as issuing a local trip command it will also send a command to trip to remote terminals to ensure that the fault is isolated at all terminals.

The second is a permissive intertripping function. A Permissive Intertripping function (PIT) is associated with the current differential protection and is visible and active if the phase current differential protection is enabled.

Note:
The term "permissive intertripping" associated with this current differential protection is not the same as that commonly used in teleprotection schemes. It is specific to this type of Current Differential protection implementation.

A device can be configured to send a permissive intertrip command over the protection communication channel. To use this function you need to map the ***Perm Intertrip*** DDB signal to one of the opto-inputs using the PSL.

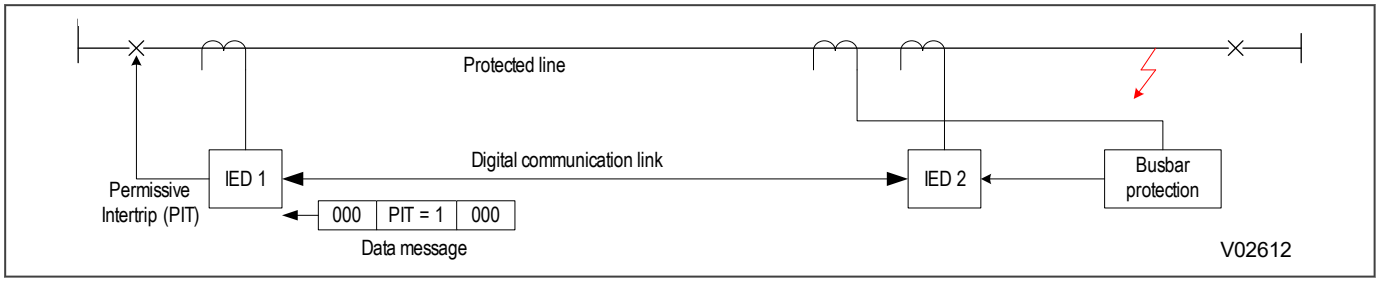


Figure 55: Permissive intertripping example

Consider the above diagram. If a fault occurs as shown, it will be seen by the busbar protection which can trip its local circuit breaker. The fault will not be seen by the differential protection, however, so the fault will continue to be fed. An input signal from the busbar protection at the faulted end can be sent as a permissive intertrip (PIT) command to a remote terminal to cause it to permissively trip the remote circuit breaker to clear the fault.

Tripping occurs if the current remains above the ***Phase Is1*** setting of the phase current differential elements while the PIT command is received. The condition must remain satisfied for a minimum time setting. The time is set in the ***PIT Time*** setting in the *CURRENT DIFF* column. The permissive intertrip (PIT) timer can be set between 0 and 200 ms. This time should be set to provide discrimination with other protection devices. For example, if there is a genuine busbar fault, the time delay should be set to allow busbar protection to clear the fault. A typical setting may be 100 to 150 ms.

You can choose whether to use the local current value sent with the PIT command to make the decision at the remote end, or whether to use the remote current value at the receiving end for the decision. This choice is made using the ***PIT I selection*** setting in the *CURRENT DIFF* column.

Note:
The permissive intertripping function always trips three-phase.

7.15 MESH CORNER AND BREAKER-AND-A-HALF SCHEMES

Where a line is fed from a mesh corner or 1½ breaker switched substation, two options are available for CT connections to the device. The first is by paralleling the two sets of line CTs into a common input. The second is by using devices with two separate sets of three-phase CT. The second option provides more stable protection and the setting can be made more sensitive.

Products are available with two sets of three-phase current inputs (CT1 and CT2). Where a line is fed from a mesh corner or 1½ breaker switched substation, two options are available for CT connections to the device. One (available on all products) is by paralleling the two sets of line CTs into a common input. The second is by using devices with two separate sets of three-phase CT. The two sets of CT inputs provide independent current measurements for use in the differential current calculations. This second option can be set to be more sensitive and provides more stability. It is ideally suited to protect mesh-corner or breaker-and-a-half switched substation applications and is therefore preferred.

If a terminal in the scheme has just a single set of CT inputs, products can be mixed and matched to suit the application as shown in the following diagram:

Products with two sets of three-phase current inputs are ideally suited to protect mesh-corner or 1½ breaker switched substation applications. The two sets of CT inputs at the mesh-corner or switched substation provide current measurement that can be used in the differential current calculations. If a terminal in the scheme has just a single set of CT inputs, products can be mixed and matched to suit the application as shown in the following diagram:

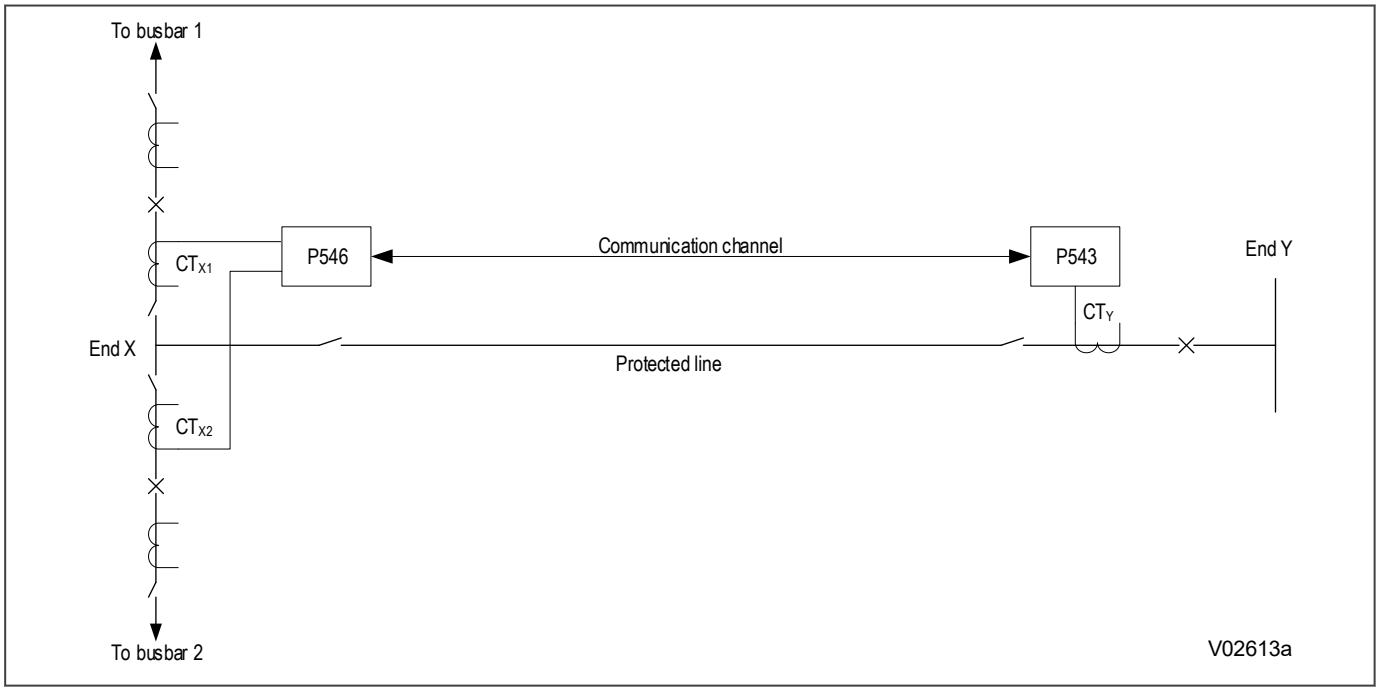


Figure 56: Breaker-and-a-half application

As shown in the figure above, a P546 is applied at End X as the line is fed from a breaker and a half substation configuration. At End Y where there is a single breaker, a P543 can be installed.

An ‘Additional Bias’ quantity is calculated at terminals which have two sets of CT inputs, and the Additional Bias is used in the calculation to determine whether to trip or to restrain.

The calculations for differential and bias currents are as follows:

At End X:

$$I_{diff} = \bar{I}_{CTX1} + \bar{I}_{CTX2} + \bar{I}_{CTY}$$

$$I\ bias = (\left|ICTX1\right| + \left|ICTX2\right| + (Additional\ Bias\ if\ non\ zero)\ or \left|IREMOTE\right|)/2$$

In this example the Additional Bias is zero as the device at the remote end has a single set of CT inputs.

The Additional Bias (to be sent to end Y) is calculated on a per phase basis by scalar summing both local currents (I_{CTX1} and I_{CTX2}) and selecting the largest of the three calculated. This current is included in the messages containing the information transmitted between terminals.

At End Y:

$$I\ diff = \bar{I}_{CTY} + \bar{I}_{CTX1} + \bar{I}_{CTX2}$$

$$I\ bias = (\left|ICTY\right| + (Additional\ Bias\ if\ non\ zero)\ or \left|IREMOTE\right|)/2$$

In this case Additional Bias is sent by End X (device with two CT inputs).

Different CT ratios can be set for CTX1 and CTX2 using the settings PhaseCT1 Primary and PhaseCT2 Primary at end X. If different CT ratios are used, the CT1 current inputs must be connected to the CT set with the highest primary rated current. CT1 is used as a reference and secondary current from CT2 is scaled down to match the reference CT1.

You cannot set PhaseCT2 Primary setting above PhaseCT1 Primary.

You should keep the ratio between PhaseCT1 Primary and PhaseCT2 Primary below 4.

7.16 STUB BUS DIFFERENTIAL PROTECTION

This product can provide stub-bus protection associated with the differential protection.

If you wish to use this feature you must ensure that the current differential protection is enabled. You will need to map one of the opto-isolated inputs to the DDB ***Stub Bus Enabled*** using the programmable scheme logic and you will need to enable the feature by setting ***Ph Diff Stub Bus*** in the *CURRENT DIFF* column to `Enabled`.

When the stub bus protection is enabled and activated by energisation of the opto-isolated input, all current values transmitted to the remote relays, and all those received from remote relays are set to zero. The Stub bus protection then provides differential protection for the stub zone. No differential intertrip or permissive intertrip signals will be issued, or acted upon by the affected terminal. Intertripping signals mapped via IM64 will be acted upon, and the affected terminal remains active to protect the isolated stub bus.

For products having two sets of CT inputs, the stub bus protection takes the two sets of current inputs and uses them as inputs to the phase differential current protection. The values are compared against the dual slope characteristics to determine whether tripping should occur or not.

For products having a single set of CT inputs, an additional setting (***Ph Is1 StubBus***) is provided. In these applications, if the stub-bus feature is enabled and activated, the protection will trip if the measured current exceeds the ***Ph Is1 StubBus*** setting.

Tripping due to the operation of the stub-bus protection is always three-phase.

The principle is outlined in the figure below:

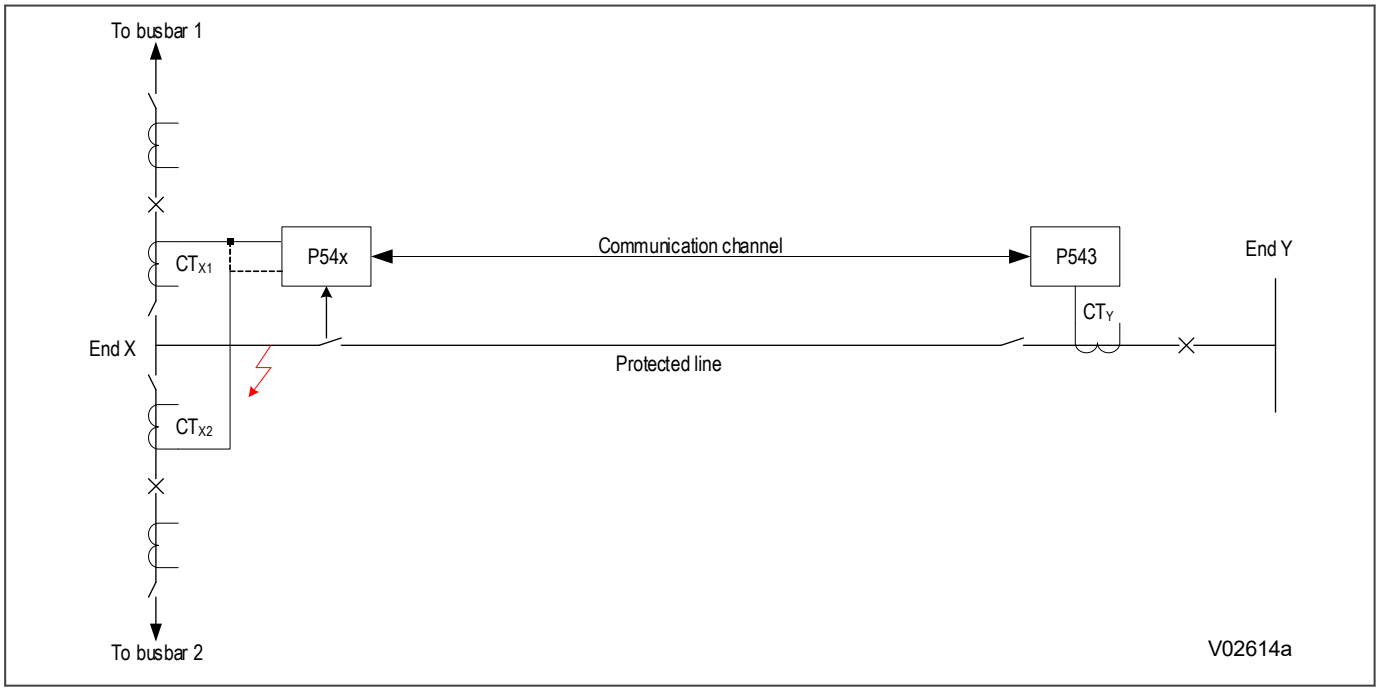


Figure 57: Stub bus protection

Note:
Models having distance protection feature a phase segregated stub bus protection associated with the distance protection elements. Where applicable these are described along with the distance elements.

7.17 DIFFERENTIAL IED COMPATIBILITY WITH PREVIOUS VERSIONS

Please refer to Appendix D for a full compatibility matrix for MiCOM P541 - P546 Line Differential Protection Relays. The matrix can be used to check communications compatibility between related devices.

7.18 APPLICATION NOTES

7.18.1 SETTING UP THE PHASE DIFFERENTIAL CHARACTERISTIC

The biased phase current differential characteristic is defined by four protection settings. Each can be set independently. This flexibility allows the characteristic to be set for particular sensitivity and current transformer requirements. To simplify setting the protection, however, we strongly recommend three of the settings be fixed as:

- ***Phase Is2*** = 2.0 pu
- ***Phase k1*** = 30% (This provides stability for small CT mismatches, while ensuring good sensitivity to resistive faults under heavy load conditions
- ***Phase k2*** = 150% (For 2 terminal applications to provides stability under heavy through fault current conditions)
- ***Phase k2*** = 100% (For 3 terminal applications to provides stability under heavy through fault current conditions)

These settings give a characteristic suitable for most applications so that only the Phase Is1 setting needs changing from the default value.

Phase Is1 is the setting which determines the minimum pick-up of the phase current differential elements. This value should be set to account for any mismatch between the current transformers at the different terminals, as well the capacitive charging current if this is not compensated.

If voltage inputs are connected, the charging current can be compensated for. To do this you need to set the ***Compensation*** setting in the *CURRENT DIFF* column to `Cap Charging` and then programme the line positive sequence capacitive susceptance value into the ***Susceptance*** setting now apparent in the *CURRENT DIFF* column. If `Cap Charging` is selected, ***Phase Is1*** may be set below the value of line charging current. We recommend that you choose ***Phase Is1*** only sufficiently below the charging current to offer the required fault resistance coverage as now described.

The table below shows some typical steady state charging currents for various lines and cables.

Voltage (kV)	Core Formation and Spacing	Conductor Size in mm2	Charging Current A/km
11 kV Cable	Three-core	120	1.2
33 kV Cable	Three-core	120	1.8
33 kV Cable	Close-trefoil	300	2.5
66 kV Cable	Flat, 127 mm	630	10
132 kV Overhead Line		175	0.22
132 kV Overhead Line		400	0.44
132 kV Cable	Three-core	500	10
132 kV Cable	Flat, 520 mm	600	20
275 kV Overhead Line		2 x 175	0.58
275 kV Overhead Line		2 x 400	0.58
275 kV Cable	Flat, 205 mm	1150	19
275 kV Cable	Flat, 260 mm	2000	24
400 kV Overhead Line		2 x 400	0.85
400 kV Overhead Line		4 x 400	0.98
400 kV Cable	Flat, 145 mm	2000	28
400 kV Cable	Tref., 585 mm	3000	33

If capacitive charging current compensation is not used, the setting of ***Phase Is1*** must be set above 2.5 times the steady state charging current. Where charging current is low or negligible, the recommended setting of 0.2 pu (factory default) should be applied.

If there is a mismatch between CTs at line ends, then the lowest primary CT rated current should be used as a reference current for p.u. calculations (assuming that the load current cannot continuously exceed this value). This means that the recommended settings ***Phase Is1*** = 0.2 pu is equal to 0.2*(the lowest primary CT rated value). The same consideration applies for other current settings such as ***Phase Is2***.

7.18.2 SENSITIVITY UNDER HEAVY LOADS

The sensitivity of the phase current differential protection is governed by its settings and also the magnitude of load current in the system. For a three-ended system, with devices LOCAL, REMOTE1, and REMOTE2, the following applies:

$$|I_{diff}| = |(\bar{I}_{LOCAL} + \bar{I}_{REMOTE1} + \bar{I}_{REMOTE2})|$$

$$|I_{bias}| = 0.5\ (|I_{LOCAL}| + |I_{REMOTE1}| + |I_{REMOTE2}|)$$

Assume a load current of I_L flowing from end LOCAL to REMOTE1 and REMOTE2. Assume also a high resistance single-end fault of current I_F, being fed from end LOCAL. In the worst case, we can also assume I_F to be in phase with I_L:

$$I_{LOCAL} = I_L + I_F$$

$$I_{REMOTE1} = -y*I_L \text{ where } 0<y<1$$

$$I_{REMOTE2} = -(1-y)\ I_L$$

$$|I_{diff}| = |I_F|$$

$$|I_{bias}| = |I_L| + 0.5\ |I_F|$$

Phase current differential protection sensitivity when $|I_{bias}| <$ *Phase Is2*:

The phase current differential protection would operate if $|I_{diff}| >$ ***Phase k1*** $|I_{bias}|$ + ***Phase Is1***

therefore:

$$|I_F| > (\textbf{\textit{Phase k1}}\ |I_L| + \textbf{\textit{Phase Is1}}) / (1 - 0.5\ \textbf{\textit{Phase k1}})$$

For ***Phase Is1*** = 0.2 pu, ***Phase k1*** = 30% and ***Phase Is2*** =2.0 pu, then

- for $|I_L|$ = 1.0 pu, the phase current differential protection would operate if $|I_F|$ > 0.59 pu
- for $|I_L|$ = 1.59 pu, the phase current differential protection would operate if $|I_F|$ > 0.80 pu

If $|I_F|$ = 0.80 pu and |I| = 1.59 pu, then $|I_{bias}|$ = 1.99 pu, which reaches the limit of the low percentage bias curve.

Phase current differential protection sensitivity when $|_{bias}|$ > Phase Is2:

The phase current differential protection would operate if $|I_{diff}| >$ ***Phase k2*** $|I_{bias}|$ - (***Phase k2*** - ***Phase k1***) ***Phase Is2*** + ***Phase Is1***

therefore:

$$|I_F| > (\textbf{\textit{Phase k2}}\ |I_L| - (\textbf{\textit{Phase k2}} - \textbf{\textit{Phase k1}})\ \textbf{\textit{Phase Is2}} + \textbf{\textit{Phase Is1}}) / (1 - 0.5\ \textbf{\textit{Phase k2}})$$

For ***Phase Is1***= 0.2 pu, ***Phase k1*** = 30%, ***Phase Is2*** = 2.0 pu and ***Phase k2*** = 100%, then,

- for $|I_L|$ = 2.0 pu, the phase current differential protection would operate if $|I_F|$ > 1.6 pu
- for $|I_L|$ = 2.5 pu, the phase current differential protection would operate if $|I_F|$ > 2.6 pu

Fault resistance coverage

Assuming the fault resistance R_F is much higher than the line impedance and source impedance, then for a 33 kV system and 400/1 CT:

$$|I_F| = (Vph\text{-}n / R_F)(1/CT\ ratio)\ pu = 47.63/R_F\ pu$$

Based on the analysis above, the phase current differential protection detects a fault current in excess of 0.59 pu with a load current of 1 pu flowing. The fault resistance is less than 47.63/0.59 = 81 ohms in this case.

With a short time overload current of 2.0 pu, the phase current differential protection can detect a fault resistance of 47.63/1.6 = 30 ohms or lower.

7.18.3 PERMISSIVE INTERTRIPPING

The permissive intertrip (PIT) timer can be set between 0 and 200 ms. This time should be set to provide discrimination with other protection devices. For example, if there is a genuine busbar fault, the time delay should be set to allow busbar protection to clear the fault. A typical setting may be 100 to 150 ms.

7.18.4 CT RATIO CORRECTION SETTING GUIDELINES

If there is no mismatch between current transformers at line ends, ***Ph CT Corr'tion*** should be set to `1` in all devices

> *Note:*
> *The following consideration includes references to currents used in Neutral Current Differential protection and protection of feeders with In-zone transformers. If not applicable they may be ignored.*

If the CTs at line ends have different primary ratings, then one of them is considered as a reference (the one with the lowest primary rating). ***Ph CT Corr'tion*** should be set to `1` in the device connected to the reference CT. For all other devices ***Ph CT Corr'tion*** is calculated as follows:

$$\textit{Ph CT Corr'tion}_{\ IEDx} = (\textit{Phase CT Primary}_{\ IEDx}) / (\textit{Phase CT Primary}_{\ REFERENCE})$$

Settings ***Phase Is1***, ***Phase Is2***, ***Id High Set***, ***Diff Is1***, ***Diff Is2*** must be calculated as pu of the reference primary rating, then converted into local primary (secondary) values. For setting ***Phase Is1*** in IEDX, the equations would be:

$$\textit{Phase Is1}\ [\text{p.u.}] = (\textit{Phase Is1}_{\ IABSOLUTE\ PRI}\ [\text{A}]) / (\textit{Phase CT Primary}_{\ REFERENCE}\ [\text{A}])$$

$$\textit{Phase Is1}_{\ IEDx\ PRI.}\ [\text{A}] = (\textit{Phase Is1}\ [\text{p.u.}])\ (\textit{Phase CT Primary}_{\ IEDx})$$

$$\textit{Phase Is1}_{\ IEDx\ SEC.}\ [\text{A}] = (\textit{Phase Is1}\ [\text{p.u.}])\ (\textit{Phase CT Sec'y}_{\ IEDx})$$

The same considerations apply to settings ***Phase Is2***, ***Id High Set***, ***In Diff Is1***, ***Diff Is2***.

Example:

Assume that we have a three-ended application with line ends X, Y, Z (500/5, 800/5, 200/1) and Current Differential settings in absolute primary values:

$$\textit{Phase Is1}_{\ ABSOLUTE\ PRI.} = 100\text{A}$$

$$\textit{Phase Is2}_{\ ABSOLUTE\ PRI.} = 1000\text{A}$$

$$\textit{Id High Set}_{\ ABSOLUTE\ PRI.} = 3000\text{A}$$

$$\textit{Diff Is1}_{\ ABSOLUTE\ PRI.} = 50\text{A}$$

$$\textit{Diff Is2}_{\ ABSOLUTE\ PRI.} = 1000\text{A}$$

Setting	End X	End Y	End Z
Phase CT Primary	500A	800A	200A
Phase CT Sec'y	5A	5A	1A
Ph CT Corr'tion	500/200 = 2.5	800/200 = 4	1 (reference)

Setting	End X	End Y	End Z
Phase Is1 [p.u.]	100/200 = 0.5	100/200 = 0.5	100/200 = 0.5
Phase Is1 (Primary)	0.5*500 = 250A	0.5*800 = 400A	0.5*200 = 100A
Phase Is1 (Secondary)	0.5*5 = 2.5A	0.5*5 = 2.5A	0.5*1 = 0.5A
Phase Is2 [p.u.]	1000/200 = 5	1000/200 = 5	1000/200 = 5
Phase Is2 (Primary)	5*500 = 2500A	5*800 = 4000A	5*200 = 1000A
Phase Is2 (Secondary)	5*5 = 25A	5*5 = 25A	5*1 = 5A
Id High Set [p.u.]	3000/200 = 15	3000/200 = 15	3000/200 = 15
Id High Set (Primary)	15*500 = 7500A	15*800 = 12000A	15*200 = 3000A
Id High Set (Secondary)	15*5 = 75A	15*5 = 75A	15*1 = 15A
In Diff Is1 [p.u.]	50/200 = 0.25	50/200 = 0.25	50/200 = 0.25
In Diff Is1 (Primary)	0.25*500 = 125A	0.25*800 = 200A	0.25*200 = 50A
In Diff Is2 (Secondary)	0.25*5 = 0.75A	0.25*5 = 0.75A	0.25*1 = 0.25A
In Diff Is1 [p.u.]	1000/200 = 5	1000/200 = 5	1000/200 = 5
In Diff Is1 (Primary)	5*500 = 2500A	5*800 = 4000A	5*200 = 1000A
In Diff Is2 (Secondary)	5*5 = 25A	5*5 = 25A	5*1 = 5A

7.18.5 FEEDERS WITH SMALL TAPPED LOADS

Where transformer loads are tapped off the protected line, it is not always necessary to install CTs at this location. If the tee-off load is light, differential protection can be configured for the main line alone. The settings ***Phase Char***, ***Phase Time Delay*** and ***Phase TMS*** or ***Phase Time Dial*** allow the differential element to time grade with IDMT overcurrent protection devices or fuses protecting the tap. This keeps stability of the differential protection for external faults on the tee circuit.

7.18.6 SETTING A TWO-TERMINAL PHASE CURRENT DIFFERENTIAL ELEMENT

All four settings are user adjustable. This flexibility in settings allows the phase current differential characteristic to be tailored to suit particular sensitivity and CT requirements. To simplify your task, we strongly recommend three of the settings be fixed to:

Phase Is2 = 2.0 pu

Phase k1 = 30%

Phase k2 = 150%

These settings will give a characteristic suitable for most applications. It leaves only the ***Phase Is1*** setting to be decided by you. The value of this setting should be in excess of any mismatch between line ends. It should also account for line charging current, where necessary.

By considering the circuit shown below, the settings for the phase current differential element can be established.

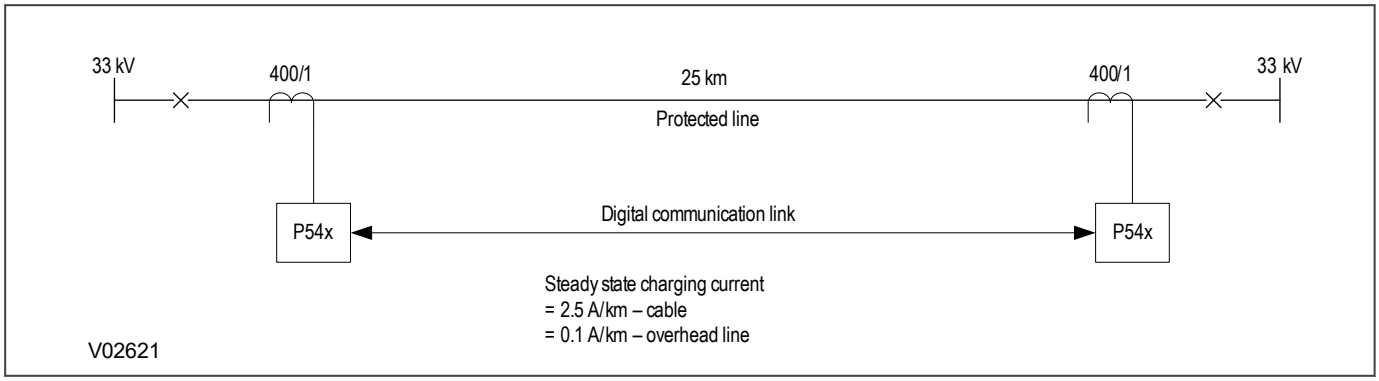


Figure 58: Typical two-terminal plain feeder circuit

In the case that voltage inputs are not in place, no facility to account for line charging current is available. The setting of ***Phase Is1*** must therefore be set above 2.5 times the steady state charging current value. In this example, assume a cable is used and there are not VT inputs connected to the device:

Phase Is1 > 2.5(Ich)

Phase Is1 > 2.5 (25 km x 2.5 A/km)

Phase Is1 > 156.25 A

The line CTs are rated at 400 amps primary. The setting of Phase Is1 must therefore exceed 156.25/400 = 0.391 pu.

Therefore select:

Phase Is1 = 0.4 pu

If VTs are connected, a facility exists to overcome the effects of the line charging current. To use this you need to set the ***Compensation*** setting in the *CURRENT DIFF* column to `Cap Charging` and then programme the line positive sequence capacitive susceptance value into the ***Susceptance*** setting now apparent in the *CURRENT DIFF* column. This can be calculated from the line charging current as follows (assuming a VT ratio of 33 kV / 110 V):

Ich = 25 x 2.5 A = 62.5 A

Susceptance B = ωC = Ich/V

B = 62.5 A/(33/√3) kV primary

B = 3.28 x 10-3 S primary

Therefore set:

B = 3.28 mS primary (= 2.46 mS secondary)

Phase Is1 may now be set below the value of line charging current if required, however we suggest that you choose ***Phase Is1*** only sufficiently below the charging current to offer the required fault resistance coverage. Where charging current is low or negligible, the recommended factory default setting of 0.2xIn should be applied.

7.18.7 SETTING A THREE-TERMINAL PHASE CURRENT DIFFERENTIAL ELEMENT

All four settings are user adjustable. This flexibility in settings allows the phase current differential characteristic to be tailored to suit particular sensitivity and CT requirements. To simplify your task, we strongly recommend three of the settings be fixed to:

Phase Is2 = 2.0 pu

Phase k1 = 30%

Phase k2 = 100%

These settings will give a characteristic suitable for most applications. It leaves only the ***Phase Is1*** setting to be decided by you. The value of this setting should be in excess of any mismatch between line ends. It should also account for line charging current, where necessary.

By considering the circuit shown below, the settings for the phase current differential element can be established.

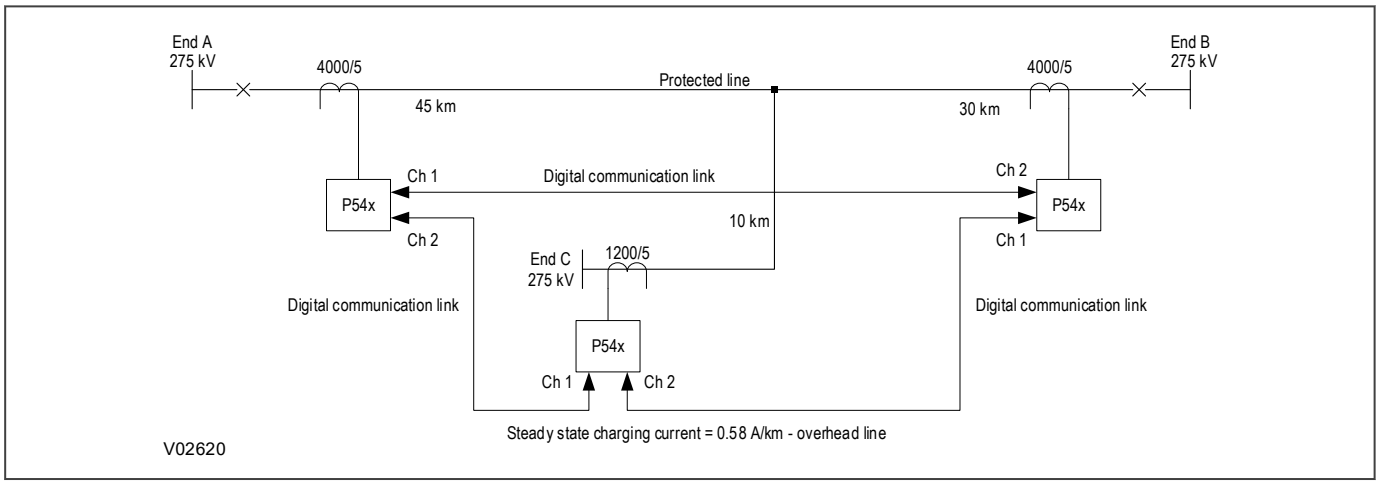


Figure 59: Typical three-terminal plain feeder circuit

If there are no VT inputs connected, the setting ***Phase Is1*** must be 2.5 times the steady state charging current suitably corrected for the different CT ratios as presented below in the calculation of charging current compensated values. For an overhead line circuit with a charging current of 0.58A/km the charging current will be:

$$Ich = 0.58\ A\ (\ 45 + 30 + 10\ ) = 49.3\ A$$

If VT inputs are connected, there is a facility to overcome the effect of charging current. To do this you need to enter the positive sequence capacitive susceptance value.

Considering the charging current on the circuit shown in the figure above, the following calculation applies:

$$Ich = 0.58\ A\ (\ 45 + 30 + 10\ ) = 49.3\ A$$

$$Susceptance = \omega C = Ich/V$$

$$B = 49.3\ A/(\ 275/\ \sqrt{3})\ kV\ primary$$

$$B = 0.31\ x\ 10\text{-}3\ S\ primary.$$

The CT ratios on the three ends are different, so it is necessary to apply a correction factor to ensure secondary currents balance for all conditions:

To calculate the correction factor (CF), the same primary current must be used even if this current is not the expected load transfer for every branch. This will ensure secondary current balance for all conditions.

CT ratio correction input data is shown in the table below:

Setting	End A	End B	End C
Phase CT Primary	4000A	4000A	1200A
Ph CT Corr'tion	4000/1200 = 3.33	4000/1200 = 3.33	1 (reference)

We recommend the following settings:

Phase Is1 = 0.2 p.u. = 0.2*1200A = 240A

Phase Is2 = 2 p.u. = 2*1200A = 2400A

Phase k1 = 30%

Phase k2 = 100%

Therefore, settings in primary/secondary values for each device can be calculated as follows:

Setting	End A	End B	End C
Phase CT Primary	4000A	4000A	1200A
Phase CT Sec'y	5A	5A	5A
Phase Is1 [p.u.]	0.2	0.2	0.2
Phase Is1 (Primary)	0.2*4000 = 800A	0.2*4000 = 800A	0.2*1200 = 240A
Phase Is1 (Secondary)	0.2*5 = 1A	0.2*5 = 1A	0.2*5 = 1A
Phase Is2 [p.u.]	2	2	2
Phase Is2 (Primary)	2*4000 = 8000A	2*4000 = 8000A	2*1200 = 2400A
Phase Is2 (Secondary)	2*5 = 10A	2*5 = 10A	2*5 = 10A

Note:
Settings shown in primary values at Ends A and B appear different compared with end C. This is not a problem as the currents at Ends A and B will be multiplied by the Correction Factor, when the differential calculation is done.

Susceptance settings for Ends A and B

With a VT ratio 275 kV/110 V and CT ratio 4000/5:

$R_{CT} = 800$

$R_{VT} = 2500$

$B = 310\ \mu S$

Secondary susceptance = $310\ \mu S(R_{VT}/ R_{CT}) = 968\ \mu S$

Susceptance settings for End C

With a VT ratio 275 kV/110 V and CT ratio 1200/5:

$B = 310\ \mu S$

Secondary susceptance = $310\ \mu S(R_{VT}/ R_{CT}) = 3.22\ mS$

7.18.8 TRANSFORMER FEEDER APPLICATION EXAMPLE

Ratio correction example:

P543 and P545 IEDs are suitable for the protection of transformer feeders. An example is shown in the figure below.

20 MVA Transformer, Dyn1, 33/11 kV

HV CT ratio - 400/1

LV CT ratio - 1500/1

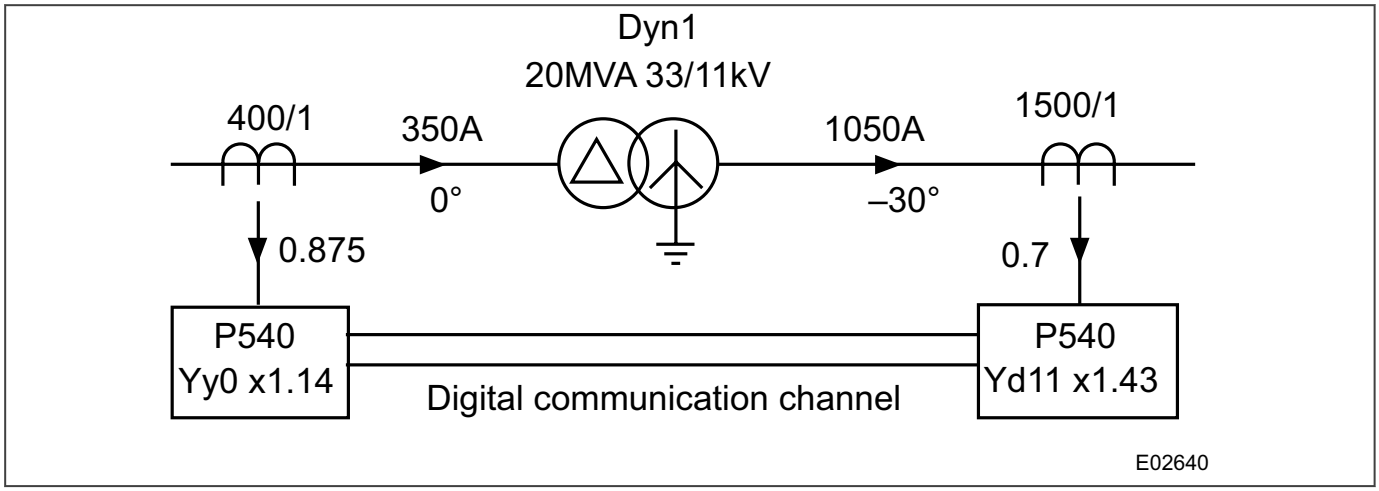


Figure 60: Typical transformer feeder circuit

Calculate the required ratio correction factor to apply to the IEDs at each line end.

33 kV full load current = 20 MVA/(33 kV.√3) = 350 A

11 kV full load current = 20 MVA/(11 kV.√3) = 1050 A

Each of these full load (reference) currents should be corrected to CT rated current:

Setting	HV Side	LV Side
Phase CT Primary	400A	1500A
Reference Primary	350A	1050A
Ph CT Corr'tion	400/350 = 1.14	1500/1050 = 1.43

When a Star/Delta software interposing CT is chosen, no additional account has to be taken for the √3 factor which would be introduced by the delta winding. This is accounted for by the IED.

Phase correction example:√

Using the same transformer as shown in the figure above it is now necessary to correct for the phase shift between the HV and LV windings.

The transformer connection shows that the delta connected high voltage line current leads the low voltage line current by 30°. To ensure that this phase shift does not create a differential current, the phase shift must be corrected in the LV secondary circuit. The LV IED software interposing CT is effectively a winding replica of the main power transformer. It not only provides a +30° phase shift, but also performs the necessary function of filtering out any LV zero sequence current component.

Hence, the HV IED setting requires no phase shift or zero sequence current filtering (as HV winding is delta connected). The LV IED setting requires phase shifting by +30° and also requires zero sequence current filtering (as LV winding is star connected).

Set: HV = Yy0

LV = Yd11 (+30°)

7.18.9 THREE WINDING TRANSFORMER IN ZONE EXAMPLE

P543 and P545 IEDs are suitable for the protection of three winding transformers in zone. An example is shown in the figure below.

100 MVA/100MVA/30MVA Transformer, Ynyn0d1, 400 kV/110 kV/30 kV

HV, 400 kV CT ratio - 600/1

MV, 110 kV CT ratio - 1200/1

LV, 30 kV CT ratio - 2000/5

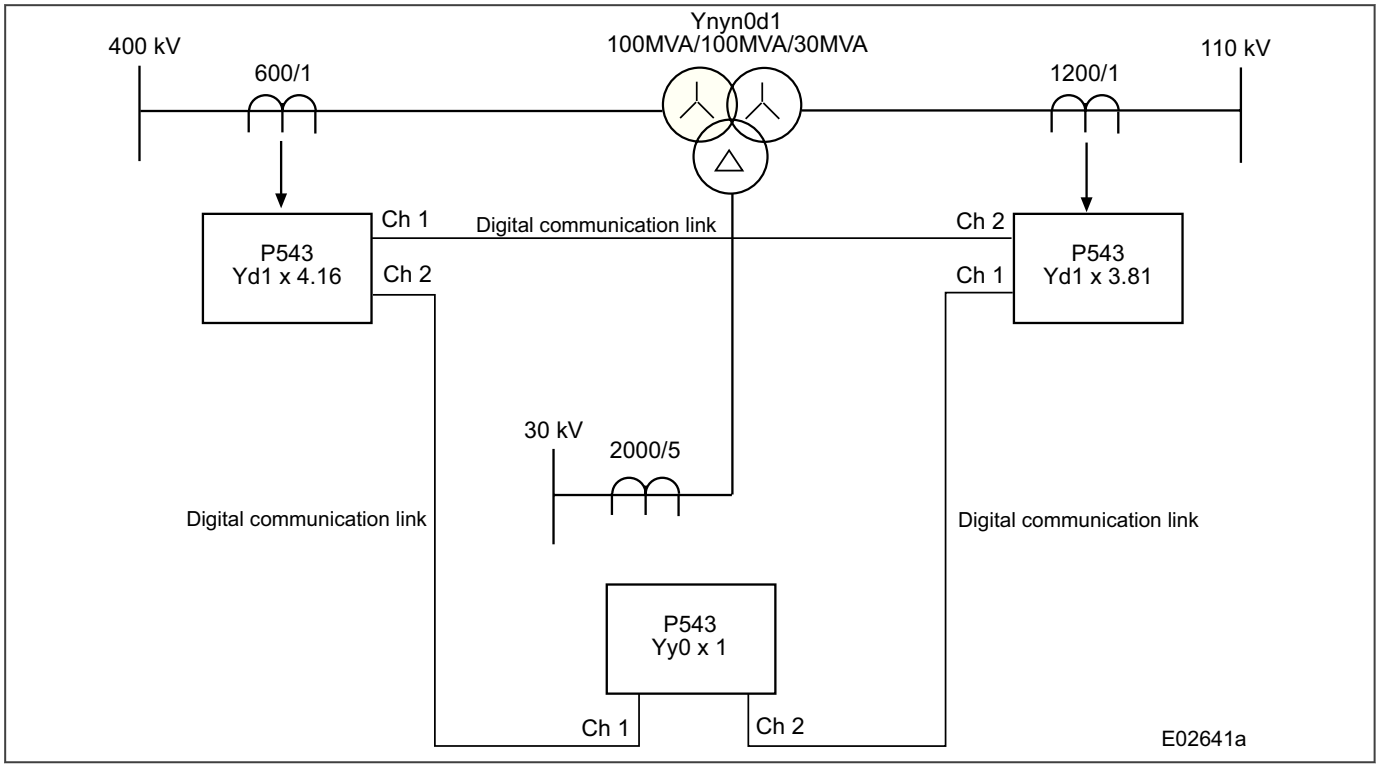


Figure 61: Three winding transformer in zone application

These three IEDs must be rated differently, i.e. 1A for HV and MV side and 5 A for 30 kV side. This does not present a problem for P54x IEDs as the digital signals representing the currents are in pu.

It is necessary to calculate the required ratio correction factor (CF) as well as the phase correction factor for each end. To choose the appropriate vector compensation, it is necessary to account for phase current and zero sequence current filtering as explained in the Transformer Feeder Example.

To calculate the correction factors, it is necessary to use the same base power (100 MVA in this particular case) for the three sides of the transformer although the third winding actually has lower rated MVA. This is to ensure that compensated currents balance for all conditions.

Setting	HV Side	MV Side	LV SIDE
Phase CT Primary	600A	1200A	2000A
Phase CT Sec'y	1A	1A	5A
Reference Primary (at 100 MVA basis)	100000/(400 √3) = 144.3A	100000/(110 √3) = 524.9A	100000 (30 √3) = 1924.5A
Ph CT Corr'tion	600/144.3 = 4.16	1200/524.9 = 2.29	2000/1924.5 = 1.04

To choose the vector compensation setting, it should be noted that the Wye connected HV line is in phase with the MV line current and leads the LV line current by 30o. Therefore for LV side, the phase shift must be compensated.

To account for the zero sequence current filtering in the case of an external earth fault, it is necessary to connect the Wye connected power transformer windings to an interposing current transformer (internal IED ICT) to trap the zero sequence current (the secondary side being connected delta).

To account for both vector compensation and zero sequence current filtering, the following vectorial compensation setting is recommended:

- For HV side = Yd1 (-30 deg)
- For MV side = Yd1 (-30 deg)
- For LV side = Yy0 (0 deg)

Note:
It is not necessary to include the √3 factor in the calculation as this is incorporated in the IED algorithm.

P543 and P545 IEDs are suitable for transformer applications, as such an inrush restrain is provided on these IEDs. By enabling inrush restrain, an additional current differential high setting (Id High set) becomes enabled.

When the inrush restrain feature is enabled, this function needs to be enabled in the IED at each line end (3 ends).

The same settings as in the previous examples are recommended:

- Is1 = 0.2 pu
- Is2 = 2 pu
- K1 = 30%
- K2 = 100%

For the current differential high setting (Id High set) the setting must be in excess of the anticipated inrush current after ratio correction. Assuming that maximum inrush is 12 times the nominal transformer current, it would be safe to set the IEDs at 15 times the nominal current, therefore the setting would be:

- Id high set: = 15 pu

Setting	HV Side	MV Side	LV Side
Phase CT Primary	600A	1200A	2000A
Phase CT Sec'y	1A	1A	5A
Reference Primary	144.3A	524.9A	1924.5A
Ph CT Corr'tion	4.16	2.29	1.04
Phase Is1 [p.u.]	0.2	0.2	0.2
Phase $Is1_{ABSOLUTE\ PRI}$	0.2*144.3 = 28.9A	0.2*524.9 = 105A	0.2*1924.5 = 384.9A
Phase Is1 (Primary)	0.2*600 = 120A	0.2*1200 = 240A	0.2*2000 = 400A
Phase Is1 (Secondary)	0.2*1 = 0.2A	0.2*1 = 0.2A	0.2*5 = 1A
Phase Is1 [p.u.]	2	2	2
Phase $Is2_{ABSOLUTE\ PRI}$	2*144.3 = 289A	2*524.9 = 1050A	2*1924.5 = 3849A
Phase Is2 (Primary)	2*600 = 1200A	2*1200 = 2400A	2*2000 = 4000A
Phase Is2 (Secondary)	2*1 = 2A	2*1 = 2A	2*5 = 10A
Id High Set [p.u.]	15	15	15
Id High $Set_{ABSOLUTE\ PRI}$	15*144.3 = 2164.5A	15*524.9 = 7873.5A	15*1924.5 = 28867.5A
Id High Set (Primary)	15*600 = 9000A	15*1200 = 18000A	15*2000 = 30000A
Id High Set (Secondary)	15*1 = 15A	15*1 = 15A	15*5 = 75A

7.18.10 MESH CORNER AND BREAKER-AND-A-HALF APPLICATION NOTES

Where a line is fed from a mesh corner or 1½ breaker switched substation, two options are available for CT connections to the device. The first is by paralleling the two sets of line CTs into a common input. The second is by using devices with two separate sets of three-phase CT. The second option provides more stable protection and the setting can be made more sensitive.

In the case of a through fault as shown in the figure below, the device connected to circuit 'A' should see no current so it remains stable. Under this condition, no bias current is measured by the device. To ensure stability, the two sets of line CTs should be the same in all characteristics and equally loaded. Then the protection connection should be at the equipotential point of the secondary leads.

In the case of circuit 'B' no differential current should result. However, a large bias current exists, providing a high degree of stability if there is a through fault. This bias also ensures stability where CTs are not closely matched. Therefore, circuit 'B' is the preferred connection for such applications, so products with two sets of three-phase CT inputs would normally be specified.

Different CT ratios can be set for CT1 and CT2. CT1 current inputs of the device must be connected to the CT set with the highest primary rated current. You cannot set ***PhaseCT2 Primary*** setting above ***PhaseCT1 Primary***. You should keep the ratio between ***PhaseCT1 Primary*** and ***PhaseCT2 Primary*** less than 4:

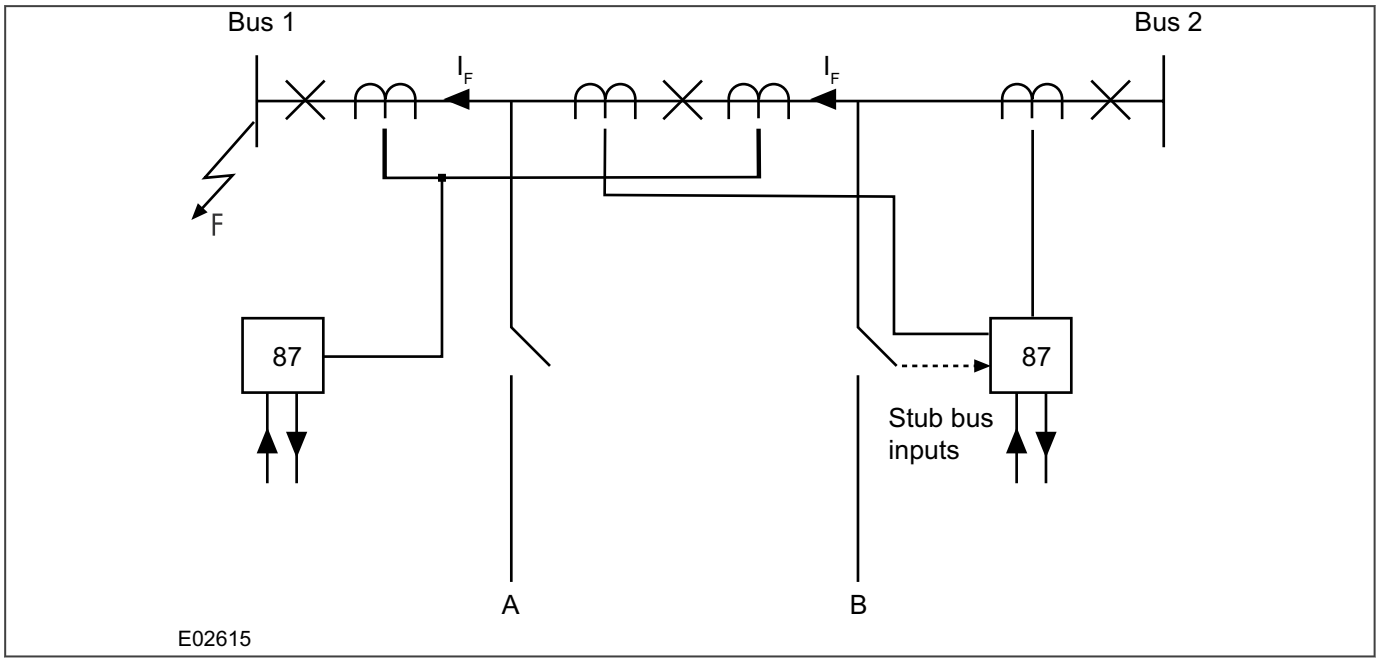


Figure 62: Breaker-and-half switched substation

7.18.11 CHANNEL SWITCH SETTING

The mapping between a logical differential communications channel (for example, the setting ***Baud Rate Ch1*** refers to logical Channel 1) and the physical fibre optic differential communications channel located at the back of the relay can be swapped/switched. This is achieved via the ***Channel Switch*** setting in the *PROT COMMS/ IM64* column. This setting is only visible for relays with two fibre optic differential communications channels.

In addition to other advantages, the capability to switch is useful in 3-ended applications. In the example below, a single order code can be used at ends A and B.

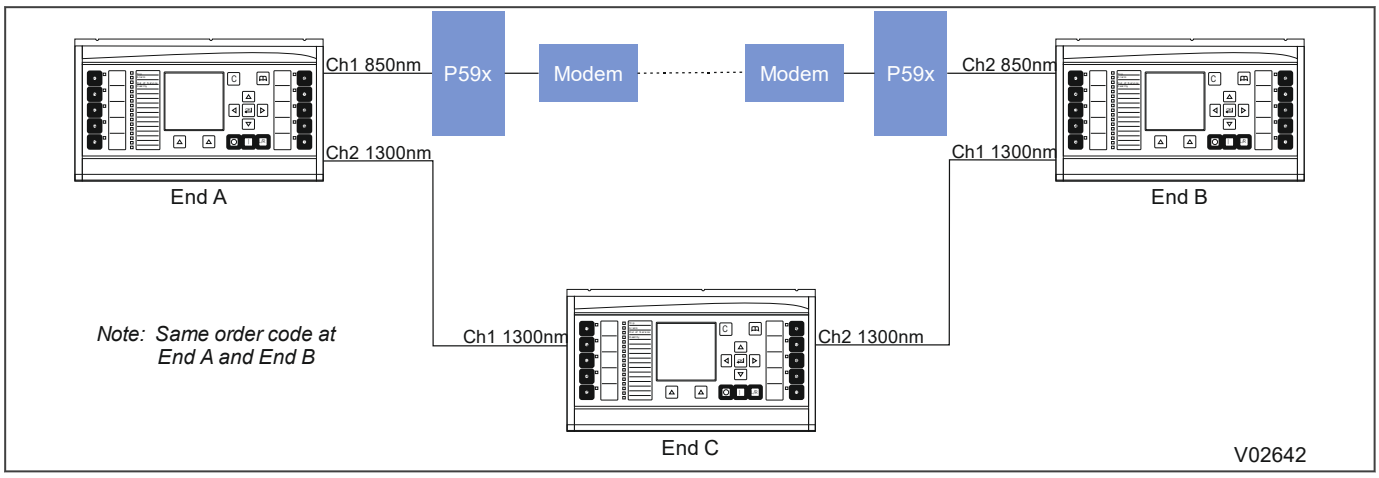


Figure 63: Three-ended switch application

CHAPTER 8

DISTANCE PROTECTION

8.1 CHAPTER OVERVIEW

This chapter introduces the principles and theory behind the protection and describes how it is implemented in this product. Guidance for applying this protection is also provided.

This chapter contains the following sections:

Chapter Overview 146
Introduction 147
Distance Measuring Zones Operating Principles 149
Quadrilateral Characteristic 161
Earth Fault Quadrilateral Characteristics 168
Phase and Earth Fault Distance Protection Implementation 185
Distance Isolated and Compensated Systems 197
Application Notes 211

8.2 INTRODUCTION

Amongst protection engineers, the basic principles of Distance Protection are widely documented and understood. If you are reading this chapter, we assume that you are familiar with the principles of distance protection and associated components such as Aided Schemes. However, to help you choose suitable settings, some of the principles of operation of the Distance Measuring Zones is included in this chapter.

8.2.1 DISTANCE PROTECTION PRINCIPLE

The principle behind Distance protection is based on using measured values of voltage and current to calculate impedance seen from a relaying point. If the impedance calculated is an unexpected value, this may indicate a fault.

The impedance of a transmission line is proportional to its length. If voltage and current signals are available at a relaying point, they can be used to calculate the impedance value seen from the relaying point. Impedance values looking forward into the line, as well as values looking in the reverse direction behind the relaying point can be calculated. The calculated impedance is compared with so called 'Reach Points'. Reach Points are impedance values, which are used to define zones of protection. The device contains settings by which you can configure these Reach Points. The zones are usually numbered (for example: Zone 1, Zone 2, Zone 3). By comparing the calculated impedance with the zone reach points, the device can determine whether a fault is present and if necessary, trip the associated circuit breakers.

8.2.2 PERFORMANCE INFLUENCING FACTORS

As well as the accuracy of the signals presented by the input transducers, an important factor that influences the performance of distance protection is the relationship between the source and line impedance. This is the System Impedance Ratio (SIR), and is defined by Z_S/Z_L.

The following figure represents a fault condition on an electrical power system, and can be used to demonstrate the relationship.

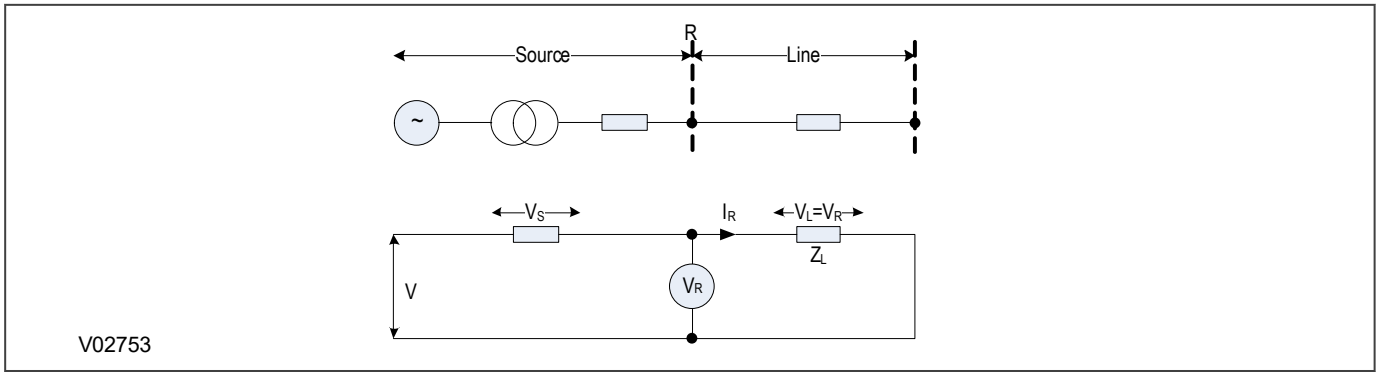


Figure 64: System impedance ratio

The voltage V applied to the impedance loop is the open circuit voltage of the power system. Point R represents the protection location; I_R and V_R are the current and voltage measured by the relay, respectively.

The impedances Z_s and Z_L are described as source and line impedances because of their position with respect to the protection location. Source impedance Z_s is a measure of the fault level at the relaying point. For faults involving earth it is dependent on the method of system earthing behind the relaying point. Line impedance Z_L is a measure of the impedance of the protected section. The voltage V_R applied to the relay is, therefore, I_RZ_L. For a fault at the reach point, this may be expressed in terms of the System Impedance Ratio, using the following expression:

$$V_R = V/(SIR+1)$$

where SIR = Z_S/Z_L

From the equation above, it can be seen that the measured voltage has a significant impact on the decision making process.

The ability of distance protection to measure accurately for a given reach point fault, depends on the voltage at the relaying location being above a minimum value at the time of the fault. If the voltage is above this minimum value, it is generally used to polarise the distance protection and indicate the direction of the fault. This is called self-polarisation.

If the voltage collapses below the minimum threshold necessary to make a sensible decision, alternative methods of polarisation to determine the direction of the fault are needed. Two methods that are applied are cross-polarisation and memory polarisation. If a fault doesn't affect all phases, the voltage signals on the healthy phases can be used for the directional decision. This is called cross-polarisation. If the fault causes all phase voltages to collapse, a stored record of the pre-fault voltage can be used to make the directional decision. This is called memory polarisation. Memory polarisation, cross-polarisation, and self-polarisation can sometimes be used in combination.

8.2.3 IMPEDANCE CALCULATION

Careful selection of the reach settings and tripping times for the various measurement zones enables correct coordination between Distance protection devices. Basic Distance protection will comprise instantaneous directional Zone 1 protection and one or more time delayed zones. A basic distance protection scheme is likely to feature 3 zones of protection, but numerical distance protection devices may have several more zones, some set to measure in the forward direction and some set to measure in the reverse direction.

Some numerical distance protection devices measure the fault voltage and current directly then calculate the impedance, after which they determine whether operation is required according to impedance boundaries defined on an R/X diagram. Many numerical IEDs emulate their traditional electro-mechanical counterparts. Rather than calculating the absolute impedance, they compare the measured fault voltage with a replica voltage derived from the fault current and the zone impedance setting to determine whether the fault is within zone or out-of-zone.

Typically, a comparator will compare either the relative amplitude or relative phase of input quantities to determine impedance limits. Limits may be either straight line characteristics (quadrilaterals), or circular characteristics (Mhos).

8.2.4 IMPLEMENTATION WITH COMPARATORS

The distance protection in this product uses measured values of voltage and current, together with setting values such as line impedance, to determine whether fault conditions exist. The determination as to whether a fault condition exists is performed by so-called ‘comparators’. These comparators use voltage and current inputs in conjunction with impedance settings to decide whether a fault is in a particular zone. Multiple zones can provide protection for the protected line as well as providing back-up protection for connected lines.

All distance zone calculations in this product are constructed using one or more comparators. Each comparator uses two vector quantities which are generally referenced as S1 and S2. S1 and S2 comparators are used to construct either circular (Mho) and/or Quadrilateral characteristics. In the case of Mho characteristics, a single comparator is used to make a tripping decision. In the case of Quadrilateral characteristics, multiple comparators are used to make a tripping decision.

8.2.5 POLARISATION OF DISTANCE CHARACTERISTICS

The distance zone characteristics are polarised (directionalised) to reflect the characteristic angle of the line. Some of the zones of the distance protection are forward looking, some are reverse looking, and some are of the offset type. Polarisation is generally achieved by directional self-polarisation, but memory-polarisation, or cross-polarisation, might be adopted for close-up zero-voltage faults.

8.3 DISTANCE MEASURING ZONES OPERATING PRINCIPLES

All distance zone characteristics in this product are constructed with one or more comparators. The comparators are used to construct either Mho, or Quadrilateral characteristics. This section outlines the principles behind the construction of the characteristics in order to provide an understanding of how best to set them.

The following table details signal definitions used to construct the measuring zone characteristics.

Name	Description
I	Current
I	Current used by the Distance protection measuring element
I_M	Residual current of parallel line (mutual current)
I_N	Neutral Current (derived)
I_{ph}	Faulted phase current (for example IA for A-N fault)
j	The complex operator
k_M	Mutual compensation co-efficient
k_{ZN}	Residual compensation co-efficient
p	Distance polarising factor. A percentage of the memory voltage polarising signal that is added to the self-polarising voltage signal to dictate the level of Mho expansion and help establish a directional decision.
R	Resistance
R	Forward Resistance Reach
R'	Reverse Resistance Reach
S	A voltage vector value comprising one or more voltage components
S_1	A voltage vector input to a comparator
S_2	A second voltage vector input to a comparator
V	Voltage
V	Voltage used by the Distance protection measuring element
V/I	Impedance measured by the Distance protection element
V_{mem}	Voltage memory signal used for polarisation
V_{ph}	Faulted phase voltage (for example VA for A-N fault)
V_{ph}/I_{ph}	Loop impedance measurement
V_S	Source voltage
X	Reactance
Z	Impedance Reach setting
Z'	Reverse Impedance Reach setting
Z_1	Positive sequence impedance
Z_{LP}	Loop impedance
$Z_{replica}$	Forward replica reach in the loop impedance plane = $Z(1+kZN.IN/Iph+kZM.IM/Iph)$
$Z'_{replica}$	Reverse replica reach in the loop impedance plane = $Z'(1+kZN.IN/Iph+kZM.IM/Iph)$
Z_S	Source impedance
σ	An angle (in degrees) usually associated with the tilt of a reactive line on a Quadrilateral characteristic
$\angle\sigma$	A vectorial operator that rotates a vector quantity by an angle of σ^o (alternative representation $e^{j\sigma}$)

Note:
The faulted phase current (I) is generally used as the reference (0°) for the vector diagrams.

8.3.1 MHO CHARACTERISTICS

There are different types of Mho characteristic, but two specific ones are well suited to introducing the defining principles. These are the directional Self-polarised Mho and the Offset Mho. Both types are used for both phase faults and earth faults.

In practice, self-polarised Mhos are rarely used since voltage collapses for close-up faults render self-polarisation unreliable. Rather, memory-polarisation components and/or cross-polarisation components are usually used to provide a polarising reference. Directional Self-Polarised Mhos, however, are simpler to understand and are used by way of introduction.

Mho characteristics are available for phase and earth-fault protection. A mix of Directional Forward, Directional Reverse, and Offset characteristics are available. Zone 1 and Zone 4 are settable as Forward or Reverse. Zones 2, 3, P and Q are settable as Forward or Reverse or Offset.

8.3.1.1 DIRECTIONAL MHO CHARACTERISTIC FOR PHASE FAULTS

The following diagram illustrates how the Directional Self-Polarised Mho characteristic for phase Distance protection is created.

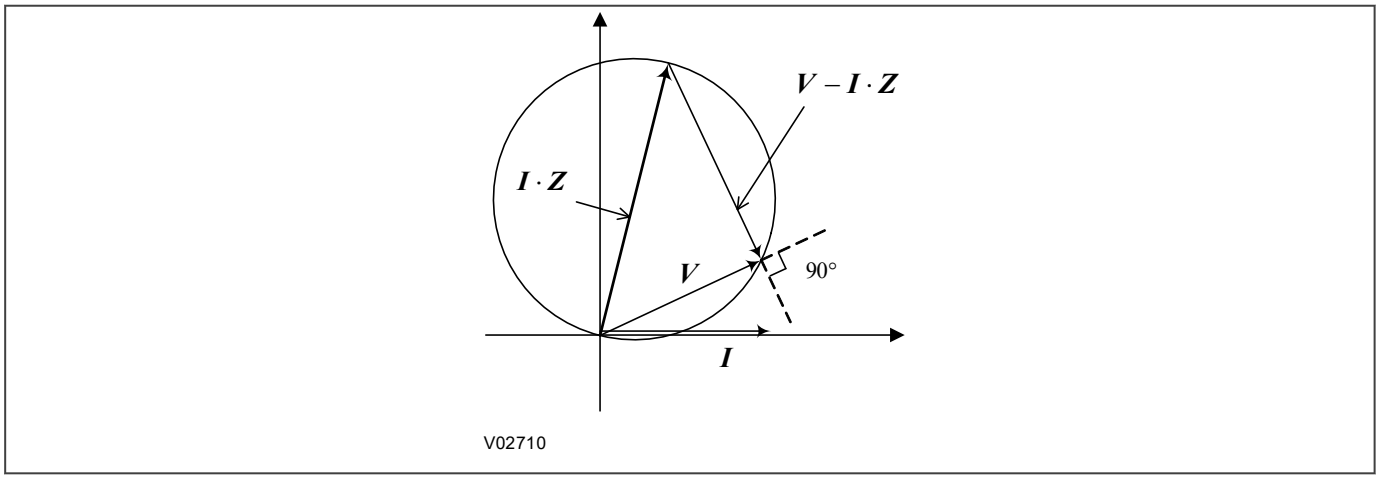


Figure 65: Directional Mho element construction

The two signals provided to the comparator are:

$S_1 = V$

$S_2 = V - I.Z$

Operation occurs when the angle between the signals is greater than 90°

8.3.1.2 OFFSET MHO CHARACTERISTIC FOR PHASE FAULTS

The following diagram illustrates how the Offset Mho characteristic for phase Distance protection is created:

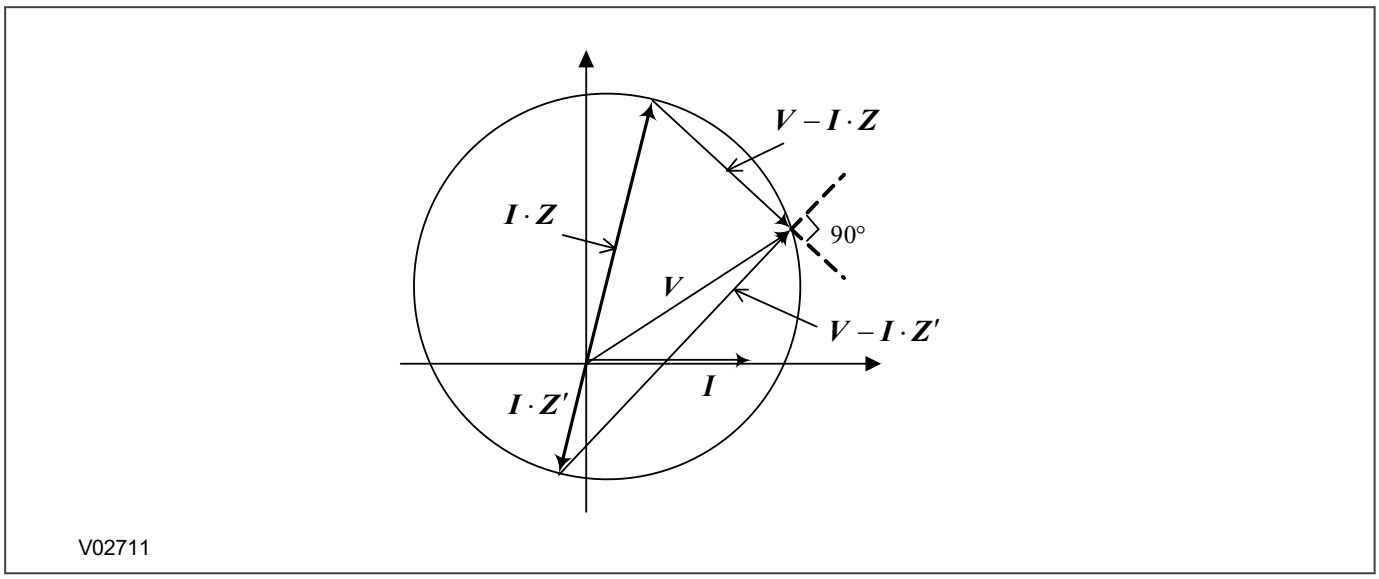


Figure 66: Offset Mho characteristic

The two signals provided to the comparator are:

$S_1 = V - IZ'$

$S_2 = V - IZ$

Operation occurs when the angle between the signals is greater than 90°

8.3.1.3 DIRECTIONAL SELF-POLARISED MHO CHARACTERISTIC FOR EARTH FAULTS

Characteristics of earth-fault elements can be represented in two different complex planes - the positive sequence impedance plane (Z_1 -plane) and the loop impedance plane (Z_{LP} -plane). The reach impedance setting defines the reach in positive sequence impedance terms. The characteristic in the Z_{LP} -plane is generally dynamic because it depends on fault currents. However, the Z_{LP}–plane representation is often more convenient for reference, especially if an injection test kit is used, which cannot apply the residual compensation to the impedance plot, or in the case that the load blinders have to be verified.

The following diagram illustrates how a directional Mho characteristic for earth-faults is created.

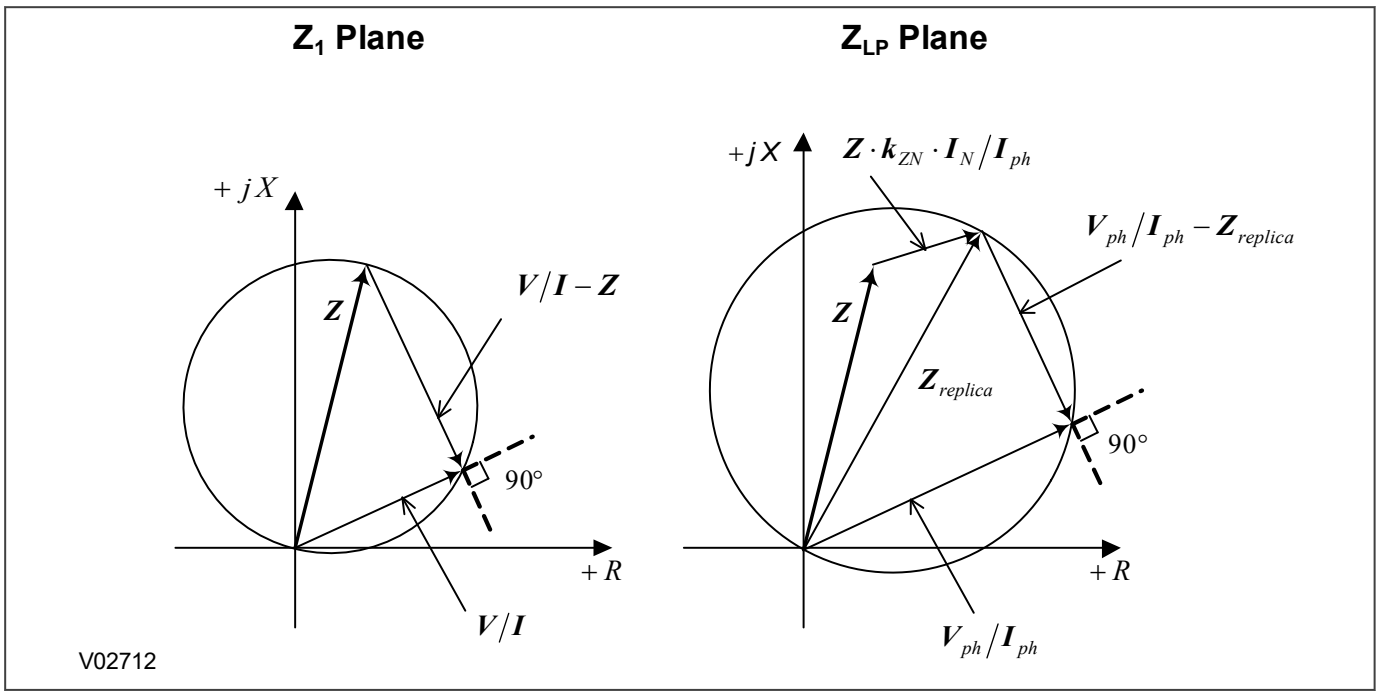


Figure 67: Directional Mho element construction - impedance domain

The two signals provided to the comparator are:

$S_1 = V$

$S_2 = V - IZ$

where (for an A-N fault for example) with residual compensation applied:

$V = V_A$

$I = I_A + k_{ZN}.I_N$

where $k_{ZN} = (Z_0 - Z_1) / 3Z_1$ and is defined by two settings: ***kZN Res Comp*** and ***KZN Res Angle***.

and if mutual compensation is applied:

$I = I_A + k_{ZN}.I_N + k_{ZM}.I_M$

where $k_{ZM} = 3Z_M / 3Z_1$ and is defined by two settings: ***kZm Mutual Set*** and ***kZm Mutual Angle***.

Operation occurs when the angle between the signals is greater than 90°.

To obtain a Z_{LP}-plane representation in the directional Mho element construction, V is replaced with V_{ph} and I is replaced with $I_{ph} + k_{ZN}.I_N$, where V_{ph} and I_{ph} are the faulty phase voltage and current respectively (assuming no mutual current compensation).

The two signals provided to the comparator in this case are:

$S_1 = V_{ph}$

$S_2 = V_{ph} - I_{ph}.Z(1+k_{ZN}.I_N/I_{ph})$

We can define a replica impedance reach, $Z_{replica}$, as:

$Z_{replica} = Z(1+k_{ZN}.I_N/I_{ph})$

or if mutual compensation is applied:

$$Z(1+k_{ZN}.I_N/I_{ph}+k_{ZM}.I_M/I_{ph})$$

Then if healthy phase currents are much less then the current of the faulty phase and the mutual compensation is disabled:

$$I_N \cong I_{ph}$$

so that

$$Z_{replica} \cong Z(1 + k_{ZN})$$

Thus the Z_{LP} plane representation of the characteristic becomes static.

8.3.1.4 OFFSET MHO CHARACTERISTIC FOR EARTH FAULTS

The diagram below illustrates how the Offset Mho characteristic for earth-fault distance protection is created in the impedance domain.

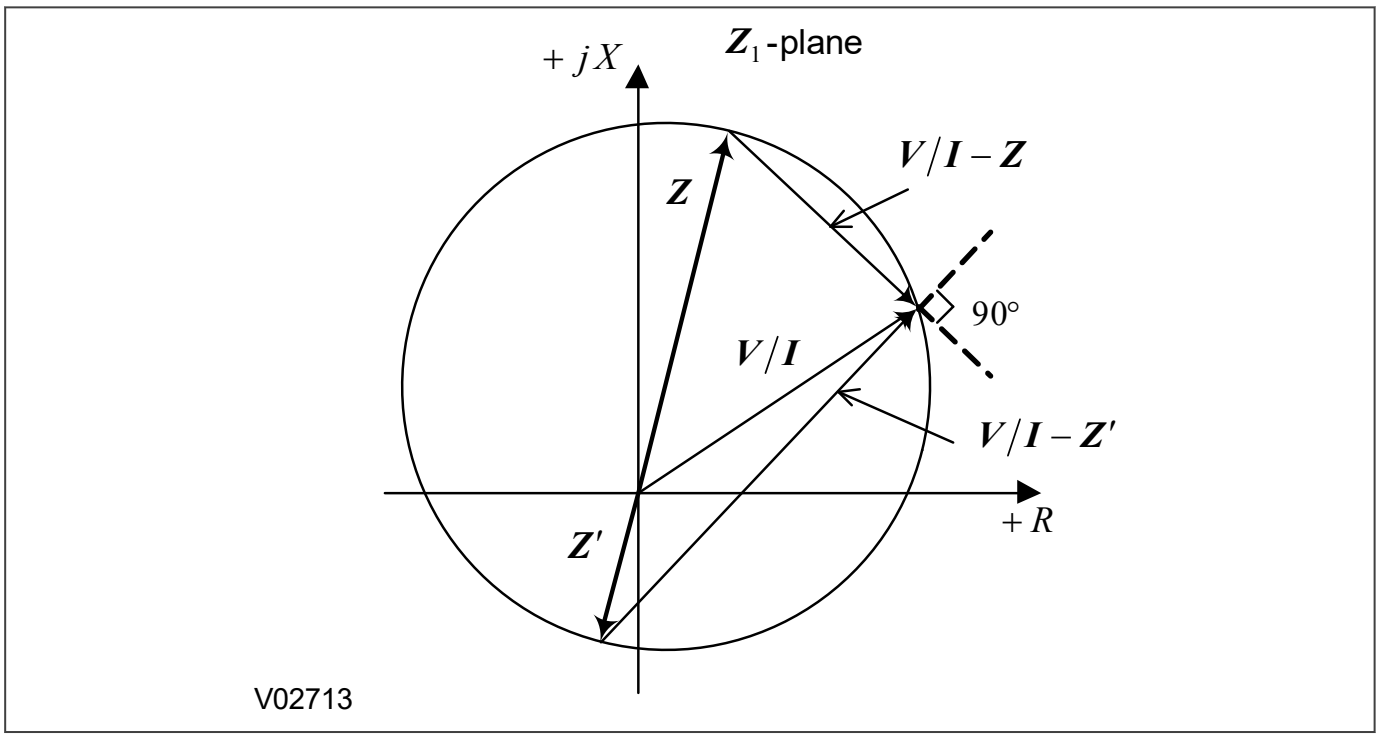


Figure 68: Offset Mho characteristics - impedance domain

The two signals provided to the comparator are:

$$S_1 = V - I.Z'$$

$$S_2 = V - I.Z$$

Operation occurs when the angle between the signals is greater than 90°.

The following diagram below how the Offset Mho characteristic for earth-fault distance protection translates to the loop impedance domain.

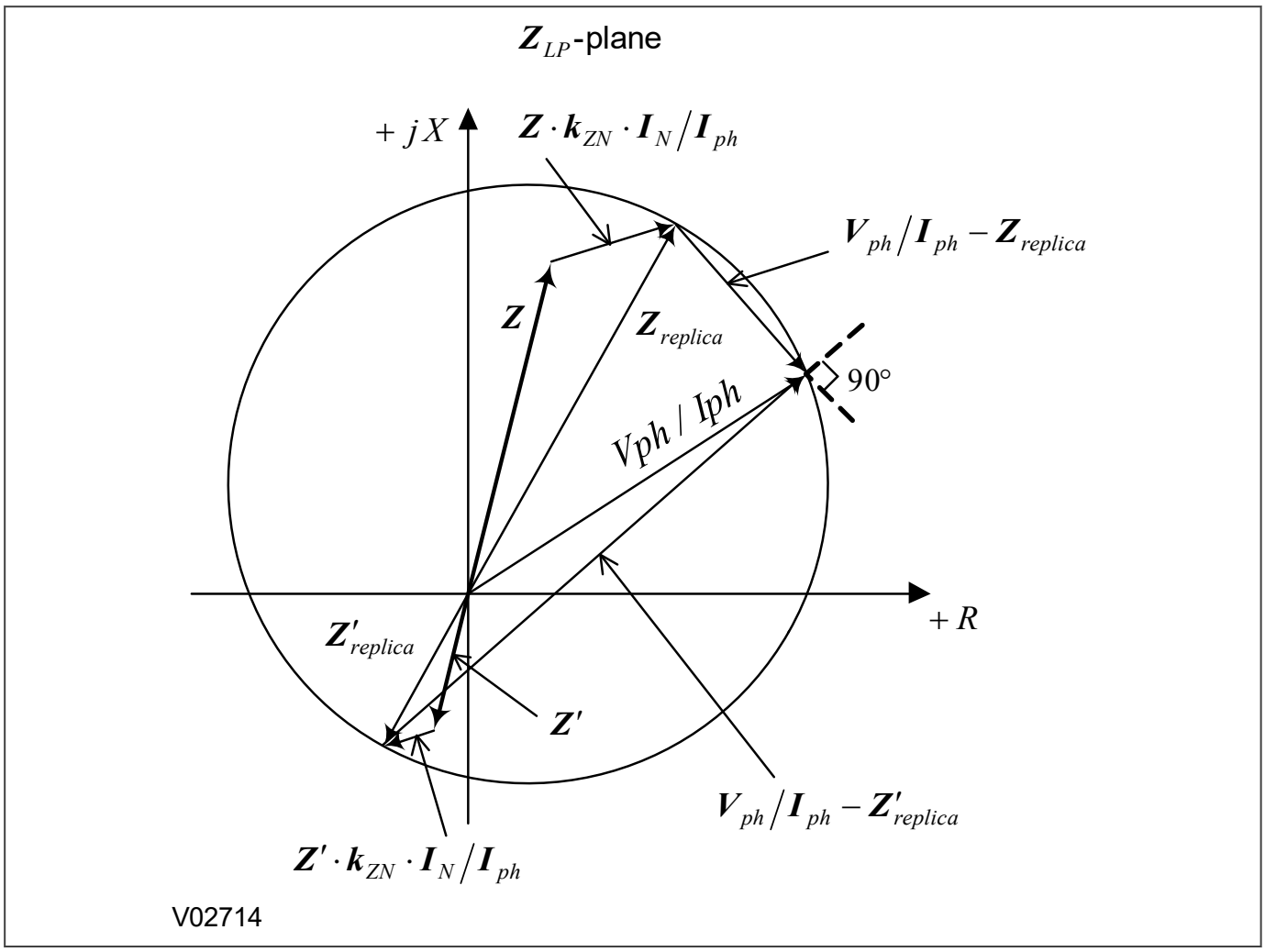


Figure 69: Offset Mho characteristics - voltage domain

where: $Z_{replica}$ is the replica forward reach and $Z'_{replica}$ is the replica reverse reach.

With mutual compensation applied:

$$Z_{replica} = Z(1+k_{ZN}.I_N/I_{ph} + k_{ZM}.I_M/I_{ph})$$

$$Z'_{replica} = Z'(1+k_{ZN}.I_N/I_{ph} + k_{ZM}.I_M/I_{ph})$$

If the healthy phase currents are much less than the current of the faulty phase, then the neutral current is approximately the same as the phase current, and the terms can be simplified as follows:

$$Z_{replica} = Z(1+k_{ZN} + k_{ZM}.I_M/I_{ph})$$

$$Z'_{replica} = Z'(1+k_{ZN} + k_{ZM}.I_M/I_{ph})$$

If the healthy phase currents are much less than the current of the faulty phase, and mutual current compensation is not applied, then these terms can be simplified as follows:

$$Z_{replica} \cong Z(1+k_{ZN})$$

$$Z'_{replica} \cong Z'(1+k_{ZN})$$

So, as with the Directional Self-Polarised Mho characteristic for earth-faults, the Z_{LP} plane representation of the characteristic becomes static.

8.3.1.5 MEMORY POLARISATION OF MHO CHARACTERISTICS

Self-Polarised Directional Mho characteristics require sufficient polarising voltage to detect the voltage angle. Therefore such a characteristic is unable to operate for close-up faults where there would be insufficient polarising voltage. To ensure the correct Mho element response for zero-voltage faults, the protection algorithm adds a percentage of voltage from the memory to the main polarising voltage as a substitute phase reference.

This technique is called memory polarising. Not only does it preserve the directional property of the Mho characteristic, it actually enhances it by dynamically expanding or contracting the characteristic.

Note:
*The **Force No Mem.** DDB may be used to force the relay to work as if the memory time has elapsed, i.e. a combination of self and cross polarisation voltage.*

Note:
*The **Self Pol** DDB indicates when the relay is working with voltage self polarisation.*

8.3.1.6 DYNAMIC MHO EXPANSION AND CONTRACTION

The signals provided to the Mho comparators for memory polarisation are:

$$S_1 = V + pV_{mem}$$

$$S_2 = V - IZ$$

where:

- V is the self-polarisation voltage
- V_{mem} is the memory polarisation voltage

Operation occurs when the angle between the signals is greater than 90°.

The memory voltage V_{mem} is the pre-fault voltage. Assuming the pre-fault current is close to zero at the relaying point, he pre-fault voltage is equal to the source voltage. Therefore:

$$V_{mem} = V_S$$

Dynamic Mho expansion for forward faults

The contribution of additional polarising input creates dynamic Mho expansion for forward faults and increases the fault arc resistance coverage.

Referring to the diagram below:

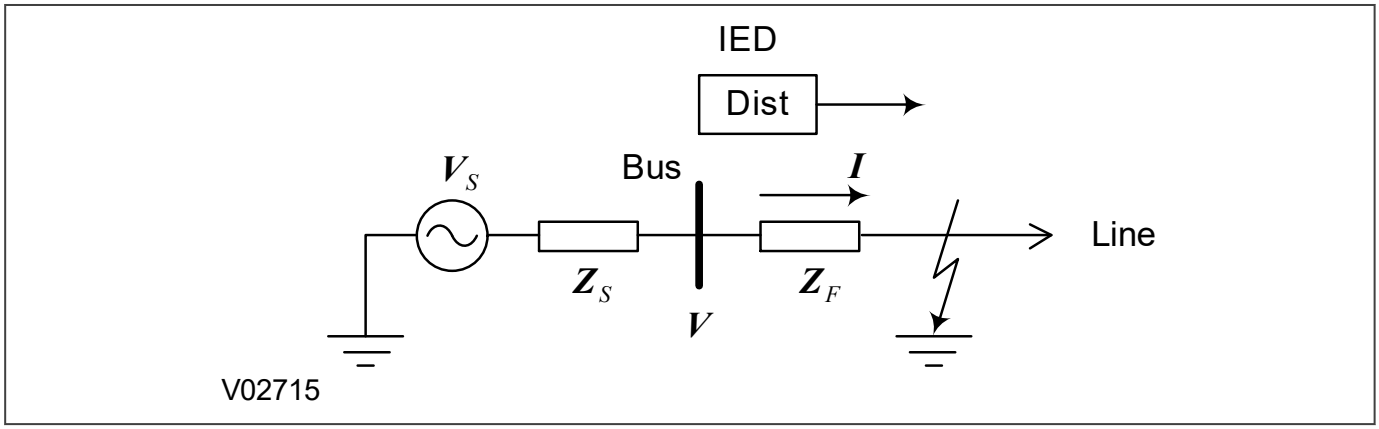


Figure 70: Simplified forward fault

For a fault condition we can write the following equations:

$$V_S = V + I.Z_S$$

$$90° \le \angle\left(V/I + \frac{p}{1+p} \cdot Z_s \right) - \angle\left(V/I - Z\right) \le -90°$$

The Mho expansion for a forward fault is illustrated in the following diagram:

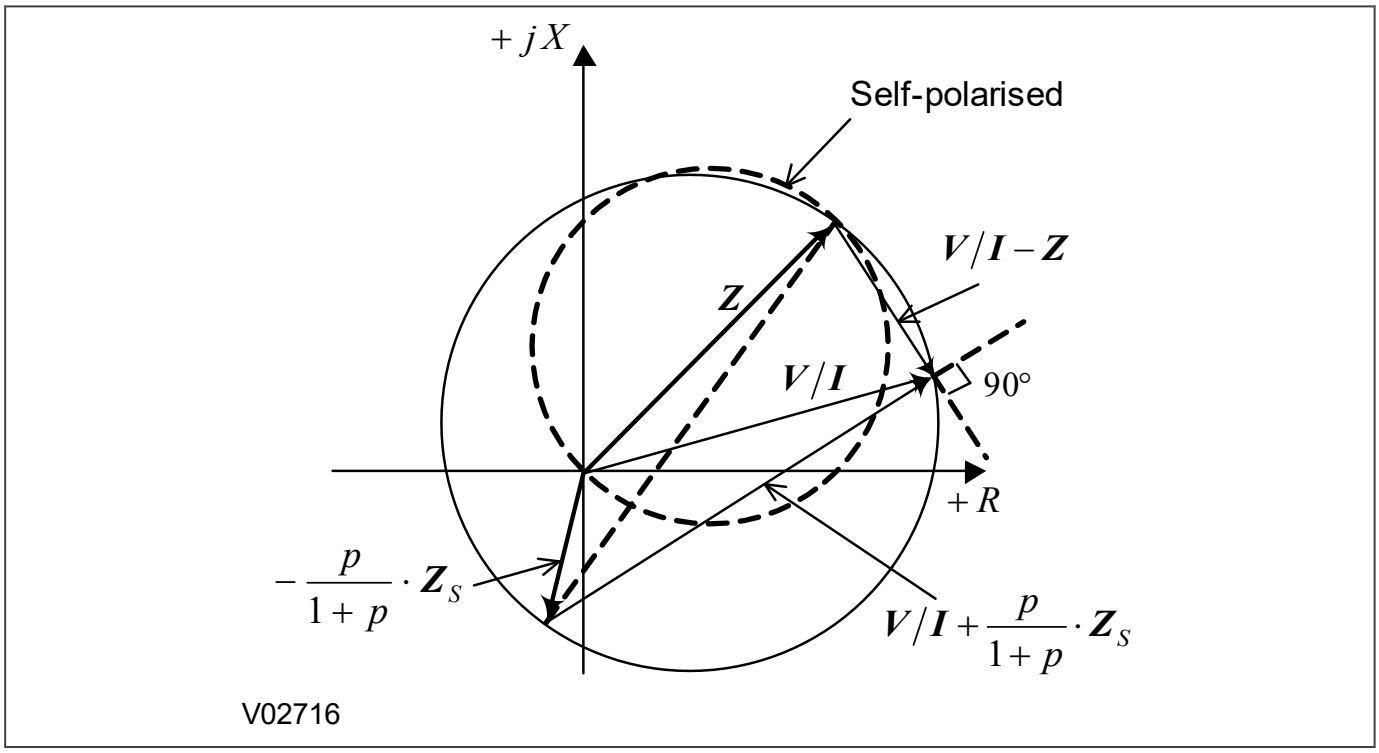


Figure 71: Mho expansion - forward fault

The Mho expansion associated with forward faults is as follows:

$$\text{Mho Expansion} = Z_S.p/(1 + p)$$

where Z_S is the impedance of the source behind the relaying point.

Using the source and line impedances is a simple way of representing the Mho expansion. The protection algorithm does not calculate Z_S internally, it only deals with the signals S_1 and S_2 provided to the Mho comparators. In some cases the source and line impedances are different from their actual values used in various power system studies. This is mainly due to pre-fault current and the residual compensation for phase-to-ground loops. To plot an accurate impedance characteristic, calculate the values of Z_S as follows:

$$Z_S = (V_{mem} - V)/I$$

Dynamic Mho contraction for reverse faults

The contribution of additional polarising input creates dynamic Mho contraction for reverse faults and enhances the directional decision

Referring to the following diagram:

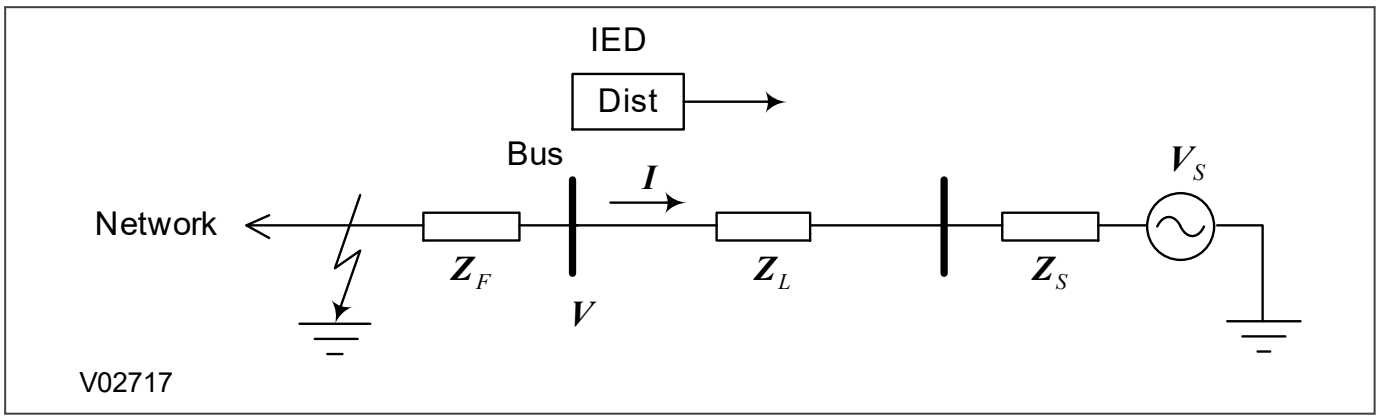


Figure 72: Simplified reverse fault

For a fault condition we can write the following equations:

$$V_S = V - I(Z_S + Z_L)$$

$$90° \le \angle\left(V/I - \frac{p}{1+p} \cdot (Z_S + Z_L) \right) - \angle(V/I - Z) \le -90°$$

The Mho contraction for a reverse fault is illustrated in the following diagram:

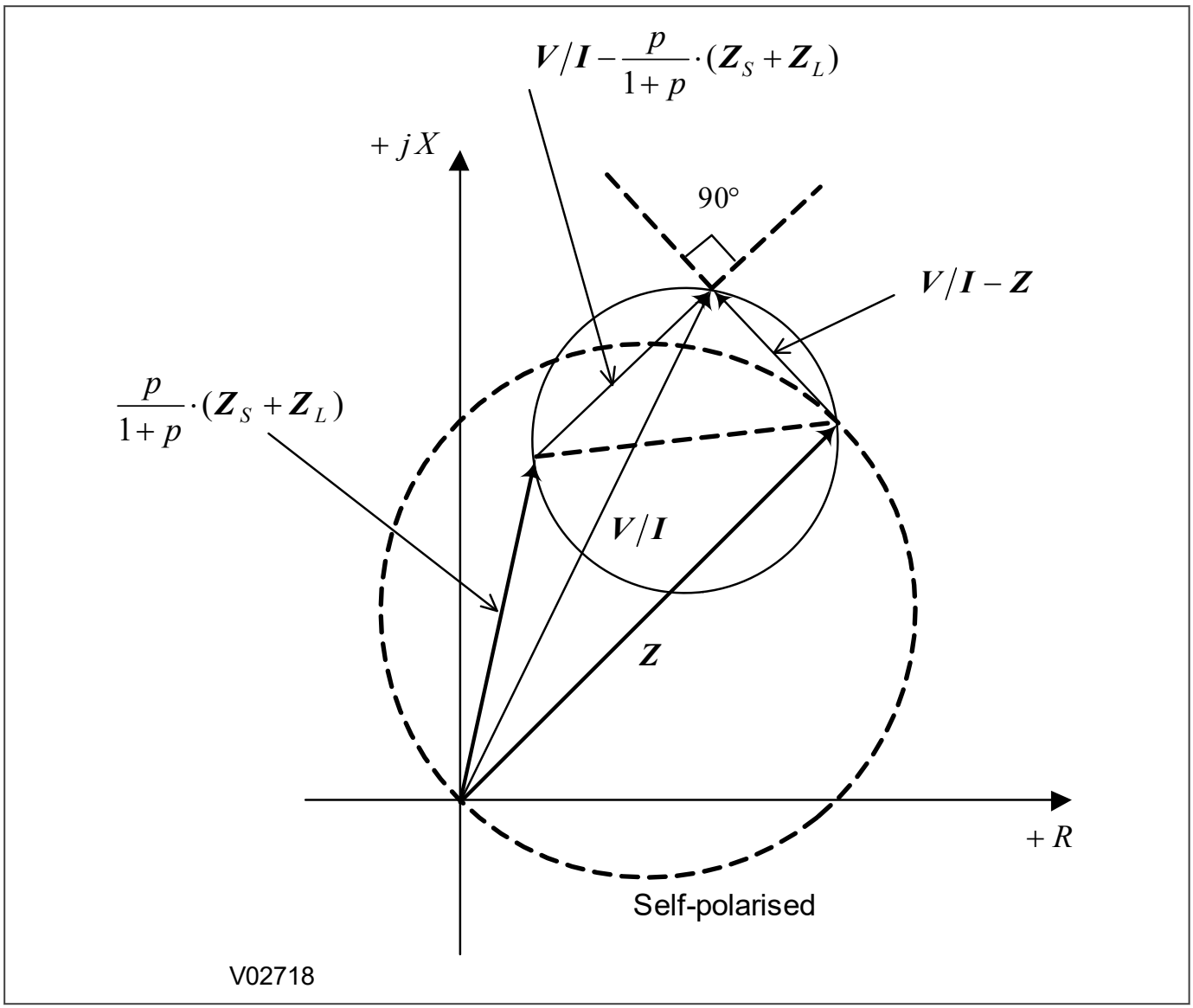


Figure 73: Mho contraction - reverse fault

The Mho contraction associated with reverse faults is as follows:

$$\text{Mho Contraction} = (Z_S + Z_L).p/(1 + p)$$

where $Z_S + Z_L$ is the impedance of the line and the source ahead of the relaying point.

Using the source and line impedances is a simple way of representing the Mho contraction. The protection does not calculate $Z_S + Z_L$ internally, it only deals with the signals S_1 and S_2 provided to the Mho comparators. In some cases the source and line impedances are different from their actual values used in various power system studies. This is mainly due to pre-fault current and the residual compensation for phase-to-ground loops. To plot an accurate impedance characteristic, calculate the values of $Z_S + Z_L$ as follows:

$$Z_S + Z_L = (V - V_{mem})/I$$

8.3.1.7 CROSS POLARISATION OF MHO CHARACTERISTICS

If the voltage collapses on a faulted phase, it may be possible to use healthy phase voltage components to derive a polarising signal to make the directional decision. This process is called cross-polarisation.

The cross-polarisation voltage is generated using phase(s) not otherwise used for the particular distance or directional measurement. While one pole is dead, and the memory is not available, the elements associated with the remaining phases are polarised as shown in the following table:

Loop	Cross Polarising Signal (No Poles Dead)	Cross Polarising if a Pole is Dead
A-N	$0.5(\alpha VB + \alpha^2 VC)$	αVB if C pole is dead or $\alpha^2 VC$ if B pole is dead
B-N	$0.5(\alpha VC + \alpha^2 VA)$	αVC if A pole is dead or $\alpha^2 VA$ if C pole is dead
C-N	$0.5(\alpha VA + \alpha^2 VB)$	αVA if B pole is dead or $\alpha^2 VB$ if A pole is dead
A-B	$\sqrt{3}VC \angle -90°$	0
B-C	$\sqrt{3}VA \angle -90°$	0
C-A	$\sqrt{3}VB \angle -90°$	0

Where α is a mathematical operator which rotates a vector through 120° and α^2 denotes a rotation of 240°.

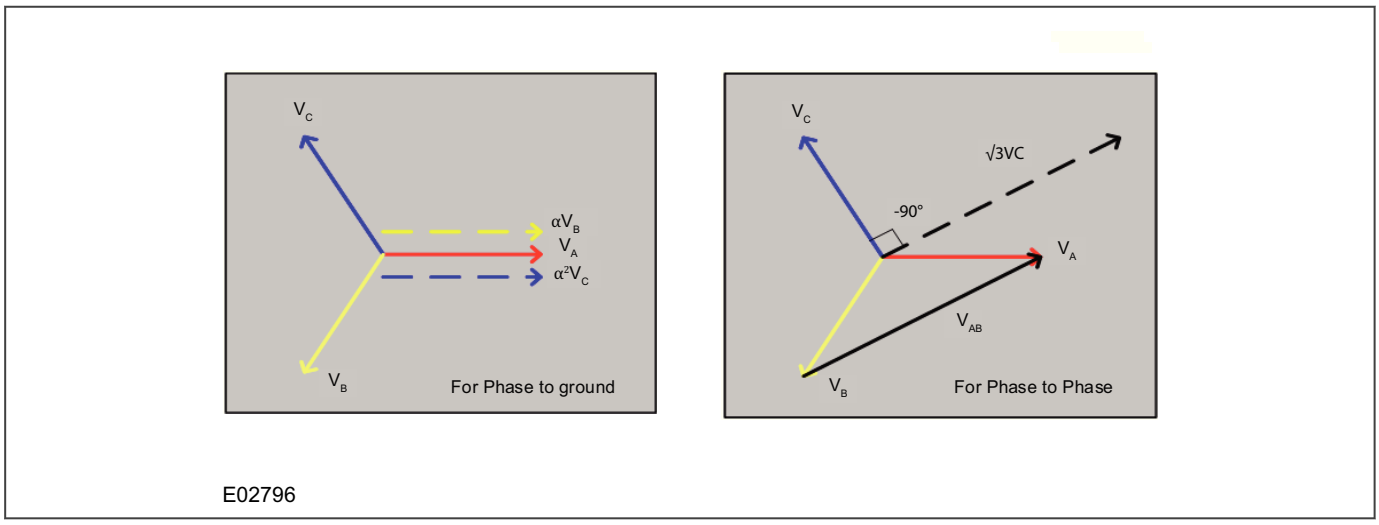


Figure 74: Cross polarising voltage for phase to ground and phase to phase faults

The table and diagram shows polarising signal contributions for each loop under the different operating conditions. The proportion of cross-polarisation voltage used is defined by the ***Dist. Polarizing*** (p) setting.

Note:
Cross polarisation is used only when there is no memory polarisation quantity available.

8.3.1.8 IMPLEMENTATION OF MHO POLARISATION

This product does not allow the directional Mho characteristics to be purely self-polarised or purely memory-polarised. The polarising voltage always contains the directly measured self-polarised voltage, onto which a percentage of the pre-fault memory voltage is added.

Note:
If no memory voltage is available or ***Force No Mem.*** *is set, then the cross-polarised quantity is used instead.*

The setting ***Dist. Polarizing*** (p) defines the amount of memory polarisation (or if need be, cross polarisation voltage), which should be added with respect to the existing self-polarising voltage so that:

$$S_1 = V + pV_{mem}.$$

The value "p" can be set from 0.2 (20%) to 5 (500%).

This will have an affect on the characteristic where operation occurs when the fault impedance lies inside a circle whose diameter is set by the points IZ and $p/(1+p)IZ_{source}$

This means for example:

- If p = 1, the characteristic will have an expansion of 50% $I_{Zsource}$
- If p = 5, the characteristic will have an expansion of 83.3% $I_{Zsource}$

The memory algorithm works as follows:

1. Memory voltage is stored for two cycles after line energisation, whereafter the voltage signals are considered valid and stored in the voltage memory buffers. The voltage memory used for polarising is taken from a buffer corresponding to a value taken two cycles previously, so the voltage memory can be used after four cycles following line energisation.
2. Following fault inception, voltage signals buffered in the polarising memory can be recycled and re-used for a period set with the ***Mem Volt Dura*** setting. This can be set between 16 and 32 cycles.
3. If a power swing condition is detected, the voltage memory signal expires after a reduced period of 3.2 cycles.
4. If the fault is cleared before the voltage memory signal expires, the memory algorithm resets and restarts the two/four cycle validation process.
5. If there is no voltage memory available (either because the line has just been energised, or because the memory voltage has expired), cross polarisation is used instead. The contribution of cross polarising signals is only used when memory polarising is invalid and is only valid for certain pole dead conditions.
6. If neither memory polarisation voltage nor cross-polarisation voltage is available (pole dead condition for phase-to-phase element), then the phase-to-phase elements are self polarised. If the polarising voltage is less than 1V, only zone 1 is allowed to operate. In this case a Mho characteristic with a reverse offset of 25% is applied. This ensures operation when closing on to a close-up three-phase fault (SOTF/ TOR condition).

One of the additional benefits of adding memory into the polarising mix is that Mho characteristics offer dynamic expansion if there is a forward fault, therefore covering greater fault arc resistance

8.4 QUADRILATERAL CHARACTERISTIC

A number of zones are provided to make up the Quadrilateral characteristics. The following diagram shows examples of Directional Forward, Directional Reverse, and Offset zones:

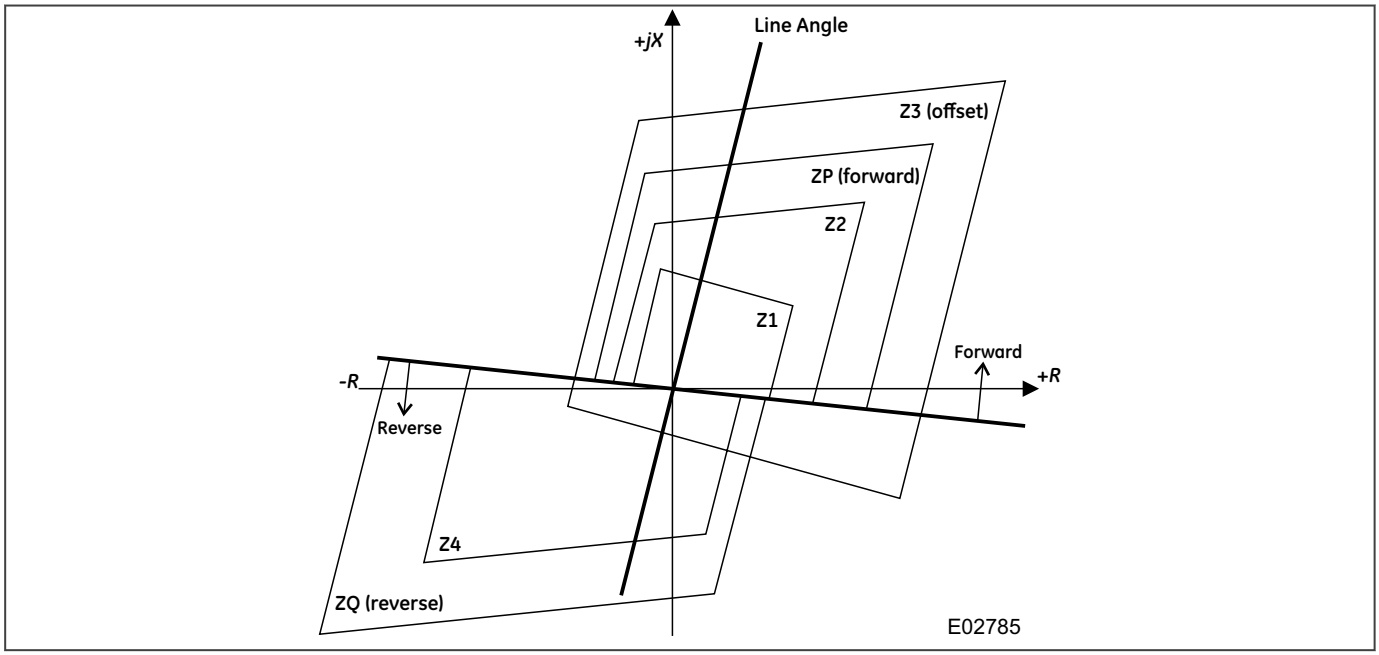


Figure 75: Simplified quadrilateral characteristics

Programmable zones (zone P and Q) are also available. Similar to Zone 3, the programmable zones can be configured as Offset, Directional Forward, or Directional Reverse.

A combination of simple comparators, each using signals derived from measured currents and voltages, determines whether measured impedance is within a tripping zone. A separate comparator is used for each line of each Quadrilateral.

Each tripping zone is constructed from a Quadrilateral based on that depicted in the following diagram:

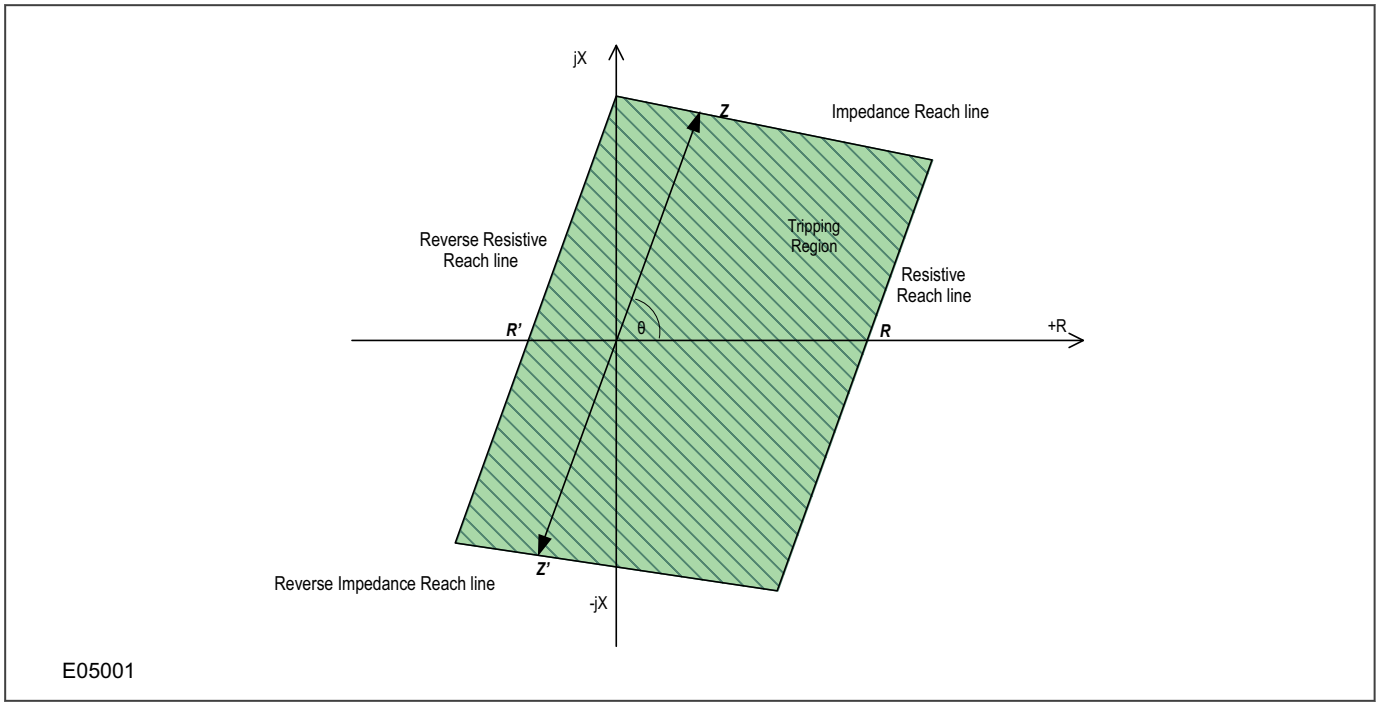


Figure 76: General quadrilateral characteristic limits

In the figure, an Offset Quadrilateral characteristic is defined by its Impedance Reach, Z, (and Reverse Impedance Reach, Z'), its Resistive Reach, R, (and Reverse Resistive Reach, R'), and the zone angle (θ).

The two near-horizontal lines (Impedance Reach Line and Reverse Impedance Reach Line) set the reactive impedance limits of the tripping zone. The two near-vertical lines (Resistive Reach Line and Reverse Resistive Reach Line) set the resistive impedance limits.

The Resistive Reach Lines (also called Resistive Blinders) are parallel and set at the angle of the zone's characteristic impedance.

The Impedance Reach Lines exhibit a characteristic tilt (slope). A line that tilts to reduce the reactive reach (negative tilt/tilt down) encourages underreaching; A line that tilts to increase the reactive reach (positive tilt/tilt up) encourages overreaching. The tilt can be used to reinforce the overreaching/underreaching requirements of the zone. For example, for an underreaching Forward zone, a negative tilt will ensure that the measurement continues to underreach, even with increasing fault resistance.

The Impedance Reach, Z, and the Resistive Reach, R, apply in the context of the direction of the protection. For a Forward Zone, or an Offset Zone, Z and R look into the protected plant. For a Reverse Zone, Z and R look behind the protected plant. Reactive Line tilts follow the same convention.

8.4.1 DIRECTIONAL QUADRILATERALS

A Directional Line overlaid onto an Offset characteristic is used to create a Directional one as shown in the following figure:

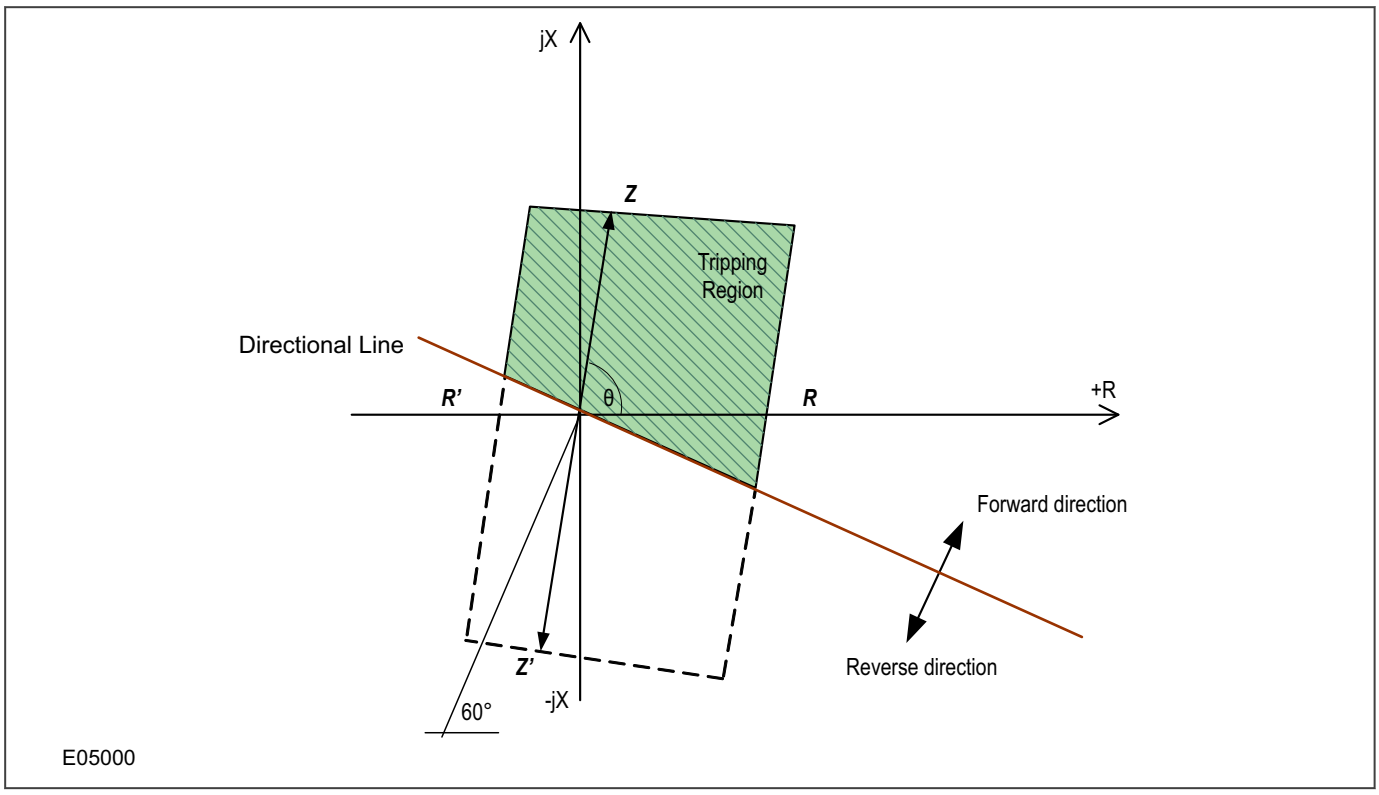


Figure 77: Directional quadrilateral characteristic

This product has a Delta Directional element that is normally used to directionalise the Distance protection.

By default, the Delta Directional element is enabled (***Dir. Status*** in *DELTADIRECTIONAL* set to `Enabled`). In this case, the Directional Line for the Quadrilateral is derived using superimposed fault-current (Delta I). When using the Delta Directional element, the Directional Line angle has a default value of 60º, but you can change it with the ***Dir. Char Angle*** setting.

If you want to use a conventional directional technique, then you can do this by disabling the Delta Directional element. The protection will then use a conventional directional element with a fixed angle of 60º. If the conventional directional decision is used, the directional elements are polarised by a mix of self (actual) and memory voltage. The polarising voltage always contains self-polarised voltage and a percentage of the pre-fault memory voltage. The setting ***Dist. Polarizing*** varies from `0.2` (20%) to `5` (500%) and defines the proportion between self-polarising voltage and memory-polarising voltage used for the directional voltage polarisation as follows:

V polarising = Vself-polariszing/***Dist. Polarizing*** + V memory-polarising

As it can be seen from the formula, the higher the setting ***Dist. Polarizing***, the higher the value of memory-polarising voltage used.

Once the memory expires, the value of V memory-polarising is replaced by V cross-polarising cross as shown in the following table:

Loop	Cross Polarising Signal (No Poles Dead)	Cross Polarising if a Pole is Dead
A-N	$0.5(\alpha VB + \alpha^2 VC)$	αVB if C pole is dead or $\alpha^2 VC$ if B pole is dead
B-N	$0.5(\alpha VC + \alpha^2 VA)$	αVC if A pole is dead or $\alpha^2 VA$ if C pole is dead
C-N	$0.5(\alpha VA + \alpha^2 VB)$	αVA if B pole is dead or $\alpha^2 VC$ if A pole is dead
A-B	$\sqrt{3}VC \angle -90º$	0
B-C	$\sqrt{3}VA \angle -90º$	0
C-A	$\sqrt{3}VB \angle -90º$	0

Where α is a mathematical operator which rotates a vector through 120° and α^2 denotes a rotation of 240°.

If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Disabled`, we recommend a setting of `1` for correct directionality in typical applications.

The relay has the facility to deter the use of memory, with the ***Force No Mem.*** DDB. This DDB forces the relay to work without voltage memory polarisation, making it operate as if the voltage memory timer ***Mem Volt Dura*** has expired.

The following figure illustrates two Offset zones that have been converted into Directional Forward zones by the overlay of a Directional Line. An Offset zone is also shown for reference.

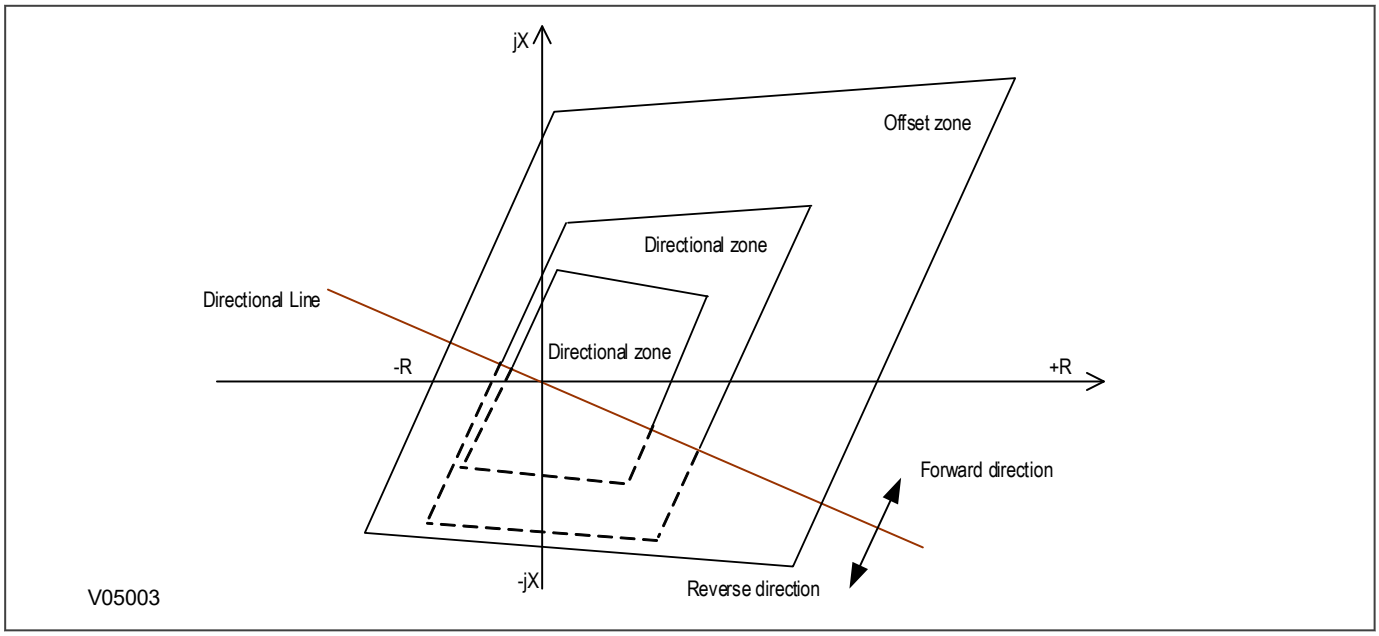


Figure 78: Quadrilateral characteristic featuring 2 directional forward zones and 1 offset zone

Directional quadrilateral limits

The implementation of Directional Quadrilaterals in this product produces Directional Zone characteristics that are formed by the combination of five comparators. Each comparator produces a straight line on the complex impedance plane. The lines produced are:

- Impedance Reach Line
- Reverse Impedance Reach Line
- Resistance Reach Line
- Reverse Resistance Reach Line
- Directional Line.

Each of the lines produced by the comparators defines a tripping limit: Impedance on one side of the line prevents tripping whereas impedance on the other side of the line may, if the other comparators agree, allow tripping. For example, impedance beyond the Impedance Reach Line will not allow tripping.

The combination of the comparator outputs produces a polygon shaped tripping region. The polygon may be either 4-sided or 5-sided. The shape depends according to the settings that are applied by the five comparators and how the Directional Line interacts with the reach lines (usually the Reverse Impedance Reach Line):

- The Directional Line may completely mask a reach line. If that is the case, the polygon will be 4-sided (quadrilateral).
- If the Directional Line intersects a reach line, the polygon will be 5-sided.

Creation of a 5-sided polygon is illustrated in the following figure:

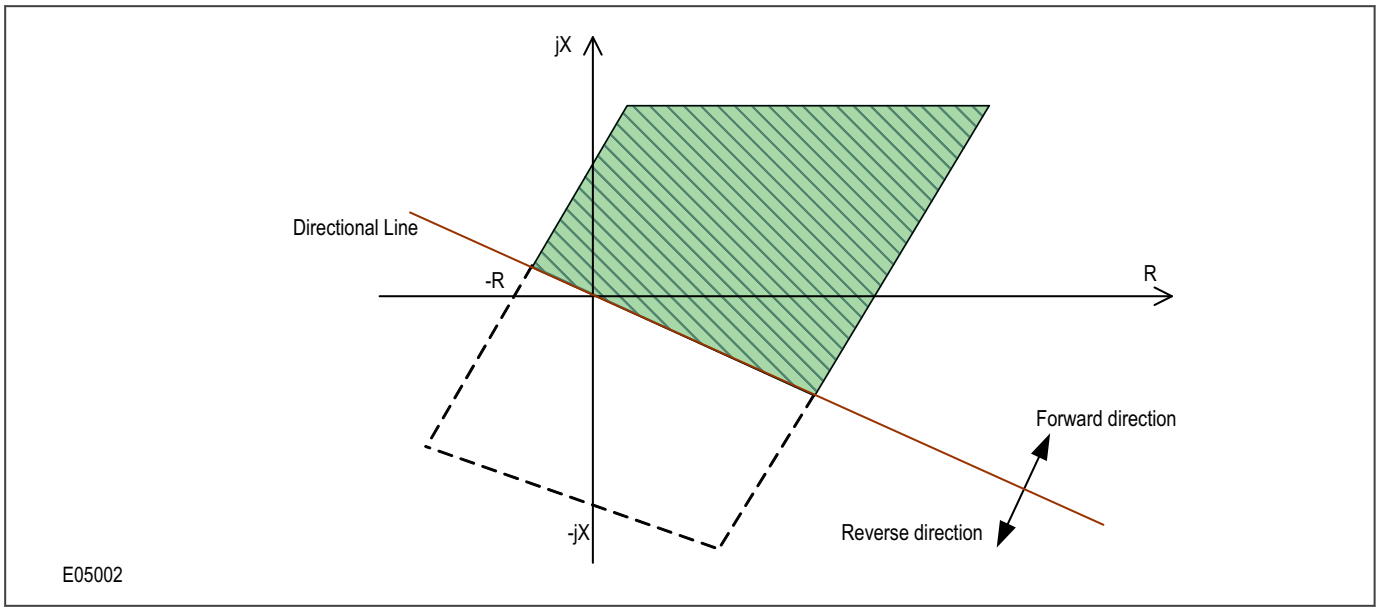


Figure 79: Five-sided polygon formed by quadrilateral characteristic with directional-line intersection of reverse impedance reach line

The applied settings will determine the intersection point. When the settings have been chosen, the following values will affect the line intersection point:

- Impedance Reach
- Reverse Impedance Reach
- Resistive Reach
- Reverse Resistive Reach
- Directional Line Angle
- Zone Characteristic Impedance Angle
- Tilt Angles of Impedance Reach Lines

The Impedance Reach, the Resistive Reach, and the Zone Characteristic Impedance Angle, can be freely assigned. The Directional Line Angle is 60º by default but can be varied if the Delta Directional element is enabled. The Tilt Angle of the impedance lines has a default setting of -3º, but some variation is allowed if the Advanced setting option is chosen.

The Reverse Impedance Reach, and the Reverse Resistive Reach are applied as a fixed ratio of the Impedance Reach and the Resistive Reach for Directional characteristics. The ratios used vary according to the zone type. The following tables present the different values for phase-phase characteristics and phase-earth characteristics. For completion, the reach limit values for Offset zones are also included (although the overlaid Directional line does not apply and the Offset characteristics will always be quadrilateral).

Phase-to-phase element reaches

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
1 Ph-Ph	Forward or Reverse	Z1 Ph. Reach	Z1	½*R1 Ph. Resistive	0.25 R
1 Ph-Ph	Rev Reach Series Comp.	Z1 Ph. Reach	Z1' Ph Rev Reach	½*R1 Ph. Resistive	½*R1' Ph Res. Rev
2 Ph-Ph	Forward or Reverse	Z2 Ph. Reach	Z2	½*R2 Ph. Resistive	0.25 R
2 Ph-Ph	Offset*	Z2 Ph. Reach	Z2' Ph Rev Reach	½*R3 Ph. Resistive	½*R2' Ph Res. Rev.

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
3 Ph-Ph	Forward or Reverse	Z3 Ph. Reach	Z3	½*R3 Ph. Resistive	0.25 R
3 Ph-Ph	Offset*	Z3 Ph. Reach	Z3' Ph Rev Reach	½*R3 Ph. Resistive	½*R3' Ph Res. Rev.
4 Ph-Ph	Reverse or Forward	Z4 Ph. Reach	Z4	½*R4 Ph. Resistive	0.25 R
P Ph-Ph	Forward or Reverse	ZP Ph. Reach	ZP	½*RP Ph Resistive	0.25 R
P Ph-Ph	Offset*	ZP Ph. Reach	ZP' Ph Rev Reach	½*RP Ph Resistive	½*RP' Ph. Res. Rev.
Q Ph-Ph	Forward or Reverse	ZQ Ph. Reach	ZQ	½*RQ Ph Resistive	0.25 R
Q Ph-Ph	Offset*	ZQ Ph. Reach	ZQ' Ph Rev Reach	½*RQ Ph Resistive	½*RQ' Ph. Res. Rev.
1e Ph-Ph	Forward or Reverse	Z1e Ph. Reach	Z1e	½*R1e Ph. Resistive	0.25 R
1e Ph-Ph	Rev Reach Series Comp.	Z1e Ph. Reach	Z1e' Ph Rev Reach	½*R1e Ph. Resistive	½*R1e' Ph Res. Rev
R Ph-Ph	Forward or Reverse	ZR Ph. Reach	ZR	½*RR Ph Resistive	0.25 R
R Ph-Ph	Offset*	ZR Ph. Reach	ZR' Ph Rev Reach	½*RR Ph Resistive	½*RR' Ph. Res. Rev.
S Ph-Ph	Forward or Reverse	ZS Ph. Reach	ZS	½*RS Ph Resistive	0.25 R
S Ph-Ph	Offset*	ZS Ph. Reach	ZS' Ph Rev Reach	½*RS Ph Resistive	½*RS' Ph. Res. Rev.

Phase-to-earth element reaches

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
1 Ph-Earth	Forward or Reverse	Z1 Gnd. Reach * (1 + k_{ZN})	Z1	R1 Gnd Resistive	0.25 R
1 Ph-Earth	Rev Reach Series Comp.	Z1 Gnd. Reach * (1 + k_{ZN})	Z1 Gnd Rev Rch * (1 + k_{ZN})	R1 Gnd Resistive	R1' Ph Res. Rev
2 Ph-Earth	Forward or Reverse	Z2 Gnd. Reach * (1 + k_{ZN})	Z2	R2 Gnd Resistive	0.25 R
2 Ph-Earth	Offset*	Z2 Gnd. Reach * (1 + k_{ZN})	Z2' Gnd Rev Rch * (1 + k_{ZN})	R3 Gnd Resistive	R2' Ph Res. Rev
3 Ph-Earth	Forward or Reverse	Z3 Gnd. Reach * (1 + k_{ZN})	Z3	R3 Gnd Resistive	0.25 R
3 Ph-Earth	Offset*	Z3 Gnd. Reach * (1 + k_{ZN})	Z3' Gnd Rev Rch * (1 + k_{ZN})	R3 Gnd Resistive	R3' Ph Res. Rev
4 Ph-Earth	Reverse or Forward	Z4 Gnd. Reach * (1 + k_{ZN})	Z4	R4 Gnd Resistive	0.25 R
P Ph-Earth	Forward or Reverse	ZP Gnd. Reach * (1 + k_{ZN})	ZP	RP Gnd Resistive	0.25 R
P Ph-Earth	Offset*	ZP Gnd. Reach * (1 + k_{ZN})	ZP' Gnd Rev Rch * (1 + k_{ZN})	RP Gnd Resistive	RP' Gnd Res. Rev
Q Ph-Earth	Forward or Reverse	ZQ Gnd. Reach * (1 + k_{ZN})	ZQ	RQ Gnd Resistive	0.25 R
Q Ph-Earth	Offset*	ZQ Gnd. Reach * (1 + k_{ZN})	ZQ' Gnd Rev Rch * (1 + k_{ZN})	RQ Gnd Resistive	RQ' Gnd Res. Rev
1e Ph-Earth	Forward or Reverse	Z1e Gnd. Reach * (1 + k_{ZN})	Z1e	R1e Gnd Resistive	0.25 R
1 Ph-Earth	Rev Reach Series Comp.	Z1e Gnd. Reach * (1 + k_{ZN})	Z1e Gnd Rev Rch * (1 + k_{ZN})	R1e Gnd Resistive	R1e' Ph Res. Rev
R Ph-Earth	Forward or Reverse	ZR Gnd. Reach * (1 + k_{ZN})	ZR	RR Gnd Resistive	0.25 R
R Ph-Earth	Offset*	ZR Gnd. Reach * (1 + k_{ZN})	ZR' Gnd Rev Rch * (1 + k_{ZN})	RR Gnd Resistive	RR' Gnd Res. Rev
S Ph-Earth	Forward or Reverse	ZS Gnd. Reach * (1 + k_{ZN})	ZS	RS Gnd Resistive	0.25 R
S Ph-Earth	Offset*	ZS Gnd. Reach * (1 + k_{ZN})	ZS' Gnd Rev Rch * (1 + k_{ZN})	RS Gnd Resistive	RS Gnd Res. Rev

Where $k_{ZN} = (Z_0 - Z_1) / 3Z_1$ and is defined by two settings: ***kZN Res Comp*** and ***KZN Res Angle***.

Note:
This is also the reverse impedance reach, if the* ***Series Comp.* *setting is* `Enabled`.

8.5 EARTH FAULT QUADRILATERAL CHARACTERISTICS

Quadrilateral characteristics are available for earth-fault protection. A mix of Directional Forward, Directional Reverse, and Offset characteristics are available. Zone 1 and Zone 4 are settable as Forward or Reverse. Zones 2, 3, P and Q are settable as Forward or Reverse or Offset. Each zone is independent and is defined by an Impedance Reach line, a Reverse Impedance Reach Line, and two resistive blinders. The two resistive blinders (Resistive Reach Line and Reverse Resistive Reach Line) are parallel to the zone characteristic impedance angle.

The two reactance lines of each Phase-Earth Quadrilateral exhibit a characteristic tilt. The tilts of the Impedance Reach Line and the Reverse Impedance Reach Line are independent. The tilt of both may be fixed. Alternatively, the lines may be allowed to vary the tilt angle according to system conditions (dynamic tilting). If the tilt of the Reverse Impedance Reach Line is fixed, the value is -3º. If the tilt of the Impedance Reach Line is fixed, the value is fixed according to the setting, σ, -(user settable between +/- 30º). To use the dynamic tilting option you must enable it. Enabling the dynamic tilt causes the slope of the reactance lines to deviate from the set values to compensate, automatically, for angular difference between fault current and polarising current.

8.5.1 EARTH FAULT REACTANCE LINES

Both forward and reverse reach reactance lines feature a fixed tilt. For the Impedance Reach line, the fixed tilt can be set to reinforce underreaching or overreaching preferences for the zone. For the Reverse Impedance Reach line, the fixed tilt is preset at -3º.

The tilting of the reactance lines can be set such that tilting will be affected by the choice of polarising quantity. If dynamic tilting is selected, the protection automatically chooses the best polarising quantity from either the phase current or negative sequence current. The choice depends on which line is being polarised and on the relationship of measured currents I2 and Iph. When I2 is used as the polarising quantity, the tilt can dynamically vary according to the angle of I2. If Iph is used, the tilt remains fixed at the set angle.

Consider polarisation of the reactance lines for the case of a phase-earth fault:

For a phase-earth fault:

$$V = Vph$$

and assuming that mutual compensation is not applied:

$$I = Iph + k_{ZN}.IN.$$

To avoid overreaching or underreaching due to the voltage drop in the arc resistance, the top line of the characteristic should be ideally tilted by an angle:

$$\angle (I_{fault} / I)$$

So that the total angle of tilt should be:

$$\angle (I_{fault} / I) + \sigma$$

where I_{fault} is the fault current and σ is the fixed tilt of the reactance line (user setting for the Impedance Reach line, fixed -3º preset for the Reverse Impedance Reach line.

If Z is the zone reach setting then the reactance line is formed by phase comparison between an operating signal V – I Z (S1), and a polarising quantity, I_{POL} (S2).

I_{fault} should be used to determine S2, but, because the Distance protection cannot measure the fault current directly (due to the unknown infeed from the remote end), I_{fault} cannot be used as the polarising current. Instead, the angle of I_{fault} must be estimated. Two proven methods to estimate the angle of I_{fault} are:

1. The angle of I_{fault} can be assumed to be close to the angle of Iph
2. The angle of I_{fault} can be assumed to be close to the angle of the negative sequence current I2.

In case 1, the angle of Iph can be used to polarise the Quadrilateral characteristic and so the tilt of the reactance line is fixed.

In case 2 the angle of I2 can be used to polarise the Quadrilateral characteristic. In this case, the reactance line tilt varies dynamically according to the angle of I2.

The reactance line follows the fault resistance impedance and tilts up or down, starting from the set initial tilt angle (σ) to avoid underreaching or overreaching.

For both fixed and dynamic tilting the validity of current polarisation is controlled by the following condition:

$$|\angle \text{I2} - \angle \text{Iph}| < 45^{\circ}$$

If this condition is not fulfilled, the assumptions that the angle of I_{fault} is close to the angle of Iph or close to the angle of I2 cannot be considered valid. Under such conditions the Quadrilateral characteristic could significantly overreach or underreach. To avoid this, the distance protection automatically switches from Quadrilateral to Mho characteristics to provide stable operation.

8.5.2 EARTH FAULT FIXED REACTANCE LINE TILTING

Each zone has an independent setting to set the tilt angle (σ) of the Impedance Reach line of the quadrilateral characteristic. If dynamic tilting is disabled, the characteristic uses this setting to apply a fixed tilt to the top line. The tilting angle is with reference to the fault current I, and is defined by:

$$\text{Tilt angle} = \text{setting } (\sigma) = \angle \text{Iph/I}$$

The setting range is +/- 30°. A negative angle sets a downward tilt and a positive angle sets an upward tilt.

Operation occurs when the operating current I lags the polarising current Iph.

The Impedance Reach line of the characteristic in the Z1 plane is shown in the following diagram:

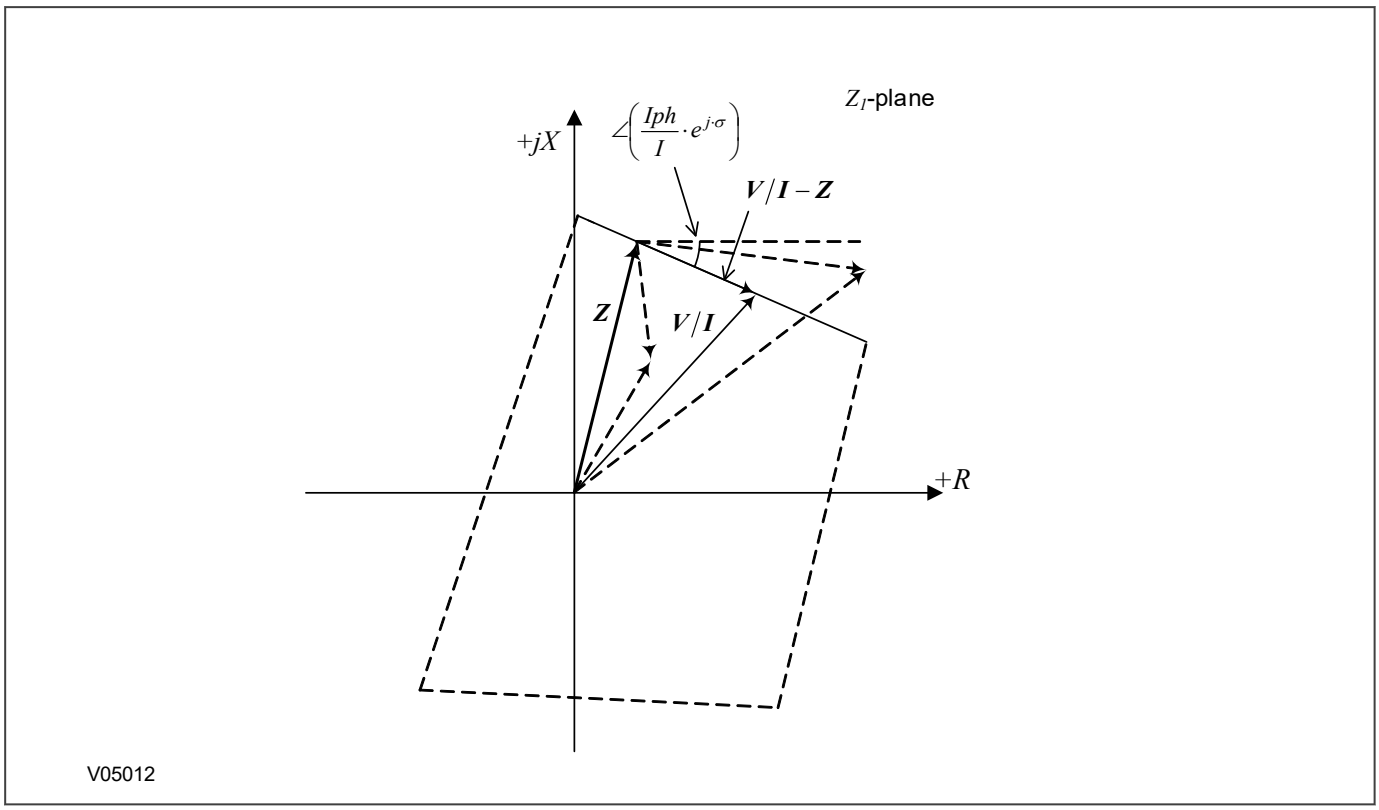


Figure 80: Impedance reach line in Z1 plane

For all V/I vectors below the Impedance Reach line, the following condition is true:

$$\angle (V/I\text{-}Z) \leq \sigma$$

or

$$\angle (V - I.Z) \leq I + \sigma$$

If mutual compensation is not applied, for an earth-fault loop

$$V = Vph$$

and

$$I = Iph + k_{ZN}.IN$$

so the signals fed into comparator are:

$$S1 = Vph - Iph.Z_{replica}$$

$$S2 = Iph \angle \sigma$$

where: $Z_{replica}$ is the replica forward reach

The impedance below the Impedance Reach line is detected when the angle between the signals is less than 0°:

For products that have mutual compensation, if the mutual compensation is applied, then

$$Z_{replica} = Z(1+k_{ZN}.IN/Iph+k_{ZM}.I_M/Iph).$$

The following figure shows the Z_{LP}-plane representation of the characteristic:

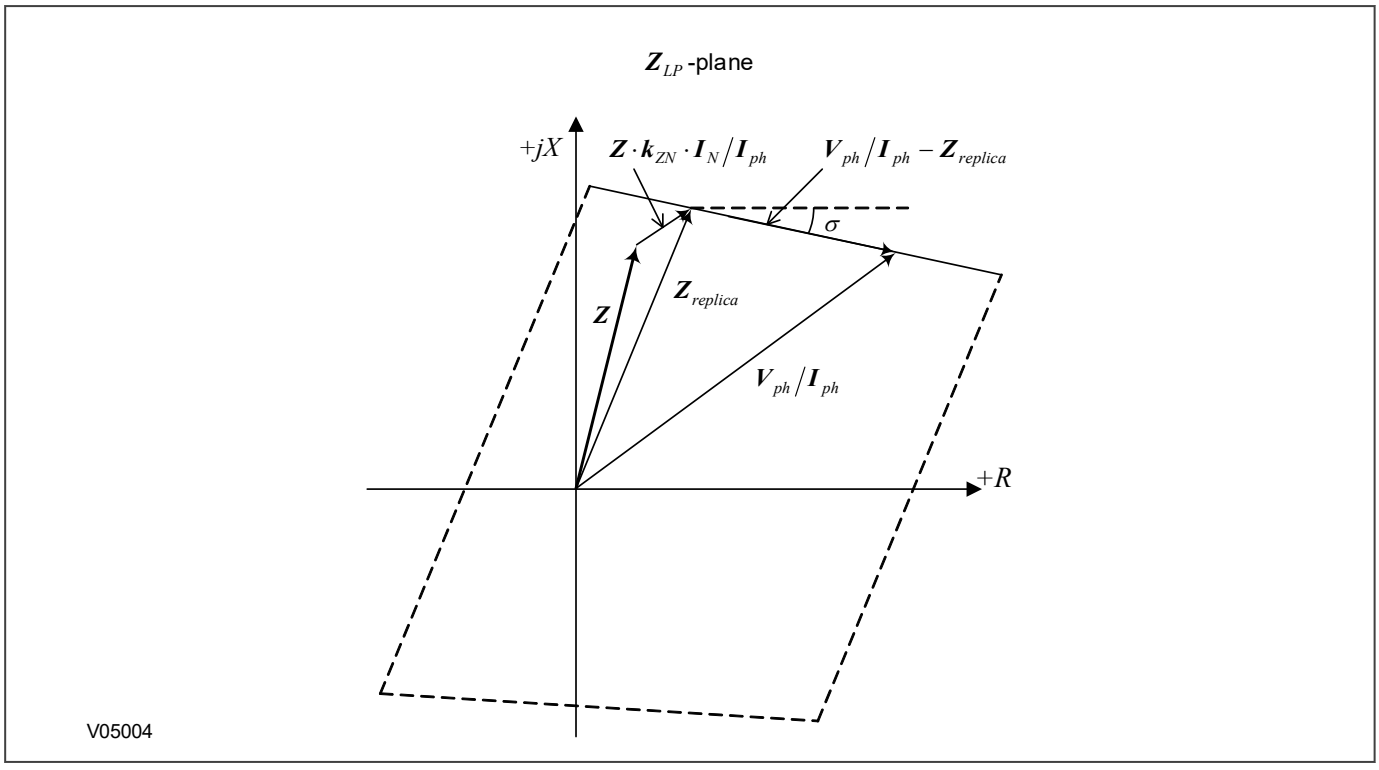


Figure 81: Impedance reach line in Z_{LP} plane

The Impedance Reach line tilting angle in the Z_{LP} plane is fixed at σ (***Zx Tilt Top Line*** setting).

The Impedance Reach line tilting angle in the Z1 plane is defined as follows:

$$\text{Tilt angle} = \angle(Iph/I) + \sigma = \angle(Iph/(Iph + kZ_N.IN)) + \sigma$$

If the healthy phase currents are much less than the current of the faulty phase, then IN ≈ Iph. The tilting angle in this case is fixed at the following value:

$$\text{Tilt angle} = \angle((1/(1 + kZN)) + \sigma$$

For products that have mutual compensation, if the mutual compensation is enabled, the tilting angle is:

$$\text{Tilt angle} = \angle(Iph/(Iph + k_{ZN}.IN + k_{ZM}.I_M)) + \sigma$$

The replica reach $Z_{replica}$ depends on the ratio of IN/Iph. If IN ≈ Iph (and if mutual compensation is not applied) then:

$$Z_{replica} = Z\ (1 + k_{ZN})$$

So the characteristic is static.

The general characteristic in the Z_{LP} plane is shown in the following figure:

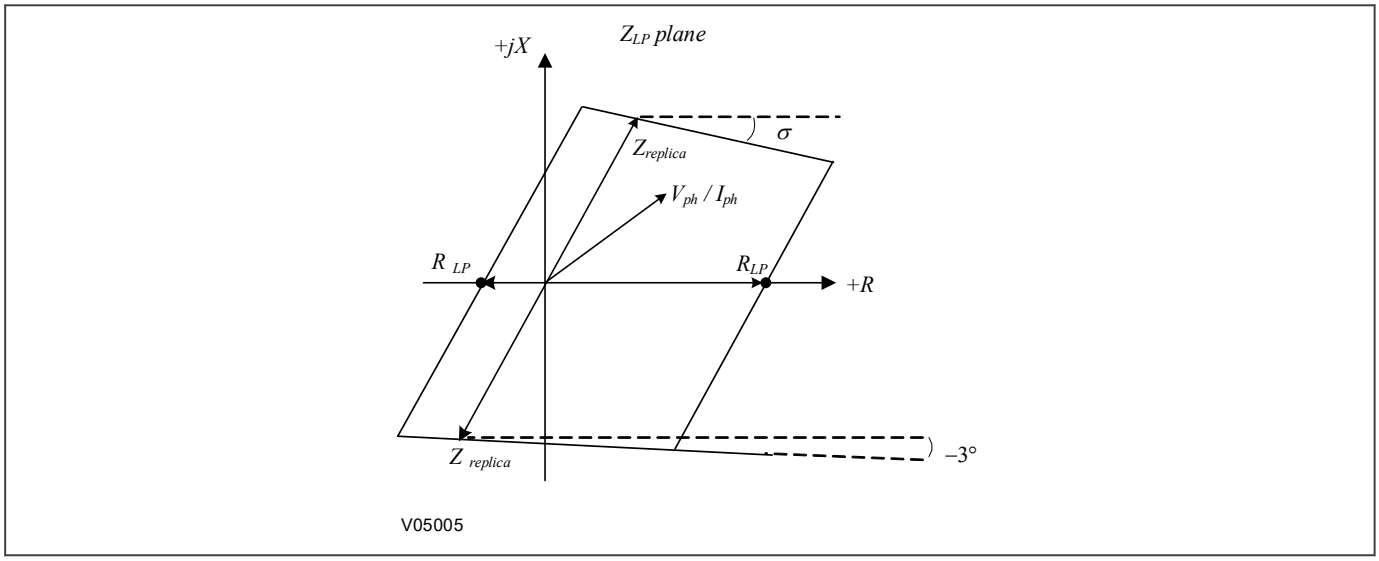


Figure 82: General characteristic in Z_{LP} plane

The comparators used for the reactance lines are as per the following table:

Zone	Line	S1	S2	Condition
Forward or Offset	Impedance Reach	Vph - Iph.Zreplica	Iph∠σ	∠S1 -∠S2 < 0°
Forward or Offset	Reverse Impedance Reach	Vph - Iph.Z'replica	Iph∠-3°	∠S1 -∠S2 > 0°
Reverse	Impedance Reach	Vph + Iph.Zreplica	-Iph∠σ	∠S1 -∠S2 < 0°
Reverse	Reverse Impedance Reach	Vph + Iph.Z'replica	-Iph ∠-3°	∠S1 -∠S2 > 0°

8.5.3 EARTH FAULT DYNAMIC REACTANCE LINE TILTING

If you enable dynamic tilting, the reactance lines of the earth-fault Distance Quadrilateral characteristic can dynamically tilt on the positive sequence impedance (Z1) plane. If the line is polarised with negative sequence current (I2), the total tilt is made up of the difference between the angle of I2 and the angle of the Distance protection current (I), plus the user-settable fixed tilt angle σ:

$$\text{Dynamic Tilt Angle} = \angle(I2 / I) + \sigma$$

The default value of the fixed tilt is -3°. It is introduced to reduce the possibility of overreach caused by any small differences between the negative sequence source impedances, and general CT/VT angle tolerances.

The tilting of Earth-Fault Quadrilateral characteristic reactance lines are constrained to prevent inappropriate excessive tilting according to the following criteria:

- The Zone 1 Impedance Reach line dynamic tilt can only be applied to bring the Resistive Reach end of the line towards the +R-axis. This ensures that Zone 1 does not overreach and maintains grading/selectivity with downstream protection.
- For the other zones (including Zone 1X and Zone 4) the dynamic tilt of the Impedance Reach line can only act in the sense to prevent underreaching. (This is particularly important for zones used to key channel-aided distance schemes).
- For Forward operating zones (except Zone 1) the Impedance Reach line dynamic tilt is applied to tilt the Resistive Reach end of the line away from the +R axis.
- For Reverse operating zones the dynamically tilting line is in the opposite quadrant of the characteristic compared with Forward/Offset Zones and the dynamic tilt moves the line away from the resistive axis.
- For Offset zones, the Impedance Reach lines tilt away from the R-axis, whilst the Reverse Impedance Reach Lines tilt towards the +R axis. This avoids overreaching in the reverse direction.
- For products that feature single-phase tripping, when one circuit breaker pole is open during a single-pole autoreclose sequence, dynamic tilting is automatically disabled. The fault current is used as the polarising signal and a fixed -7° tilt is applied. The additional tilt reduces the possibility of overreach caused by using the faulted phase as the reference.

Note:
The tilting of the zones remains unaltered if the default direction is changed.
Zone 1 always behaves as an underreaching zone regardless of the zone direction.
All other directional zones behave as overreaching zones regardless of zone direction.

Note:
Zone 1X used in Zone 1 Extension Schemes uses the Zone 2 tilt settings to ensure that it does not underreach.

Dynamic tilting of reactance lines only occurs when the line is polarised with I2. If Iph is used as the polarising quantity the tilt of the Impedance Reach line is fixed. If fixed tilting is selected, Iph is always used. If dynamic tilting is enabled, then the protection will decide whether to use I2 or Iph (and hence whether dynamic tilting will apply) according to the angular relationship between I2 and Iph.

The following criteria are applied:

- If the angle between I2 and Iph is more than 45°, the Quadrilateral characteristics are disabled and Mho characteristics are used instead.
- If the angle between I2 and Iph is less than 45°, Leading and lagging polarising currents are allocated according to the phase relations between I2 and Iph as presented in the diagram below:

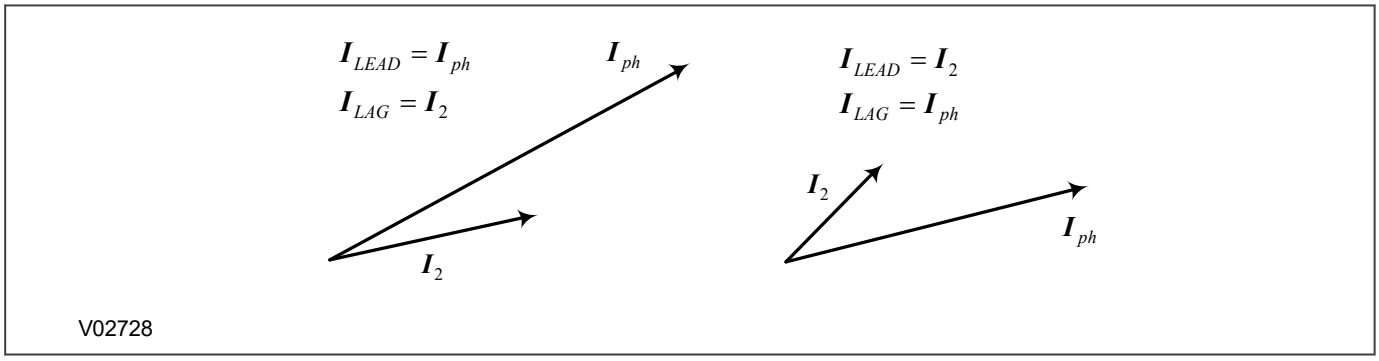


Figure 83: Phase relations between I2 and Iph for leading and lagging polarising currents

The comparators used for the reactance lines are allocated as per the following table:

Zone	Line	S1	S2	Condition
Zone 1	Impedance Reach	Vph - IphZ$_{replica}$	$I_{LAG}\angle\sigma$	$\angle S1 - \angle S2 < 0°$
Zone 1	Reverse Impedance Reach	Vph - IphZ'$_{replica}$	$I_{LAG}\angle -3°$	$\angle S1 - \angle S2 > 0°$
Forward or Offset zones (except Zone 1)	Impedance Reach	Vph - IphZ$_{replica}$	$I_{LEAD}\angle\sigma$	$\angle S1 - \angle S2 < 0°$
Forward or Offset* zones (Zone 1 and Zone 1e, where ***Series Comp.*** is `Enabled`)	Reverse Impedance Reach	Vph - IphZ'$_{replica}$	$I_{LAG}\angle -3°$	$\angle S1 - \angle S2 > 0°$
Reverse	Impedance Reach	Vph + IphZ$_{replica}$	$-I_{LEAD}\angle\sigma$	$\angle S1 - \angle S2 < 0°$
Reverse	Reverse Impedance Reach	Vph + Iph Z'$_{replica}$	$-I_{LAG}\angle -3°$	$\angle S1 - \angle S2 > 0°$

Note:
** This is also the reverse impedance reach, if the **Series Comp.** setting is `Enabled`.*

If I_{LEAD} is I2 the lines are dynamically tilted up from the fixed angle.

If I_{LEAD} is Iph, the fixed tilt applies.

If I_{LAG} is I2, the lines are dynamically tilted down from the fixed angle.

If I_{LAG} is Iph, the fixed tilt applies.

8.5.4 EARTH FAULT RESISTIVE BLINDERS

The Resistive Reach settings are used to select the resistive limits of the Quadrilaterals.

The Earth Fault reach settings are set according to the positive sequence line impedance, so are generally identical to the settings of the Phase Fault elements.

Since the Earth Fault reach settings are set according to the positive sequence line impedances, the relationship between the positive sequence impedances and the earth-fault loop impedances needs to be understood.

Consider the general characteristic in the Z1 plane shown in the following figure:

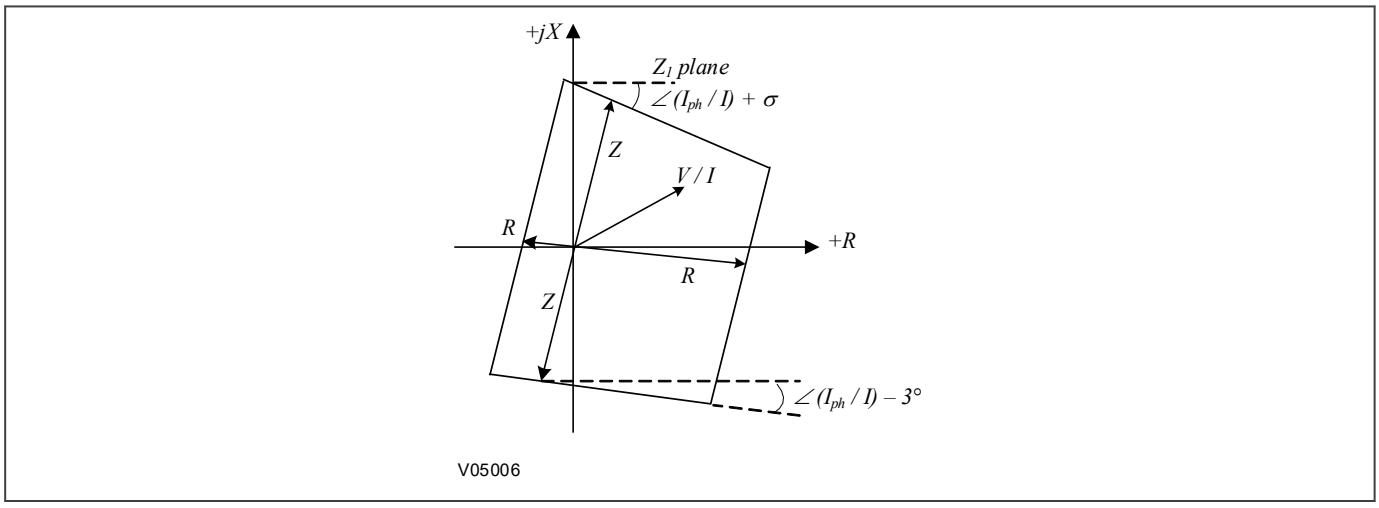


Figure 84: General characteristic in Z1 plane

$$R = R_{LP}\,(Iph/I) \text{ and } R' = R'_{LP}.(Iph/I)$$

$$I = Iph + k_{ZN}.IN$$

For products that have mutual compensation, if the mutual compensation is enabled, then

$$I = Iph + k_{ZN}.IN + k_{ZM}.IM$$

If the healthy phase currents are much less than the current of the faulty phase and the mutual compensation is disabled, then IN ≈ Iph (the faulty phase current) and the characteristic in the Z1 plane is simplified:

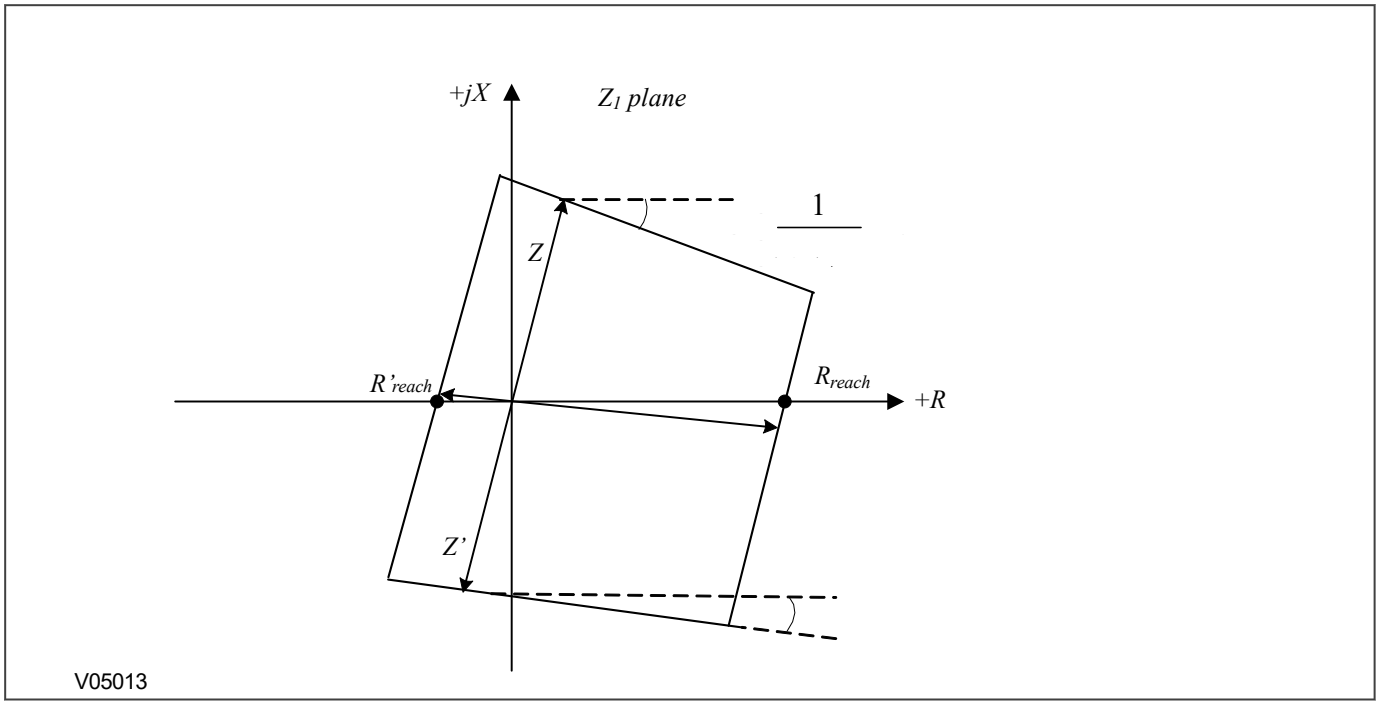


Figure 85: Simplified characteristic in Z1 plane

$$R_{reach} = ((RLP./(1 + k_{ZN})).\sin(Z + \alpha)),$$

$$R'reach = ((R'LP./(1 + k_{ZN})).\sin(Z + \alpha)),$$

where: α is the angle of $1/(1 + k_{ZN})$:

$$\alpha = (1/(1 + k_{ZN}))$$

In typical cases the sine ratio coefficient term is close to unity so the simplified equations can be used:

$$R_{reach} = R_{LP} / | (1 + k_{ZN}) |,$$

$$R'_{reach} = R'_{LP} / | (1 + k_{ZN}) |,$$

So in terms of replica impedances and loop resistances, the comparators used for the resistance lines are as per the following table:

Zone	Line	S1	S2	Condition
Forward or Offset	Resistive reach	$Vph - Iph.R_{LP}$	$Iph.Z_{replica}$	$\angle S1 - \angle S2 > 0°$
Forward or Offset	Reverse resistive reach	$Vph - Iph.R'_{LP}$	$Iph.Z_{replica}$	$\angle S1 - \angle S2 < 0°$
Reverse	Resistive reach	$Vph + Iph.R_{LP}$	$-Iph.Z_{replica}$	$\angle S1 - \angle S2 > 0°$
Reverse	Reverse resistive reach	$Vph + Iph.R'_{LP}$	$-Iph.Z_{replica}$	$\angle S1 - \angle S2 < 0°$

The Resistive Impedance Reach side of the earth zone is controlled by the Resistive Reach setting applied (***Rx Gnd Resistive***). This defines the fault arc resistance that can be detected for a single phase-earth fault. For such a fault, the fault resistance appears in the total fault loop (out and return loop), in which the line impedance is Z_1 x $(1 + k_{ZN})$, if IN ≅ Iph.

Most injection test sets plot impedance characteristics in positive sequence terms, so that the right-hand intercept appears less than the setting applied (***Rn Gnd Resistive*** /(1+ k_{ZN})). The left hand side is set by the ***Rn Gnd Res Rev*** setting and acts similarly.

Note:
The resistive reach lines of earth-fault Quadrilateral characteristics are not affected by the type of tilting used by the reactive lines (fixed or dynamic), nor by the angle values.

8.5.5 EARTH FAULT QUADRILATERAL CHARACTERISTICS SUMMARY

The inputs to the comparators used for the earth-fault Quadrilaterals are summarised in the following table:

Zone	Line	S1	S2	Condition
Zone 1	Impedance Reach	Vph - Iph.$Z_{replica}$	I_{LAG} ∠ σ	∠S1 -∠S2 < 0°
Zone 1	Reverse Impedance Reach	Vph - Iph.$Z'_{replica}$	I_{LAG} ∠-3°	∠S1 -∠S2 > 0°
Forward or Offset zones (except Zone 1)	Impedance Reach	Vph - Iph.$Z_{replica}$	I_{LEAD} ∠ σ	∠S1 -∠S2 < 0°
Forward or Offset* zones (Zone 1 and Zone 1e, where ***Series Comp.*** is `Enabled`)	Reverse Impedance Reach	Vph - Iph.$Z'_{replica}$	I_{LAG} ∠-3°	∠S1 -∠S2 > 0°
Reverse	Impedance Reach	Vph + Iph.$Z_{replica}$	-I_{LEAD} ∠ σ	∠S1 -∠S2 < 0°
Reverse	Reverse Impedance Reach	Vph + Iph.$Z'_{replica}$	-I_{LAG} ∠-3°	∠S1 -∠S2 > 0°
Forward or Offset	Resistive Reach	Vph - Iph.R_{LP}	Iph.$Z_{replica}$	∠S1 -∠S2 > 0°
Forward or Offset	Reverse Resistive Reach	Vph - Iph.R'_{LP}	Iph.$Z_{replica}$	∠S1 -∠S2 < 0°
Reverse	Resistive Reach	Vph + Iph.R_{LP}	-Iph.$Z_{replica}$	∠S1 -∠S2 > 0°
Reverse	Reverse Resistive Reach	Vph + Iph.R'_{LP}	-Iph.$Z_{replica}$	∠S1 -∠S2 < 0°

Note:
This is also the reverse impedance reach, if the **Series Comp. setting is `Enabled`.*

If dynamic tilting is selected, then:

If I_{LEAD} is I2 the lines are dynamically tilted up from the fixed angle (Forward sense)

- If I_{LEAD} is Iph, the fixed tilt applies.
- If I_{LAG} is I2, the lines are dynamically tilted down from the fixed angle (Forward sense)
- If I_{LAG} is Iph, the fixed tilt applies.

If fixed tilting is selected, then he current input quantity for S2 is Iph in all cases.

The positive sequence reach settings used for the Earth-Fault Quadrilateral characteristics are summarised in the table below:

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
1 Ph-Earth	Forward	Z1 Gnd. Reach * (1 + kZN)	Z1	R1 Gnd Resistive	0.25 R
1 Ph-Earth	Rev Reach Series Comp.	Z1 Gnd. Reach * (1 + kZN)	Z1' Gnd Rev Rch * (1 + kZN)	R1 Gnd Resistive	R1' Ph Res. Rev
2 Ph-Earth	Forward	Z2 Gnd. Reach * (1 + kZN)	Z2	R2 Gnd Resistive	0.25 R
2 Ph-Earth	Offset	Z2 Gnd. Reach * (1 + kZN)	Z2' Gnd Rev Rch * (1 + kZN)	R2 Gnd Resistive	R2' Ph Res. Rev
3 Ph-Earth	Forward	Z3 Gnd. Reach * (1 + kZN)	Z3	R3 Gnd Resistive	0.25 R

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
3 Ph-Earth	Reverse	Z3 Gnd. Reach * (1 + kZN)	Z3	R3 Gnd Resistive	0.25 R
3 Ph-Earth	Offset	Z3 Gnd. Reach * (1 + kZN)	Z3' Gnd Rev Rch * (1 + kZN)	R3 Gnd Resistive	R3' Ph Res. Rev
4 Ph-Earth	Reverse	Z4 Gnd. Reach * (1 + kZN)	Z4	R4 Gnd Resistive	0.25 R
P Ph-Earth	Forward	ZP Gnd. Reach * (1 + kZN)	ZP	RP Gnd Resistive	0.25 R
P Ph-Earth	Reverse	ZP Gnd. Reach * (1 + kZN)	ZP	RP Gnd Resistive	0.25 R
P Ph-Earth	Offset	ZQ Gnd. Reach * (1 + kZN)	ZP' Gnd Rev Rch * (1 + kZN)	RP Gnd Resistive	RP' Gnd Res. Rev
Q Ph-Earth	Forward	ZQ Gnd. Reach * (1 + kZN)	ZQ	RQ Gnd Resistive	0.25 R
Q Ph-Earth	Reverse	ZQ Gnd. Reach * (1 + kZN)	ZQ	RQ Gnd Resistive	0.25 R
Q Ph-Earth	Offset	ZQ Gnd. Reach * (1 + kZN)	ZQ' Gnd Rev Rch * (1 + kZN)	RQ Gnd Resistive	RQ' Gnd Res. Rev
1e Ph-Earth	Forward	Z1e Gnd. Reach * (1 + kZN)	Z1e	R1e Gnd Resistive	0.25 R
1e Ph-Earth	Rev Reach Series Comp.	Z1e Gnd. Reach * (1 + kZN)	Z1e' Gnd Rev Rch * (1 + kZN)	R1e Gnd Resistive	R1e' Ph Res. Rev
R Ph-Earth	Forward	ZR Gnd. Reach * (1 + kZN)	ZR	RR Gnd Resistive	0.25 R
R Ph-Earth	Reverse	ZR Gnd. Reach * (1 + kZN)	ZR	RR Gnd Resistive	0.25 R
R Ph-Earth	Offset	ZR Gnd. Reach * (1 + kZN)	ZR' Gnd Rev Rch * (1 + kZN)	RR Gnd Resistive	RR' Gnd Res. Rev
S Ph-Earth	Forward	ZS Gnd. Reach * (1 + kZN)	ZS	RS Gnd Resistive	0.25 R
S Ph-Earth	Reverse	ZS Gnd. Reach * (1 + kZN)	ZS	RS Gnd Resistive	0.25 R
S Ph-Earth	Offset	ZS Gnd. Reach * (1 + kZN)	ZS' Gnd Rev Rch * (1 + kZN)	RS Gnd Resistive	RS' Gnd Res. Rev

where $k_{ZN} = (Z_0 - Z_1) / 3Z_1$ and is defined by two settings: ***kZN Res Comp*** and ***KZN Res Angle***.

8.5.6 QUADRILATERAL CHARACTERISTIC FOR PHASE FAULTS

Quadrilateral characteristics are available for phase fault protection. A mix of Directional Forward, Directional Reverse, and Offset characteristics is available. Zone 1, Zone 1e and Zone 4 are Directional Forward or Reverse. Other zones can be set independently as Offset, Directional Forward, or Directional Reverse. Each zone is independent and is defined by an Impedance Reach Line, a Reverse Impedance Reach Line, and two resistive blinders. The two resistive blinders (Resistive Reach Line and Reverse Resistive Reach Line) are parallel to the zone characteristic impedance angle. The two reactance lines of each Quadrilateral exhibit a characteristic tilt. In the phase fault characteristics the tilt of the Reverse Impedance Reach Line is preset, whilst you can choose the tilt angle for the Impedance Reach Line.

8.5.6.1 PHASE FAULT IMPEDANCE REACH LINE

The tilt of the top line can be set independently for each zone. It is defined by a reach setting, Z, and a tilt angle, σ, as shown in the following diagram:

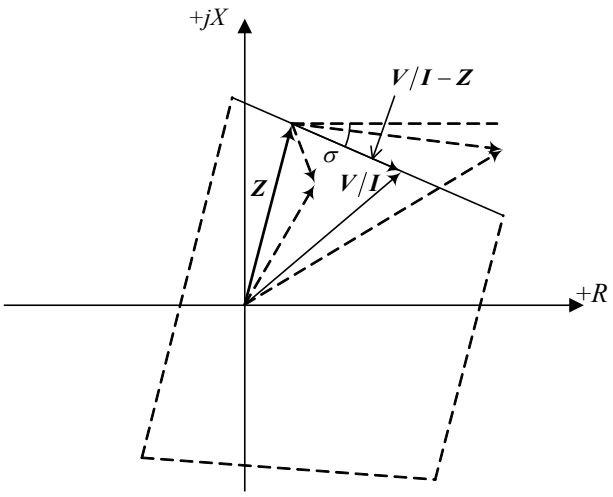


Figure 86: Impedance reach line construction

Referenced to the fault current I, the angle of tilt is equal to the setting σ. A negative angle sets a downward tilt and a positive angle sets an upward tilt. Operation can occur when the operating signal lags the polarising signal. A negative angle sets a downward tilt and a positive angle sets an upward tilt.

For all V/I vectors below the Impedance Reach line, the following condition is true:

$$\angle (V/I - Z) \leq \sigma$$

or

$$\angle (V - I.Z) \leq \angle I.\angle \sigma$$

The resultant two signals provided to the comparator are:

$$S_1 = V - I.Z$$

$$S_2 = I.\angle \sigma$$

Impedance on the tripping side of the Impedance Reach line is detected when the angle between S1 and S2 is less than 0°.

8.5.6.2 REVERSE IMPEDANCE REACH LINE

The quadrilateral distance characteristics include a reverse impedance reach line Z' associated with each zone. For a directional forward or reverse zone, Z' is normally a fixed percentage (100% of Z) of the forward reach (Z) in the opposite direction. This line is completely independent of the directional line and has no bearing on the relay performance except in cases of protected lines with series compensation and adjacent lines. If the relay is set with ***Series Comp.*** `Enabled`, the value of Z' is no longer fixed at 100% but settable as a percentage of the reach. The reason for this is because a series capacitor in the protected or adjacent lines can invert the inductive nature of the apparent fault impedance due to the series capacitor. Therefore, the impedance seen by a relay can be seen as a capacitance. Thus, the apparent impedance lies in the capacitive reactance quadrants (i.e. into the II or IV quadrants). This effect could be augmented due to throttling effects.

Notice that for an offset zone, Z' is a setting: **Zn' Ph Rev Reach** for phase elements or **Zn' Gnd Rev Rch** for earth elements.

The Reverse Impedance Reach line of the phase quadrilateral elements has a tilt that is fixed at -3° as shown in the following diagram:

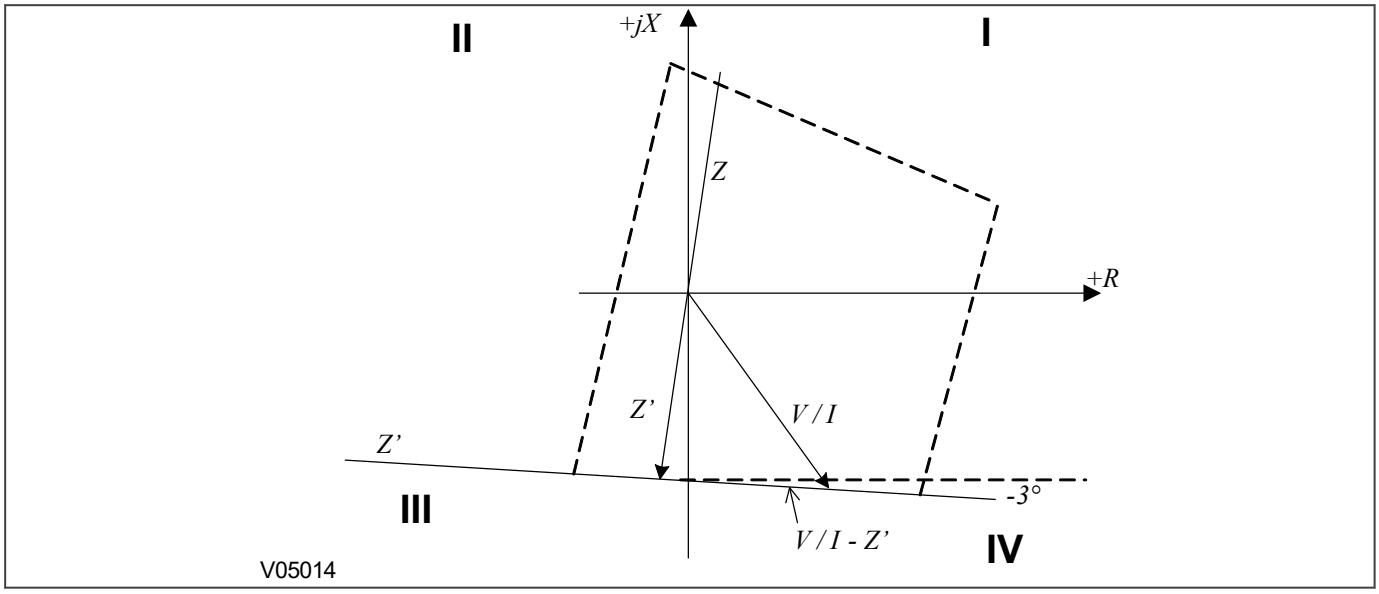


Figure 87: Reverse impedance reach line construction

The signals provided to the comparator are:

$S_1 = V - I.Z'$

$S_2 = I.\angle -3°$

Impedance on the tripping side of the Reverse Impedance Reach line is detected when the angle between S1 and S2 is greater than 0°.

To make sure the desired fault impedance is seen in the characteristic in cases of series compensated lines, it is necessary to check the limits of the characteristic, i.e. the reverse impedance reach Z'.

Here after there are some extreme examples of short lines adjacent to long lines and very strong infeeds which could cause a considerable displacement of the impedance locus towards the capacitive reactive impedance.

Reverse impedance reach in Zone 1

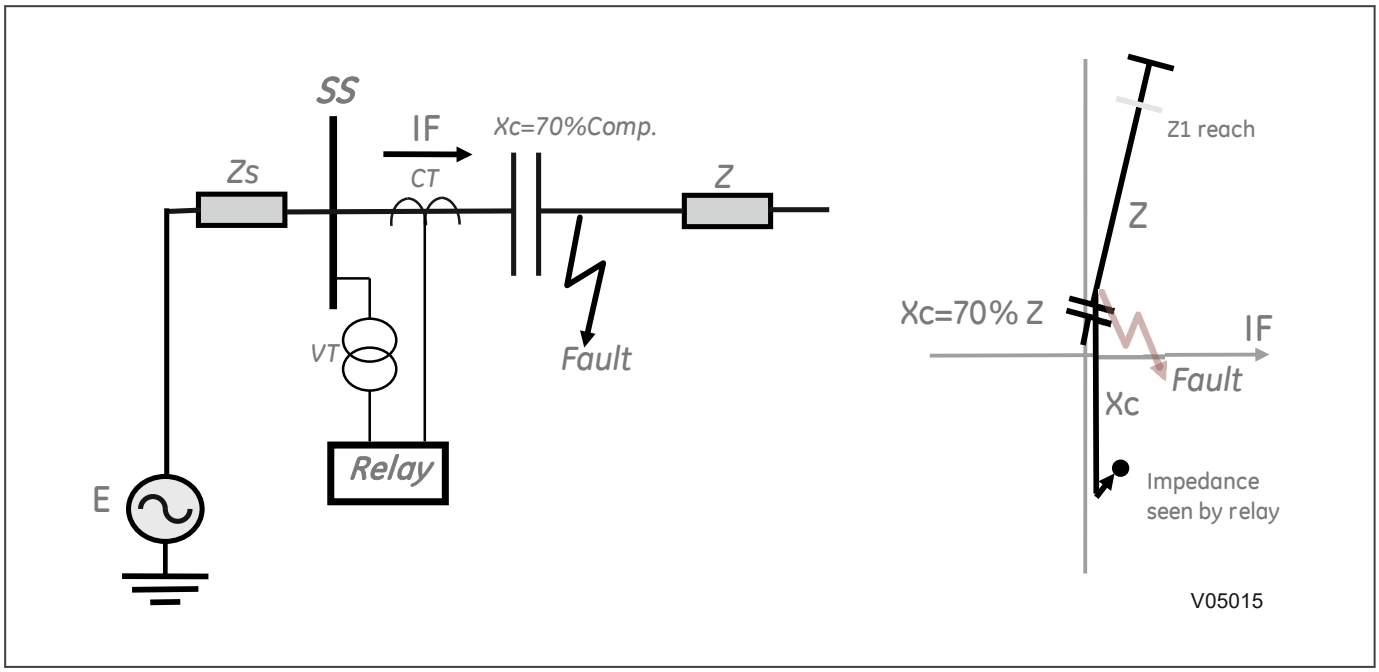


Figure 88: Zone 1 reverse impedance reach

With the location of the VT shown in figure above:

Z Line = 100%

Z Capacitor = 70% of Z line

With setting Zone 1 = 0.8*(1 - 0.7) = 0.24 of Z line

Impedance seen by relay is shown in figure.

Allowing for 20% errors for the measured impedance = 70%/80% = 87.5%

Zone 1 reverse reach setting should be 87.5%/24% ~ 400% of Zone 1 reach

Reverse impedance reach for Zone 3 set as offset or directional forward

From the following figure:

Typical Zone 3 forward reach = (1 + 4*(1+13)) * 1.2 = 68.4

Z for a fault in Fault 1 = 1 – (0.7*4)*(1+13) = -38.2

Reverse setting = 38.2/68.4 ~ 0.56* Z3 forward reach. Therefore, reverse reach would be 100% of forward Zone 3 reach.

This applies if the zone 3 is set as is directional forward or offset.

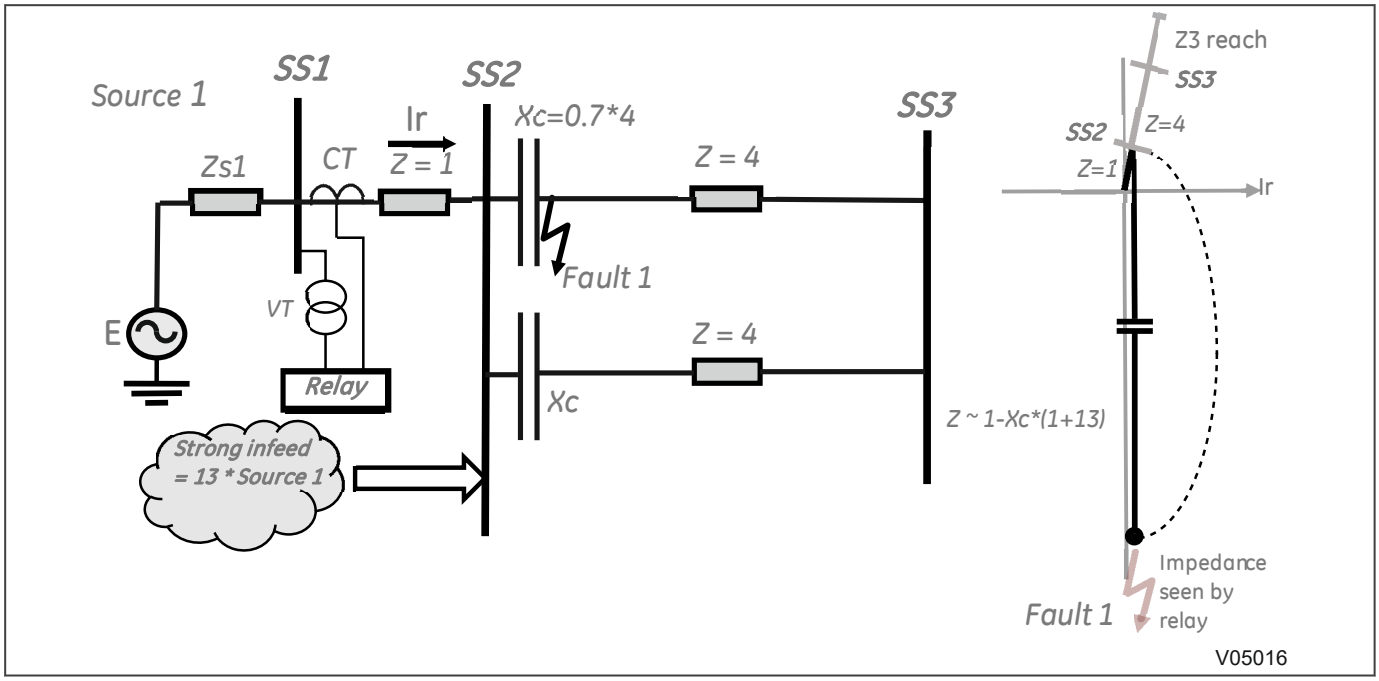


Figure 89: Zone 3 reverse impedance reach set as directional forward or offset

Reverse impedance reach for Zone 4 set as directional reverse

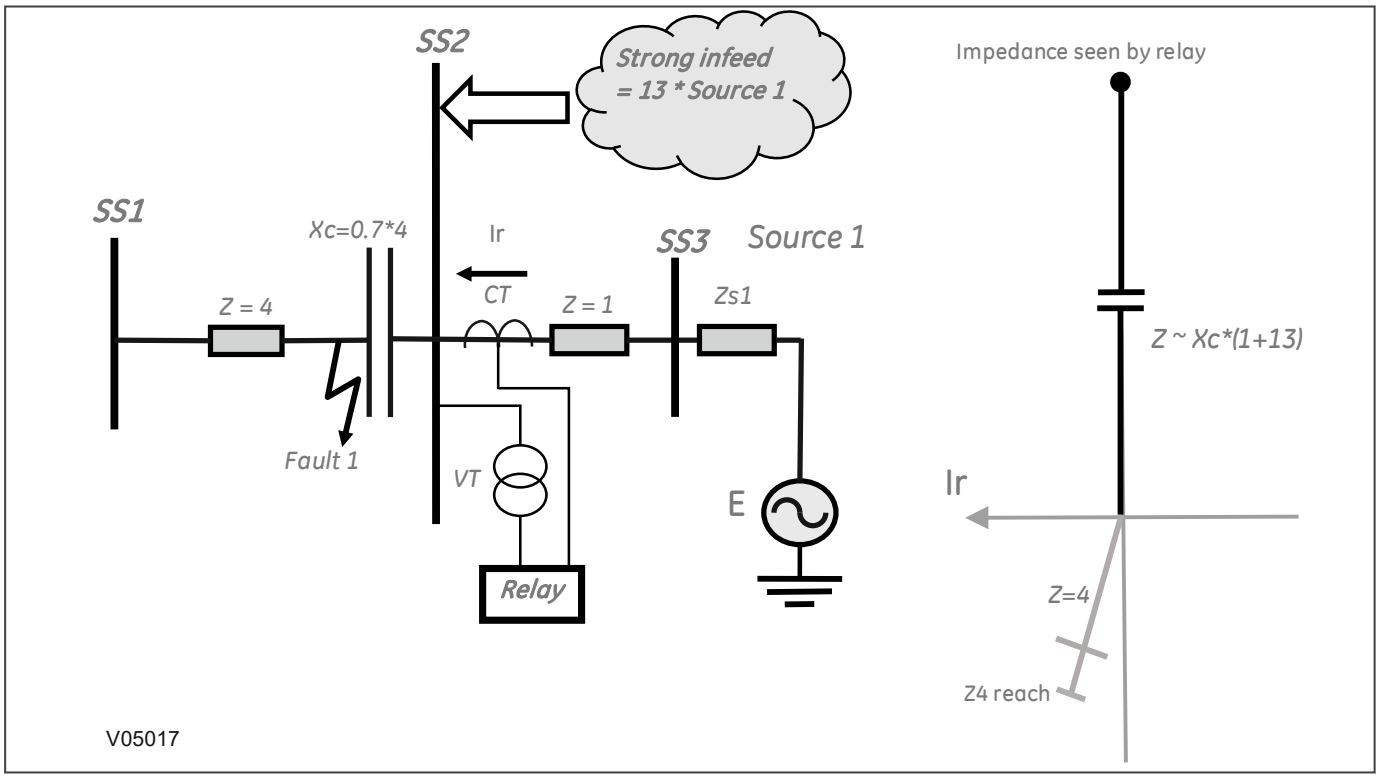


Figure 90: Zone 4 reverse impedance reach set as directional reverse

Typical reverse reach setting is to cover at least to SS1. Therefore, Zone 4 = 1.2 * (13+1) * 4 = 67.2

Consider the impact of fault 1, reverse Z4 reach setting = 1.2 * (13+1) * (4*0.7) = 47

Therefore, reverse reach must be approximately 100% of the Zone 4 reach.

With these examples, it is possible to conclude reasonable settings for the reverse impedance reach lines Z' (**Zn' Ph Rev Reach** and **Zn' Gnd Rev Rch**) for series compensated lines and the associated adjacent lines.

8.5.6.3 PHASE FAULT RESISTIVE REACH LINE

Refer to the following figure:

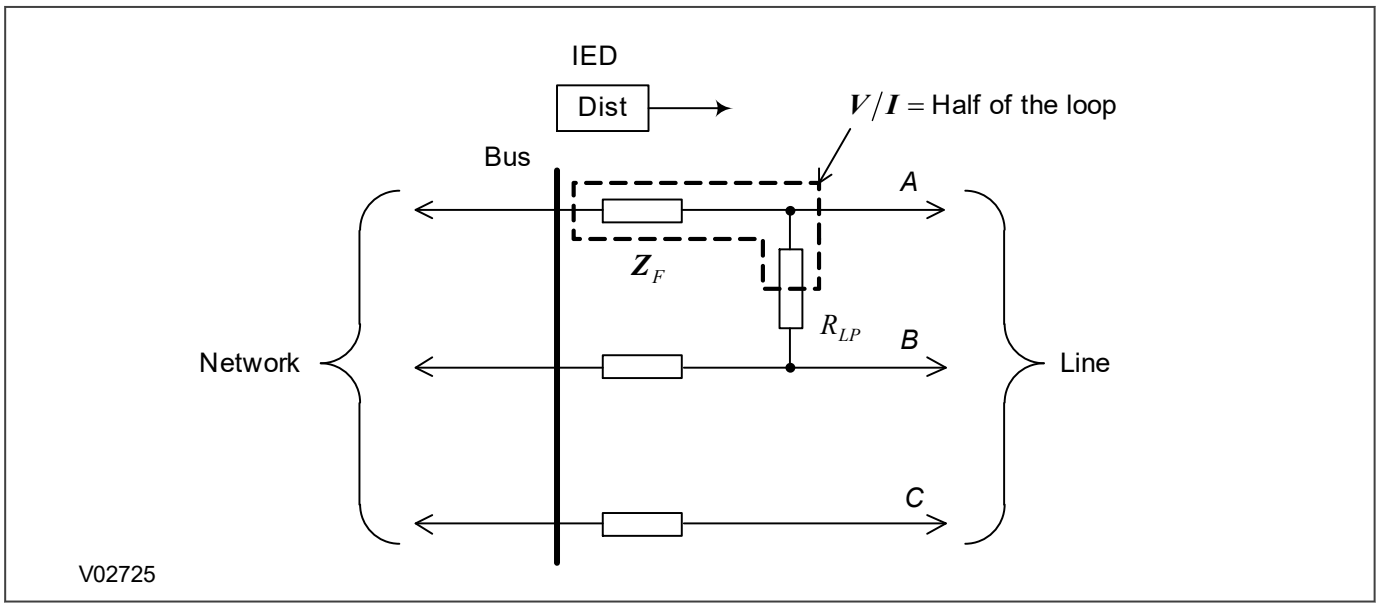


Figure 91: Resistive reach of phase elements

The setting ***Rx Ph. Resistive*** defines the complete loop resistive reach R_{LP} of the Distance Protection.

Since a phase-to-phase distance element measures half of the loop, the right-hand resistive reach R, of the characteristic is equal to half of the setting value.

$$R = \frac{1}{2}\ \textit{Rx Ph. Resistive}$$

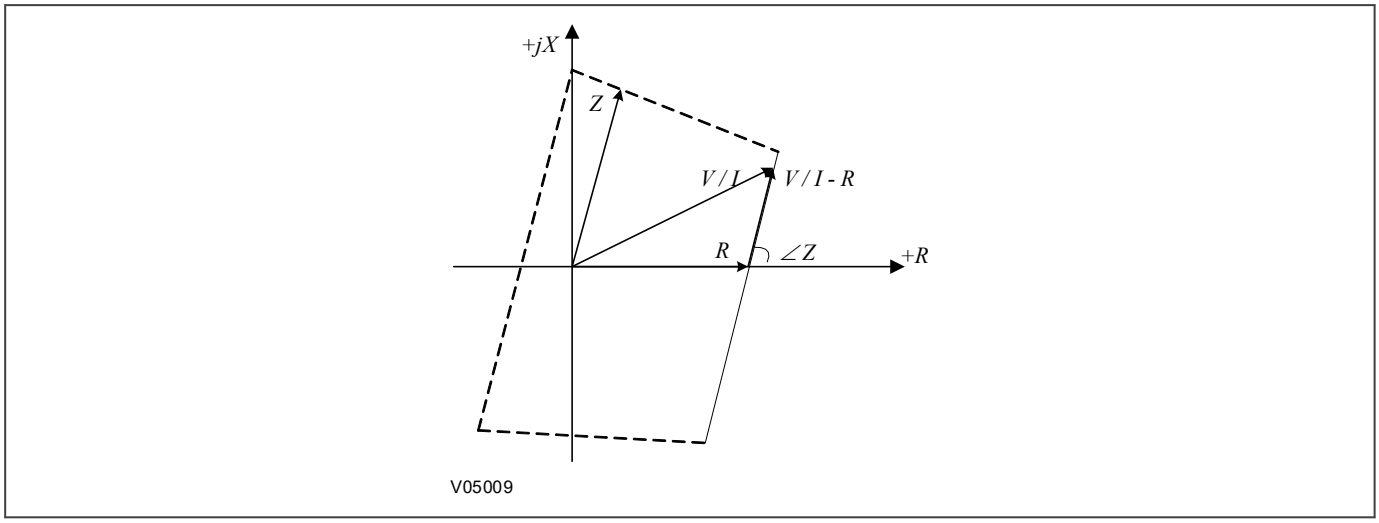


Figure 92: Resistive reach line construction

For all V/I vectors which are on the left side of the right blinder the following condition is true:

$$\angle (V/I - R) \leq Z$$

or

$$\angle (V - I.R) \leq \angle I.Z$$

The two signals provided to the comparator are:

$$S_1 = V - I.R$$

$$S_2 = I.Z$$

The impedance on the left side of the right hand resistive line is detected when the angle between S1 and S2 is greater than 0°.

8.5.6.4 PHASE FAULT REVERSE RESISTIVE REACH LINE

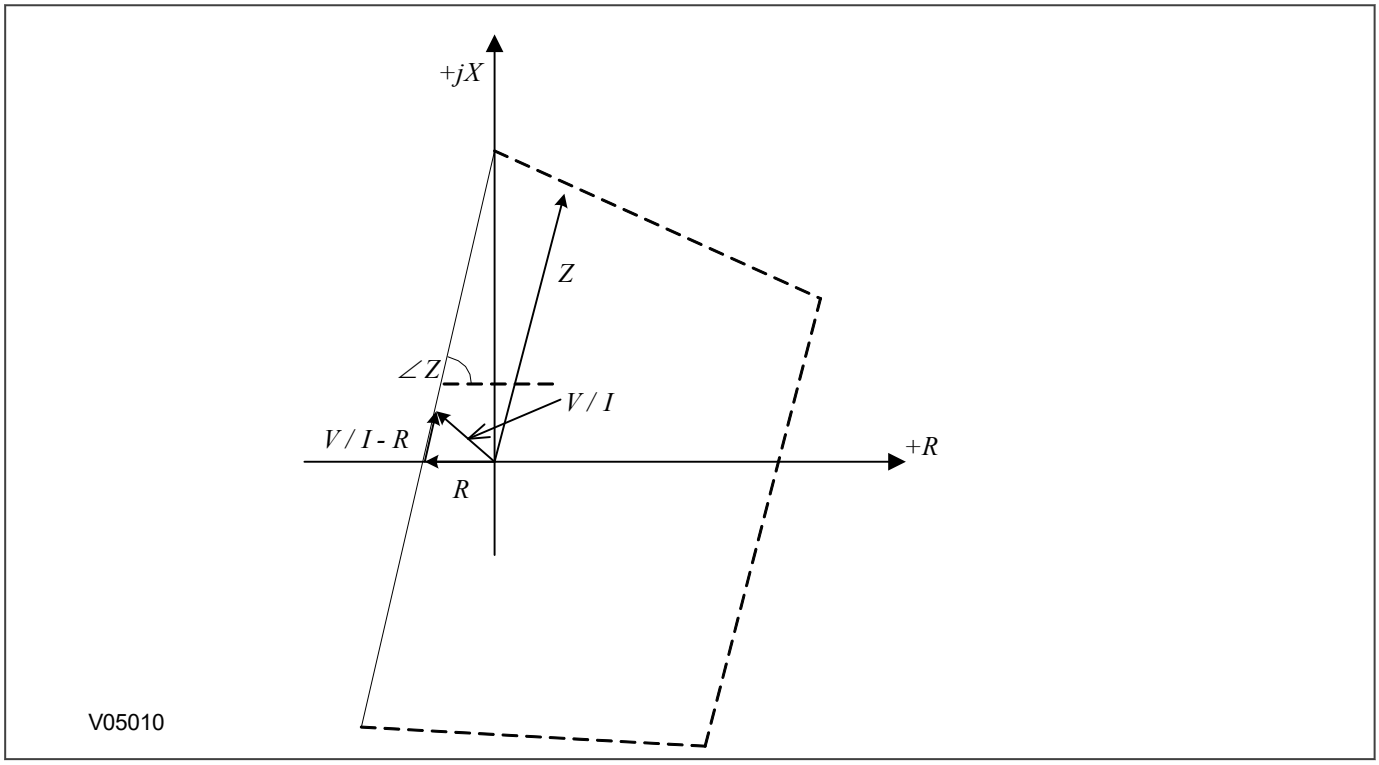


Figure 93: Reverse resistive reach line construction

For an offset zone, R' is the settable reverse resistive reach (=½*__Rx' Ph Res. Rev.__). . For a directional zone, R' is fixed at 25% of the Resistive Reach (=½*__Rx Ph Res. Rev.__), acting in the opposite direction.

The two signals provided to the comparator are:

$$S_1 = V - I.R$$

$$S_2 = I.Z$$

The impedance on the right side of the left hand resistive line is detected when the angle between S1 and S2 is less than 0°.

8.5.6.5 PHASE FAULT QUADRILATERAL CHARACTERISTIC SUMMARY

The phase fault Quadrilateral characteristics are summarised in the following figure and tables:

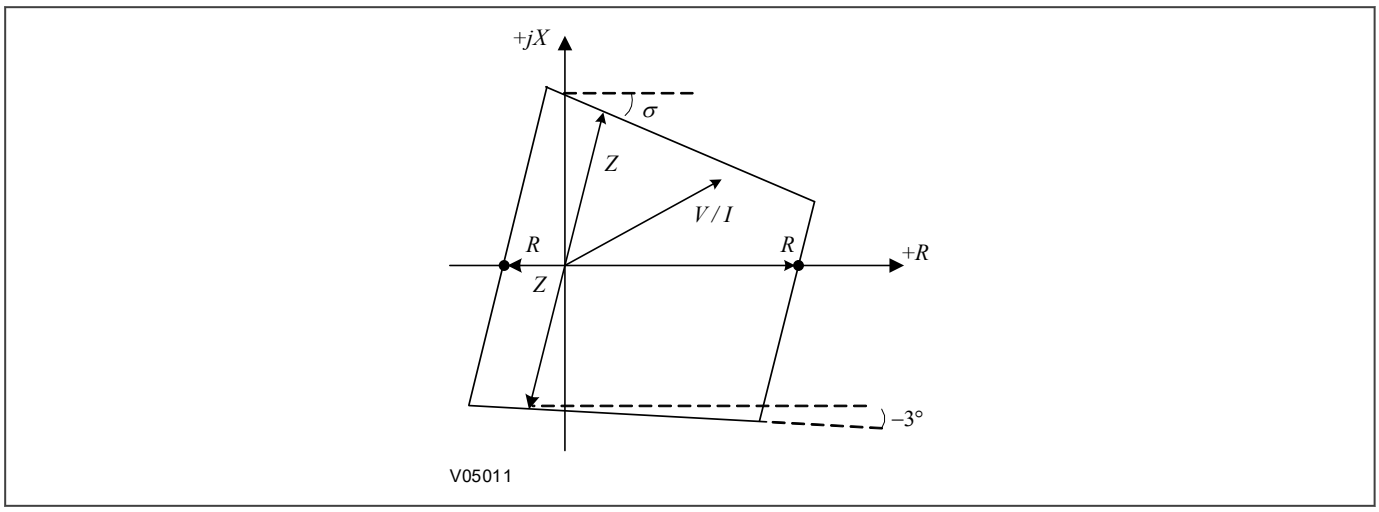


Figure 94: Phase fault quadrilateral characteristic summary

The comparators used for the Phase-Fault Quadrilateral zones are summarised in the following table:

Zone	Line	S1	S2	Condition (∠S1 - ∠S2)
Forward/Offset	Impedance Reach Line	V – I.Z	I.∠ σ°	<0°
Forward/Offset	Reverse Impedance Reach Line	V – I.Z'	I.∠ 3°	>0°
Forward/Offset	Resistive Reach Line	V – I.R	I.Z	>0°
Forward/Offset	Reverse Resistive Reach Line	V – I.R'	I.Z	<0°
Reverse	Impedance Reach Line	V + I.Z	-I.∠ σ°	<0°
Reverse	Reverse Impedance Reach Line	V + I.Z'	-I.∠ 3°	>0°
Reverse	Resistive Reach Line	V + I.R	-I.Z	>0°
Reverse	Reverse Resistive Reach Line	V + I.R'	-I.Z	<0°

The positive sequence reach settings used for the Phase-Fault Quadrilateral characteristics are summarised in the following table:

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
1 Ph-Ph	Forward	Z1 Ph. Reach	Z1	½*R1 Ph. Resistive	0.25 R
1 Ph-Ph	Reverse	Z1 Ph. Reach	Z1	½*R1 Ph. Resistive	0.25 R
1 Ph-Ph	Rev Reach Series Comp.	Z1 Ph. Reach	Z1' Ph Rev Reach	½*R1 Ph. Resistive	½*R1' Ph Res. Rev.
1e Ph-Ph	Forward	Z1e Ph. Reach	Z1e	½*R1e Ph. Resistive	0.25 R
1e Ph-Ph	Reverse	Z1e Ph. Reach	Z1e	½*R1e Ph. Resistive	0.25 R
1e Ph-Ph	Rev Reach Series Comp.	Z1e Ph. Reach	Z1e' Ph Rev Reach	½*R1e Ph. Resistive	½*R1e' Ph Res. Rev.
2 Ph-Ph	Forward	Z2 Ph. Reach	Z2	½*R2 Ph. Resistive	0.25 R
2 Ph-Ph	Reverse	Z2 Ph. Reach	Z2	½*R2 Ph. Resistive	0.25 R
2 Ph-Ph	Offset*	Z2 Ph. Reach	Z2' Ph Rev Reach	½*R2 Ph. Resistive	½*R2' Ph Res. Rev.
3 Ph-Ph	Forward	Z3 Ph. Reach	Z3	½*R3 Ph. Resistive	0.25 R
3 Ph-Ph	Reverse	Z3 Ph. Reach	Z3	½*R3 Ph. Resistive	0.25 R

Zone	Type	Impedance Reach Z	Reverse Impedance Reach Z'	Resistive Reach R	Reverse Resistive Reach R'
3 Ph-Ph	Offset*	Z3 Ph. Reach	Z3' Ph Rev Reach	½*R3 Ph. Resistive	½*R3' Ph Res. Rev.
4 Ph-Ph	Forward	Z4 Ph. Reach	Z4	½*R4 Ph. Resistive	0.25 R
4 Ph-Ph	Reverse	Z4 Ph. Reach	Z4	½*R4 Ph. Resistive	0.25 R
4 Ph-Ph	Offset*	Z4 Ph. Reach	Z4' Ph Rev Reach	½*R4 Ph. Resistive	½*R4' Ph Res. Rev.
P Ph-Ph	Forward	ZP Ph. Reach	ZP	½*RP Ph Resistive	0.25 R
P Ph-Ph	Reverse	ZP Ph. Reach	ZP	½*RP Ph Resistive	0.25 R
P Ph-Ph	Offset*	ZP Ph. Reach	ZP' Ph Rev Reach	½*RP Ph Resistive	½*RP' Ph. Res. Rev.
Q Ph-Ph	Forward	ZQ Ph. Reach	ZQ	½*RQ Ph Resistive	0.25 R
Q Ph-Ph	Reverse	ZQ Ph. Reach	ZQ	½*RQ Ph Resistive	0.25 R
Q Ph-Ph	Offset*	ZQ Ph. Reach	ZQ' Ph Rev Reach	½*RQ Ph Resistive	½*RQ' Ph. Res. Rev.
R Ph-Ph	Forward	ZR Ph. Reach	ZR	½*RR Ph Resistive	0.25 R
R Ph-Ph	Reverse	ZR Ph. Reach	ZR	½*RR Ph Resistive	0.25 R
R Ph-Ph	Offset*	ZR Ph. Reach	ZR' Ph Rev Reach	½*RR Ph Resistive	½*RR' Ph. Res. Rev.
S Ph-Ph	Forward	ZS Ph. Reach	ZS	½*RS Ph Resistive	0.25 R
S Ph-Ph	Reverse	ZS Ph. Reach	ZS	½*RS Ph Resistive	0.25 R
S Ph-Ph	Offset*	ZS Ph. Reach	ZS' Ph Rev Reach	½*RS Ph Resistive	½*RS' Ph. Res. Rev.

Note:
** This is also the reverse impedance reach, if the **Series Comp.** setting is* `Enabled`.

8.6 PHASE AND EARTH FAULT DISTANCE PROTECTION IMPLEMENTATION

The Distance protection requires line data to be input to operate correctly. You must first input the data using the settings in the *LINE PARAMETERS* column.

The Distance protection has a Setting Mode which is set to `Simple` by default. We recommend the default for most applications. Instead of entering distance zone impedance reaches in ohms, zone settings are simply entered in terms of percentage of the protected line data specified in the ***Line Impedance*** setting in the *LINE PARAMETERS*. The setting assumes that the residual compensation factor is equal for all zones. The protection calculates the required reach settings from the percentage settings. The calculated zone reaches are available for viewing but you cannot change the values.

An `Advanced` Setting Mode allows individual distance ohmic reaches and residual compensation factors to be entered for each zone. When advanced mode is selected, all 'percentage' settings associated with the `Simple` setting mode are hidden and the Distance zone settings need to be entered for each zone in the *DIST. ELEMENTS* column.

8.6.1 PHASE FAULT CHARACTERISTICS

Each phase zone can be `Enabled` or `Disabled` using the ***Zone Ph Status*** settings in the *DISTANCE SETUP* column.

Characteristics can be either 'Quadrilateral' (polygon), or Mho (circular). The chosen characteristic applies to all zones. All distance elements are directionalised and use residual compensation of the corresponding phase fault reach.

8.6.2 EARTH FAULT CHARACTERISTICS

Each ground zone can be `Enabled` or `Disabled` using the **Zone Gnd Status** settings in the *DISTANCE SETUP* column.

Characteristics can be either 'Quadrilateral' (polygon), or Mho (circular). The chosen characteristic applies to all zones. All distance elements are directionalised and use residual compensation of the corresponding phase fault reach.

8.6.3 DISTANCE PROTECTION TRIPPING DECISION

A fault is detected if the phase voltage drops below 70%, or if the phase selector picks up. When a fault is detected, the protection stores values recorded over the two previous cycles. These are used to provide a reference for memory polarisation, etc, as the fault is processed.

For security, a number of criteria must be satisfied before the distance protection issues a trip command. These are as follows:

- The phase selector needs to identify the faulted phases and ensure that only the correct distance measuring zones can issue a trip. Possible phase selections are AN, BN, CN, AB, BC, CA, and ABC. For double phase-earth faults, the selection is AB, BC or CA, with N (neutral) for indication only.
- For the selected phase-earth elements the phase and the neutral currents must exceed the minimum sensitivity threshold. For the selected phase-to-phase elements the loop current must exceed the minimum sensitivity threshold. By default, this sensitivity is 5%In for phase-earth faults and, for phase-to-phase faults both of the faulted phases must exceed 5%In. You can raise this minimum sensitivity if necessary, but this is not normally required.
- For an earth-fault distance element to operate, the corresponding biased neutral current detector must have picked up.
- The faulted phase impedance must appear in a tripping (measuring) zone, corresponding to the phase selection.

- For directional zones, the directionality element must agree with the tripping zone. Zones 1, 2, and 4 are always directional whereas other zones are only directional if set as directional. In directional zones the directionality element must agree with the tripping zone. For example, Zone 1 is a Forward Directional zone and must not trip for Reverse faults. Therefore a Zone 1 trip is only allowed if the directionality element issues a Forward decision. Zone 4 is reverse-looking so needs a Reverse decision by the directionality element.
- The set time delay for the measuring zone must expire, with the measured fault impedance remaining inside the zone characteristic for the duration of the delay time. Typically, Zone 1 has no time delay (instantaneous), whereas all other zones have time delays.
- Where channel-aided distance schemes are used, the time delay tZ2 for overreaching Zone 2 may be bypassed for some of the schemes.

8.6.4 DISTANCE PROTECTION PHASE SELECTION

Phase selection allows the product to identify exactly which phases are involved in a fault and enables the correct measuring zones to trip.

Operation of the distance elements is controlled by a Superimposed Current Phase Selector. For a period of two-cycles after pick-up of the phase selector, only elements associated with the fault type selected by the phase selector are allowed to operate. If these elements do not operate, all elements are enabled for the following five cycles, before the phase selector returns to its quiescent state.

Operation of an enabled distance element during the two-cycle, or five-cycle period, causes the phase selector state to be maintained until the element resets. An exception to this is when the phase selector changes decision while an element is operated. In this case, the selected elements are reset and the two cycle period restarts with the new selection.

Note:
Any existing trip decision is not reset under this condition. After the first cycle following a selection, the phase selector is only permitted to change to a selection involving additional phases.

On double phase-to-earth faults, only the phase-to-phase elements are enabled. This is because they are generally more accurate under these conditions than earth fault elements. A biased neutral current level detector operates to indicate the involvement of earth in the fault.

8.6.4.1 FAULTED PHASE SELECTION

The faulted phase or phases are selected by comparing the magnitudes of the three phase-to-phase superimposed currents. A single phase-to-earth fault produces the same superimposed current on two of these signals and zero on the third. A phase-to-phase or double-phase-to-earth fault produces one signal which is larger than the other two. A three phase fault produces three superimposed currents which are the same size. The figure below shows how the change in current can be used to select the faulted phases for a C phase-to-ground (CN) fault.

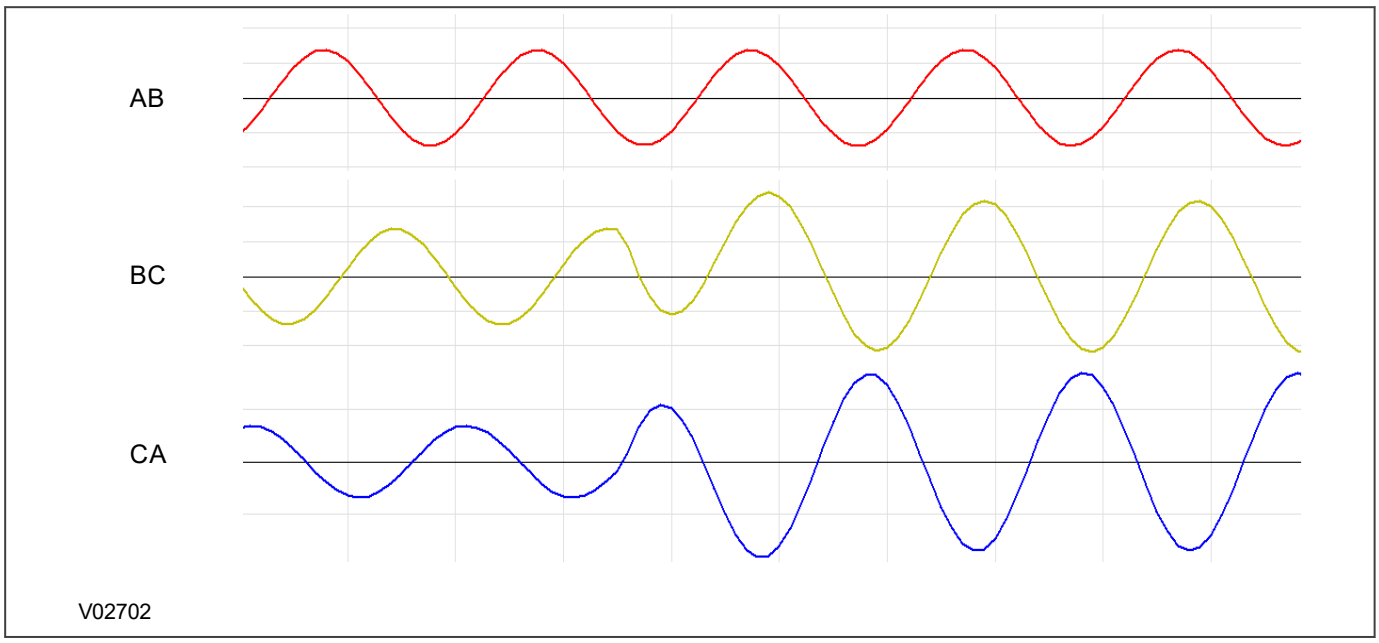


Figure 95: Phase to phase current changes for C phase-to-ground (CN) fault

As default, phase selection is made when any superimposed current exceeds 5% of nominal current (0.05 In).

Any superimposed current greater than 80% of the largest superimposed current is included in the phase selection logic.

For applications which might experience high levels of sub-synchronous currents, the phase selector automatically raises the threshold from the default 5% of In, in order to prevent sporadic operation whilst maintaining high sensitivity to faults.

Note:
If you test the distance elements using test sets, which do not provide a dynamic model to generate true fault delta conditions, you need to set ***Static Test Mode*** *to* `Enabled` *in the COMMISSION TESTS column. This disables phase selector control and forces the distance protection to use a conventional (non-delta) directional line.*

The phase selector picks up on fault detection, and enables Distance protection on all elements which have been selected by the pick-up. These elements are enabled for 2 cycles, and normally this will result in tripping. On double ground-to-phase faults, only appropriate phase elements are enabled. This is because they are generally more accurate than ground elements under these conditions. If, however, tripping is not initiated within the 2 cycles, for the following 5 cycles all Distance elements (including all phase-earth elements) are enabled. During these five cycles, this could lead to incorrect operation of earth-fault elements in case of an out-of-zone double-phase-earth fault. This is because one of the phase-earth elements could demonstrate significant overreach, which may result in maloperation. To help prevent this, a Biased Neutral Current Detector and a fault-type supervision are incorporated.

8.6.5 BIASED NEUTRAL CURRENT DETECTOR AND FAULT-TYPE SUPERVISION

The Biased Neutral Current Detector permits the earth-fault elements to operate only if sufficient neutral current is detected. The Biased Neutral Current Detector characteristic is illustrated in the following figure.

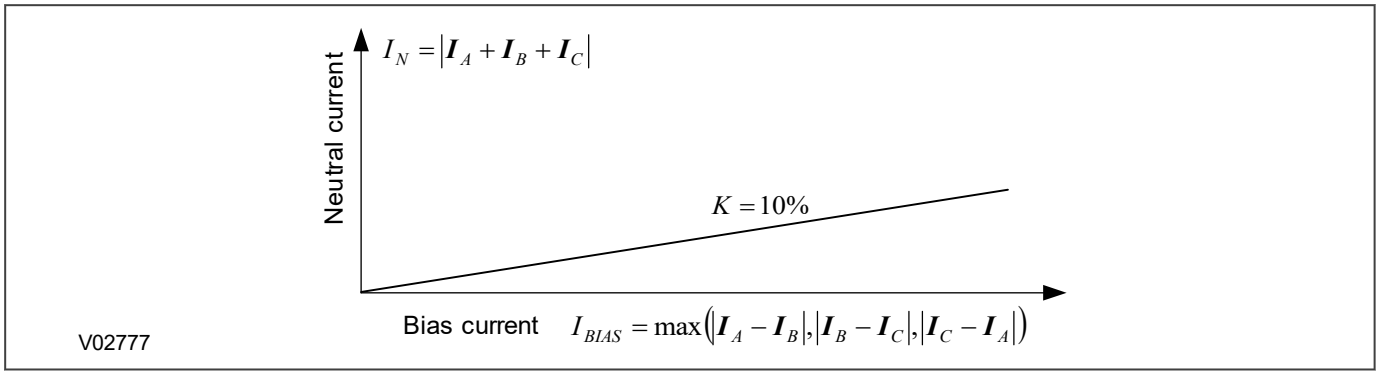


Figure 96: Biased neutral current detector characteristic

The neutral current detector uses the maximum of the three phase current differences as a biasing value. The slope of the characteristic is fixed at 10%.

Biasing the neutral current detector assures that the detector is sensitive enough to operate for any single-phase fault, without the risk of picking up on neutral spill current during phase-to-phase faults. The neutral spill current might arise from mismatched current transformers or current transformer saturation. The biasing also ensures that the earth fault distance elements are generally disabled for double-phase-to-earth faults with high resistance in the neutral. Such faults can occur in resistively earthed systems, or in solidly earthed systems due to high arc resistance. Given that these conditions are very similar to pure phase-to-phase faults, the earth fault distance elements can exhibit high measuring errors which the use of the neutral current detector overcomes.

There is additional supervision to inhibit the phase to ground loops in case of double phase to ground faults. This technique checks the absolute angle between the zero-sequence current and the negative sequence current. It allows the phase to ground element to operate only if the absolute angle between the negative sequence current and the zero-sequence current is less than 50°. This supervision is only used in certain scenarios when the relay is in the 5 cycle period state.

8.6.6 DIRECTIONALISING THE DISTANCE ELEMENTS

By default a Delta technique is used for directionalising the Distance protection. It acts on step-changes (Deltas) of current and voltage to determine whether potential fault conditions are in the forward or reverse direction. The Delta voltage and current thresholds used in the Distance Directional decision are fixed for optimum performance. The Directional characteristic angle, (also known as the relay characteristic angle - RCA) is set to 60° by default, but you can change this to suit your application using the ***Dir. Char Angle*** setting in the *DISTANCE SETUP* column.

The Delta Directional technique needs the changes in voltage and current to exceed the preset thresholds, in order to determine forward and reverse decisions. If these thresholds are not exceeded, but a potential fault is detected, the Distance protection reverts to a conventional directional technique with memory polarisation of the voltage.

If you don't want to use the Delta directional technique, set ***Dir. Status*** in the *DISTANCE SETUP* column to `Disabled` in which case memory polarisation is used.

8.6.7 DELTA DIRECTIONAL ELEMENT

Where Distance protection is being applied, a 'Delta' algorithm is provided to directionalise all the distance elements; mho and quadrilaterals. If the Delta directional is not used i.e. If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Disabled`, the relay reverts to a conventional directional line for mho and quadrilateral. This conventional line is depicted in the DIRECTIONAL QUADRILATERALS section.

If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Enabled`, the IED will also switch to a conventional line if:

- it is set to `Enabled` in ***Static Test*** under *COMMISSION TESTS*
- if there is not enough Delta V and Delta I measurement
- if the memory has elapsed or is not valid (SOTF condition)

If Delta directional is used in conjunction with aided schemes, this Delta algorithm can also provide additional protection in the form of directional comparison protection.

8.6.7.1 DELTA DIRECTIONAL PRINCIPLE AND SETUP

Delta directional looks at the relative phase angle of the superimposed current ΔI (delta I) compared to the superimposed voltage ΔV (delta V), at the instant of fault inception. The delta is only present when a fault occurs and a step change from the pre-fault steady-state load is generated by the fault.

Under healthy network conditions the system voltage is close to Vn nominal and load current flows. Under such steady-state conditions, if the voltage measured on each phase now is compared with a stored memory from exactly two power-system cycles previously, the difference between them is zero. Zero voltage change (ΔV = 0) and zero current change (ΔI = 0), except when there are changes in load current.

When a fault occurs on the system, the delta changes measured are:

ΔV = fault voltage (time “t”) - pre-fault healthy voltage (t-2 cycles)

ΔI = fault current (time “t”) - pre-fault load current (t-2 cycles)

The delta measurements are a vector difference, resulting in a delta magnitude and angle. Under healthy system conditions the pre-fault values are those measured 2 cycles earlier. When a fault is detected the pre-fault values are retained for the duration of the fault.

The changes in magnitude are used to detect the presence of the fault and the angles are used to determine whether the fault is in the Forward or Reverse direction.

The following figure shows the superimposed (delta) sequence networks for a single phase to earth fault.

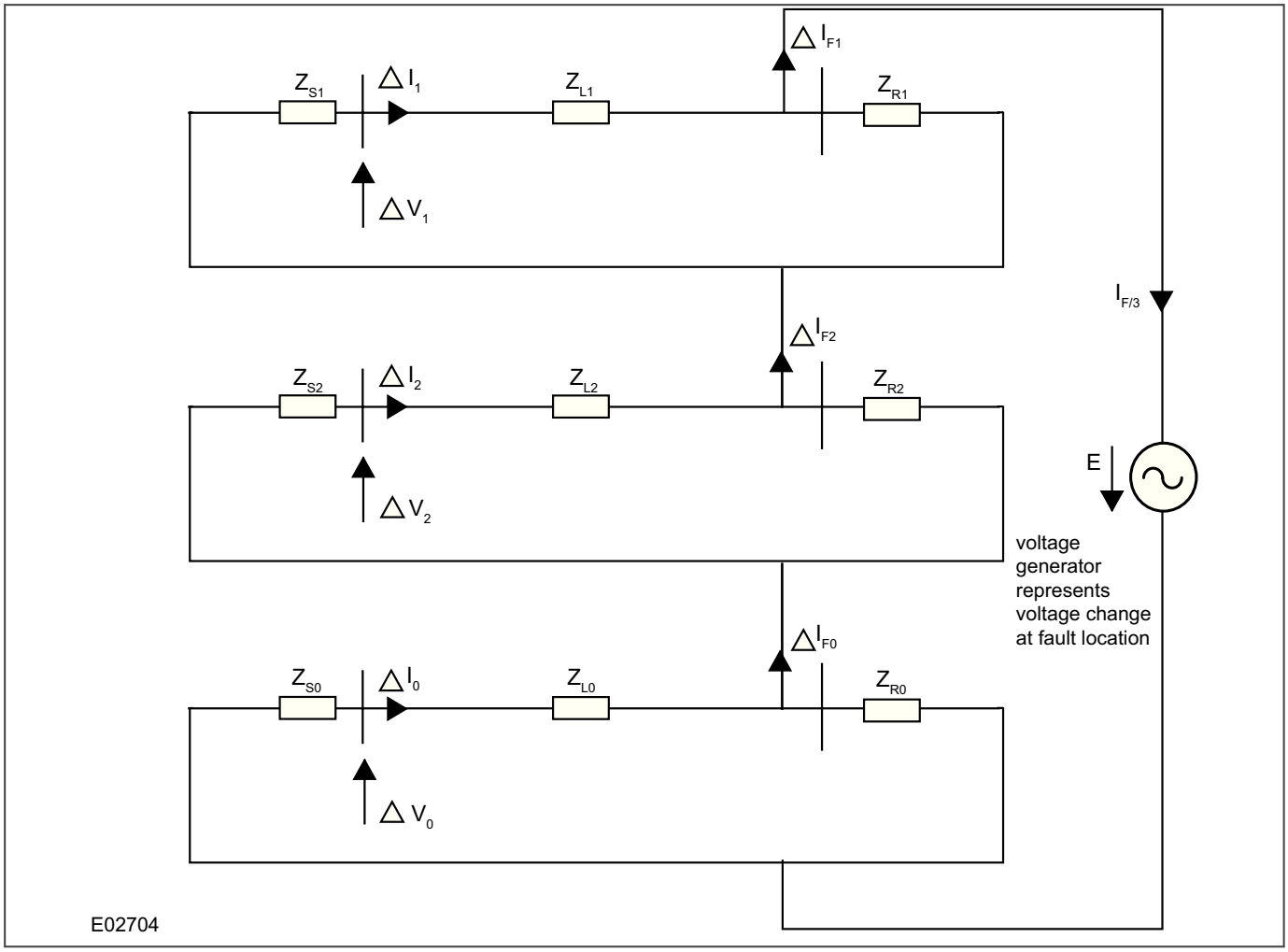


Figure 97: Superimposed sequence networks connection for an internal A-N fault

The fault is shown near to the busbar at end R of the line, and results in a connection of the positive, negative, and zero sequence networks in series. The delta diagram shows that any fault is a generator of Δ, connected at the location of the fault inception. The characteristics of the deltas are:

- The ΔI generated by the fault is equal to the total fault arc current.
- The ΔI splits into parallel paths, with part contribution from source “S” and part from remote end “R” of the line. Therefore each element measures a lower proportion of ΔI.
- The ΔV generated by the fault is equal to the fault arc voltage minus the pre-fault voltage, so it is in anti-phase with the pre-fault voltage.
- The ΔV measured by the protection is the voltage drop across the source impedance behind the protection location. This is generally smaller than the DV measured at the fault location, because the voltage collapse is smaller nearer to the source than at the fault.
- For fault detection, the measured ΔI and ΔV associated with the fault must be greater than the ***Dir I Fwd*** and ***Dir V Fwd*** settings respectively.

8.6.7.2 DELTA DIRECTIONAL DECISION

Delta quantities are generated when a fault starts. The following criteria characterise the fault direction:

For a forward fault:

ΔV is a decrease in voltage, so it is in the negative sense. ΔI is a forward current flow, so it is in the positive sense. Where ΔI and ΔV are approximately in anti-phase, the fault is forward. The exact angle relationship for the forward fault is:

$$\Delta V / \Delta I = -(\text{Source impedance } Zs)$$

where Zs is the source impedance behind the protection.

For a reverse fault

ΔV is a decrease in voltage, so it is in the negative sense. ΔI is an outfeed flowing in the reverse direction, so it is in the negative sense. Where ΔI and ΔV are approximately in phase, the fault is reverse. The exact angle relationship for the reverse fault is:

$$\Delta V / \Delta I = (\text{Remote Source impedance } Zr + ZL)$$

where ZL is the protected line impedance and Zr is the remore end source impedance.

A directional characteristic angle (RCA) setting (***Dir. Char Angle***) allows you to set the centre of the directional characteristic according to the amount by which the current nominally lags the reference ΔV. The characteristic boundary is then +/- 90° either side of the set characteristic angle.

Note:
If Delta directional aided scheme is not used, Distance zone directionalising uses fixed operating thresholds: ΔV=0.5V and ΔI=5%In. If the fault ΔV is below the setting of 0.5V, a conventional distance line ensures correct forward/reverse polarising. For Delta directional aided schemes, sufficient ΔV must be present for tripping to occur.

The delta directional element will produce a forward decision when the angle between the delta volts and delta current shifted by the ***Dir. Char Angle*** setting is greater than 90°. The ***Dir. Char Angle*** setting is the characteristic angle of the source impedance, Zs.

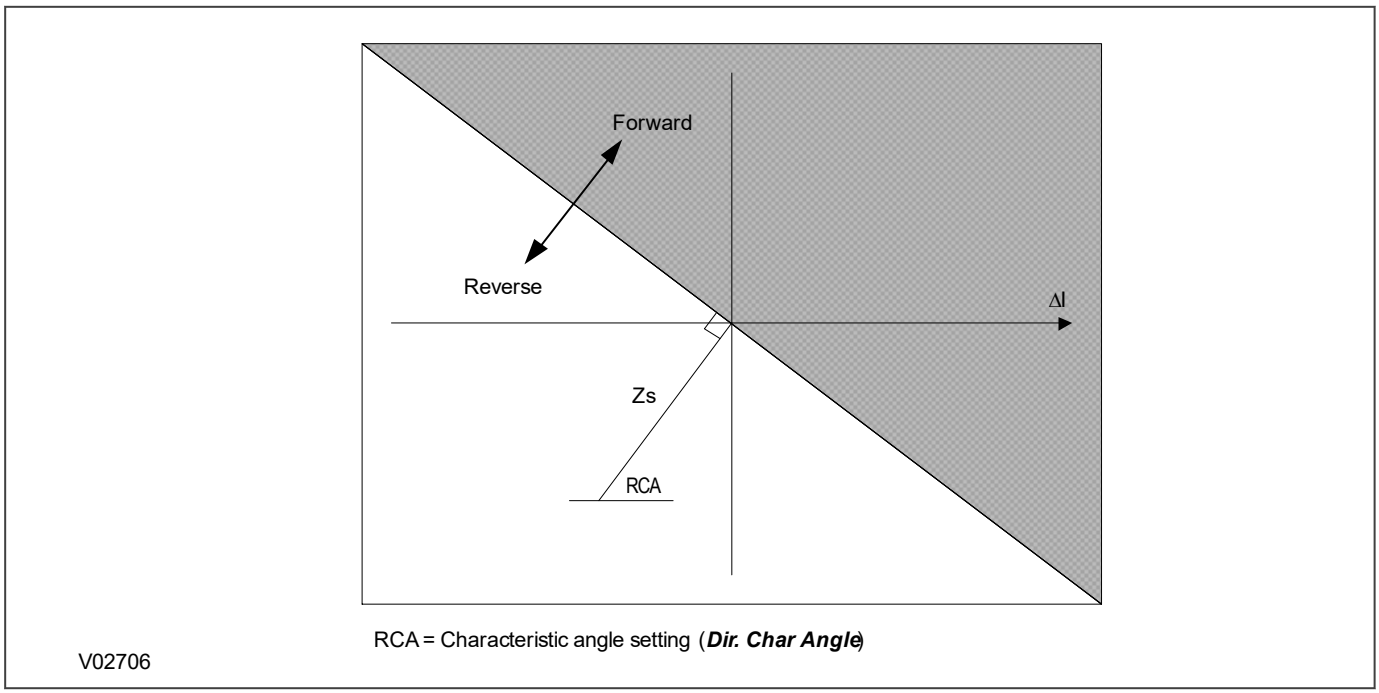


Figure 98: - ΔV Forward and Reverse tripping regions

To facilitate testing of the distance elements using test sets, which do not provide a dynamic model to generate true fault delta conditions, set the ***Static Test*** setting in the *COMMISSION TESTS* column to `Enabled`. This disables phase selector control and forces the protection to use a conventional (non-delta) directional line.

Note:
Some test sets with dynamic models have the facility to include a DC offset. We strongly recommend the use of the DC offset because the waveform created with no DC offset sometimes creates a current step that is not realistic and this could cause a problem in the delta algorithm.

8.6.8 DISTANCE ELEMENT ZONE SETTINGS

The settings for the Distance protection are contained in the *DISTANCE SETUP* and *DIST. ELEMENTS* columns of the relevant settings group.

The Distance protection has a ***Setting Mode*** which is set to `Simple` by default. We recommend the default for most applications.. Instead of entering distance zone impedance reaches in ohms, zone settings are simply entered in terms of percentage of the protected line data specified with the ***Line Impedance*** setting in the *LINE PARAMETERS* column. The setting assumes that the residual compensation factor is equal for all zones. The protection calculates the required reach settings from the percentage settings. The calculated zone reaches are available for viewing but you cannot change a value.

An ‘Advanced’ Setting Mode allows individual distance ohmic reaches and residual compensation factors to be entered for each zone. When ‘Advanced’ mode is selected, all ‘percentage’ settings that are associated to ‘Simple’ setting mode in the *DISTANCE SETUP* column will be hidden and the Distance zone settings need to be entered for each zone in the *DIST. ELEMENTS* column.

If you use the ‘Simple’ Settings Mode, the *DIST. ELEMENTS* column contains a list of what settings have been automatically calculated and applied. This list is useful as a reference for commissioning and periodic injection testing. If you use the ‘Advanced’ Setting Mode, however, you must enter all settings for each zone.

Note:
Distance zones are directionalised by a Delta Directional decision. The characteristic angle for this decision is set with the Delta Directional configuration, in the DISTANCE SETUP column. The default setting is 60°.

8.6.8.1 ADVANCED DISTANCE ZONE SETTINGS

The ***Setting Mode*** is set in the *DISTANCE SETUP* column. There are two possible modes; simple and advanced.

If set to `Simple`, you need only to enter the line parameters such as length, impedances and residual compensation found in the *LINE PARAMETERS* column. You set the reach in terms of percentage of the protected line.

We recommend the `Advanced` setting for networks where the protected and adjacent lines are of dissimilar construction, requiring independent zone characteristic angles and residual compensation. In this setting mode all individual distance ohmic reach and residual compensation settings and operating current thresholds per each zone are accessible.

If you use the advanced setting mode, you also need to set the minimum current sensitivity for each zone (***Zn Sensit. Iph>n***, and ***Zn Sensit. Ignd>n***).

The current sensitivity setting for each zone is used to set the minimum current that must flow in each of the faulted phases before a trip can occur. For example, if a phase A-B line fault is present, the protection must measure both currents Ia and Ib above the minimum set sensitivity.

The default setting is 7.5% In for Zones 1 and 2, and 5% In for other zones, ensuring that distance element operation is not constrained, right through to an SIR ratio of 60.

When quadrilateral characteristics are used, you can set the tilt angle of the impedance reach lines.

In *Advanced s*etting mode, the impedance reach lines of the quadrilateral characteristics are fixed, but not as horizontal reactance lines. To account for phase angle tolerances in the current and voltage transformers, etc., the lines are tilted downwards at a droop of -3°.

In *Advanced s*etting mode, the tilt of the top lines can be changed from these values.

8.6.8.2 DISTANCE ZONE SENSITIVITIES

In the *Simple* ***Setting Mode*** a minimum current sensitivity applies but the value is automatically calculated and applied based on the data entered in the 'Simple' settings fields. The criteria used to calculate the setting value are needed for a minimum value of current flowing in the faulted loop and for the Zone reach point voltage. For Zones other than 1 or 2, the minimum current must be greater than 5% of the rated current and the minimum voltage at the Zone reach point must be 0.25V. The current equating to the reach point criteria can be expressed as 0.25/Zone reach and the sensitivity can be expressed as:

$$\text{Sensitivity} = \max(5\%\text{In}, (0.25/\text{Zone reach}))$$

Zones 1 and 2 are set less sensitive than the reverse Zone 4. This ensures stability of the protection in either an overreaching or a blocking scheme. For Zones 1 and 2, the same criteria are applied as for the other Zones. Also a minimum sensitivity criterion is applied, depending on the Zone 4 sensitivity. The sensitivity must exceed 1.5 x Zone 4 sensitivity and can be expressed as:-

$$\text{Sensitivity (Z1, Z2)} = \max(5\%\text{In}, (0.25/\text{Zone reach}), (1.5 \times \text{Zone 4 sensitivity}))$$

Or

$$\text{Sensitivity (Z1, Z2)} = \max(5\%\text{In}, (0.25/\text{Zone reach}), (1.5 \times (0.25/\text{Zone 4 reach})))$$

The dependency on the Zone 4 element always applies, even if Zone 4 is disabled.

The default reach setting for Zones 1, 2, and 4 are 80%, 120%, and 150% respectively. For these settings the zone-dependent terms can be reduced to:

$$0.25/\text{Zone 1 reach} = 0.25/(0.8 \times \text{line impedance})$$

$$0.25/\text{Zone 2 reach} = 0.25/(1.2 \times \text{line impedance})$$

$$1.5 \times (0.25/\text{Zone 4 reach}) = 0.25/\text{line impedance}$$

In such cases, for Zone 1, the dominant Zone reach term is that of Zone 1 and the equation can be reduced to:

$$\text{Sensitivity (Z1)} = \max(5\%\text{In}, (0.25/(0.8 \times \text{line impedance})))$$

For lines with an impedance of less than 6.25 Ω the Zone 1 reach term dominates and the sensitivity is greater than 5% In. Above this line impedance the sensitivity is 5% In.

Similarly, for Zone 2, the dominant Zone reach term is that of Zone 4 and the equation can be reduced to:

$$\text{Sensitivity (Z2)} = \max(5\%\text{In}, (0.25/\text{line impedance}))$$

For lines with an impedance of less than 5 Ω the Zone reach term dominates and the sensitivity is greater than 5% In. Above this line impedance the sensitivity is 5% In.

In *Advanced* setting mode the same qualifications for distance zone minimum sensitivity as minimum sensitivity should be applied to ensure distance element accuracy.

8.6.9 CAPACITOR VT APPLICATIONS

The device provides a setting for capacitor-coupled voltage transformer (CVT) applications. This setting is ***CVT Filters*** and is found in the *DISTANCE SETUP* column. The default setting is *Disabled* which us used for conventional wound voltage transformers. If CVTs are used you can set ***CVT Filters*** to either *Passive*, or *Active* to reduce the effects of transient components caused by close up faults.

8.6.9.1 CVTS WITH PASSIVE SUPPRESSION OF FERRORESONANCE

Passive suppression to reduce the effects of transient components that could be caused by close up faults uses an anti-resonance design and the resulting transient distortion is fairly small. Passively suppressed CVTs are sometimes classed as type 2. In passive CVT applications, the effect on characteristic accuracy is generally negligible for source to line impedance ratios of less than 30 (SIR < 30). However, with a high Source-to-Line Impedance Ratio (SIR), it is advisable to set ***CVT Filters*** to `Passive`.

By setting ***CVT Filters*** to `Passive`, the protection can trip at sub-cycle speeds, unless the actual SIR is above that which is set. If the SIR is estimated to be higher than the setting, the instantaneous operating time is increased by about a quarter of a power frequency cycle. The protection estimates the SIR as the ratio of nominal rated voltage Vn to the size of the comparator vector IZ (in volts):

$$SIR = Vn/IZ$$

where:

- Vn = Nominal phase to neutral voltage
- I = Fault current
- Z = Reach setting for the zone concerned

Therefore, for slower operation, I needs to be low, as restricted by a relatively weak infeed and Z needs to be small, as for a short line.

8.6.9.2 CVTS WITH ACTIVE SUPPRESSION OF FERRORESONANCE

Active suppression to reduce the effects of transient components that could be caused by close up faults uses a tuned L-C circuit in the CVT. The damping of transients is not as efficient as for passive suppression. Active suppression CVTs are often called type 1 CVTs. In active CVT applications, to ensure reach point accuracy, the ***CVT Filters*** setting should be set to `Active`. The protection varies according to the calculated source to line impedance ratio SIR (= Vn / IZ).

where:

- Vn = Nominal phase to neutral voltage
- I = Fault current
- Z = Reach setting for the zone concerned

Sub-cycle tripping is maintained for lower SIRs, up to a ratio of 2. The instantaneous operating time is increased by about a quarter of a power frequency cycle at higher SIRs.

Transients caused by voltage dips, however severe, do not affect the protection's directional measurement because it uses voltage memory.

8.6.10 LOAD BLINDING

Load blinders are provided for both phase and earth fault distance elements, to prevent incorrect-tripping for heavy load flow. A blinder envelope which surrounds the expected worst case load limits should be configured to block tripping for any impedance measured in the blinded region. Only a fault impedance which is outside the area bounded by the load blinders is allowed to cause a trip. The blinder characteristics are shown in the following figure:

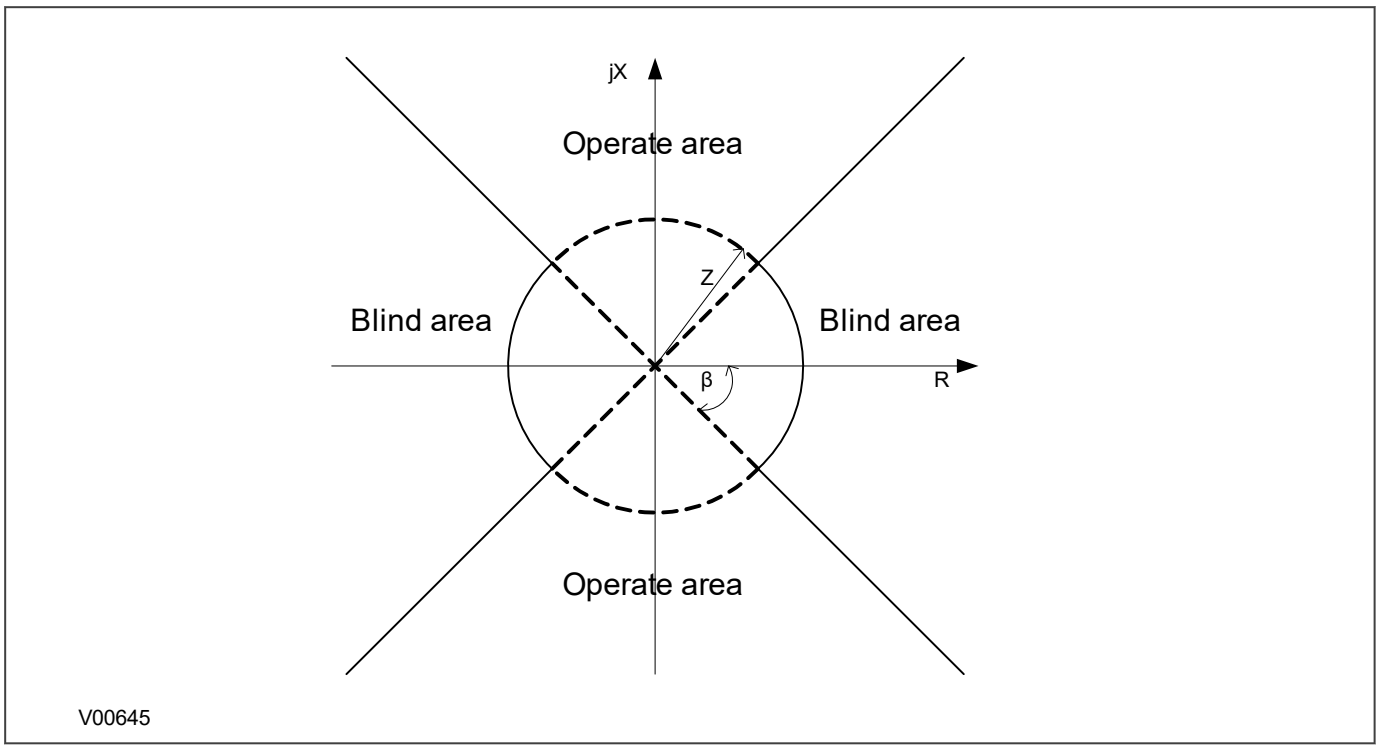


Figure 99: Load blinder characteristics

- Z denote values for the Load/B Impedance settings. These set the radius of the phase and earth under-impedance circle.
- ß denote values for the Load/B Angle settings. These set the angle of the two blinder boundary lines for phase and earth - the gradient of the rise or fall with respect to the resistive axis.

The protection can allow the load blinder to be bypassed any time that the measured voltage for the phase in question falls below an undervoltage setting. Under such circumstances, the low voltage could not be attributed to normal voltage excursion tolerances on load. A fault must be present on the phase in question, so it is acceptable to override the blinder action and allow the Distance protection to trip for an in-zone measurement. The advantage of bypassing the load blinders is that the resistive coverage for faults near to the protection location can be higher.

To use the load blinders you must set the ***Load Blinders*** setting to `Enabled`. You then set appropriate values for the blinder impedance using the ***Z< Blind Imp Ph*** and ***Z< Blind Imp Gnd*** settings, the β values using the ***Load/B Angle Ph*** and ***Load/B Angle Gnd*** settings, and the undervoltage threshold using the ***Load Blinder V<*** setting.

8.6.11 CROSS COUNTRY FAULT PROTECTION

"Cross country fault" is a term that has been adopted to cover a fault scenario where two separate single-phase faults occur on a system together. For example, where single-pole tripping is employed, if a single phase-to-earth fault occurs, the voltages on the other phases can rise above normal. This may cause a breakdown elsewhere on the system and result in another fault involving a different phase to the one on which the original fault occurred.

The distance protection in this product features cross-country override logic, which is built into the phase selector. The logic is dedicated to providing Cross-Country fault protection for solidly-earthed systems. It ensures correct operation a fault in Zone 1 that may evolve to involve a different phase. For isolated or compensated earthing systems a settable phase preferential logic will be used for cross-country faults instead.

The cross-country override logic:

- Prevents possible false operation of the phase-phase distance elements whilst allowing the appropriate Zone1 phase-earth element to trip.
- Acts when the distance protection makes a multiple phase selection (where more than one phase is involved in the fault), but only one Zone 1 phase-earth element picks up. Only "on-angle" operation of the Zone 1

phase-earth element can activate the logic. this prevents incorrect operation due to impedance encroachment.

- Allows only one Zone 1 phase-earth element to operate. The operation of that element must match the phase pick-up indication of the phase selector. For example, if the original phase selection indicated involvement of only B and C phases, the logic could allow a BN trip or a CN trip to override the phase-phase selection, but override by the AN element is not allowed.
- Does not apply if more than one forward Zone 1 element picks up. In this case the fault is considered multi-phase and the protection trips three-pole.

Note:
Load blinding can be applied for phase and earth characteristics. Residual compensation is not applied. Phase characteristics use phase-to-phase voltage and phase-to-phase current. Earth fault characteristics use phase-to-neutral voltage and phase-to-neutral current.

8.7 DISTANCE ISOLATED AND COMPENSATED SYSTEMS

8.7.1 PETERSEN COIL EARTHED SYSTEMS

A Petersen Coil earthing system is used in compensated earthing systems, as well as being used in cases of high impedance earthing. Petersen Coil earthed systems (also called compensated or resonant systems) are commonly found in areas where the system consists mainly of rural overhead lines. They are particularly beneficial in locations which are subject to a high incidence of transient faults. In a Petersen Coil earthed system, the network is earthed via a reactor, whose reactance is tuned to be nominally equal to the total system capacitance to earth. Similar to insulated systems, if a single-phase to earth fault is applied to a Petersen Coil earthed system, under steady state conditions no earth fault current flows. The effectiveness of the method in reducing the current to zero is dependent on the accuracy of the tuning of the reactance value and any changes in system capacitance (for example due to system configuration changes) require changes to the coil reactance. In practice, perfect matching of the coil reactance to the system capacitance is difficult to achieve, so that a small earth fault current will flow.

In isolated and compensated earthed systems, if an earth fault current is below a certain level, then the fault will self-extinguish due to the low current magnitude. It therefore appears as a transient phenomenon. The figure below shows earth fault current levels, below which they self-extinguish on these types of system. Statistics demonstrate that around 80% of earth faults in Petersen Coil earthed systems self-extinguish. This, in part, explains their popularity.

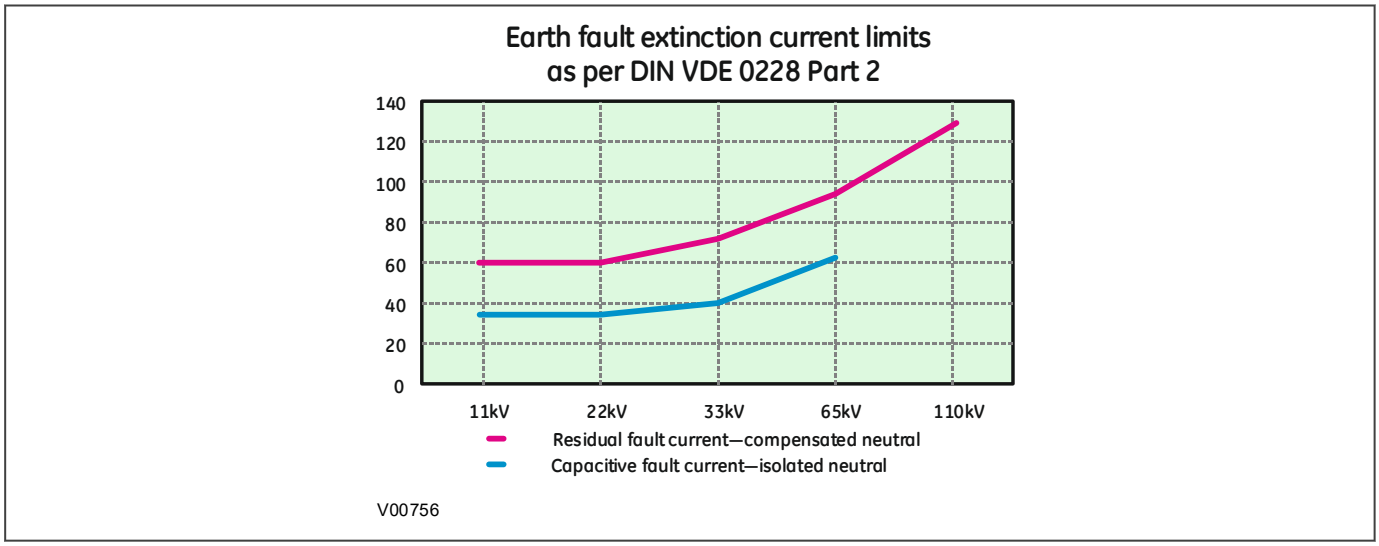


Figure 100: Current level (amps) at which transient faults are self-extinguishing

The following figure depicts a simple network earthed through a Petersen Coil reactance. It can be shown that if the reactor is correctly tuned, theoretically no earth fault current will flow.

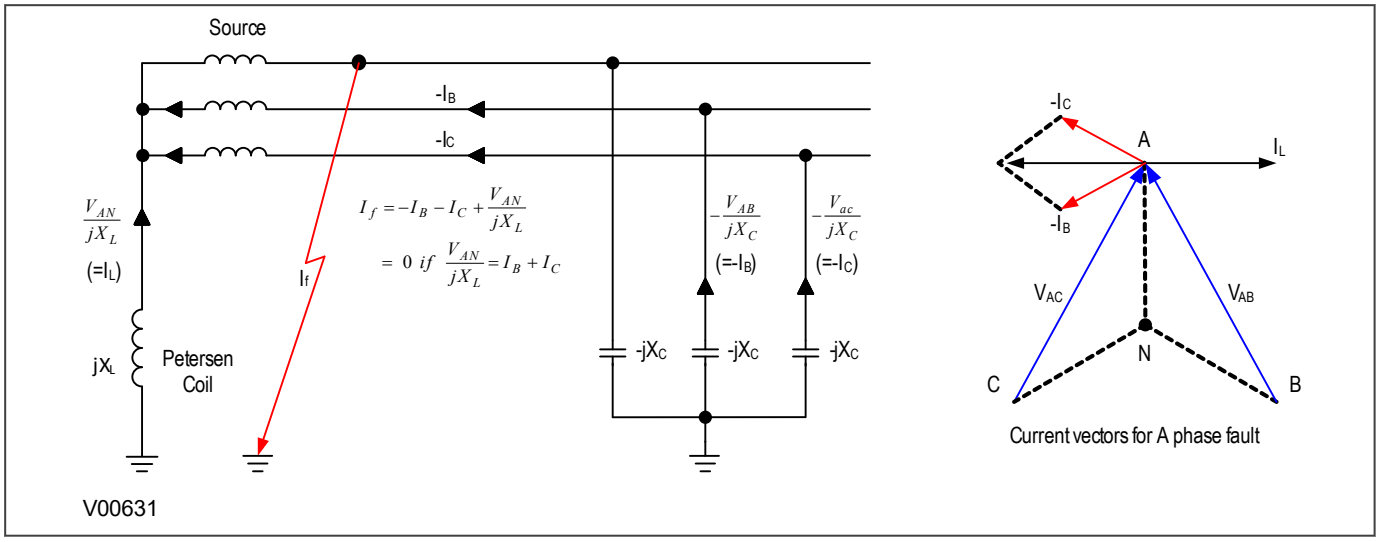


Figure 101: Earth fault in Petersen Coil earthed system

Consider a radial distribution system earthed using a Petersen Coil with a phase to earth fault on phase C, shown in the figure below:

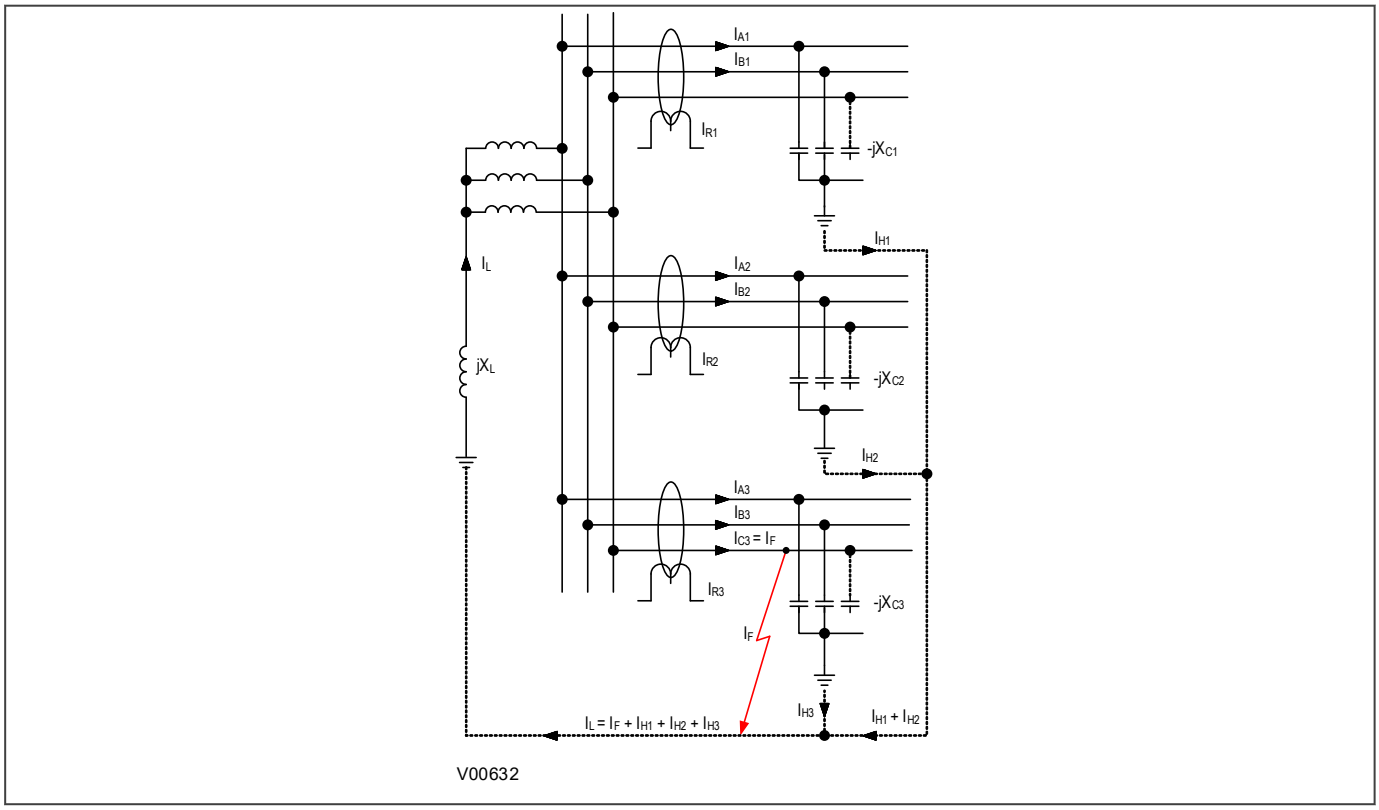


Figure 102: Distribution of currents during a Phase C fault

Assuming that no resistance is present in X_L or X_C, the resulting phasor diagrams will be as shown in the figure below:

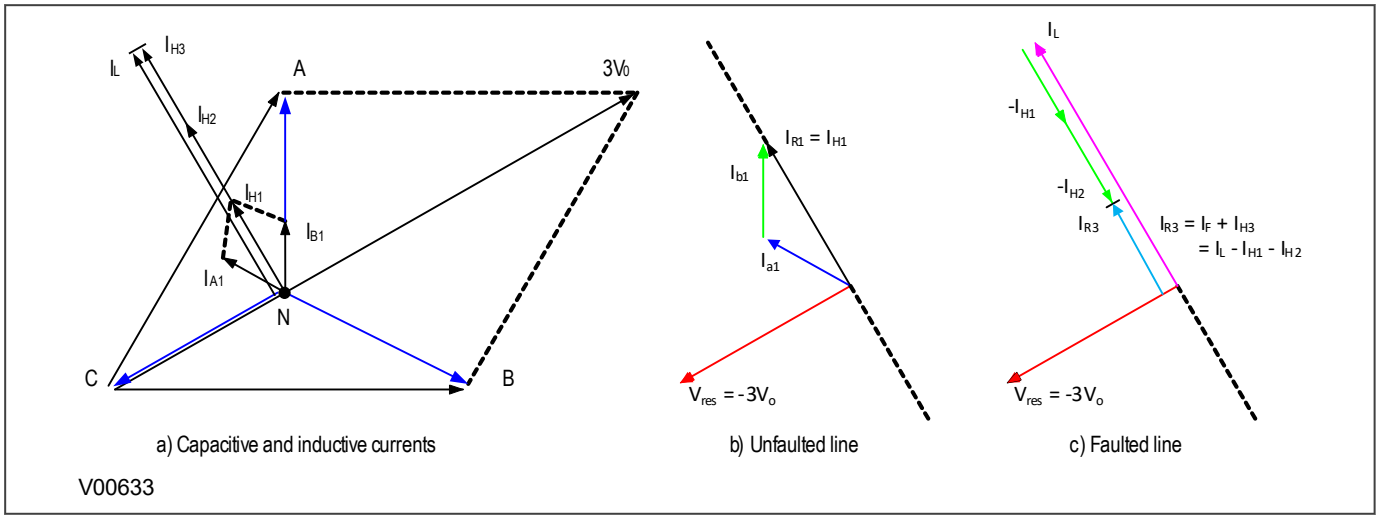


Figure 103: Phasors for a phase C earth fault in a Petersen Coil earthed system

It can be seen that:

- The voltage in the faulty phase reduces to almost 0V
- The healthy phases raise their phase to earth voltages by a factor of √3
- The triangle of voltages remains balanced
- The charging currents lead the voltages by 90°

Using a core-balance current transformer (CBCT), the current imbalances on the healthy feeders can be measured. They correspond to simple vector addition of I_{A1} and I_{B1}, I_{A2} and I_{B2}, I_{A3} and I_{B3}, and they lag the residual voltage by exactly 90º.

The magnitude of the residual current I_{R1} is equal to three times the steady-state charging current per phase. On the faulted feeder, the residual current is equal to I_L - I_{H1} - I_{H2} (C). This is shown in the zero sequence network shown in the following figure:

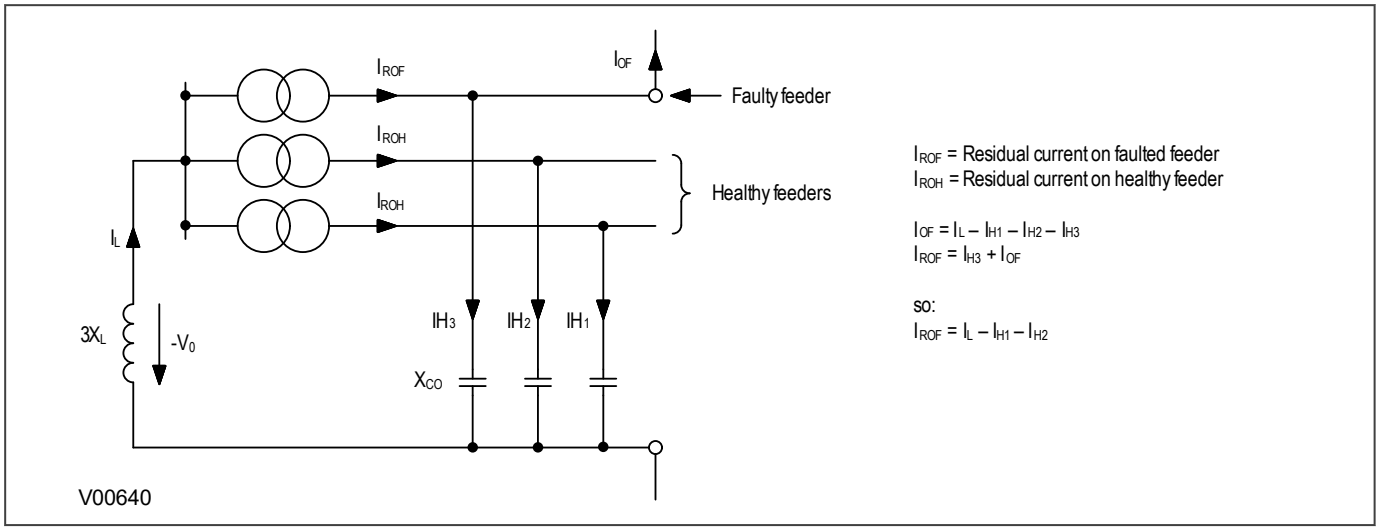


Figure 104: Zero sequence network showing residual currents

In practical cases, however, resistance is present, resulting in the following phasor diagrams:

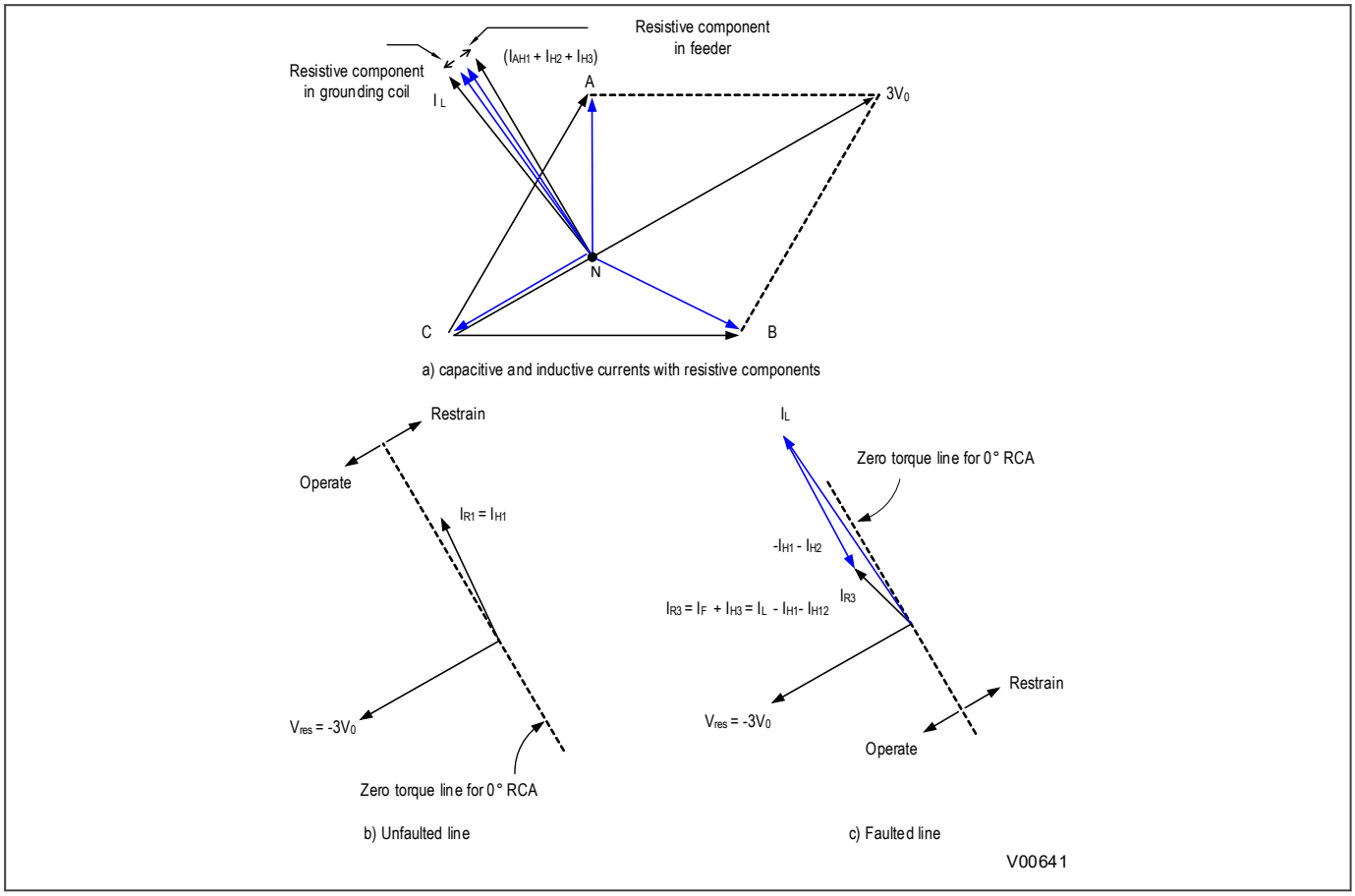


Figure 105: Phase C earth fault in Petersen Coil earthed system: practical case with resistance present

If the residual voltage is used as the polarising voltage, the residual current is phase shifted by an angle less than 90° on the faulted feeder, and greater than 90° on the healthy feeders. With an RCA of 0°, the healthy feeder residual current will fall in the 'restrain' area of the characteristic while the faulted feeder residual current falls in the 'operate' area.

Often, a resistance is deliberately inserted in parallel with the Petersen Coil to ensure a measurable earth fault current and increase the angular difference between the residual signals to reinforce the directional decision.

Directionality is usually implemented using a Wattmetric function, or a transient earth fault detection function (TEFD), rather than a simple directional function, since they are more sensitive. For further information about TEFD, refer to Transient Earth Fault Detection in the Current Protection Functions chapter.

8.7.2 EARTH FAULT DISTANCE PROTECTION FOR ISOLATED AND COMPENSATED SYSTEMS

There are four types of fault that need to be considered when providing distance protection for isolated or compensation earthed systems. These are faults involving three phases, phase to phase faults, faults involving just a single-phase to earth, and cross-country faults involving separate single phase to earth faults.

Faults involving three phases and phase to phase faults do not require special attention; tripping is in accordance with zone impedance limits, fault direction, and zone time delay.

Faults on isolated or compensated earthed systems involving single-phase to earth, or cross-country faults do require special attention.

8.7.2.1 SINGLE-PHASE TO EARTH FAULTS ON ISOLATED OR COMPENSATED SYSTEMS

On isolated or compensated earthed systems, a single-phase to earth fault does not lead to a short circuit as only a small capacitive or compensated current flows to earth. In most cases, the earth fault will self-extinguish. In the remaining cases, the system can continue to operate with the earth fault present, until the fault is located and removed by isolating the faulted feeder. Indication of the earth fault can be provided by Wattmetric function, or a Transient Earth Fault Detection function (TEFD).

For a fault on a solidly earthed network, distance protection is required to trip as quickly as possible to isolate the fault. This is for all fault types including a single-phase to earth fault. In isolated or compensation-earthed systems, a single-phase to earth fault needs to be correctly identified for network control, but instantaneous tripping should not happen since the system can be (at least for a certain period of time) remain connected - as the magnitude of the fault current will not be very high - and/or the fault will in most cases self-extinguish.

Moreover, for a solid earth fault, the voltage on the faulted phase may be 0V across the whole of the galvanically connected network. Using a collapsed voltage in conjunction with the load current would give measured impedance values on the faulted phase of 0Ω across the network, causing incorrect, and uncontrolled, tripping.

Since distance protection should not operate for a single-phase to earth fault, pick up of fault detection elements under single-phase to earth fault conditions must not lead to tripping. This can be a particular problem on large isolated networks, where capacitance to earth is large. When a single-phase to earth fault occurs, the voltages on the unfaulted phases increase relative to earth, and so too do the associated capacitive earth currents. During the initial half cycle after fault inception, the arc-ignition earth current amplitude of the disturbance may be much higher than nominal current, with a frequency close to the nominal system frequency. To prevent incorrect detection during single-phase to earth faults, it is common practice to delay single-phase to earth fault detection on isolated or compensation-earthed systems by a short delay. This delay is bypassed if the fault evolves into a double earth fault.

8.7.2.2 CROSS-COUNTRY FAULTS ON ISOLATED OR COMPENSATED SYSTEMS

While a single-phase to earth fault is present on an isolated or compensation earthed system, the phase to earth voltage on the healthy phases rises by a factor of $\sqrt{3}$. Due to this rise, double earth faults (or cross-country faults) may result. The double earth fault is similar to a two-phase fault; however, for the double earth faults, the fault path is from one earth-fault location to another, via earth. The second fault may be anywhere on the system, depending on where the weakest point in the insulation is located.

The likelihood of a double earth fault increases as the size of the network increases. The protection strategy usually applied for cross-country faults is to isolate one of the fault locations, with the expectation that the second fault location will then self-extinguish similar to a single-phase to earth fault. The faulted line can then be tripped manually once the fault location has been identified. Distance protection applied to isolated systems must have a so-called double earth fault phase preference, which selects a predefined phase earth loop for measurement across the entire galvanically connected network.

In the case of cross-country faults, measurements from the phase to phase loops between the two fault locations do not produce useful results as the phase currents belong to different short circuit loops. For the second fault, earth loops will measure the fault impedance more accurately. For a cross-country fault, all devices across the network should follow either a so-called "cyclic" logic or an "acyclic" logic to select a phase preference for the impedance measurement. This is used to determine which part of the system should be isolated by three-phase tripping. Tripping will allow the rest of the network to continue to operate (single earth-fault present, but supply maintained). Then, when the single phase-earth fault has been located, the faulted section can be tripped manually.

The most commonly used phase preference logic is C(A) acyclic (that is C before A before B), but other preferences can be used.

8.7.3 IMPLEMENTATION OF DISTANCE PROTECTION FOR ISOLATED AND COMPENSATED NETWORKS

When applying distance protection to compensated or isolated systems, the following key points must be taken into account:

- Distance protection must not trip for a single-phase to earth fault
- In the case of cross-country faults, the protection methods are different from that of solidly earthed systems. In this case either a cyclic or an acyclic logic should be used to select a phase preference for the impedance measurement

8.7.3.1 NETWORK EARTHING SYSTEM SETTING

The setting ***Dist.Earth Mode*** in the *DISTANCE SETUP* column defines the behaviour of the distance protection function according to the type of earthing system. The setting options are:

- *Is/Comp Earthing* for isolated or compensated systems
- *Standard* for directly earthed systems

If *Is/Comp Earthing* is selected:

- Distance protection is blocked for a single-phase to earth fault
- A earth fault is detected using the neutral current (IN) and/or the neutral voltage (VN)
- It has no influence on two-phase or three-phase fault performance
- In the case of cross-country faults, either a cyclic or an acyclic logic is invoked to select a phase preference for the impedance measurement
- The DDB signal ***Is/Comp Enabled*** (1983) is asserted

8.7.3.2 FIRST EARTH FAULT DETECTION

In isolated or compensated mode, no trip should occur for a single phase to earth fault. Moreover its detection by means of an impedance criteria would lead to false information as voltages around the galvanic network will be 0V for the faulty phase. Instead, an earth fault is detected by comparing I_N and/or V_N with a settable threshold.

You can choose to use V_N only, I_N only, V_N OR I_N, or V_N AND I_N as your selection criteria. The mode is set by the setting ***1P Mode*** in the *DISTANCE SETUP* column. The single-phase to earth fault signal (***IS/Comp EF***) is then produced after a time delay set by ***1P Time delay***.

I_N> can be set from 0.05In to 1In in steps of 10 mA. V_N can be set from 1V to 80V in steps of 1 V.

A pick-up timer, is available for the detection of the first earth fault. This can be set from 0 to 10 seconds in steps of 10 ms.

The mode selector decides whether the single-phase to earth fault is determined by VN> only, IN> only, VN> or IN>, or VN> and IN>. The mode is set by the setting ***1P Mode*** in the *DISTANCE SETUP* column. The single-phase to earth fault signal (***IS/Comp EF***) is then produced after a time delay set by 1P Time delay.

8.7.3.2.1 NEUTRAL VOLTAGE CRITERIA

The influence of earth current in a fault can be determined by considering the changes in phase to phase and neutral displacement voltages. During earth faults, a significant displacement of the neutral voltage is expected, whilst no imbalance of the voltage triangle is to be expected. The following figure shows a Phase A to earth fault.

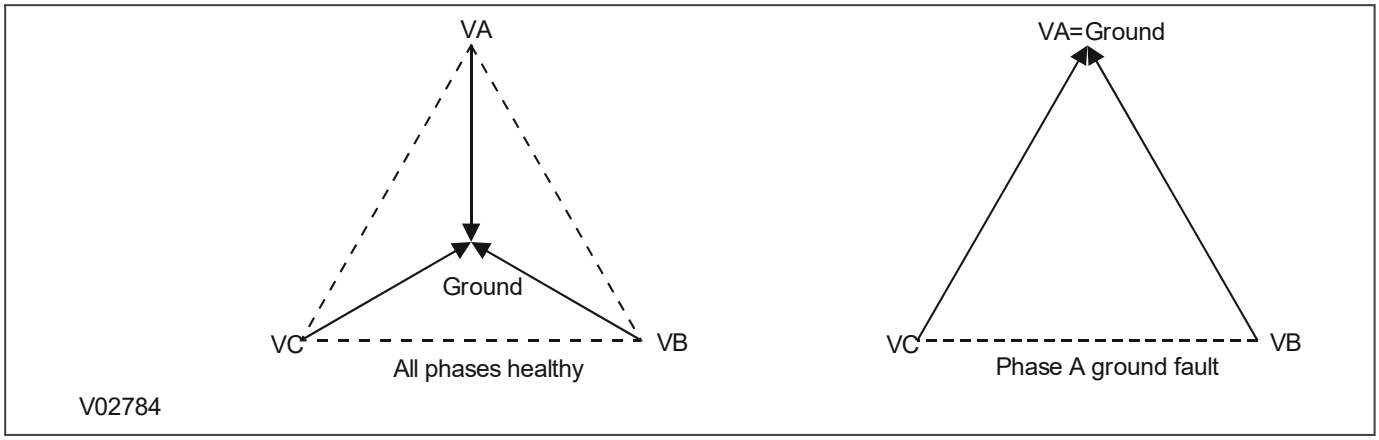


Figure 106: Voltage distribution in an isolated system for a Phase-A-to-Earth fault

Therefore, we can establish an earth fault by seeing if the neutral voltage V_N exceeds a settable threshold ***VN> Voltage Set***, and checking whether the phase-phase voltages are still balanced.

0.8(max. V_{ph-ph}) < (min. V_{ph-ph})

Neutral displacement is established by comparing the neutral voltage VN with a threshold set by the setting, ***VN> Voltage Set***

8.7.3.2.2 NEUTRAL CURRENT CRITERIA

The bias neutral level detector (LDBN), detailed in the Biased Neutral Current Detector section, is used to improve stability and is complemented with an additional minimum threshold controlled by setting ***IN> Current set*** . A negative sequence current check is also performed for long and heavily loaded lines.

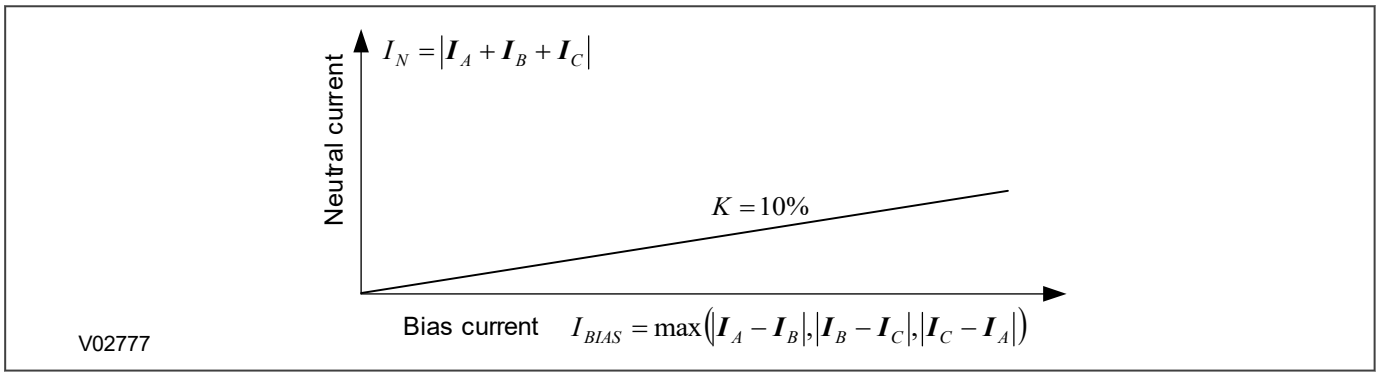


Figure 107: Biased Neutral Current Detector

8.7.3.2.3 RELEVANT SETTINGS FOR FIRST EARTH FAULT DETECTION

The following settings are visible if the setting ***Dist.Earth Mode*** is set to `Is/Comp Earthing`.

IN> Current Set: Sets the threshold for the first fault earth fault overcurrent (default – 0.1In)

VN> Voltage Set: Sets the threshold for the first fault earth fault overvoltage (default – 12V)

1P Mode: Sets the first fault detection method (default – VN>)

1P Time Delay: Sets the first fault pickup delay (default – 50 ms)

8.7.3.2.4 FIRST EARTH FAULT DETECTION

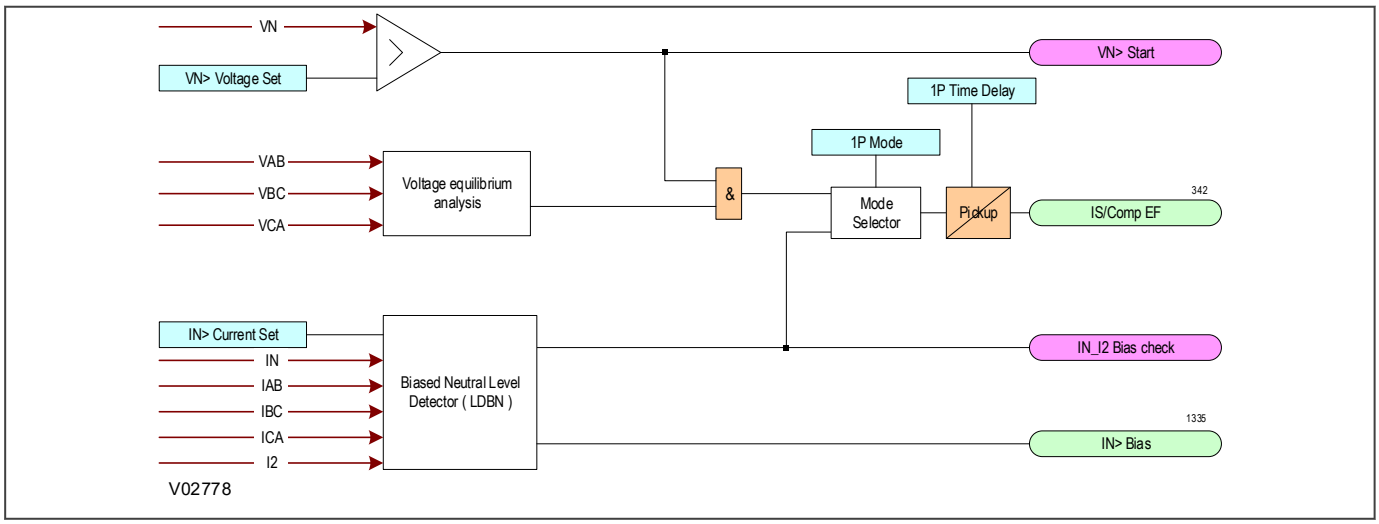


Figure 108: First earth fault detection

Detection of the first fault primes the detection of a second earth fault and blocks tripping of phase to phase elements for zones 1,2,3,4 (zones P, Q, R and S do not get blocked). It also creates a DDB signal indicating a single-phase earth fault (***IS/Comp EF***). Typically, with zones P and Q, the external starting zones will be used to detect if a second earth loop converges into the impedance characteristic.

The *VN*> *Start* signal is established by comparing the neutral voltage *VN* with a threshold set by the setting ***VN> Voltage Set***. This signal is gated with another signal indicating whether the phase voltage triangle is balanced or not and then fed into the mode selector. If the voltage triangle is balanced and there is an overvoltage condition, then a single-phase fault is indicated.

The mode selector decides whether the single phase-to-earth fault is determined by *VN*> only, *IN*> only, *VN*> or *IN*>, or *VN*> and *IN*>. The mode is set by the setting ***1P Mode*** in the *DISTANCE SETUP* column. The single phase-to-earth fault signal (***IS/Comp EF***) is then produced after a time delay set by ***1P Time Delay***.

8.7.3.3 FAULT DETECTION LOGIC

It is unlikely that a second fault would occur on the same phase, because the phase to neutral voltage on this phase has collapsed to zero as a result of the first fault. However, a second fault is highly likely in one of the other phases as the voltage has increased by a factor of √3 and the extra voltage will put more stress on the insulation, increasing the likelihood of a fault further down the line.

A second earth fault (on a different phase) will cause an imbalance in the voltage triangle. This is used as part of the second fault detection process. The criteria for the detection of a second fault is as follows:

A second earth fault is confirmed if a first earth fault has been detected AND the phase to phase voltage triangle is unbalanced AND the neutral voltage has exceeded the set threshold AND the neutral current has exceeded the level set by the threshold together with the bias neutral level detector (LDBN).

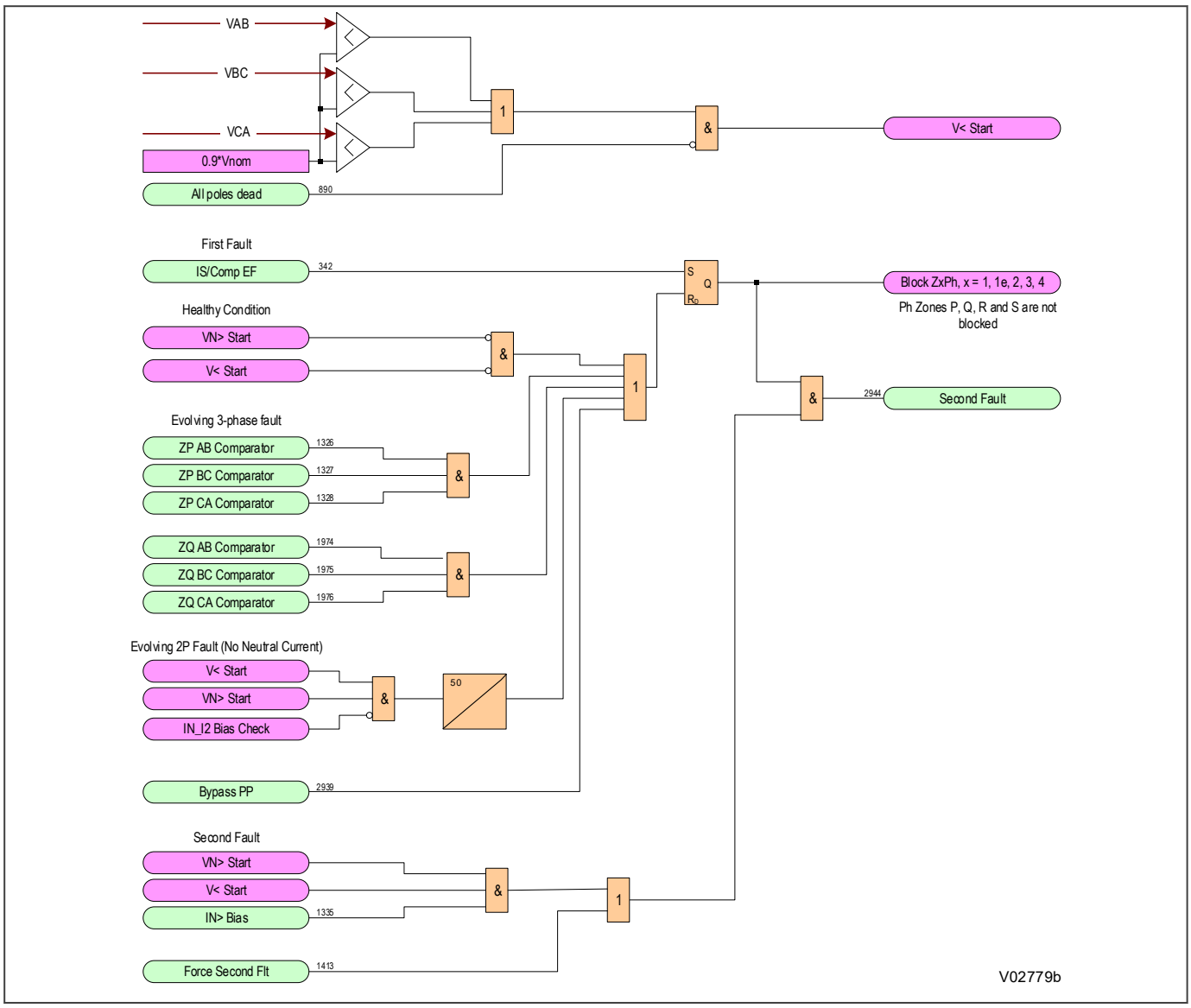


Figure 109: Second earth fault detection logic

A second fault is detected if additionally there is a neutral overvoltage, imbalance in the voltage triangle (phase undervoltage) and there is enough neutral overcurrent (a minimum of 50 mA for correct device operation).

8.7.3.4 PHASE PREFERENTIAL LOGIC

With double earth faults (cross-country faults), the aim is to isolate one of the fault locations and expect that the fault at the other location will self-extinguish, or will be tripped manually after successful detection. To achieve this for isolated or compensated systems, the distance protection must have a preference as to which phase-to-earth loop to measure.

There are two types of priority criteria; acyclic and cyclic.

Acyclic criteria are such that one of the phases is always the lowest priority. For example, A(B) Acyclic logic means: phase A is higher priority than phase B, phase B is higher priority than phase C, and phase C is the lowest priority and will never be selected, therefore C has the lowest priority. Acyclic criteria are most commonly used for distribution systems.

Cyclic criteria are such that the priorities of the phases are always compared cyclically. For example, C(A) Cyclic logic means: phase C is higher priority than phase A, phase A is higher priority than phase B, but in this case phase B priority is higher than phase C.

The definitions of all acyclic and cyclic combinations are listed in the following table:

Criterion	Priority	Convergent Loops	Selected Phase
A(B) acyclic	A before B, B before C	AN, BN BN, CN CN, AN AN, BN, CN	AN BN AN AN
B(A) acyclic	B before A, A before C	AN, BN BN, CN CN, AN AN, BN, CN	BN BN AN BN
A(C) acyclic	A before C, C before B	AN, BN BN, CN CN, AN AN, BN, CN	AN CN AN AN
C(A) acyclic	C before A, A before B	AN, BN BN, CN CN, AN AN, BN, CN	AN CN CN CN
B(C) acyclic	B before C, C before A	AN, BN BN, CN CN, AN AN, BN, CN	BN BN CN BN
C(B) acyclic	C before B, B before A	AN, BN BN, CN CN, AN AN, BN, CN	BN CN CN CN
A(C) cyclic	A before C, C before B, B before A	AN, BN BN, CN CN, AN AN, BN, CN	BN CN AN AN
C(A) cyclic	C before A, A before B, B before C	AN, BN BN, CN CN, AN AN, BN, CN	AN BN CN CN

You can set the phase preference with the ***Phase prio. 2pG*** setting in the *SCHEME LOGIC* column.

Note:
*The **Phase prio. 2pG** setting is visible only when the **Dist.Earth Mode** setting is set to `Is/Comp Earthing` and the **BasicScheme Mode** setting is set to `Alternative`.*

8.7.3.4.1 PRIORITY SETTING ENABLE LOGIC

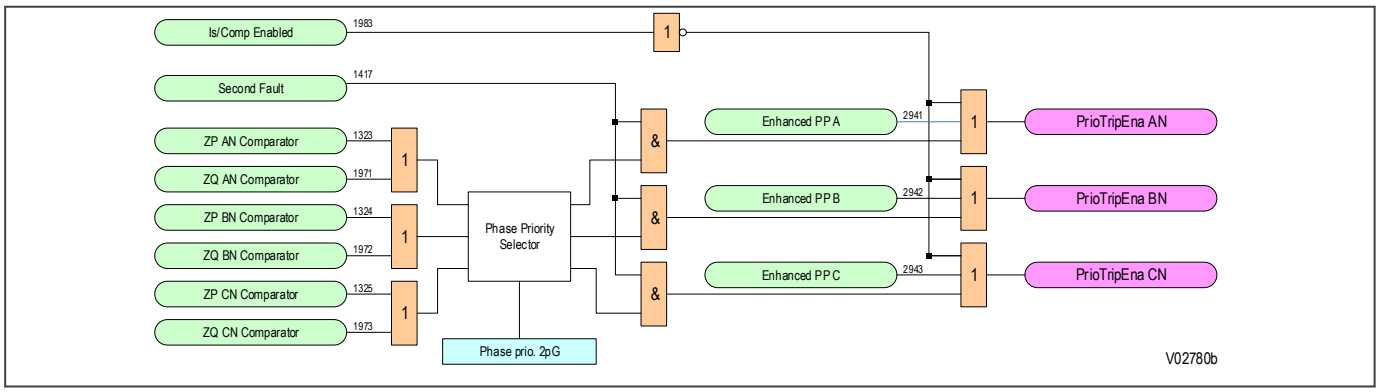


Figure 110: Priority setting enable logic

Note:
The phase preference priority selector requires that at least two of the phase to ground loops, as indicated in the table above, are in Zone P or Q.

In isolated and compensated systems, if the coil is bypassed/faulted and the system becomes effectively solidly earthed, the distance relay shall behave as normal, i.e. no pre-determined phase preference logic to decide which loop will trip. When the coil is in service/not-faulted, the IED shall operate with the phase preference logic. In order to enable this operation and bypass the phase preference logic, an external signal or an internal function can be linked to the DDB 1412 ***ByPass PP*** . This linked input could be an overcurrent start or an external input indicating the coil is bypassed/faulted for example.

8.7.3.4.2 ZONE STARTING LOGIC

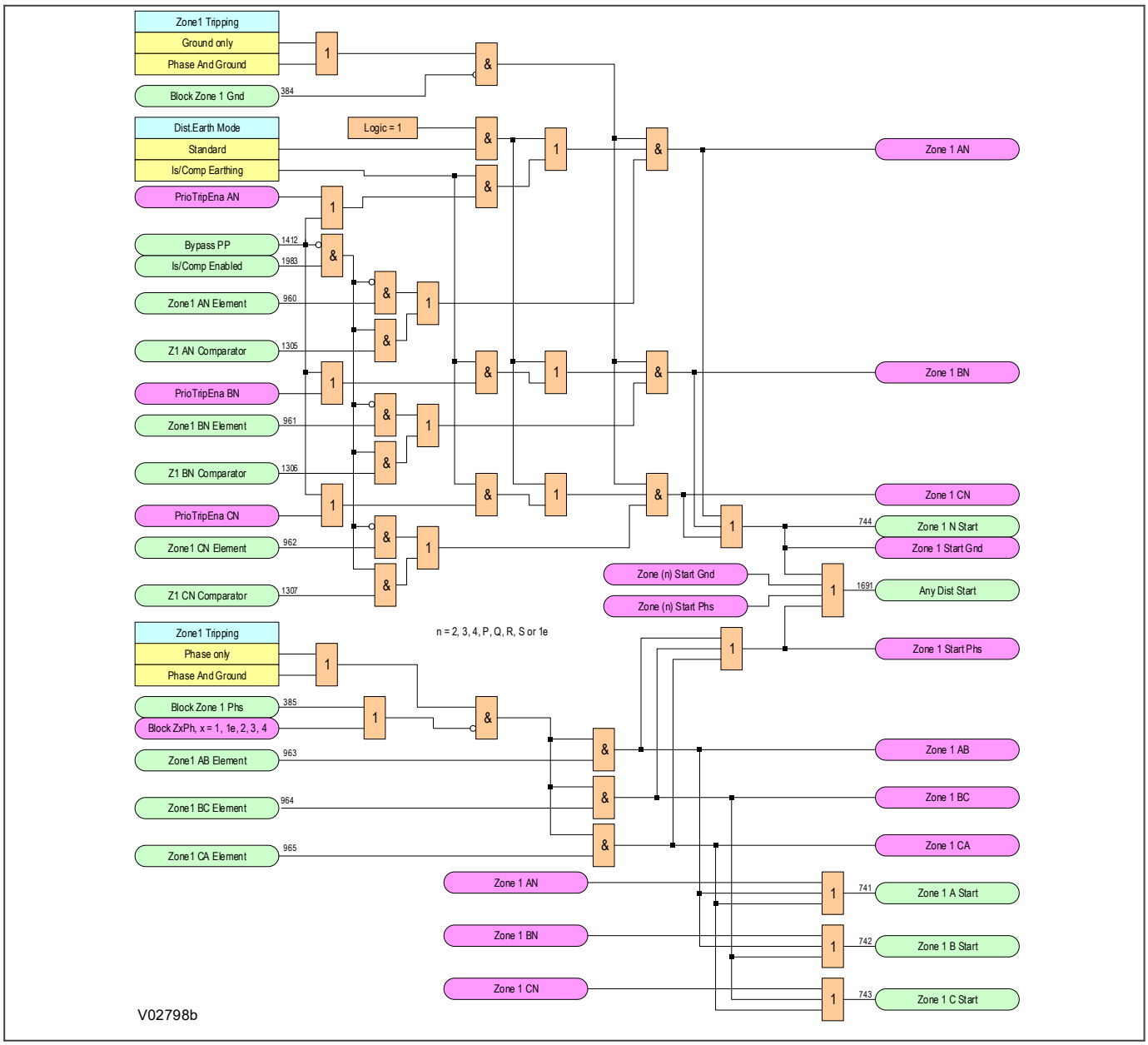


Figure 111: Zone starting logic

8.7.3.4.3 ZONE TIMER LOGIC

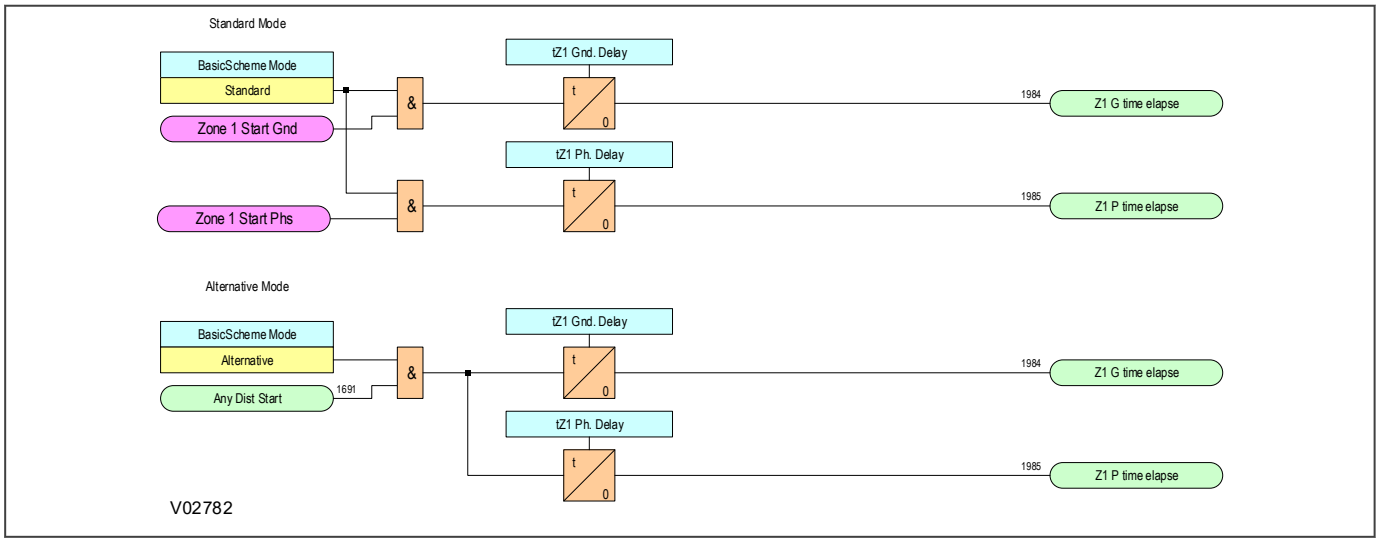


Figure 112: Zone timer logic

Note:
Although the diagram above shows zone 1 logic only, the logic for all other zones follows the same principals.

8.7.3.4.4 ZONE TRIP LOGIC

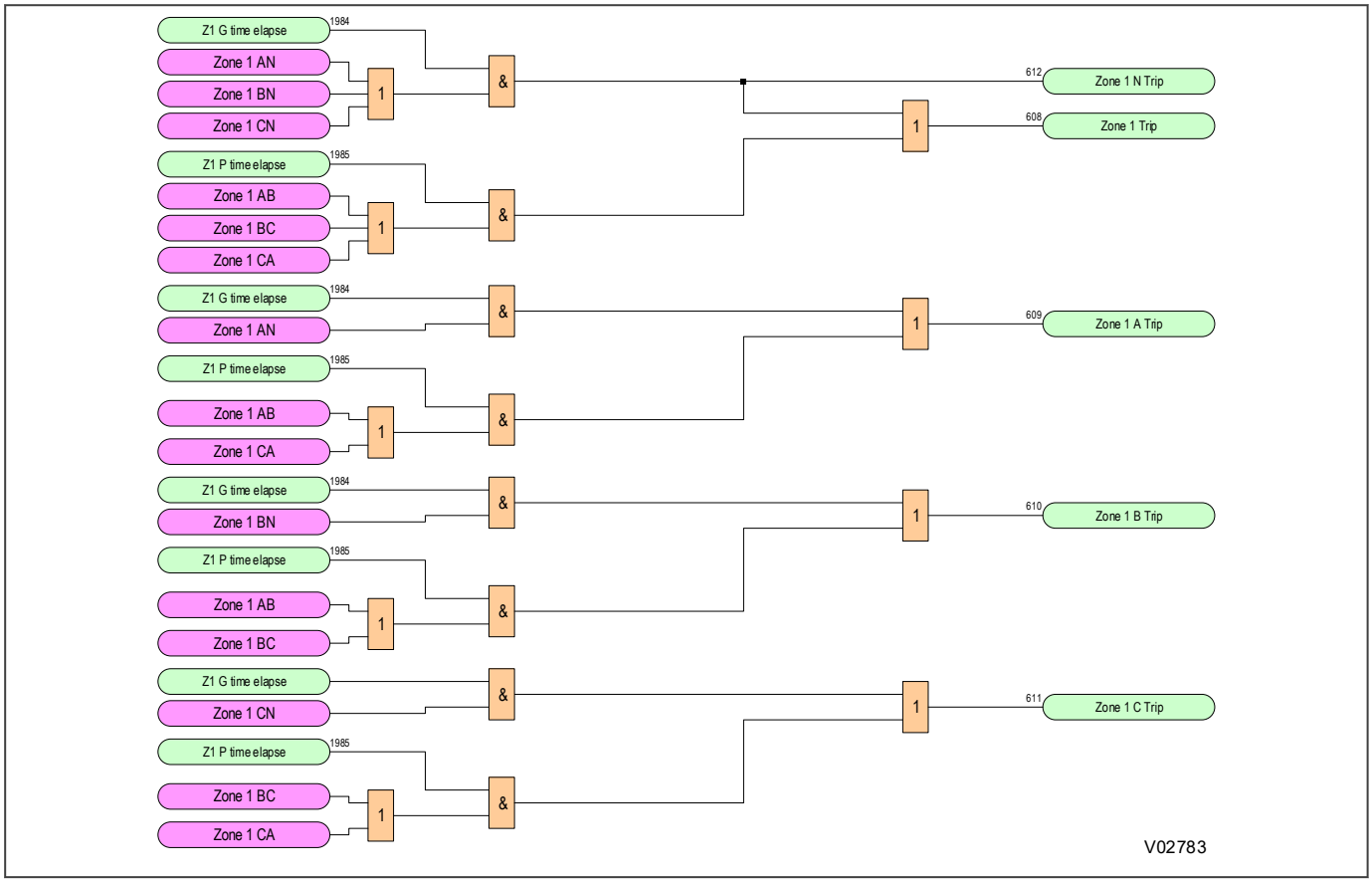


Figure 113: Zone trip logic

Note:
Although the diagram above shows zone 1 logic only, the logic for all other zones follows the same principals.

8.8 APPLICATION NOTES

8.8.1 SETTING MODE CHOICE

This product has two setting modes for distance protection: *Simple*, or *Advanced*. In the majority of cases, we recommend the *Simple* setting. Using the *Simple mode*, you need only enter the line parameters such as length, impedances and residual compensation. You set the reach in terms of percentage of the protected line.

We recommend the *Advanced* setting mode for networks where the protected and adjacent lines are of dissimilar construction, requiring independent zone characteristic angles and residual compensation. In *Advanced* setting mode all individual distance ohmic reach and residual compensation settings and operating current thresholds are accessible for every zone.

8.8.2 OPERATING CHARACTERISTIC SELECTION

In general, we recommend the following characteristics:

- For short line applications: Select Mho for phase fault zones and quadrilateral for earth fault zones.
- For open delta (vee-connected) voltage transformer applications: Set Mho for phase fault distance protection. For Earth Fault protection, disable the Earth Fault Distance elements and use Directional Earth Fault instead.

8.8.2.1 PHASE CHARACTERISTIC

The phase characteristic selection is common to all zones, allowing Mho or quadrilateral selection. Generally, the characteristic chosen matches utility practice. Generally we would recommend a Mho characteristic for line protection and a quadrilateral characteristic for cable applications.

The following figure shows the basic settings needed to configure a forward-looking quadrilateral zone (blinder not shown).

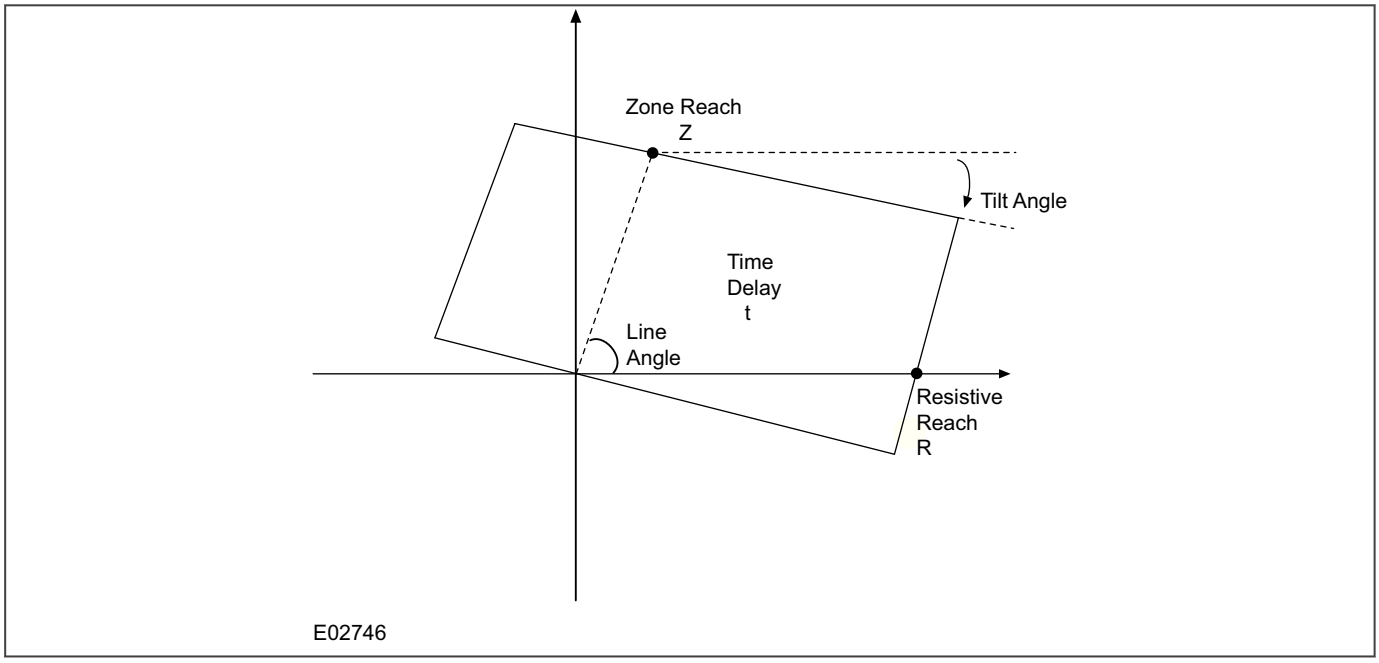


Figure 114: Settings required to apply a quadrilateral zone

The following figure shows the basic settings needed to configure a forward-looking mho zone, assuming that the load blinder is enabled.

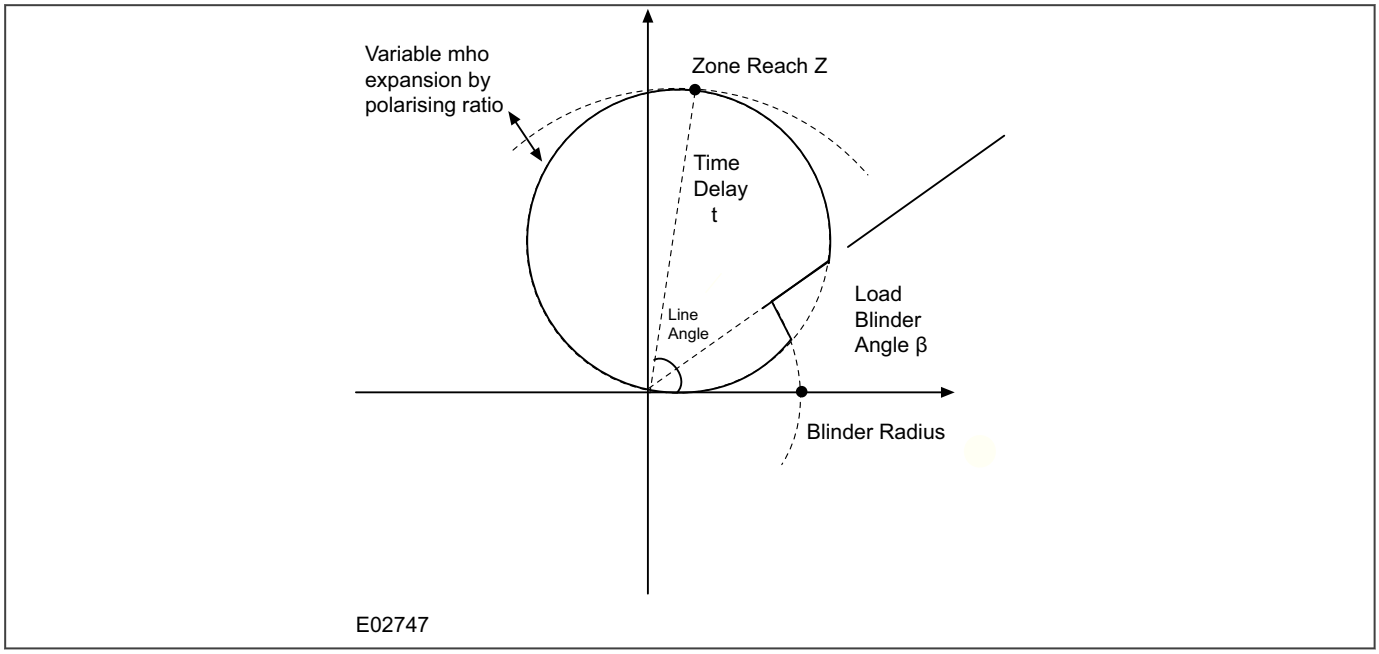


Figure 115: Settings required to apply a Mho zone

8.8.2.2 EARTH FAULT CHARACTERISTIC

The earth fault characteristic selection is common to all zones, allowing Mho or quadrilateral selection. Generally, the characteristic chosen matches utility practice. Generally we would recommend a Mho characteristic for line protection and a quadrilateral characteristic for cable applications.

Quadrilateral earth-fault characteristics are also recommended for all lines shorter than 10miles (16km). This ensures that the resistive fault arc coverage does not depend on Mho circle dynamic expansion and is a known set value.

8.8.3 ZONE REACH SETTING GUIDELINES

The Zone 1 elements of a Distance protection should be set to cover as much of the protected line as possible, allowing instantaneous tripping for as many faults as possible. In most applications the Zone 1 reach (Z1) should not be able to respond to faults beyond the protected line. For an underreaching application the Zone 1 reach must therefore be set to account for any possible overreaching errors. These errors come from measuring errors, the current and voltage transformers, and inaccurate line impedance data. We therefore recommend that the reach of the Zone 1 distance elements is restricted to 80% of the protected line impedance (positive phase sequence line impedance), with Zone 2 elements set to cover the final 20% of the line.

The Zone 2 elements should be set to cover the 20% of the line not covered by Zone 1. Allowing for underreaching errors, the Zone 2 reach (Z2) should be set in excess of 120% of the protected line impedance for all fault conditions. Where aided tripping schemes are used, fast operation of the Zone 2 elements is required. It is therefore beneficial to set Zone 2 to reach as far as possible, such that faults on the protected line are well within reach. A constraining requirement is that, where possible, Zone 2 does not reach beyond the Zone 1 reach of adjacent line protection. For this reason the Zone 2 reach should be set to cover up to 50% of the shortest adjacent line impedance, if possible.

The Zone 3 elements would usually be used to provide overall back-up protection for adjacent circuits. The Zone 3 reach (Z3) is therefore set to approximately 120% of the combined impedance of the protected line plus the longest adjacent line. A higher apparent impedance of the adjacent line may need to be allowed where fault current can be fed from multiple sources or flow through parallel paths.

Zone 3 may also be programmed with a slight reverse (“rev”) offset, in which case its reach in the reverse direction is set as a percentage of the protected line impedance too. This would typically provide back-up protection for the local busbar, where the offset reach is set to 20% for short lines (<30km) or 10% for longer lines.

Zone 3 may also be set as a reverse directional zone. The setting chosen for Zone 3, if used, depends on its application. Typical applications include its use as an additional time delayed zone or as a reverse back-up protection zone for busbars and transformers.

Programmable zone elements can be set with the same options as Zone 3 (Forward, Reverse or Offset). A programmable zone can be used as an additional forward protection zone if custom and practice requires using more than three forward zones of Distance protection.

The Zone 4 elements may also provide back-up protection for the local busbar. Where Zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, Zone 4 must reach further behind the protection than Zone 2 for the remote end protection. In such cases the reverse reach should be:

- Mho: Z4 > Remote Zone 2 reach x 120%
- Quadrilateral: Z4 > (Remote Zone 2 reach x 120%) minus the protected line impedance

Note:
In the case of the Mho, the line impedance is not subtracted. This ensures that whatever the amount of dynamic expansion of the circle, the reverse looking zone always detects all solid and resistive faults capable of detection by Zone 2 at the remote line end.

8.8.3.1 QUADRILATERAL RESISTIVE REACHES

Two setting modes are possible for resistive reach coverage, which can be set by the ***Quad Resistance*** Setting:

`Common`: In this mode, all zones share one common fault resistive reach setting

`Proportional`: With this mode, the ratio of zone reach to resistive reach is the same for all zones. The ***Fault Resistance*** setting defines a reference fault at the remote end of the line. The resistive reach is set at the same percentage of the fault resistance as the Zone Reach setting. For example, if the Zone 1 reach is 80% of the protected line, its resistive reach is 80% of the reference fault resistance.

The `Proportional` setting is used to avoid zones being excessively broad (width of the resistive reach compared to the length of the impedance reach). In general, for easiest injection testing, the aspect ratio of any zone is best within the 1 to 15 range:

$$1/15\text{th} <= \text{Z reach} / \text{R reach setting} <= 15$$

The resistive reach settings should be selected according to utility practice. If no such guidance exists, a starting point for Zone 1 is:

- Cables: Resistive Reach = 3 x Zone 1 reach
- Overhead lines: Resistive Reach = [2.3 - 0.0045 x Line length (km)] x Zone 1 reach
- Lines longer than 400km: 0.5 x Zone 1 reach

Note:
Because the fault current for an earth fault may be limited by tower footing resistance, high soil resistivity, and weak infeeding; any arcing resistance is often higher than for a corresponding phase fault at the same location. It may be necessary to set the Rn Gnd Resistive settings to be higher than the Rn Ph Resistive setting. A setting of Rn Gnd Resistive three times that of Rn Ph Resistive is not uncommon.

8.8.4 EARTH FAULT RESISTIVE REACHES AND TILTING

The protection allows two different methods of tilting the Impedance Reach line.

- Automatic adjustment of the top reactance line angle (dynamic tilting)
- Fixed setting of the top line that overrides dynamic tilting (fixed tilting)

8.8.4.1 DYNAMIC TILTING

The dynamic tilting requirements are different for long lines and short lines:

Long lines

In the case of medium and long line applications where quadrilateral distance earth-fault characteristics are used, ***Zn Dynamic Tilt*** should be enabled and the starting tilt angle should be -3° (as per the default settings). This tilt compensates for possible current and voltage transformer and line data errors.

For high resistive faults during power exporting, the underreaching Zone 1 is only allowed to tilt down by the angle difference between the faulted phase and negative sequence current ∠(Iph-I2) starting from the –3° set angle. This ensures stability of Zone 1 for high resistance faults beyond the Zone 1 reach even during heavy load conditions (high load angle between two voltage sources) and sufficient sensitivity for high resistance internal faults. The tilt angle for all other zones (that are by nature overreaching zones) remain at -3°.

In the case of power importing, Zone 1 remains at –3° while all other zones are allowed to tilt up by the ∠(Iph-I2) angle difference, starting from –3°. This increases the Zone 2 and Zone 4 resistive reaches and secures correct operation in permissive overreach and blocking type schemes.

Short lines

For very short lines, typically below 10Miles (16km), the ratio of resistive to reactance reach setting (R/X) could easily exceed 10. For such applications the geometrical shape of the quadrilateral characteristic could be such that the top reactance line is close or even crosses the resistive axis as presented in the following figure:

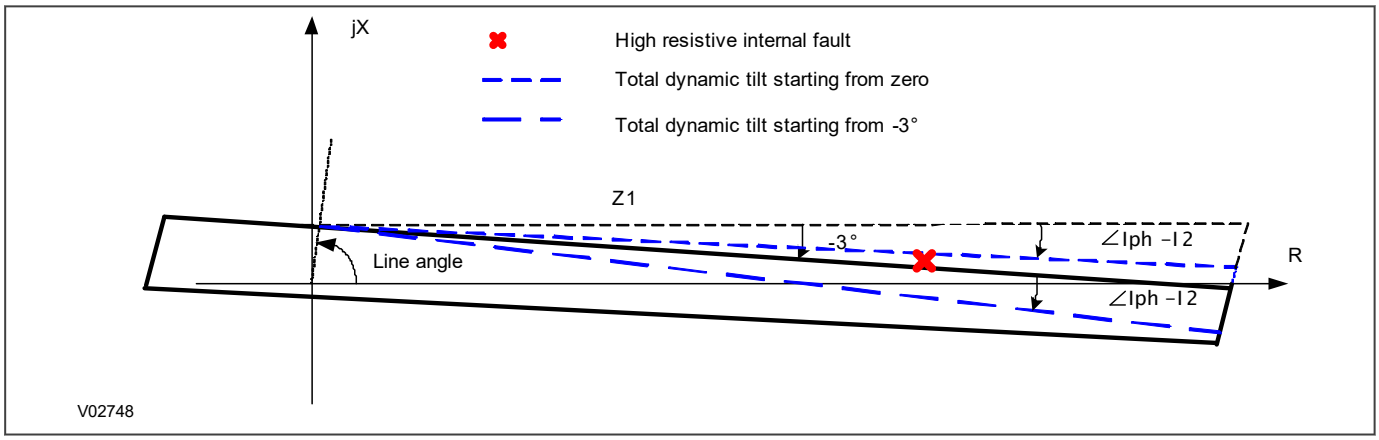


Figure 116: Over-tilting effect

In the case of high resistance external faults on a short line, particularly under heavy power exporting conditions, Zone 1 remains stable due to dynamic downwards tilting of the impedance reach line. However, the detection of high resistance internal faults especially towards the end of the line needs consideration. In such applications you can choose to detect high resistance faults using highly sensitive Aided Directional Earth Fault scheme, or to clear the fault with Distance ground protection. For the Distance to operate, it is necessary to eliminate over-tilting for internal faults by reducing the initial -3° tilting angle to zero so that the overall impedance reach line tilt is equal to ∠(Iph-I2) angle only.

As shown in the previous figure, the internal resistive fault then falls in the Zone 1 operating characteristic. However, for short lines the load angle is relatively low when compared to long transmission lines for the same transfer capacity and therefore the impedance reach line dynamic tilting may be moderate. Therefore it may be necessary to reduce the Zone 1 reach to guarantee Zone 1 stability. This is particularly recommended if the distance protection is operating in an aided scheme. To summarise, for very short lines with large R/X setting ratios, we recommend settiing the initial tilt angle to zero and the Zone 1 reach to 70-75% of the line impedance.

The above discussion assumes homogenous networks where the angle of the negative sequence current derived at relaying point is very close to the total fault current angle. If the network is non-homogenous, there is a difference in

angle that causes inaccurate dynamic tilting. Therefore in such networks either quadrilateral with fixed tilt angle or mho characteristic should be considered to avoid Zone 1 overreach.

Note:
You can also use Delta Directional schemes to detect high resistance faults.

8.8.4.2 FIXED TILTING

As an alternative to dynamic tilting, you can set a fixed tilt angle. This is used for applications where the power flow direction is unidirectional.

Exporting End

To secure stability, the tilt angle of Zone 1 at the exporting end has to be set negative and above the maximum angle difference between sources feeding the resistive faults. This data should be known from load flow study, but if unavailable, the minimum recommended setting would be the angle difference between voltage and current measured at local end during the heaviest load condition coupled with reduced Zone 1 reach of 70-75% of the line impedance.

Note:
With a sharp fixed tilt angle, the effective resistive coverage would be significantly reduced. Therefore for short lines, dynamic tilting (with variable tilt angle depending on fault resistance and location) is preferred. For all other overreaching zones, set the tilting angle to zero.

Importing End

Set zone 1 tilt angle to zero and for all other zones the typical setting should be positive and between +5° and +10°.

Note:
The setting accuracy for overreaching zones is not crucial because it does not pose a risk for distance maloperation. The purpose is to boost Zone 2 and Zone 4 reach and improve the performance of Aided Schemes.

8.8.5 PHASE FAULT ZONE SETTINGS

If you use the `Advanced` ***Setting Mode***, in addition to the reach and compensation settings, you have additional settings to enter.

Each zone has a minimum current sensitivity setting (***Zn Sensit. Iph>***) which sets the minimum current that must be flowing in each of the faulted phases before a trip can occur. It is recommended to leave these settings at their default. An exception is where the protection is made less sensitive to match with other protection existing on the power system, or to grade with the pickup setting of any ground overcurrent protection for tee-off circuits.

When quadrilateral characteristics are used, the tilt angles of the impedance reach lines can be set.

By factory default, the impedance reach lines of the quadrilateral characteristics are not fixed as horizontal reactance lines. To account for phase angle tolerances in the line transformers, etc., the lines are tilted downwards at a droop of -3°. This tilt down helps to prevent Zone 1 overreach.

The fixed tilt setting on the phase elements may also be used to compensate for overreach effects when pre-fault heavy load export is flowing. In such cases, fault arc resistance is phase shifted on the impedance polar plot, tilting down towards the resistive axis and not appearing to be fully resistive in nature. For long lines with heavy power flow, the zone 1 top line might be tilted downwards in the range –5° to –15°, mimicking the phase shift of the resistance.

Note:
A negative angle is used to set a downwards tilt gradient, and a positive angle to tilt upwards.

Note:
Mho characteristics have an inherent tendency to avoid unwanted overreaching, making them very desirable for long line protection.

8.8.6 DIRECTIONAL ELEMENT FOR DISTANCE PROTECTION

Distance zones are directionalised by the Delta decision. For Delta directional decisions, the relay characteristic angle (RCA) settings must be based on the average source + line impedance angle for a fault anywhere internal or external to the line. Typically, the ***Dir Char Angle*** is set to 60°, as it is not essential for this setting to be precise. When a fault occurs, the delta current is never close to the characteristic boundary, so an approximate setting is good enough.

The 60° angle is associated with mainly inductive sources and suits most applications. However, in series compensated line applications where the capacitor is physically located behind the line voltage transformer, the Delta directional characteristic angle needs adjusting. In such applications the capacitor is included in the equivalent source impedance. Then the overall source impedance seen by the protection becomes predominantly capacitive if the inductance of the normally strong source is less than the capacitor value. In this case, the calculated operating angle during an internal fault may not fall within the default 60° Delta directional line operating boundary. This could lead to an incorrect (reverse) directional decision. A zero degree shift is most suitable for such a fault. However, the constraining factor is the case of external faults for which the source is always inductive regardless of the degree of compensation and for which the 60° shift is most appropriate. To ensure correct, reliable and fast operation for both fault locations in the case of predominantly capacitive source, we recommend a ***Dir Char Angle*** setting of 30°.

If ***Dir. Status*** in *DELTADIRECTIONAL* is set to `Disabled`, we recommend a setting of `1` (100%). With this setting, a mix of self-polarisation and memory-polarisation adequate for most applications is applied.

8.8.7 DELTA DIRECTIONAL ELEMENT SETTING GUIDELINES

For the Delta directional element, the relay characteristic angle (RCA) settings must be based on the average source + line impedance angle for a fault anywhere internal or external to the line. Typically, the ***Dir Char Angle*** is set to 60°, as it is not essential for this setting to be precise. When a fault occurs, the delta current will never be close to the characteristic boundary, so an approximate setting can be applied.

8.8.7.1 DELTA THRESHOLDS

For best performance, set the ***Dir. I Fwd*** current threshold at 10 to 20% In. This ensures detection of all fault types if the fault current contribution to an earth fault at the remote end of the line generates at least this amount of delta. To select the correct Delta V Forward setting, refer to the following table which compares SIR (Source to Line impedance ratio) with recommended Delta V Forward setting (ΔV Fwd).

Lowest SIR Ratio of the System	Recommended ΔV Fwd (as a % of Vn)
>= 0.3	4%
>= 0.5	6%
>= 1	9%
>= 2	13%
>= 3	15%
>= 5	17%
>= 10	19%

Lowest SIR Ratio of the System	Recommended ΔV Fwd (as a % of Vn)
25 - 60	21%

The reverse fault detectors must be set more sensitively, as they are used to invoke the blocking and current reversal guard elements. We suggest that all reverse detectors are set at 66 to 80% of the setting of the forward detector, typically:

- ***Dir. V Rev*** = ***Dir. V Fwd*** x 0.66
- ***Dir. I Rev*** = ***Dir. I Fwd*** x 0.66

Due to the implementation method, Deltas are present only for 2 cycles on fault inception. If any distance elements are enabled, these will automatically allow the delta forward or reverse decisions to seal-in, until such time as the fault is cleared from the system. Therefore as a minimum, some distance zone(s) must be enabled in the DISTANCE SETUP column as fault detectors. It does not matter what time delay is applied for the zone(s). This can either be the typical distance delay for that zone or set to 'Disabled' in the SCHEME LOGIC column, if no distance tripping is required. As a minimum, Zone 3 must be enabled, with a reverse reach such as to allow seal-in of Dir. Rev, and a forward reach to allow seal-in of Dir. Fwd.

The applicable reaches would be:

- Zone 3 Forward: Set at least as long as a conventional Zone 2 (120-150% of the protected line)
- Zone 3 Reverse: Set at least as long as a conventional Zone 4, or supplement by assigning Zone 4 if a large reverse reach is not preferred for Zone 3.

We generally advise a Mho characteristic in such starter applications, although quadrilaterals are acceptable. As the Mho starter is likely to have a large radius, we strongly advise applying the Load Blinder.

8.8.8 FILTERING SETUP

A number of filters and features are provided to help avoid false tripping during conditions that can be challenging to distance protection.

8.8.8.1 DISTANCE DIGITAL FILTER

In most applications, we recommend setting the ***Digital Filter*** setting to `Standard`. This ensures that the protection provides fast, sub-cycle tripping. In certain rare cases, such as where lines are immediately adjacent to High Voltage DC (HVDC) transmission, the current and voltage inputs may be severely distorted under fault conditions. The resulting non-fundamental harmonics could affect the reach point accuracy of the protection. To prevent the protection being affected, you should select the `Special Applics` setting to enable the special applications filter.

> *Note:*
> *When using the Special Applications filter the instantaneous operating time is increased by about a quarter of a power frequency cycle.*

8.8.8.2 SETTING UP CVTS

CVTs with passive suppression of ferroresonance

Set ***CVT Filters*** to `Passive` for any type 2 CVT (those with an anti-resonance design). You need to apply an SIR cut-off setting, above which the protection operation is deliberately slowed by a quarter of a cycle. A typical SIR setting is 30, below which the protection trips sub-cycle, and if the infeed is weak the CVT filter adapts to slow the protection and prevent transient overreach.

CVTs with active suppression of ferroresonance

Set ***CVT Filters*** to `Active` for any type 1 CVT.

8.8.9 LOAD BLINDING SETUP

We strongly recommend enabling the load blinder, especially for lines above 150km (90miles) and for any networks where power swings might be experienced. This will prevent non-harmonic low-frequency transients causing load encroachment problems.

The impedance radius must be set lower than the worst-case loading, and this is often taken as 120% overloading in one line, multiplied by two to account for increased loading during outages or fault clearance in an adjacent parallel circuit. Then an additional allowance for measuring tolerances results in a recommended setting typically between a quarter and one third of the rated full load current:

$$Z <= (\text{Rated phase voltage } Vn)/(I_{FLC} \times 3)$$

When the load is at the worst-case power factor, it should remain below the beta (β) setting. So, if we assume a typical worst case 0.85 power factor, then:

$$\beta >= \text{Cos}^{-1}(0.85) + 15° \text{ margin} >= 47°$$

and to ensure that line faults are detected:

$$\beta <= (\text{Line Angle} - 15°).$$

In practice, an angle half way between the worst-case leading load angle, and the protected line impedance angle, is often used.

This product has a facility to allow the load blinder to be bypassed any time that the measured voltage for the phase in question falls below an undervoltage (***Load Blinder V<***) setting. Under such circumstances, the low voltage would not be explained by normal voltage excursion tolerances on-load. A fault must be present on the phase in question, and it is acceptable to override the blinder action and allow the distance zones to trip according to the entire zone shape. The benefit is that the resistive coverage for faults near to the protection location can be higher.

The undervoltage setting must be lower than the lowest phase-neutral voltage under heavy load flow and depressed system voltage conditions. The recommended ***Load Blinder V<*** setting is 70% Vn.

8.8.10 POLARISING SETUP

You can choose how much memory polarisation to mix with self-polarisation using the ***Dist. Polarizing*** setting. Some recommendations are:

Cable applications

Use 20% (0.2) memory. This results in minimum Mho expansion and keeps the protected line section well within the expanded Mho, thereby ensuring better accuracies and faster operating times for close-up faults. This matches the guidance previously provided for LFZP123 or LFZR applications for cable feeders

Series compensated lines

Use the maximum memory polarisation (setting = 5). The large memory content ensures correct operation even with the negative reactance effects of the compensation capacitors seen either within the zones, or within the line impedance.

Short lines

For lines shorter than 10miles (16km), or with an SIR higher than 15, use the maximum memory polarisation (setting = 5). This ensures sufficient characteristic expansion to cover fault arc resistance.

General line applications

Use any setting between 0.2 and 1.

8.8.11 DISTANCE PROTECTION WORKED EXAMPLE

This section presents a worked example of how to set the Distance protection. For this case study, we assume that Zone 1 Extension is not used, and that only three zones are required for basic Distance protection (Zones 1 and 2 Forward Directional, and Zone 3 Forward Offset). The following settings are derived:

- Line Impedance
- Residual Compensation
- Zone 1 reach settings for phase-faults and earth-faults
- Zone 2 reach settings for phase-faults and earth-faults
- Zone 3 reach settings for phase-faults and earth-faults
- Zone 3 reverse reach settings
- Zone 4 reach settings (for use with Permissive Overreach or Blocking schemes if needed)
- Load avoidance

The settings are applicable whether the Distance protection characteristics are set to Mho, or Quadrilateral. If you choose Quadrilateral however, you will need to consider the Resistive reaches of Quadrilaterals.

For this study, we wish to protect one line of a double 230kV, 100km line between a substation at Green Valley and a substation at Blue river. There are generating sources at Tiger Bay, 80 km from Green Valley and at Rocky Bay, 60 km from Blue River.

The single-line diagram for the system is shown in the following figure:

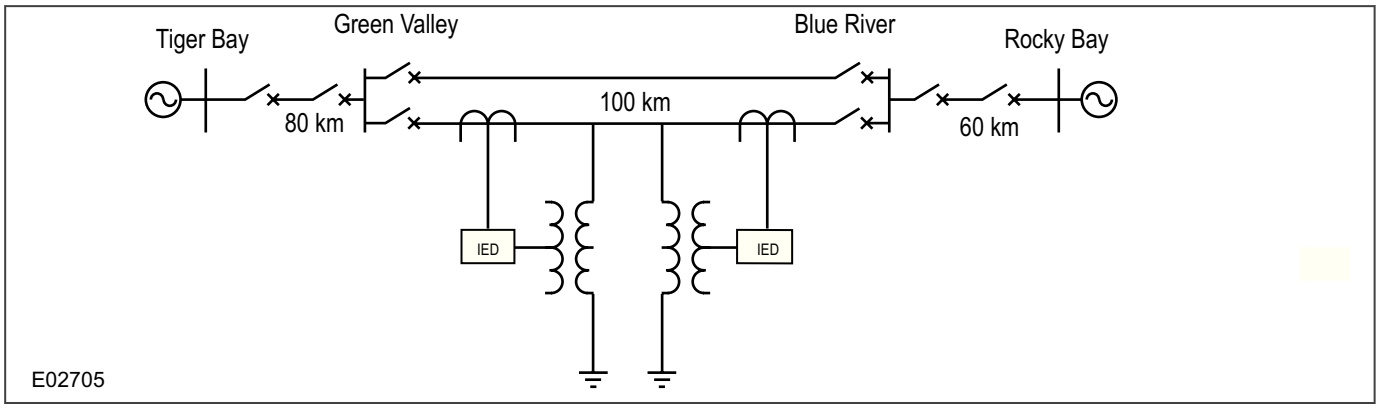


Figure 117: Example power system

The system data is as follows:

- System Voltage: 230kV
- System earthing: Solid
- CT ratio: 1200 : 5
- VT ratio: 230 000 : 115
- Line length: 100km
- Positive sequence line impedance (Z1): 0.089 + j0.476 ohms/km = 0.484∠79.4°
- Zero sequence line impedance (Z0): 0.426 + j1.576 ohms/km = 1.632∠74.8°
- Z0/Z1: 3.372∠–4.6°
- Green Valley substation fault level: 2000 MVA to 5000 MVA
- Blue river substation fault level: 1000 MVA to 3000 MVA
- Circuit continuous rating: 400 MVA
- Worst case power factor of load: 0.85

8.8.11.1 LINE IMPEDANCE CALCULATION

Ratio of secondary to primary impedance = (1200/5)/(230000/115) = 0.12

Total primary line impedance (for 100 km length) = 100 x 0.484∠79.4° Ω

Total secondary impedance = (0.12 x 100 x 0.484)∠79.4° = 5.81∠79.4° Ω

Therefore set secondary values as follows:

Line Angle = 80°

Line Impedance = 5.81 Ω

8.8.11.2 RESIDUAL COMPENSATION FOR EARTH FAULT ELEMENTS

The residual compensation factor can be applied independently to certain zones if required. This is a useful feature where line impedance characteristics change between sections or where hybrid circuits are used. In this example this is not the case, so a common kZN factor can be applied to each zone. This is set as ratio ***kZN Res Comp***, and angle ***KZN Res Angle***:

We know that

$$k_{ZN} = (Z_0 - Z_1)/3Z_1$$

Now, performing the calculations iwht the given values ...

$$|Z_0 - Z_1| = 1.15$$

$$|3Z_1| = 1.452$$

$$\angle(Z_0-Z_1) = 72.9°$$

$$\angle 3Z_1 = 79.4°$$

Thus ...

$$kZ_N = 0.79 \angle -6.5°$$

Therefore set:

kZN Res Comp = 0.79

KZN Res Angle = -6.5°

8.8.11.3 ZONE 1 PHASE AND GROUND REACH SETTINGS

For the protection at Green Valley:

The required Zone 1 reach is to be 80% of the line impedance between Green Valley and Blue River substations.

Using the ***Setting Mode*** `Simple`:

- Set ***Zone 1 Ph Status*** and ***Zone 1 Gnd Stat.*** to `Enabled`
- Set ***Zone 1 Ph Reach*** and ***Zone 1 Gnd Reach*** to 80%

From this the protection algorithm automatically calculates the required Ohmic reaches.

Alternatively, using the ***Setting Mode*** `Advanced`, the values can be calculated and entered manually as follows:

Required Zone 1 reach = 0.8 x 100 x 0.484∠79.4° x 0.12 = 4.64∠79.4° Ω secondary

So:

- Set ***Z1 Ph. Reach*** and ***Z1 Gnd. Reach*** = 4.64 Ω
- Set ***Z1 Ph. Angle*** and ***Z1 Gnd. Angle*** = 80°

8.8.11.4 ZONE 2 PHASE AND GROUND REACH SETTINGS

For the protection at Green Valley:

In *Advanced* mode:

Required Zone 2 impedance = line impedance of Green Valley to Blue River + 50% line impedance from Blue River to Rocky Bay

= (100+30) x 0.484∠79.4° x 0.12

= 7.56 ∠79.4° Ω secondary

So:

- Set ***Z2 Ph. Reach*** and ***Z2 Gnd. Reach*** = 7.56 Ω
- Set ***Z2 Ph. Angle*** and ***Z2 Gnd. Angle*** = 80°

Alternatively, in *Simple* setting mode, this reach can be set as a percentage of the protected line. Typically a figure of at least 120% of the line between Green Valley and Blue River is used.

8.8.11.5 ZONE 3 PHASE AND GROUND REACH SETTINGS

For the protection at Green Valley:

In *Advanced* mode:

Required Zone 3 impedance = 1.2(line impedance of Green Valley to Blue River) + line impedance from Blue River to Rocky Bay

= 1.2*(100+60) x 0.484∠79.4° x 0.12

= 11.15 ∠79.4° Ω secondary

So:

- Set ***Z3 Ph. Reach*** and ***Z2 Gnd. Reach*** = 11.15 Ω
- Set ***Z2 Ph. Angle*** and ***Z2 Gnd. Angle*** = 80°

Alternatively, in *Simple* setting mode, this reach can be set as a percentage of the protected line.

8.8.11.6 ZONE 3 REVERSE REACH SETTINGS

For the protection at Green Valley:

In the absence of special requirements, because the protected line length is more than 30km, Zone 3 can be given a small reverse reach – say 10%.

Using *Advanced* mode, in the *DISTANCE SETUP* column, set:

- ***Z3' Ph Rev Reach*** and ***Z3' Gnd Rev Rch*** = 0.1*5.81 = 0.58 Ω

8.8.11.7 ZONE 4 REVERSE REACH SETTINGS

For the protection at Green Valley:

Where Zone 4 is used to provide reverse directional decisions for Blocking or Permissive Overreach schemes, Zone 4 must reach further behind the local protection than Zone 2 of the remote protection. This can be achieved by setting Zone 4 ≥ 1.2 x Remote Zone 2 reach, where mho characteristics are used.

Remote Zone 2 Reach = line impedance of Green Valley to Blue River + 50% line impedance from Green valley to Tiger Bay

= (100 + 40) x 0.484∠79.4° x 0.12

$= 8.13\angle 79.4° \ \Omega$ secondary

Zone 4 Reach $\geq (8.13\angle 79.4° \times 120\%) - 5.81\angle 79.4°$

$= 3.95\angle 79.4° \ \Omega$ secondary

This is the minimum Zone 4 Reach setting, so:

- ***Set Z4 Ph. Reach*** and ***Z4 Gnd. Reach*** = 3.96 Ω
- ***Set Z4 Ph. Angle*** and ***Z4 Gnd. Angle*** = 80°

8.8.11.8 LOAD AVOIDANCE

The maximum full load current of the line can be determined from the calculation:

$$I_{FLC} = [(\text{Rated MVAFLC}) / (\sqrt{3} \times \text{Line kV})]$$

The settings must allow for a level of overloading, typically a maximum current of 120% I_{FLC} prevailing on the system transmission lines. Also, for a double circuit line, during the auto-reclose dead time of fault clearance on the adjacent circuit, twice this level of current may flow on the healthy line for a short period of time. Therefore the circuit current loading could be 2.4 x I_{FLC}.

With such a heavy load flow, the system voltage may be depressed, typically with phase voltages down to 90% of Vn nominal.

Allowing for a tolerance in the measuring circuit inputs (line CT error, VT error, protection accuracy, and safety margin), this results in a load impedance which might be 3 times the expected rating.

To avoid the load, the blinder impedance needs to be set:

$$Z \leq (\text{Rated phase-ground voltage Vn}) / (I_{FLC} \times 3)$$

$$= (115/\sqrt{3}) / (I_{FLC} \times 3)$$

Set the V< Blinder voltage threshold at the recommended 70% of Vn = 66.4 x 0.7 = 45 V.

8.8.11.9 QUADRILATERAL RESISTIVE REACH SETTINGS

If applying Quadrilateral characteristics, as well as the Impedance Reaches, the Resistive Reaches also need to be considered. The Resistive reaches of the phase-fault elements must be set to cover the maximum expected phase-to-phase fault resistance. The Resistive reaches of the earth-fault elements should take into account the arc-resistance and the tower footing resistance.

Phase-fault elements

Ideally, the Resistive reach should be set greater than the maximum fault arc resistance for a phase-phase fault (Ra), calculated in terms of the minimum expected phase-phase fault current, the maximum phase conductor separation, according to the formula developed by (van) Warrington as:

$$Ra = (28710 \times L)/If \times 1.4$$

where:

- If = Minimum expected phase-phase fault current (A)
- L = Maximum phase conductor separation (m)

Typical figures for Ra are given, for different values of minimum expected phase fault currents, in the following table:

Conductor Spacing (m)	Typical System Voltage (KV)	RA for IF = 1 KA	RA for IF = 2 KA	Ra for If = 3 kA
4	110 - 132	7.2 Ω (primary)	2.8 Ω (primary)	1.6 Ω (primary)
8	220 - 275	14.5 Ω (primary)	5.5 Ω (primary)	3.1 Ω (primary)

Conductor Spacing (m)	Typical System Voltage (KV)	RA for IF = 1 KA	RA for IF = 2 KA	Ra for If = 3 kA
11	380 - 400	19.9 Ω (primary)	7.6 Ω (primary)	4.3 Ω (primary)

Note:
For circuits with infeed from more than one terminal, the fault resistance will appear greater. This is because the protection cannot measure the current contribution from a remote terminal. The apparent fault resistance increase could be between 2 to 8 times the calculated resistance. For this reason, we recommended setting the zone Resistive reaches to 4 times the calculated arc resistance.

In this example, the minimum phase fault level is 1000 MVA. This is equivalent to an effective short-circuit fault feeding impedance of:

$$Z = kV^2/MVA = 230^2/1000 = 53\ \Omega \text{ (primary)}$$

The lowest phase fault current level is equivalent to:

$$Ifault = (MVA \times 1000)/(\sqrt{3} \times kV)$$

$$= (1000 \times 1000)/(\sqrt{3} \times 230)$$

$$= 2.5\ kA$$

Giving, according to the (van) Warrington formula, an arc resistance of:

$$Ra = 4\ \Omega$$

Iterative calculations could be performed to refine the expected fault current (which decreases as refined values of Ra are included in the calculation), but as Ra is relatively small compared to the initially calculated value of Z, this value is acceptable.

To compensate for remote infeed a small additional factor can be added to account for the expected fault current being lower than that used in the calculation. So rather than set the zone Resistive reaches to 4 times the calculated arc resistance, a factor of 5 could be used.

Using a factor of 5 gives a minimum setting of:

$$\text{Phase Resistive Reach} = 5 \times Ra = 20\ \Omega \text{ (primary value)}$$

The Phase Resistive Reach could be set higher than this (for example using the rule-of-thumb: [2.3 - 0.0045 x Line length (km)] x Zone 1 reach), so typically it would be set higher than 20Ω but lower than the Load Avoidance setting.

Earth-fault elements

Fault resistance would comprise arc-resistance and tower footing resistance. A typical resistive reach coverage setting would be 40 Ω (primary).

For high resistance earth faults, the situation could arise where no distance elements would operate. In such cases, supplementary earth fault protection (for example Aided DEF protection) should be applied. If supplementary earth fault protection is used, large resistive reaches for Earth-Fault Distance protection do not need to be used so that the Earth-Fault Resistive reach can be set according to the utility practice. In the absence of specific guidance, a recommendation for setting Zone 1 is:

- Cables: Resistive Reach = 3 x Zone 1 reach
- Overhead lines: Choose Resistive Reach in the range [2.3 - 0.0045] x Line length(km) x Zone 1 Reach
- Lines longer than 400 km: Choose Resistive Reach = 0.5 x Zone 1 Reach

8.8.12 TEED FEEDER APPLICATIONS

Distance protection can be applied to protect three terminal lines (teed feeders). Interconnecting three terminals, however, affects the apparent impedances seen by the distance elements and creates certain problems.

Consider, as an example, the following figure which represents a teed feeder with terminals A, B, and C, with a fault applied near to terminal B:

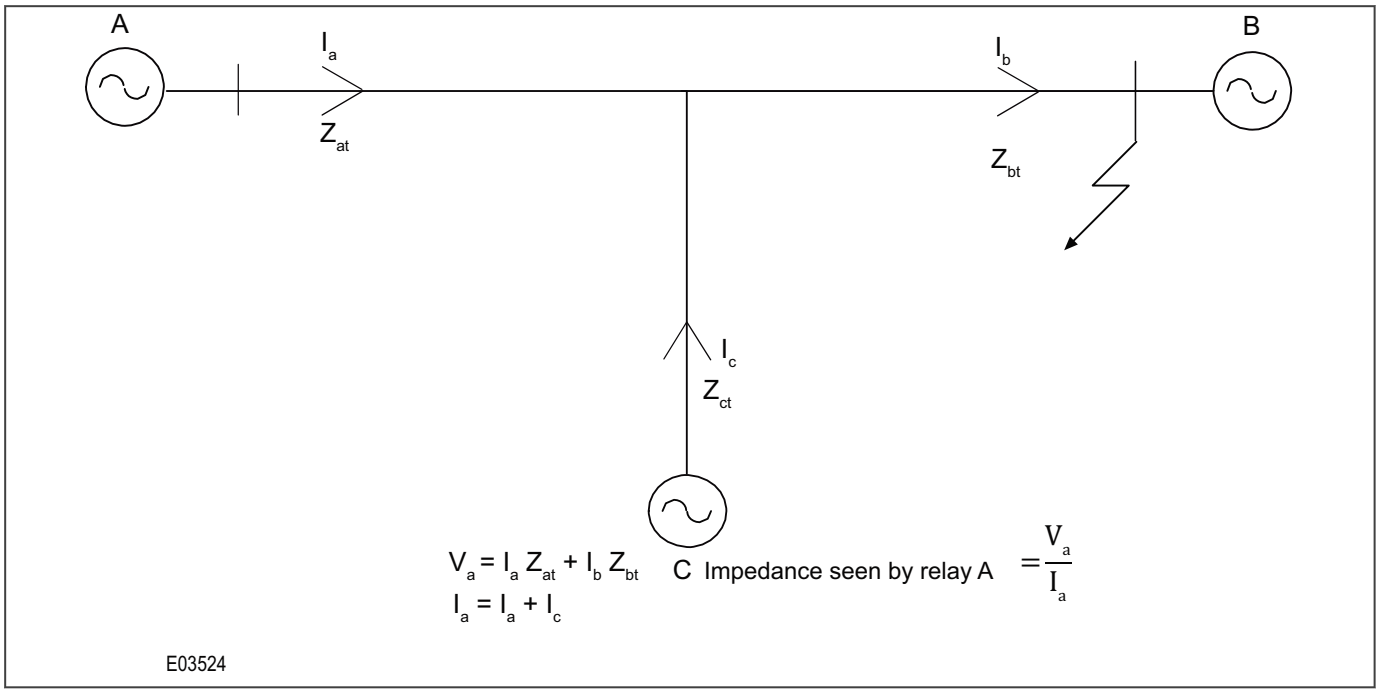


Figure 118: Apparent impedances seen by distance protection on a teed feeder

The impedance seen by the distance elements at terminal A is given by:

$$Za = Zat + Zbt + [Zbt.(Ic/Ia)]$$

For faults beyond the Tee point, with infeed from terminals A and C, the distance elements at A (and C) will underreach. If terminal C is a relatively strong source, the underreaching effect at A can be substantial. If Zone 2 was set to a typical value of 120% of line AB, the element may fail to operate for internal faults. To compensate, the Zone 2 element must be set to further overreach by a factor which takes into account the effect of the infeed from the tee-point.

So, if infeed is present on a teed circuit, all Zone 2 elements should be set to overreach both of their remote terminals by a factor which takes into account the effect of the infeed from the tee-point.

Like overreaching of Zone 2 elements, underreaching of Zone 1 elements must also be assured. Zone 1 elements at each terminal must be set to underreach the true impedance to their nearest terminal (limiting case = no infeed to the tee-point - hence no overreach contribution).

Changing the reach requirements to match the infeed expectations is possible using the alternative setting group feature. Tailoring setting group contents to the different conditions, coupled with appropriate setting group switching, enables the changing reach requirements to be met.

Carrier aided schemes can also be used in conjunction with distance elements to protect teed feeders. Although Permissive Overreaching and Permissive Underreaching schemes may be used, they suffer some limitations. Blocking schemes are generally considered to be the most suitable.

For a full explanation of Teed Feeders applications in carrier aided schemes, please refer to the Carrier Aided Schemes chapter.

CHAPTER 9

CARRIER AIDED SCHEMES

9.1 CHAPTER OVERVIEW

This chapter contains the following sections:

Chapter Overview 226
Introduction 227
Aided Distance Scheme Logic 228
Aided DEF Scheme Logic 253
Aided Delta Scheme Logic 268
DE Teleprotection Schemes 279
Application Notes 281

9.2 INTRODUCTION

The provision of communication channels between the terminals of a protected transmission line or distribution feeder enables unit protection to be applied.

Protection devices located at different terminals can be configured to communicate with one another in order to implement unit protection schemes. The exchange of simple ON/OFF command signals allows unit protection to be achieved with Distance Protection schemes (Aided Distance), Directional Earth Fault schemes (Aided DEF) and if applicable, Delta Directional Comparison Protection schemes (Aided Delta). Schemes where a communication channel is used to send command signals between line ends are known as Carrier Aided Schemes.

The terms ‘simplex’ and ‘duplex’ are used to describe the type of communication channel used. Simplex communication, also sometimes referred to as half-duplex, requires only a single communication channel between line ends. Signals can be sent in both directions but not at the same time. Duplex communication requires two communication channels between line ends (one in each direction). Duplex communication allows signals to be sent and received at the same time.

9.3 AIDED DISTANCE SCHEME LOGIC

When the Carrier Aided schemes are used in conjunction with the Distance protection, you can choose whether to use them with the phase distance elements only, the earth-fault (ground) distance elements only, or for both phase and earth fault elements.

9.3.1 CARRIER AIDED SCHEMES IMPLEMENTATION

With Aided Distance protection, tripping schemes are used to connect similar devices at different terminals on the protected line to provide fast clearance for faults anywhere along the line.

For distance protection It is typical to set Zone 1 distance protection elements to cover only 80% of a line from the relaying point. Faults on the other 20% of the line would generally be cleared by a delayed Zone 2 element, which could be hundreds of milliseconds after the fault inception. There is, however, a limit to the amount of arc resistance and tower footing resistance that can be adequately covered by distance IEDs, since the coverage is limited by their ohmic reach. If extremely high values of ground fault resistance are expected, then an optional directional comparison earth fault scheme (Aided DEF) can be used to complement the distance schemes.

Aided distance schemes assure fast clearance for faults on the entire circuit by communicating command signals.

For the the communication between local and remote terminals InterMiCOM 64 (IM64) can be used.

9.3.1.1 CARRIER AIDED SCHEME TYPES

This product has two independent Carrier Aided Schemes (Aided Scheme 1 and Aided Scheme 2). The two schemes are independent, but the design of both is the same. Each of the two Carrier Aided Schemes provides the following options:

- Permissive Underreaching Schemes (PUR, PUTT)
- Permissive Overreaching Schemes (POR, POTT)
- Blocking Scheme (Block 1)
- Blocking Scheme (Block 2)
- Unblocking POR Scheme
- Unblocking PUR Schemes
- Programmable
- Programmable Unblocking

Additional Aided 1 Schemes include:

- DE Z1e
- DE Perm. Z1e
- DE Block Z1e

The underreaching options can be used to implement Carrier Aided Distance schemes. The other options can be used with any Carrier Aided scheme application.

The following diagram shows how the schemes can be assigned.

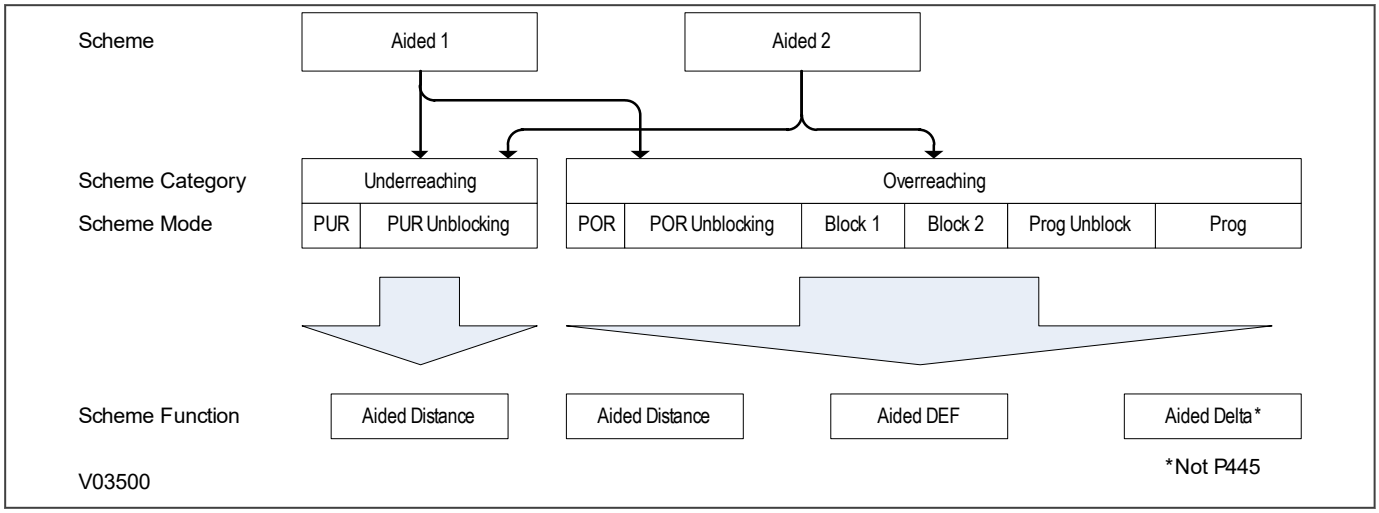


Figure 119: Scheme Assignment

9.3.1.2 DEFAULT CARRIER AIDED SCHEMES

This product provides support for two Carrier Aided schemes, which can operate in parallel. The schemes are referred to as 'Aided Scheme 1' and 'Aided Scheme 2'. The schemes have been designed to operate independently with a separate communication channel dedicated to each one, but they can share a single communication channel if necessary. If both schemes are used and they share a common channel then, if one of the schemes initiates transmission of a command signal, both schemes will receive the command and act upon it.

If you don't want to use the Aided schemes, you should set the relevant ***Aid. 1 Selection*** and ***Aid.2 Selection*** settings (in the *SCHEME LOGIC* column) to `Disabled`. If the setting(s) are enabled, you are provided with a choice of schemes; standard transfer tripping schemes, blocking schemes, or custom programmable schemes.

You select the type of scheme you want to use, and then you choose whether to use it in conjunction with the Distance protection, and/or the Aided DEF protection.

The scheme options are:

- `Disabled`: No scheme is implemented
- `PUR`: Permissive Underreach Transfer Tripping (PUPP, PUR, or PUTT) scheme
- `PUR Unblocking`: Perrmissive Underreach Unblocking scheme
- `POR`: Permissive Overreach Transfer Tripping (POP, POR, or POTT) scheme
- `POR Unblocking`: Permissive Overreach Unblocking scheme
- `Blocking1`: Current reversal guard signal is sent to qualify reverse looking Zone 4 elements
- `Blocking2`: Received current reversal guard signal qualifies reverse looking Zone 4 elements
- `Prog. Unblocking`: Allows you to define which elements are used to assert signals for Overreach Unblocking.
- `Programmable`: Allows you to define which elements are used to assert signals for Overreach Transfer Tripping, by using a custom send mask

Additional Aided 1 Schemes include:

- DE Z1e
- DE Perm. Z1e
- DE Block Z1e

Note:
The PUR schemes are only suitable for Distance protection. Therefore, if a PUR scheme is selected, the option to allocate to other protection is not available.

Note:
For Aided Scheme 1, PUR, POR and blocking schemes can be achieved with 1 channel or 3 channel signalling for Distance protection only. Aided DEF or Aided Delta cannot be done with 3 channel signalling.



Caution:
Zone 1,2 and 4 are required to implement the *PUR*/*POR* and Blocking Aided Schemes. In this case, zone 1 and zone 2 should be forward and zone 4 should be reverse. Therefore, if the relay's *Setting Mode* is set to *Advanced* and any Zone direction has been selected that compromises the Aided Schemes, then the Aided Distance Schemes should be forced to be disabled by the user.

9.3.2 PERMISSIVE UNDERREACH SCHEME

The simplest Carrier Aided scheme mode for use with distance-type applications is the Permissive Under-reach Protection scheme, variously referred to as PUR, PUP, and PUTT. We normally use the term PUR.

To use this scheme, you need to set the relevant setting (***Aid. 1 Selection*** or ***Aid. 2 Selection***) in the *SCHEME LOGIC* column to *PUR*.

The channel for a PUR scheme is keyed (that means that the aiding signal is asserted) if an under-reaching Zone 1 element operates. If the remote device detects a forward fault and this signal is received, then the remote protection operates without further delay. Faults in the last 20% of the protected line are therefore cleared with minimal time delay.

Note:
This assumes a 20% typical end-zone when Zone 1 is set to 80% of the protected line.

The following are some of the main features and requirements for a permissive under-reaching scheme.

- Only a simplex channel is required.
- Scheme security is high, because the signalling channel is only keyed for faults in the protected line.
- If the circuit breaker at the remote terminal is open, faults in the remote 20% of the line are cleared using the Zone 2 time delay of the local protection.
- If there is a weak-infeed, or zero-infeed from the remote terminal, (current below the protection sensitivity), faults in the remote 20% of the line are cleared using the Zone 2 time delay of the local protection.
- If the signalling channel fails, basic distance scheme tripping remains available.

The PUR logic is:

- Send logic: Assert signal if Zone 1 element operates
- Permissive trip logic: Trip if the Zone 2 element picks up AND the Carrier Aided signal is received

The figure below shows the simplified scheme logic:

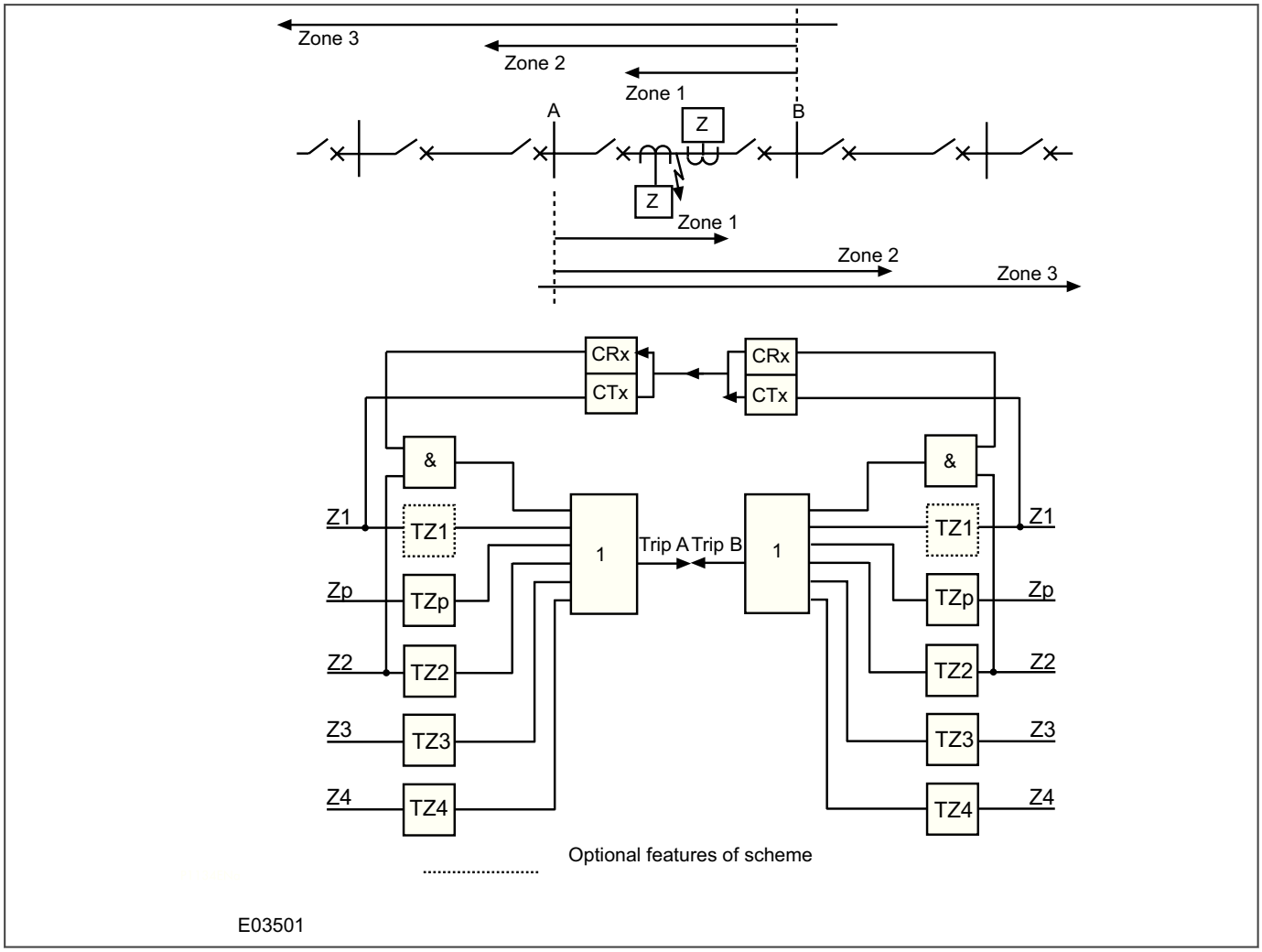


Figure 120: Aided distance PUR scheme

9.3.3 PERMISSIVE OVER-REACH SCHEME

Permissive Over-reach schemes are variously referred to as POR, POP, POTT. We normally use the term POR.

In a Permissive Overreach scheme the channel is keyed (that means that the aiding signal is asserted) by the pickup of an over-reaching Zone 2 element.

To use this scheme, you need to set the relevant setting (***Aid. 1 Selection*** or ***Aid. 2 Selection***) in the *SCHEME LOGIC* column to `POR`.

If a remote protection element detects a forward fault and receives a POR signal, the protection operates without further delay. Faults in the last 20% of the protected line are therefore cleared with minimal time delay.

> *Note:*
> *This assumes a 20% typical end-zone when Zone 1 is set to 80% of the protected line.*

The following are some of the main features and requirements for a POR scheme:

- The scheme requires a duplex signalling channel to prevent possible maloperation if a carrier is keyed for an external fault. Because the signalling channel can be keyed for faults external to the protected zone, it is vital

that they are only received by, and acted upon by, the intended recipient. A simplex channel cannot assure this.

- A POR scheme may be more advantageous than a PUR scheme for the protection of short transmission lines. This is because the resistive coverage of the Zone 2 elements may be greater than that of the Zone 1 elements (in the case of Mho elements)
- Current reversal guard logic prevents healthy-line protection maloperation for high speed current reversals that can be experienced on double circuit line applications, which can be caused by sequential opening of circuit breakers.
- If the signalling channel fails, basic distance scheme tripping remains available.

The POR logic is:

- Send logic: Assert signal if Zone 2 element picks up.
- Permissive trip logic: Trip if the Zone 2 element operates AND the Channel Aided signal is received.

The POR scheme also uses the reverse looking zone 4 as a reverse fault detector. This is used in the current reversal logic and in the weak infeed echo feature, shown dotted in the figure below:

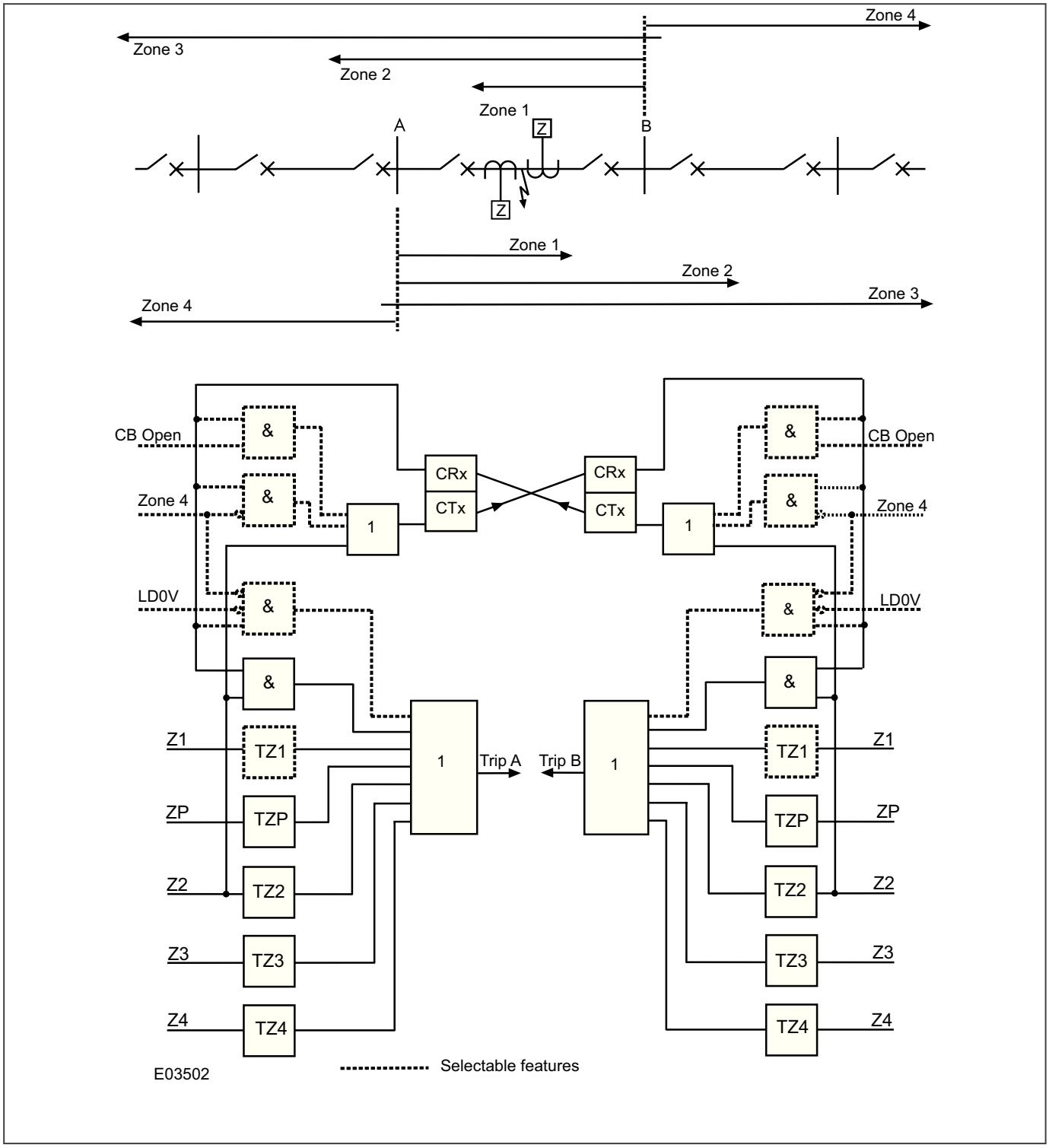


Figure 121: Aided distance POR scheme

The POR scheme is enhanced by POR Trip Reinforcement, and POR Weak Infeed features.

9.3.3.1 PERMISSIVE OVERREACH TRIP REINFORCEMENT

The send logic in the POR scheme is arranged so that for any trip command at a local end, the local protection sends a Channel Aided signal to the remote end(s). This facilitates fault isolation at each terminal as quickly as possible. The send signal is generated by the ***Any Trip*** command, and it is sent on any channel that is being used.

This feature is called permissive trip reinforcement. It is designed to ensure that synchronous tripping occurs at all protected terminals.

9.3.3.2 PERMISSIVE OVERREACH WEAK INFEED FEATURES

Special weak infeed logic (WI) can be used with the POR schemes. The ***Weak Infeed*** setting can be found in the *SCHEME LOGIC* column. ***Weak Infeed*** can be set to `Echo`, `Echo and Trip`, or `Disabled`.

Weak infeed echo

For a POR scheme, a signal is normally sent only if the appropriate signal associated with the pick up of the sending zone detects a fault. However, under some circumstances, the fault current infeed at one line end may be so low that it is insufficient to operate any of the distance zones. In another scenario, if a circuit breaker at one of the terminals is in an open state, the current infeed will be zero. These scenarios are termed Weak Infeed (WI) conditions. Without special attention they could result in slow fault clearance at the terminal that is feeding the fault current (called the 'strong infeed' terminal). This would typically result in tripping after the Zone 2 time delay (tZ2). To avoid Zone 2 delayed tripping, a device subject to Weak Infeed conditions can be set to echo signals received on the Channel Aided link back to the initiating IED without delay. This allows the devices at points of strong infeed to permissively trip instantaneously.

The Weak Infeed Echo Send logic is:

- No Distance Zone Operation has been detected, but a POR Aided signal has been received.

Weak infeed echo and trip

The Weak infeed echo logic will produce an aided trip at a strong infeed terminal, but it does not produce a trip at the weak infeed. Setting ***Weak Infeed*** to `Echo and Trip` allows tripping of the weak infeed circuit breaker of a faulted line. Three undervoltage elements, ***Va<***, ***Vb<*** and ***Vc<*** are used to detect the line fault at the weak infeed terminal. This voltage check prevents tripping during spurious operations of the channel or during channel testing.

The Weak Infeed Echo and Trip logic is:

- No Distance Zone Operation has been detected, but a POR signal has been received, AND a ***V<*** condition exists.

Weak infeed tripping is time delayed according to the value set in the ***WI Trip Delay*** settingin the *SCHEME LOGIC* column. Due to the use of phase segregated undervoltage elements, single-phase tripping can be enabled for WI trips if required. If single-phase tripping is disabled, under Weak Infeed conditions, three-phase tripping will occur after the ***WI Trip Delay*** time has expired.

Weak infeed trip can be blocked with the ***Blk WITrip PDead*** setting when the line is dead (All Poles Dead) after a settable amount of time ***WItrip Pdead Dly***. This feature is `Disabled` by default.

CB open echo

A feature is provided which enables fast tripping to be maintained along the whole length of the protected line, even when one terminal is open. This is the ***CB Open Echo*** feature and is initiated by a settable time ***CB Open Echo Dly*** (250ms by default) after the ***Breaker Open*** optical isolator has been energised. This time delay prevents an unnecessary open terminal echo due to the delay in drop off of the signal send following a trip. However, there will be no time delay introduced in echoing the signal when the breaker is already open. This feature is `Enabled` by default.

9.3.4 PERMISSIVE SCHEME LOSS OF GUARD

This scheme is intended for use with frequency shift keyed (FSK) power line carrier (PLC) communications.

When the protected line is healthy, a guard frequency is sent between line ends to verify the channel is in service. However, when a line fault occurs and a permissive trip signal must be sent over the line, the power line carrier frequency is shifted to a different (trip) frequency. Therefore the distance function should receive either the guard frequency or the trip frequency, but not both together. For certain fault types, the line fault can attenuate the PLC

signals so the permissive signal is lost and not received at the other line end. To overcome this problem, when the guard is lost and no trip frequency is received, the protection opens a window of time during which the permissive scheme logic acts as though a trip signal had been received. Two opto-isolated inputs need to be assigned: One is for Channel Receive; The second is designated Loss of Guard (the inverse function to guard received).

The Loss of Guard logic is described in the table below:

System Condition	Permissive Channel Received	Loss of Guard	Permissive Trip Allowed	Alarm Generated
Healthy Line	No	No	No	No
Internal Line Fault	Yes	Yes	Yes	No
Unblock	No	Yes	Yes, during a 150 ms window	Yes, delayed on pickup by 150 ms
Signalling Anomaly	Yes	No	No	Yes, delayed on pickup by 150 ms

The window of time during which the unblocking logic is enabled starts 10ms after the guard signal is lost, and continues for 150ms. The 10ms delay gives time for the signalling equipment to change frequency, as in normal operation. For the duration of any alarm condition, Zone 1 extension logic is invoked if the ***Z1 Ext Scheme*** setting is set to operate for channel failure.

9.3.5 CURRENT REVERSAL GUARD LOGIC

For double circuit lines, the fault current direction can change in one circuit when circuit breakers open sequentially to clear the fault on the parallel circuit. The change in current direction causes the overreaching distance elements to see the fault in the opposite direction to the direction in which the fault was initially detected (settings of these elements exceed 150% of the line impedance at each terminal). The race between operation and resetting of the overreaching distance elements at each line terminal can cause permissive overreach, and blocking schemes to trip the healthy line. A system configuration that could result in current reversals is shown in the figure below. For a fault on line L1 close to circuit breaker B, as circuit breaker B trips it causes the direction of current flow in line L2 to reverse. Current reversal guard logic is incorporated in this product to prevent POR and Blocking schemes from tripping incorrectly during current reversal conditions.

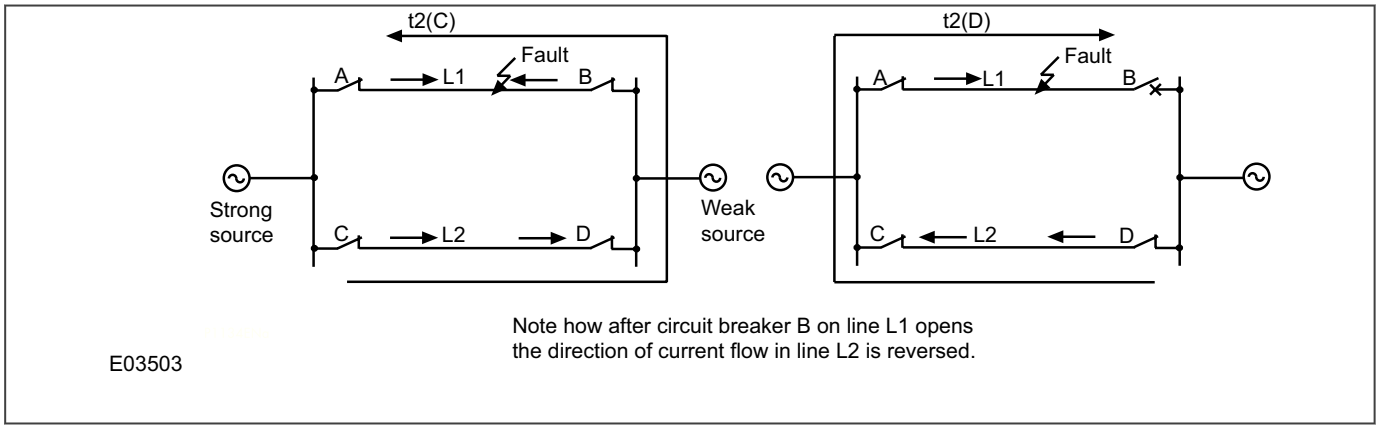


Figure 122: Example of fault current reversal of direction

The current reversal guard incorporated in the permissive overreach scheme logic is initiated when the reverse looking Zone 4 elements operate on a healthy line.

Once the reverse looking Zone 4 elements have operated, the permissive trip logic and signal send logic are inhibited at substation D. The reset of the current reversal guard timer is initiated when the reverse looking Zone 4 resets. A time delay ***tReversal Guard*** is required in case the overreaching trip element at end D operates before the signal send from the protection at end C has reset. Otherwise this would cause the product at D to overreach.

Permissive tripping for the products at D and C substations is enabled again once the faulted line is isolated and the current reversal guard time has expired.

The current reversal guard incorporated in the blocking scheme logic is initiated when a blocking element picks-up to inhibit the channel-aided trip. When the current reverses and the reverse looking Zone 4 elements reset, the blocking signal is maintained by the timer ***tReversal Guard***. Therefore, the protections in the healthy line are prevented from overreaching due to the sequential opening of the circuit breakers in the faulted line. After the faulted line is isolated, the reverse-looking Zone 4 elements at substation C and the forward looking elements at substation D reset.

Two variants of Blocking scheme are available:

- Blocking 1 (Reversal Guard applied to the Signal Send)
- Blocking 2 (Reversal Guard applied to the Signal Receive)

9.3.6 AIDED DISTANCE BLOCKING SCHEMES

Two default Blocking schemes are provided:

- Blocking 1
- Blocking 2

The two schemes are similar. Both schemes feature current reversal guard signals used in conjunction with reverse looking Zone 4 elements. In the Blocking 1 scheme, the current reversal guard signal applies to the send signal, whereas in the Blocking 2 scheme, the current reversal guard signal applies to the receive signal.

The signalling channel is keyed from operation of the reverse-looking Zone 4 elements. If the remote zone 2 element picks up, it operates after the trip delay if no block is received. Listed below are some of the main features and requirements for a Blocking scheme:

- Blocking schemes require only a simplex communication channel.
- Reverse-looking Zone 4 is used to send a blocking signal to the remote end to prevent unwanted tripping.
- When a simplex channel is used, a blocking scheme can easily be applied to a multi-terminal line provided that outfeed does not occur for any internal faults.
- The blocking signal is transmitted over a healthy line, and so problems associated with power line carrier signals failing are avoided.
- Blocking schemes provide similar resistive coverage to the permissive overreach schemes.
- Fast tripping occurs at a strong source line end, for faults along the protected line section, even if there is weak- or zero- infeed at the other end of the protected line.
- If a line terminal is open, fast tripping still occurs for faults along the whole of the protected line length.
- If the signalling channel fails to send a blocking signal during a fault, fast tripping occurs for faults along the whole of the protected line, but also for some faults in the next line section.
- If the signalling channel is taken out of service, the protection operates in the conventional basic mode.
- A current reversal guard timer is included in the logic to prevent unwanted tripping on healthy circuits during current reversal situations on a parallel circuits.

The Blocking scheme logic is:

- Send logic: Assert carrier if Reverse Zone 4 element picks up
- Trip logic: Trip if the Zone 2 element picks up if no carrier is received, but only after the Aided Signal Delay time out

The figure below shows the simplified scheme logic.

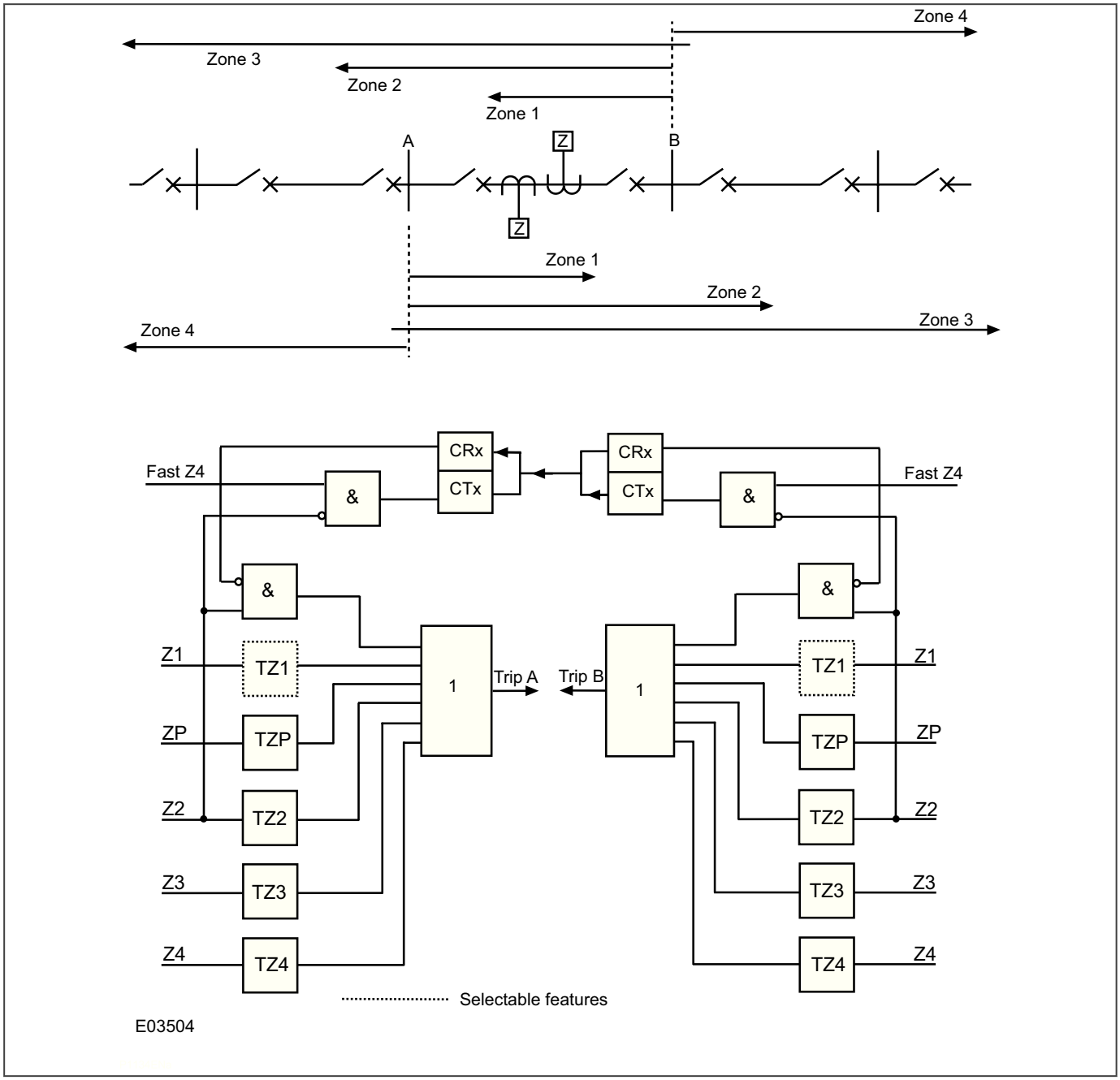


Figure 123: Aided distance blocking scheme (BOP)

9.3.7 AIDED DISTANCE UNBLOCKING SCHEMES

The Unblocking schemes are specifically designed for use with Power Line Carrier (PLC) communications where different frequencies are used to indicate that a guard (no-fault condition) or a trip (fault condition) signal should be transmitted to the remote terminal(s). Normally, either a guard signal or a trip signal should be transmitted and received. Under certain fault conditions however, the PLC signal can be heavily attenuated or even lost completely. In such conditions, Permissive Overreach Unblocking schemes allow the permissive tripping to operate for a short period after the carrier is lost. This ensures fast, selective fault clearance.

To use this scheme you need to assign two inputs. Generally, the inputs are mapped to opto-inputs in the default PSL. The table below shows a default mapping for Aided Scheme 1.

DDB Signal (Opto-input)	DDB Signal
Input L3 (DDB: 34)	***Aided 1 Scheme Rx*** (DDB: 493)
Input L4 (DDB: 35)	***Aided 1 COS/LGS*** (DDB: 492)

The ***Aided 1 Scheme RX*** signal corresponds to a 'channel-receive' signal for scheme 1. The ***Aided 1 COS/LGS*** signal corresponds to a 'channel out of service' or 'loss of guard' signal ('Loss of guard' is the inverse signal to 'guard received').

As well as the default mapping, it is possible to map the signals to other inputs if required.

The window during which the unblocking logic is enabled starts 10ms after the guard signal is lost and continues for 150ms. The 10ms delay gives time for the signalling equipment to change frequency.

Note:
*If the **Z1 Ext Scheme** setting is set to operate for channel failure, the Zone 1 extension logic will be invoked if a channel failure is detected.*

This scheme type also provides Loss of Guard logic as described below.

System Condition	Permissive Channel Received	Loss of Guard	Permissive Trip Allowed	Alarm Generated
Healthy Line	No	No	No	No
Internal Line Fault	Yes	Yes	Yes	No
Unblock	No	Yes	Yes, during a 150 ms window	Yes, delayed on pickup by 150 ms
Signalling Anomaly	Yes	No	No	Yes, delayed on pickup by 150 ms

9.3.8 AIDED DISTANCE LOGIC DIAGRAMS

9.3.8.1 AIDED DISTANCE SEND LOGIC

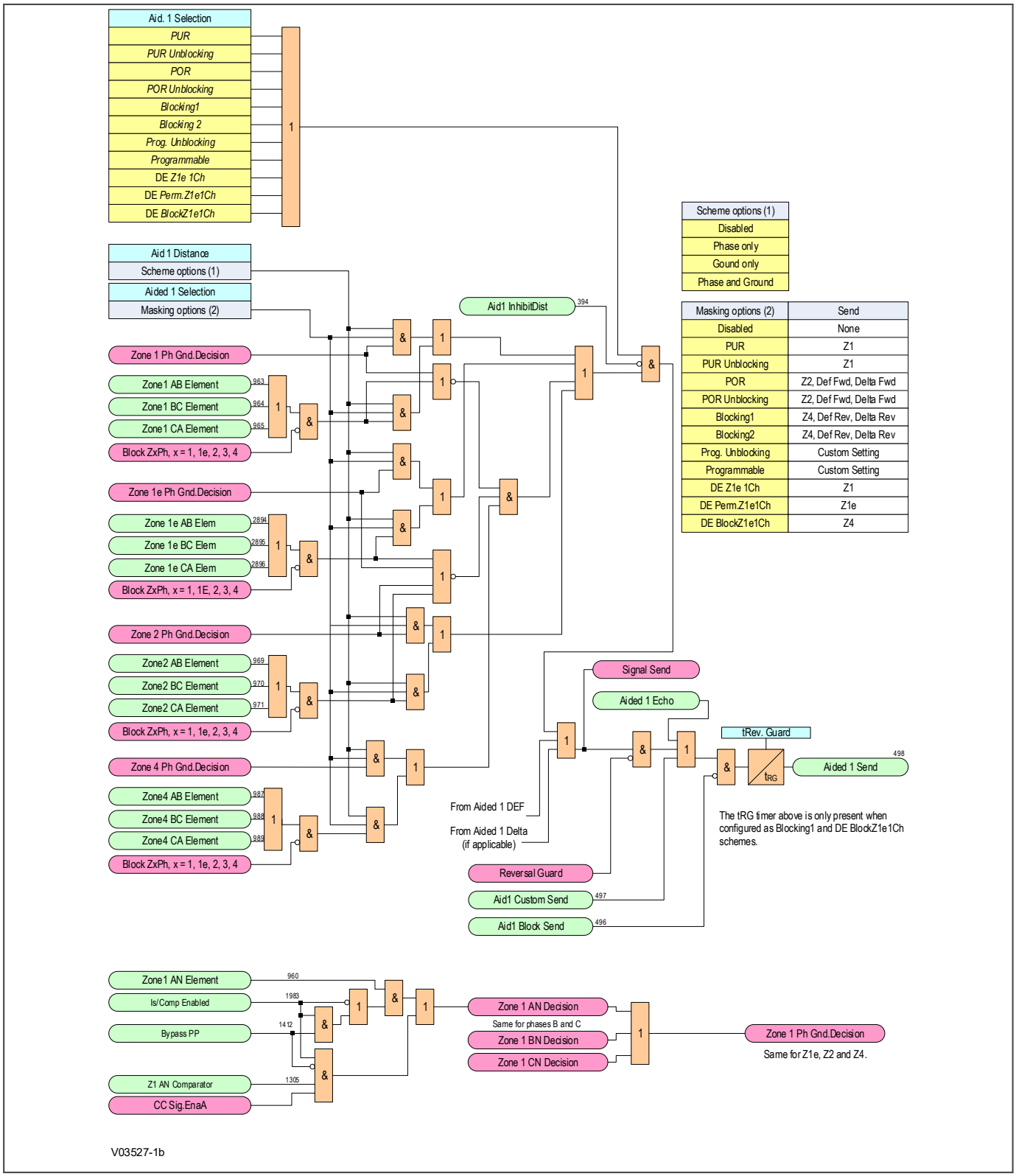


Figure 124: Aided distance send logic 1Ch

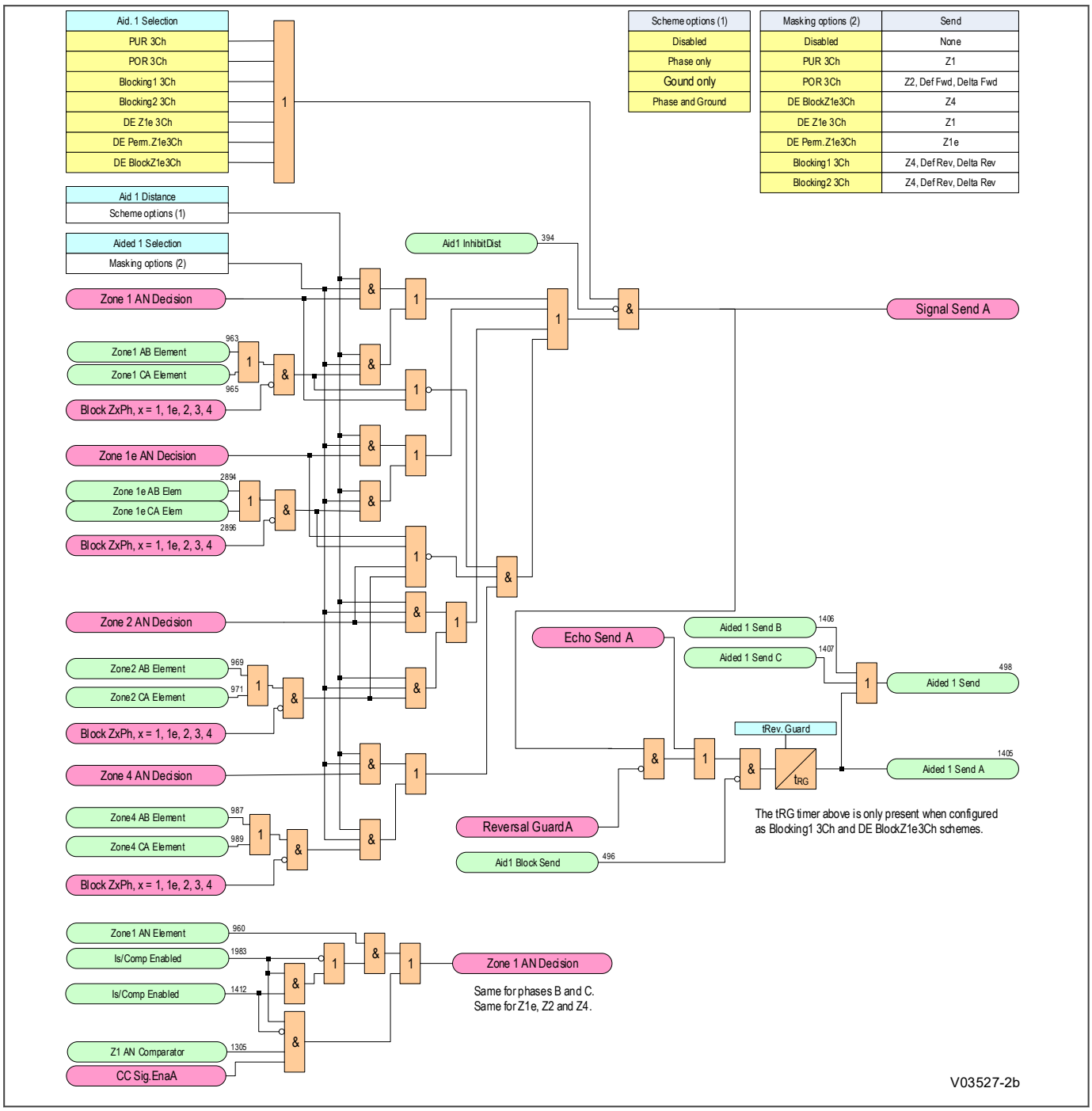


Figure 125: Aided distance send logic ACh

Note:
The logic shown above is for A Channel. B and C channels operate on similar principles.

9.3.8.2 CARRIER AIDED SCHEMES RECEIVE LOGIC

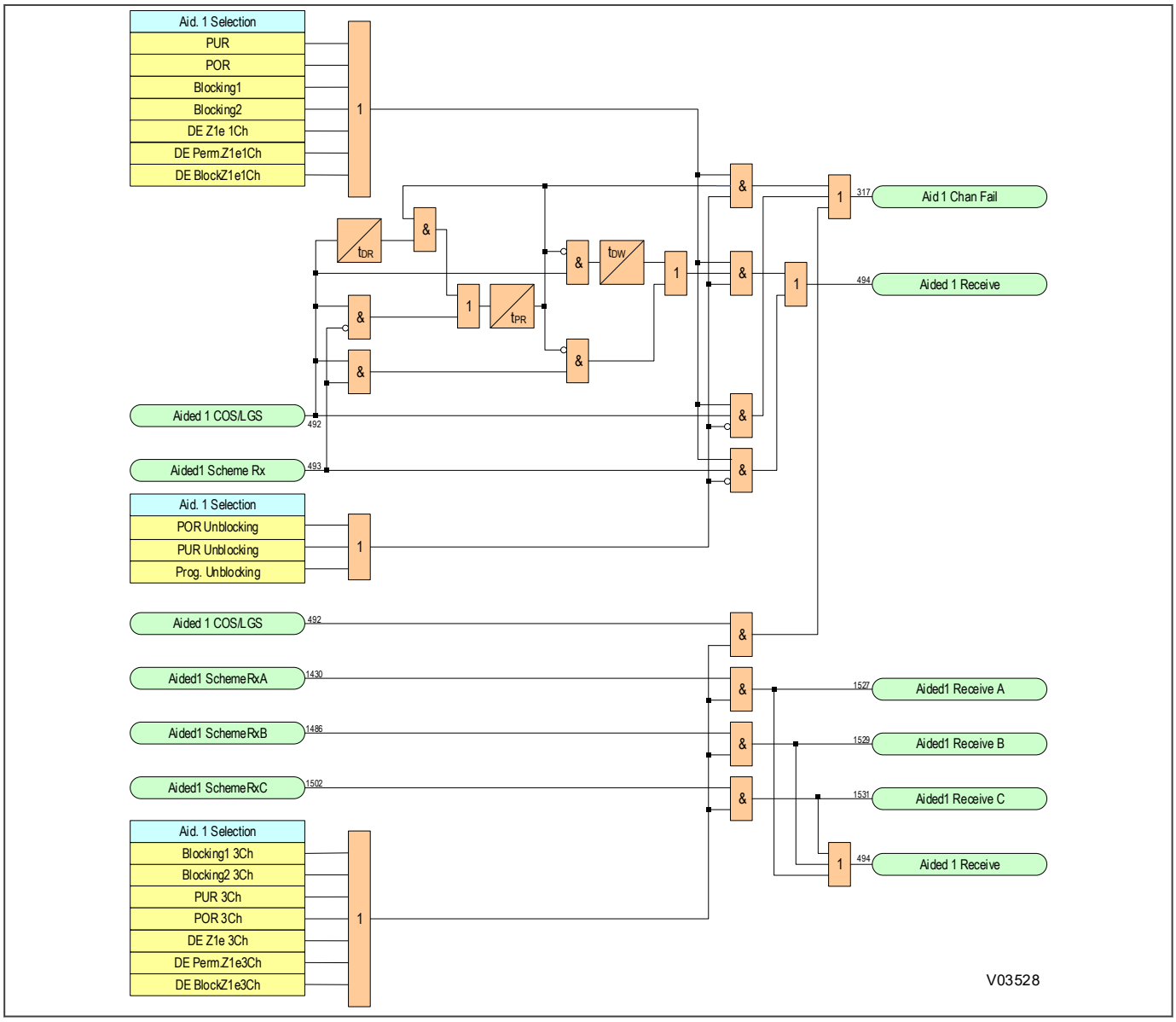


Figure 126: Carrier aided schemes receive logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.3.8.3 AIDED DISTANCE TRIPPING LOGIC

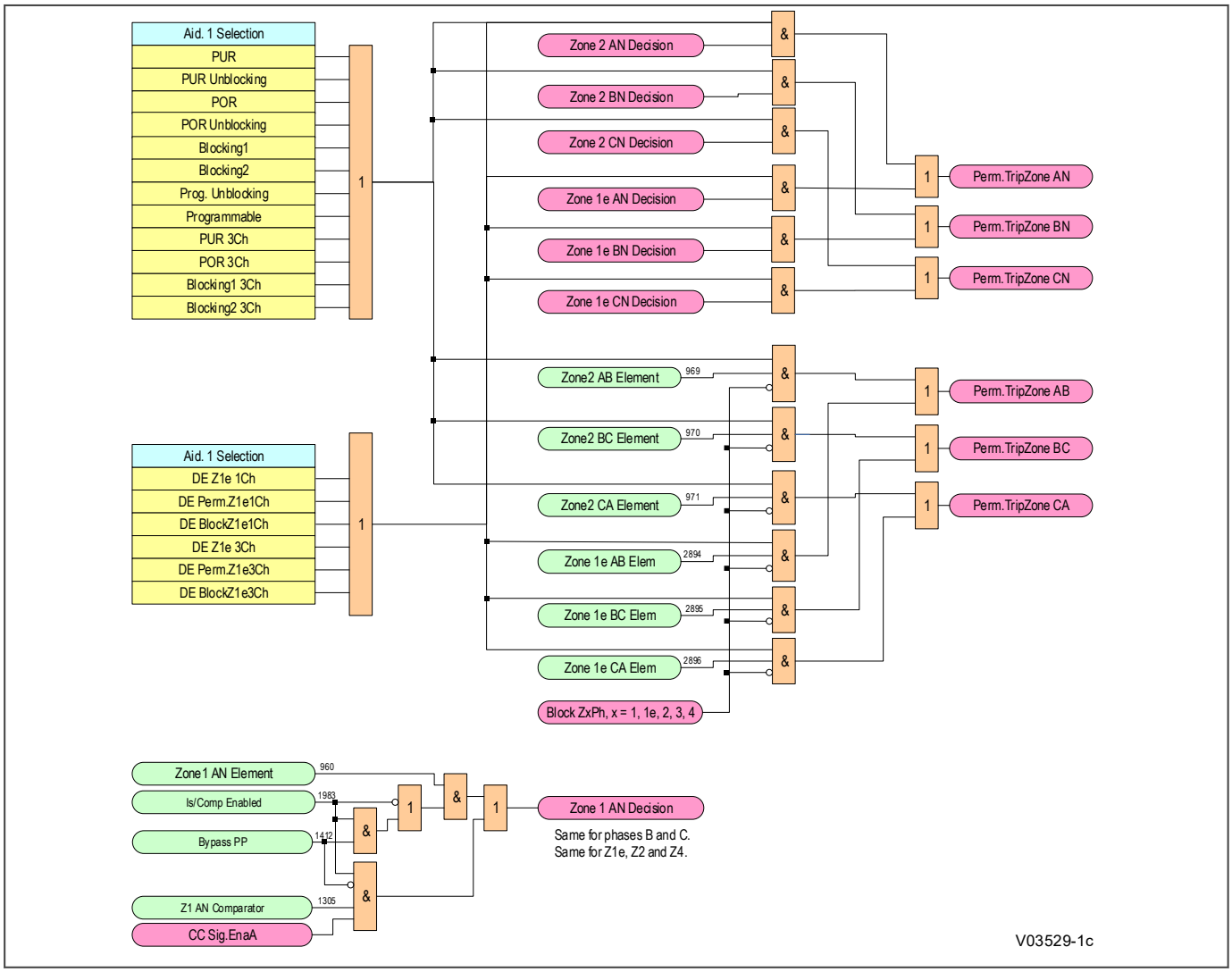


Figure 127: Aided distance tripping logic 1Ch (1 of 2)

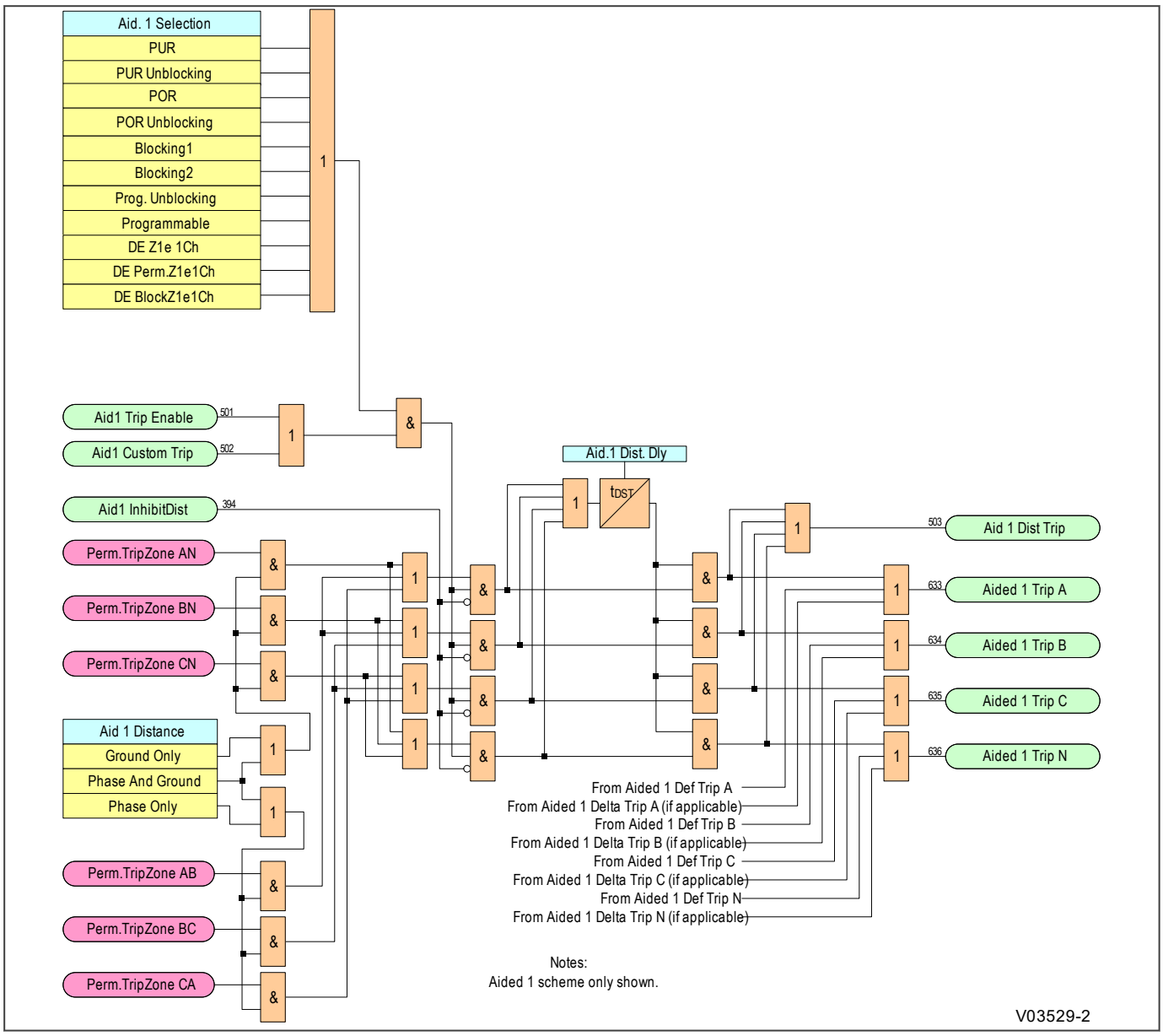


Figure 128: Aided distance tripping logic 1Ch (2 of 2)

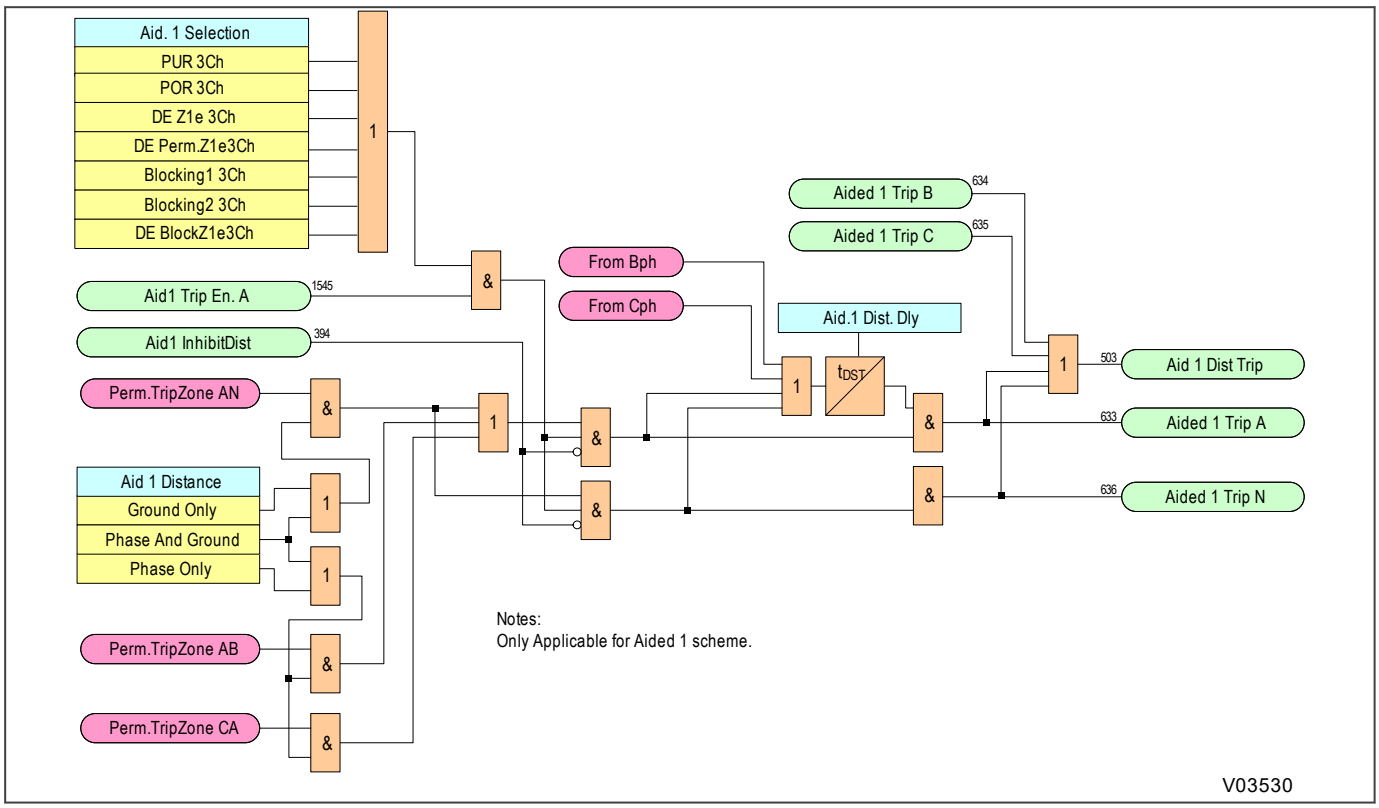


Figure 129: Aided distance tripping logic ACh

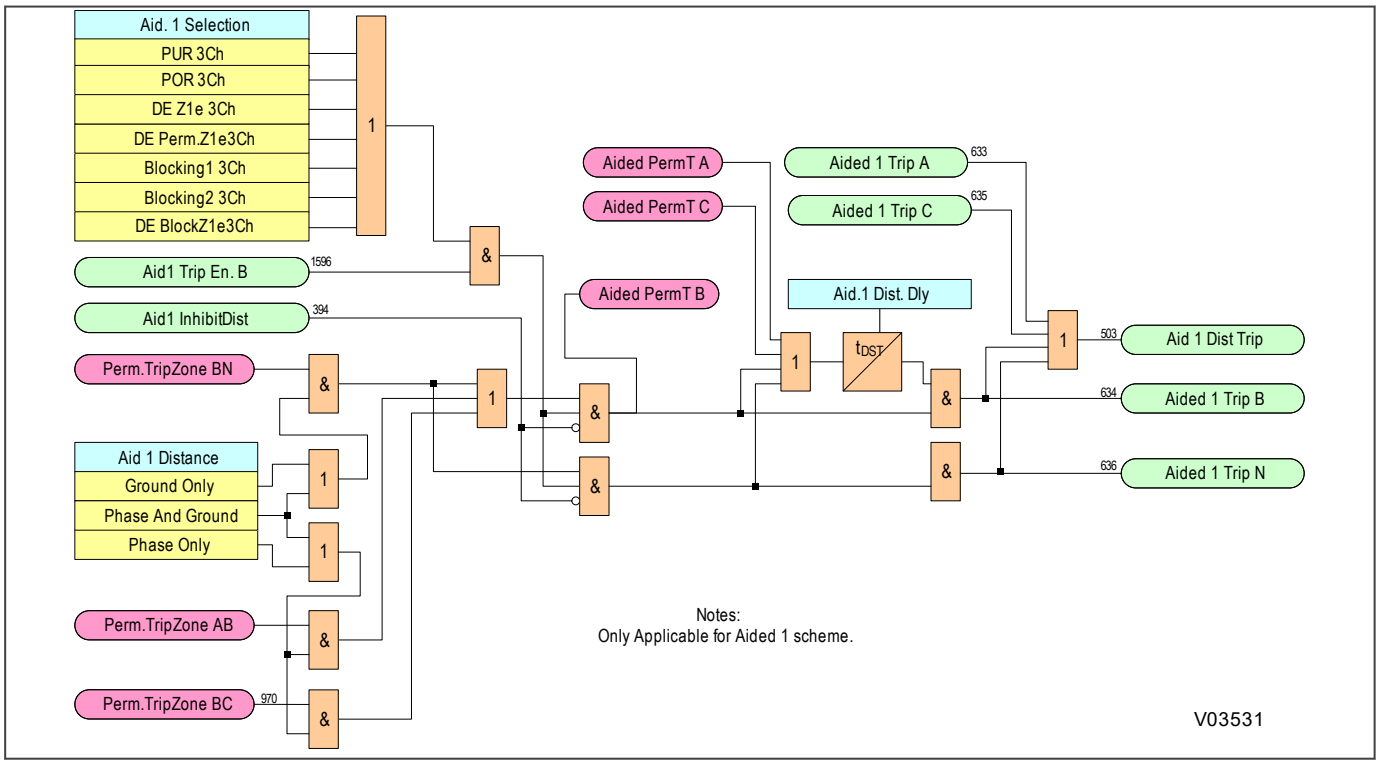


Figure 130: Aided distance tripping logic BCh

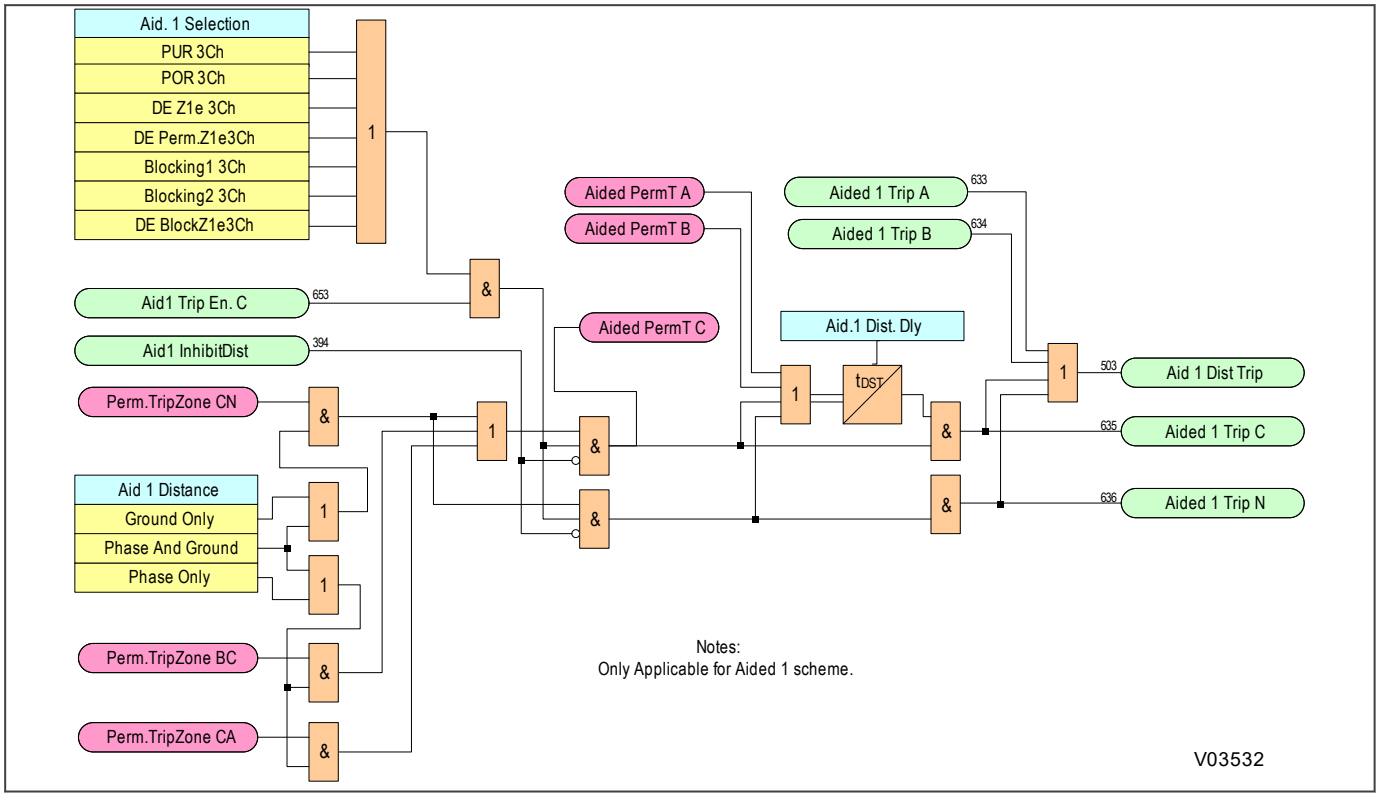


Figure 131: Aided distance tripping logic CCh

9.3.8.4 PUR AIDED TRIPPING LOGIC

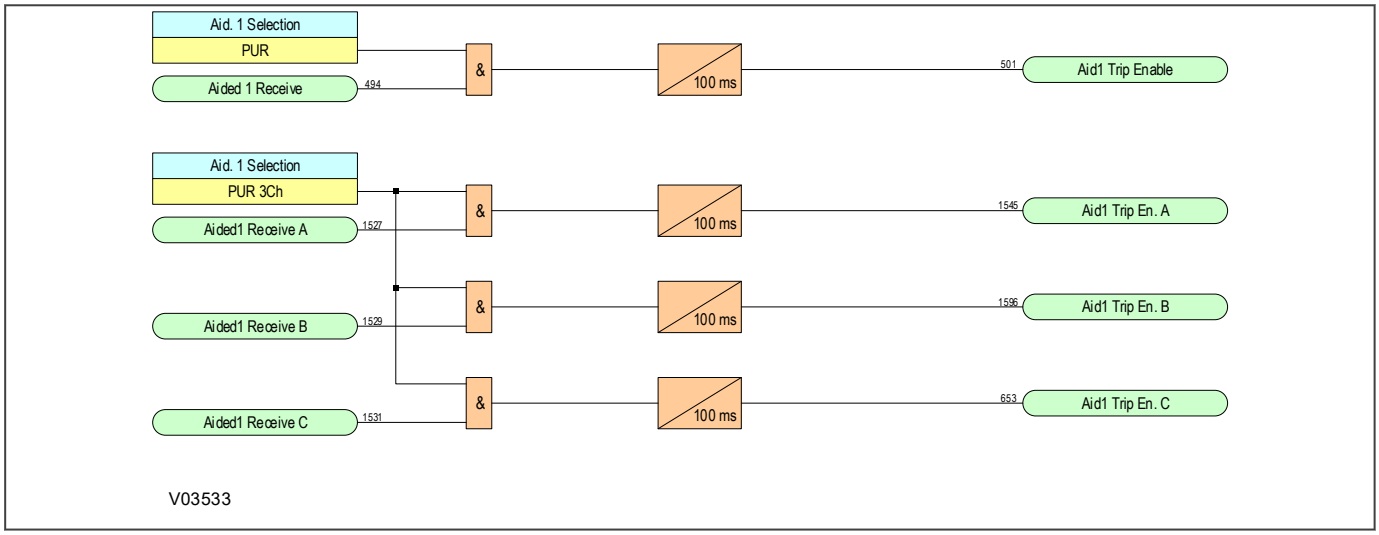


Figure 132: PUR aided tripping logic

9.3.8.5 POR AIDED TRIPPING LOGIC

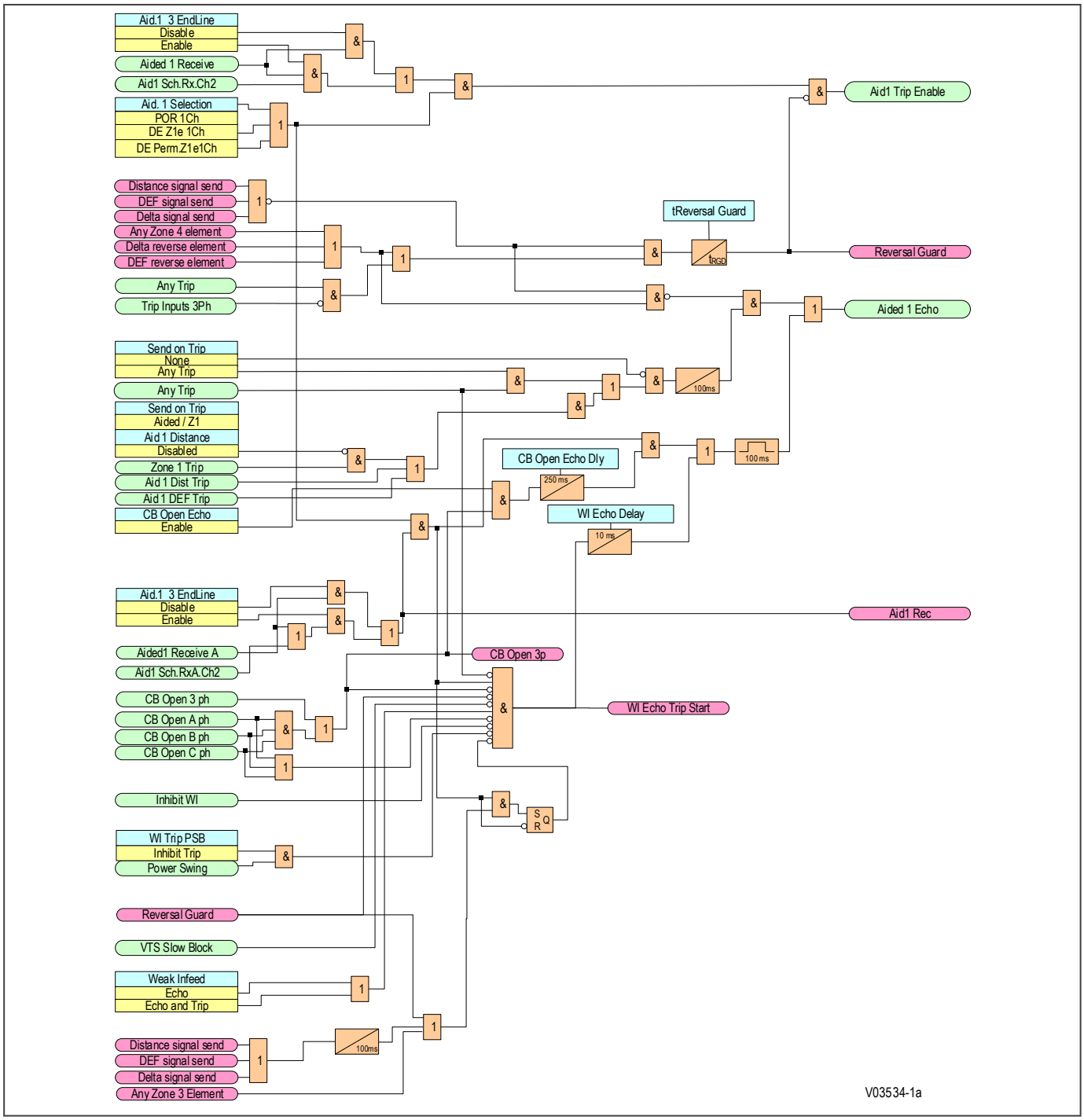


Figure 133: POR aided tripping logic 1Ch (1 of 2)

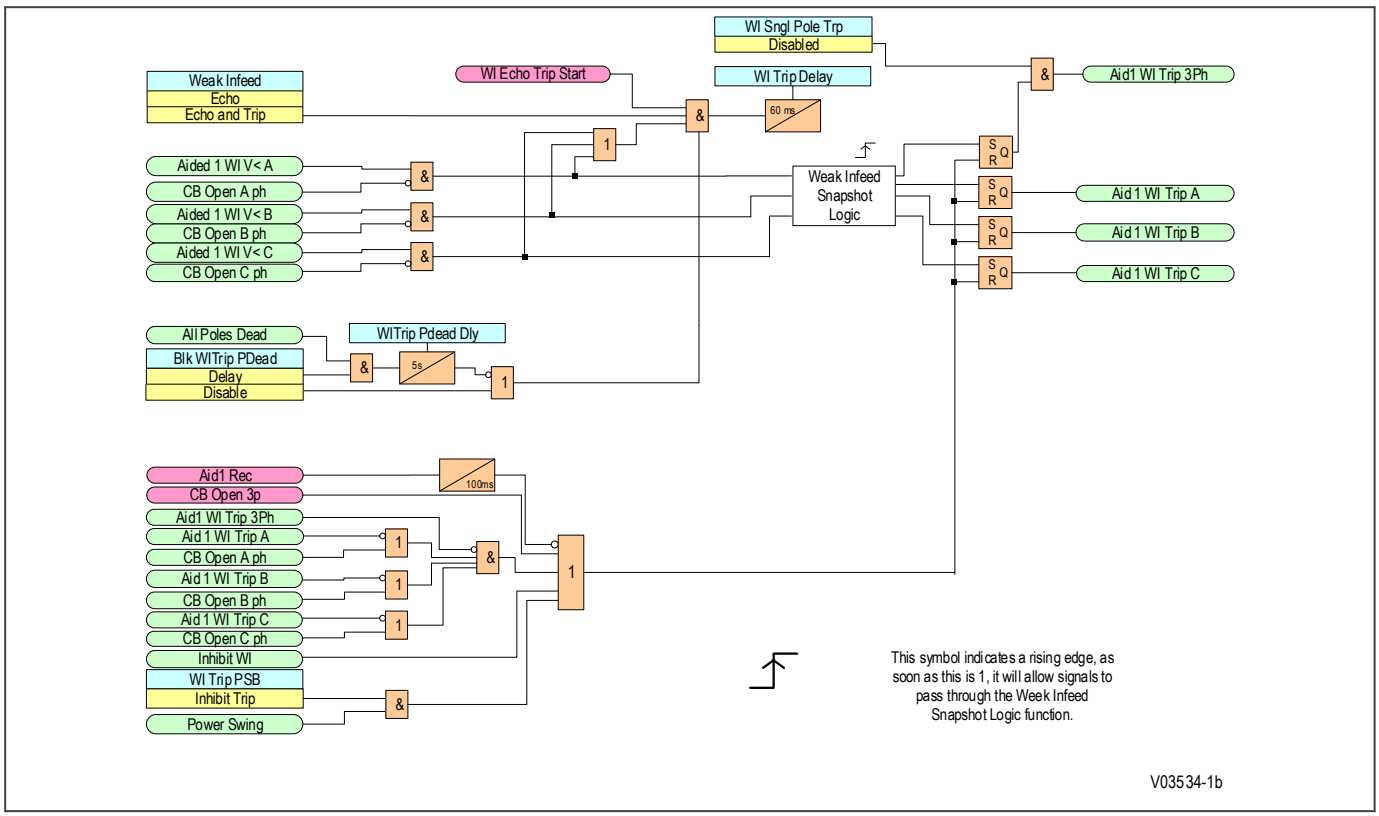


Figure 134: POR aided tripping logic 1Ch (2 of 2) - weak infeed trip

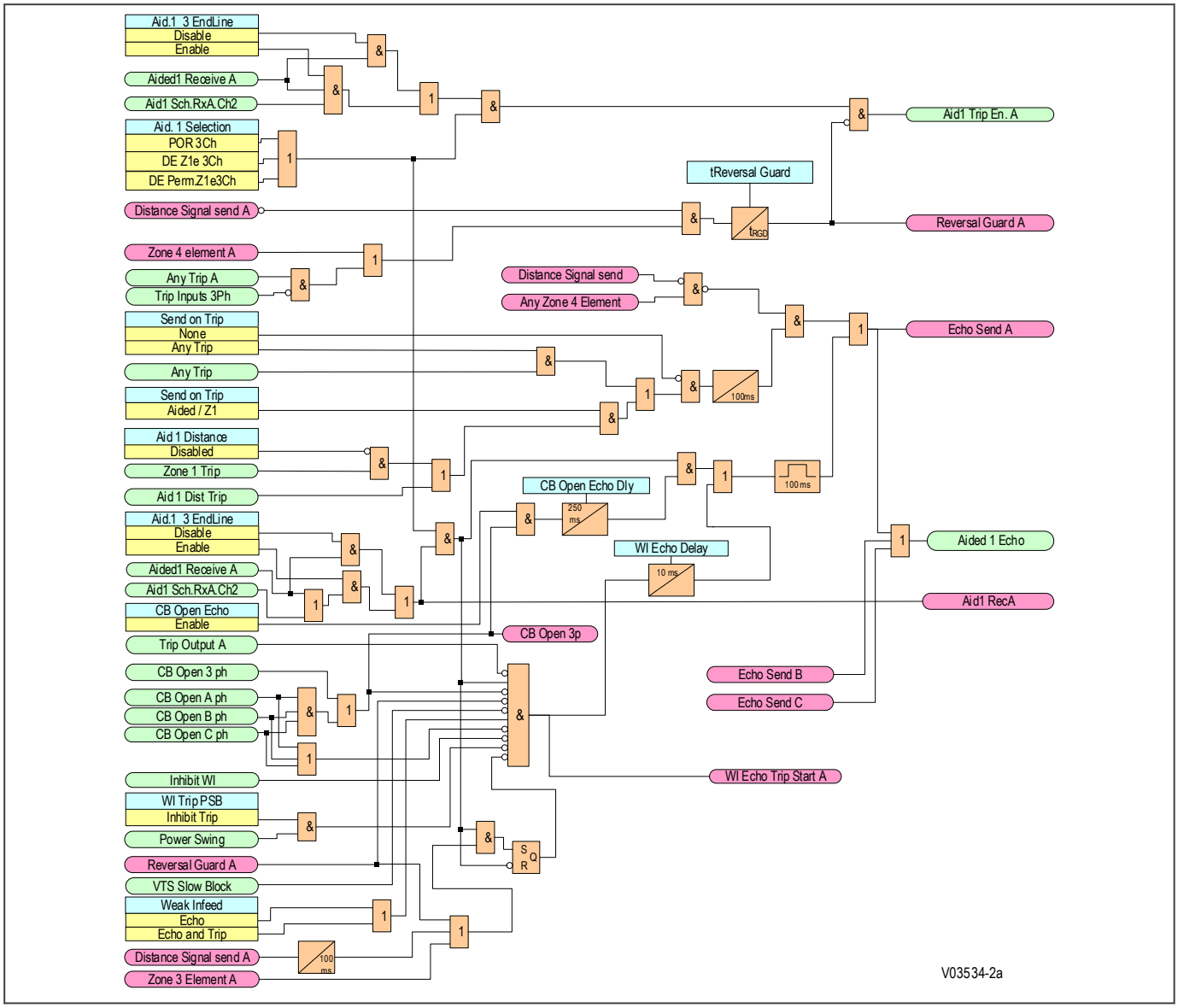


Figure 135: POR aided tripping logic ACh (1 of 2)

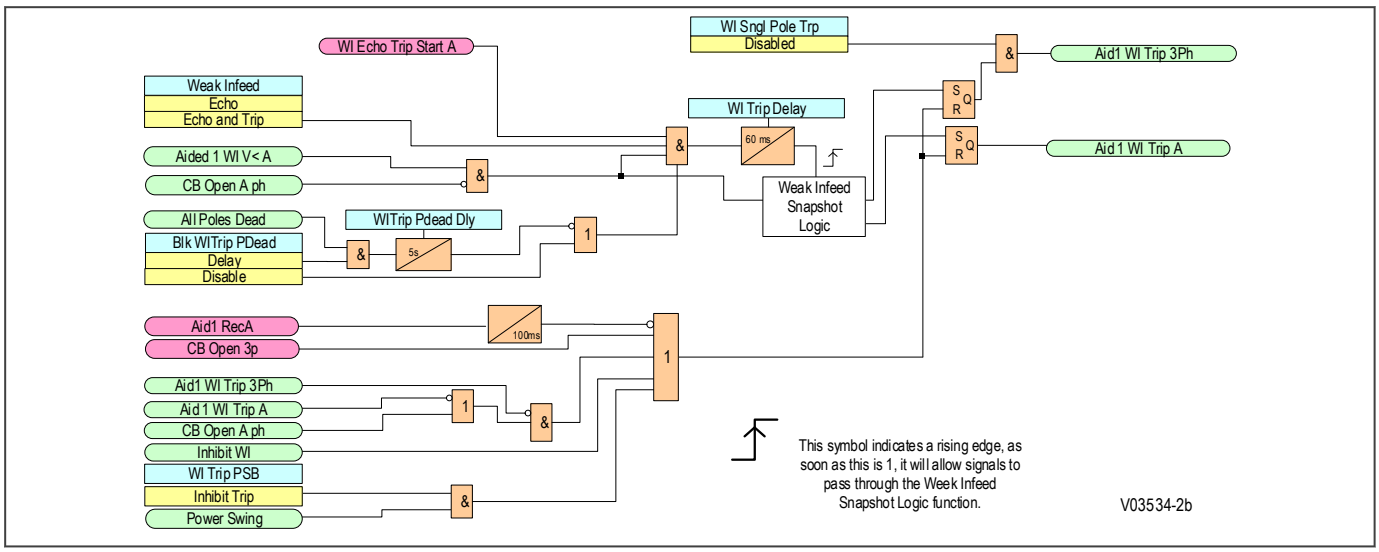


Figure 136: POR aided tripping logic ACh (2 of 2) - weak infeed trip

Note:
The logic shown above is for A Channel. B and C channels operate on similar principles.

9.3.8.6 POR AIDED TRIPPING LOGIC

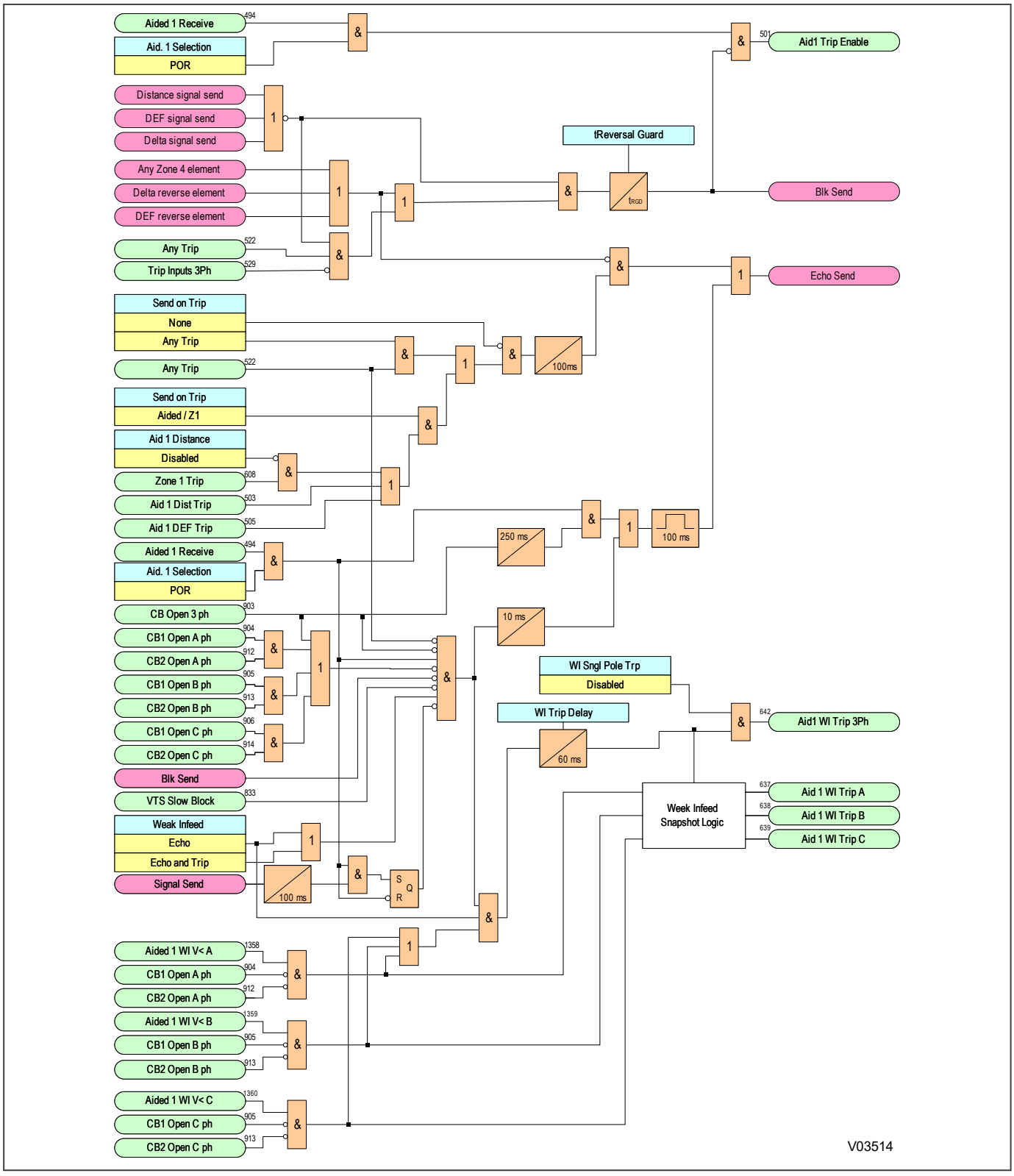


Figure 137: POR aided tripping logic

9.3.8.7 AIDED SCHEME BLOCKING 1 TRIPPING LOGIC

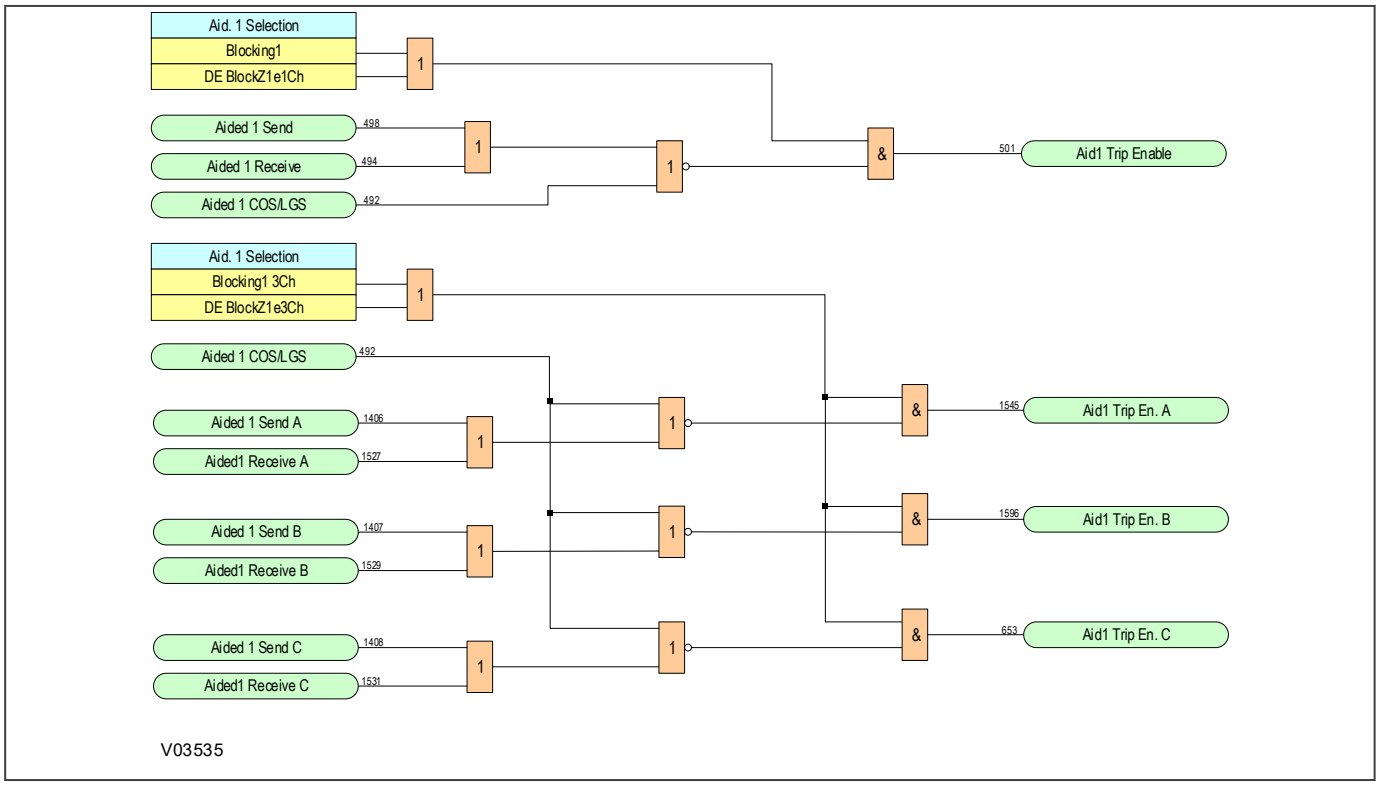


Figure 138: Aided scheme blocking 1 tripping logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.3.8.8 AIDED SCHEME BLOCKING 2 TRIPPING LOGIC

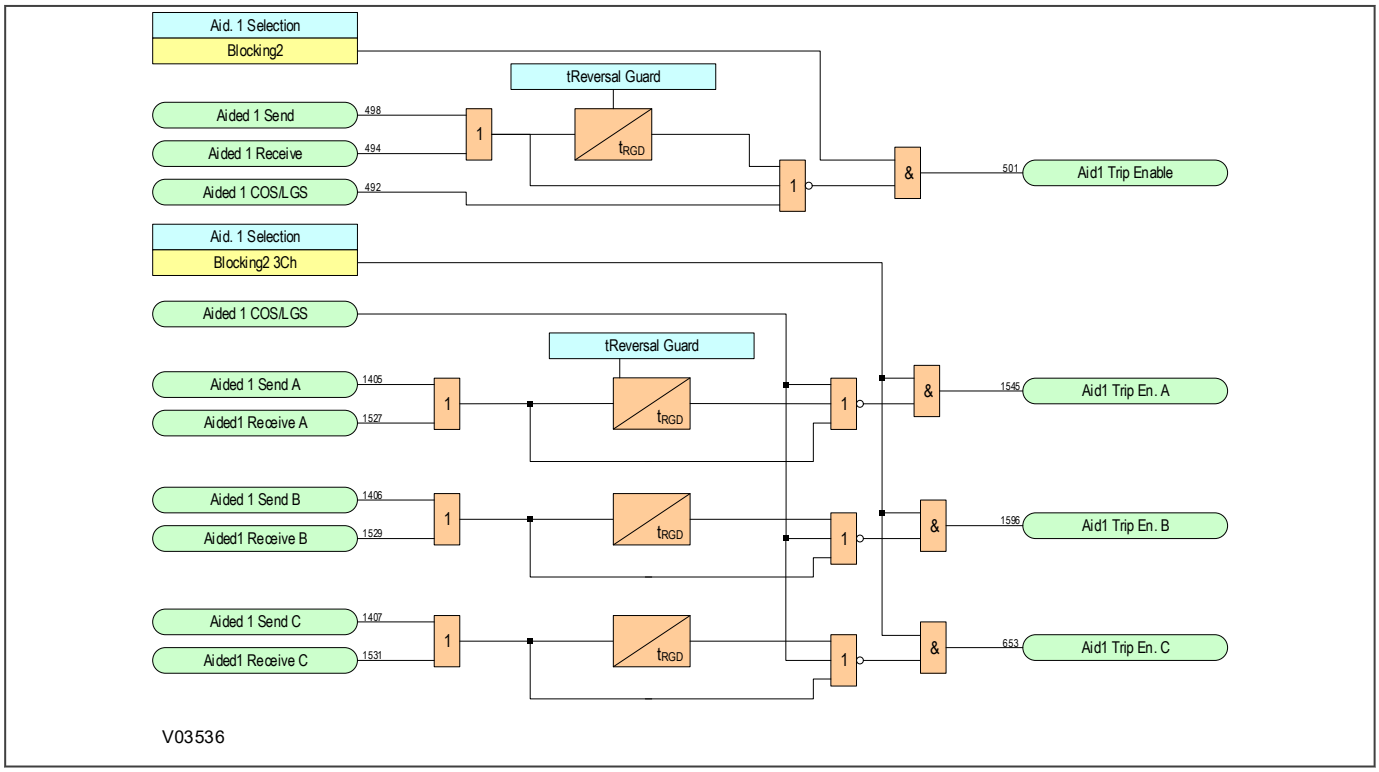


Figure 139: Aided scheme blocking 2 tripping logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.4 AIDED DEF SCHEME LOGIC

9.4.1 AIDED DEF INTRODUCTION

High resistance faults may be difficult to detect using distance protection. A Directional Earth Fault DEF element is sometimes used in conjunction with a communication scheme to provide protection against such faults. The use of Aided-Trip logic in conjunction with the DEF element allows faster trip times, and can facilitate single-phase tripping, if needed.

To use the Aided DEF protection you will need appropriate communication channels between terminals in the scheme. The Programmable Scheme Logic (PSL) allows you to map signals for communication over the channels. The signals you map may be signals to be sent to a remote terminal, or signals expected to be received from a remote terminal. Two Aided DEF schemes are available.

With Aided DEF protection, the residual current (earth fault current) is compared with a threshold to determine the presence of a fault, and a directionalising quantity to determine its direction. Directional measurements from protecting terminals are then used in conjunction with teleprotection signals between the terminals, and aided scheme logic to determine whether the fault is within the protected line (and hence trip), or outside the protected line (and hence restrain).

9.4.2 IMPLEMENTATION

Aided DEF protection can be used with permissive over-reach schemes or blocking schemes.

The Aided DEF protection is enabled using the ***Directional E/F*** setting in the *CONFIGURATION* column. This makes the settings in the *AIDED DEF* column visible.

The Aided DEF requires a polarising quantity (selected in the ***DEF Polarizing*** setting) in conjunction with a characteristic angle setting (***DEF Char. Angle***) to make the directional decision.

For all models a signal derived from the phase voltage inputs can be used for polarisation. For certain models with more VT inputs, a directly measured input can be used.

You have a choice between Zero Sequence Polarising or Negative Sequence Polarising for the Aided DEF element. If you choose Zero Sequence Polarisation, you have a choice to enable an innovative feature known as Virtual Current Polarisation to enhance the Aided DEF function.

Aided DEF protection is blocked if any of the following conditions are met:

- An ***Any Trip*** signal is asserted by one of the integrated protection functions
- The phase selector picks up on more than one phase
- Any of the signals ***Pole Dead A***, ***Pole Dead B***, or ***Pole Dead C*** are asserted

9.4.3 AIDED DEF POLARISATION

There are essentially two ways of establishing the direction of an earth fault:

- Zero sequence polarisation
- Negative sequence polarisation

Zero Sequence polarisation normally uses the measurement of residual voltage (VN). This can only be achieved if a 5-limb VT or three single-phase VTs are used. A special form of zero sequence polarisation called Virtual Current Polarisation is also possible with this device. Virtual Current Polarisation allows directionalisation for low levels of polarisation voltage.

9.4.3.1 ZERO SEQUENCE POLARISING

Residual voltage is generated during earth faults. This zero-sequence quantity can be used to polarize the directional decision of Aided DEF protection. This device can derive residual voltage if connected to a suitable voltage transformer (VT) arrangement.

For the Aided DEF to use a derived voltage signal, the three phase voltage inputs must be supplied from a 5-limb VT, or from three single-phase VTs having the primary star-point earthed. These VT arrangements allow the passage of residual flux and hence allow the device to derive the required residual voltage. A 3-limb VT has no path for residual flux and is therefore unsuitable for zero-sequence Polarisation.

Small levels of residual voltage may be present under normal system conditions due to system imbalances, VT inaccuracies and device tolerances. You can set a threshold (***DEF VNPol Set***) to provide stability against Aided DEF operation under these conditions. Residual voltage (***Vres***) is nominally 180° out of phase with residual current so Aided DEF elements are polarised from the -Vres quantity. This 180° phase shift is automatically compensated in this device.

For products designed to control dual circuit breaker applications you can choose to re-allocate the second check-synchronism VT to provide a measured voltage input to the Aided DEF function. To do this you need to set ***VT2 Selection*** to `Broken Delta` in the *CT AND VT RATIOS COLUMN*. This then reveals the ***DEF Vnpol Input*** setting in the *AIDED DEF* column which can be set to `Measured` or `Derived`.

9.4.3.1.1 VIRTUAL CURRENT POLARISING

A technique called Virtual Current Polarising can allow the Aided DEF protection to operate even if the Polarising voltage is below the ***DEF VNPol Set*** threshold. If the superimposed current phase selector associated with the Distance protection has identified a faulted phase, for example phase A, it removes that phase voltage from the residual calculation Va + Vb + Vc, leaving only Vb + Vc. The resultant Polarising voltage has a large magnitude and is in the same direction as –Vres. This allows the protection to be applied even where very solid earthing behind the protection prevents residual voltage from being developed.

This technique of subtracting the faulted phase is described as Virtual Current Polarising because it removes the need to use current Polarising from a current transformer (CT) in a transformer star (wye)-earth connection behind the device.

If you don't want to use this feature you should set ***Virtual I Pol*** to `Disabled` so that removal of the faulted phase voltage from the residual voltage calculation does not happen. The Aided DEF protection is then Polarised by the residual voltage only.

The directional criteria with zero sequence (virtual current) Polarisation are as follows:

Directional forward

$$90° < (\text{angle}(VNpol) + 180°) - (\text{angle}(IN) - RCA) < 90°$$

Directional reverse

$$90° > (\text{angle}(VNpol) + 180° - (\text{angle}(IN) - RCA) > 90°$$

This is represented in the following figure:

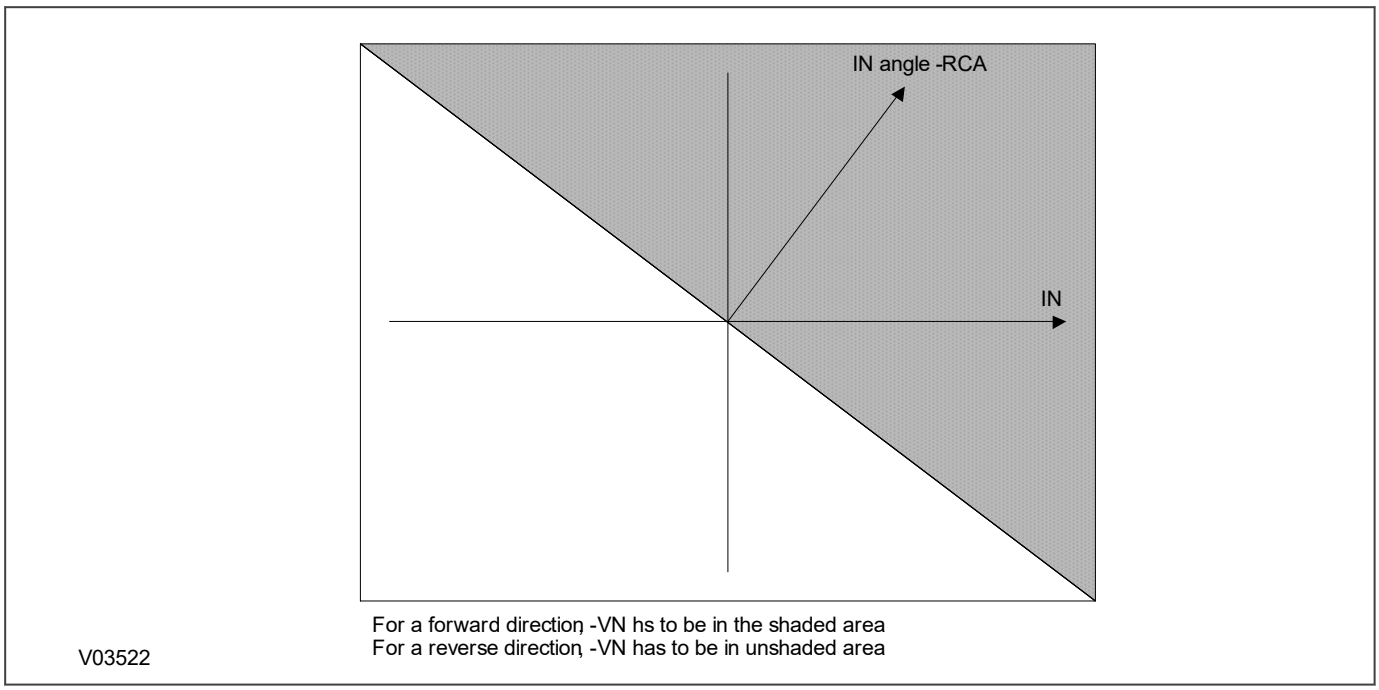


Figure 140: Virtual current polarisation

The Polarising voltage (VNpol) is as per the table below and RCA is the relay characteristic angle defined by the ***DEF Char. Angle*** setting.

Phase Selector Pickup	VNpol
A Phase Fault	VB + VC
B Phase Fault	VA + VC
C Phase Fault	VA + VB
No Selection	VN = VA + VB + VC

Note:
*The virtual current polarisation works if the **DEF Polarizing** setting is `Zero Sequence`, the **Virtual I Pol** setting is `Enabled`, and the VN voltage is less than the selected value of the **DEF VNpol Set** setting.*

9.4.3.2 NEGATIVE SEQUENCE POLARISING

In certain applications, residual voltage polarisation of Aided DEF may not be possible, or it may be problematic. Example cases are:

- Where a 3-limb voltage transformer is fitted, which has no path for residual flux.
- Where the application features a parallel line and zero sequence mutual coupling may exist.

The problems in these applications can be alleviated using negative phase sequence (nps) voltage for polarisation. The nps voltage threshold must be set in the cell ***DEF V2pol Set***.

Note:
This setting is 3 times V2.

Note:
*The current quantity used for operation of the Aided DEF when it is nps Polarised is the residual current, not the nps current, i.e. settings **DEF FWD** Set and **DEF REV Set** are for residual current.*

Note:
*The minimum negative sequence current required for nps polarisation is the value set by the setting, **DEF REV Set***

The directional criteria with negative sequence polarisation are as follows:

Directional forward

$$-90° < [(\text{angle}(V2) + 180°) - (\text{angle}(I2) - RCA)] < 90°$$

Directional reverse

$$-90° > [(\text{angle}(V2) + 180°) - \text{angle}(I2) - RCA)] > 90°$$

where RCA is the relay characteristic angle set in the ***DEF Char. Angle*** setting.

This is represented in the following figure:

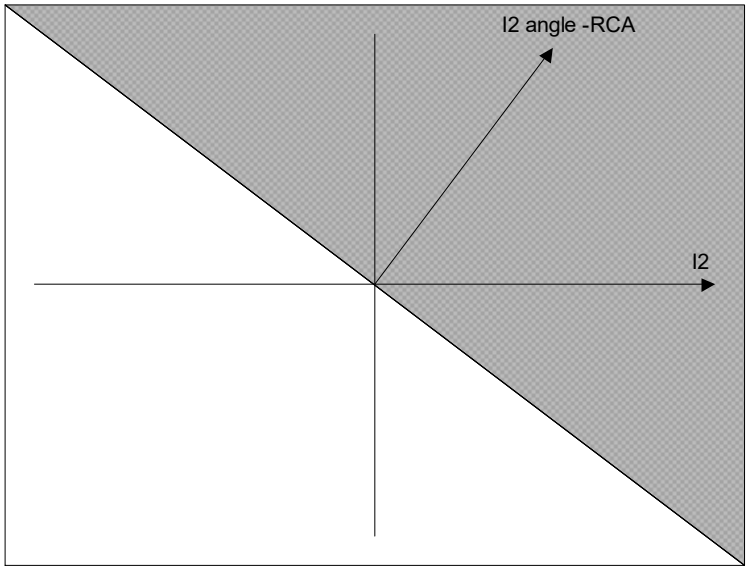


Figure 141: Directional criteria for residual voltage polarisation

9.4.4 AIDED DEF SETTING GUIDELINES

To use Aided DEF protection you need to set the polarisation and the thresholds. Polarisation can be achieved using either zero sequence signals or negative sequence signals.

For zero sequence polarised Aided DEF, the typical zero sequence voltage on a healthy system can be as high as 1% (i.e.: 3% residual), and the voltage transformer (VT) error could be 1% per phase. A ***VNpol Set*** setting between 1% and 4%.Vn is typical, to avoid spurious detection on standing signals. The residual voltage measurement provided in the *MEASUREMENTS 1* column may assist in determining the required threshold setting during commissioning, as this will indicate the level of standing residual voltage present. The Virtual Current Polarising feature will create a polarising voltage, which is always large regardless of whether actual VN is present.

With Aided DEF, the residual current under fault conditions lies at an angle lagging the polarised voltage. Hence, negative characteristic angle settings are required for Aided DEF applications. This is set in cell ***DEF Char. Angle*** in the *EARTH FAULT* settings.

The following angle settings are recommended for a residual voltage polarised device:-

- Solidly earthed distribution systems: -45°
- Solidly earthed transmissions systems: -60°

If ***Virtual I Pol*** is set to 'Disabled' it prevents checking of the faulted phase and subsequent removal of the faulted phase voltage. The aided DEF protection is then polarised by the residual voltage only.

For negative sequence polarisation, the relay characteristic angle settings (***DEF Char. Angle***) must be based on the angle of the upstream negative phase sequence source impedance. A typical setting is -60°.

The ***DEF FWD Set*** setting determines the current sensitivity (trip sensitivity) of the aided DEF aided scheme. This setting must be set higher than any standing residual current unbalance. A typical setting will be between 10% and 20% In.

The ***DEF REV Set*** setting determines the current sensitivity for the reverse earth fault. The setting must always be below the aided DEF forward threshold for correct operation of blocking schemes and to provide stability for current reversal in parallel line applications. The recommended setting is 2/3 of the Aided DEF forward setting.

Note:
*The **DEF REV Set** setting has to be above the maximum steady state residual current imbalance.*

9.4.5 AIDED DEF POR SCHEME

The scheme has the same features and requirements as the corresponding Distance scheme and provides sensitive protection for high resistance earth faults.

The signalling channel is keyed from operation of the forward ***DEF Fwd Set*** element. If the remote device has also detected a forward fault, it operates with no additional delay when it receives this signal.

The logic is:

- Send logic: Key channel if ***DEF Fwd Set*** picks up
- Permissive trip logic: Trip if ***DEF Fwd Set*** picks up AND the channel key is received

The figure below shows the element reaches, and the simplified scheme logic of the Aided DEF POR scheme.

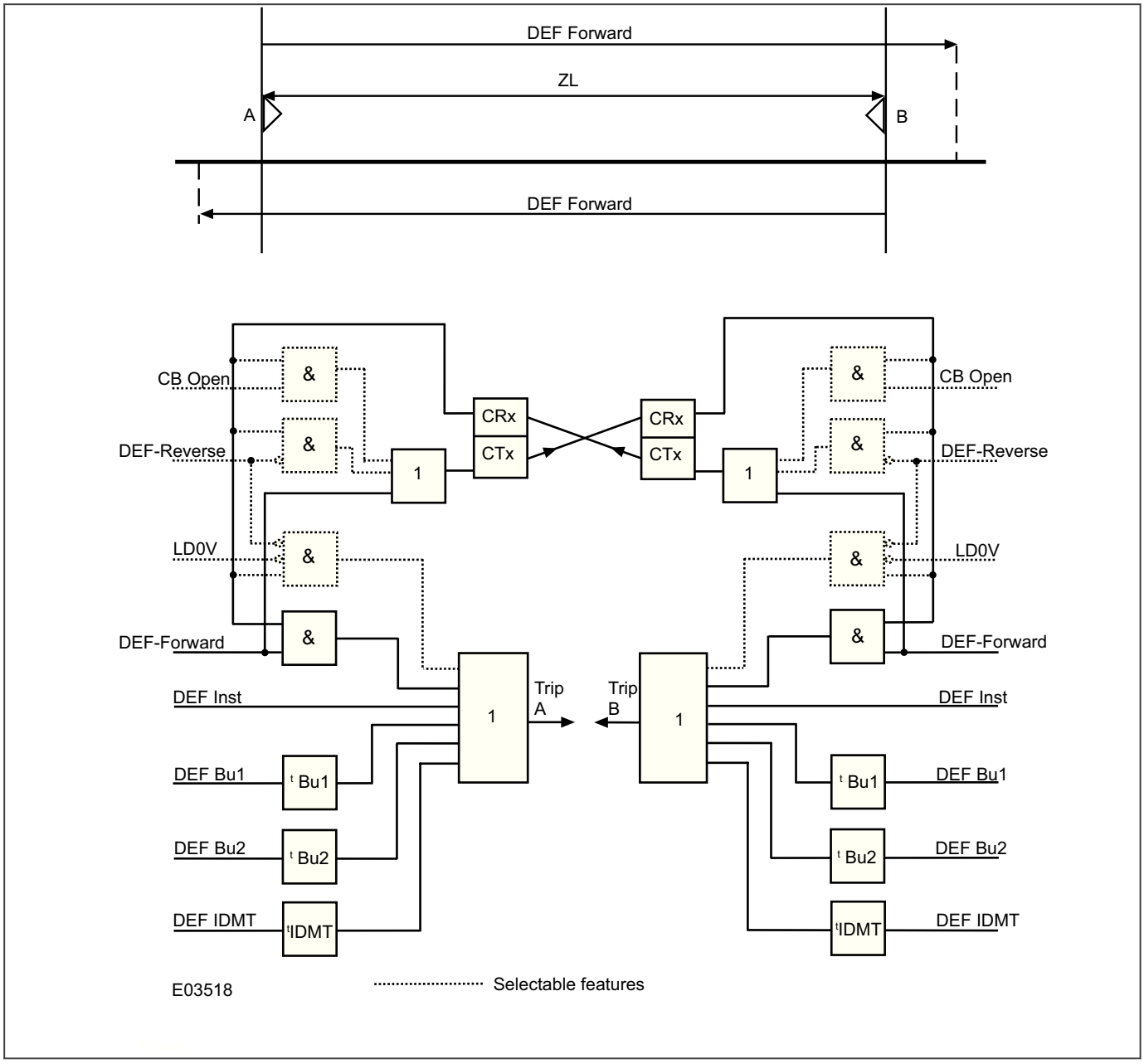


Figure 142: Aided DEF POR scheme

9.4.6 AIDED DEF BLOCKING SCHEME

The scheme has the same features/requirements as the corresponding Distance scheme and provides sensitive protection for high resistance earth faults.

The signalling channel is keyed from operation of the reverse Aided DEF element (***DEF REV Set***). If the remote device's forward Aided DEF element (***DEF FWD Set***) has picked up, it operates after the ***Aid. 1 DEF Dly.*** expires if no block is received.

Where 't' is shown in the diagram this signifies the time delay associated with an element. To allow time for a blocking signal to arrive, a short time delay on aided tripping must be used.

The logic is:

- Send logic: Key channel if ***DEF REV Set*** picks up
- Trip logic: Trip if ***DEF FWD*** Set AND Channel NOT Received, after ***Aid. 1 DEF Dly.*** expires.

The figures below show the element reaches, and the simplified scheme logic of the Aided Directional Earth Fault (Aided DEF) Blocking scheme.

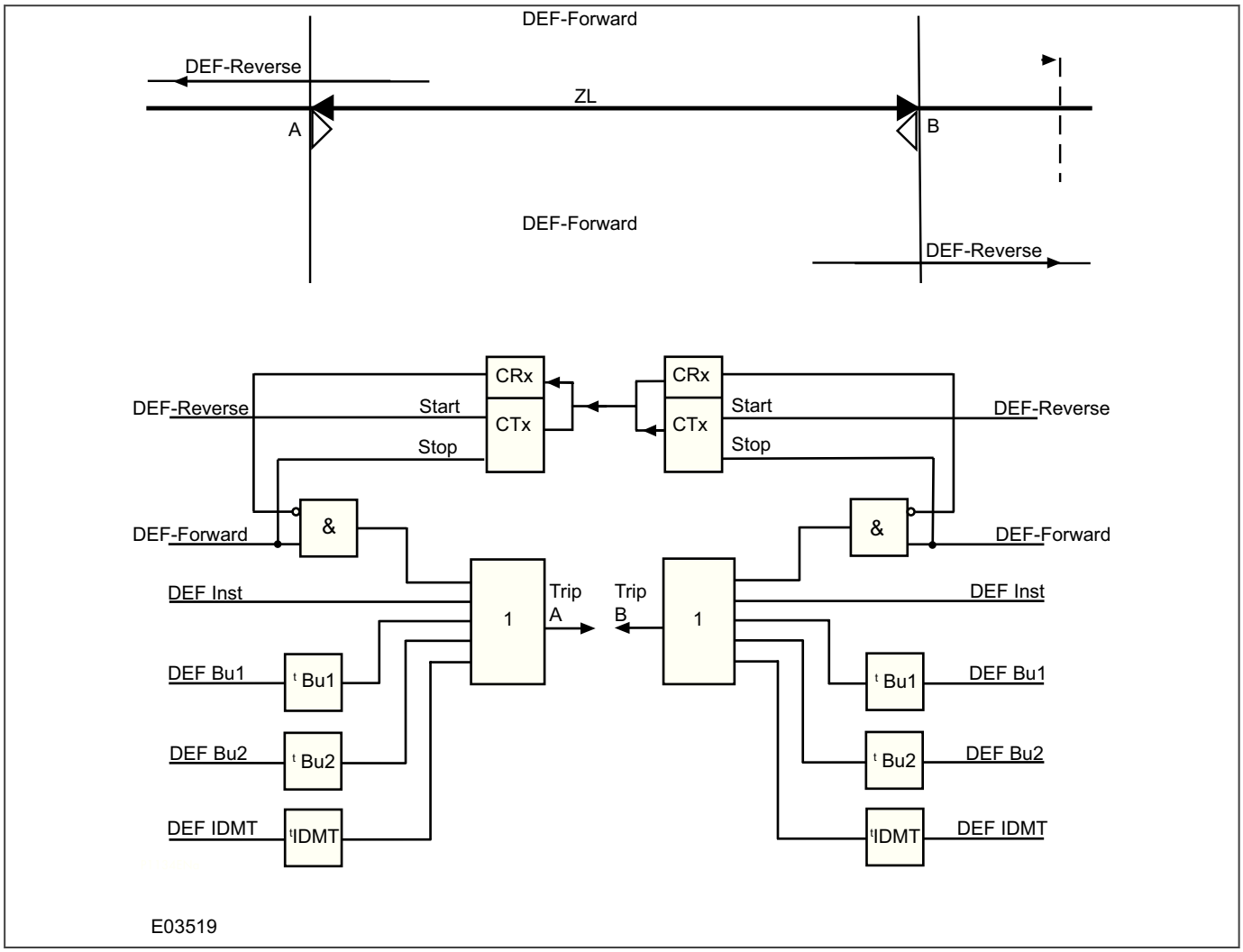


Figure 143: Aided DEF blocking scheme

9.4.7 AIDED DEF LOGIC DIAGRAMS

9.4.7.1 DEF DIRECTIONAL SIGNALS

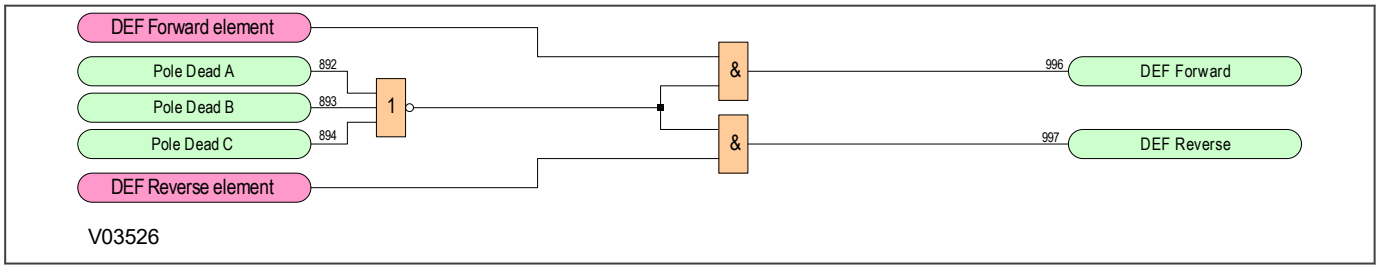


Figure 144: DEF directional signals

9.4.7.2 AIDED DEF SEND LOGIC

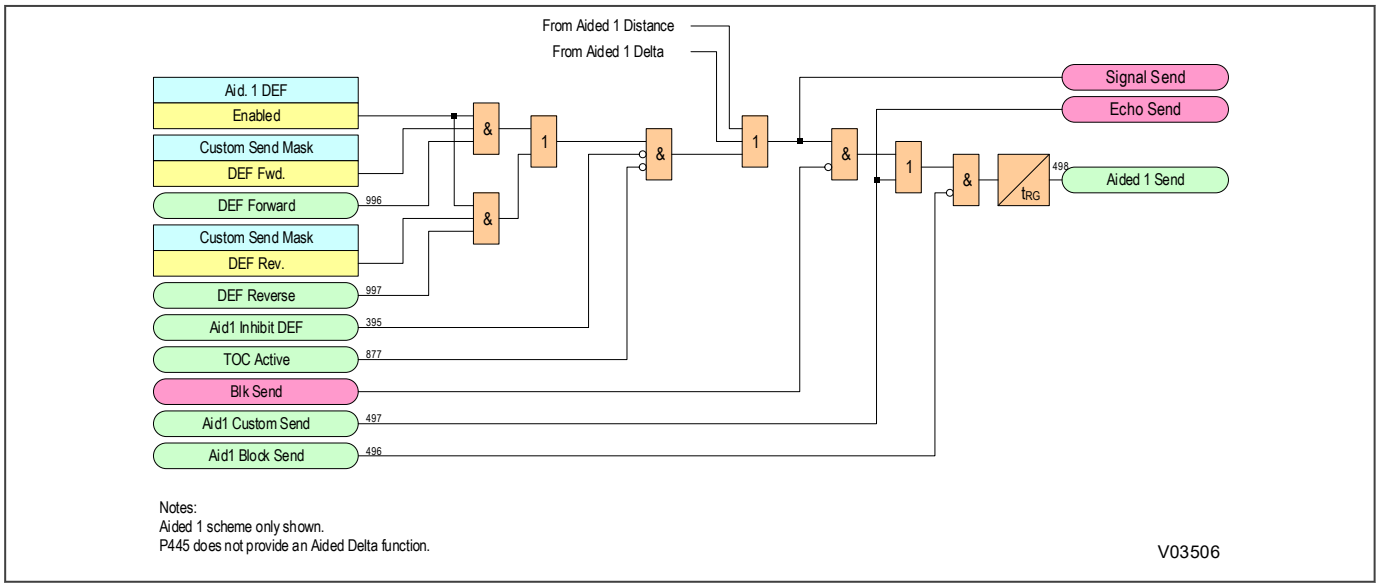


Figure 145: Aided DEF send logic

9.4.7.3 CARRIER AIDED SCHEMES RECEIVE LOGIC

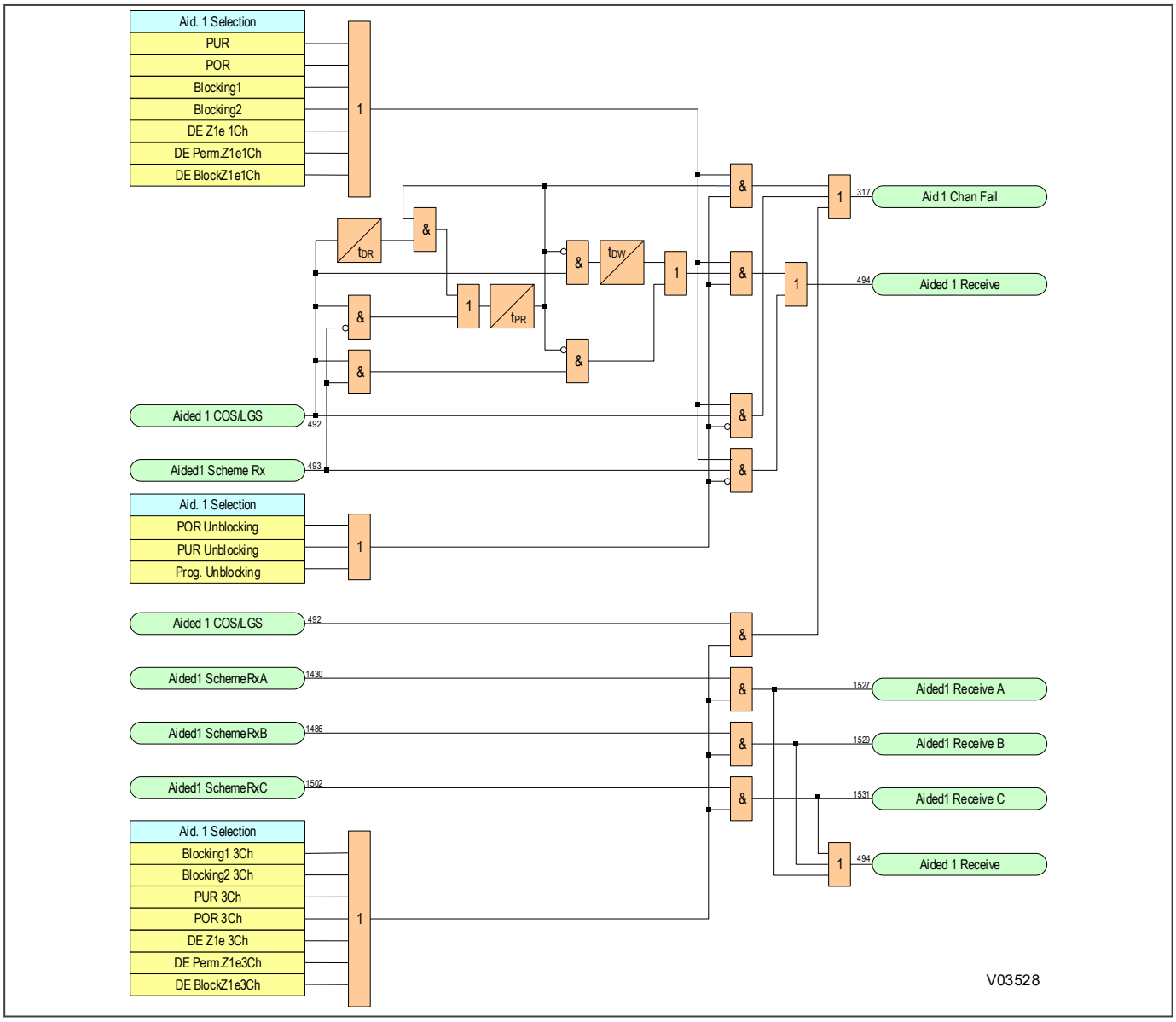


Figure 146: Carrier aided schemes receive logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.4.7.4 AIDED DEF TRIPPING LOGIC

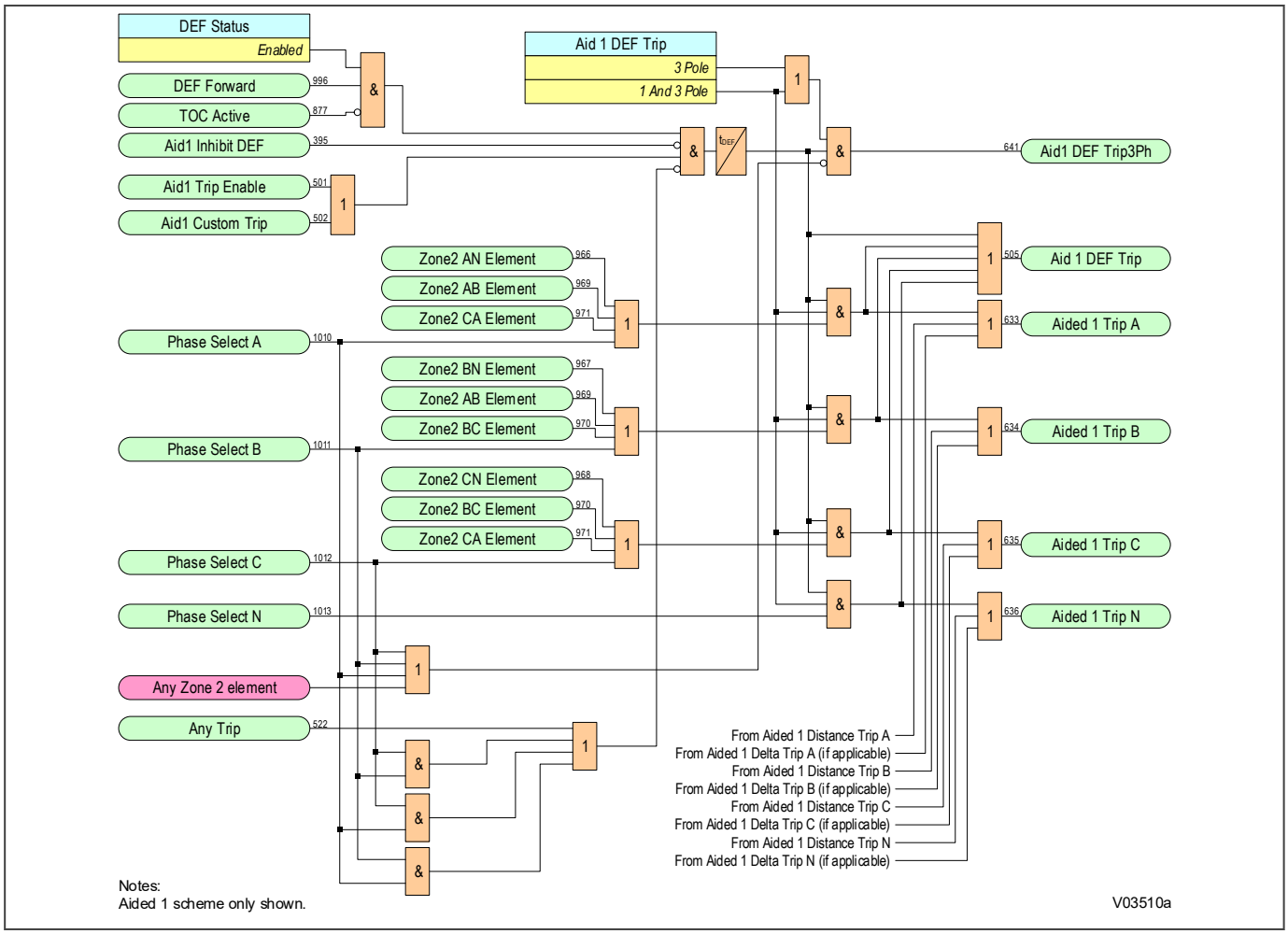


Figure 147: Aided DEF tripping logic

9.4.7.5 POR AIDED TRIPPING LOGIC

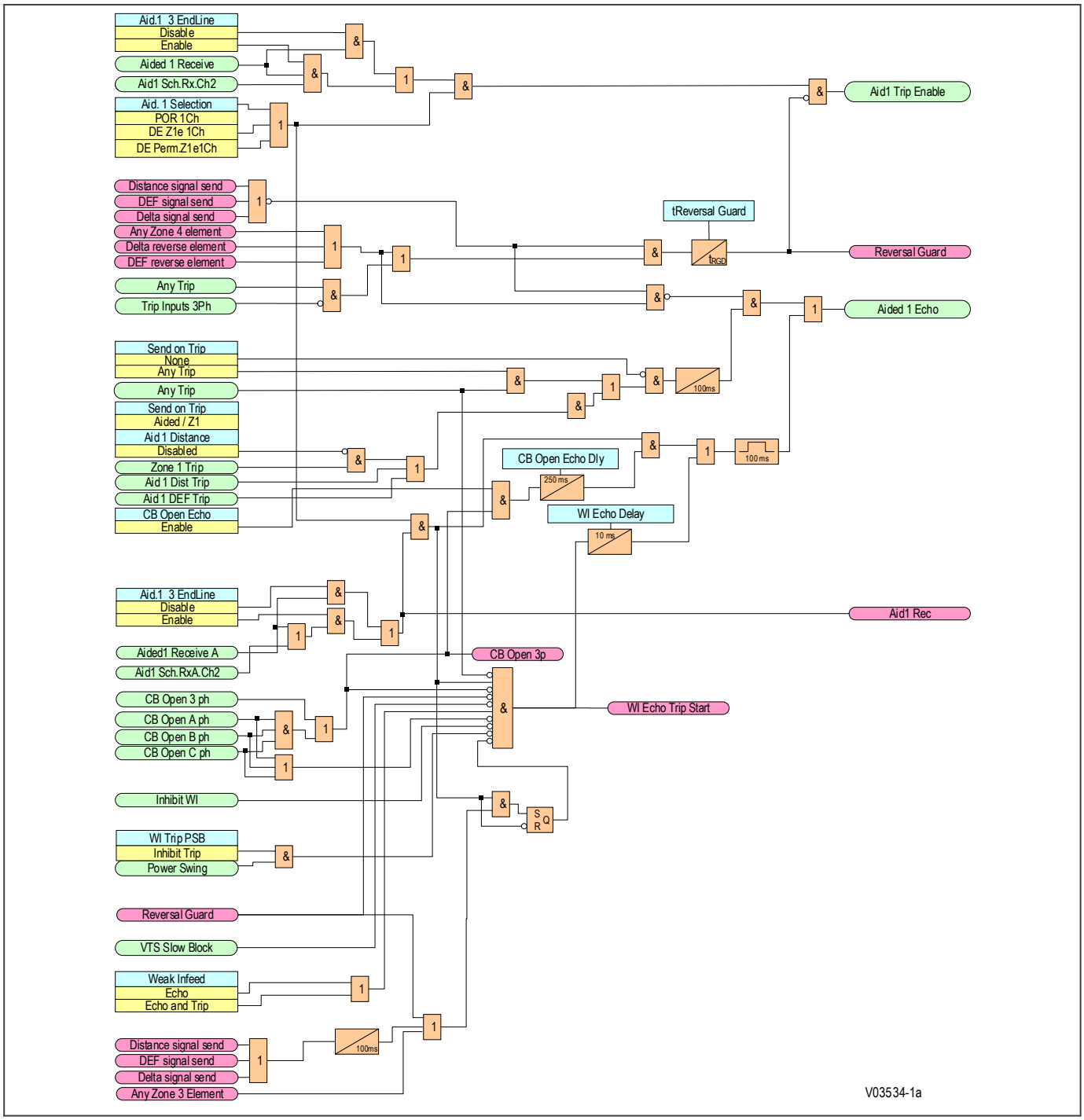


Figure 148: POR aided tripping logic 1Ch (1 of 2)

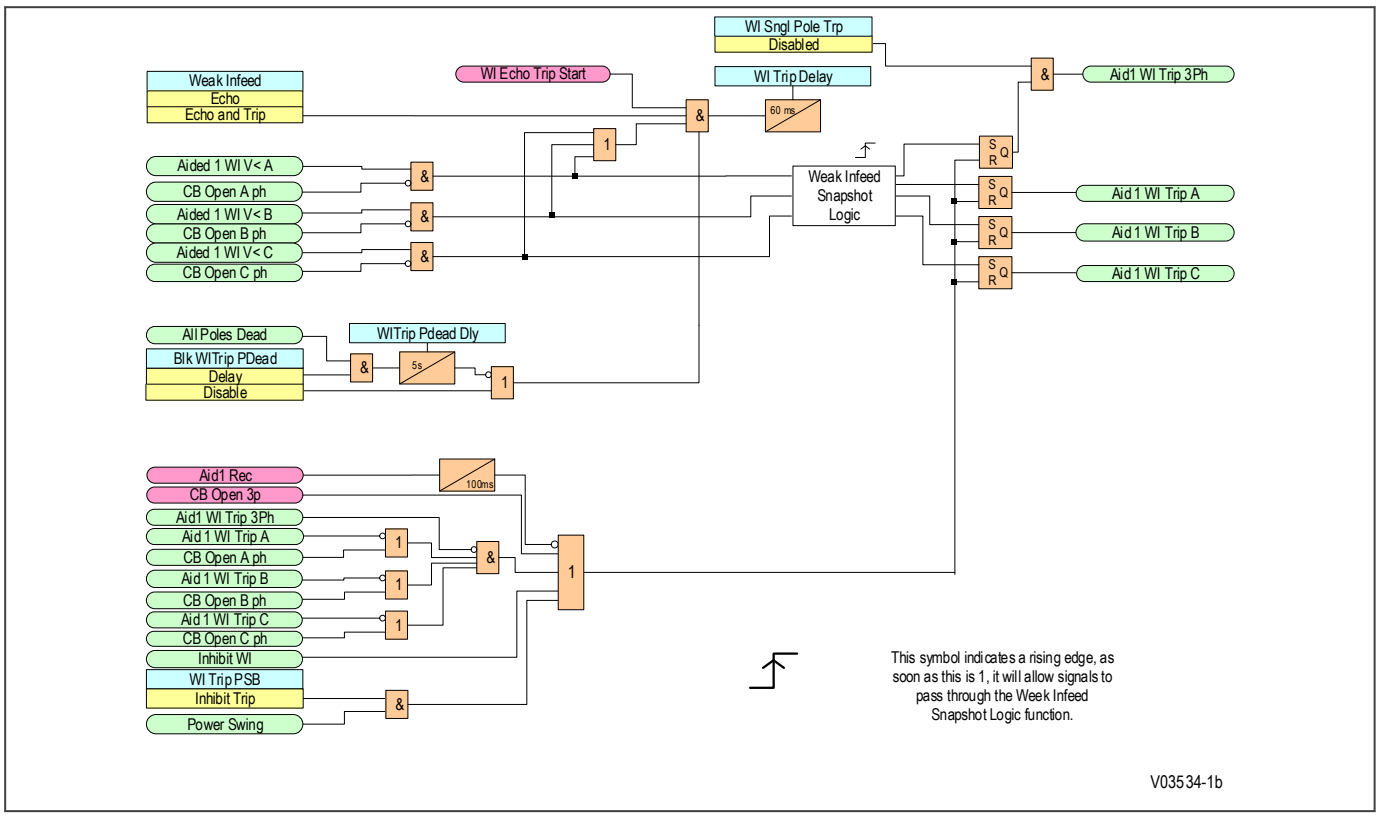


Figure 149: POR aided tripping logic 1Ch (2 of 2) - weak infeed trip

9.4.7.6 POR AIDED TRIPPING LOGIC

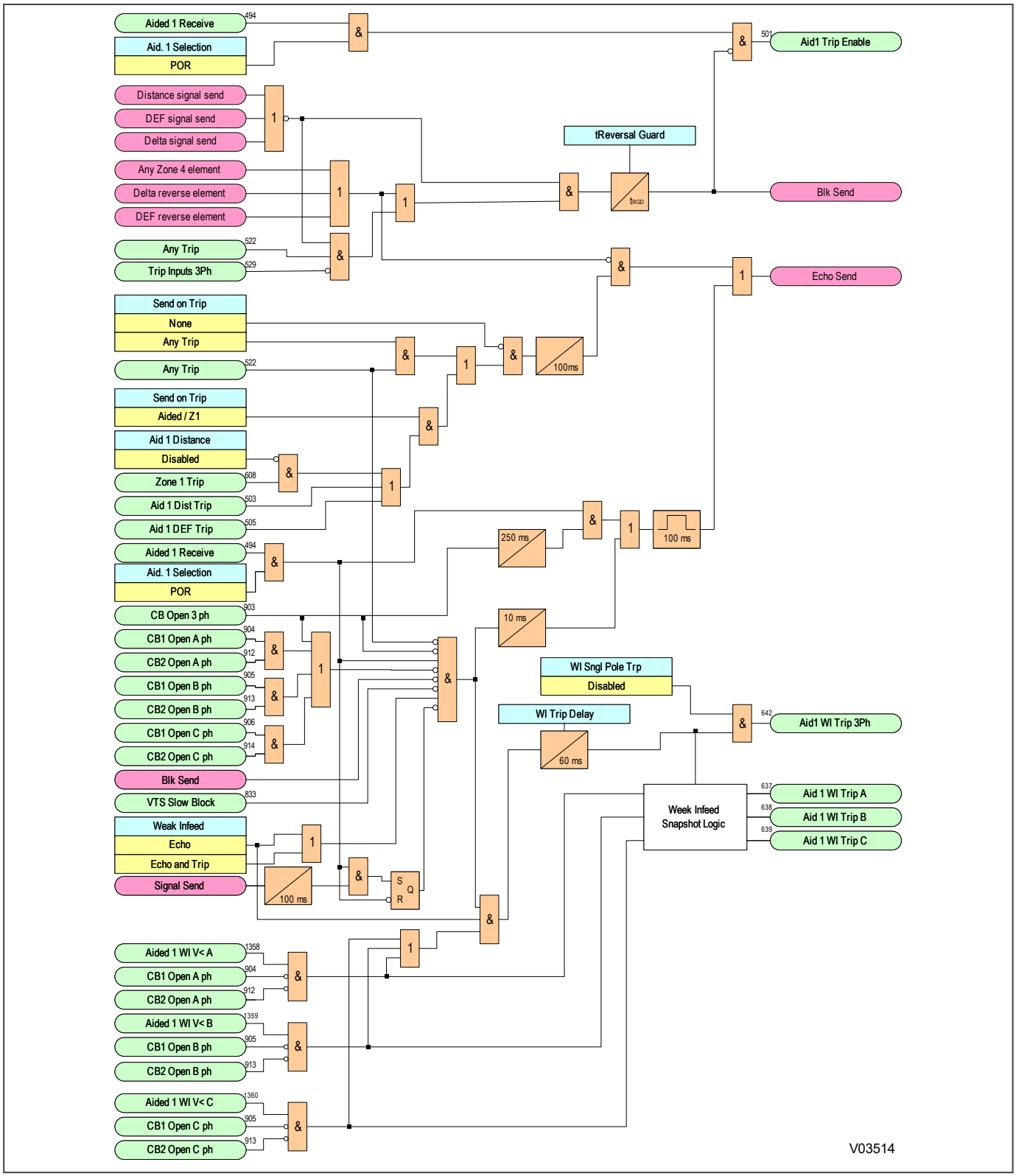


Figure 150: POR aided tripping logic

9.4.7.7 AIDED SCHEME BLOCKING 1 TRIPPING LOGIC

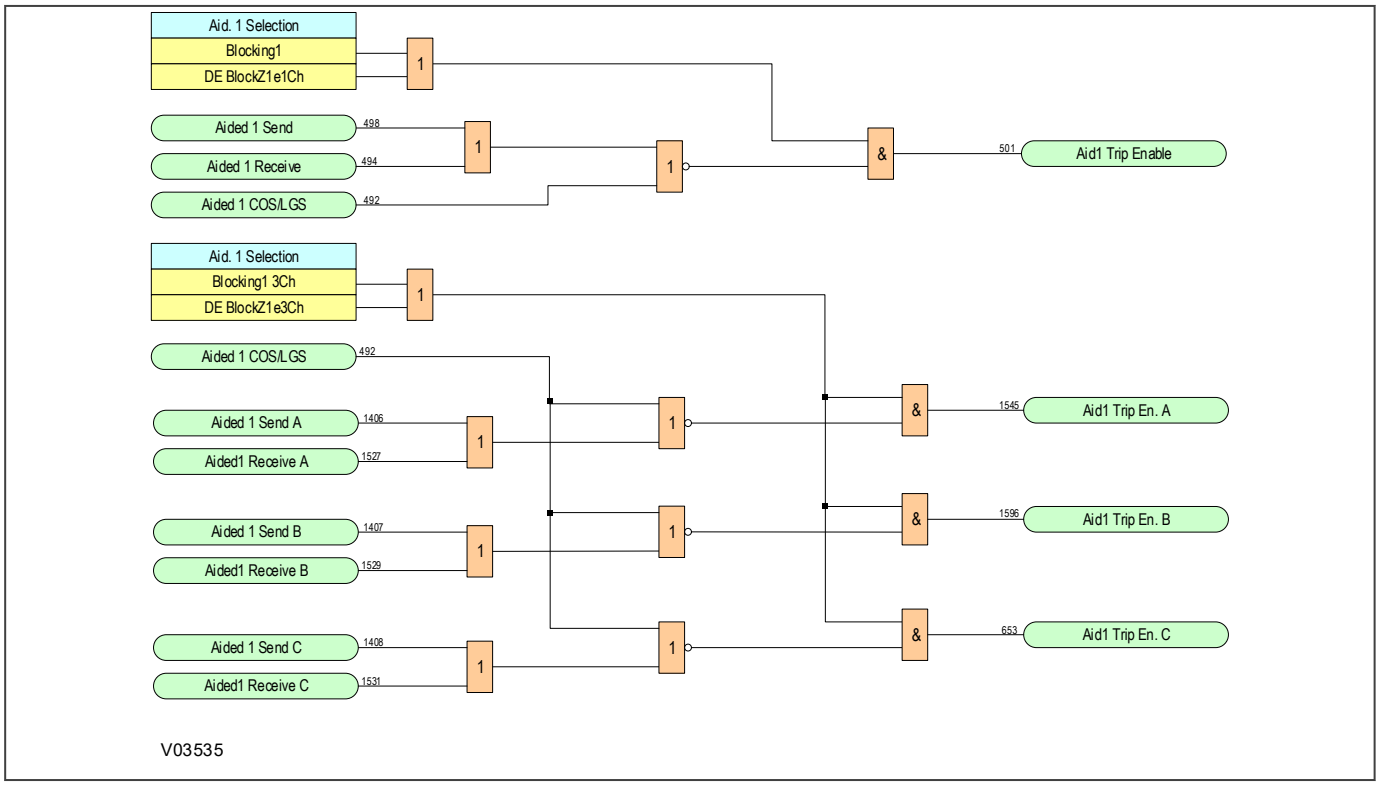


Figure 151: Aided scheme blocking 1 tripping logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.4.7.8 AIDED SCHEME BLOCKING 2 TRIPPING LOGIC

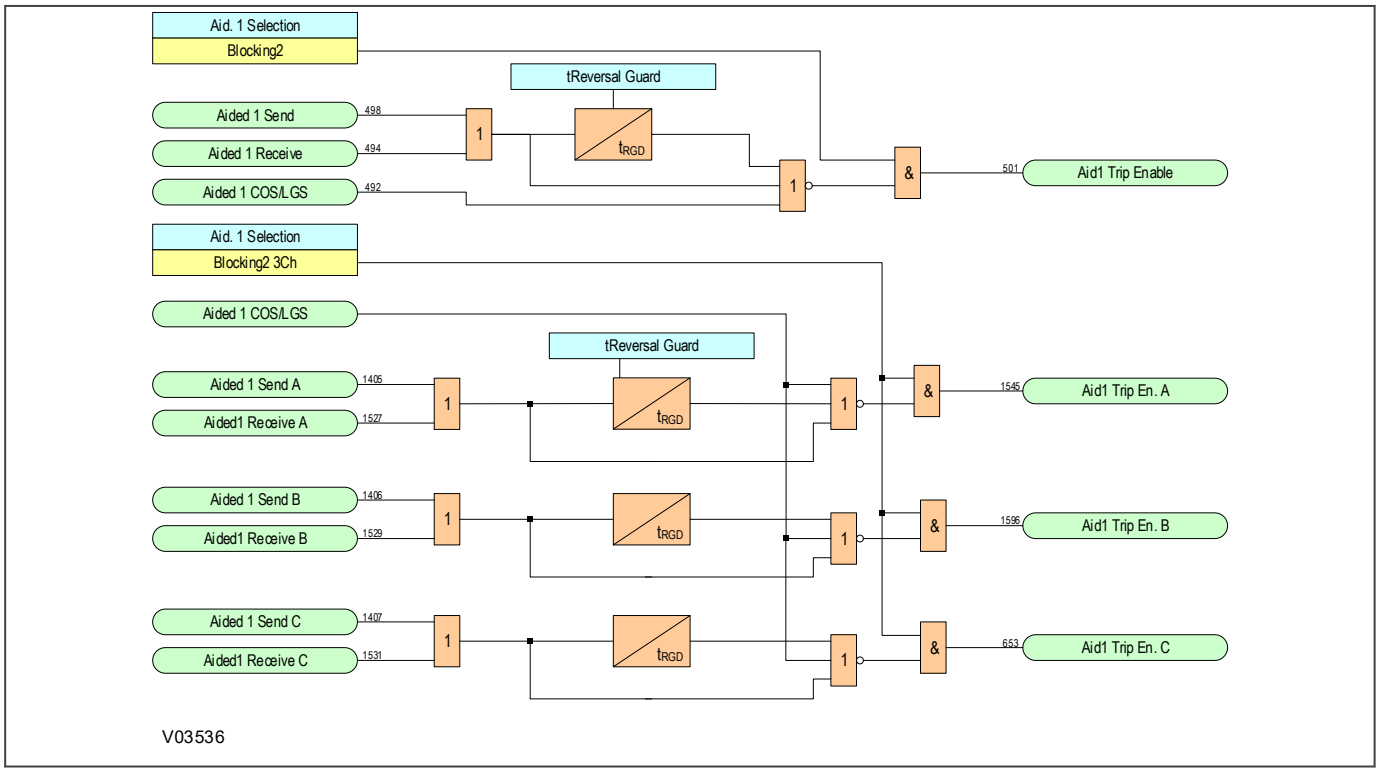


Figure 152: Aided scheme blocking 2 tripping logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.5 AIDED DELTA SCHEME LOGIC

If either a Permissive Overreaching scheme or a Blocking schemes is selected, it can be used to implement Directional Comparison(Aided Delta) protection.

Caution:
Aided Delta should not be used on a communications channel if that channel is being used to implement an Aided Distance Scheme or an Aided DEF scheme. You should ensure that the Aided Distance and Aided DEF elements are disabled if you want to apply the Aided Delta (Directional Comparison Protection).

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.5.1 AIDED DELTA POR SCHEME

The channel for an Aided Delta POR scheme is keyed by operation of the overreaching Delta Forward elements. If the remote device has also detected a forward fault upon receipt of this signal, the protection operates.

If the signalling channel fails, Basic distance scheme tripping is available.

The logic is:

- Send logic: Key channel if a Detla Fault Forward is detected
- Permissive trip logic: Trip if a Delta Fault Forward AND a keyed channel is received.

This scheme is shown in the figure below.

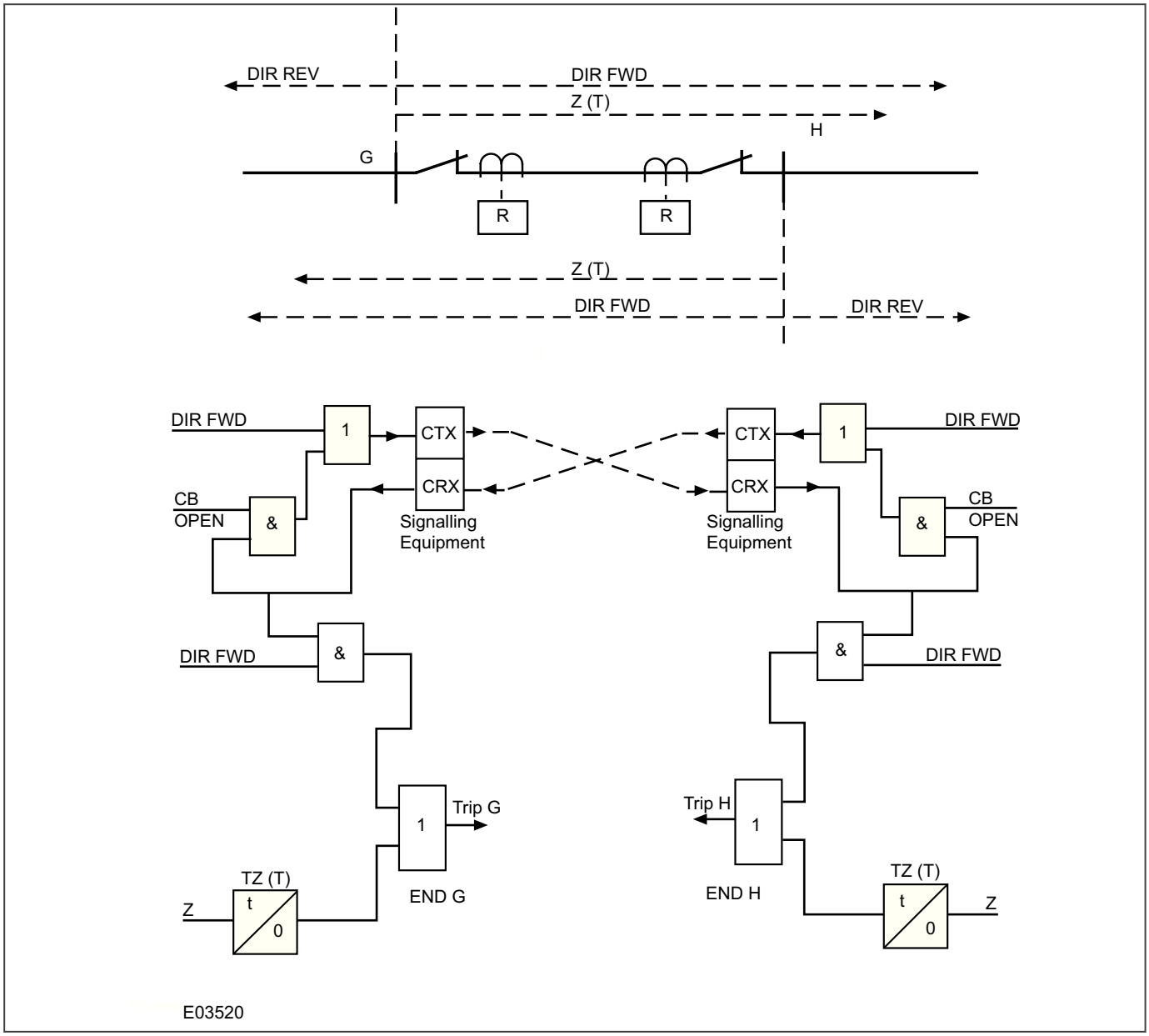


Figure 153: Aided delta POR scheme

9.5.2 AIDED DELTA BLOCKING SCHEME

The signalling channel is keyed from operation of the Delta Reverse elements. If the remote device has detected Delta Forward, it operates after the trip delay if no block is received.

The logic is:

- Send logic: Key channel if a Delta Fault Reverse condition is detected
- Trip logic: Trip if a Delta Fault Forward condition is detected, AND a keyed channel signal is NOT received, before the Aided Delta Delay timer expires.

This scheme is shown in the figure below.

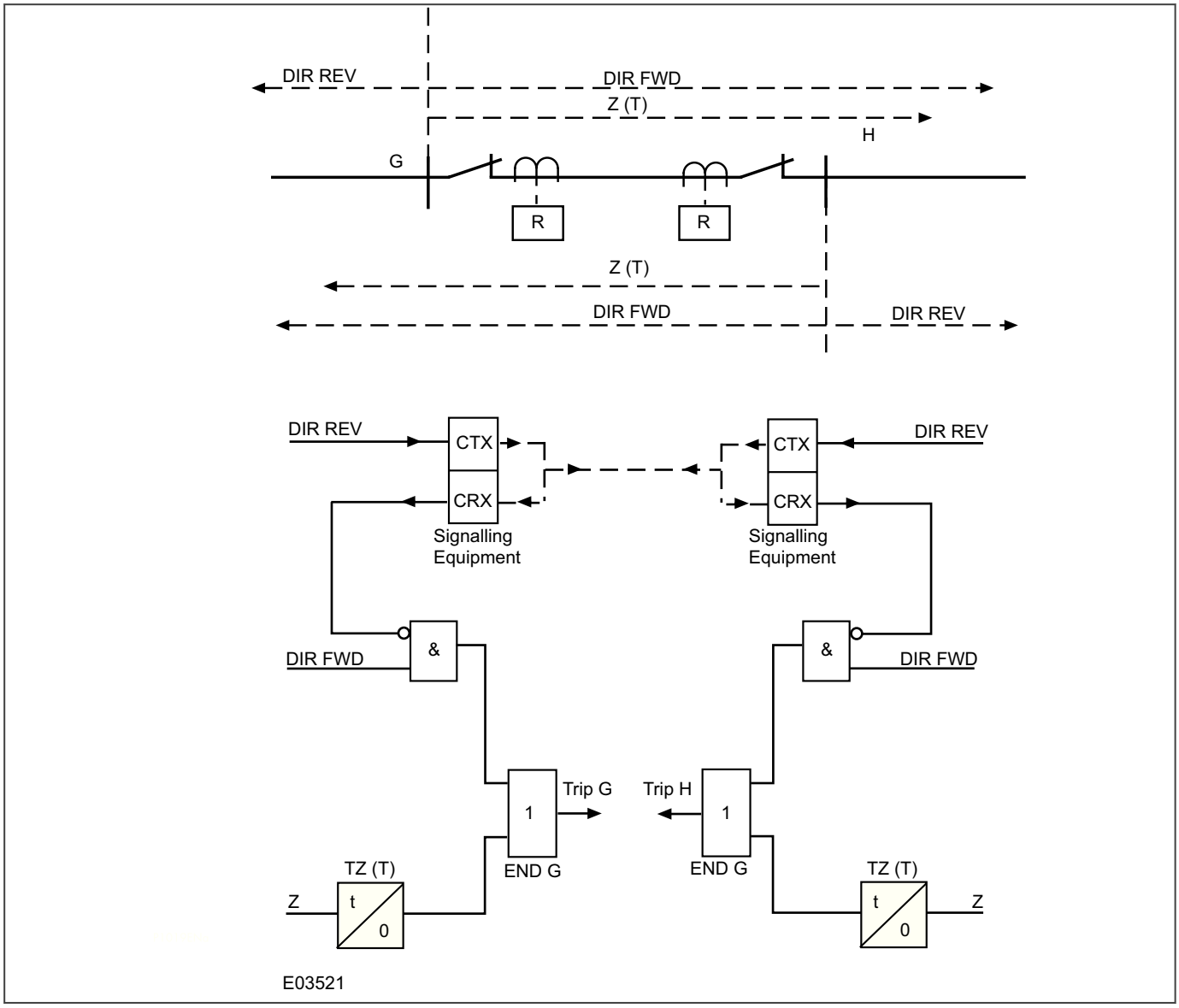


Figure 154: Aided delta blocking scheme

9.5.3 AIDED DELTA LOGIC DIAGRAMS

9.5.3.1 AIDED DELTA SEND LOGIC

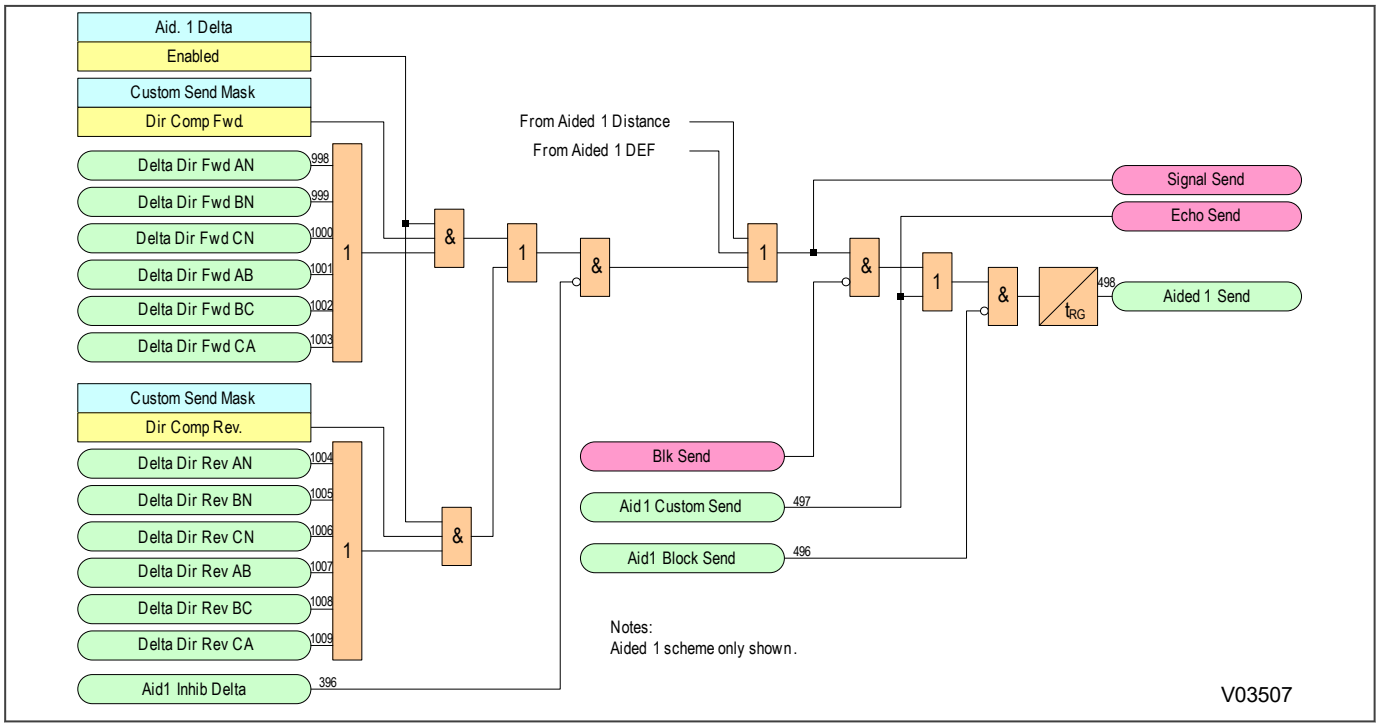


Figure 155: Aided delta send logic

9.5.3.2 CARRIER AIDED SCHEMES RECEIVE LOGIC

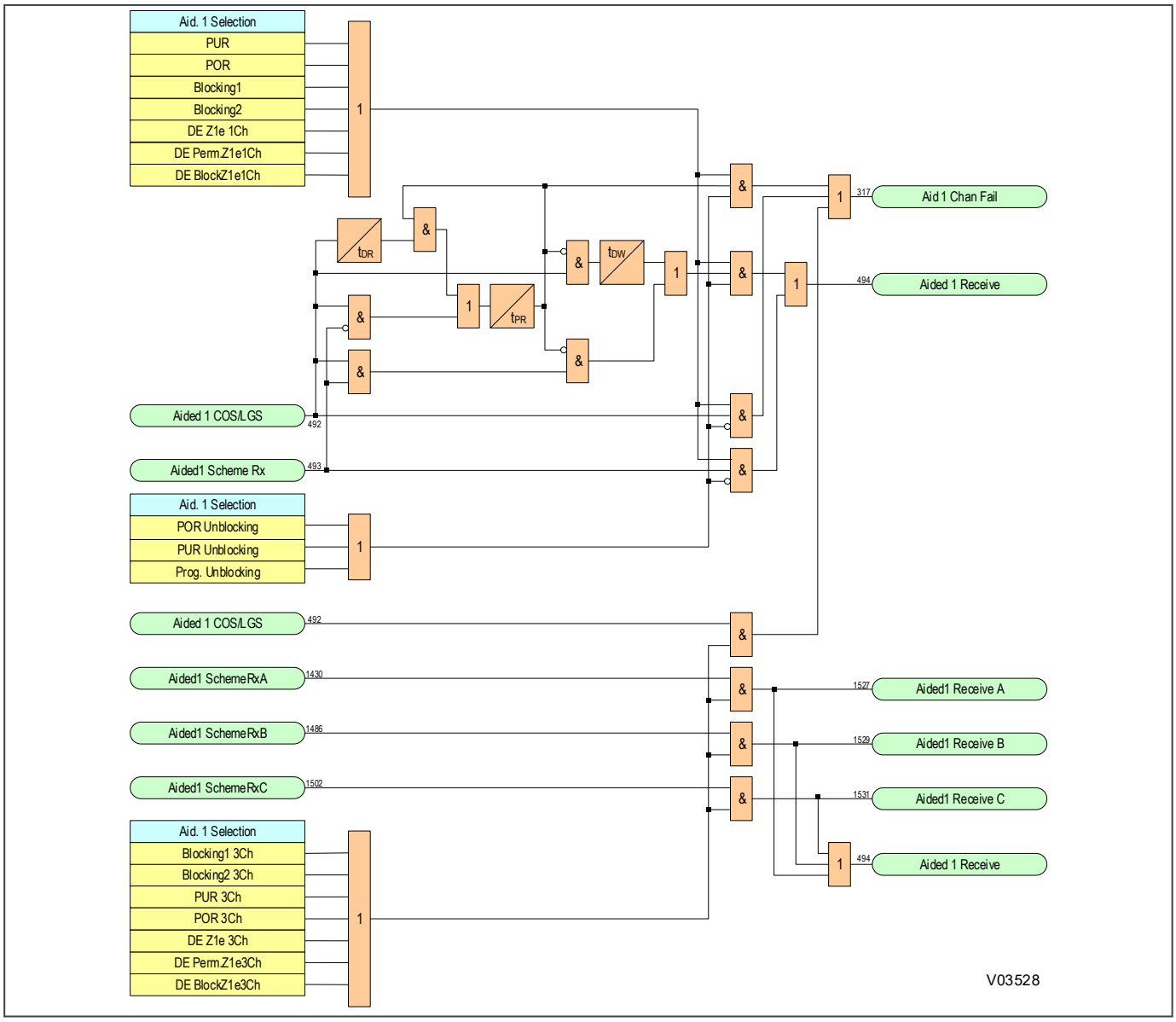


Figure 156: Carrier aided schemes receive logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.5.3.3 AIDED DELTA TRIPPING LOGIC

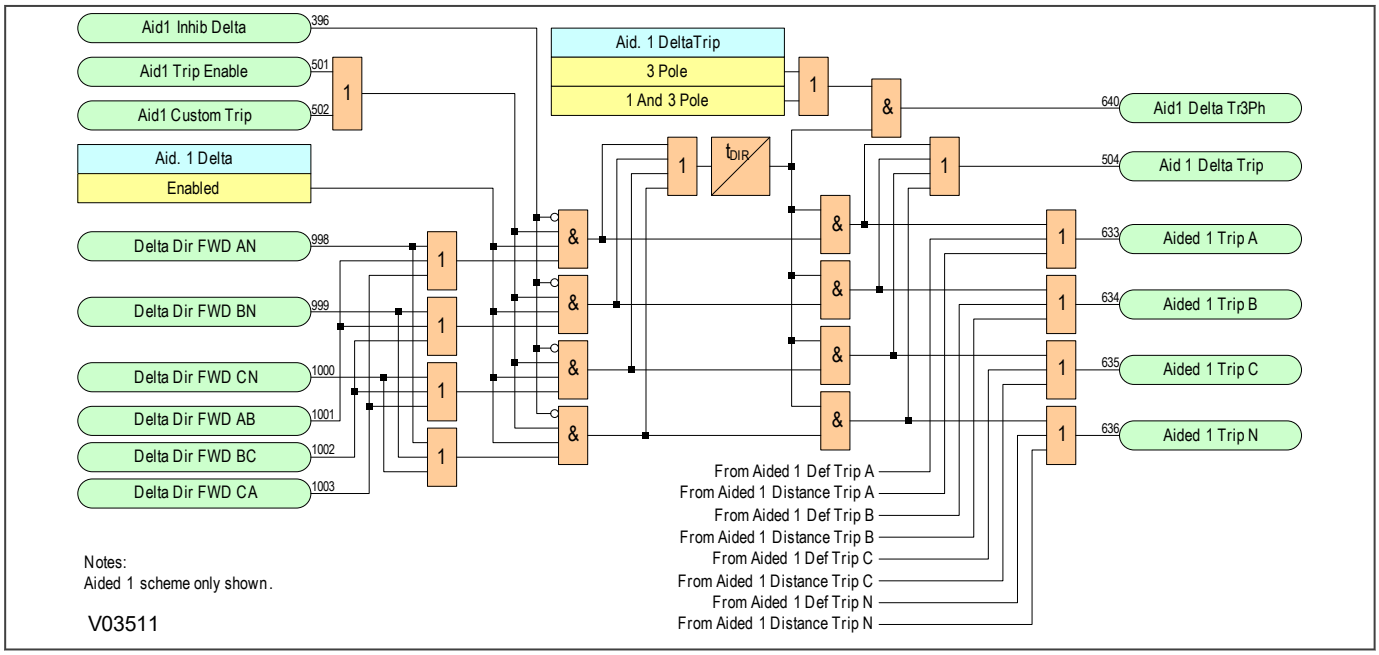


Figure 157: Aided delta tripping logic

9.5.3.4 POR AIDED TRIPPING LOGIC

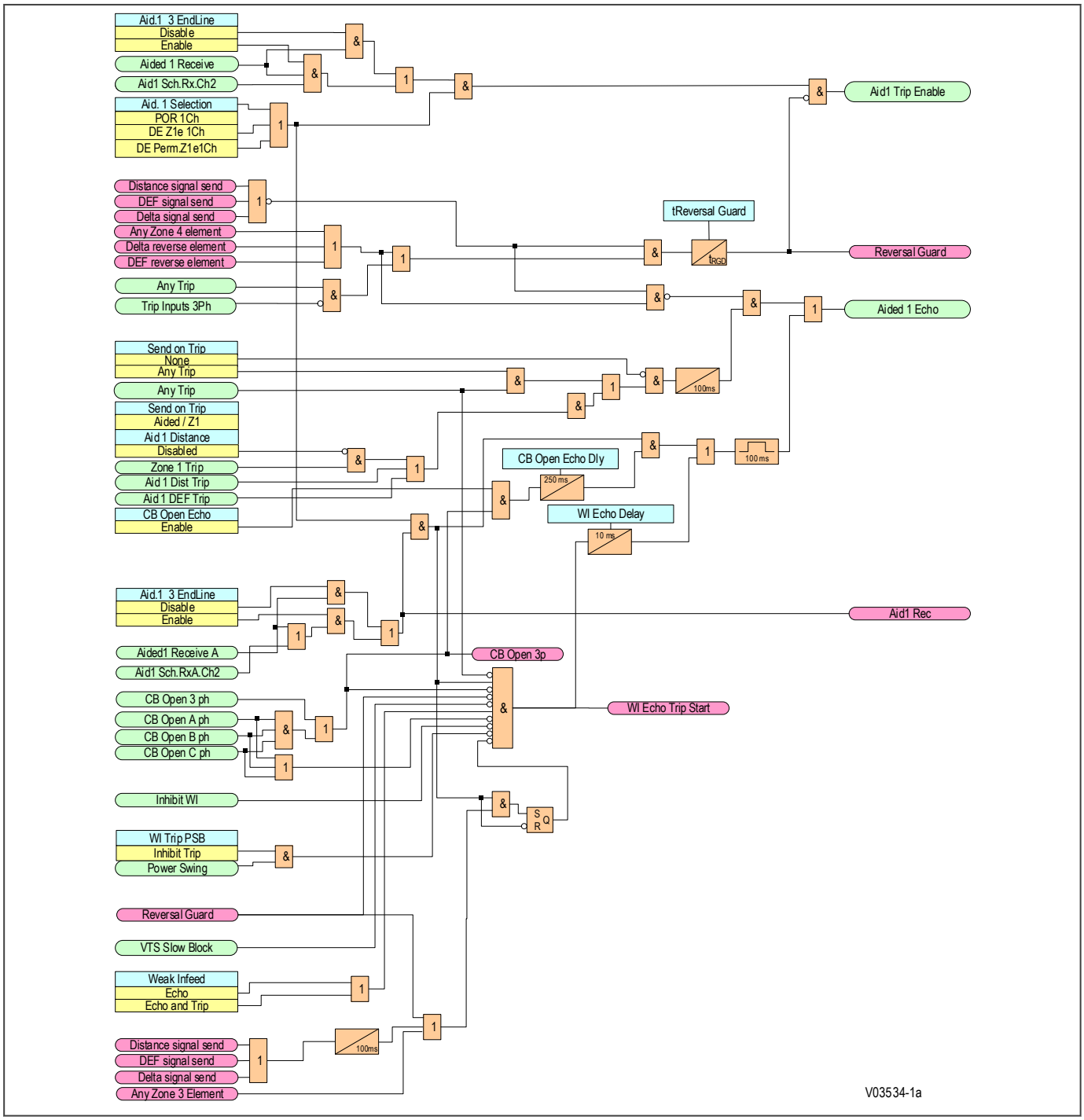


Figure 158: POR aided tripping logic 1Ch (1 of 2)

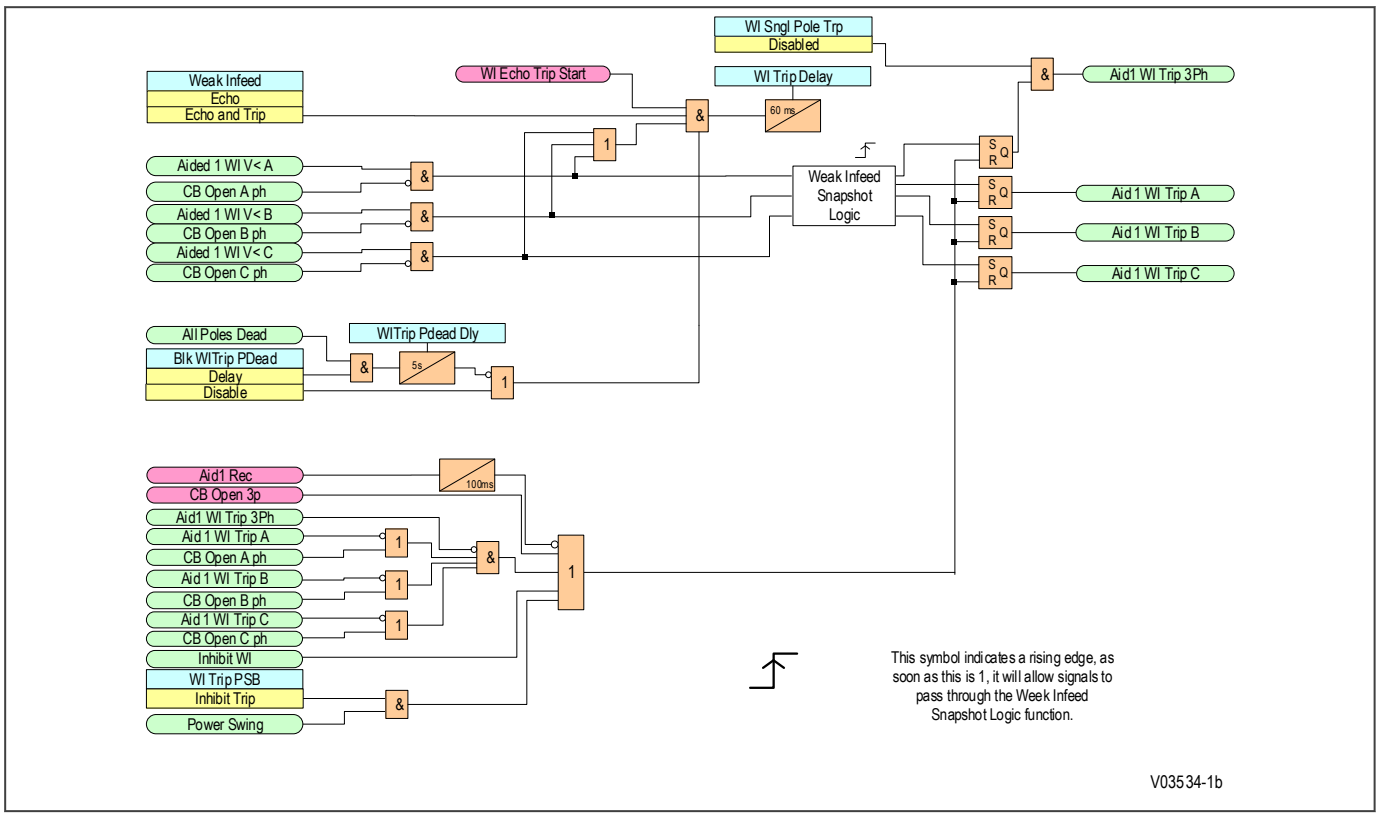


Figure 159: POR aided tripping logic 1Ch (2 of 2) - weak infeed trip

9.5.3.5 POR AIDED TRIPPING LOGIC

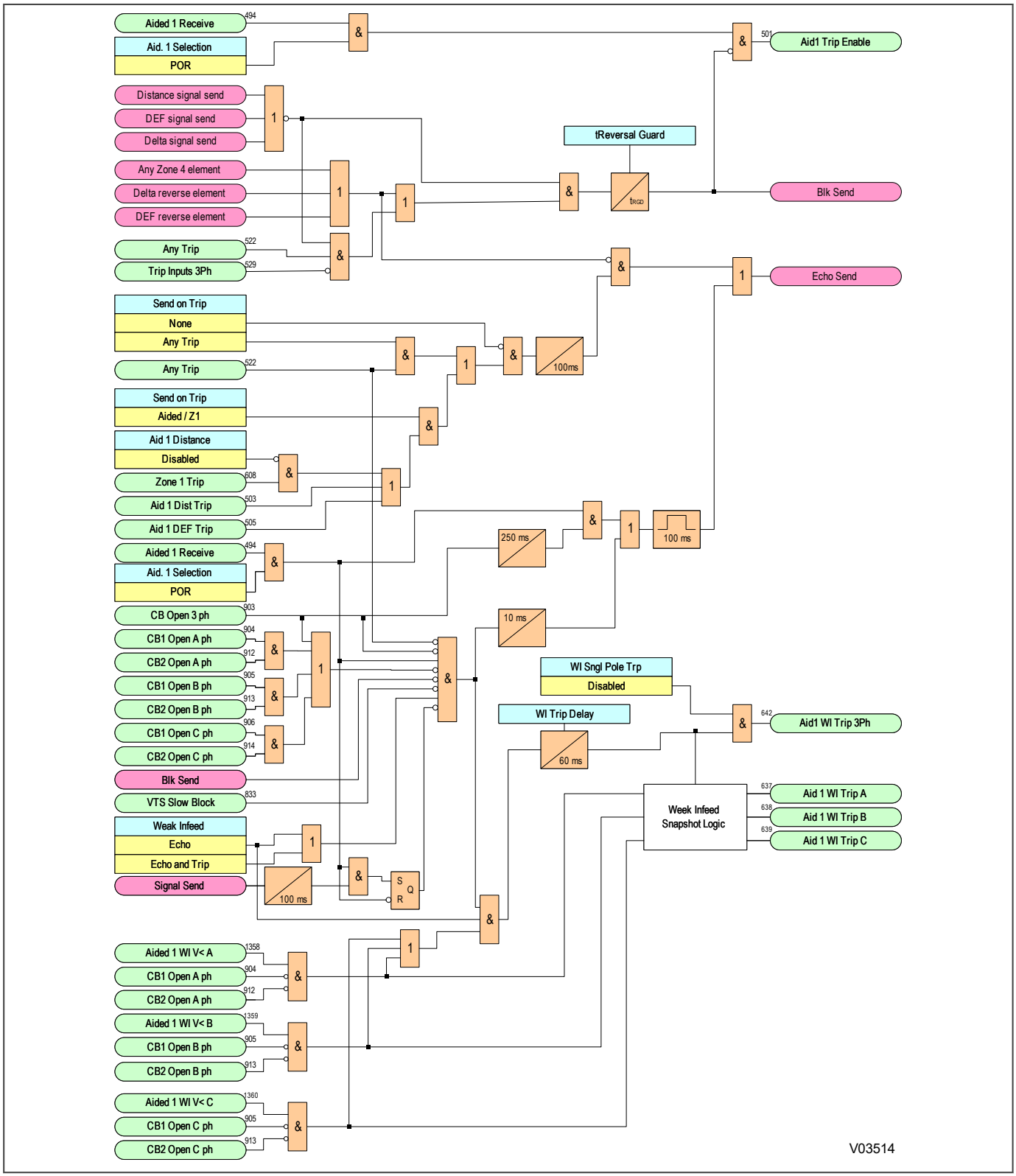


Figure 160: POR aided tripping logic

9.5.3.6 AIDED SCHEME BLOCKING 1 TRIPPING LOGIC

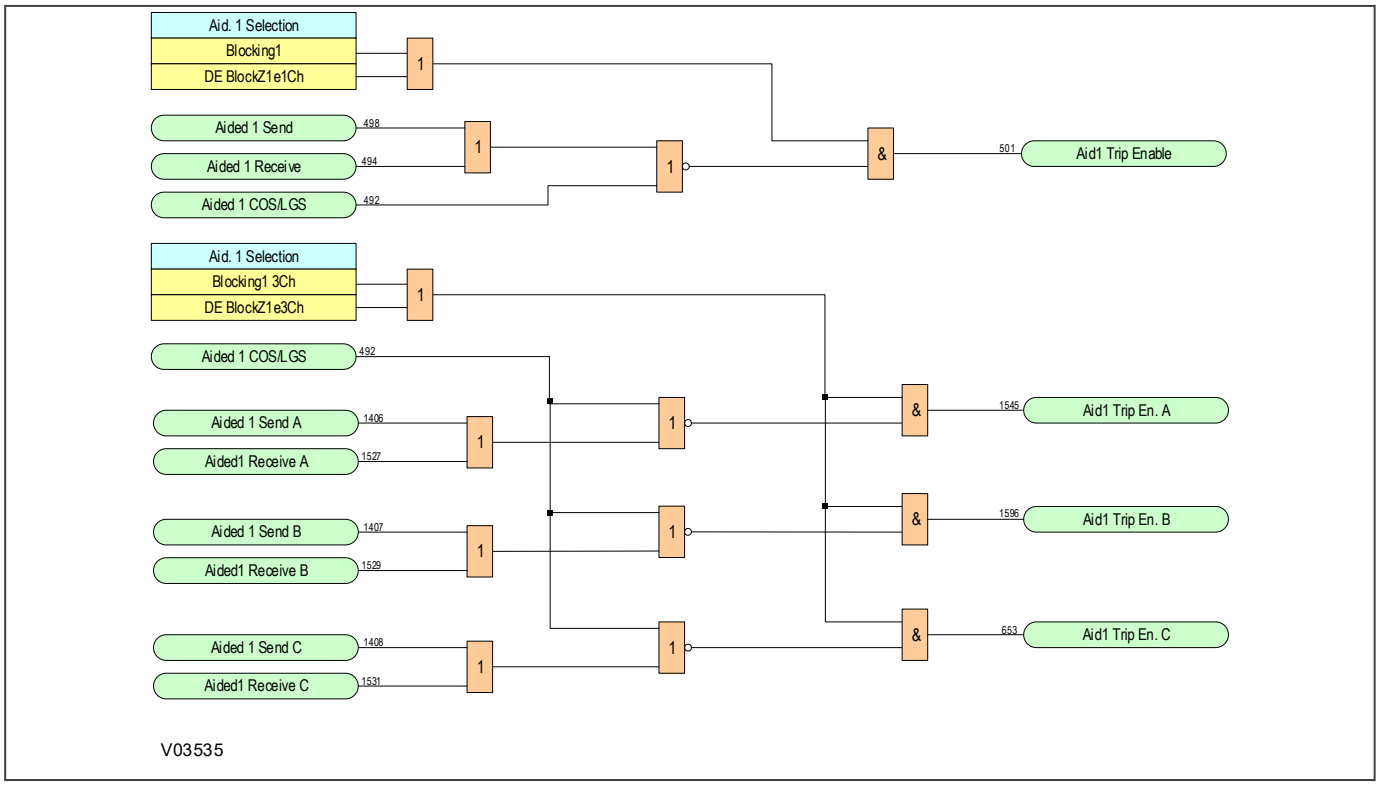


Figure 161: Aided scheme blocking 1 tripping logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.5.3.7 AIDED SCHEME BLOCKING 2 TRIPPING LOGIC

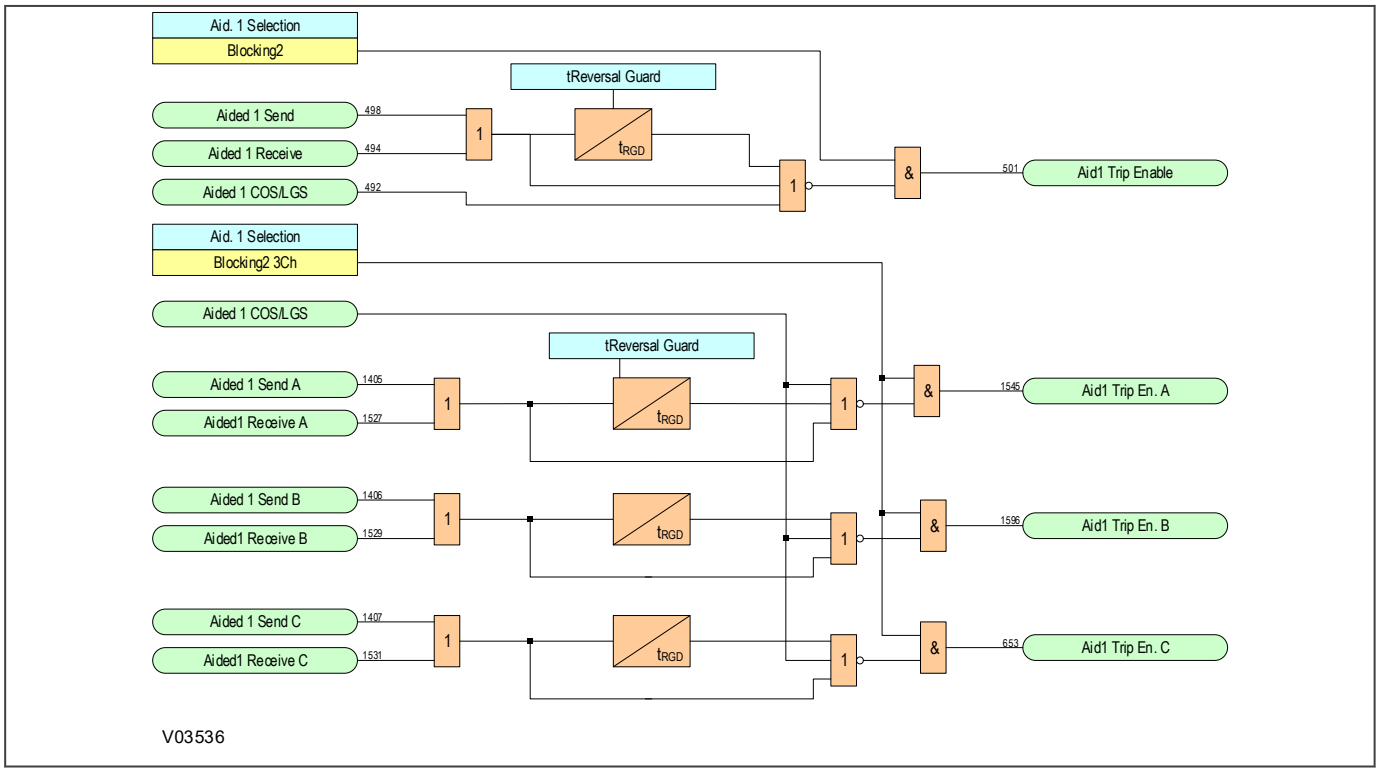


Figure 162: Aided scheme blocking 2 tripping logic

Note:
An Aided Distance scheme requires communication of the aided-carrier command signal(s) between line ends. Where phase-segregated carrier-aided Distance schemes are supported, three command signals must be communicated (one to supervise the tripping of each phase). Otherwise a single command transfer (universally applicable to all phases) is required.
An Aided Delta scheme requires a separate communication command channel to transmit a composite Delta Directional signal (universally applicable to all phases) between line ends.
An Aided DEF scheme requires a separate communication command channel to transmit the aided-carrier command signal (universally applicable to all phases) between line ends. If a three-pole-tripping carrier-aided Distance scheme is implemented (i.e NOT phase-segregated) then a single, common, aided carrier signal may be shared between similar carrier-aided Distance and DEF schemes.

9.6 DE TELEPROTECTION SCHEMES

The following teleprotection schemes are specific for DE:

- DE Zone 1 Extension Scheme 1 Ch (***DE Z1e 1Ch***) to work with a common channel send
- DE Zone 1 Extension Scheme 3 Ch (***DE Z1e 3h***) to work with a per phase channel send
- DE Permissive Zone 1 Extension Scheme 1 Ch (***DE Perm.Z1e1Ch***) to work with a common channel send
- DE Permissive Zone 1 Extension Scheme 3 Ch (***DE Perm.Z1e3Ch***) to work with a per phase channel send
- DE Blocking Scheme for 1 Ch. Setting ***DE BlockZ1e1Ch*** to work with a common channel send
- DE Blocking Scheme for 3 Ch. Setting ***DE BlockZ1e3Ch*** to work with a per phase channel send

These schemes only exist within *AIDED SCHEME 1*.

These schemes work with zone “Z1e” . This zone is completely independent of *ZONE 1 EXTENSION* (Z1x) under the *AIDED SCHEME 1*. This Z1e is an independent standalone zone which can be set and behaves like the other zones in the relay. DE schemes use zone Z1e to key the permissive channel and allow the permissive or unblocking trip.

This Z1e zone can be set Forward or Reverse. Please note, if it is going to be used for the DE schemes, it must be set as forward for either keying or permitting the teleprotection scheme.

If any of these schemes are selected, it is possible to initiate or block the Autoreclose . Please refer to setting GROUP x *AUTORECLOSE* ***Dist Aided AR\Initiate AR*** or ***Block AR***.

9.6.1 DE SCHEME DESCRIPTION

Zone 1 extension scheme 1 Ch (*DE Z1e 1Ch*) and Zone 1 extension scheme 3 Ch (*DE Z1e 3Ch*)

These schemes use the existing scheme logic as per POR 1Ch and POR 3Ch, but sending and receiving zones are as follows:

Send logic: Zone 1

Permissive Trip Logic: Z1e AND Channel receive (done in a per phase basis for ***DE Z1e 3Ch***)

The scheme will trip after the existing time delay ***Aid.1 Dist. Dly*** has elapsed.

Permissive Zone 1 extension scheme 1 Ch (*DE Perm.Z1e1Ch*) and permissive zone 1 extension scheme 3 Ch (*DE Perm.Z1e3Ch*)

These schemes use the existing scheme logic as per POR 1Ch and POR 3Ch, but sending and receiving zones are as follows:

Send logic: Z1e

Permissive Trip Logic: Z1e AND Channel receive (done in a per phase basis for ***DE Perm.Z1e3Ch***)

The scheme will trip after the existing time delay ***Aid.1 Dist. Dly*** has elapsed.

Blocking scheme for 1Ch *DE BlockZ1e1Ch* and blocking scheme for 3Ch *DE BlockZ1e3Ch*

These schemes use the existing scheme logic as per Blocking Scheme 1 Blocking1 1Ch and Blocking1 3Ch, but sending and receiving zones are as follows:

Block Send logic: Zone 4

Trip Logic: Z1e AND No Channel receive (in a per phase basis for ***DE BlockZ1e3Ch***)

The scheme will trip after the existing time delay ***Aid.1 Dist. Dly*** has elapsed. In this case, for tripping, enough time must be allowed for the remote relay signal to pick-up and for channel delay.

Note:
When a scheme is used as 3Ch, Aided DEF or Aided Delta cannot be used.

9.7 APPLICATION NOTES

9.7.1 AIDED DISTANCE PUR SCHEME

This scheme allows an instantaneous Zone 2 trip on receipt of the signal from the underreaching element of the remote end protection.

The logic is:

- Send logic: Zone 1
- Permissive Trip logic: Zone 2 plus channel received

The time delay setting (***Aid.1 Dist. Dly***, ***Aid.2 Dist. Dly***) should be set to 0 ms for fast fault clearance.

9.7.2 AIDED DISTANCE POR SCHEME

This scheme allows This scheme allows an instantaneous Zone 2 trip on receipt of the signal from the overreaching element of the remote end protection.

The logic is

- Send logic: Zone 2
- Permissive Trip logic: Zone 2 plus channel received

The time delay setting (***Aid.1 Dist. Dly***, ***Aid.2 Dist. Dly***) should be set to 0 ms for fast fault clearance.

The POR scheme also uses the reverse looking zone 4 IED as a reverse fault detector. This is used in the current reversal logic and in the optional weak infeed echo feature.

Weak infeed

Where weak infeed tripping is employed, a typical voltage setting is 70% of rated phase-neutral voltage. Weak infeed tripping is time delayed according to the ***WI Trip Delay*** value, usually set at 60ms.

Current reversal guard

The recommended setting is:

- ***tReversal Guard*** = Maximum signalling channel reset time + 60 ms.

9.7.3 AIDED DISTANCE BLOCKING SCHEME

This scheme uses a reverse looking zone 4 element to block operation of a forward looking zone 2 element at the remote end protection.

The logic is:

- Send logic: Reverse Zone 4
- Trip logic: Zone 2, plus Channel NOT Received

To allow time for a blocking signal to arrive, a short time delay must be allowed before tripping (***Aid.1 Dist. Dly***, ***Aid. 2 Dist. Dly***). The recommended delay is as follows:

- Recommended setting = Maximum signalling channel operating time + one power frequency cycle.

Note:
Two variants of a Blocking scheme are provided, Blocking 1 and Blocking 2. Both schemes operate similarly, except that the reversal guard timer location in the logic changes. Blocking 2 may sometimes allow faster unblocking when a fault evolves from external to internal, and hence a faster trip.

Current reversal guard

The recommended settings are as follows:

- Where Duplex signalling channels are used: Set ***tReversal Guard*** to the maximum signalling channel operating time + 20ms.
- Where Simplex signalling channel is used: Set ***tReversal Guard*** to the combination of the maximum signalling channel operating time, minus the minimum signalling channel reset time, and add 20ms.

9.7.4 AIDED DEF POR SCHEME

This scheme allows an instantaneous DEF trip of a local terminal if it sees a forward fault AND it receives a signal from the remote end protection indicating that it is too has seen a forward fault.

The logic is:

- Send logic: DEF forward
- Permissive Trip logic: DEF forward plus channel received

The time delay would normally be set to 0 ms.

9.7.5 AIDED DEF BLOCKING SCHEME

This scheme prevents DEF tripping of a local terminal if it receives a signal from the remote end protection indicating that the fault is in the reverse direction, and hence out of zone.

The logic is:

- Send logic: DEF reverse
- Trip logic: DEF forward plus channel NOT received, with a small set delay

To allow time for a blocking signal to arrive, a short time delay on aided tripping must be used. The recommended delay time setting (***Aid. 1 DEF Dly.***, ***Aid. 2 DEF Dly.***) is the maximum signalling channel operating time +20 ms.

9.7.6 AIDED DELTA POR SCHEME

This scheme allows an instantaneous Delta trip of a local terminal if it sees a forward fault AND it receives a signal from the remote end protection indicating that it is too has seen a forward fault.

- Send logic: Delta fault Forward
- Permissive Trip logic: Delta fault Forward plus channel received

The time delay (***Aid. 1 Delta Dly***, ***Aid. 2 Delta Dly***) should be set to 0 ms for fast fault clearance.

Current reversal guard

Current reversals during fault clearances on adjacent parallel lines need to be treated with care.To prevent maloperation, a current reversal guard timer must be set.

The recommended setting (***tReversal Guard***) is the maximum signalling channel reset time + 35 ms.

9.7.7 AIDED DELTA BLOCKING SCHEME

This scheme prevents Delta tripping of a local terminal if it receives a signal from the remote end protection indicating that the fault is in the reverse direction, and hence out of zone.

- Send logic: Delta fault reverse
- Trip logic: Delta fault forward plus channel NOT received, delayed by Tp (a short time delay)

Recommended delay setting (***Aid. 1 Delta Dly***, ***Aid. 2 Delta Dly***): Maximum signalling channel operating time + 6ms.

Current reversal guard

Current reversals during fault clearances on adjacent parallel lines need to be treated with care.To prevent maloperation, a current reversal guard timer must be set.

The recommended setting (***tReversal Guard***) is the maximum signalling channel reset time + 35 ms.

9.7.8 TEED FEEDER APPLICATIONS

Distance protection can be applied to protect three terminal lines (teed feeders). Interconnecting three terminals, however, affects the apparent impedances seen by the distance elements and creates certain problems.

Consider, as an example, the following figure which represents a teed feeder with terminals A, B, and C, with a fault applied near to terminal B:

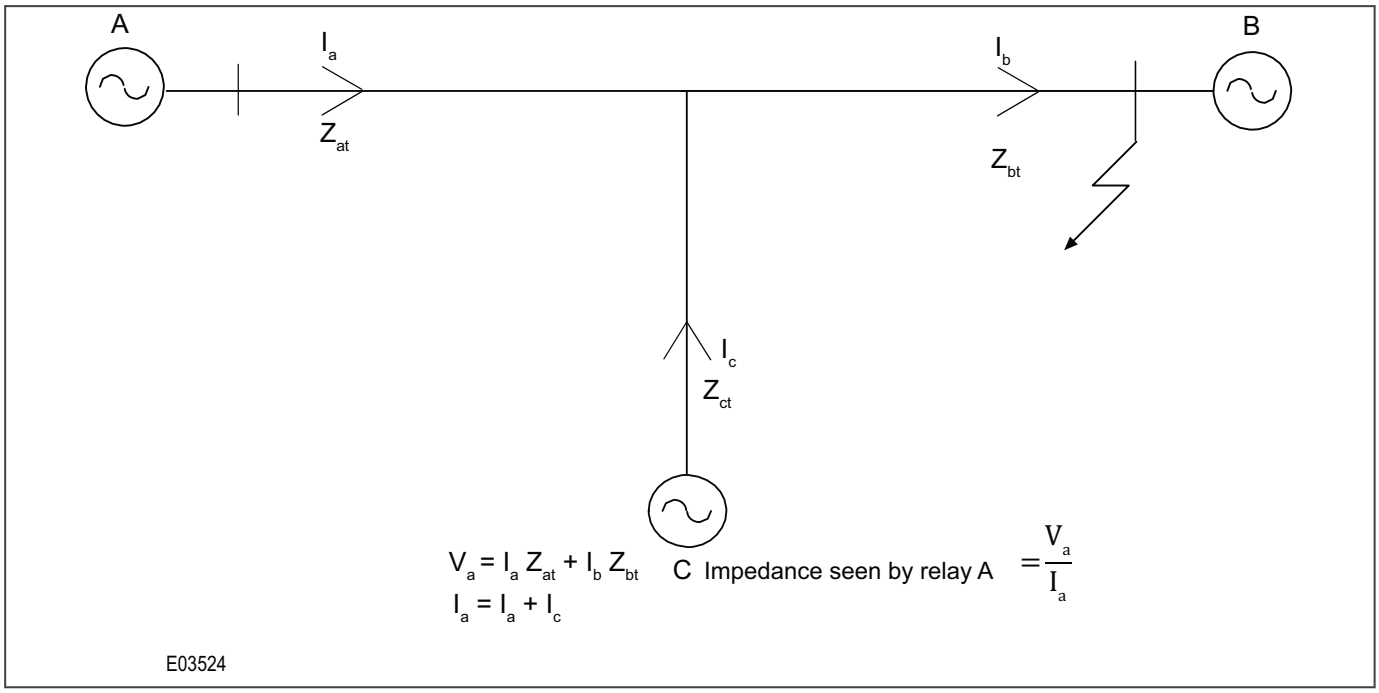


Figure 163: Apparent impedances seen by distance protection on a teed feeder

The impedance seen by the distance elements at terminal A is given by:

$$Za = Zat + Zbt + [Zbt.(Ic/Ia)]$$

For faults beyond the Tee point, with infeed from terminals A and C, the distance elements at A (and C) will underreach. If terminal C is a relatively strong source, the underreaching effect at A can be substantial. If Zone 2 was set to a typical value of 120% of line AB, the element may fail to operate for internal faults. To compensate, the Zone 2 element must be set to further overreach by a factor which takes into account the effect of the infeed from the tee-point.

So, if infeed is present on a teed circuit, all Zone 2 elements should be set to overreach both of their remote terminals by a factor which takes into account the effect of the infeed from the tee-point.

Like overreaching of Zone 2 elements, underreaching of Zone 1 elements must also be assured. Zone 1 elements at each terminal must be set to underreach the true impedance to their nearest terminal (limiting case = no infeed to the tee-point - hence no overreach contribution).

Changing the reach requirements to match the infeed expectations is possible using the alternative setting group feature. Tailoring setting group contents to the different conditions, coupled with appropriate setting group switching, enables the changing reach requirements to be met.

Carrier aided schemes can also be used in conjunction with distance elements to protect teed feeders. Although Permissive Overreaching and Permissive Underreaching schemes may be used, they suffer some limitations. Blocking schemes are generally considered to be the most suitable.

9.7.8.1 POR SCHEMES FOR TEED FEEDERS

A Permissive Overreach (POR) scheme requires the use of two signalling channels between each pair of terminals. On a teed feeder, a permissive trip is issued only if local Zone 2 operation (or Aided Z1 in case of DE schemes) is accompanied by receipt of signals from both remote terminals. The 'AND' function of received signals can either be implemented using external logic, or within the internal Programmable Scheme Logic (PSL).

Alternatively, using the ***Aid. 1 3 EndLine*** setting in the *AIDED SCHEME 1* column, the relay will:

- Include an AND gate with the two input receive signals ***Aided 1 Receive*** and ***Aid Ch.Rx.Ch2*** for Aided tripping and Weak Infeed Trip
- Include an OR gate with the two input receive signals ***Aided 1 Receive*** and ***Aid Ch.Rx.Ch2*** for Echo purposes

This is intended for use in the following scenario. Consider the three-ended scheme in the figure below. With a STRONG End A and weaker Ends B and C, relays at End B and C are set with Echo (not weak infeed trip). In this case, we can assume Zone 2 at End A can see all faults up to the busbar Ends B and C.

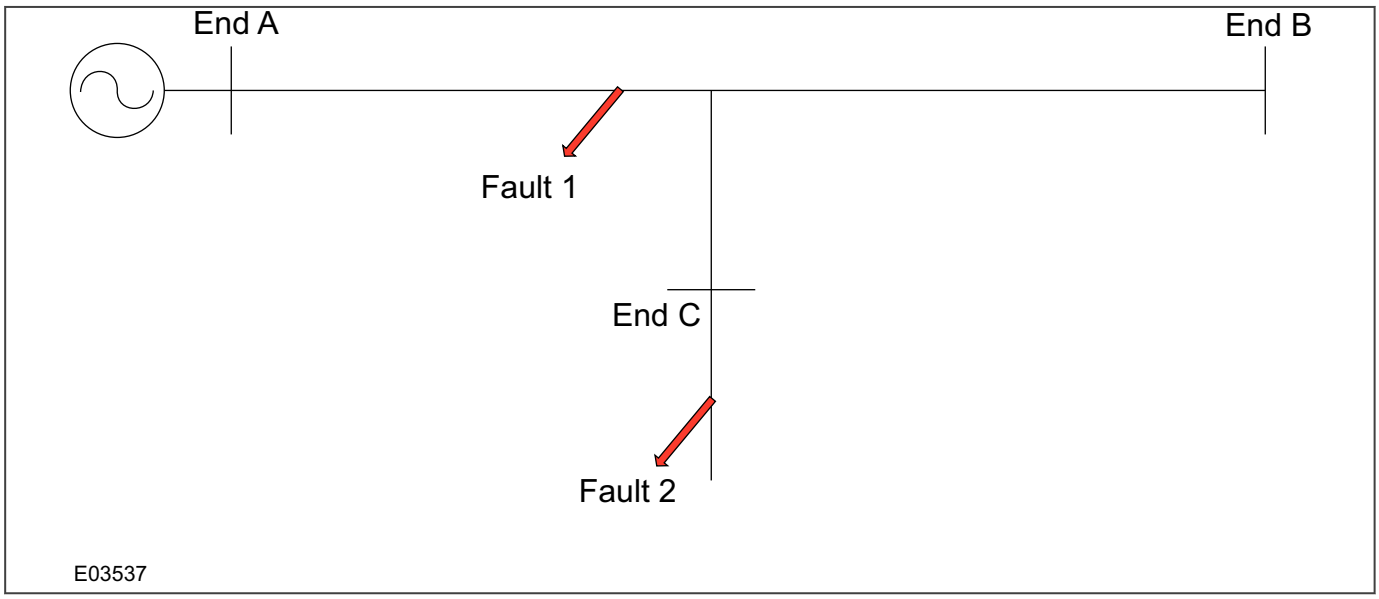


Figure 164: POR tee feeder fault example

For Fault 1

- End A: Sees the fault in Zone 2 and sends a signal to End C and B.
- End B Echo send: Does not see the fault and, because it is an OR from both signals receive, it will send a signal back to A and C. It will not trip because it is only an Echo
- End C Echo send: Does not see the fault at all and because is an OR from both signals receive, it will send a signal back to A and B . It will not trip because it is only set as an Echo
- End A: Will trip as the permissive is an AND from receive signals from End B and C fault and sees the fault in Zone 2

End B and C can also be set as a Weak Infeed Trip and as long as these relays receive a signal from both remote ends, and conditions are met (voltage below setting ***WI V<Thresh***., No CB open, No Distance, etc.), the relay will trip with Weak Infeed.

For Fault 2

- End A: Sees the fault in Zone 2 and sends a signal to End C and B.
- End B Echo send: Does not see the fault and, because is an OR from both Signals receive, it will send a signal back to A and C. It will not trip because it is only set as an Echo
- End C Echo send: It will see the fault in the reverse direction and therefore will not send the echo and will not trip.
- End A: Will not trip, as the permissive trip is an AND from both Signals receive from End B and C fault and in this case NO signal has been received from End C

To ensure operation for internal faults in a POR scheme, the protection at each of the three terminals should be able to see a fault anywhere on the protected feeder. This may demand very large Zone 2 reach settings to address the apparent impedances seen by the Distance elements.

Although POR schemes are feasible for teed feeders, the signalling requirements and the very large Zone 2 settings can make its use unattractive.

If Zone 2 has to be too large, there are some scheme equivalents to POR that use an independent overreaching zone ***Z1e***, which can be used for this purpose. These schemes are ***DE Perm Z1e 1ch*** and ***DE Perm Z1e 3ch***

9.7.8.2 PUR SCHEMES FOR TEED FEEDERS

For a Permissive Underrreaching (PUR) scheme, the signalling channel is only keyed for internal faults. The channel is keyed by Zone 1 operation. Aided tripping will occur at a receiving terminal if its overreaching Zone 2 setting requirements have been met.

On teed feeder applications, a permissive trip is issued at a terminal if that terminal's Zone 2 operation is accompanied by receipt of a signal from EITHER remote terminal. This makes the signalling channel requirements for a PUR scheme less demanding than for a Permissive Overreach (POR) scheme. Either a common power line carrier (PLC) signalling channel or a triangulated signalling arrangement can be used, making a PUR scheme generally more attractive than a POR scheme for protecting for a teed feeder.

It must be recognised, however, that there are cases where instantaneous tripping will not occur with PUR schemes. The following figure illustrates three cases for which delayed tripping will occur:

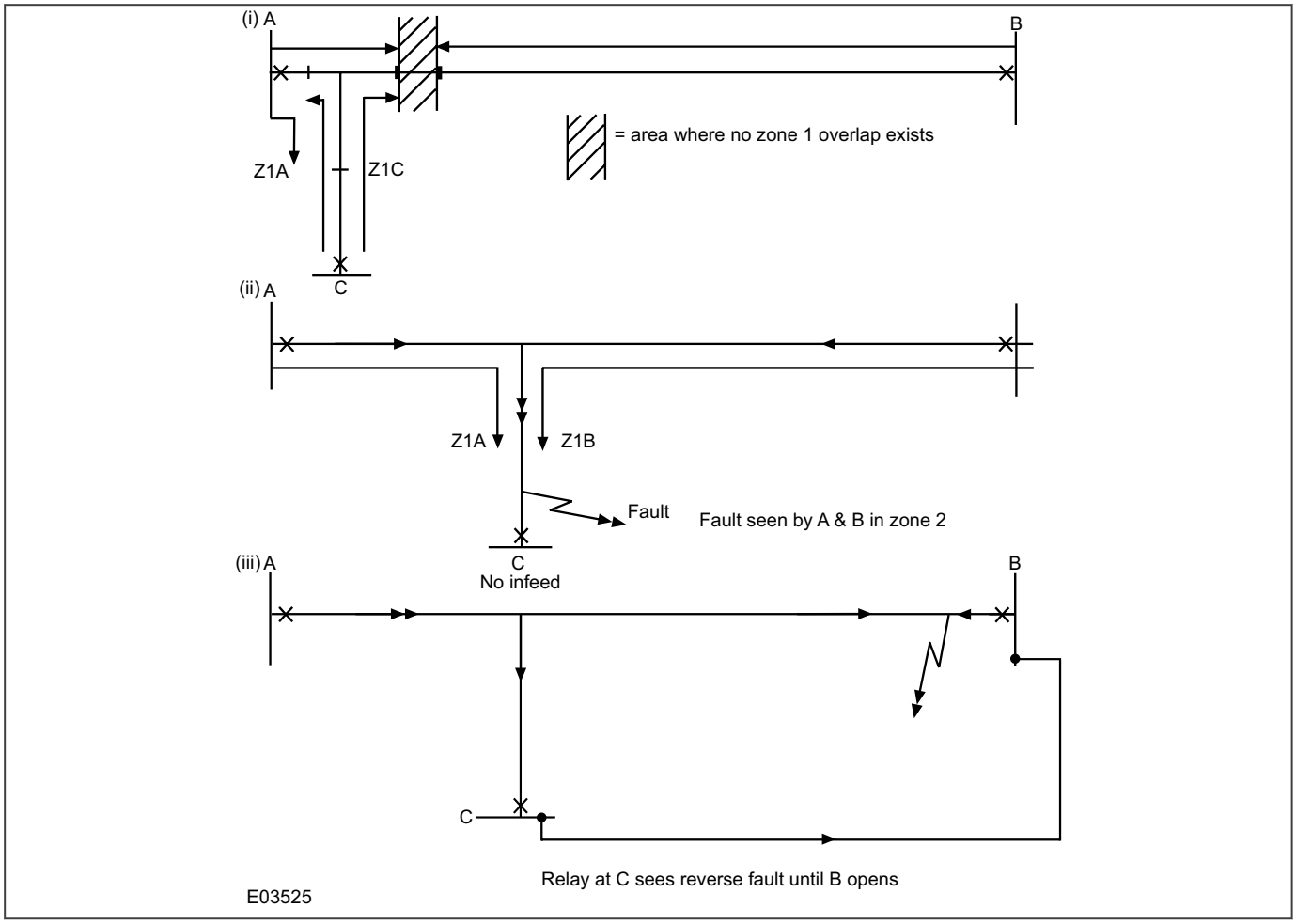


Figure 165: Problematic fault scenarios for PUR scheme application to teed feeders

- Scenario (i) shows a short tee connected to one nearby terminal and one distant terminal. In this case, Zone 1 elements set to 80% of the shortest connected feeder length don't all overlap, resulting in a section not covered by any Zone 1 element. Any fault in this section would rely on delayed Zone 2 tripping.
- Scenario (ii) shows an example where terminal C has no infeed. Distance elements at C may not operate for faults close to the terminal. As the fault is outside the Zone 1 reaches of A and B, clearance will rely on delayed Zone 2 tripping at A and B.
- Scenario (iii) shows an example where outfeed from terminal C feeds an internal fault via terminal B. In this case, terminal C will not see the fault until the breaker at B has operated. The result would be sequential (and hence delayed) tripping.

9.7.8.3 BLOCKING SCHEMES FOR TEED FEEDERS

With Blocking schemes, high speed operation can be achieved for circuits where there is no current infeed from one or more terminals. This makes Blocking schemes particularly suitable for protection of teed feeders. The scheme also has the advantage that the signalling requirement can be realised with one simplex channel.

Note:
Triangulated simplex channels could be used in place of a common simplex one if prefered.

As with Permissive Underreaching (PUR) schemes, a limitation of a Blocking scheme implementation is a scenario where outfeed from one terminal feeds an internal fault via another terminal. The terminal with the outfeed sees a

reverse fault condition. This results in a blocking signal being sent to the two remote terminals. Although the fault will be cleared, tripping will be prevented until the Zone 2 time delay has expired.

CHAPTER 10

NON-AIDED SCHEMES

10.1 CHAPTER OVERVIEW

This chapter describes the distance schemes that do not require communication between the ends (Non-Aided Schemes).

This chapter contains the following sections:

Chapter Overview 289
Non-Aided Schemes 290
Basic Schemes 291
Trip On Close Schemes 295
Zone 1 Extension Scheme 300
Loss of Load Scheme 302

10.2 NON-AIDED SCHEMES

This product provides Distance protection. The Distance protection has been designed for use as a standalone non-unit protection, or for use with communications systems to provide unit protection (Carrier Aided schemes).

Standalone operation provides basic scheme Distance protection (e.g. instantaneous Zone 1 operation, delayed Zone 2 protection and further delayed Back-up protection, etc.). It also implements some special standalone schemes that don’t require communications. These are known as Non-Aided Distance Schemes.

The non-aided schemes provided in this product can be divided into the following categories:

- Basic schemes
- Trip On Close schemes
- Zone 1 Extension scheme
- Loss of Load scheme

The settings for these Non-Aided Distance Schemes are located in the *SCHEME LOGIC* column.

10.3 BASIC SCHEMES

Basic Scheme operation is always executed if distance elements are enabled. It is the process by which the measured line impedance is compared against the Distance measuring zone configuration (reach settings and timers). Instantaneous or time delayed tripping or blocking signals may be issued for a specific zone according to its settings and the measured impedance values.

There are nine basic scheme zones; Zone 1, Zone 1e, Zone 2, Zone 3, Zone 4, Zone P, Zone Q, Zone R and Zone S.

The Basic Scheme settings include:

- A mode setting, which is common to all zones
- Zone Tripping settings for each zone
- Zone phase delay settings for each zone
- Zone ground delay settings for each zone

On a per-zone basis, phase and earth-fault elements may be set to have different time delays.

To supplement Basic Scheme operation, there are also standalone scheme designs (Non-Aided Distance Schemes) that provide timely clearance for particular fault scenarios where carrier aided signalling is either not available, or is unnecessary. These scenarios cover Trip on Closure (including Switch On to Fault, and Trip on Reclose), Loss of Load, and Zone1 Extension.

The Basic Scheme is continually executed, regardless of any carrier-aided acceleration schemes which may be enabled.

10.3.1 BASIC SCHEME MODES

The operation of distance zones according to their set time delays is called the basic scheme. The basic scheme always runs, regardless of any channel-aided acceleration schemes which may be enabled.

The ***BasicScheme Mode*** setting defines how the timers associated with the different Distance zones in the Basic Scheme are initiated by pick up (start) of zone elements.

In `Standard` mode, a zone timer starts only when the corresponding distance zone start occurs.

In `Alternative` mode, if a condition causes any of the enabled Distance elements to start, then the ***Any Distance Start*** DDB signal is asserted. This starts the timers associated with all enabled zones (phase zone timers and earth zone timers are started). The timers are reset if the ***Any Distance Start*** signal resets. If a Distance zone measuring element is picked up when its associated zone timer times-out, a trip is issued for that zone element.

The `Alternative` mode is especially suitable for evolving faults, since all zone timers will be initiated at initial fault inception, rather than waiting to start a timer as additional phases become faulted. This minimises the overall fault clearance time as the fault develops.

The two modes are described by the following logic diagrams.

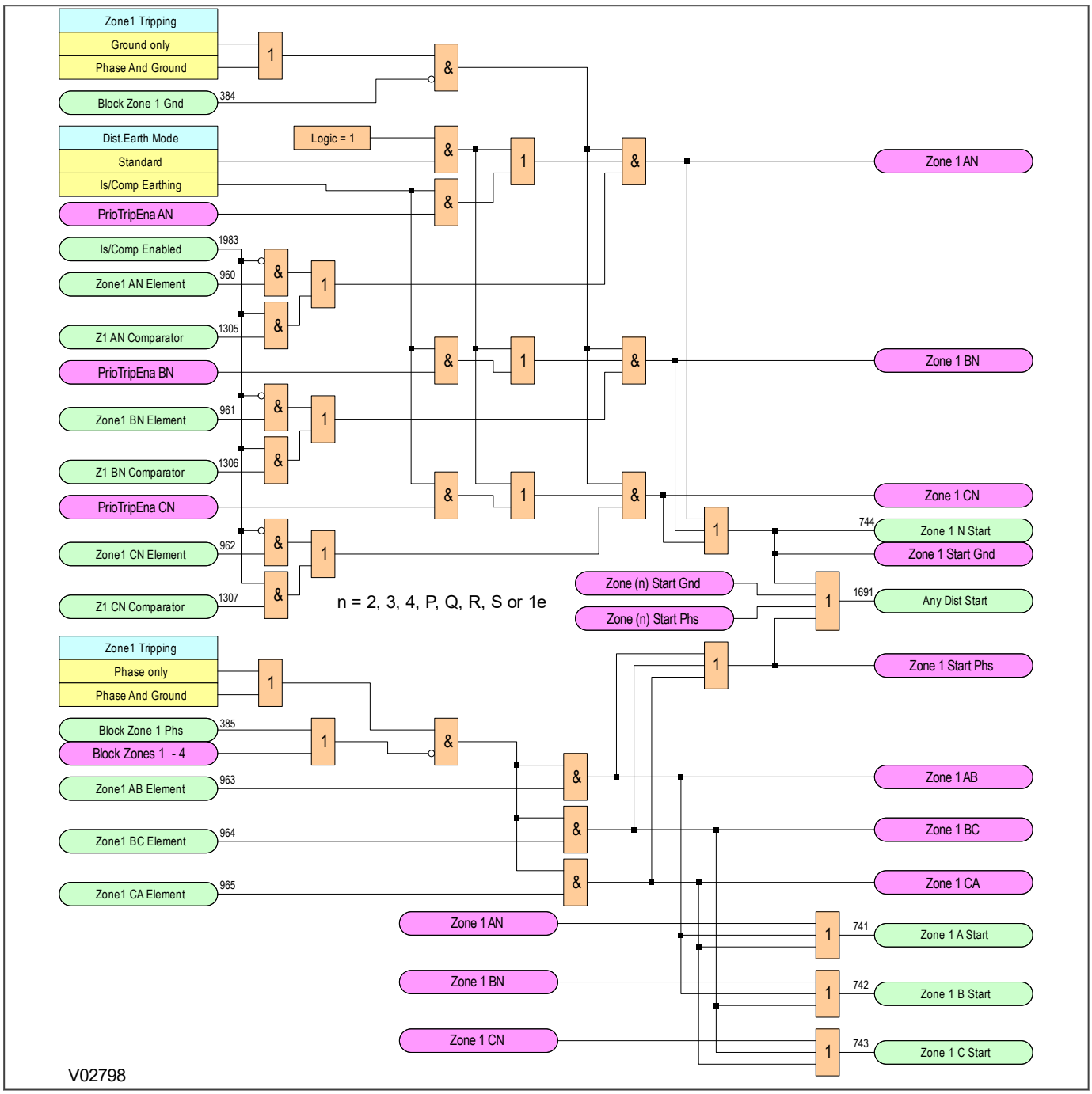


Figure 166: Zone starting logic

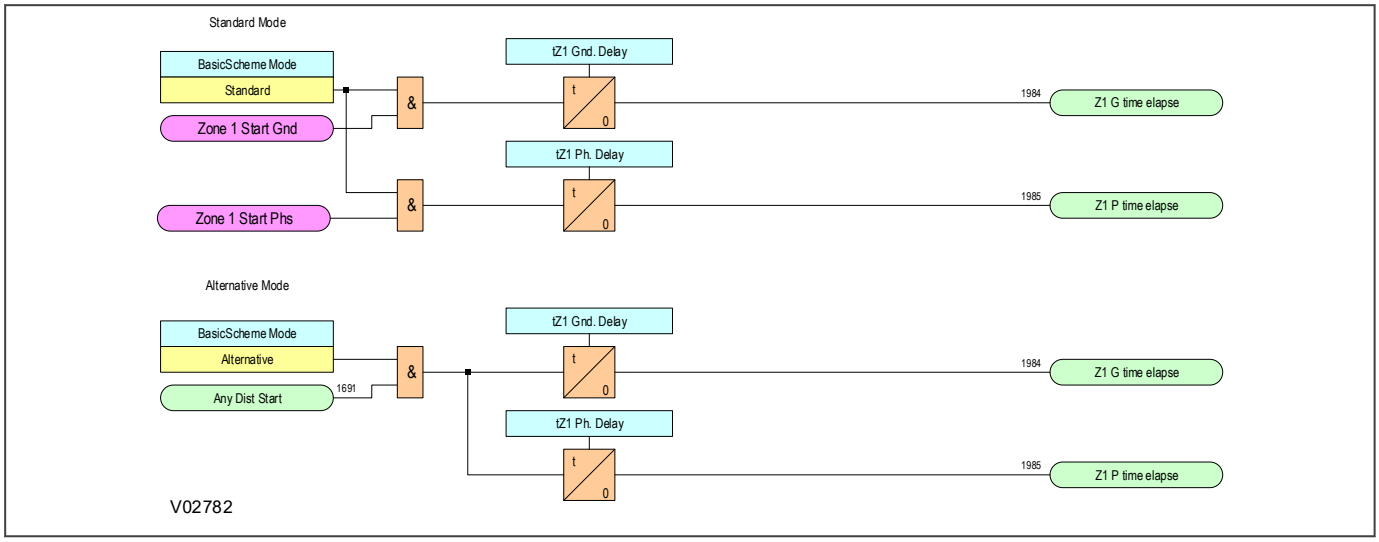


Figure 167: Zone timer logic

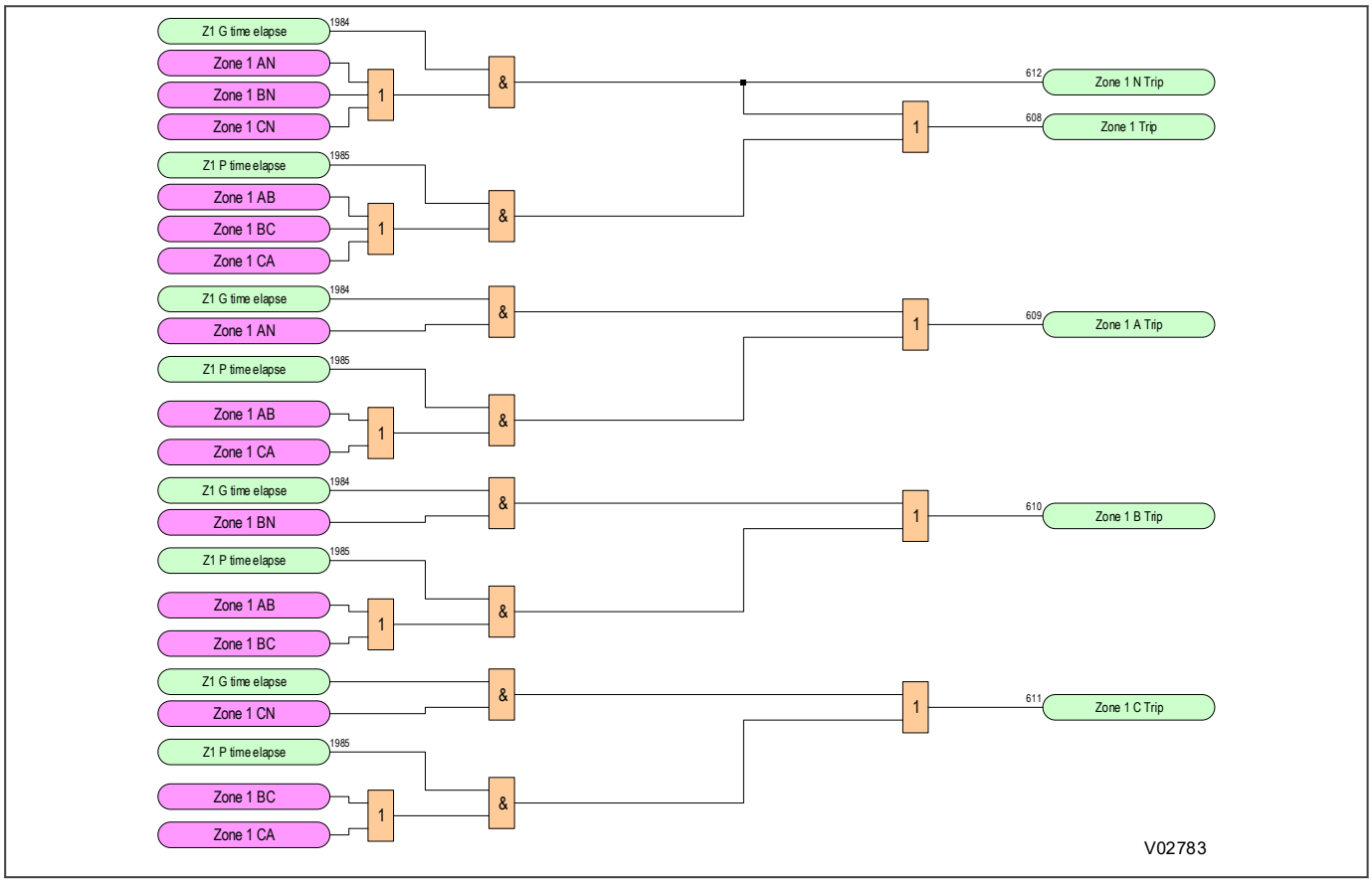


Figure 168: Zone trip logic

10.3.2 BASIC SCHEME SETTING

The Zone 1 time delay (tZ1) is generally set to zero, giving instantaneous operation.

The Zone 2 time delay (tZ2) is set to co-ordinate with Zone 1 fault clearance time for adjacent lines. The total fault clearance time consists of the downstream Zone 1 operating time plus the associated breaker operating time. Allowance must also be made for the Zone 2 elements to reset following clearance of an adjacent line fault and also for a safety margin. A typical minimum Zone 2 time delay is of the order of 200 ms.

The Zone 3 time delay (tZ3) is typically set with the same considerations made for the Zone 2 time delay, except that the delay needs to co-ordinate with the downstream Zone 2 fault clearance. A typical minimum Zone 3 operating time would be in the region of 400 ms.

The Zone 4 time delay (tZ4) needs to coordinate with any protection for adjacent lines in the protection's reverse direction.

Separate time delays can be applied to both phase and ground fault zones, for example where ground fault delays are set longer to time grade with external ground/earth overcurrent protection.

Any zone (#) which may reach through a power transformer reactance, and measure secondary side faults within that impedance zone should have a small time delay applied. This is to avoid tripping on the inrush current when energising the transformer.

As a general rule, if the Zone Reach setting is greater than 50% of the transformer reactance, set the Zone delay to be 100 ms or greater. Alternatively, the 2nd harmonic detector output (which is available in the Programmable Scheme Logic) may be used to block zones that may be at risk of tripping on inrush current. Settings for the inrush detector are found in the *SUPERVISION* column.

The figure below shows the typical application of the Basic scheme.

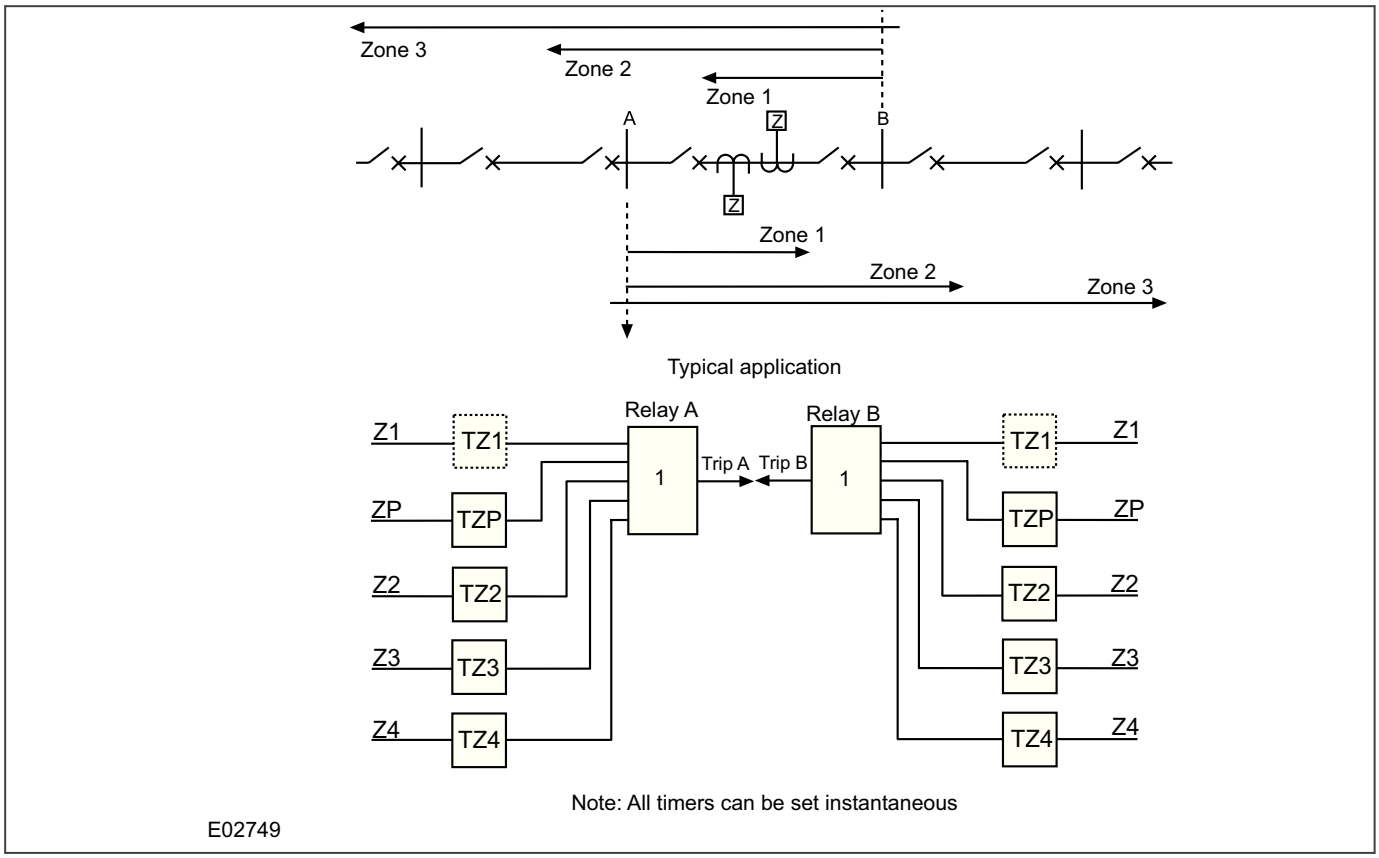


Figure 169: Basic time stepped distance scheme

10.4 TRIP ON CLOSE SCHEMES

Logic is provided for situations where special tripping may be necessary following closure of the associated circuit breaker. Two cases of Trip on Close (TOC) logic are catered for:

- Switch on to Fault (SOTF)
- Trip on Reclose (TOR)

SOTF provides instantaneous operation of selected elements if a fault is present when manual closure of the circuit breaker is performed.

TOR provides instantaneous operation of selected elements if a persistent fault is present when the circuit breaker attempts autoreclosure.

The SOTF and TOR functions are known as Trip on Close logic. These two methods can operate independently, or in parallel, according to the settings selection, and the settings are located in the *TRIP ON CLOSE* section of the *SCHEME LOGIC* column of the menu.

SOTF and TOR are complemented by Current No Voltage level detectors (also known as CNV level detectors).

CNV detection is associated with the functionality used to determine pole dead conditions and so the CNV level detectors are set using the *POLEDEAD VOLTAGE* and *UNDERCURRENT* settings located in the *CB FAIL & P.DEAD* column.

By default, the current threshold is 0.05 x In, and the voltage threshold is 38.1 V.

A 10ms time delay is included in the logic to avoid possible race conditions between fast operating level detectors.

> *Note:*
> *The Current no Volts function uses the same phase current input signals that are used by the local overcurrent protection elements. In cases of products with more than one set of input CTs, the currents are combined and used in the same way for the CNV function as they are for the overcurrent and measurements functions.*

The following figures outline the functionality of the Trip on Close feature and the complementary Current No Volt level detectors.

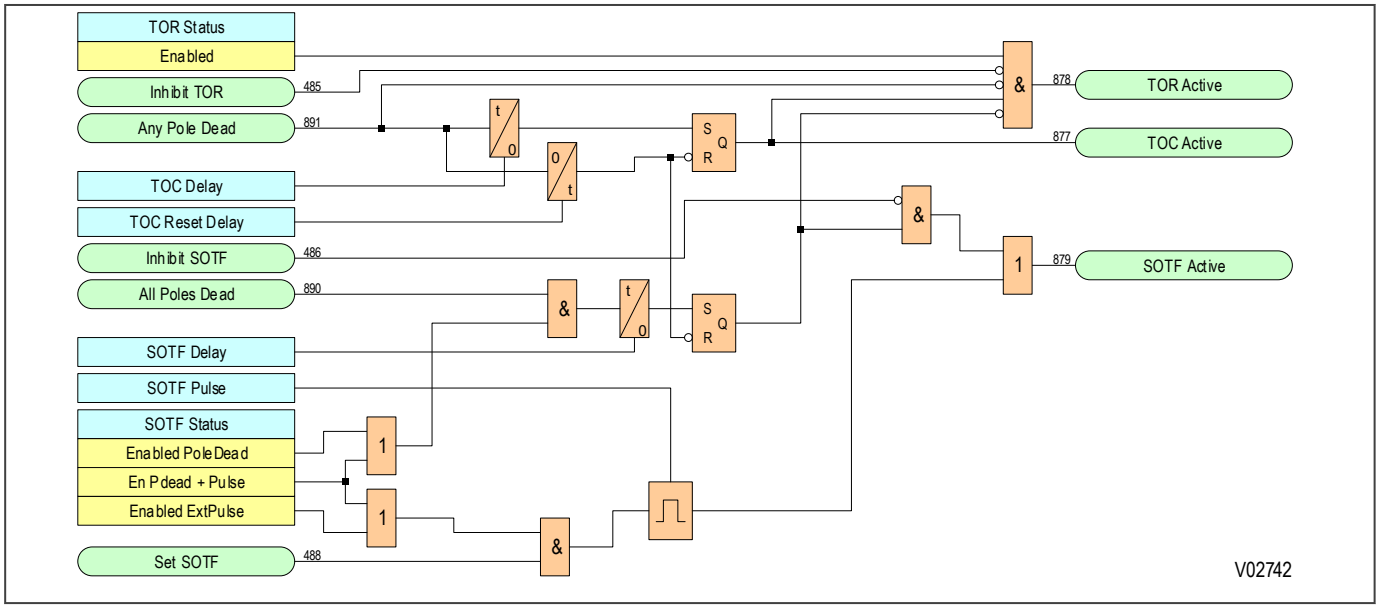


Figure 170: Trip on close logic

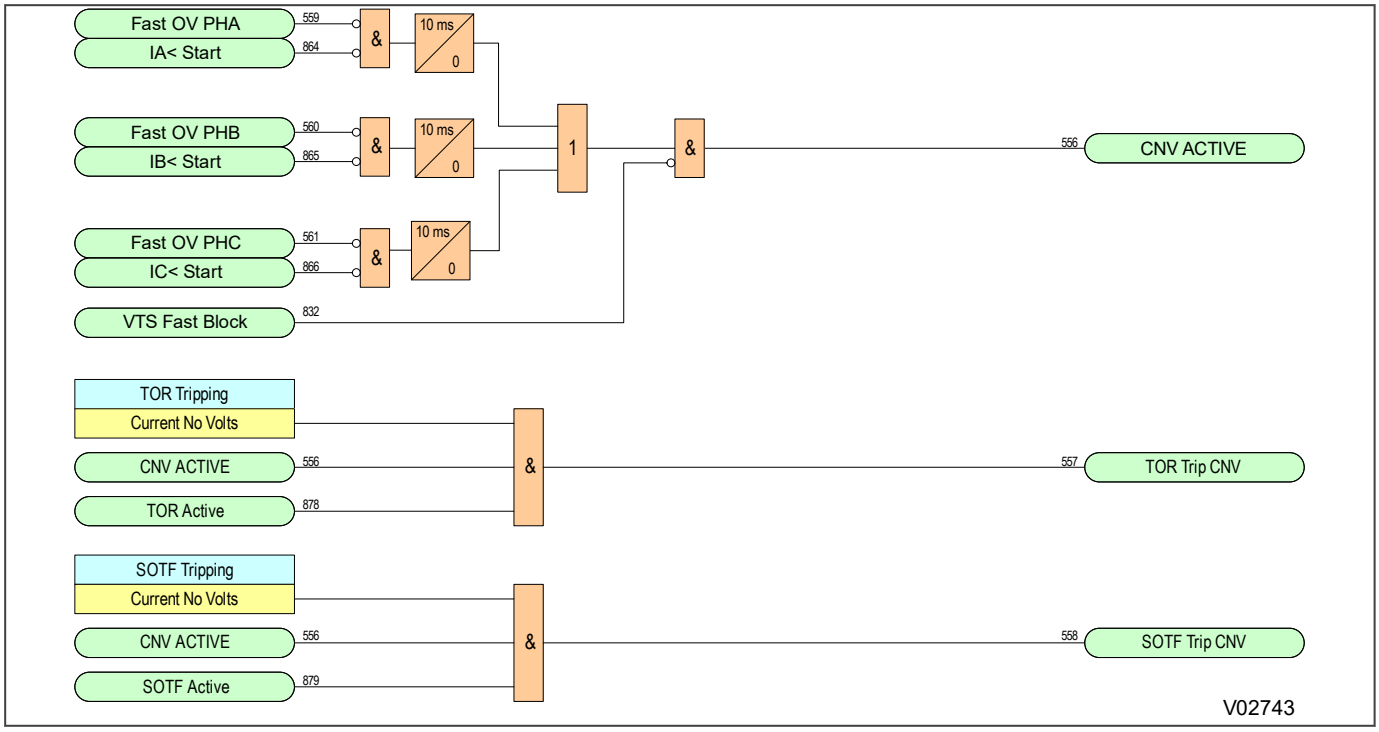


Figure 171: Trip on close based on CNV level detectors

10.4.1 SWITCH ON TO FAULT (SOTF)

You can use the ***SOTF Status*** setting to activated SOTF in in three different ways. It can be:

- Enabled using the pole dead detection logic. If an 'All Pole Dead' condition is detected, the ***SOTF Delay*** timer starts. Once this timer expires, SOTF is enabled and stays active for the period set in the ***TOC Reset Delay*** setting.
- Enabled by an external pulse. SOTF is enabled after an external pulse linked to DDB ***Set SOTF*** is ON. The external pulse could be a circuit breaker close command, for example. The function stays active for the duration of the ***SOTF Pulse*** setting.
- Enabled using both pole dead detection logic and an external pulse.

Three pole instantaneous tripping (and auto-reclose blocking) occurs for any fault detected by the selected zones or Current No Volt level detectors when in SOTF mode. Whether this feature is enabled or disabled, the normal time delayed elements or aided channel scheme continues to function and can trip the circuit.

The ***SOTF Delay*** is a pick up time delay that starts after opening all three poles of a circuit breaker (CB). If the CB is then closed after the set time delay has expired, SOTF protection is active. SOTF provides enhanced protection for manual closure of the breaker (not for auto-reclosure). This setting is visible only if `Enabled PoleDead` or `En Pdead + Pulse` are selected to enable SOTF.

While the Switch on to Fault Mode is active, the protection trips instantaneously for pick up of any zone selected in these links. To operate for faults on the entire circuit length, you should select at least Zone 1 and Zone 2 using the SOTF Tripping setting . If no elements are selected, the normal time delayed elements and aided scheme provide the protection.

A user settable time window during which the SOTF protection is available through the ***SOTF Pulse*** setting This setting is visible only if `Enabled ExtPulse` or `En Pdead + Pulse` are selected to enable SOTF.

10.4.1.1 SWITCH ONTO FAULT MODE

To ensure fast isolation of faults (for example a closed three phase earthing switch), on energisation enable this feature with appropriate zones or Current No Volt (CNV) level detectors, depending on utility practices.

When busbar voltage transformers are used, the ***Pole Dead*** signal is not produced. Connect circuit breaker auxiliary contacts for correct operation. This is not necessary if the SOTF is activated by an external pulse.

- ***SOTF Delay***: The time chosen should be longer than the slowest delayed-auto-reclose dead time, but shorter than the time in which the system operator might re-energise a circuit once it had opened/tripped. We recommend 110 seconds as a typical setting.
- ***SOTF Pulse***: Typically this could be set to at 500ms. This time is enough to establish completely the voltage memory of distance protection.
- ***TOC Reset Delay***: We recommend 500ms as a typical setting (chosen to be in excess of the 16 cycles length of memory polarising, allowing full memory charging before normal protection resumes).

10.4.1.2 SOTF TRIPPING

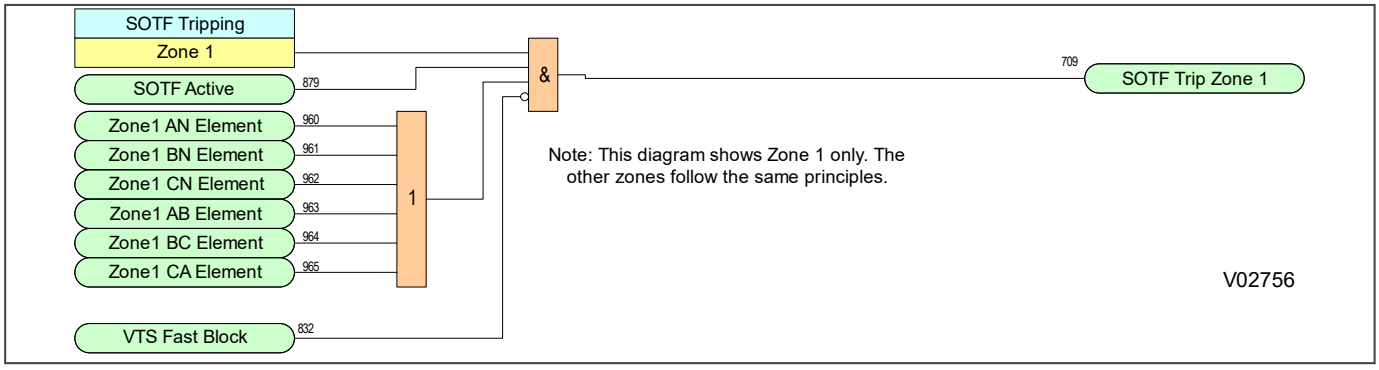


Figure 172: SOTF tripping

10.4.1.3 SOTF TRIPPING WITH CNV

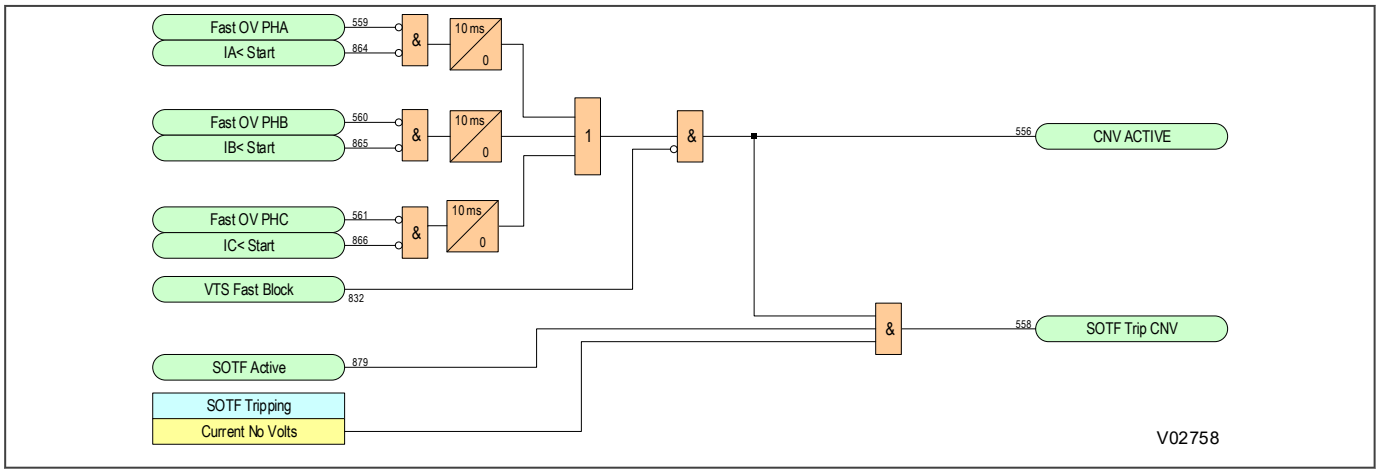


Figure 173: SOTF tripping with CNV

10.4.2 TRIP ON RECLOSE (TOR)

Trip On Reclose (TOR) is special protection following auto-reclosure. The ***TOR status*** setting is used to enable or disable TOR. When enabled, TOR is activated after the TOC Delay expires, ready for application when an auto-reclose shot occurs.

When this feature is enabled, the protection operates in 'Trip on Reclose mode' for a period following circuit breaker (CB) closure. Three-phase instantaneous tripping occurs for any fault detected by the selected zones or CNV level detectors. Whether this feature is enabled or disabled, the normal time-delayed elements or aided channel scheme continue to function and can trip the circuit.

The SOTF and TOR features stay in service for the duration of the ***TOC Reset Delay*** time, once the circuit is energised. The delay timer starts on CB closure and is common for SOTF and TOR protection. Once this timer expires after successful closure, all protection reverts to normal.

A user settable time delay (***TOC Delay***) starts when the CB opens, after which TOR is enabled. The time delay must not exceed the minimum Dead Time setting of the auto-reclose because both times start simultaneously and TOR protection must be ready by the time the CB closes on potentially persistent faults.

While the Trip on Reclose Mode is active, the protection trips instantaneously for pick up of any selected Distance zone. You select the zone with the ***TOR Tripping*** setting. For example, Zone 2 could operate without waiting for the usual time delay if a fault is in Zone 2 on CB closure. Also Current No Volts can be mapped for fast fault clearance on line reclosure on a permanent fault. To operate for faults on the entire circuit length, at least Zone 1 and Zone 2 should be selected. If no elements are selected, the normal time delayed elements and aided scheme provide the protection. TOR tripping is three-phase and auto-reclose is blocked.

10.4.2.1 TRIP ON RECLOSE MODE

To ensure fast isolation of all persistent faults following the circuit breaker reclosure, enable this feature with appropriate zones selected or Current No Volt (CNV) level detectors.

- ***TOC Delay***: The Trip on Reclose (TOR) is activated after ***TOC Delay*** has expired. The setting must not exceed the minimum autoreclose ***Dead Time*** setting to make sure that the TOR is active immediately on reclose command.
- ***TOC Reset Delay***: We recommend 500ms as a typical setting.

10.4.2.2 TOR TRIPPING LOGIC FOR APPROPRIATE ZONES

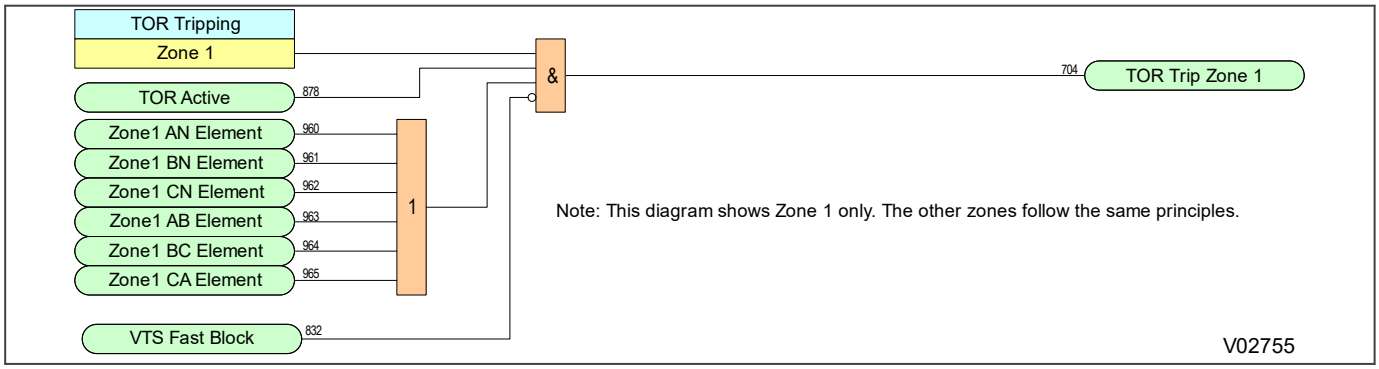


Figure 174: TOR tripping logic for appropriate zones

10.4.2.3 TOR TRIPPING LOGIC WITH CNV

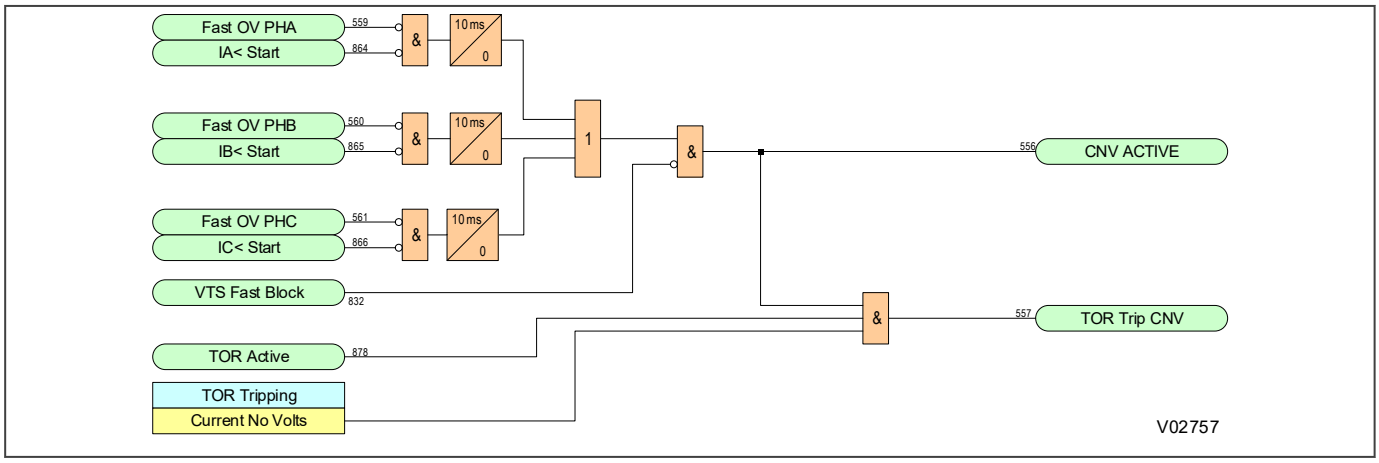


Figure 175: TOR tripping logic with CNV

10.4.3 POLARISATION DURING CIRCUIT ENGERGISATION

While the Switch on to Fault (SOTF) and Trip on Reclose (TOR) modes are active, the directionalised distance elements are partially cross polarised from other phases. The same proportion of healthy phase to faulted phase voltage, as given by the ***Dist. Polarizing*** setting in the *DISTANCE SETUP* menu, is used.

Partial cross polarisation is therefore substituted for the normal memory polarising, for the duration of the ***TOC Delay***. If insufficient polarising voltage is available, a slight reverse offset (approximately 25% of the forward reach) is included in the Zone 1 characteristic to enable fast clearance of close up three-phase faults.

10.5 ZONE 1 EXTENSION SCHEME

Auto-reclosure is widely used on radial overhead line circuits to re-establish supply following a transient fault. A Zone 1 extension scheme may be applied to a radial overhead feeder to provide high speed protection for transient faults along the whole of the protected line. The figure below shows the alternative reach selections for zone 1: Z1 or the extended reach Z1X.

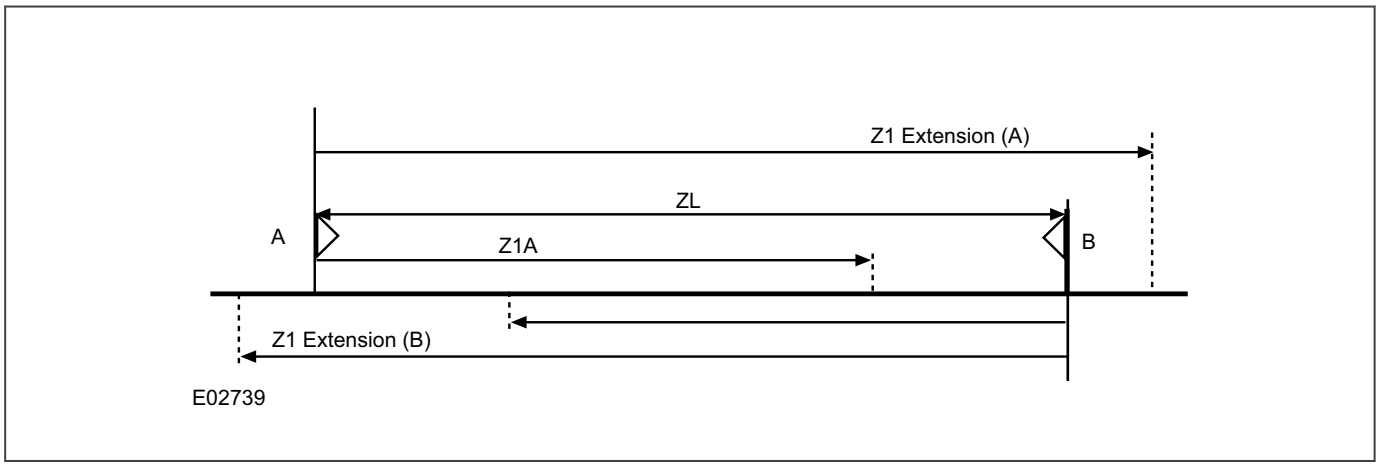


Figure 176: Zone 1 extension scheme

In this scheme Zone 1X is enabled and set to overreach the protected line. A fault on the line, including one in the end 20% not covered by Zone 1, results in instantaneous tripping followed by autoreclosure. Zone 1X has resistive reaches and residual compensation similar to Zone 1. The autorecloser is used to inhibit tripping from Zone 1X so that on reclosure the device operates with Basic scheme logic only, to co-ordinate with downstream protection for permanent faults. Therefore transient faults on the line are cleared instantaneously, which reduces the probability of a transient fault becoming permanent. However, the scheme can operate for some faults on an adjacent line, although this is followed by autoreclosure with correct protection discrimination. Increased circuit breaker operations would occur, together with transient loss of supply to a substation.

Fault Trip	Z1X Time Delay
First fault trip	= tZ1
Fault trip for persistent fault on auto-reclose	= tZ2

The Zone 1 extension scheme can be disabled, permanently enabled or just brought into service when the communication channel fails and the aided scheme is inoperative. If used in conjunction with a channel-aided scheme, Z1X can be set to be enabled when Ch1 or Ch2 fails, or when all channels fail, or when any channel fails.

Zone 1 extension schemes have the following reaches:

- ***Z1 Ext Ph*** range 100% to 9999 % with steps of 1%
- ***Z1 Ext Gnd*** range 100% to 9999 % with steps of 1%
- ***Z1 Ext Ph R*** range 100% to 200% with steps of 1%
- ***Z1 Ext Gnd R*** range 100% to 200% with steps of 1%

Note:
Beyond 500/IN ohms accuracy of the measurement is not guaranteed. The multiplier should result in no more than 500/IN.

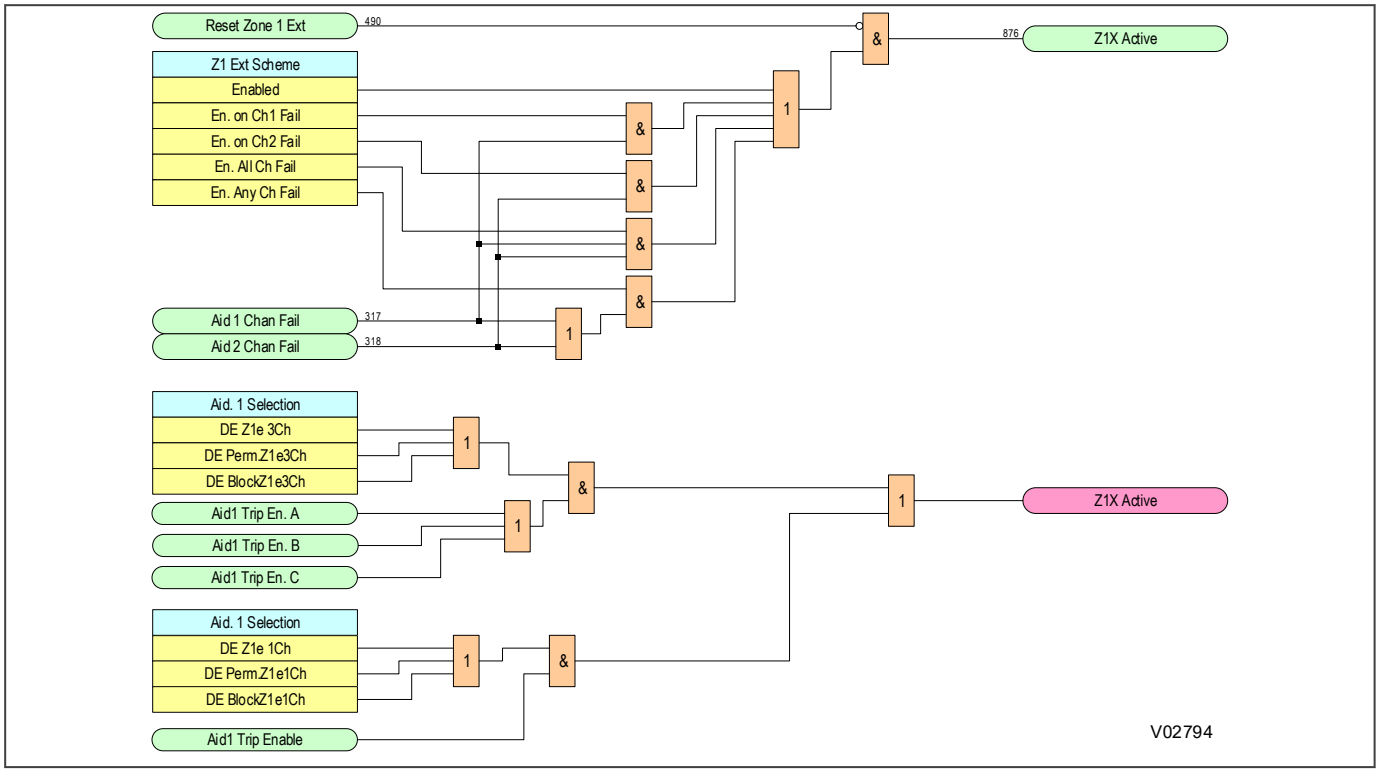


Figure 177: Zone 1 extension logic

10.6 LOSS OF LOAD SCHEME

The Loss of Load Scheme provides fast unit protection performance for most fault types occurring on a double-end fed line or feeder, but it does not need communications.

It is used on circuits that are designed for three-pole tripping, and provides protection for faults involving one or two phases. It is not suitable for single-pole tripping applications, and it cannot protect against three-phase faults.

The scheme does not require communications, but it can be used alongside carrier aided schemes if communications are available.

The Loss-of-Load scheme can be permanently enabled, permanently disabled, or enabled if communication failure compromises channel-aided scheme operation. If used in conjunction with a channel-aided scheme, loss of load can be set to be enabled if only Channel 1 fails, or if only Channel 2 fails, or if both channels fail, or if either channel fails. Aided scheme communication failure is detected by permissive scheme unblocking logic, or the presence of a Channel Out of Service (COS) input.

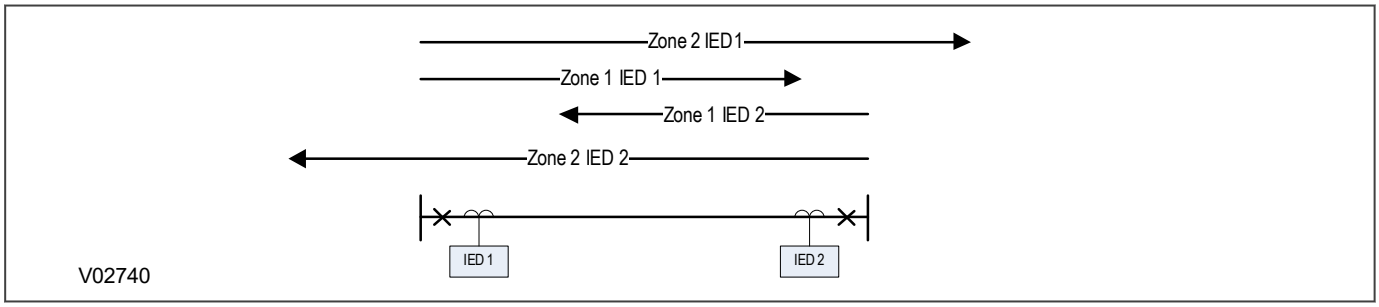


Figure 178: Loss of load accelerated trip scheme

Any fault in the reach of Zone 1 results in fast tripping of the local circuit breaker. For an end zone fault for IED 1 (near IED 2) with remote infeed (from IED 2), the remote breaker is tripped in Zone 1 by the remote device at IED 2. The local device (IED 1) can recognise this by detecting loss of load current in the healthy phases. This condition, in conjunction with operation of a Zone 2 comparator at IED 1P, can be used to trip the local circuit breaker.

Before an accelerated trip can occur, load current must be detected before the fault. The loss of load current opens a window during which time a trip occurs if a Zone 2 comparator operates. A typical setting for this window is 40ms as shown in the figure below, although this can be altered in the ***LoL Window*** setting. The accelerated trip is delayed by 18ms to prevent initiation of a loss of load trip due to circuit breaker pole discrepancy occurring for clearance of an external fault. The local fault clearance time can be deduced as follows:

$$t = Z1d + 2CB + LDr + 18ms$$

where:

- Z1d = Maximum downstream zone 1 trip time
- CB = Breaker operating time
- LDr = Upstream level detector (***LOL <1***) reset time

For circuits with load tapped off the protected line, care must be taken in setting the loss of load feature to ensure that the undercurrent level detector setting is above the tapped load current. When selected, the loss of load feature operates with the main distance scheme that is selected. This provides high speed clearance for end zone faults when the Basic scheme is selected or, with permissive signal aided tripping schemes, it provides high speed back up clearance for end zone faults if the channel fails.

Note:
Loss of load tripping is only available where three pole tripping is used.

Note:
*Assertion of the **Any Trip** DDB signal or the **Inhibit LOL** DDB signal will prevent LOL tripping.*

The detailed Loss of Load logic diagram is shown below:

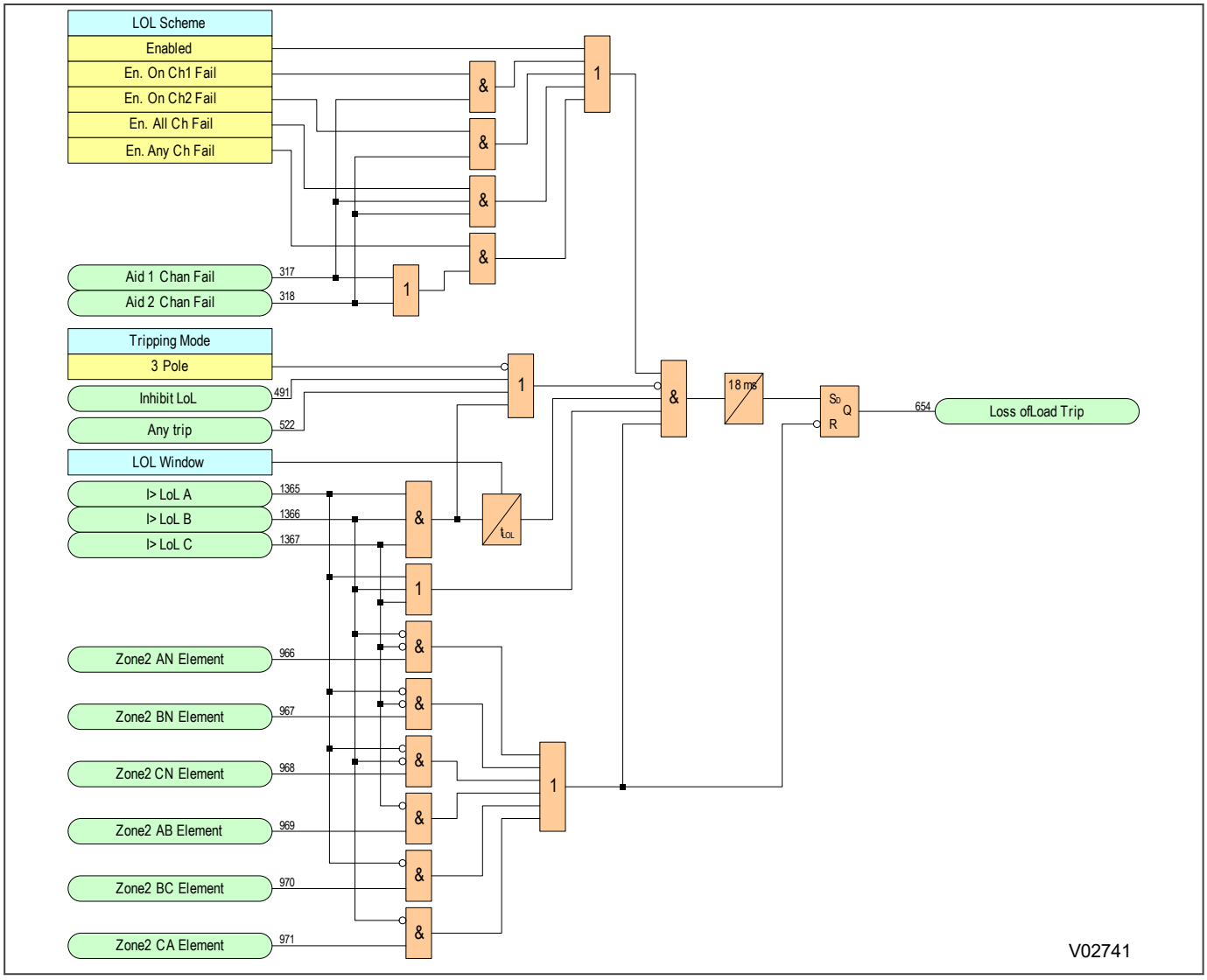


Figure 179: Loss of load logic

CHAPTER 11

POWER SWING FUNCTIONS

11.1 CHAPTER OVERVIEW

This chapter describes special blocking and protection functions, which use Power swing Analysis.

This chapter contains the following sections:

Chapter Overview 305
Introduction to Power Swing Blocking 306
Power Swing Blocking 308
Out of Step Protection 323

11.2 INTRODUCTION TO POWER SWING BLOCKING

Power swings are variations in power flow that occur when the voltage phase angles at different points of generation shift relative to each other. They can be caused by events such as fault occurrences and subsequent clearance. Power swings may be classified as stable or unstable.

A stable power swing is one where, following a disturbance, all sources of generation return to a state where they are all generating synchronous voltages. An unstable power swing is one where at least one source of generation cannot restore operation that is synchronous with the rest of the system. In this case the poles of one source of generation slip with respect to those of another. This condition is known as Pole Slipping.

A power swing may cause the impedance presented to Distance protection to move away from the normal load area and into one or more of its tripping characteristics. Without attention this could lead to unwanted or uncontrolled tripping.

Note:
Power swings do not involve earth, so only phase-phase impedances are affected.

For stable power swings, distance protection should not trip. To prevent tripping, a Power Swing Blocking (PSB) function is usually provided to compliment Distance protection.

For unstable power swings, there may be a strategy for instigating a controlled system split. In this case, distance protection should not trip during loss of stability. If unstable power swings or Pole-Slipping conditions might be expected, certain points on the network may be designated as split points, where the network should be split if unstable (or potentially unstable) conditions occur. Strategic splitting of the system can be achieved by means of dedicated Out-of-Step Tripping protection (OOS or OST protection). Or it may be possible to achieve splitting by strategically limiting the duration for which the operation of a specific distance protection is blocked during power swing conditions.

A method often used to help understand power system stability and Pole Slipping is called Equal Area Criterion. This is based on a number of operational curves as outlined in the figure below:

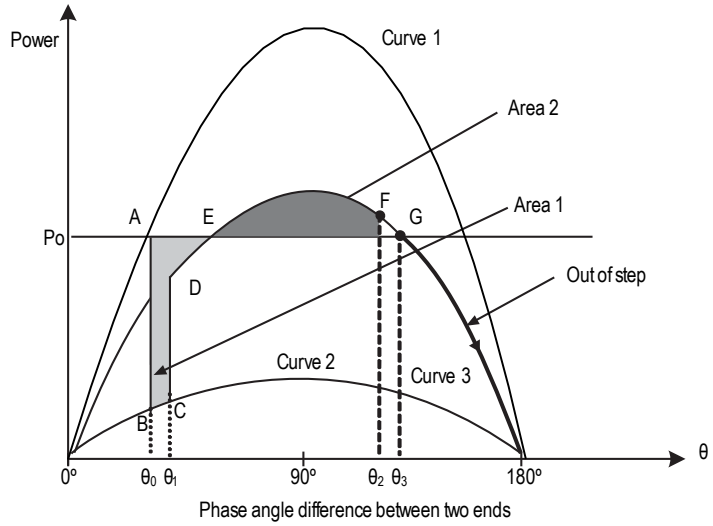


Figure 180: Power transfer related to angular difference between two generation sources

The figure describes the behaviour of a power system with parallel lines connecting two sources of generation.

- Curve 1 represents pre-fault system operation through parallel lines where the transmitted power is Po.
- Curve 2 represents transmitted power during a phase-phase-earth fault.
- Curve 3 represents a new power curve when the faulted line is tripped.

At fault inception, the operating point A moves to B, which is a reduced power transfer level. There is, therefore, a surplus of power (A to B) at that sending end and a corresponding deficit of power at the receiving end. The sending end generators start to speed up, and the receiving end generators start to slow down, so the phase angle θ increases, and the operating point moves along curve 2 until the fault is cleared (point C). At this point, the phase angle is θ1. The operating point now moves to point D on curve 3 which represents the power transfer curve when just one line is in service. There is still a power surplus at the sending end and a deficit at the receiving end, so the generators continue to lose synchronism and the operating point moves further along curve 3.

If, at some point between E and G (point F) the generators are rotating at the same speed, the phase angle will stop increasing. According to the Equal Area Criterion, this occurs when Area 2 is equal to Area 1. The sending end will now start to slow down and receiving end to speed up. Therefore, the phase angle starts to decrease and the operating point moves back towards E. As the operating point passes E, the net sending end deficit again becomes a surplus and the receiving end surplus becomes a deficit, so the sending end generators begin to speed up and the receiving end generators begin to slow down. With no losses, the system operating point will oscillate around point E on curve 3, but in practise the oscillation is damped, and the system eventually settles at operating point E.

So, if Area 1 is less than Area 2, the system will oscillate but will stay in synchronism. This swing is usually called a recoverable, or stable, power swing. If, on the contrary, the system passes point G with a further increase in angle difference between sending and receiving ends, the system loses synchronism and becomes unstable. This will happen if the initial power transfer Po is so high that the Area 1 is greater than Area 2. This power swing is not recoverable and is usually called an Out-of-Step condition or a Pole Slip condition. In such a case, only system separation and subsequent re-synchronising of the generators can restore normal system operation.

The point G is shown at approximately 120°, but this can vary. If, for example, the pre-fault transmitted power (Po) was high and the fault clearance was slow, Area 1 would be greater. For the system to recover from this case, the angle θ would be closer to 90º. Similarly, if the pre-fault transmitted power Po was low and fault clearance fast, Area 1 would be small, and the angle θ could go closer to 180º with the system remaining stable.

11.3 POWER SWING BLOCKING

A power swing may cause the impedance presented to the distance function to move away from the normal load area and into one or more of its tripping zones. Stable power swings should not cause the distance protection to trip. Therefore, if the power swing is deemed to be stable, the distance protection function for the zone in question is blocked. Unstable power swings should result in either tripping of the relevant protection element, or a system split. Therefore, the distance protection element should also be blocked for unstable power swings if there is a strategy for a controlled system split.

11.3.1 POWER SWING DETECTION

There are two power swing detection modes: `Advanced` and `Conventional`. You can set this with the ***Power Swing Mode*** setting.

Advanced mode provides 'settings-free' operation. This uses a superimposed current technique (also known as a delta technique). This technique is suitable for power swings in the normal to fast frequency range (>0.5Hz)

To detect slower power swings (<0.5Hz), a supplementary technique based on impedance characteristics is used. This so called slow swing technique will invoke the power swing blocking function should the power swing be to slow for the delta technique to operate. The impedance method uses zone 7 and zone 8 concentric quadrilateral impedance characteristics. Power swing detection is achieved by measuring the time taken for the impedance trajectory to cross through zone 8 into zone 7 (delta Z). In `conventional` mode, the impedance method is used for all power swings.

Once a power swing is detected the following actions occur:

- Relevant distance elements are blocked (if blocking is enabled).
- All zones are switched to self-polarised mho characteristics with 10% offset reach for maximum stability during the swing.

11.3.1.1 SETTINGS-FREE POWER SWING DETECTION

By "Settings-Free", we mean that there is no need to define any characteristic criteria. The only settings needed are to define what to do in the event of a power swing (Allow trip, block, or unblock with a delay).

The settings-free power swing detection technique uses a superimposed current detector (ΔI), as used in the phase selector. For each phase loop (A-B, B-C, C-A), the actual measured current is compared with the measured current from exactly two cycles earlier (present in a 2-cycle FIFO buffer). If there is a difference between the two (ΔI), this indicates that something is happening on that current loop.

The superimposed current (ΔI) is compared with a set threshold (set at 5%In) to produce a switching signal PH1. This switching signal is used as an input to the power swing blocking function. It also triggers the current sample values in the 2-cycle FIFO butter to be stored in memory for further current comparisons.

Superimposed currents appear during both fault conditions, and power swings. For fault conditions, superimposed components will not normally extend beyond two cycles. Under power swing conditions however, superimposed components persist beyond two cycles. We can use this fact to differentiate between faults and power swings.

During a power swing (in the absence of a fault), the phase selector will indicate a three-phase selection, or a phase-phase selection if one pole is dead. So if superimposed components persist for three cycles, and a “faulted-phase” indication of “three-phase with one pole dead” is present during those three cycles, a power swing has been detected and the relevant signals are asserted.

After a power swing condition has been detected, the ΔI threshold used by the phase selector is increased and the current values present in the two cycle buffer are stored. This provides coverage for faults that might occur whilst a power swing is in progress.

For a fault condition, the superimposed current detector should reset after two cycles, because once the fault current values enter the FIFO buffer, this will be compared with the present fault current and the superimposed current will return to zero. This will allow the power swing detection function to reset.

Configuring settings-free power swing detection

The power swing detection based on superimposed current requires no system study. You just need to decide whether a zone should be blocked or allowed to trip if a power swing is detected. You do this zone by zone using the zone specific settings. For example the zone 1 setting is ***Zone 1 Ph. PSB***. The available options are `Blocking`, `Allow Trip`, or `Delayed Unblock`.

11.3.1.1.1 TIMING OF THE PHASE SELECTOR SIGNALS

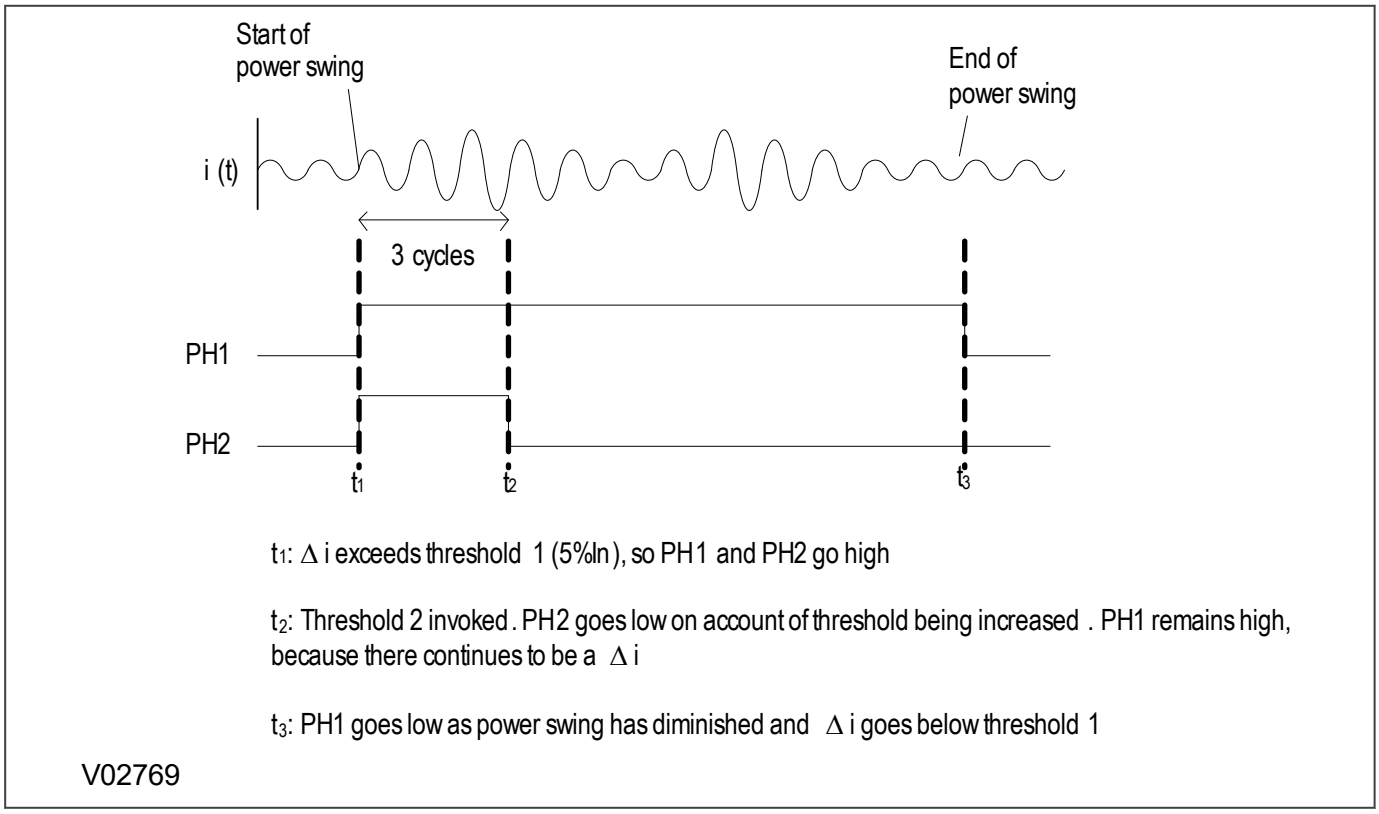
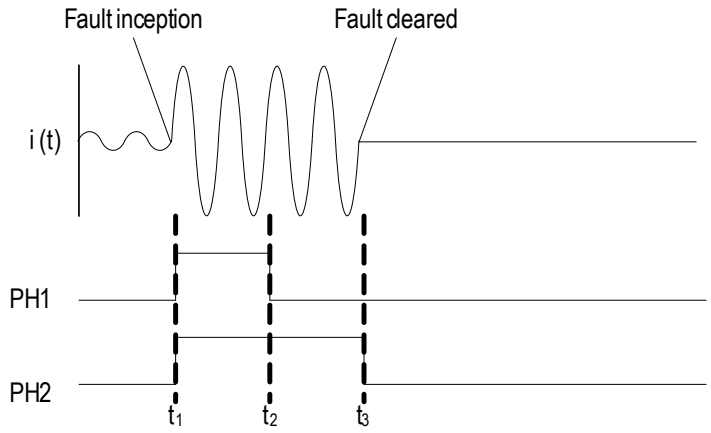


Figure 181: Phase selector timing for power swing condition



t_1: Δ i exceeds threshold 1 (5%In), so PH1 and PH2 go high

t_2: Fault current value appears in 2 cycle buffer . This equals present fault current value so Δ i is reduced to zero. PH1 therefore goes low. PH2 remains high because value in PH 2 memory is a stored value .

t_3: Fault is cleared so PH 2 goes low. PH1 stays low even though there is a new Δ I, because the absolute current value is also taken into consideration .

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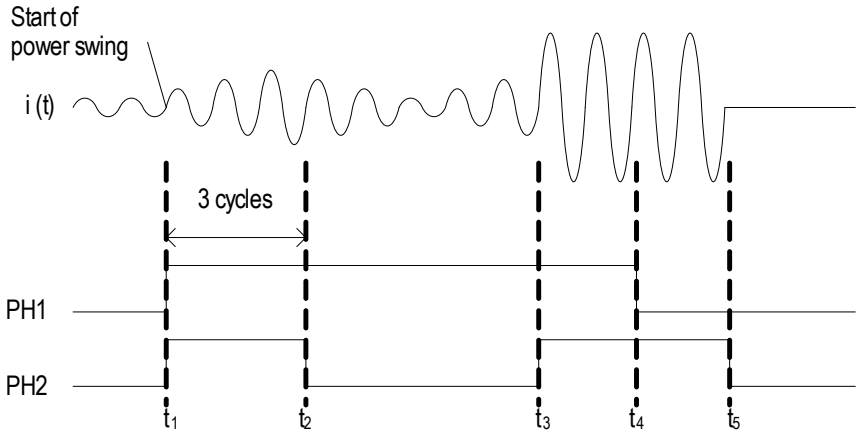
Figure 182: Phase selector timing for fault condition



t_1: Δ i exceeds threshold 1 (5%In), so PH1 and PH2 go high

t_2: Threshold 2 invoked (10%In). PH2 goes low on account of threshold being increased (from 5%IN to 10%In). PH1 remains high, because there continues to be a Δ i

t_3: Fault inception . Δ i exceeds threshold 2 (10%In), so PH2 goes high

t_4: 2 cycles after fault inception , PH1 goes low

t_5: Fault cleared , so PH2 goes low

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Figure 183: Phase selector timing for fault during a power swing

11.3.1.2 SLOW POWER SWING DETECTION

For slow power swings (0.5Hz and below) where the superimposed current may remain below the minimum 5%In threshold needed for the superimposed current (ΔI) detector, a different detection method is used. This method is called Slow Swing detection. This method requires the ***Slow Swing*** setting to be enabled.

> *Note:*
> *If the Slow Swing feature is not Enabled, very slow power swings (< 0.5 Hz) may not be detected.*

The Slow Swing method is based on changing impedance measurements and uses a pair of configurable concentric quadrilateral zones on the impedance plane (Zone 7 and Zone 8). Since power swings don't involve earth, the impedance measurements are based on positive sequence quantities and only phase-phase measurements are necessary. The characteristic is shown in the following figure:

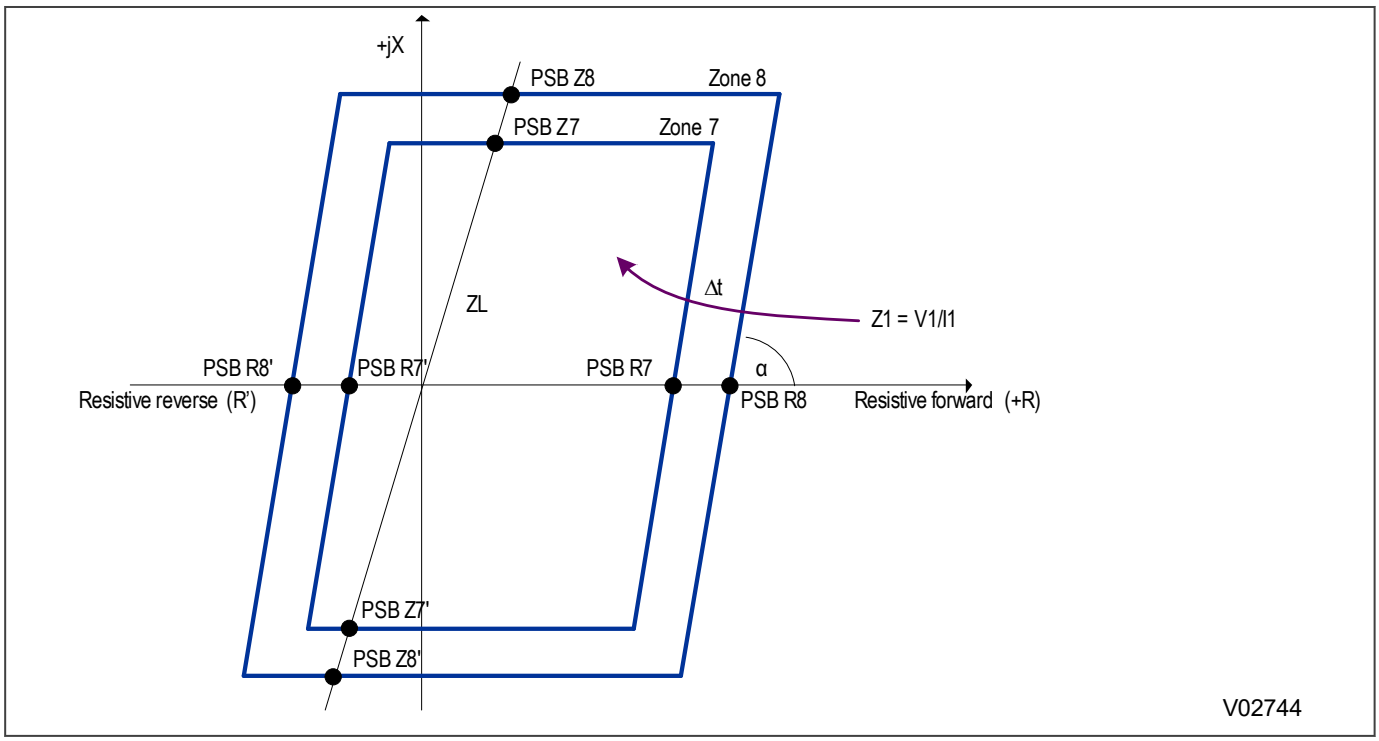


Figure 184: Slow power swing detection characteristic

The elapsed time defines the rate of change of impedance. If the rate of change is high, the change is due to a fault. If the rate of change is low, the protection indicates a slow power swing. So, if the time taken for the impedance trajectory to pass through zone 8 into zone 7 is greater than the time defined by the PSB timer, a slow power swing is deemed to be in progress. If the time taken for the impedance trajectory to pass through zone 8 into zone 7 is less than that defined by the PSB timer, it is deemed to be a fault.

In other words, a power swing is indicated if the following condition is true:

$\Delta\tau >$ ***PSB Timer***

Both Zone 7 and Zone 8 characteristics are based on the positive sequence impedance measurement; $Z_1 = V_1/I_1$. The minimum current (sensitivity) needed for Zone 7 and Zone 8 measurements is 5%In.

Configuring slow swing detection

Slow Swing power swing detection and blocking must first be enabled with the ***Slow Swing*** setting. After this, you need to configure the resistive and impedance reach settings to define the concentric quadrilateral characteristics for zones 7 and 8:

PSB R7: forward resistive reach for zone 7

PSB R7': reverse resistive reach for zone 7

PSB R8: forward resistive reach for zone 8

PSB R8': reverse resistive reach for zone 8

PSB Z7: forward impedance reach for zone 7

PSB Z7': reverse impedance reach for zone 7

PSB Z8: forward impedance reach for zone 8

PSB Z8': reverse impedance reach for zone 8

You also need to configure the impedance phase angle α. This is the same for zone 7 and zone 8. To do this you need to set ***Alpha Z7/Z8*** between 20° and 90°.

The ***PSB timer*** setting defines the minimum time that the impedance trajectory must take to cross through zone 8 into zone 7 ($\Delta\tau$) before a power swing is deemed to have taken place. A power swing is indicated if $\Delta\tau >$ ***PSB Timer***.

11.3.1.3 POWER SWING DETECTION (ALARMING AND BLOCKING)

Detection of power swings

A power swing may cause the impedance presented to a distance relay to move away from the normal load area and into one or more of its tripping characteristics. In the case of a stable power swing it is important that the relay should not trip. The relay should also not trip during loss of stability since there may be a utility strategy for controlled system break up during such an event.

The power swing detection in the 5th Generation is an advanced technique that uses superimposed current (ΔI) detector similar to the phase selection principle described above. However for the power swing detector the current is always compared to that 2 cycles previous. For a fault condition this power swing detector (PSD) will reset after 2 cycles as no superimposed current is detected.

For a power swing, PSD will measure superimposed current for longer than 2 cycles, and it is the length of time for which the superimposed current persists that is used to distinguish between a fault and a power swing. A power swing is deemed to be in progress if a three phase selection, or a phase to phase selection when one pole is open, produced in this way is retained for more than 3 cycles, as shown in the figure above. At this point the required distance zones can be blocked, to avoid tripping should the swing impedances cross into a tripping zone.

In order to detect slow power swings, when the superimposed current remains below the minimum threshold (5%In), a complementary method of detection could be used. This method requires zone 5 to be set. For the zone 5 setting, no system study is required, it is only necessary to set the R5 and R5' reach below the minimum possible load impedance, as explained in the Application Section. If the fault impedance remains within a zone 5 for at least 1 cycle without phase selection operation, the slow swing is declared. This complementary method works in parallel to the automatic, setting free technique explained above.

Zone 5 has a dual purpose: OST protection and slow swing detection. There is no conflict in zone 5 settings, i.e. zone 5 settings for OST protection (if applied) perfectly suit slow swing detection.

Actions upon power swing detection

Once a power swing is detected the following actions occur:

- Distance elements are blocked on selected zones providing blocking is enabled
- All zones are switched to self polarised mho characteristics for maximum stability during the swing
- A power swing block alarm is issued when the swing impedance enters a distance zone. The condition of entering an impedance zone avoids alarming for low current momentary swings that settle quickly
- When a power swing is in progress, the minimum threshold used by the phase selector is increased to twice the maximum superimposed current prevailing in the swing. Therefore, the phase selector resets once a power swing is detected. It can then be used to detect a fault during a power swing.

Detection of a fault during a power swing

A fault is detected during a swing when the phase selector operates, based on its increased threshold. Therefore, any operation of the phase selector will cause PSB unblocking, and allow a trip. Example scenarios are:

- A fault causes the delta current measured to increase above twice that stored during the swing (a step change in delta I rather than the expected gradual transition in a power swing).

Actions upon detection of a fault during a power swing (distance option only)

- The block signal is only removed from zones that start within 2 cycles of a fault being detected. This improves stability for external faults during power swings. Any measuring zone that was detecting an impedance within its characteristic before The phase selector detected the fault will remain blocked. This minimizes the risk of tripping for a swing impedance that may naturally be passing through Zone 1, and could otherwise cause a spurious trip if all zones were unblocked on fault inception. Any measuring zone that picks up beyond the two cycle window will remain blocked. This minimises the risk of tripping for a continued swing that may pass through Zone 1, and could otherwise cause a spurious trip if all zones were allowed to unblock together.

Power swing settings

The power swing detection is setting free aided with slow swing detection that uses zone 5 and does not require any system study. The only setting available to a user, apart from zone 5, is to decide whether a zone should be blocked or allowed to trip after a power swing is detected. Zone by zone, it is possible to select one mode from the following:

Allow Trip	should a power swing locus remain within a trip zone characteristic for a duration equal to the zone time delay, the trip will be allowed to happen;
Blocking	to keep stability for that zone, even if a power swing locus should enter it;
Delayed Unblock	maintains the block for a set duration. If the swing is still present after the “PSB Timeout Set” window has expired, tripping is allowed as normal.

Other setting possibilities are:

- Selection of PSB as “Indication” only will raise an alarm, without blocking any zones.
- The PSB Unblock Dly function allows for any power swing block to be removed after a set period of time. For a persistent swing that does not stabilise, any blocked zones will be made free to trip once the timer has elapsed. In setting which relays will unblock, the user should consider which relay locations are natural split points for islanding the power system.
- The PSB Reset Delay is a time delay on drop-off timer, which maintains the PSB detection even after the swing has apparently stabilised. It is used to ensure that where the swing current passes through a natural minimum and delta I detection might reset, that the detection does not drop out/chatter. It can therefore be used to ensure a continual Power Swing indication when pole slipping (an unstable out of step condition) is in progress.

A simplified logic diagram showing operation of the power swing blocking is shown below:

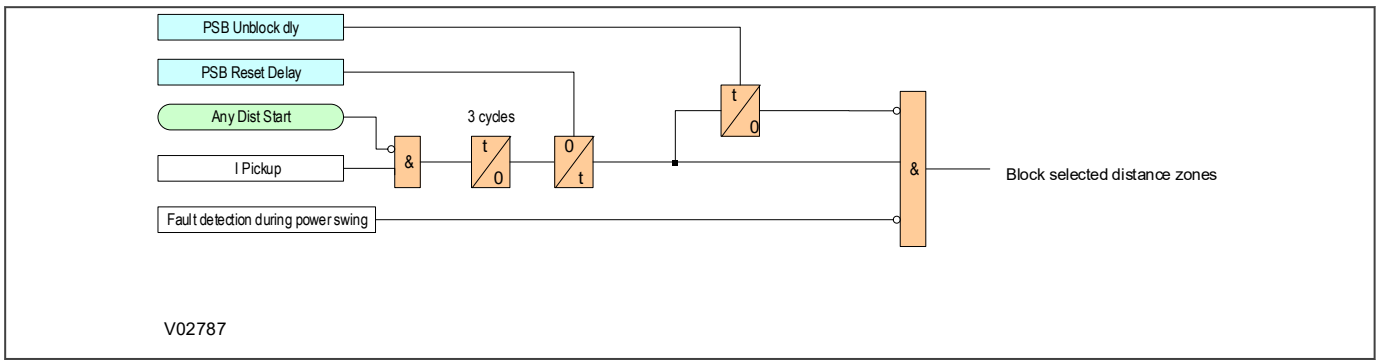


Figure 185: Power swing blocking Logic

Out of step detection and tripping

Out of Step protection is used to split the power system into possibly stable areas of generation and load balance during unstable power oscillations. The points at which the system should be split are determined by detailed system stability studies.

The 5th Generation Out of Step function has 4 different setting options:

1. Disabled
2. Predictive OST
3. OST
4. Predictive OST or OST

When set `Disabled`, Out of Step function is not operational. The 5th Generation also provides an option to split the system in advance by selecting the Predictive OST (sometimes called an early OST) in order to minimise the angle shift between two ends and aid stability in the split areas. The third setting option is to split the system on detection of the out of step condition i.e. when a pole slip occurs. The fourth option is a combination of the two.

Out of step detection

The Out of Step detection is based on the well proven $\Delta Z/\Delta t$ principle associated with two concentric polygon characteristic, as presented in the figure below.

Characteristic

Both polygon characteristics are independent and have independent settings for their respective reactance and resistive reaches.

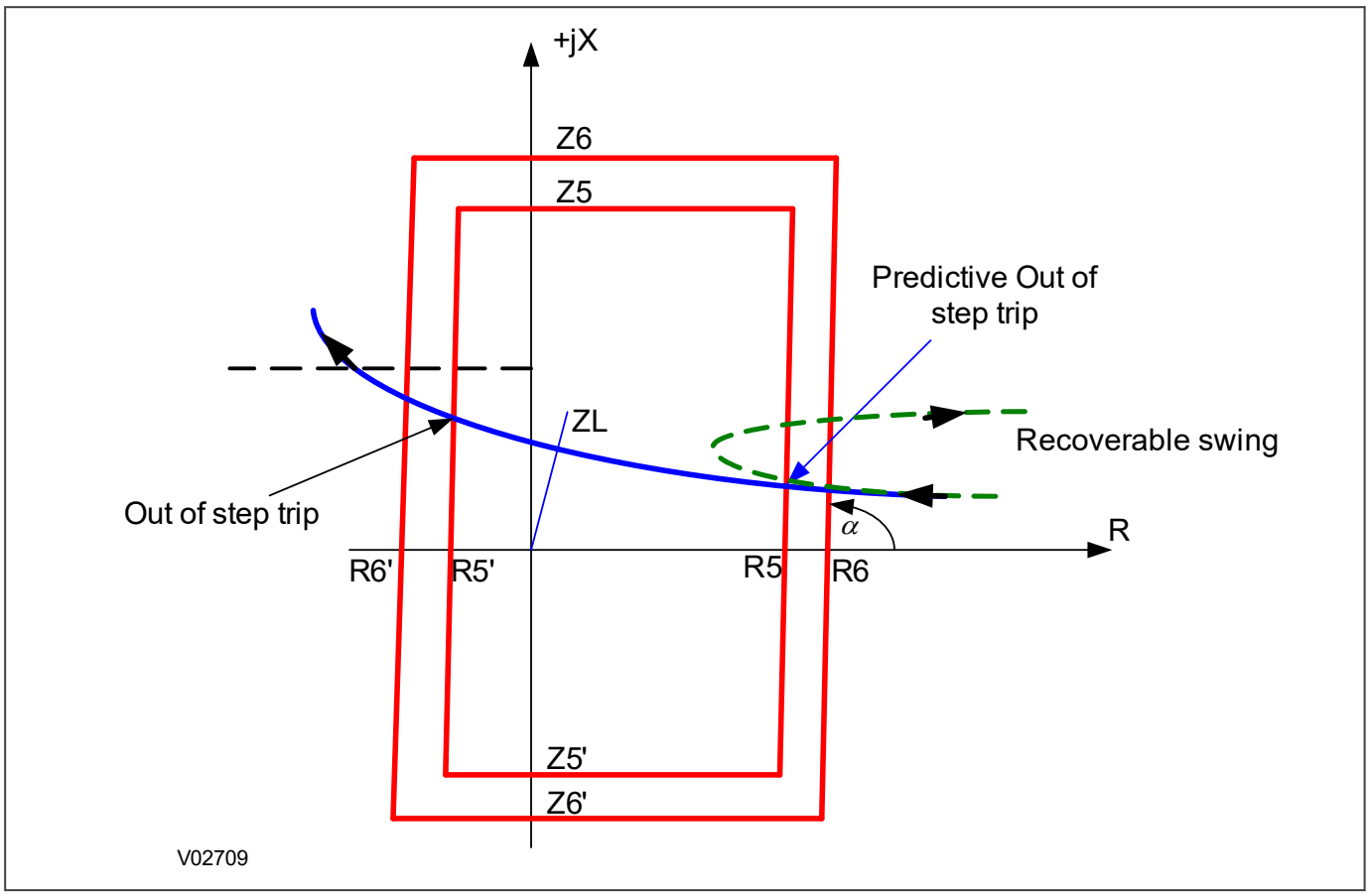


Figure 186: Out of step detection characteristic

Both the inner (Zone 5) and outer (Zone 6) characteristics, as shown above, are settable in positive sequence impedance terms to ensure correct Out of Step detection during open pole swing conditions. Hence, there is only one Z5 and Z6 positive sequence impedance polygon characteristic instead of 6 characteristics for each measured loop. The measured positive sequence impedance is calculated as:

Z1 = V1/I1

Where V1 and I1 are positive sequence voltage and current derived from the measured phase quantities. Note that during symmetrical power oscillations, there is no difference between phase impedance loops and positive sequence impedance loop, whilst for the open pole oscillations the phase and positive sequence impedances are different. This fact must be taken into account during testing/commissioning.

All four resistive blinders are parallel, using the common angle setting ‘α’ that corresponds to the angle of the total system impedance ZT (= ZS + ZL + ZR), where ZS and ZR are equivalent positive sequence impedances at the sending and receiving ends and ZL positive sequence line impedance. Tilting of the reactance line and residual compensation is not implemented.

In figure above, the solid impedance trajectory represents the locus for the non-recoverable power oscillation, also known as pole slip or out of step condition. The dotted impedance trajectory on the other hand represents a recoverable power oscillation, usually called swings.

Operating principle

The Out of Step detection algorithm is based on measuring the speed of positive sequence impedance passing through the set ΔZ region. As soon as measured positive sequence impedance touches the outer polygon, a timer is started.

If the disturbance takes less than 25 ms from entering zone 6 to entering zone 5, the relay will consider this to be a power system fault and not an out of step trip condition. The timer of 25 ms is a fixed timer in the logic and not user

accessible. During a power system fault, the speed of impedance change from a load to a fault is fast, but the relay may operate slower for marginal faults close to a zone boundary, particularly for high resistive faults inside the zone operating characteristic and close to the Z5 boundary. Therefore, the fixed time of 25 ms is implemented to provide sufficient time for a distance element to operate and therefore to distinguish between a fault and an extremely fast power system oscillation.

If the disturbance takes more than 25 ms but less than DeltaT set time from entering Zone 6 to entering Zone 5, this will be seen as a very fast oscillation. Therefore, the relay will trip if setting option 2 or 4 was selected. The minimum DeltaT setting is 30 ms, allowing 5 ms margin to the fixed 25 ms timer.

If the disturbance takes longer than the DeltaT setting time to enter Zone 5 after entering Zone 6 then it is considered as a slow power oscillation. On entering Z5, the relay will record the polarity of the resistive part of the positive sequence impedance. Two scenarios are possible:

1. If the resistive part of the positive sequence impedance leaves Z5 with the same polarity as previously recorded on entering Zone 5, it is deemed a recoverable swing. No tripping will be issued.
2. If the resistive part of the positive sequence impedance has the opposite polarity when exiting Zone 5 to that of the recorded polarity on Zone 5 entering, an Out of Step condition is recognised, followed by the tripping if setting option 3 or 4 was selected. It should be noted that in the case when the DeltaT timer did not expire and setting option 3 is selected, the Out of Step condition will also be detected, followed by OST operation.

As the tripping mode for the detected Out of Step condition is always 3 ph trip, the 'Predictive OST' and OST DDB signals are mapped to the 3ph tripping in the default PSL. Also, Out of Step operation will block auto-reclose function. The Out of Step tripping time delay TOST is also available to delay the OST tripping command until the angle between internal voltages between two ends are at 240 deg closing towards 360 deg. This is to limit the voltage stress across the circuit breaker. In the case of a fault occurring during the swing condition, the out of step tripping function will be blocked.

The Out of Step algorithm is completely independent from the distance elements and setting free power swing detection function. The load blinder does not have any effect on the OST characteristics. For the Out of Step operation, the minimum positive sequence current of 5%In must be present.

The Out of Step algorithm is given in the figure below.

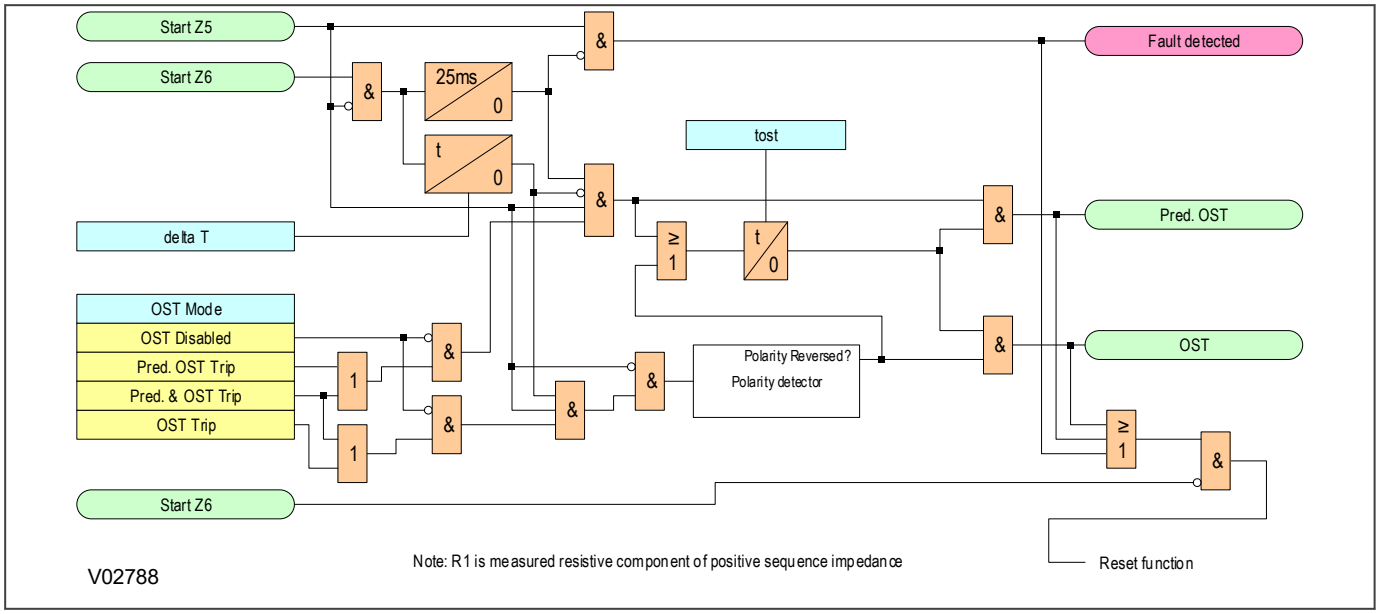


Figure 187: Out of Step Logic

11.3.2 DETECTION OF A FAULT DURING A POWER SWING

Faults are characterised by step changes in superimposed current (ΔI) rather than more gradual transitions symptomatic of a power swing.

When a power swing is in progress, the threshold for the phase selector is increased to a value twice that of the maximum prevailing superimposed current caused by the swing. A fault will cause a ΔI greater than this raised threshold, so the fault will be detected by the phase selector. Operation of the phase selector in this condition unblocks the PSB function, to allow tripping of Distance elements.

To provide stability for external faults, the blocking signal is only removed from zones that start within two cycles of the phase detector recognising the fault:

Any Distance element measuring an impedance inside its characteristic before the phase selector detects the fault remains blocked. This prevents tripping for a swing impedance that may be coincidentally passing through a fast-acting zone, and which could cause spurious tripping if all elements were unblocked without qualification.

Any Distance element that measures an impedance inside its characteristic after the two cycle ΔI window of the phase selector has expired, remains blocked. This prevents tripping for a continued swing that may pass through a fast acting zone which could cause spurious tripping if the element was allowed to unblock by an unqualified phase selector reset.

11.3.3 POWER SWING BLOCKING CONFIGURATION

To use the Power Swing function, you must ensure that the ***PowerSwing Block*** setting in the CONFIGURATION column is set to `Enabled`. You can set Power Swing Blocking to `Indication` (where alarms are raised but no blocking is imposed), or to Blocking (where blocking actions are imposed).

To define what the action the PSB function should take, you need to set the distance zones. The distance power swing zones for phase and earth are available under the *POWER SWING BLK.* column

The following options are available for each of the PSB zones:

`Allow Trip`: If a power swing locus stays in the Distance characteristic for a duration equal to the element time delay, the trip is allowed.

`Blocking`: Prevents tripping for that element, even if a power swing locus enters the element's characteristic.

`Delayed Unblock`: This maintains the block for a set duration after a power swing has been detected. To use it, you must set ***PSB Unblocking*** to `Enabled`, and then set the desired ***PSB Unblock dly*** time for removing the block.

> *Note:*
> *The **PSB Unblock dly** timer is common to all elements.*

The ***PSB Unblock dly*** is used to time the duration for which the swing is present. The intention is to allow the distinction between a stable and an unstable swing. If after the timeout period the swing has still not stabilised, the block for selected zones can be released (unblocking), giving the opportunity to split the system. If no unblocking is required, set to maximum (10 s).

There is a further timer associated with the PSB function. This is the ***PSB Reset Delay*** timer. This timer is provided to maintain the power swing detection for a period after the superimposed current detection (ΔI) has reset. ΔI naturally tends to zero twice during each power swing cycle (around the current maxima and minima in the swing element). A short time delay ensures continued PSB pick-up during these ΔI minima.

The ***PSB Reset Delay*** is used to maintain the PSB status when ΔI naturally is low during the swing cycle (near the current maxima and minima in the swing envelope). A typical setting of 0.2s is used to seal-in the detection until ΔI has chance to appear again.

The ***WI Trip PSB*** setting determines what will happen if a power swing is detected whilst the Weak Infeed (WI) tripping feature is being used and the WI condition is present for longer than the ***WI Trip Delay*** time. If `Blocking` is selected, the weak infeed operation will be disabled for the duration of the swing. If `Delayed Unblock` is chosen, the weak infeed element block will be removed after drop off timer ***PSB Unblock dly*** has expired, even if the swing is still present. This allows system separation when swings fail to stabilise. In `Allow trip` mode, the weak infeed element is unaffected by power swing detection.

11.3.4 POWER SWING LOAD BLINDING BOUNDARY

If the product has load blinding enabled, the following applies for phase-to-phase loops:

Impedance values, which are inside the load blinder boundaries and close to it for more than one cycle, are indicative of a power swing. The power swing region is represented by the shaded area in the following diagram.

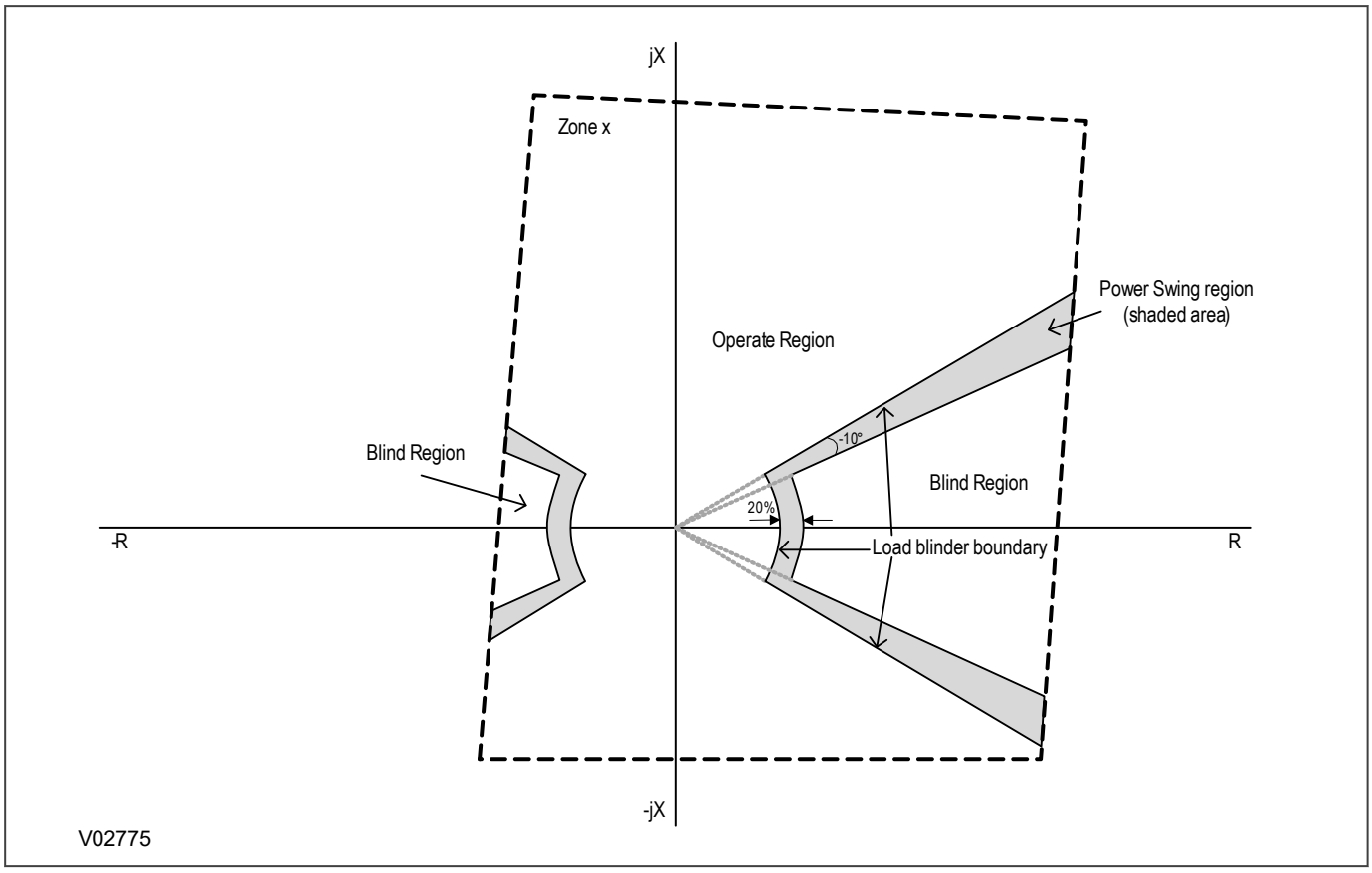


Figure 188: Load blinder boundary conditions

The area is defined by lines created with angles fixed at 10° closer to the resistive axis than those created by the load blinder angle setting (***Load/B Angle Ph*** and ***Load/B Angle Gnd*** -10°, shown in the shaded Power Swing region in the diagram above) and a circular arc with a radius concentric with, and equivalent to 20% greater than, the load blinder impedance setting (**Z< Blinder Imp Ph** and **Z< Blinder Imp Gnd** +20%, shown in the shaded Power Swing region in the diagram above).

Note:
This power swing conditions are completely independent of the slow swing associated with Zone 7 and Zone 8.

11.3.5 POWER SWING BLOCKING LOGIC

The Power Swing function follows the logic diagram below:

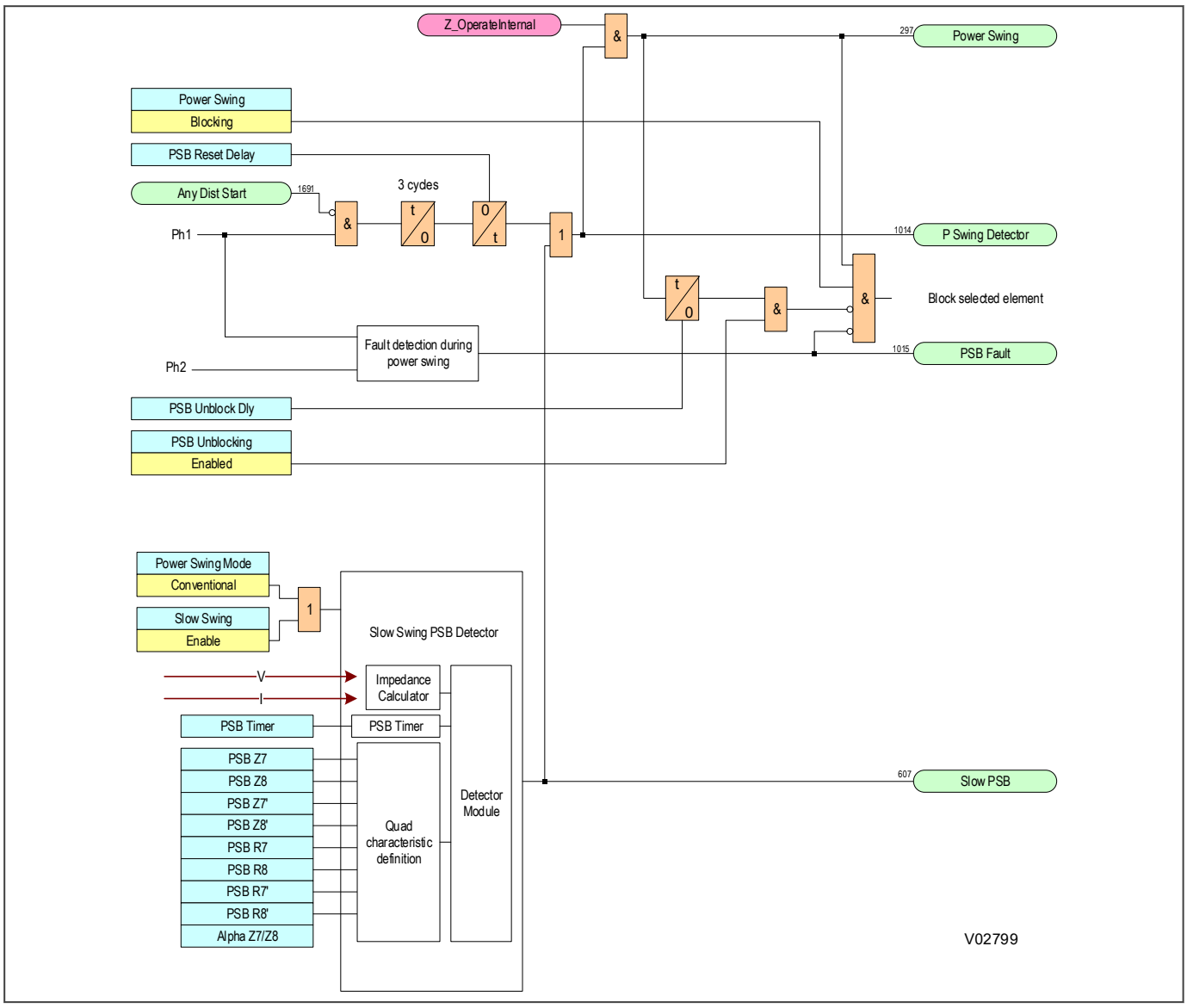


Figure 189: Power swing blocking logic

Note:
This is a simplified representation to highlight the outputs of the Power Swing Blocking function.

11.3.6 POWER SWING BLOCKING SETTING GUIDELINES

Power sing blocking (PSB) should normally only be enabled in transmission system applications. Power swings are not expected to occur at distribution level.

The main power swing detection technique used in this product can detect power swings faster than 0.5Hz without you having to set any parameters. This method relies on superimposed current (ΔI) component techniques to automatically detect power swings. The threshold to detect a power swing is 5%In. During power oscillations slower than 0.5Hz the continuous ΔI phase current integral to the detection technique may be less than the 5%In threshold. So it may not operate. Slow swings usually occur following sudden load changes or single pole tripping on weak systems where the displacement of initial power transfer is not severe. Generally, swings of up to 1Hz are recoverable, but the swing impedance may stay longer inside the Distance characteristics than might be expected before the oscillations are damped by the power system. Therefore, to guarantee system stability during very slow

swings, we recommend setting ***Slow Swing*** to `Enabled` to complement the automatic setting-free detection algorithm.

To configure the slow power swing function you need to set the resistive and reactive limits of the Zone 7 and Zone 8 quadrilaterals. You also need to set the ***PSB Timer*** which defines the critical time period of the transition between the two zones and which is characteristic of the slow swing.

Whichever power swing detector is responsible for applying PSB, the removal of PSB is defined by two settings – the ***PSB Reset Delay*** and (if an unblocking philosophy is employed) the ***PSB Unblock dly***.

11.3.6.1 SETTING THE RESISTIVE LIMITS

The Zone 7 quadrilateral should encompass all distance elements to be blocked during a power swing condition. The Zone 8 quadrilateral should be set smaller than the minimum possible load impedance. The security margin for both conditions should be at least 20%, also a margin of at least 10% should be provided between Zone 7 and Zone 8:

$$R8 > 1.1(R7)$$

We recommend setting the magnitudes of R7' and R8' equal to R7 and R8 respectively:

$$R7' = -R7,\ R8' = -R8.$$

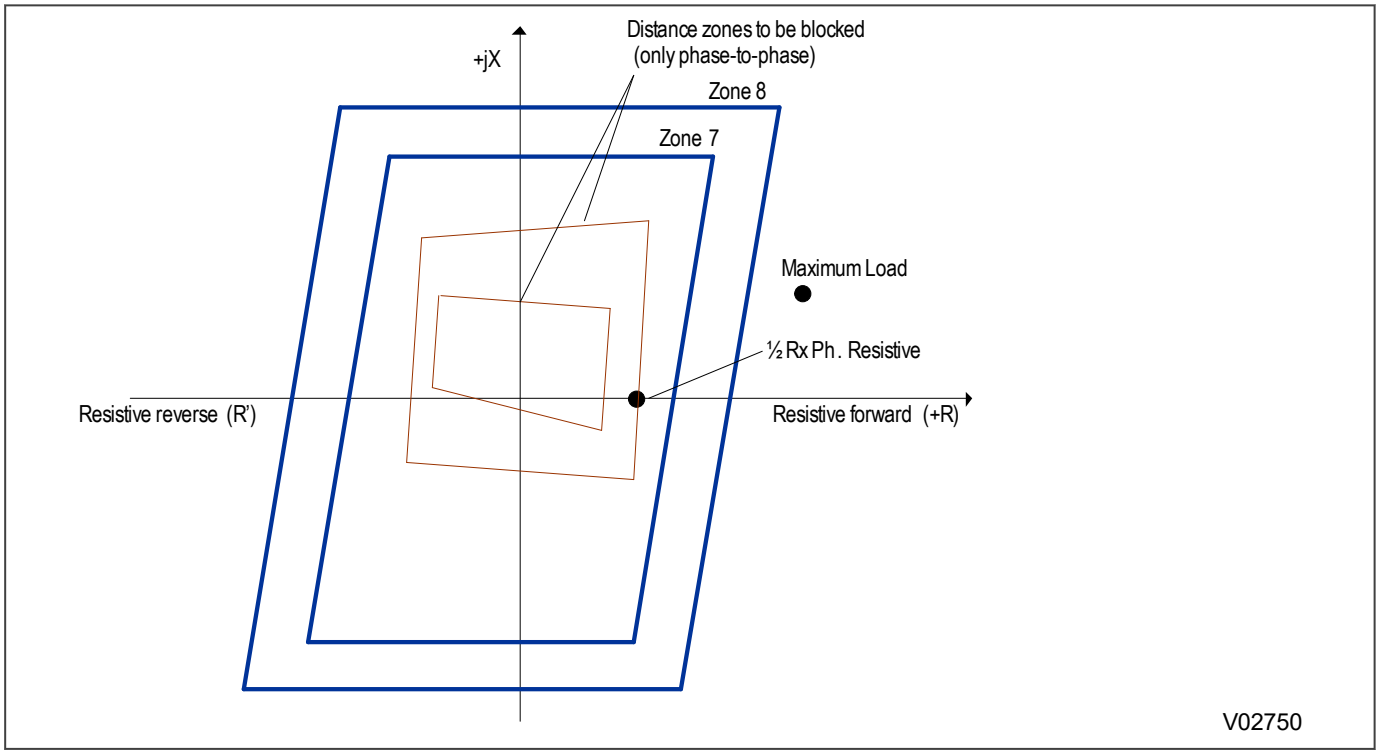


Figure 190: Setting the resistive reaches

11.3.6.2 SETTING THE REACTIVE LIMITS

The inner Zone 7 should be set in excess of total impedance Z_T , which include local source impedance Z_S , line impedance Z_L and remote source impedance Z_R. Only positive sequence impedances should be considered. The security margin for this condition should be at least 20%. The recommended margin between Z7 and Z8 settings is 10%:

$$Z8 = 1.1(Z7)$$

We recommend setting the magnitudes of Z7' and Z8' equal to Z7 and Z8 respectively

$$Z7' = -Z7,\ Z8' = -Z8$$

The angle Alpha should be set equal to the angle of the total impedance Z_T:

$$\alpha = \angle Z_T$$

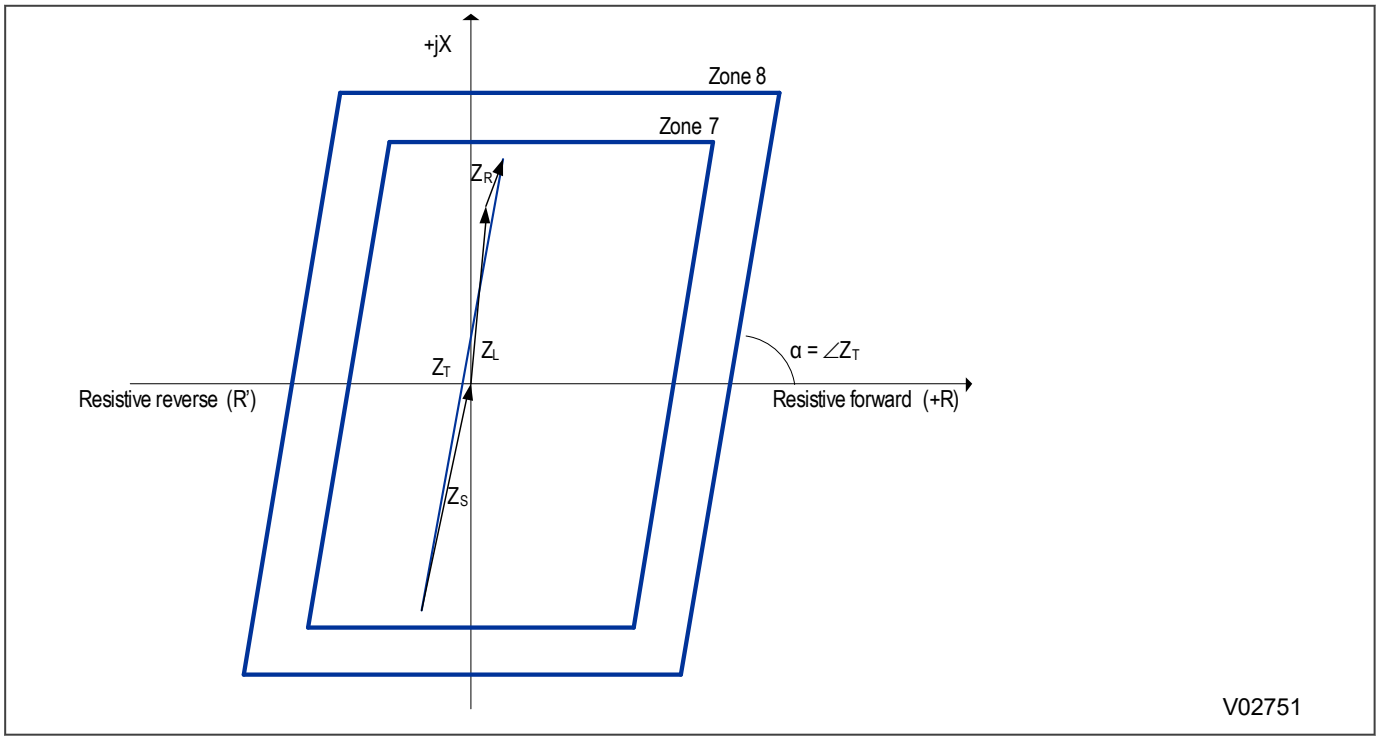


Figure 191: Reactive reach settings

11.3.6.3 PSB TIMER SETTING GUIDELINES

The Setting PSB Time setting can be calculated as follows:

$$\Delta t = \frac{(\theta_1 - \theta_2) \cdot f_{nom}}{f_{PS}}$$

where

- angles θ_1 and θ_2 are defined in the following figure
- f_{nom} is the nominal frequency
- f_{PS} is the maximum Power Swing frequency to be taken into account

Since any power swing with f_{PS} >= 0.5Hz can be detected by the setting-free delta current algorithm, only power swings with f_{PS} < 0.5Hz Hz need to be considered for Slow Power Swing detection. We recommended setting f_{PS} to 1Hz because this value provides sufficient security margin.

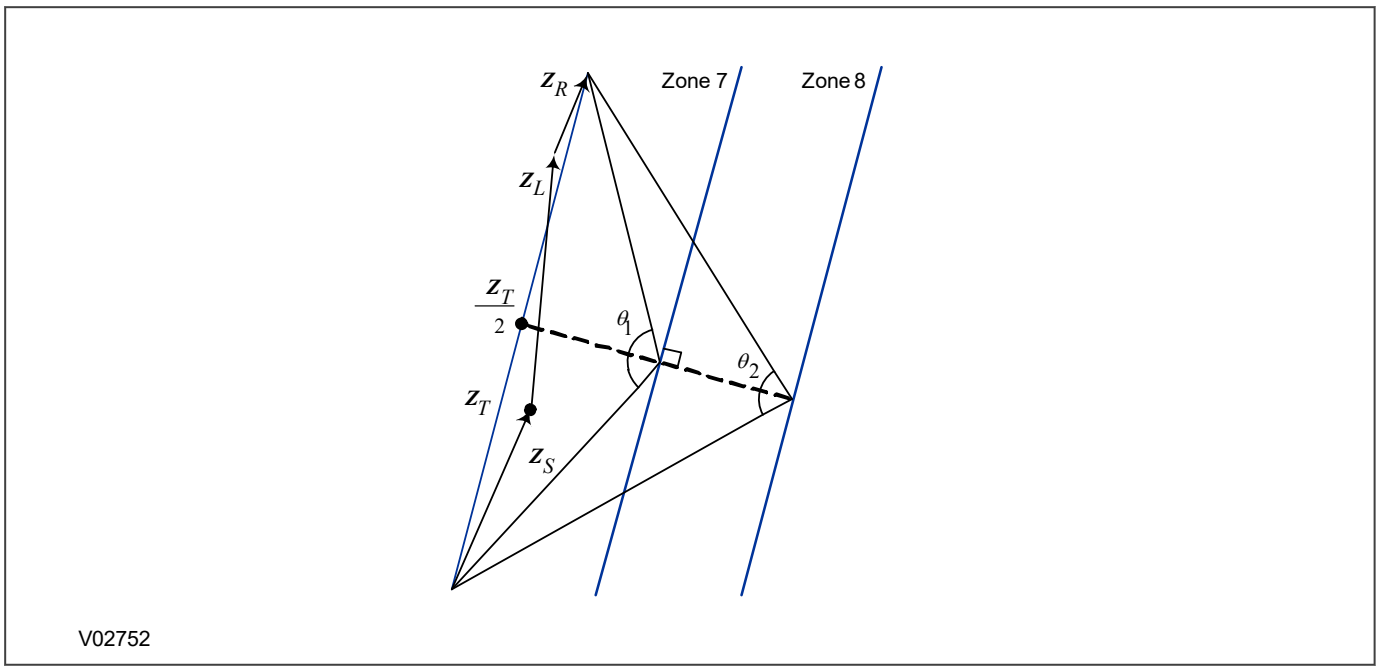


Figure 192: PSB timer setting guidelines

11.4 OUT OF STEP PROTECTION

Out-of-Step detection is based on the speed and trajectory of measured positive sequence impedance passing through a particular characteristic. During power system disturbances such as faults and power swings, measured impedance moves away from normal load values. Power swings, where the system voltage angles change relative to each other, can be either stable (recoverable) or unstable (non-recoverable). It is the unstable power swings that result in an Out-of-Step condition.

For stable power swings the relative phase angles will oscillate, but these oscillations will fade and synchronism between generating sources will be maintained. Detecting stable power swings is necessary to prevent unwanted tripping of impedance measuring protection elements if the swing impedance transiently passes through the fault impedance zone.

Unstable power swings (which can be destructive) result in sources of generation losing synchronism. This is called pole slipping. Detecting unstable power swings allows controlled tripping to split the systems into stable areas so that synchronism is maintained in each area. This is called Out-of-Step tripping (OOS or OST).

As well as tripping for Out-of-Step conditions, it is possible to predict OST conditions. This allows controlled tripping and consequent splitting of the system to recover stable operation before pole slipping occurs. This is called Predictive Out-of-Step tripping (Predictive OST).

Out-of-Step and Predictive Out-of-Step protection is based on changing impedance measurements, and uses a pair of configurable quadrilateral characteristics in the impedance plane (Zone 5 and Zone 6).

Out of Step protection is used to split the power system into more stable areas of generation and load balance during unstable power oscillations. The points at which the system should be split are determined by detailed system stability studies.

11.4.1 OUT OF STEP DETECTION

The Out of Step detection is based on the well proven $\Delta Z/\Delta t$ principle associated with two concentric polygon characteristic, as shown below:

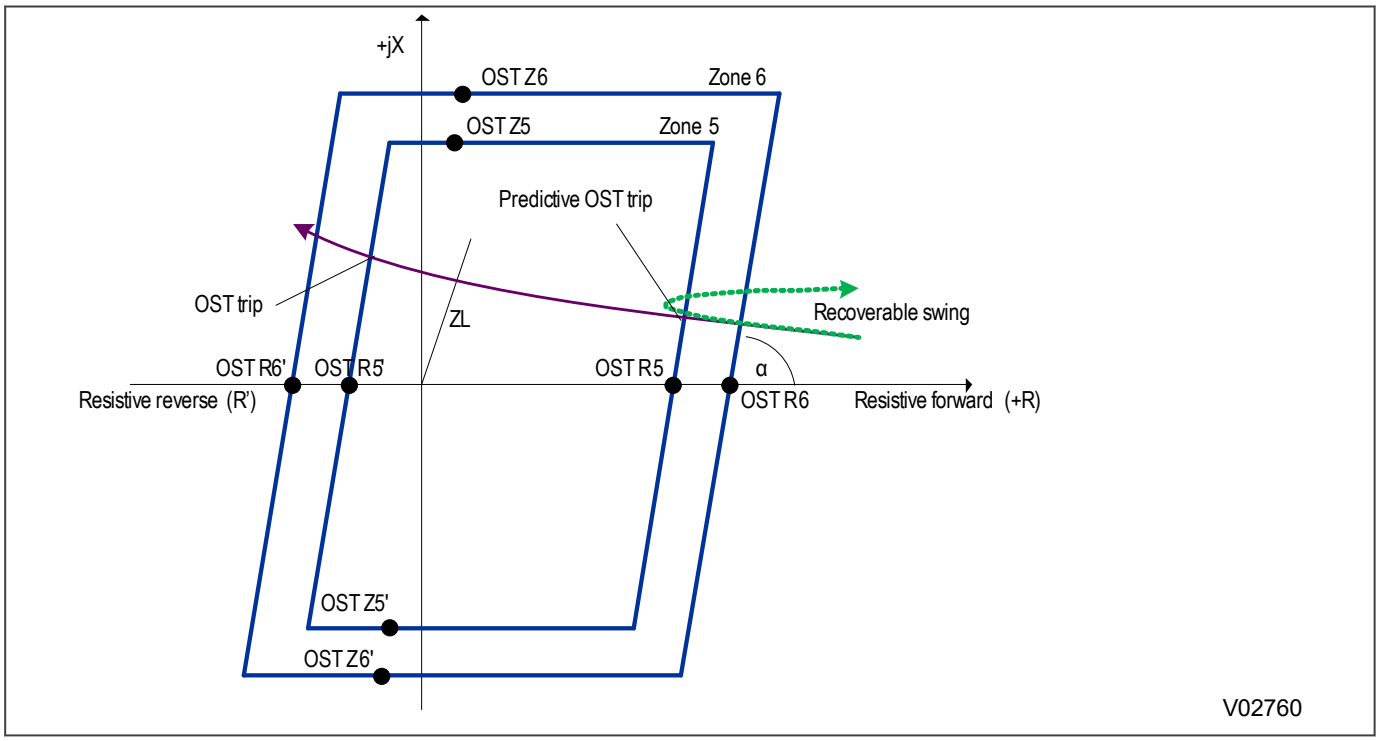


Figure 193: Out of step detection characteristic

The OST principle uses positive sequence impedances. The positive sequence impedance is calculated as $Z_1 = V_1/I_1$, where V_1 and I_1 are the positive sequence voltage and current quantities derived from the measured phase quantities. The concentric quadrilaterals are designated Zone 5 and Zone 6. Zone 5 encompasses possible system fault impedances and sits within Zone 6. Because OST and Predictive OST quadrilaterals are based on positive sequence impedances, all OST conditions are covered by a single measurement. Both quadrilaterals are independent and have independent reach settings.

All four resistive blinders are parallel, using the common angle setting (α) that corresponds to the angle of the total system impedance ($Z_T = Z_S + Z_L + Z_R$), where Z_S and Z_R are equivalent positive sequence impedances at the sending and receiving ends and Z_L positive sequence line impedance. The reactance lines are also parallel as neither reactance line tilting nor esidual compensation is implemented.

In the figure, the purple solid impedance trajectory represents the locus for the non-recoverable power sawing, known as a pole slip or Out Of Step condition. The dotted green impedance trajectory represents a recoverable power swing.

11.4.2 OUT OF STEP PROTECTION OPERATING PRINCIPLE

The Out of Step function has four different setting options, which are only visible if the ***PowerSwing Block*** is enabled in the *CONFIGURATION* column:

- `OST Disabled`: Disables the Out of Step function.
- `Pred. OST Trip`: Splits the system in advance. It minimizes the angle shift between two ends and aids stability in the split areas.
- `OST Trip`: Splits the system when an out of step condition is detected, which is when a pole slip occurs.
- `Pred. & OST Trip`: For this mode both methods are available, and the final trip condition is detected based on either of predictive method or OST Trip method.

The Out-of-Step detection algorithm is based on the speed of the positive sequence impedance passing through the characteristic. When the positive sequence impedance enters the outer quadrilateral (Zone 6) a timer is started. The timer is stopped after the positive sequence impedance passes through the inner quadrilateral (zone 5). Let us call this time the zone 6 to zone 5 transition time.

If this time is less than 25 ms, the protection considers this to be a power system fault, not an Out-of-Step condition. This 25 ms time is fixed and cannot be set. During a power system fault, the speed of change from a load impedance to a fault impedance is fast, but the protection may operate slower for marginal faults close to a zone boundary. This is particularly the case for high resistive faults inside the zone operating characteristic and close to the Zone 5 boundary. The fixed time of 25 ms is implemented to provide sufficient time for a distance element to operate and therefore to distinguish between a fault and an extremely fast power swing.

If the zone 6 to zone 5 transition time takes more than 25 ms but less than the set ***delta T*** time, this is treated as a very fast power swing and the protection will trip if either the `Pred. OST Trip` or the `Pred. & OST Trip` options are selected and the Out-of-Step tripping time delay (***Tost***) has expired. The minimum ***delta T*** setting is 30 ms, allowing 5 ms margin with the fixed 25 ms timer.

If the zone 6 to zone 5 transition time takes longer than the set ***delta T*** time, it is considered as a slow power swing. On entering Zone 5, the protection records the polarity of the resistive part of the positive sequence impedance. From this state, two outcomes are possible:

- If the resistive part of the positive sequence impedance leaves Zone 5 with the same polarity as previously recorded on entering Zone 5, it is considered to be a recoverable swing. In this case, the protection does not trip.
- If, when exiting Zone 5, the resistive part of the positive sequence impedance has the opposite polarity to that of the recorded polarity on entering Zone 5, an Out-of-Step condition is recognised. This is followed by tripping if either `Pred. OST Trip` or `Pred. & OST Trip` is selected.

As the tripping mode for the detected Out-of-Step condition is always three-phase, the ***Pred. OST*** and ***OST*** DDB signals are mapped to the three-phase tripping signal in the default programmable scheme logic.

The Out-of-Step tripping time delay (***Tost***), delays the OST tripping command until the angle between internal voltages between the two ends are at 240 degrees closing towards 360 degrees. This limits the voltage stress across the circuit breaker. If a fault occurs during the swing condition, the Out-of-Step tripping function is blocked.

The Out-of-Step algorithm is completely independent from the distance elements and the power swing detection function. The load blinder does not affect the OST characteristics. In common with other similar functions, a minimum positive sequence current of 5%In is needed for Out-of-Step operation.

11.4.3 OUT OF STEP LOGIC DIAGRAM

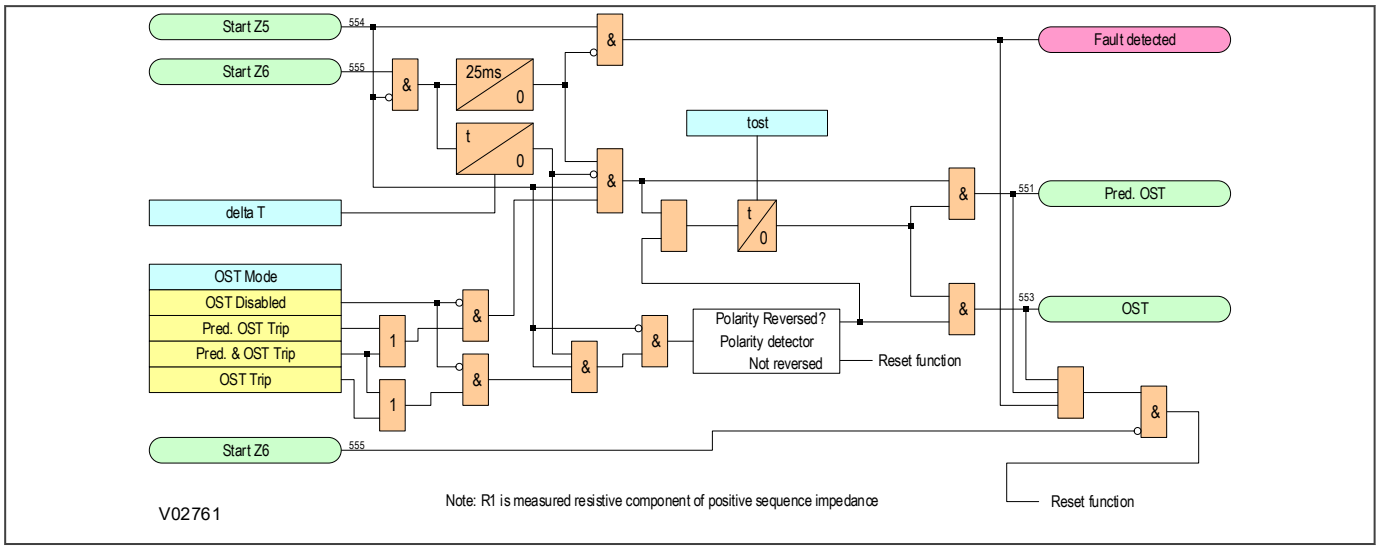


Figure 194: Out of step logic diagram

11.4.4 OST APPLICATION NOTES

This product provides integrated Out-of-Step protection, which avoids the need for a separate stand alone Out-of-Step device. This section provides guidance on how to configure Out of Step protection.

If you are going to use either of the *predictive* OST options (*Pred. OST Trip* or *Pred. & OST Trip)* you must conduct detailed system studies to determine accurate settings. This is because high setting accuracy is needed to avoid premature system splitting in the case of severe power oscillations that do not lead to pole slip conditions.

Using the *non-predictive* OST Trip setting is simpler. You can can set it by knowing just the total system impedance, Z_T, and the system split points.

11.4.4.1 SETTING THE OST MODE

The OST Mode setting provides four options:

- *OST Disabled*
- *Pred. OST Trip*
- *OST Trip*
- *Pred. & OST Trip*

Setting *OST Trip* is the most commonly used approach when this protection is applied. *OST Trip* should be used when Out-of-Step conditions are probable. If Out-of-Step conditions are detected, the OST command will be issued to split the system at the pre-determined points. A disadvantage of the *OST Trip* option compared with the 'Predictive' options is that tripping will take a little longer so that the power oscillations may escalate further after separation and the split parts may become separately unstable. An advantage, however, is that the decision to split the system will always be valid even if the accurate system data and setting parameters cannot be obtained.

The predictive setting options *Pred. OST Trip* and *Pred. & OST Trip* are recommended for systems where Out-of-Step conditions could possibly occur, and where an early system split should minimise the phase shift between generation sources. This should maximise the chances for the separated parts of the system to stabilise as quickly as possible. Special care must be taken when these settings are used to ensure that the circuit breakers at the different terminals do not open when the voltages at different ends are in anti-phase. This is because most circuit breakers are not designed to break current at double the nominal voltage. Attempting to break the current at double the nominal voltage could lead to flash-over and circuit breaker damage.

'Predictive' settings are designed to detect and trip for fast power oscillations. When predictive tripping is used with a circuit breaker capable of operating in typically two-cycles, the two voltages angles may rapidly move in opposite directions at the time of opening the circuit breaker. So, if you use the predictive settings you need to apply settings that will ensure that the circuit breaker opening occurs well before the phase difference between the different terminals approaches 180º. This means that accurate settings can only be determined by exhaustive system studies.

The setting *Pred. & OST Trip* provides two stages of OST. If a power system oscillation is very fast, the combination of ΔR (the difference between the Zone 5 and Zone 6 resistive reaches), and the ***Delta T*** settings, must be set so that *Pred. OST Trip* operates. If the oscillation is slower, the condition for the predictive OST is not met and so tripping is dictated by the OST condition being met. For the OST condition to be met, the resistive component of the impedance must leave Zone 5 with opposite polarity compared with when it entered. If the polarity is opposite when Zone 5 resets, OST will trip. If the polarity is the same when Zone 5 resets, OST will not trip. This distinguishes between a slower non-recoverable oscillation and recoverable swings.

You should disable OST for applications on lines where unrecoverable power oscillations are not expected, or not expected to be severe. This is likely to apply to strong interconnected systems operating with three-phase tripping.

11.4.4.1.1 DETERMINING THE LIMITS OF THE OST CHARACTERISTIC

The figure below shows the OST characteristic in conjunction with the system impedance, ZT, and particularly the relationship with the resistive reach of the Zone 5 element.

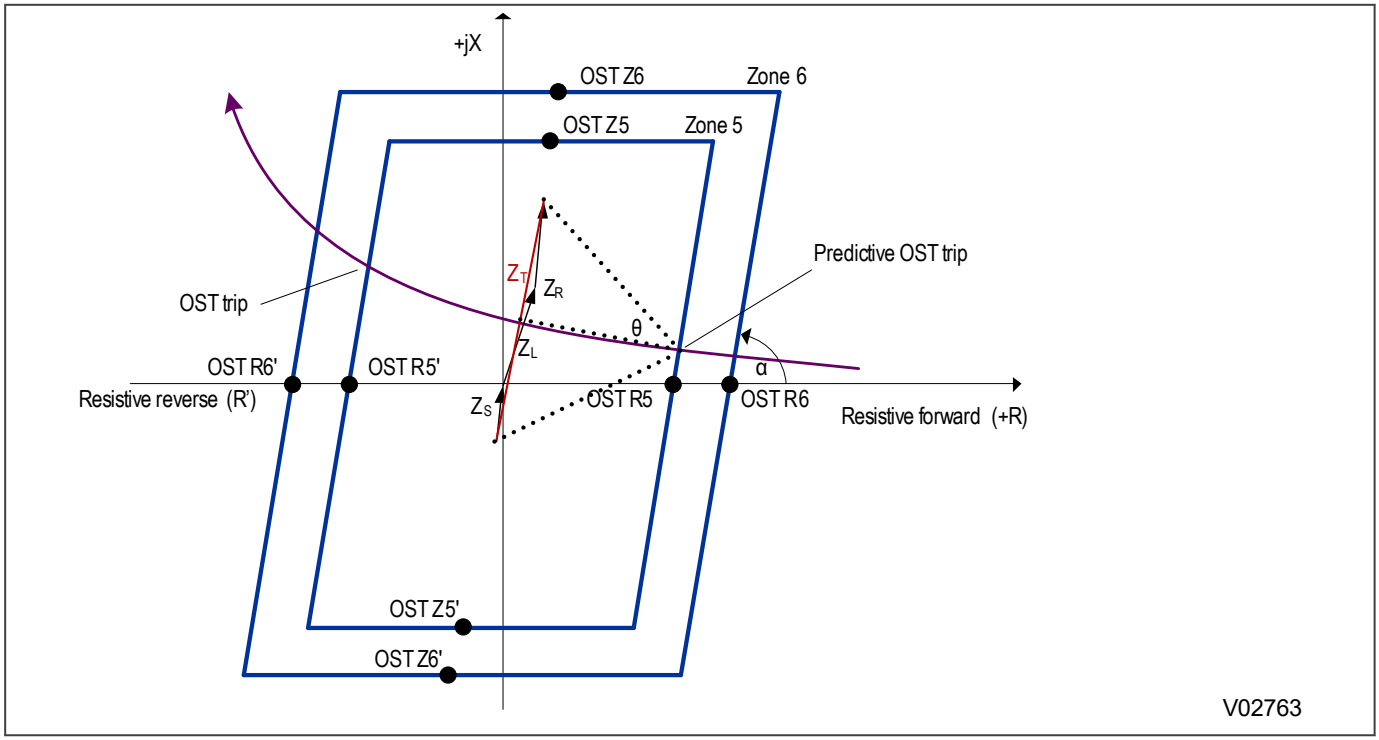


Figure 195: OST setting determination for the positive sequence resistive component OST R5

Z_T is the total system positive sequence impedance equal to $Z_S + Z_L + Z_R$, where Z_S and Z_R are the equivalent positive sequence impedances at the sending and receiving ends and Z_L is the positive sequence line impedance.

θ is the angular difference between the voltages at the sending and receiving ends beyond which no system recovery is possible.

To determine the settings for OST, the minimum inner resistive reach of OST R5 (R5min) needs to be calculated.

The figure above shows that:

$$R5min = (Z_T/2) / \tan(\theta/2$$

Next the maximum (limit value) for the outer resistive reach ***OST R6*** (R6 max) needs to be calculated. Referring to the figure below, point A must not overlap with the load area for the worst assumed power factor of 0.85 and the lowest possible Z_T angle α.

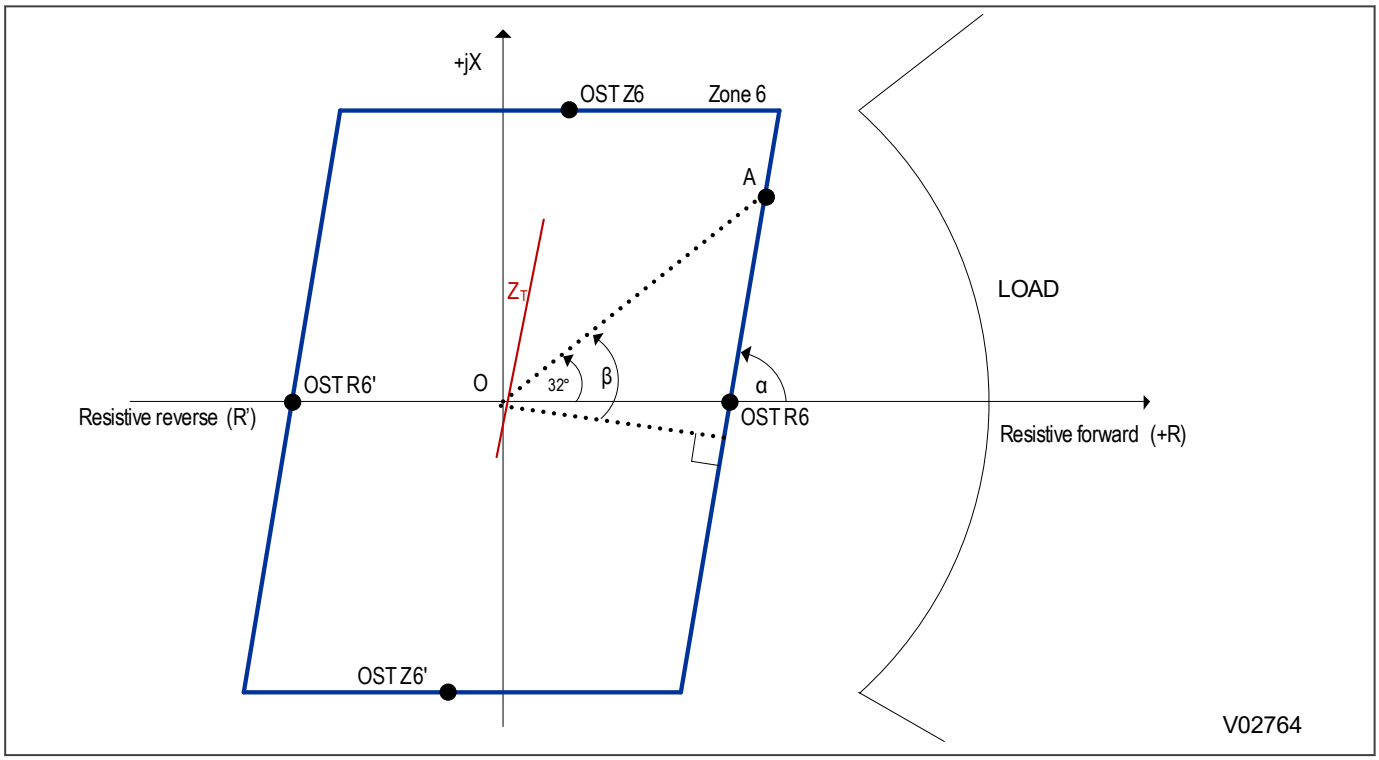


Figure 196: OST R6max determination

$$\beta = 32 + 90 - \alpha$$

$$Z \text{ load min} = OA$$

Where:

- Z load min is the minimum load impedance radius
- 32º is the load angle that corresponds to the lower power factor of 0.85
- α is the load blinder angle (Blinder Angle) that matches the Z_T angle

Therefore:

$$R6max < Z \text{ load min}(\text{Cos } \beta)$$

Starting from the limit values R5min and R6max, the actual ***OST R5*** and ***OST R6*** reaches will be set in conjunction with the ***Delta T*** setting.

Note:
The R6max reach must be greater than the maximum resistive reach of any distance zone to ensure correct initiation of the 25 ms and Delta T timers. However, the R5min reach could be set below the distance maximum resistive reach (inside the distance characteristic) if an extensive resistive coverage is required, meaning that Out-of-Step protection does not pose a restriction to the quadrilateral applications.

For each zone, we receommend setting the positive and negative limits to be the same so, OST R5' = OST R5, OST Z5' = OST Z5, OST R6' = OST R6, and OST Z6' = OST Z6.

11.4.4.1.2 SETTING OST Z5 AND OST Z6

Setting of the reactance lines ***OST Z5*** and ***OST Z6*** depends on how far from the protection location the power oscillations are to be detected. Normally, there is only one point for initial splitting of the system; and that point will be determined by system studies. For that reason, the Out-of-Step protection must be enabled at that location and disabled on all others. To detect the Out-of-Step conditions, the ***OST Z5'***, ***OST Z5***, ***OST Z6'***, and ***OST Z6*** settings must be set to comfortably encompass the total system impedance Z_T. A typical setting could be:

$$OST\ Z5 = OST\ Z5' = Z_T$$

The ***OST Z6*** and ***OST Z6'*** settings are not of great importance and could be set to 1.1 x ***OST Z5***.

11.4.4.1.3 SETTING OST R5, OST R6 AND DELTA T

The R5min and R6max settings determined above represent *limit* values. The actual ***OST R5*** and ***OST R6*** values need to be determined in relation to the ***Delta T*** timer.

Predictive OST setting

For the `Pred. OST Trip` setting, it is important to:

- Set ***OST R6*** equal to R6max
- Set ***OST R5*** as close as practical to R6max

The aim of pushing the ***OST R5*** setting to the right is to detect fast oscillations as soon as possible, in order to gain sufficient time to operate the breaker before the two source voltages are in opposite directions. The only restriction is the limitation of the ***Delta T*** minimum time delay of 30ms and the speed of oscillation.

You should set ***Delta T*** such that it does not expire after the positive sequence impedance has passed the ***OST R6*** – ***OST R5*** region.

For this setting, you need to know the rate-of-change of swing impedance when crossing the ***OST R6*** – ***OST R5*** region. This must therefore be based on system studies.

Note:
*You cannot assume that the rate-of-change of positive sequence impedance while crossing the **OST R6** – **OST R5** region is the same as the average rate-of-change of positive sequence impedance for the whole swing cycle. A false assumumption could lead to incorrect predictive OST operation.*

Note:
*For a fault, the **OST R6** – **OST R5** region will be crossed faster than 25ms, therefore even very fast oscillations up to 7Hz will not be mistaken as a fault condition and predictive OST will not operate.*

OST setting

For the `OST Trip` setting option, such a precise setting of the blinders and ***Delta T*** is not necessary. This is because for a wide ΔR region and a short ***Delta T*** setting, any oscillation will be successfully detected. However, the fault impedance must pass through the ΔR region faster than the ***Delta T*** setting.

Therefore, for the *OST Trip* setting, assume that θ = 120° and set:

- ***OST R5*** = ***OST R5'*** = R5min = Z_T/3.46
- ***OST R6*** = ***OST R6'*** = R6max
- ***Delta T*** = 30 ms

Delta T always expires. Therefore, the setting value given above will secure the detection of a wide range of oscillations, starting from very slow oscillations (caused by recoverable swings) up to a fastest oscillation limit of 7Hz. Note that any fault impedance will pass the ***OST R6*** – ***OST R5*** region faster than the minimum settable ***Delta T*** time of 30ms.

Predictive and OST setting

The recommendations for *Pred. & OST Trip* are the same as for *Pred. OST Trip*.

11.4.4.1.4 SETTING THE OST TIME DELAY

For either of the predictive OST settings, the OST time delay setting (***Tost***) must be set zero.

For the *OST Trip* setting, ***Tost*** would normally be set to zero, but if you want to operate the breaker at an angle closer to 360º (when voltages are in phase) you could apply a time delay.

11.4.4.1.5 BLINDER ANGLE SETTING

Set ***Angle Z5/Z6***, α, the same as the total system impedance angle, Z_T.

11.4.4.1.6 OST FOR SERIES COMPENSATED LINES

The maximum phase currents during an Out-of-Step condition rarely exceed 2In, which corresponds to the minimum swing impedance passing through Zone 1. Since the Metal-Oxide Varistors (MOV) bypass level is normally set between 2-3In, they will not operate during the power oscillations and therefore in the majority of applications they will not make any impact on Out-of-Step operation.

In the worst case, power oscillations are triggered on fault clearance on a parallel line. Approximately twice the load current starts flowing through the remaining circuit. This increases further and eventually exceeds the MOV threshold. The ***OST R6*** - ***OST R5*** region is usually set far from Zone 1, therefore it is unlikely that the positive sequence impedance's trajectory can traverse in and out of the set ΔR region due to the operation of MOVs. If MOVs do operate in the ΔR region, a timer that has been initiated may reset and be reinitiated, or the impedance may remain in the ΔR region for slightly longer. This is because resistive and capacitive components are added to the measured impedance during MOV operation as shown in the figure below. This effect may have an impact on the ***Delta T*** measurement if the *Pred. OST Trip* setting is used. If the recommendation to set R5min as close as practically possible to R6max is followed, it is unlikely that the swing currents will exceed the MOV threshold in the ΔR region. If a study shows that the MOVs could operate within the ΔR region, we recommend setting *Pred. & OST Trip* operating mode to cover all eventualities.

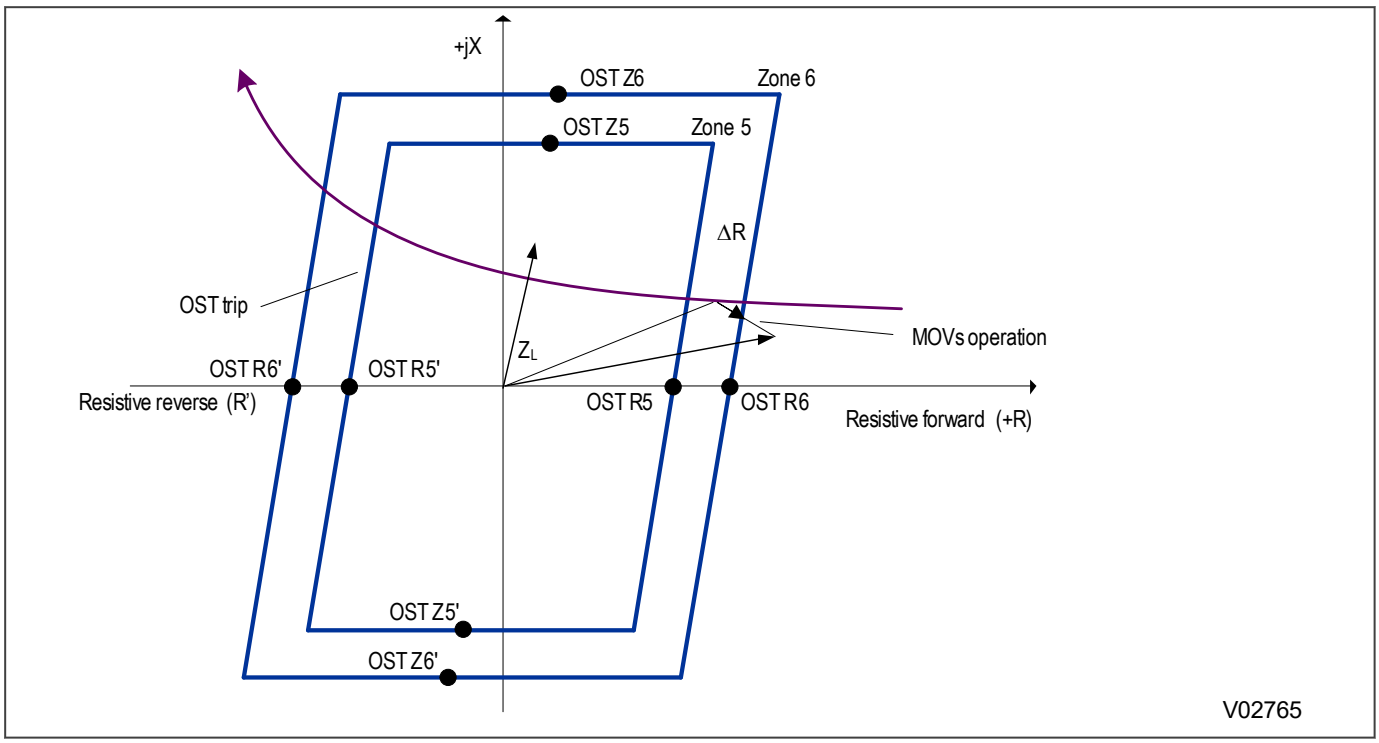


Figure 197: Example of timer reset due to MOVs operation

Note:
*If the **OST Trip** setting is chosen, the timer when triggered, will eventually expire as the power oscillations progress, therefore the MOV operation will not have any impact on Out-of-Step operation.*

11.4.4.2 POWER SWING ALARMING AND BLOCKING

The PSB technique employed in the 5th Generation has the significant advantage that it is adaptive and requires no user-set thresholds in order to detect swings faster than 0.5 Hz. The PSB relies on the delta techniques internal to the relay, which automatically detect swings. During the power oscillations slower than 0.5 Hz the continuous ΔI phase current integral to the detection technique for swing conditions may fall below the sensitive threshold of ΔI=0.05 In therefore may not operate. These slow swings will usually occur following sudden load changes or single pole tripping on the weaker systems where the displacement of initial power transfer is not severe. The slow swings of up to 1 Hz are by its nature recoverable swings but the swing impedance may stay longer inside the distance characteristics until the oscillations are damped by the power system. Therefore, to guarantee system stability during very slow swings it is recommended to set a blinder to complement the automatic, setting free detection algorithm. Zone 5 is used as a blinder for slow swing detection as well as for the Out of Step (OST) protection described in the next section. Zone 5 settings are therefore visible even if OST protection is disabled. The slow swing condition will be declared if positive sequence impedance is detected inside zone 5 for more than a cycle without phase selection operation. The slow swing detection operates in parallel to automatic swing detection mechanism.

No system calculation is needed for zone 5 setting, it is only important to set zone 5 smaller than the minimum possible load impedance with a security margin:

In case the OST is enabled the R5, R5', Z5 and Z5' settings will be adequate for very slow swing detection. If, however, the OST protection is disabled, set:

R5=R5'=0.85 x Z<

Z5=Z5'=2 x Zline

where Z< is load blinder radius.

The user decides which zones are required to be blocked.

Two timers are available:

The ***PSB Reset Delay*** is used to maintain the PSB status when ΔI naturally is low during the swing cycle (near the current maxima and minima in the swing envelope). A typical setting of 0.2 s is used to seal-in the detection until ΔI has chance to appear again.

The ***PSB Unblock Dly*** is used to time the duration for which the swing is present. The intention is to allow the distinction between a stable and an unstable swing. If after the timeout period the swing has still not stabilised, the block for selected zones can be released (“unblocking”), giving the opportunity to split the system. If no unblocking is required at the location of this relay, set to maximum (10 s).

PSB can be disabled on distribution systems, where power swings would not normally be experienced.

11.4.4.3 CRITICAL STABILITY ANGLE

What is the angle between two ends when a power system oscillation could be declared as a pole slip?

Consider the power angle curves shown in the figure below.

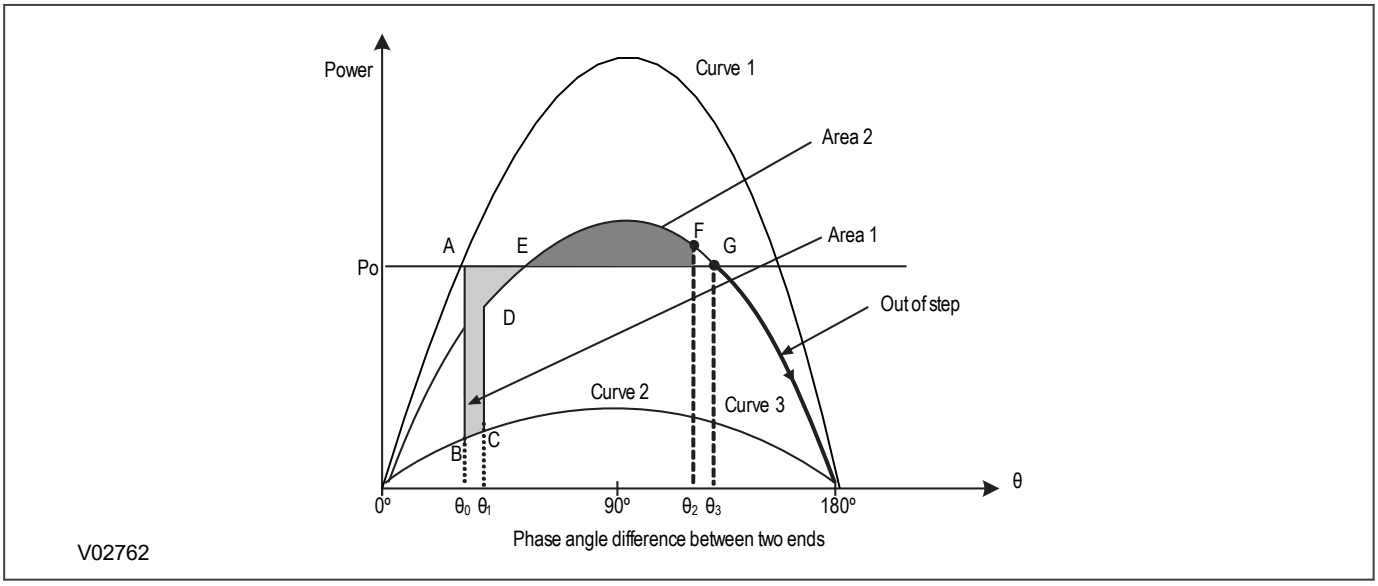


Figure 198: Power transfer in relation to angle difference θ between 2 ends

The figure above represents power angle curves, with no AR being performed, as follows:

Curve 1 - Pre-fault system operation via parallel lines where transmitted power is Po

Curve 2 - Transmitted power significantly reduced during two-phase to ground fault

Curve 3 - New power curve when the parallel line is tripped (fault cleared)

It can be seen that at a fault instance, the operating point A moves to B, with a lower transfer level. There is therefore a surplus of power ΔP=AB at the sending end and the corresponding deficit at the receiving end. The sending end machines start to speed up, and the receiving end machines to slow down, so phase angle θ increases, and the operating point moves along curve 2 until the fault is cleared, when the phase angle is θ1. The operating point now moves to point D on curve 3 which represents one line in service. There is still a power surplus at the sending end, and deficit at the receiving end, so the machines continue to drift apart and the operating point moves along curve 3. If, at some point between E and G (point F) the machines are rotating at the same speed, the phase angle will stop increasing. According to the Equal Area Criterion, this occurs when area 2 is equal to area 1. The sending end will now start to slow down and receiving end to speed up. Therefore, the phase angle starts to decrease and the operating point moves back towards E. As the operating point passes E, the net sending end deficit again becomes a surplus and the receiving end surplus becomes a deficit, so the sending end machines begin to speed up and the receiving end machines begin to slow down. With no losses, the system operating point

would continue to oscillate around point E on curve 3, but in practise the oscillation is dumped, and the system eventually settles at operating point E.

To resume, if area 1<area 2, the system will stay in synchronism. This swing is usually called a recoverable power swing. If, on contrary, the system passes point G with a further increase in angle difference between sending and receiving ends, the system drifts out of synchronism and becomes unstable. This will happen if the initial power transfer Po was set too high in the figure above, so that the area 1 is greater than area 2. This power swing is not recoverable and is usually called out of step or out of synchronism or pole slip condition. After this, only system separation and re-synchronising of the machines can restore normal system operation.

In the figure above, the point G is shown at approximately 120° deg, but it is not true in all cases. If, for example the pre-fault transmitted power (Po) was too high and if the fault clearance was slow, the area 1 will be greater so for the system to recover the angle θ would be close to 90 deg. On contrarily, if the pre-fault transmitted power Po was low and fault clearance fast, the area 1 will be small, so that based on area comparison, the angle θ could go closer to 180 deg and the system will still remain stable.

The actual angle difference at which system will become unstable could only be determined by a particular system studies, but for the purpose of settings recommendation where ‘OST’ setting is selected, the typical angle beyond which system will not recover is assumed to be 120 deg.

Setting option recommendation

The relay provides 4 different setting options:

1. Disabled
2. Predictive OST
3. OST
4. Predictive OST or OST

Set Option 1 on all lines except the line where tripping due to unrecoverable power oscillations is required or for the system where power oscillations are not severe - mainly in well interconnected systems operating with 3 phase tripping.

Setting Option 2 (and 4) is the best setting option from the system point of view, perhaps not being widely used in the past. Some utilities prefer an early system split to minimise the angle shift between ends and maximise the chances for the remaining two halves to stabilise as quickly as possible. Special care must be taken when this method is applied to ensure that the actual circuit breaker opening does not occur when the internal voltages at two ends are in anti phase. This is due to the fact that most breakers are not designed to interrupt at double nominal voltage and any attempt to break at that point would lead to flash over and possible circuit breaker damage. The fact is that setting Option 2 (and 4) will be mainly applied do detect and trip fast power oscillations. When this is coupled with a typical 2 cycle circuit breaker operating time, the two voltages angles may rapidly move in opposite directions at the time of opening the circuit breaker. Therefore, if this setting option is chosen, the above facts must be taken into account so that the actual CB opening must occur well before the angle difference between two ends approaches 180 degrees. On that basis, accurate settings have to be determined based on exhaustive system studies.

Setting Option 3 is the most commonly used approach. Once the Out of Step conditions are detected, the OST command will split the system at pre-determined points. The slight disadvantages of this method in comparison to Option 2 (and 4) is that the power oscillation will escalate further, thus causing more difficulties for the split parts to remain stable but the advantage is that the timing of the circuit breaker operation (‘tripping angle’) is easily controlled and the decision to split the system will be correct even if errors were made in the system data and setting parameters. This extra security is achieved by measuring and confirming the change of polarity of the resistive part of positive sequence impedance on zone 5 exit (reset).

Setting Option 4 provides 2 stages of Out of Step detection and tripping. If the power system oscillation is very fast, the combination of ΔR and Delta t setting (as discussed below) must be set in such a way that ‘Predictive OST’ operates. If however the oscillation is slower, the condition for the ‘Predictive OST’ will not be met and the ‘OST’ will operate later upon Z5 reset, providing that the change in polarity of the resistive component was detected. This is to distinguish between a slower non-recoverable oscillation and recoverable swings.

Blinder limits determination

Consider the Out of Step characteristic versus angle θ between two ends.

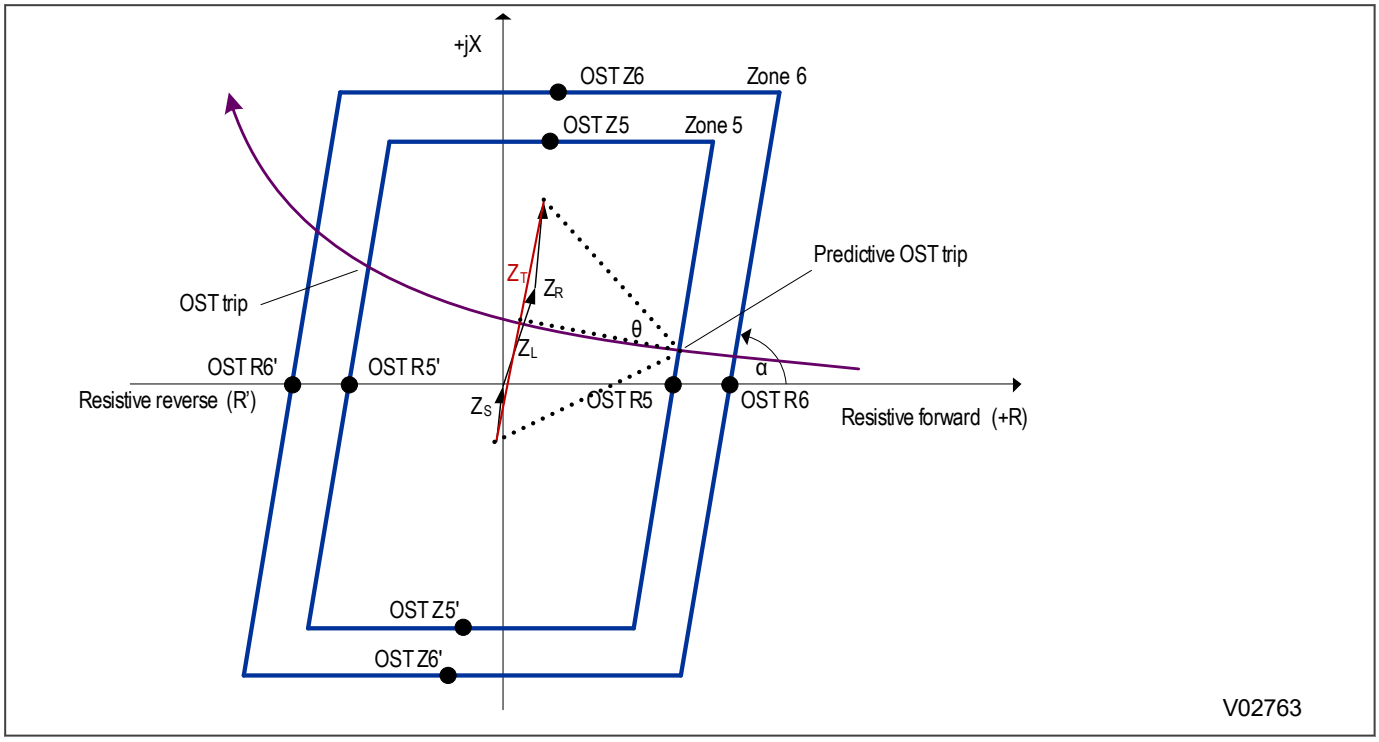


Figure 199: Setting determination for the positive sequence resistive component R5

Firstly, determine the minimum inner resistive reach R5.

The figure above shows:

$$R5\min = \frac{\frac{ZT}{2}}{\tan^{\angle}/_{2}}$$

Where ZT is a total system positive sequence impedance that equals to ZS + ZL + ZS, where ZS and ZR are equivalent positive sequence impedances at the sending and receiving ends and ZL positive sequence line impedance. ‘θ’ is an angle difference between the internal voltages at sending and receiving ends beyond which no system recovery is possible.

The next step is to determine the maximum (limit value) for the outer resistive reach R6. It must be insured that Point A in Figure 8 does not overlap with the load area for the worst assumed power factor of 0.85 and the lowest possible ZT angle .α

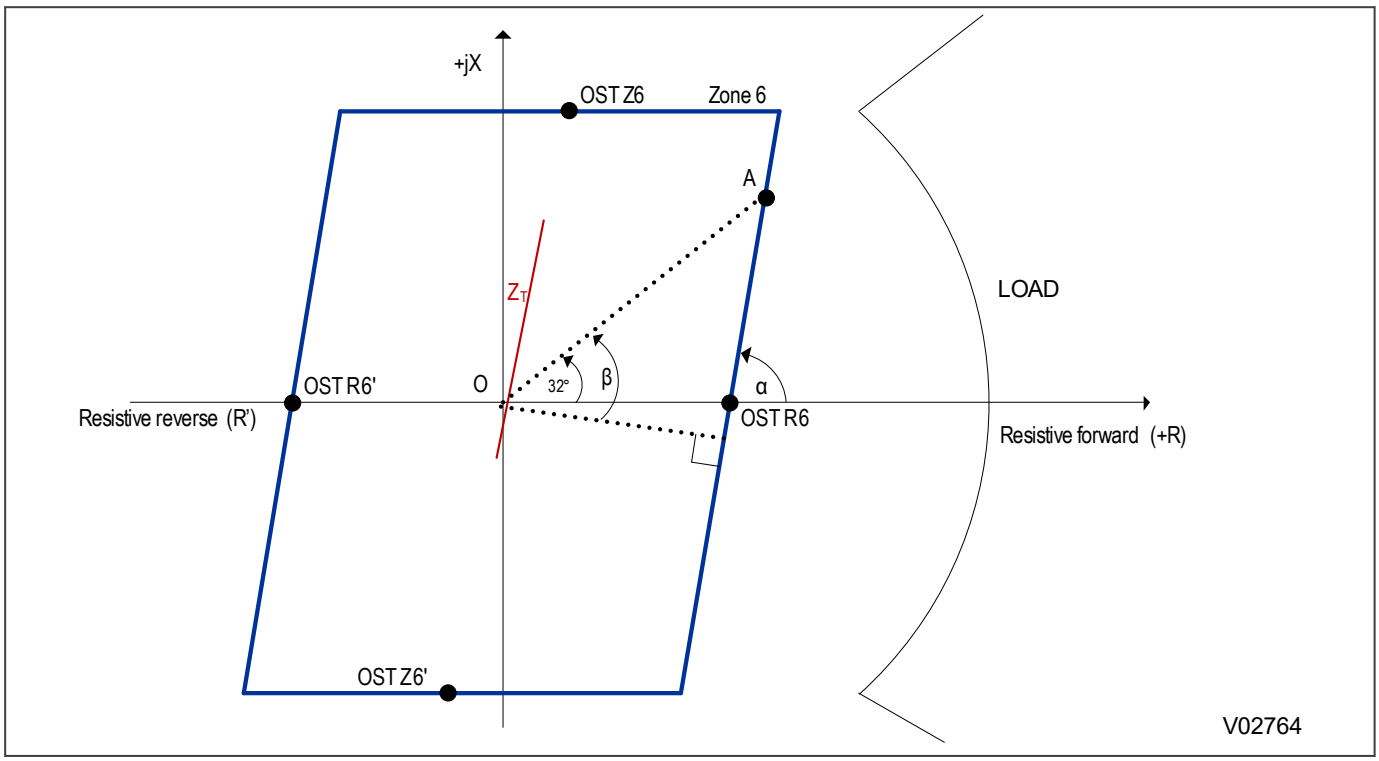


Figure 200: $R6_{MAX}$ determination

$\beta = 32 + 90 - \alpha$

Z load min = OA

$R6_{MAX} <$ Zload min x cos β

Where:

- Zload min is the minimum load impedance radius calculated above which already has built in sufficient margin
- 32 deg is the load angle that corresponds to the lower power factor of 0.85
- 'α' is the load blinder angle that matches ZT angle

The setting of negative resistance R5' should equal the R5 to accommodate the 'load import' condition. Starting from the limit values $R5_{MIN}$ and $R6_{MAX}$ the actual R5 and R6 (including the corresponding R5' and R6') reaches will be set in conjunction with the 'Delta t' setting below.

Note:
$R6_{MAX}$ reach must be greater than the maximum resistive reach of any distance zone to ensure correct initiation of the 25 ms and 'Delta t' timers. However, the R5MIN reach could be set below the distance maximum resistive reach (inside the distance characteristic) if an extensive resistive coverage is required, meaning that Out of Step protection does not pose a restriction to the quad applications.

Setting of reactance lines Z5 and Z6 will depend on how far from the relay location the power oscillations are to be detected. Normally, there is only one point where the system is to be initially split and that point will be determined by system studies. For that reason, the Out of Step protection must be enabled at that location and disabled on all others. To detect the Out of step conditions, the Z5'-Z5 and Z6'-Z6 setting must be set to comfortably encompass the total system impedance ZT, as shown in the figure above Typical setting could be:

Z5 = Z5' = 1/2 x 2 ZT = ZT

The Z6 and Z6' setting is not of great importance and could be set to Z6 = Z6' = 1.1 x Z5

Delta t, R5 and R6 setting determination

The $R5_{MIN}$ and $R6_{MAX}$ settings determined above are only limit values, the actual R5 and R6 need to be determine in relation to the 'Delta t' timer.

Predictive OST setting:

For the 'Predictive OST' setting it is important to:

- Set R6 (and R6') equal to $R6_{MAX}$
- Set R5 as close as practical to $R6_{MAX}$

The aim of pushing the R5 setting to the right is to detect the fast oscillation as soon as possible to gain sufficient time to operate the breaker before the two source voltages are in opposite direction. The only restriction would be the limitation of the 'Delta t' minimum time delay of 30 ms and the speed of oscillation. Set 'Delta t' so that the following condition is satisfied:

Note:
'Delta t' does not expire after positive sequence impedance has passed the R6-R5 region

For this setting, knowledge of the accurate rate of change of swing impedance when crossing the R6-R5 region is essential and therefore must be based on system studies.

Assumption that the rate of change of the positive sequence impedance during crossing the R6-R5 region is average rate of change for the whole swing cycle is wrong and could easily lead to incorrect 'Predictive OST' operation.

Note:
For the fault, the R6-R5 region will be passed faster than 25 ms, therefore even very fast oscillations of 7 Hz will not be mistaken with the fault condition and 'Predictive OST' will not operate.

OST setting:

For the 'OST' setting option the precise setting of blinders and 'Delta t' is not necessary. This is based on the fact that:

The wider the ΔR region and the shorter the Δt setting, any oscillation will be successfully detected. The only condition is that the fault impedance must pass through the ΔR region faster than Δt setting.

Therefore, for the 'OST' setting assume that $\theta = 120°$ and set:

- R5 = R5' = $R5_{MIN}$ = ZT/3.46
- R6 = R6' = $R6_{MAX}$
- Delta t = 30 ms

The point is that 'Delta t' always expires, therefore the above setting will secure the detection of a wide range of oscillations, starting from very slow oscillations caused by recoverable swings up to the fastest oscillation of 7 Hz. It should be noted that any fault impedance will pass the R6-R5 region faster than the minimum settable 'Delta t' time of 30 ms.

Predictive OST or OST setting:

As per 'Predictive OST' above.

Tost (trip delay) setting

Tost must be set zero for setting Option 2 and 4 above.

For setting Option 3, Tost should normally be set to zero. It is only the case if a user wants to operate breaker at the angle closer to 360 degrees (when voltages are in phase) when time delay could be applied.

Blinder angle setting

Set blinders angle 'α' same as total system impedance ZT angle.

Out of step operation on series compensated lines

The maximum phase currents during out of step condition rarely exceed 2xIn RMS, which corresponds to the minimum swing impedance passing through zone 1. Since the Metal-Oxide Varistors (MOV) bypass level is normally set between 2-3In, they will not operate during the power oscillations and therefore in majority of applications will not make any impact on Out of Step operation.

Consider a worst case scenario when the power oscillations are triggered upon fault clearance on the parallel line. In that case approximately twice the load current will start flowing through the remaining circuit, increase further and eventually exceed the MOV threshold. Since the R6-R5 region is usually set far from zone 1 the chances that the positive sequence impedance's trajectory may traverse in and out of the set ΔR region due to MOV's operation, are remote. If MOV's do operate within the ΔR region (see the figure below), a timer, that has been initiated, may reset and be re-initiated or the impedance may remain within ΔR region for a slightly longer duration. This is due to the fact that resistive and capacitive components will be added to the measured impedance during MOV operation as per figure below. This effect may have an impact on the 'Delta t' measurement if 'Predictive OST' setting is used. If the recommendation to set R5MIN as close as practically possible to the R6MAX is followed, the chances that the swing currents will exceed MOV threshold within the ΔR region is very remote. If a study shows that the MOV's could operate within the ΔR region, it is recommended to set 'Predictive OST and OST' operating mode to cover all eventualities.

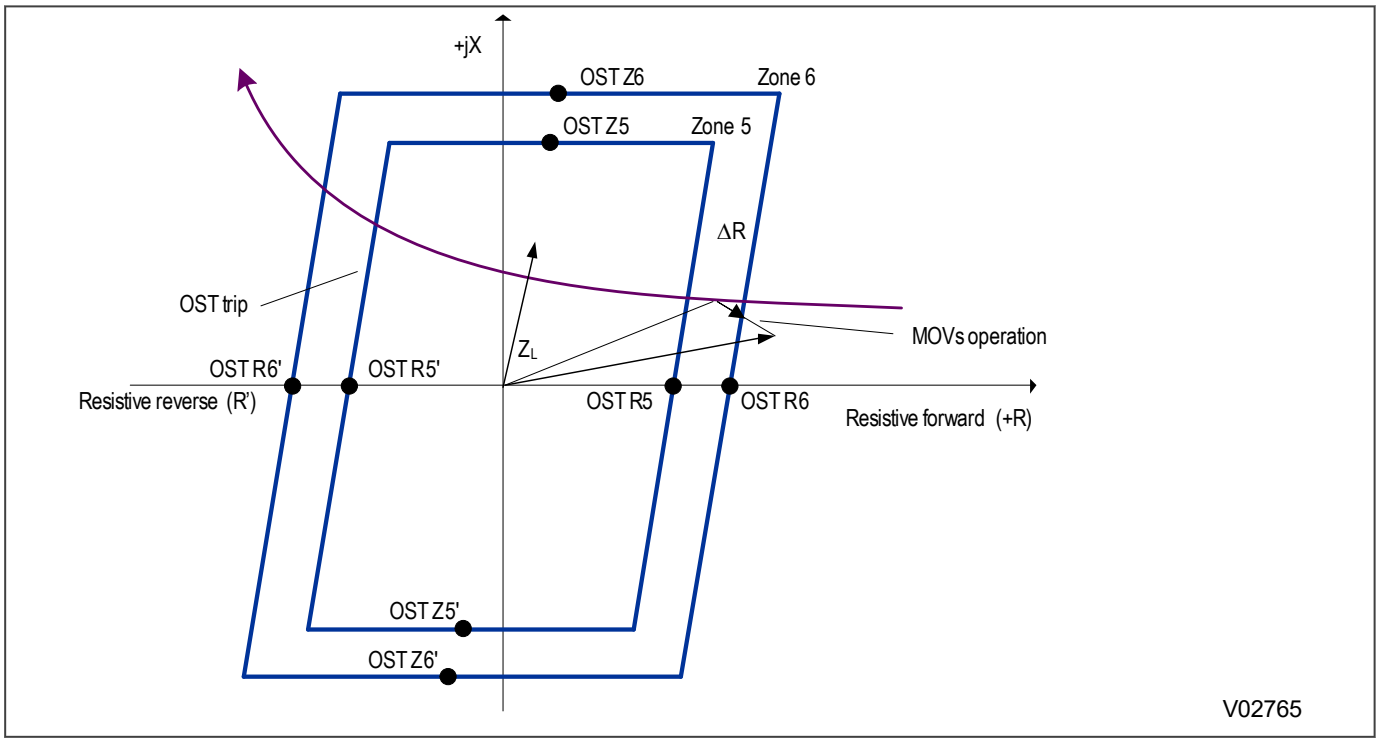


Figure 201: Example of timer reset due to MOV's operation

Note:
If 'OST' setting is chosen, the timer when triggered, will eventually expire as the power oscillations progress, therefore MOV operation will not have any impact on Out of Step operation.

CHAPTER 12

AUTORECLOSE

12.1 CHAPTER OVERVIEW

Selected models of this product provide sophisticated Autoreclose (AR) functionality. The purpose of this chapter is to describe the operation of this functionality including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 338
Introduction to Autoreclose 339
Autoreclose Implementation 342
Logic Modules (Single CB) 349
Logic Modules (Dual CB) 380
Setting Guidelines 435

12.2 INTRODUCTION TO AUTORECLOSE

Approximately 80 - 90% of faults on transmission lines and distribution feeders are transient in nature. This means that most faults do not last long, and are self-clearing if isolated. A common example of a transient fault is an insulator flashover, which may be caused, for example, by lightning, clashing conductors, or wind-blown debris. Protection functions detecting the flashover will cause one or more circuit breakers to trip and may also remove the fault. If the source is removed, the fault does not recur if the line is re-energised.

The remaining 10 – 20% of faults are either semi-permanent or permanent. A small tree branch falling onto the line for example, could cause a semi-permanent fault. Here the cause of the fault would not be removed by immediate tripping of the circuit, but could possibly be burnt away during a time-delayed trip. Permanent faults could be broken conductors, transformer faults, cable faults or machine faults, which must be located and repaired before the power supply can be restored. In many fault incidents, if the faulty line is immediately tripped out, and time is allowed for the fault arc to de-ionise, reclosing the circuit breakers will result in the line being successfully re-energised.

Autoreclose schemes are used to automatically reclose a circuit breaker a set time after it has been opened due to operation of a protection element. On EHV transmission networks, Autoreclose is usually characterised by high-speed single-phase operation for the first attempt at reclosure. This is intended to help maintain system stability during a transient fault condition. On HV/MV distribution networks, Autoreclose is applied mainly to radial feeders, where system stability problems do not generally arise, and is generally characterised by delayed three-phase operation with potentially multiple reclosure attempts.

Autoreclosing provides an important benefit on circuits using time-graded protection, in that it allows the use of instantaneous protection to provide a high speed first trip. With fast tripping, the duration of the power arc resulting from an overhead line fault is reduced to a minimum. This lessens the chance of damage to the line, which might otherwise cause a transient fault to develop into a permanent fault. Using instantaneous protection also prevents blowing of fuses in teed feeders, as well as reducing circuit breaker maintenance by eliminating pre-arc heating. When instantaneous protection is used with Autoreclose, the scheme is normally arranged to block the instantaneous protection after the first trip. Therefore, if the fault persists after re-closure, the time-graded protection will provide discriminative tripping resulting in the isolation of the faulted section. However, for certain applications, where the majority of the faults are likely to be transient, it is common practise to allow more than one instantaneous trip before the instantaneous protection is blocked.

Some schemes allow a number of re-closures and time-graded trips after the first instantaneous trip, which may result in the burning out and clearance of semi-permanent faults. Such a scheme may also be used to allow fuses to operate in teed feeders where the fault current is low.

When considering feeders that are partly overhead line and partly underground cable, any decision to install Autoreclose should be subject to analysis of the data (knowledge of the frequency of transient faults). This is because this type of arrangement probably has a greater proportion of semi-permanent and permanent

faults than for purely overhead feeders. In this case, the advantages of Autoreclose are small. It can even be disadvantageous because re-closing on to a faulty cable is likely to exacerbate the damage.

12.2.1 ADAPTIVE AUTORECLOSE OVERVIEW

Application of high-speed single-phase reclosing helps to increase the system stability limit as the system voltage and short circuit level increase. In order to have successful single-phase reclosing, the reclosing time should be greater than the de-ionisation duration of the fault arc, which will vary based on several factors like duration of fault, system voltage, fault location, atmospheric conditions, capacitive coupling to adjacent conductors and many other factors. In general, the circuit voltage is the predominating factor influencing the de-ionising time. For single pole autoreclosure there is another effect which has a significant influence on the success of the autoreclosure. The primary arc current is interrupted by disconnecting the faulted phase from the sources by opening the circuit breakers at both ends of the line. After this a secondary arc can prevent the fault clearance. During the single pole dead time capacitive and inductive coupling from the other two phases induces a voltage into the open phase conductor which feeds the secondary arc. The secondary arc is an arc between the open phase and earth which is fed by the two healthy phases via capacitive coupling. The voltage measured at the disconnected phase is characterised by the ohmic nonlinear behaviour of the secondary arc. If the secondary arc is extinguished the

equivalent circuit changes to a linear capacitive behaviour of the phase to earth capacitance of the open conductor. The voltage and current goes back to normal conditions after successful reclosing.

In the majority of cases, a fixed dead time setting is applied for transmission line autoreclose schemes. This may cause a problem if the dead time is not long enough for the fault arc to fully de-ionize. Reclosing before the arc extinction can result in arc restrike and could cause the line protection to trip again, which may incur more stress on the power system. Under certain conditions, the reclosing onto the fault may put system stability at risk or damage the equipment. Hence it is desirable to have an adaptive high-speed reclosing scheme that has a variable dead time interval to allow the breaker to close only after the fault arc has extinguished.

The patented adaptive autoreclose (AAR) technique in this relay overcomes the above issue for single pole autoreclose applications by detecting whether the fault arc is extinguished or not and adapts the dead time. AAR uses the pattern of the faulted phase voltage in the complex plane, which is compared with the other two healthy phase voltages, to distinguish between transient and permanent faults in the case of a single-phase earth fault in the transmission line. Also, it can detect when the arc is extinguished in case of a temporary fault and hence it can facilitate successful high-speed reclosing of a transmission line.

For a single-phase fault if the fault is permanent, the faulted phase voltage magnitude and angle do not change with time after line isolation. Whereas, for a transient fault, the faulted phase voltage magnitude increases as the arc resistance increases until the arc is extinguished. Moreover, the angle of faulted phase voltage at the moment when the arc is extinguished lags 90° the angle of faulted phase voltage immediately after line isolation.

The following facts can be observed for the secondary arc of single phase faults.

Fact 1. In the case of a permanent fault, the faulted phase voltage magnitude and angle remains almost constant after line isolation after the switching transients are damped.

Fact 2. In the case of a transient fault, the voltage magnitude drops immediately after the line isolation and then it slowly increases until the arc is extinguished.

Fact 3. In the case of a transient fault, after the line isolation, the angle δ either drops immediately and then increases slowly or increases from the beginning until the arc is extinguished.

δ is the angle between the sum of healthy phase voltages (δh, δk) and the faulted phase (δs) at line end, δ= δh+δk-δs

|Vs| is the voltage magnitude of the faulted phase at line end

For example, for an A phase fault, |Vs| is the A phase voltage magnitude and δ is the angle between the sum of healthy phase voltages B and C (δh, δk) and the faulted A phase voltage at line end (δs), δ= δB+δC- δA

Fact 4. In case of a transient fault, when the arc is extinguished, the magnitude of faulted phase voltage (|Vs|) either becomes constant after a small drop or becomes oscillatory with a constant DC component.

Fact 5. In case of a transient fault, when the arc is extinguished, the angle δ becomes constant or oscillatory with a constant DC component.

Based on the above-mentioned facts, a new algorithm is used to detect a permanent fault and the time of arc extinction in case of a transient fault. The adaptive reclosing function is initiated by the breaker open status which is also used for the faulted phase selection. The breaker interruption should be detected in less than two cycles in order to detect the fast extinguishing arcs. If the fault is a single-phase to ground fault, the faulted phase voltage is selected and the adaptive reclosing algorithm can be initiated.

Angle δ is calculated and the magnitude of the faulted phase voltage (|Vs|) is monitored to determine the reference time (t_{ref}). t_{ref} is the time that |Vs| starts increasing after the drop that occurs after line isolation. t_{ref} can be determined easily by calculation of the minimum |Vs| after the initiation. If |Vs| keeps to be greater than its minimum value for a cycle, the time point after that cycle and the corresponding δ are assigned to t_{ref} and δ_{ref}. If the reference time could not be found within 10 cycles after algorithm initiation, the time point after the 10 cycles and the corresponding δ are assigned to t_{ref} and δ_{ref}. The latter case normally happens only for permanent faults because the voltage magnitude does not increase after line isolation.

After algorithm initiation, δ and |Vs| is low-pass filtered to attenuate all the unwanted transients. Then, the long-window derivation of the filtered signals is obtained by fitting a line to the last 6 cycles of the data. The slope of the

fitted line is used as a long-window derivation. This method provides a smooth and reliable estimate for derivations of δ and |Vs|.

Fact 1 can be used to detect any permanent fault. This can be done by checking δ, δd and |Vs|d. If |Vs| and δ remain almost constant, δ_d and $|Vs|_d$ derivatves become very small (close to zero) and ($\delta - \delta_{ref}$) will be small as well.

Fact 2 to Fact 5 can be used to detect the transient fault and the time that the arc is extinguished. As per Facts 2 and 4, |Vs| slowly increases after t_{ref} until the arc is extinguished. This means that, after t_{ref}, |Vs|d is positive until the arc is extinguished where $|Vs|_d$ either becomes negative and then zero or becomes oscillatory with a zero DC component. As per Facts 3 and 5, δ slowly increases after t_{ref} until the arc is extinguished. This means that, after t_{ref}, δ_d is positive until the arc is extinguished where δ_d becomes zero or oscillatory with a zero DC component. Simply by checking the above-mentioned criteria, the permanent fault and transient fault with arc extinction time can be detected.

12.3 AUTORECLOSE IMPLEMENTATION

Before describing this function it is first necessary to understand the following terminology:

- A **Shot** is an attempt to close a circuit breaker using the Autoreclose function.
- **Multi-shot** is where more than one **Shot** is attempted.
- **Single-shot** is where only one **Shot** is attempted.
- **Dead Time** denotes the time between initiation of the Autoreclose operation and the attempt to close the circuit breaker. The dead time is normally a fixed time delay but can be can set to adaptive for single pole autoreclose schemes where it is dependent on the arc extinction time for a transient single-phase fault.
- **Reclaim time** is the time following the initiation of the circuit breaker closing and the resetting of the Autoreclose scheme should the Autoreclose attempt be successful and the protection does not detect a subsequent fault condition.
- **High-speed Autoreclose** is generally regarded as an Autoreclose application where the **Dead Time** is less than 1 second.
- **Delayed Autoreclose** is generally regarded as an Autoreclose application where the **Dead Time** is greater than 1 second.

This product features a multiple-shot Autoreclose function, which is suitable for both High-speed Autoreclose and Delayed Autoreclose.

The Autoreclose function can be set to perform a single-shot, two-shot, three-shot or four-shot cycle. Dead Times for all shots can be adjusted independently.

If a circuit breaker closes successfully at the end of the Dead Time, a Reclaim Time starts. If the circuit breaker does not trip again, the Autoreclose function resets at the end of the Reclaim Time. If the protection trips again during the Reclaim Time, the sequence advances to the next shot in the programmed cycle. If all programmed reclose attempts have been made and the circuit breaker does not remain closed, the Autoreclose function goes into Lockout, whereupon manual intervention is required.

An Autoreclose cycle can be initiated by operation of an internal or external protection element provided it is mapped correctly, and that the circuit breaker is closed when the protection operates.

You can choose to initiate the Dead Time on:

- Protection operation
- A protection reset
- A Line Dead condition
- Circuit breaker operation

At the end of the relevant Dead Time, provided system conditions are suitable, a circuit breaker close signal is given. The system conditions to be met for closing are that:

- the system voltages are in synchronism
- or that the dead line/live bus or live line/dead bus conditions exist as indicated by the internal system check synchronising element
- and that the circuit breaker closing spring, or other energy source, is fully charged as indicated by the circuit breaker healthy input.

The circuit breaker close signal is removed when the circuit breaker closes.

If the protection trips and the circuit breaker opens during the Reclaim Time, the Autoreclose function either advances to the next shot in the programmed cycle, or if all programmed reclose attempts have been made, goes into Lockout. Each time a closure is attempted, a sequence counter is incremented by 1 and the Reclaim Time starts again.

Autoreclose is configured in the *AUTORECLOSE* column of the relevant settings group. The function is disabled by default. If you wish to use it, you must enable it first in the *CONFIGURATION* column.

The Autoreclose function is a logic controller implemented in software. It takes inputs and processes them according to defined logic to generates appropriate outputs. The logic is controlled by user prescribed settings and commands. The controlling logic is complex and so, in order to facilitate its design and understanding, it is decomposed into smaller logic functions which, when combined together implement the complete scheme. This section concludes with a summary of:

- the logic inputs to the Autoreclose function,
- the logic outputs from the Autoreclose function
- the Autoreclose operating sequence
- the high-level design of the system logic functionality

12.3.1 AUTORECLOSE LOGIC INPUTS FROM EXTERNAL SOURCES

Logic inputs control the operation of the Autoreclose function. The logic inputs are mapped using DDB signals in the PSL.

Generally the inputs are from external equipment connected to opto-isolated inputs. They can also come from communications inputs, and some are internally derived.

This section provides an overview of the logic inputs originating from external sources.

12.3.1.1 CIRCUIT BREAKER HEALTHY INPUT

For circuit breakers to close, it needs energy. This energy usually comes from a spring (spring-charged circuit breakers) or from gas pressure (gas pressurised circuit breakers). After closing, it is necessary to re-establish sufficient energy in the circuit breaker before it can be closed again.

DDB signal inputs to the Autoreclose function allow the health of circuit breakers to be mapped to the logic. when asserted, these signals demonstrate that there is sufficient energy available to close and trip the circuit breaker before initiating a circuit breaker close command. If the signal indicating the health of the circuit breaker is low, and remains low for a defined period set in the circuit breaker healthy timer, the circuit breaker locks out and stays open.

If the circuit breaker healthy signal is not mapped in the PSL, the DDB signal defaults to high so that Autoreclose may proceed.

12.3.1.2 INHIBIT AUTORECLOSE INPUT

A logic input can be used to inhibit the Autoreclose function. The signal is mapped to the DDB signal ***Inhibit AR*** in the PSL.

Energising the input inhibits any auto-switching of connected circuit breakers. Any Autoreclose in progress is reset and inhibited but not locked out. This function ensures that auto-switching does not interfere with any manual switching. A typical application is on a mesh-corner scheme where manual switching is being performed on the mesh, for which any Autoreclose would cause interference.

For products that are capable of single-phase tripping and Autoreclose, if a single-phase Autoreclose cycle is in progress and a single pole of the circuit breaker is tripped when the inhibit Autoreclose signal is raised, the circuit breaker is instructed to trip all phases, ensuring that all poles are in the same state (and avoiding a pole stuck condition) when subsequent closing of the circuit breaker is attempted.

12.3.1.3 BLOCK AUTORECLOSE INPUT

External inputs can be used to block the Autoreclose function. If Autoreclose is in progress when the signal is asserted, it forces a lockout.

Typically this feature is used where Autoreclose may be required for some protections functions but not required for others. An example is on a transformer feeder, where Autoreclose can be initiated from the feeder protection but blocked from the transformer protection.

It can also be used if an Autoreclose cycle is likely to fail for conditions associated with the protected circuit, such as during the Dead Time, if a circuit breaker indicates that it is not healthy to switch.

12.3.1.4 RESET LOCKOUT INPUT

If a condition that forced a lockout has been removed, the lockout can be reset by energising a logic input appropriately mapped in the PSL. Energising the input will also reset any Autoreclose alarms.

12.3.1.5 POLE DISCREPANCY INPUT

Circuit breakers with independent mechanisms for each pole (phase), normally incorporate a mechanism to cater for cases where the phases are not together. This automatically trips all three phases if they are either not all open, or not all closed.

During single-phase Autoreclosing a pole discrepancy condition is necessarily introduced, but the pole discrepancy device should not operate for this condition. This can be achieved using a delayed action pole discrepancy device with a delay longer than the single-pole Autoreclose Dead Time (***SP AR Dead Time*** setting).

Alternatively, an input can be used for external devices to indicate a pole discrepancy condition. The pole discrepancy input is activated by an external device to indicate that all three poles of a circuit breaker are not in the same position. If mapped in the PSL, energising the input forces three-phase tripping (providing there is not a single-phase Autoreclose in progress). Otherwise, a signal indicating single-phase Autoreclose in progress can be used to inhibit the external pole discrepancy device.

12.3.1.6 EXTERNAL TRIP INDICATION

Protection operation from a different device can be used to initiate the Autoreclose function. By default these external trip inputs are mapped to initiate Autoreclose and to initiate breaker failure protection (if the functions are enabled). These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL however, the external device can use this product to trip connected circuit breakers.

12.3.2 AUTORECLOSE LOGIC INPUTS

This section provides an overview of the logic inputs, which are derived internally.

12.3.2.1 TRIP INITIATION SIGNALS

The phase A, phase B and phase C trip inputs are used to initiate single-phase and three-phase autoreclose. For the Autoreclose to work, you must ensure that these Trip Input signals remain appropriately mapped in the PSL.

12.3.2.2 CIRCUIT BREAKER STATUS INPUTS

Circuit breaker status information must be available as logic input(s) for Autoreclose to work. You can select whether to use CB open, CB closed, or both, as inputs. The settings are made in the *CB CONTROL* column of the menu, and you need to ensure that the PSL mapping of the chosen input(s) is correct.

12.3.2.3 SYSTEM CHECK SIGNALS

System Check and Check Synchronisation functions produce signals which are used by the Autoreclose logic ensure that the Autoreclose function is applied only when the system is in a suitable condition.

12.3.3 AUTORECLOSE LOGIC OUTPUTS

Output signals are provided to provide indication of an Autoreclose in progress (ARIP). An ARIP signal is asserted when an Autoreclose sequence starts. It remains high from initiation, either until lockout, or until successful Autoreclose.

An Autoreclose lockout condition resets any ‘Autoreclose in progress’ and associated signals. Signals are available to indicate that Autoreclose is in progress and that a circuit breakers has been successfully closed.

12.3.4 AUTORECLOSE OPERATING SEQUENCE

The Autoreclose sequence is controlled by so-called Dead Timers. Dead Time Control settings are used to select the conditions that initiate Dead Timers in the Autoreclose sequence (for example protection operate, protection reset, CB open, etc.). This section describes typical AR operation sequences in which Dead Timers start when protection operation resets.

Note:
In a multi-shot AR sequence, a number of Dead Timers are used (one for each shot). All Dead Timers are enabled when the sequence is initiated, but each timer only starts when the particular shot with which it is associated is triggered.

12.3.4.1 AR TIMING SEQUENCE - TRANSIENT FAULT

The figure below describes the operating sequence for a single-shot Autorecloser for a transient fault that clears when the faulted line is isolated.

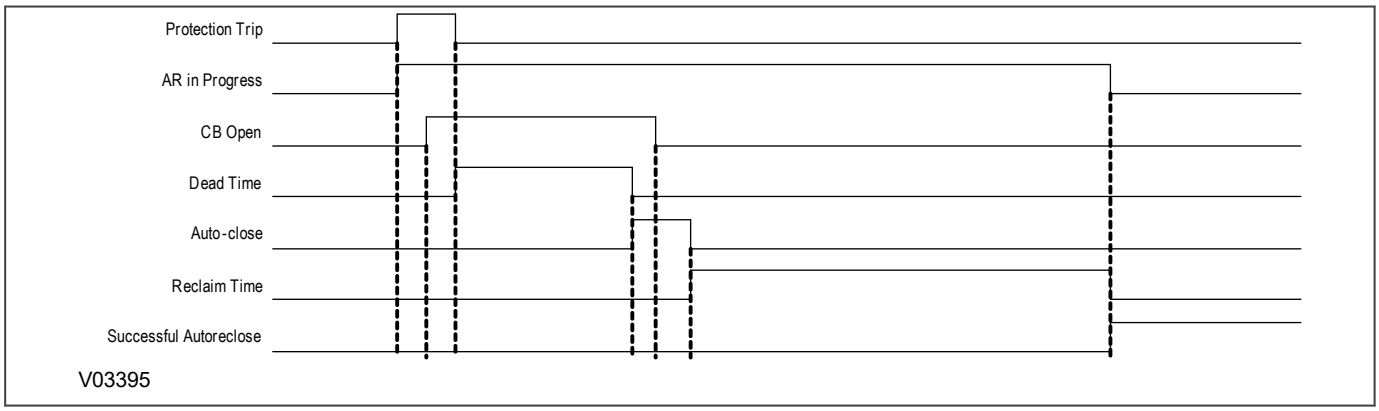


Figure 202: Autoreclose sequence for a transient fault

Following fault inception, the protection operates and issues a trip signal. At the same time the Autoreclose in Progress signal is asserted. Shortly afterwards the circuit breaker will open as indicated by the CB Open signal. Opening of the CB clears the fault and the protection resets. When this happens, the Dead Timer is started and the output remains high until the Dead Time setting expires, whereupon it resets and the Autorecloser issues the Auto-close command to close the circuit breaker. As the fault has been cleared, the circuit breaker closes and remains closed. When the Auto-close pulse is removed, the Reclaim Timer starts. If no further fault is detected before the Reclaim Timer expires, the Autoreclose is considered to be successful and this is indicated by the Successful Autoreclose signal.

12.3.4.2 AR TIMING SEQUENCE - TRANSIENT FAULT DUAL CB

The figure below describes the operating sequence for a single-shot on a dual CB (2CB) Autorecloser for a transient fault that clears when the faulted line is isolated.

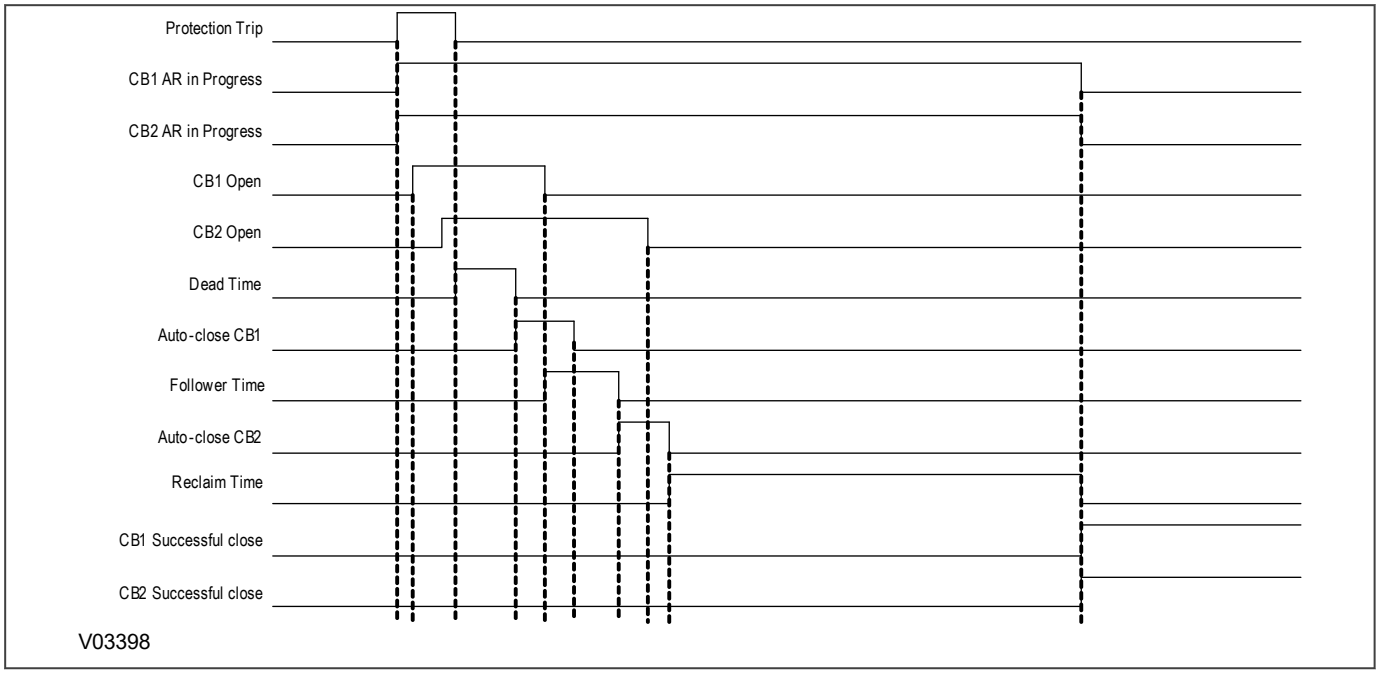


Figure 203: Dual CB autoreclose sequence for a transient fault

Following fault inception, the protection operates and issues a trip signal. At the same time an Autoreclose in Progress signal is asserted for each CB. Shortly afterwards, CB1 will open as indicated by the CB1 Open signal and after a short delay CB2 opens. Opening of CB2 clears the fault and the protection resets. When this happens, the Dead Timer is started and the output remains high until the Dead Time setting expires, whereupon it resets and the Autorecloser issues the Auto-close command to close CB1. When CB1 closes, the Follower Timer starts. When the Follower Timer expires, the Autorecloser issues the Autoclose command to close CB2. After CB2 has closed, as the fault has been cleared, both CBs remain closed. When the Auto-close 2 pulse is removed, the Reclaim Timer starts. If no further fault is detected before the Reclaim Timer expires, the Autoreclose is considered to be successful and this is indicated by the Successful Autoreclose signals.

12.3.4.3 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT

The figure below shows a single-shot AR operating sequence where the fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows an evolving fault inception occurring before the Reclaim Time has expired. When the Autorecloser recognises that the protection has tripped, the cycle is terminated. The Autorecloser goes into Lockout, and the Autoreclose in Progress signal is reset.

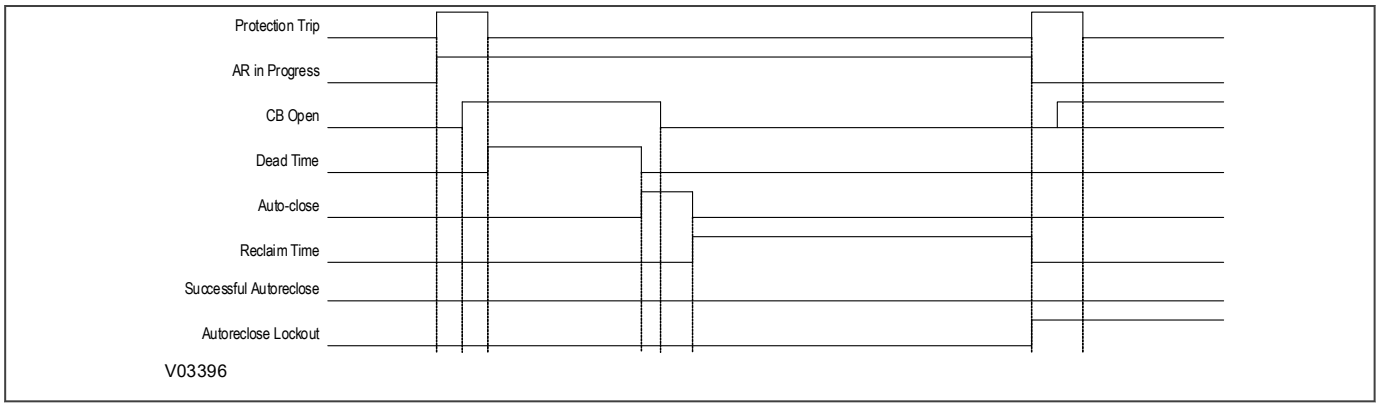


Figure 204: Autoreclose sequence for an evolving or permanent fault

12.3.4.4 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT DUAL CB

The figure below shows a single-shot AR operating sequence where the fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows an evolving fault inception occurring before the Reclaim Time has expired. When the Autorecloser recognises that the protection has tripped, the cycle is terminated. The Autorecloser goes to Lockout, and the AR in Progress signals are reset

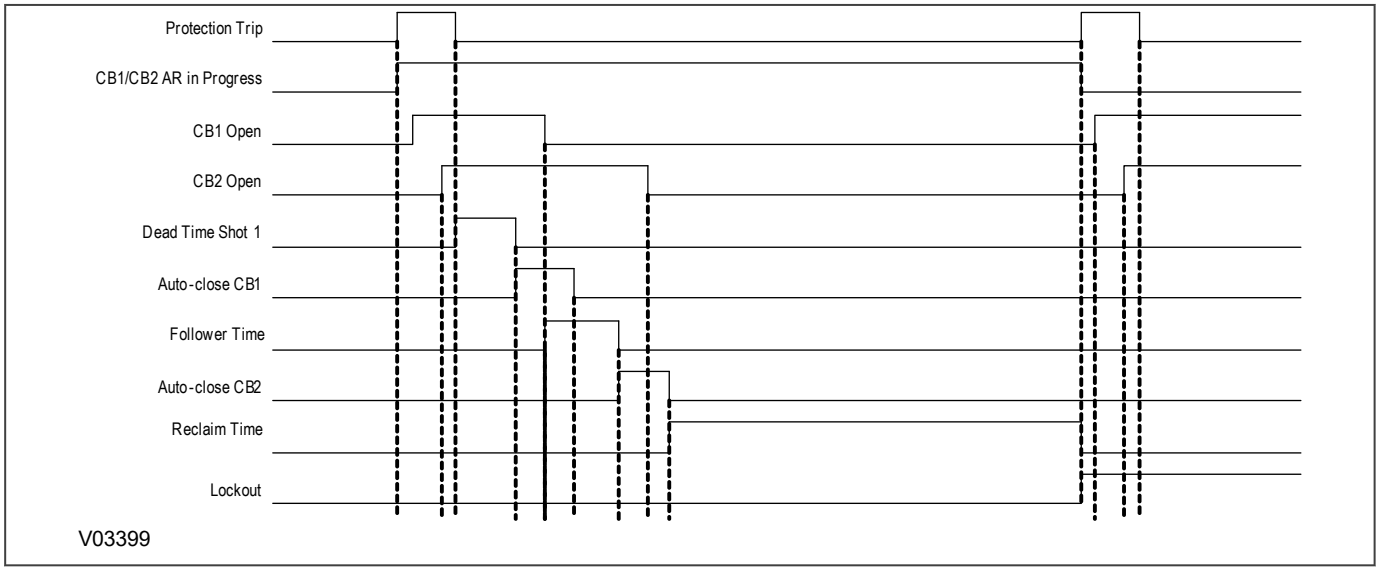


Figure 205: Autoreclose sequence for an evolving/permanent fault on a dual CB application

12.3.4.5 AR TIMING SEQUENCE - EVOLVING/PERMANENT FAULT SINGLE-PHASE

If the Autorecloser is set for single-phase operation, then single phase operation is only allowed on the first shot. Subsequent tripping will be three-phase only until the AR has been successful or until AR has locked out as shown in the figure below.

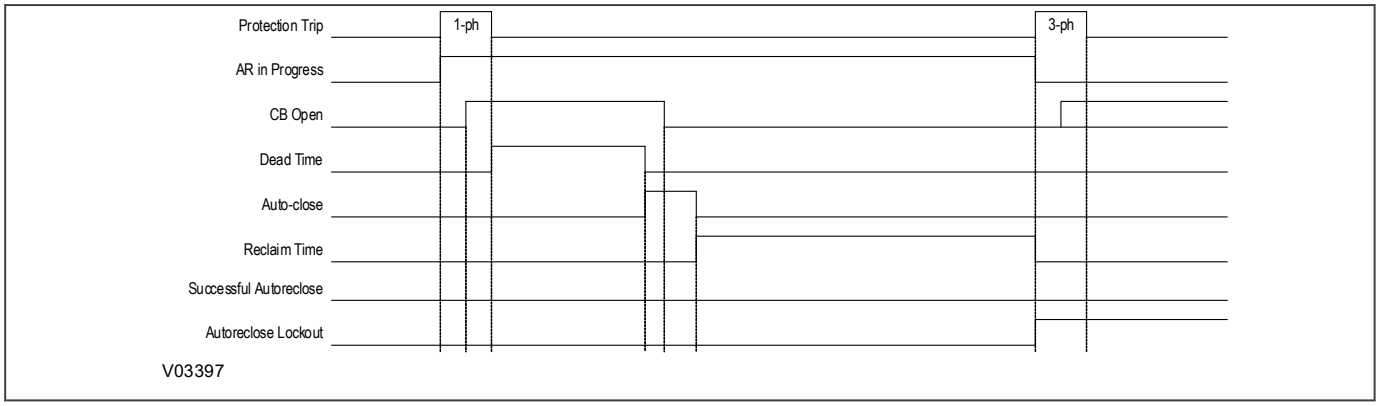


Figure 206: Autoreclose sequence for an evolving or permanent fault - single-phase operation

12.3.4.6 AR TIMING SEQUENCE - PERSISTENT FAULT

The figure below shows the start of a multi-shot AR operating sequence where a single-phase fault is not cleared by the first AR cycle. The sequence starts in a similar way to that of a transient fault, but in this case the fault is not transient (it may be permanent, or it may evolve into a fault involving more than one phase). This case shows a second fault inception occurring before the Reclaim Time has expired. The significant point here is that after the first trip has occurred, the Autorecloser forces the 2 CBs into three-pole operation and different Dead Timers are used for the single-phase cycle compared with the three-phase cycle.

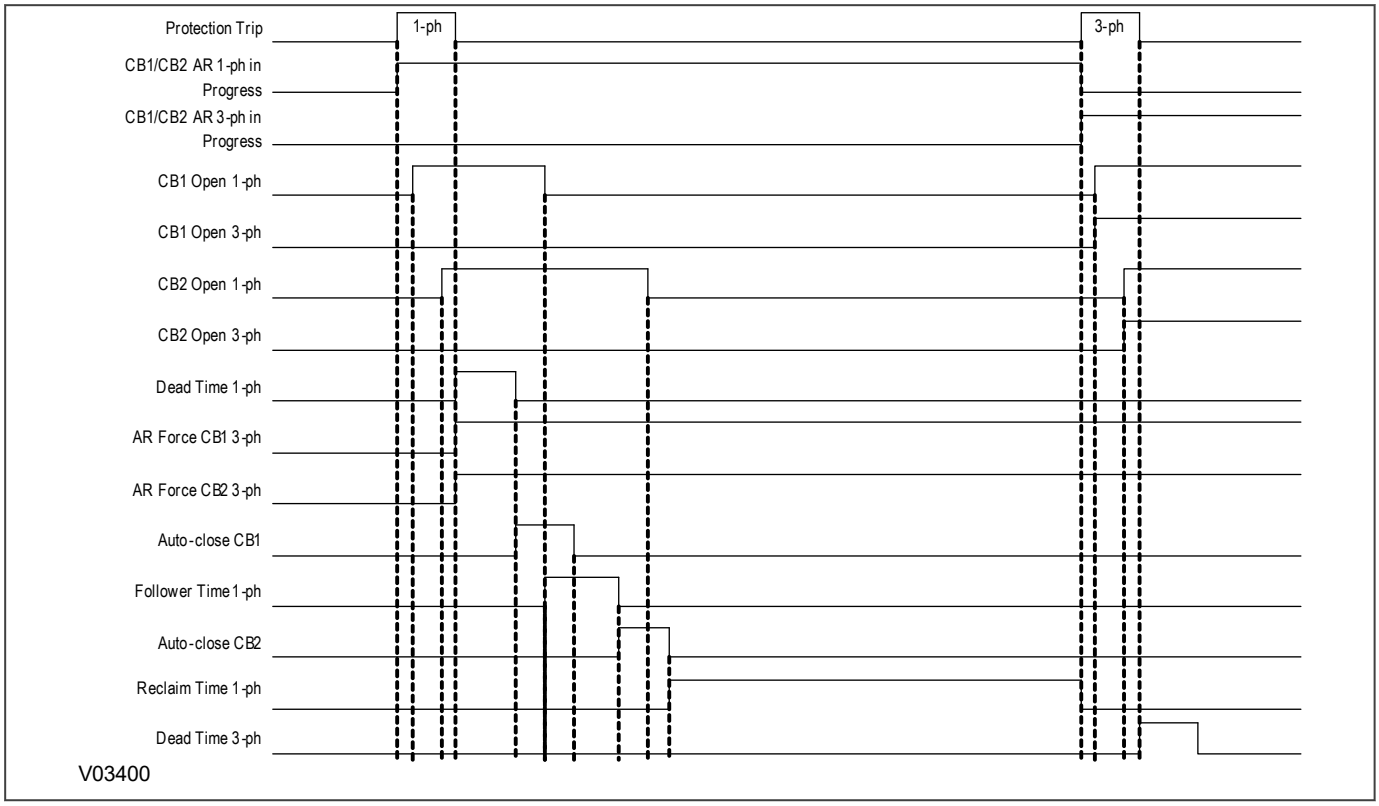


Figure 207: Autoreclose sequence for a persistent fault on a multishot dual CB application set for single-phase operation

Note:
For three-phase Autoreclosing, for the first shot only, Autoreclose can be performed without checking that the voltages are in synchronism using a setting. This setting, CB1L SC Shot 1 or CB2L SC Shot 1, can be enabled to perform synch-checks on shot 1 for CB1 or CB2, or disabled to not perform the checks.

12.4 LOGIC MODULES (SINGLE CB)

This section contains a complete set of logic diagrams for single CB models, which will help to explain the Autoreclose function. Most of the logic diagrams shown are logic modules that comprise the overall Autoreclose system. Some of the diagrams shown are not directly related to Autoreclose functionality, however, they may use some inputs or produce outputs that are used by the Autoreclose system. The diagrams shown in this section are for the sake of completeness.

"Mod" numbers indicate the related Module Numbers of the fixed logic (as mentioned in the Figure description).

"Mod" numbers in red indicate Module Numbers applicable only for dual breaker logic.

12.4.1 CIRCUIT BREAKER STATUS MONITOR

The Circuit Breaker State Monitor logic is part of the Monitoring and Control functionality and is fully described in that chapter. The logic diagram is repeated in this section because some of the outputs of this logic module are used as inputs to some of the Autoreclose logic modules.

12.4.1.1 CB STATE MONITOR LOGIC DIAGRAM

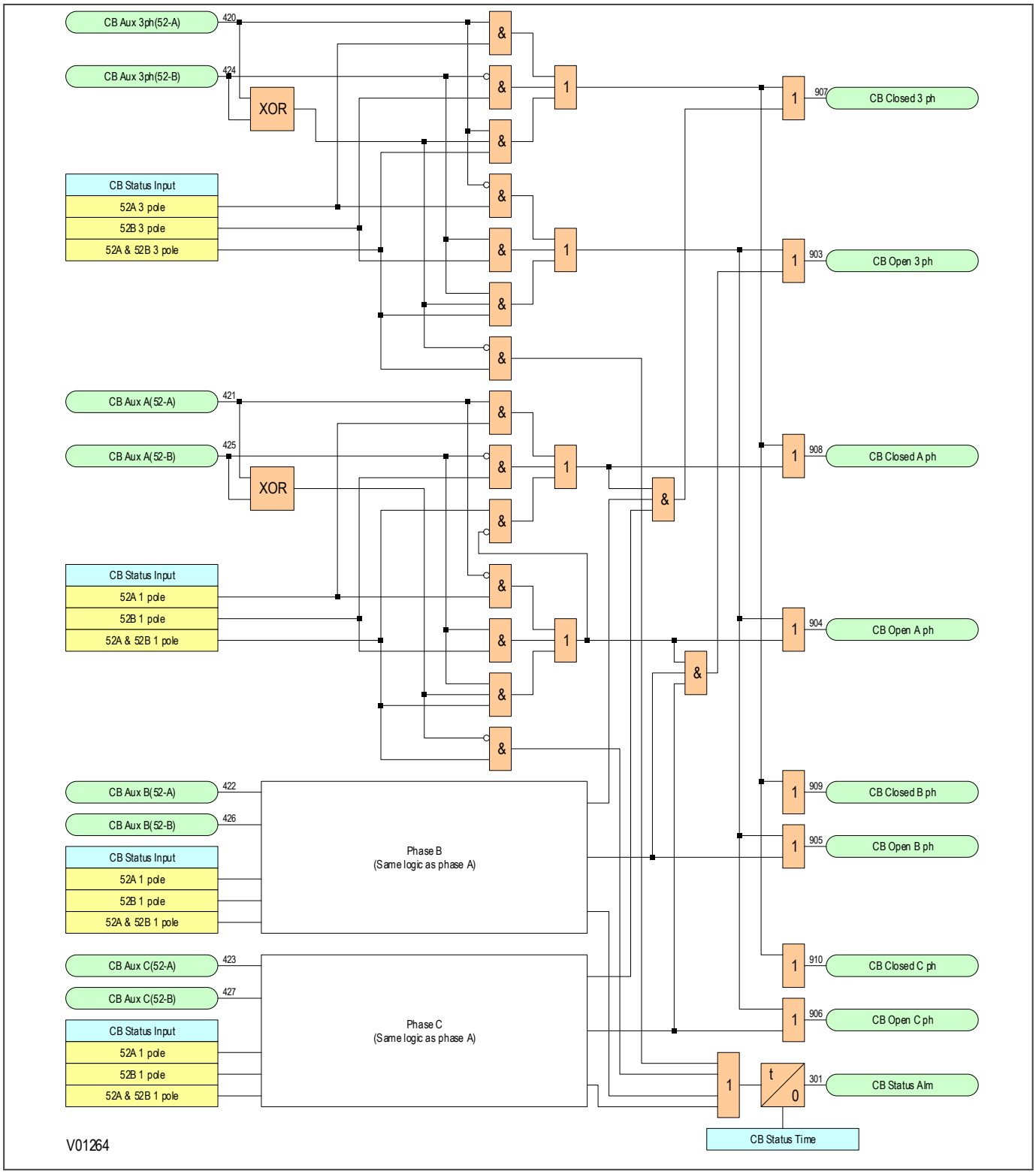


Figure 208: CB state monitor logic (module 1)

12.4.2 CIRCUIT BREAKER OPEN LOGIC

The Circuit Breaker Open logic module produces internal signals indicating the open status of one or more phases. These signals are used by some of the Autoreclose logic modules.

12.4.2.1 CIRCUIT BREAKER OPEN LOGIC DIAGRAM

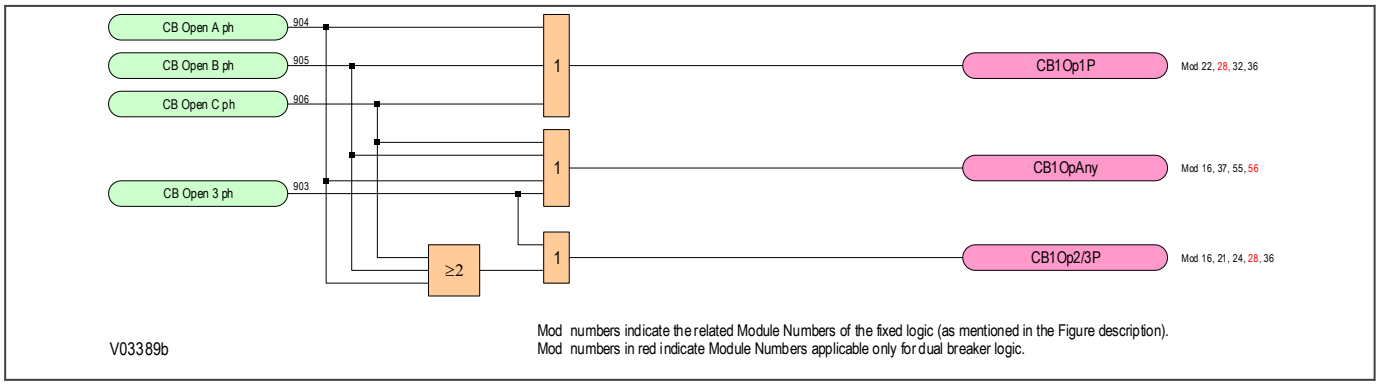


Figure 209: Circuit breaker open logic (module 3)

12.4.3 CIRCUIT BREAKER IN SERVICE LOGIC

For Autoreclose to proceed, a circuit breaker has to be in service when the Autoreclose is initiated. A circuit breaker is considered to be in service if it has been closed for more than the CB IS Time setting.

For applications with fast-acting circuit breaker auxiliary switches, a time delay setting CB IS Memory Time is provided. This is used to ensure correct operation if a delay between the circuit breaker tripping and recognition by the protection, is expected.

When an Autoreclose cycle starts, the “in service” signal for a circuit breaker stays set until the Autoreclose cycle finishes.

The circuit breaker “in service” signal resets if the circuit breaker opens, or if the corresponding Autoreclose in progress (ARIP) signal resets.

12.4.3.1 CIRCUIT BREAKER IN SERVICE LOGIC DIAGRAM

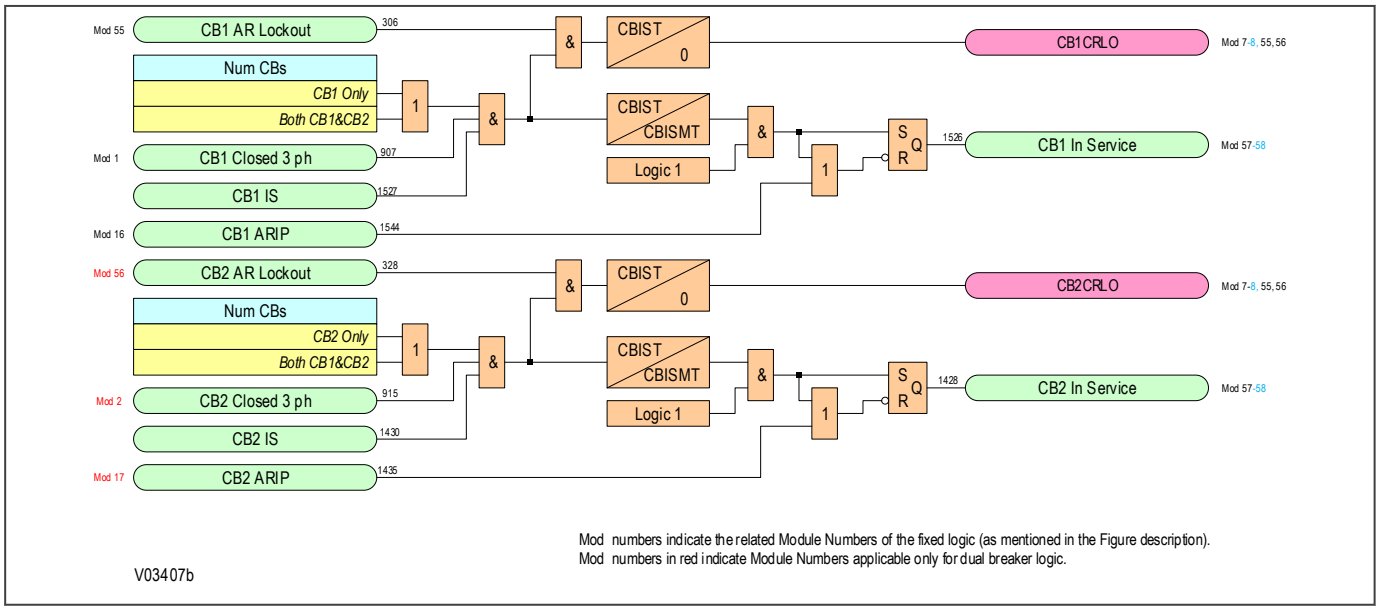


Figure 210: CB in service logic (module 4)

12.4.3.2 AUTORECLOSE OK LOGIC DIAGRAM

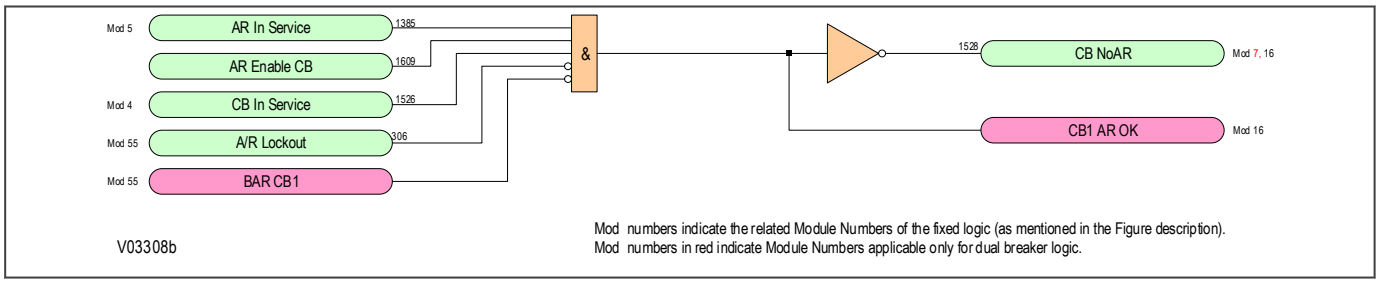


Figure 211: Autoreclose OK logic (module 8)

12.4.4 AUTORECLOSE ENABLE

The Autoreclose function must be enabled in the *CONFIGURATION* column before it can be brought into service. It can be brought into service by:

- using an opto-input mapped to the ***AR Enable*** DDB signal
- pulsing the DDB signal ***AR Pulse On*** (use ***AR Pulse Off*** to bring it out of service)
- programming a function key on the HMI.
- if applicable, using IEC 60870-5-103 communications

A further validation signal is also required to switch on Autoreclose. This is the DDB signals ***AR Enable CB***. Once Autoreclose is in service, the ***AR In Service*** DDB signal is asserted and the ***AR Status*** cell in the *CB CONTROL* column is set accordingly.

12.4.4.1 AUTORECLOSE ENABLE LOGIC DIAGRAM

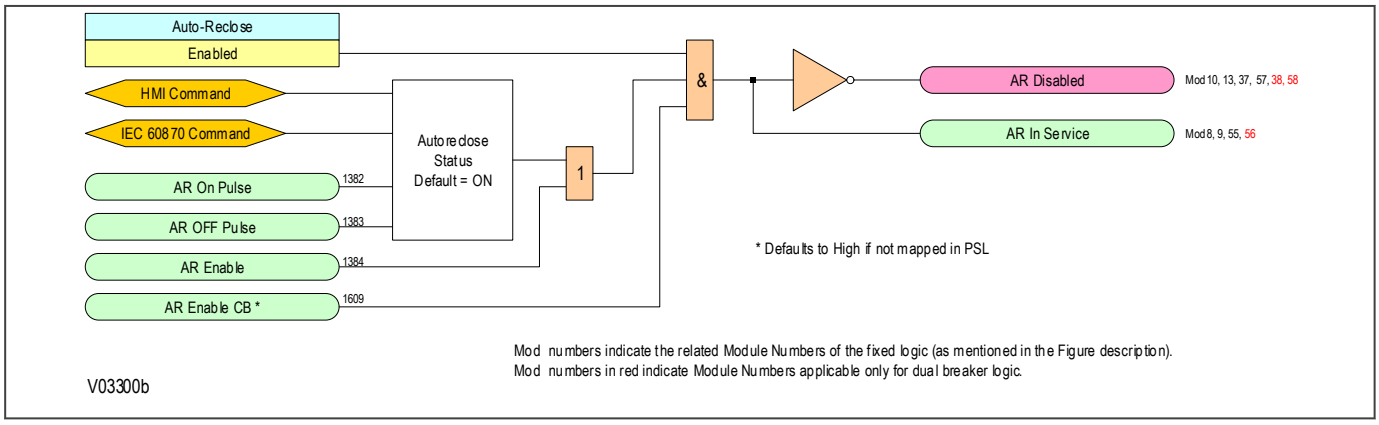


Figure 212: Autoreclose enable logic (module 5)

12.4.5 AUTORECLOSE MODES

The device can provide Single-phase and/or Three-phase Autoreclose. The Autoreclose mode is configured by the ***AR Mode*** setting in the *AUTORECLOSE* column. You can choose from:

- Single-phase (`AR 1P`)
- Three-phase (`AR 3P`)
- Single-phase and Three-phase (`AR 1/3P`)
- Controlled by commands from DDB signals that must be mapped to opto-isolated inputs in the PSL (`AR Opto`).

Single-phase Autoreclosing is permitted only for the first shot of an Autoreclose cycle. In a multi-shot Autoreclose cycle the second and subsequent trips will always be three-phase.

For multi-phase faults, you can use the ***Multi Phase AR*** setting in the *AUTORECLOSE* column to configure the following options:

- Allow Autoreclose for all fault types (`Allow Autoclose`)
- Block Autoreclose for 2-phase and 3-phase faults (`BAR 2 and 3 ph`)
- Block Autoreclose for 3-phase faults (`BAR 3 Phase`)

12.4.5.1 SINGLE-PHASE AND THREE-PHASE AUTORECLOSE

Single-phase autoreclose only

If single-phase Autoreclose is enabled, the logic allows only a single shot Autoreclose. For a single-phase fault, the single phase dead timer ***SP AR Dead Time*** starts, and the DDB signal ***CB AR 1pole in prog*** is asserted, which indicates that single-phase Autoreclose is in progress. In this case, for a multi-phase fault the logic triggers a three-phase trip and goes to lockout.

Three-phase autoreclose only

During three-phase Autoreclose, for any fault, the three-phase dead timers: ***3P AR DT Shot 1***, ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** are started and the DDB signal ***CB AR 3pole in prog*** is asserted, which indicates that three-phase Autoreclose is in progress.

If three-phase only Autoreclose is enabled, the logic forces a three-phase trip by setting the DDB signal ***AR Force 3 pole*** for any single-phase fault.

Single-phase and three-phase autoreclose

With single-phase and three-phase Autoreclose enabled then, if the first fault is a single-phase fault the single-phase dead time ***SP AR Dead Time*** is started and the single-phase Autoreclose in progress signal is asserted. If the first fault is a multi-phase fault the three phase dead timer ***3P AR DT Shot 1*** is started and the three-phase Autoreclose in progress signal is asserted. If set to allow more than one reclose (***AR Shots*** >'1') then any subsequent faults are converted to three-phase trips by setting the force three-pole tripping signal. The three-phase dead times ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** (Dead Times 2, 3, 4) are started for the 2nd, 3rd and 4th trips (shots) respectively. The DDB signal ***AR 3pole in prog*** is asserted. If a single-phase fault evolves to a multi-phase fault during the single-phase dead time (***SP AR Dead Time***), single-phase Autoreclose is stopped. The single-phase Autoreclose in progress signal is reset, the three-phase Autoreclose in progress signal is set, and the three-phase dead timer ***3P AR DT Shot 1*** is started.

12.4.5.2 AUTORECLOSE MODES ENABLE LOGIC DIAGRAM

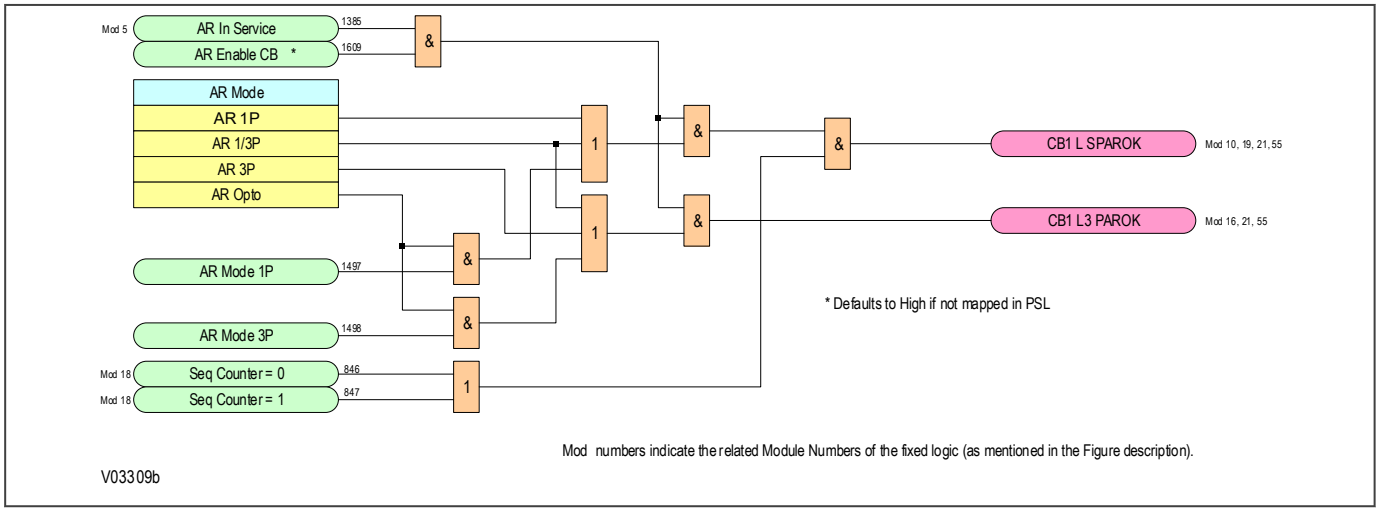


Figure 213: Autoreclose modes enable logic (module 9)

12.4.6 AR FORCE THREE-PHASE TRIP LOGIC

Following single-phase tripping, while the Autoreclose cycle is in progress, and upon resetting of the protection elements, tripping switches to three-phase.

Any protection operations that occur for subsequent faults while the Autoreclose cycle remains in progress will be tripped three-phase.

12.4.6.1 AR FORCE THREE-PHASE TRIP LOGIC DIAGRAM

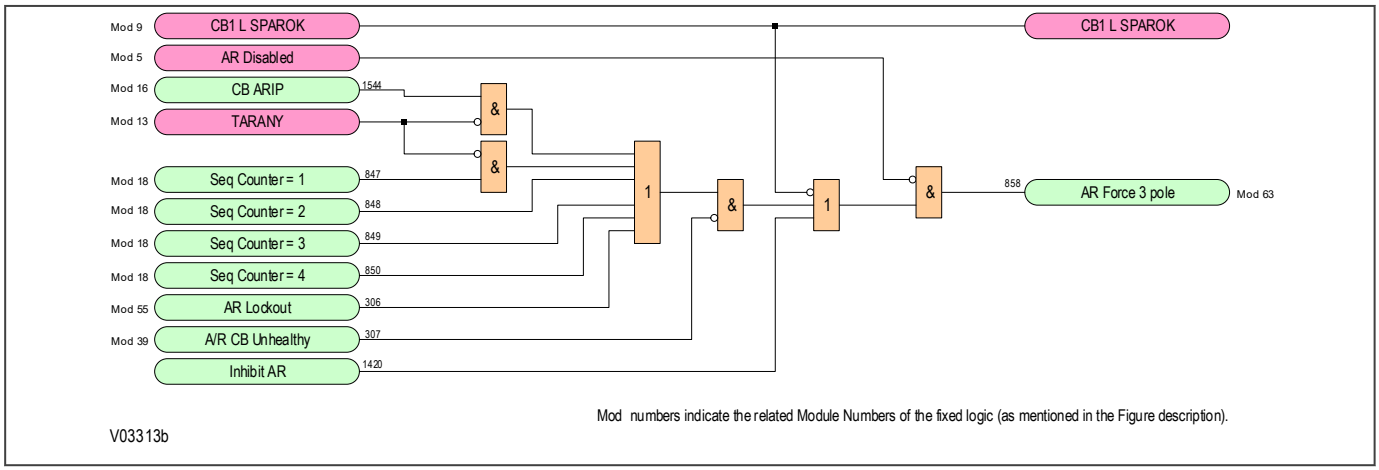


Figure 214: Force three-phase trip logic (module 10)

When a three-phase trip is forced, the DDB signal ***AR Force 3 pole*** is asserted.

12.4.7 AUTORECLOSE INITIATION LOGIC

Autoreclose initiation starts Autoreclose for a circuit breaker only if Autoreclose is enabled for the circuit breaker, and the circuit breaker is in service. When an Autoreclose cycle is started, Autoreclose in progress (ARIP) is indicated. The indication remains until the end of the cycle. The end of the cycle is signified by successful Autoreclose, or by lockout.

Autoreclose cycles can be initiated by:

- Protection functions internal to the product
- A Trip Test feature
- External protection equipment
- Evolving fault combinations

Internal protection functions

Many of the protection functions in the product can be programmed to initiate or block Autoreclose. The associated settings are found in the Autoreclose column and the available options are `No Action`, `Initiate AR`, or `Block AR`. If set to `Block AR` operation of the protection function blocks the Autoreclose function and forces a lockout.

Trip test feature

The ***Test Autoreclose*** command cell in the *COMMISSION TESTS* column can be used to initiate an Autoreclose cycle. Each option provides a 100 ms pulse output. There is also a 'No Operation' option to exit the command field without initiating a test.

External protection equipment

Protection operation from a different device can be used to initiate Autoreclose via PSL. By default these external trip input signals are mapped to initiate Autoreclose. These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL, however, the external device can use this product to trip connected circuit breakers.

Evolving fault combinations

The Autoreclose function would normally be initiated by a single condition (such as a single-phase fault). If, however, the system conditions evolve such that other conditions that could initiate Autoreclose, then the dynamics

of the Autoreclose logic need to adapt. For example, if a single-phase fault evolves into a multi-phase fault, then the operation of the Autorecloser must consequently adapt. To achieve this signals are generated to indicate conditions such as evolving faults, re-operation of protection, combinations of initiation by internal protection, external protection, or test features, which control the Autoreclose sequencing.

Records of initiating conditions are stored and used to control the sequencing. Initiation can be from a protection function integrated in the product, from external protection and internal sources such as the Autoreclose test function. Initiation can be further qualified by the phases causing the initiation. These conditions are stored in signals that generally feature “MEM”- memory, or “AR” – Autoreclose, in the signal name.

12.4.7.1 AUTORECLOSE INITIATION LOGIC DIAGRAM

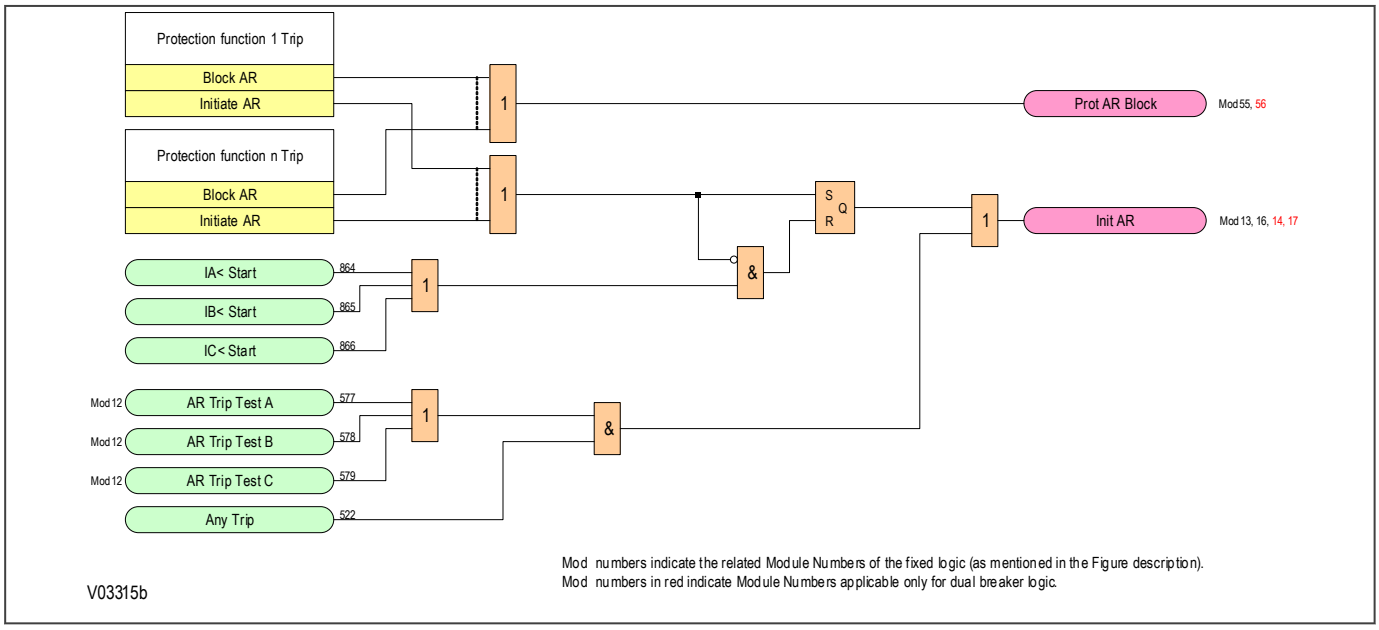


Figure 215: Autoreclose initiation logic (module 11)

12.4.7.2 AUTORECLOSE TRIP TEST LOGIC DIAGRAM

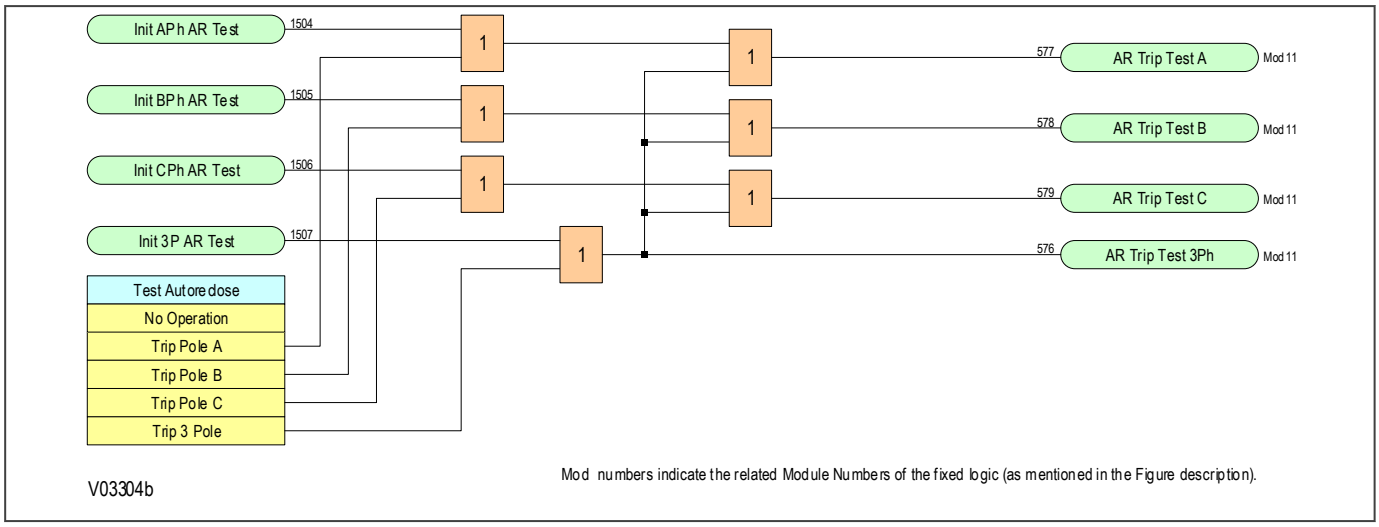


Figure 216: Autoreclose trip test logic (module 12)

12.4.7.3 AR EXTERNAL TRIP INITIATION LOGIC DIAGRAM

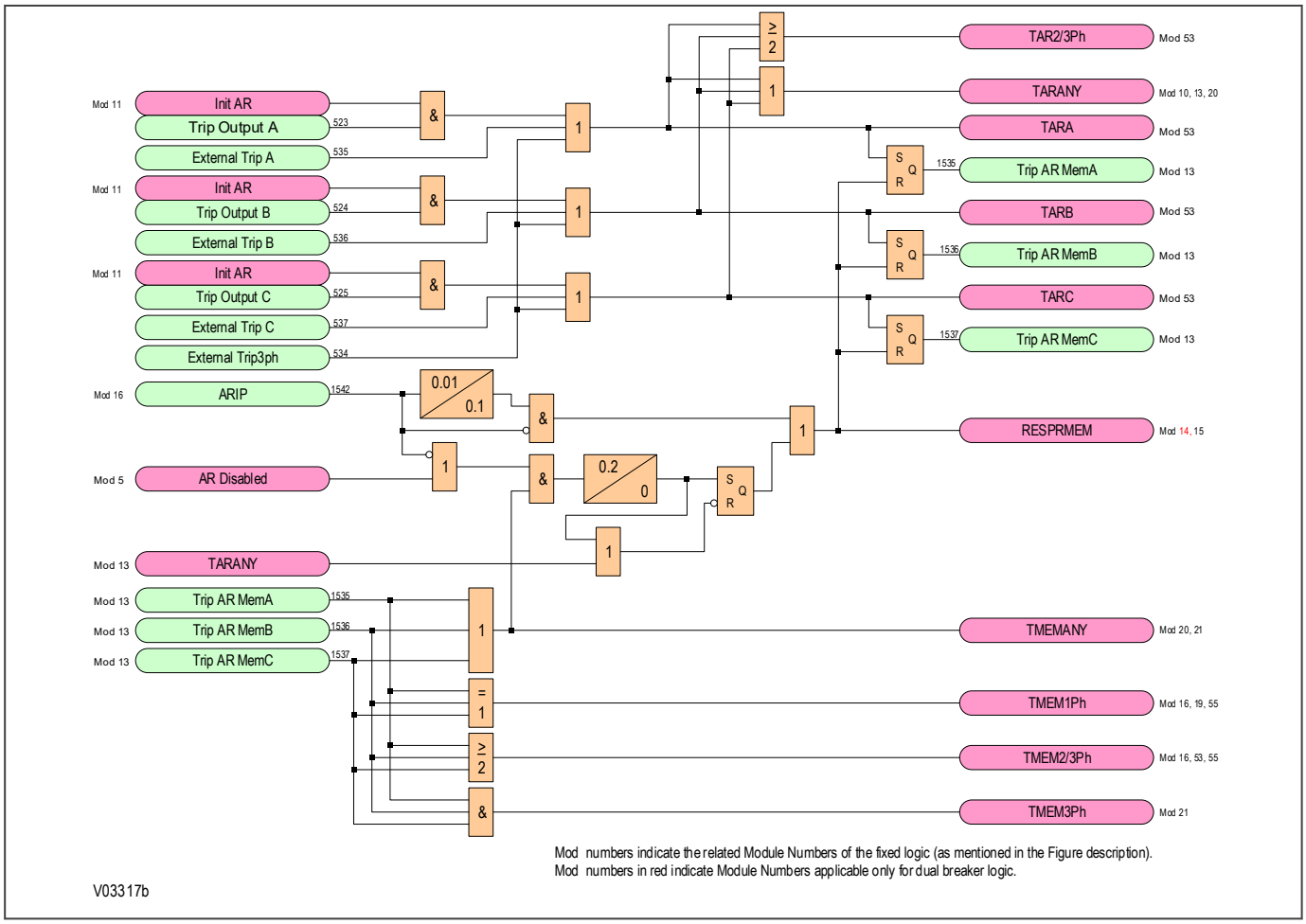


Figure 217: Autoreclose initiation by external trip or evolving conditions (module 13)

Note:
The signals must be mapped as shown in the default PSL scheme.

12.4.7.4 PROTECTION REOPERATION AND EVOLVING FAULT LOGIC DIAGRAM

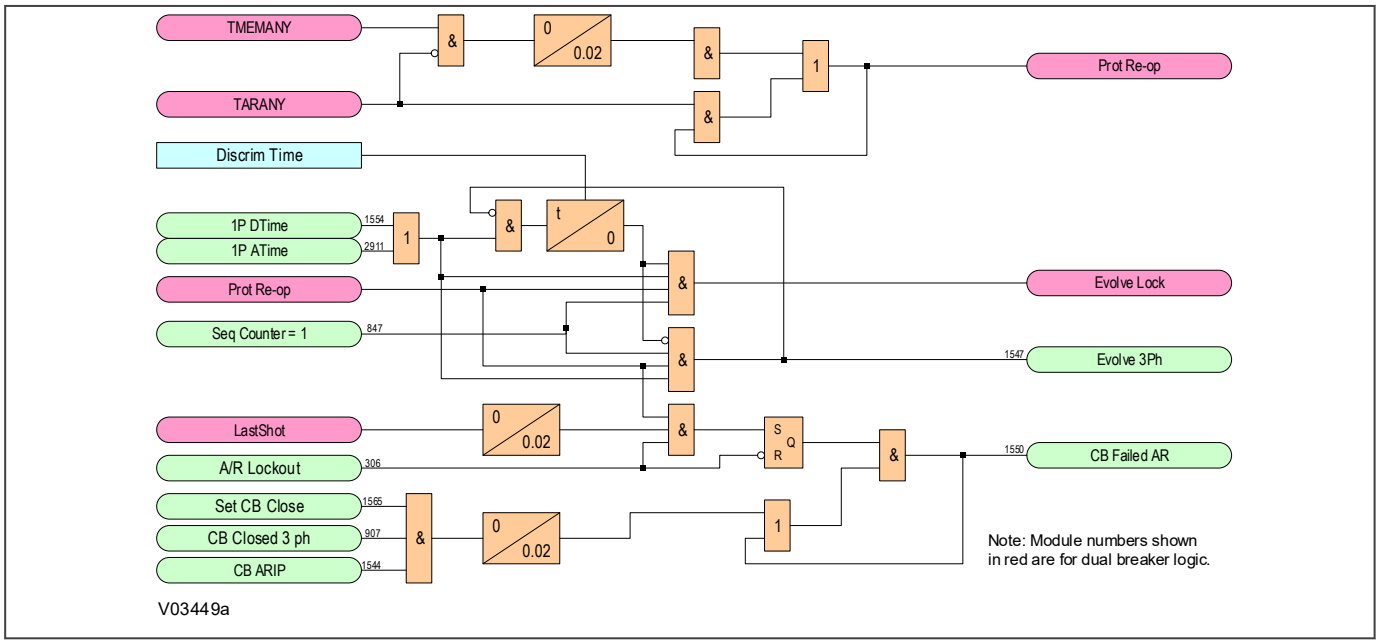


Figure 218: Protection reoperation and evolving fault logic (module 20)

12.4.7.5 FAULT MEMORY LOGIC DIAGRAM

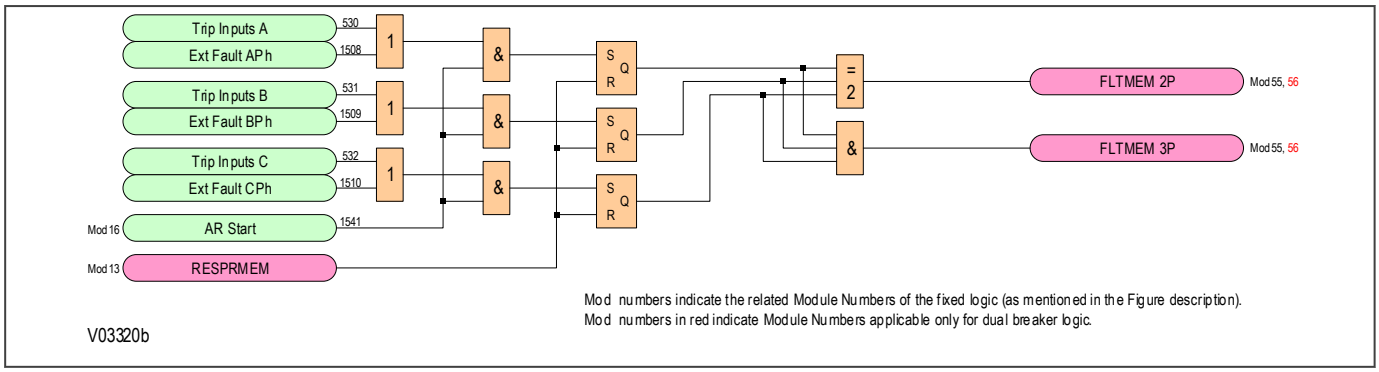


Figure 219: Fault memory logic (module 15)

12.4.8 AUTORECLOSE IN PROGRESS

The AR In Progress module produces various signals to indicate to other modules and functions that an Autoreclose operation is currently in progress.

12.4.8.1 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM

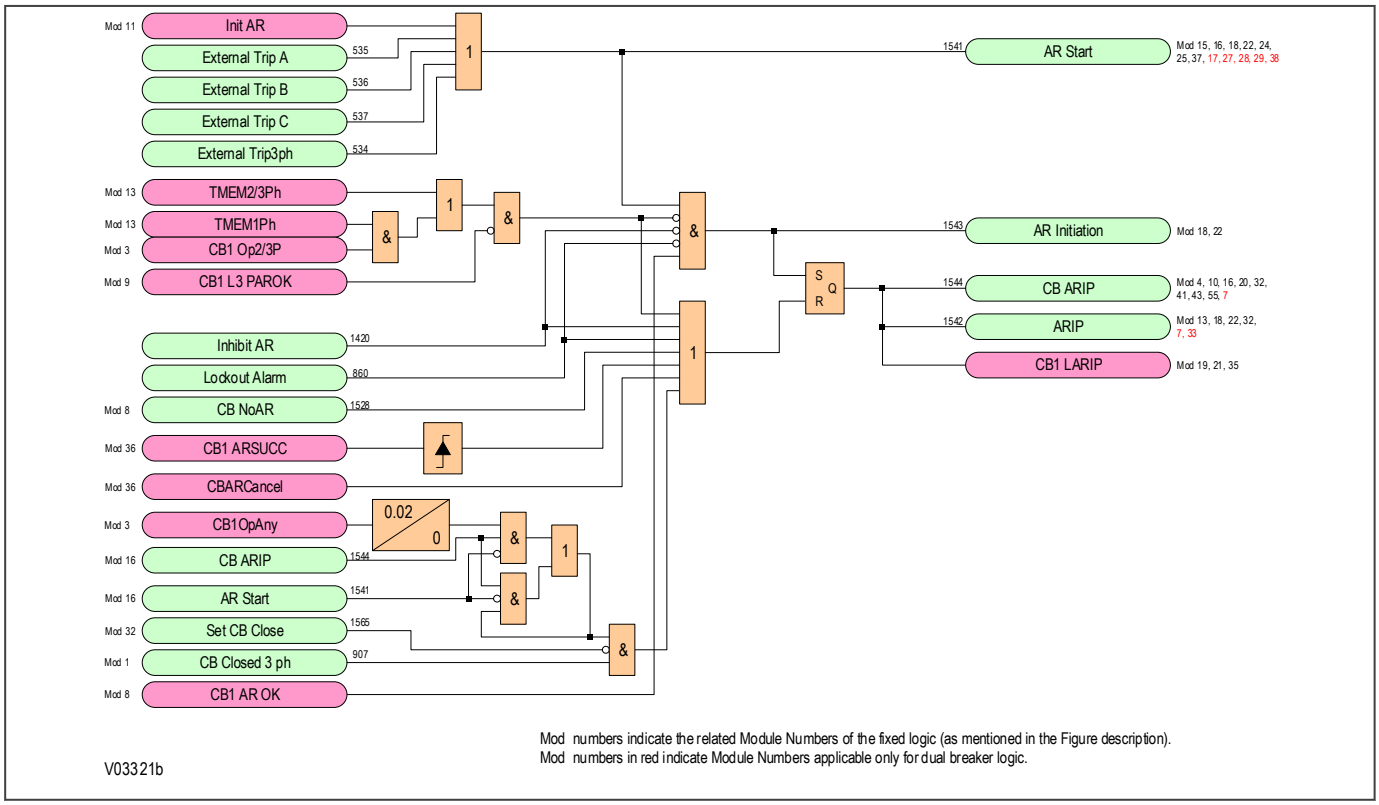


Figure 220: Autoreclose in progress logic (module 16)

12.4.9 SEQUENCE COUNTER

The Autoreclose logic includes a counter for counting the number of Autoreclose shots. This is referred to as the sequence counter. The sequence counter has a value of zero if Autoreclose is not in progress. Following a trip, and subsequent Autoreclose initiation, the sequence counter is incremented. The counter provides output signals indicating how many initiation events have occurred in any Autoreclose cycle. These signals are available as user indications and are used in the logic to select the appropriate dead times or, for a persistent fault, force a lockout.

It is possible to skip the first Autoreclose attempt by enabling the ***AR Skip Shot 1*** setting. If this is set, the sequence counter will skip the first Autoreclose attempt (Shot 1) and move to the second (Shot 2) immediately upon Autoreclose initiation. Each time the protection trips the sequence counter is incremented by 1. The Autoreclose logic compares the sequence counter value to the number of Autoreclose shots setting ***AR Shots***. If the counter value exceeds this setting then the Autoreclose is locked out. If Autoreclose is successful, the sequence counter resets to zero.

12.4.9.1 AUTORECLOSE SEQUENCE COUNTER LOGIC DIAGRAM

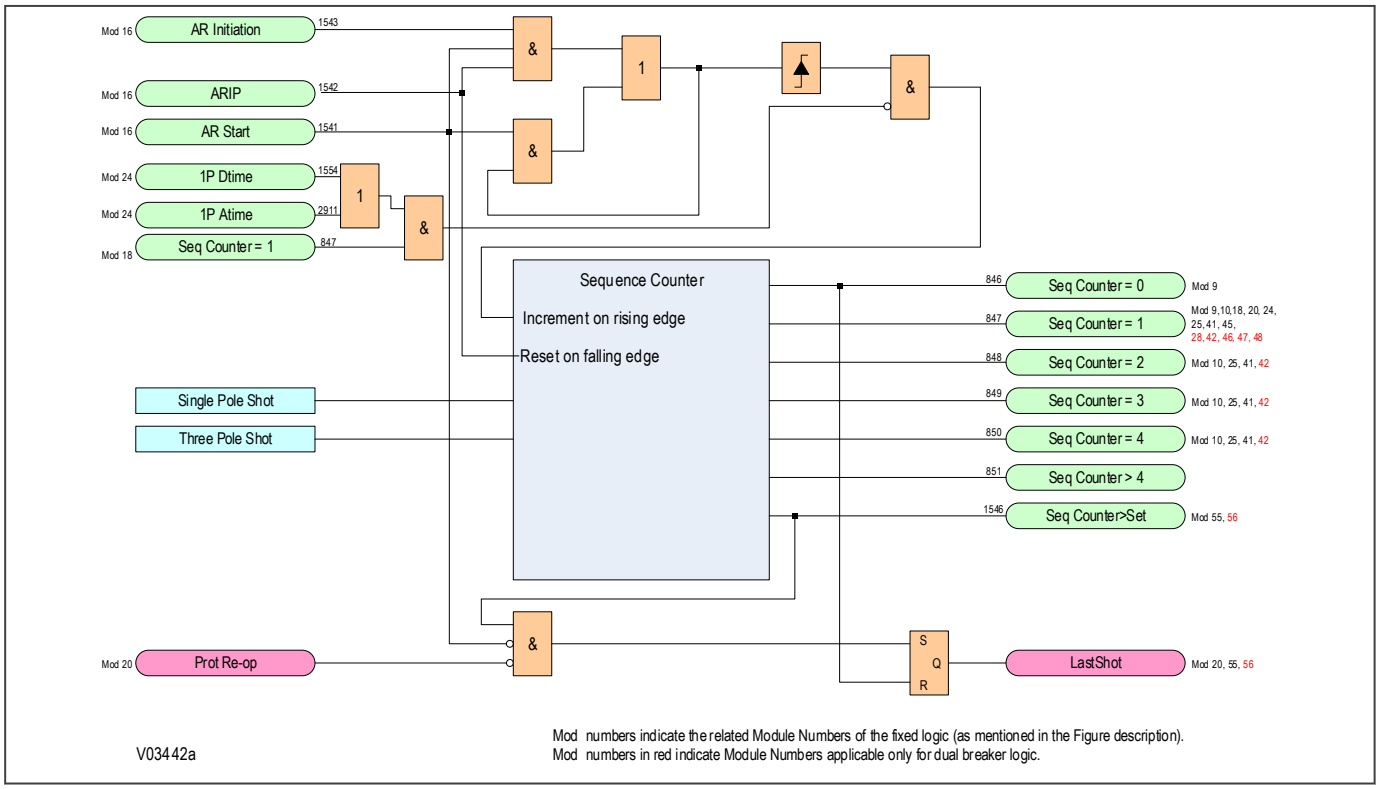


Figure 221: Autoreclose sequence counter logic (module 18)

12.4.10 AUTORECLOSE CYCLE SELECTION

The Autoreclose cycle selection logic is responsible for determining whether the Autoreclose will start as single-phase or three-phase.

12.4.10.1 SINGLE-PHASE AUTORECLOSE CYCLE SELECTION LOGIC DIAGRAM

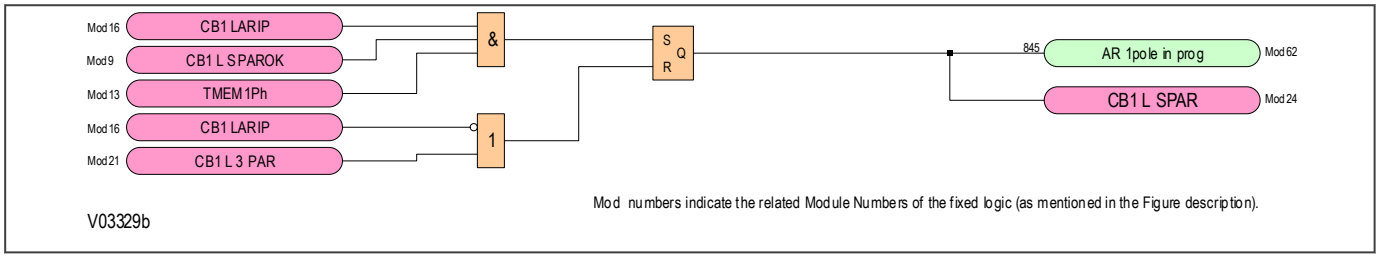


Figure 222: Single-phase autoreclose cycle selection logic (module 19)

12.4.10.2 3-PHASE AUTORECLOSE CYCLE SELECTION

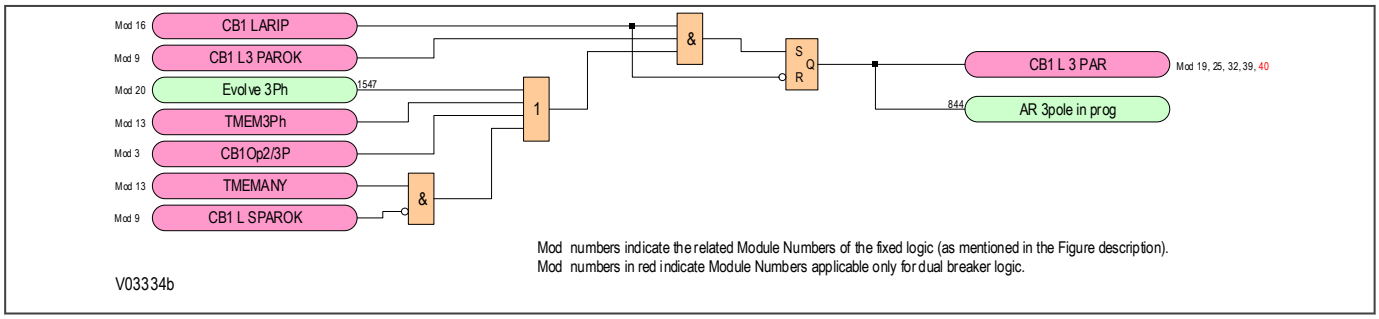


Figure 223: Three-phase autoreclose cycle selection logic (module 21)

12.4.11 DEAD TIME CONTROL

Once an Autoreclose cycle has started, the conditions to enable the dead time to run are determined by the menu settings, the circuit breaker status, the protection status, the nature of the AR cycle (single-phase or three-phase), and the opto-isolated inputs from external sources.

Three settings are involved in controlling the dead time start:

- ***DT Start by Prot***
- ***3PDTStart WhenLD***
- ***DTStart by CB Op***

The ***DT Start by Prot*** determines how the protection action will initiate a dead time. The setting is always visible and has three options `Protection Reset`, `Protection Op` (protection operation), and `Disable` which should be selected if you don't want protection action to start the dead time. These options set the basic conditions for starting the dead time.

Selecting protection operation to start the dead time can, optionally, be qualified by a check that the line is dead.

Selecting protection reset to start the dead time can, optionally, be qualified by a check, that the circuit breaker is open (***DTStart by CB Op***) before starting the dead time. For three-phase tripping applications, there is a further option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time.

If ***DT Start by Prot*** is disabled, the circuit breaker must be open for the dead time to start. For three-phase tripping applications, there is an option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time. To check that the line is dead, set ***3PDTStart WhenLD*** to `enabled`. To check that the circuit breaker is open, set ***DTStart by CB Op*** to `Enabled`.

12.4.11.1 DEAD TIME START ENABLE LOGIC DIAGRAM

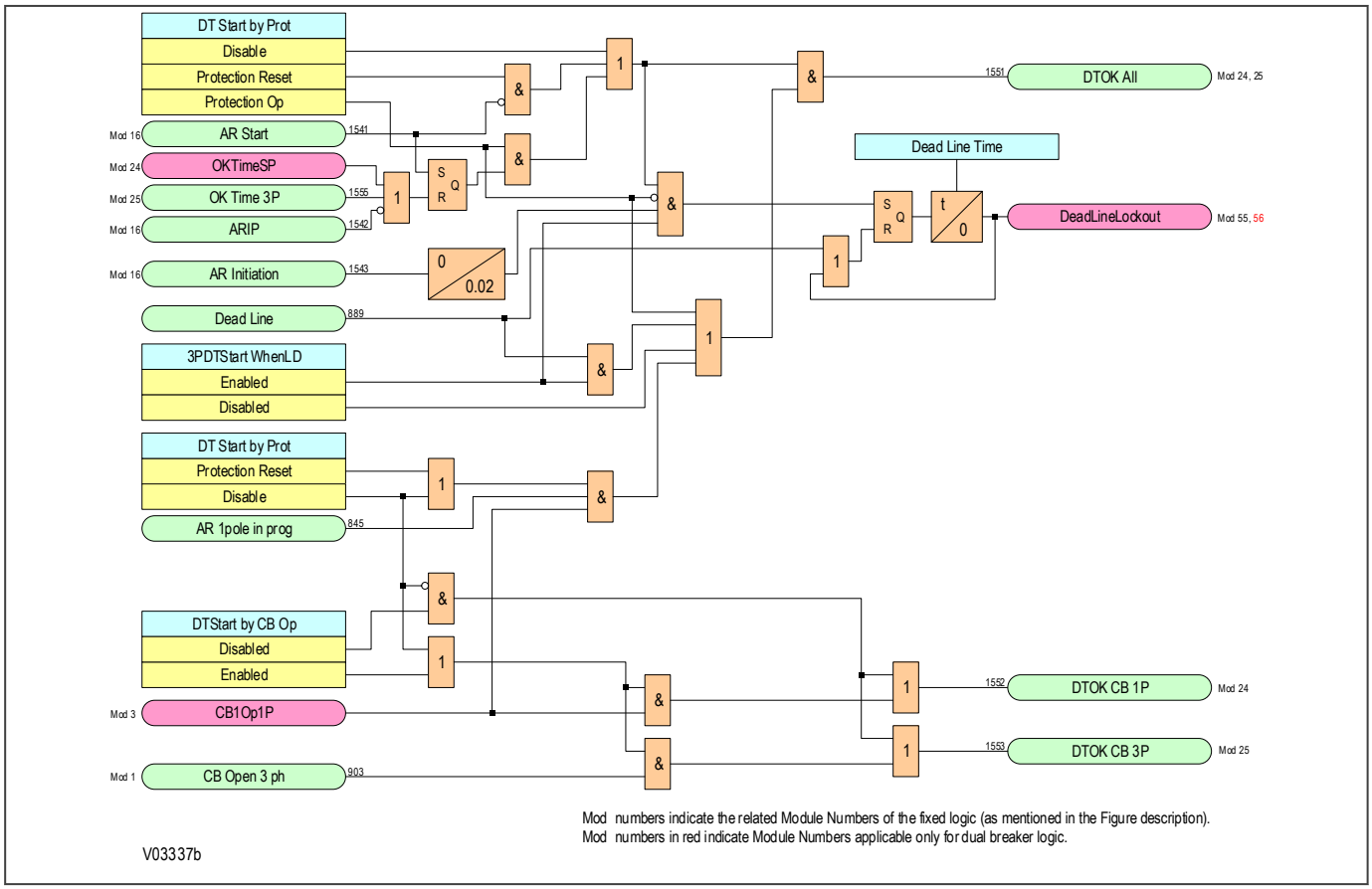


Figure 224: Dead time start enable logic (module 22)

12.4.11.2 SINGLE-PHASE DEAD TIME AND ADAPTIVE AUTORECLOSE (AAR) LOGIC

The autoreclose scheme is adaptive when the ***Adaptive SP AR*** setting is `Enabled`. The adaptive autoreclose is only available for single pole autoreclose applications. When adaptive autoreclose is enable, ***SP AR Dead Time*** is hidden, and two new timer settings are visible: ***SP Min Dead Time*** and ***SP Max Dead Time***. Those two timers are the limits of the single pole dead time.

The Fault Type and Arc Extinction (FTAE) detection algorithm is initiated when the ***Adaptive SP AR*** setting is `Enabled` and the ***OkTimeSP*** signal of the dead time is high, as shown in Module 24.

The breaker open status (***CB Open A PH***/***CB Open B PH*** /***CB Open C PH***) signals are used to identify the single phase to ground fault isolation. The phase voltage information is provided to a six cycle buffer and the δ and |Vs| and derivatives are fed to the ***FTAED*** Module.

The output signals from the ***FTAED*** Module are the ***P_Fault***, ***T_Fault*** and the ***Arc complete*** signals (DDBs: 2909 AAR Perm Flt, 2910 AAR Temp Flt and 2924 AAR Arc Extinct) which indicate a permanent fault detection, transient fault detection and arc extinction.

The ***T_Fault*** signal is high during a transient fault condition and the Arc complete signal is high only after complete de-ionisation of the faulted arc during transient fault conditions. During a permanent fault condition, the ***P_Fault*** output signal of the AAR module is high, and it is routed to the AR lockout logic diagram (Module 55) to stop further autoreclose actions if required.

The ***CB1SPDTCOMP*** and ***CB1SPATCOMP*** signals in Module 24 are inputs to the Circuit Breaker Auto Close Logic Diagram (Module 32). The ***CB1SPDTCOMP*** signal is high in cases where the ***Adaptive SP AR*** is setting is `0` and ***CB1SPATCOMP*** is high in cases where the ***Adaptive SP AR*** setting is `1`.

12.4.11.3 1-PHASE DEAD TIME LOGIC DIAGRAM

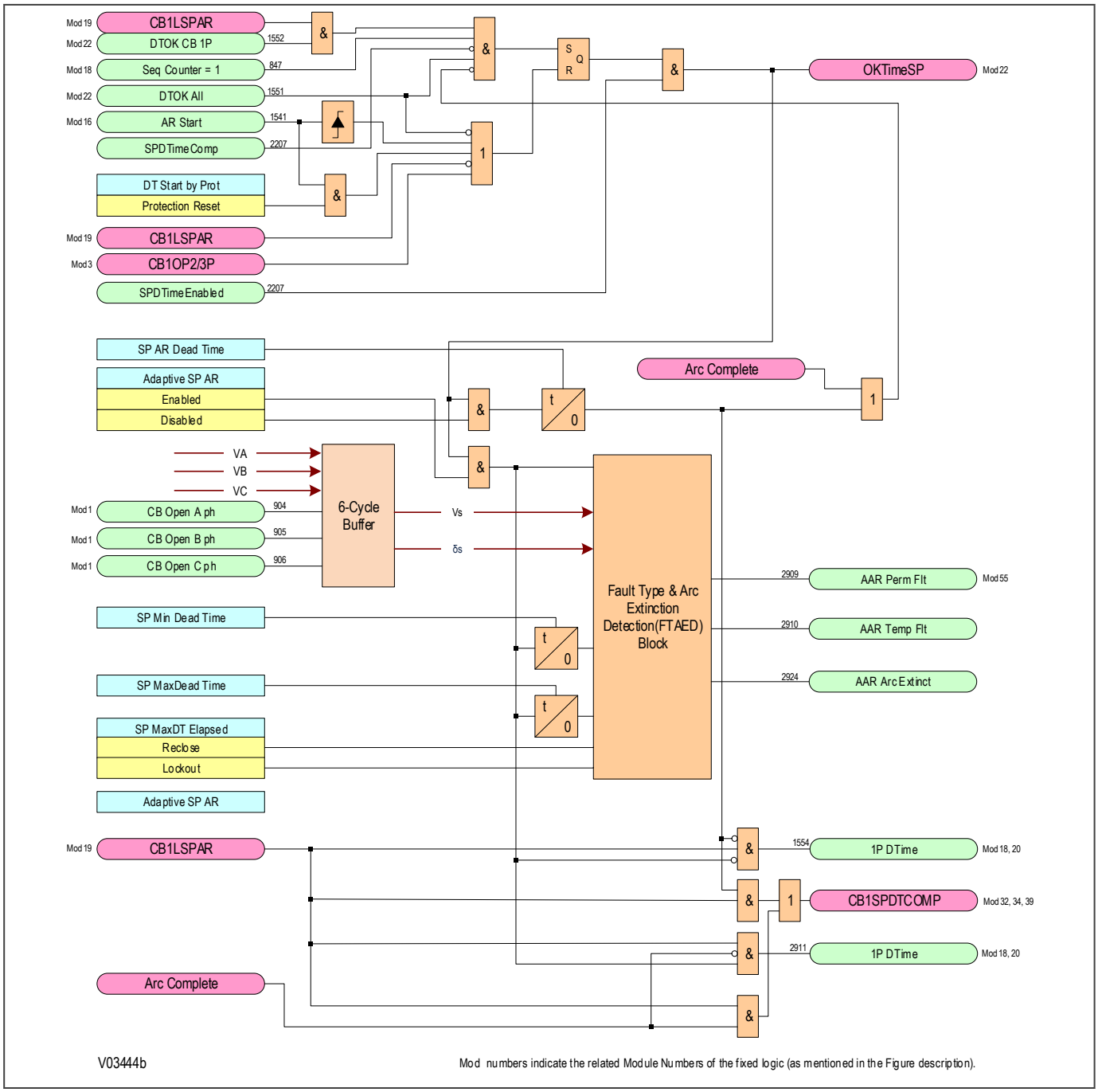


Figure 225: Single-phase dead time logic (module 24)

12.4.11.4 3-PHASE DEAD TIME LOGIC DIAGRAM

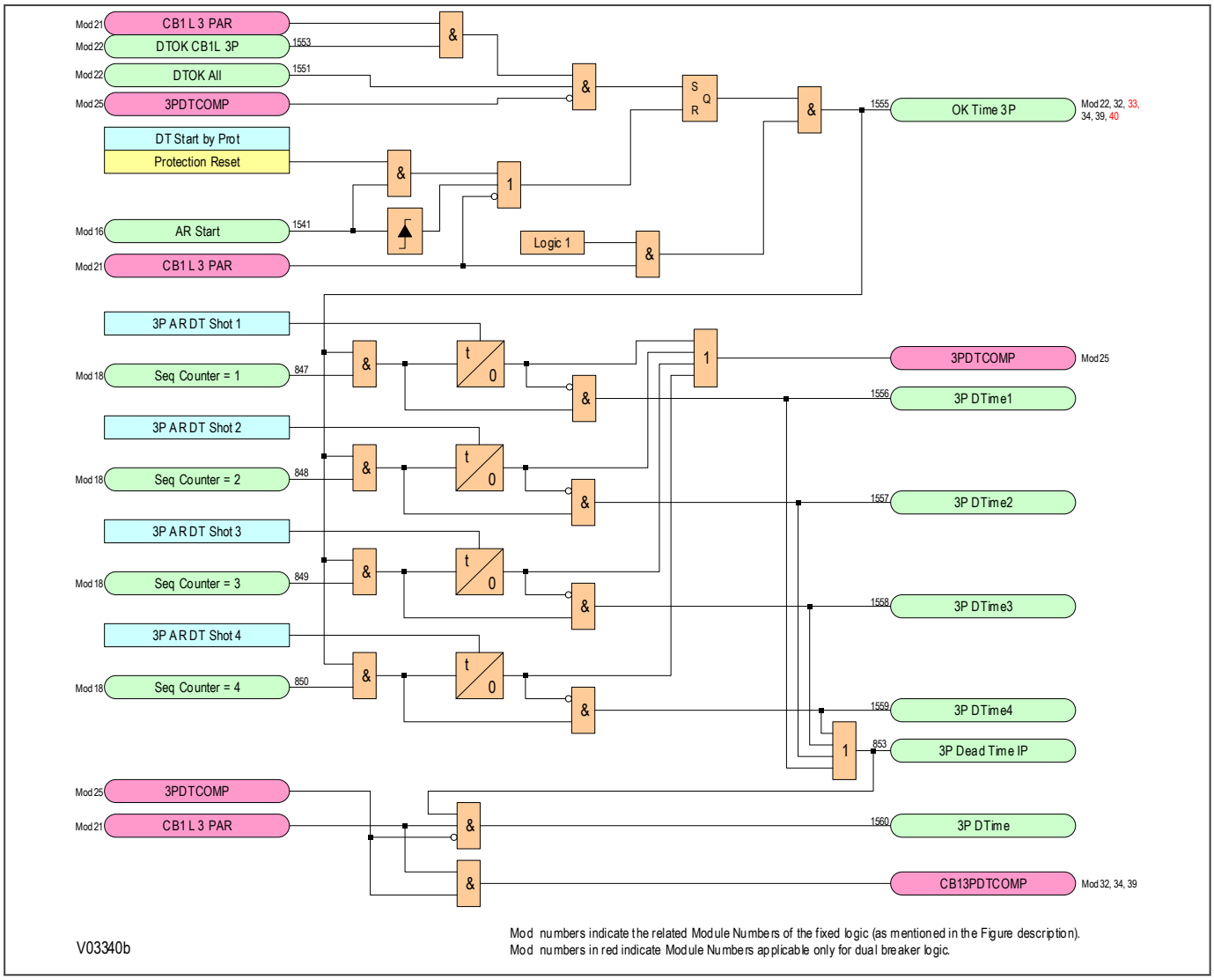


Figure 226: Three-phase dead time logic (module 25)

12.4.12 CIRCUIT BREAKER AUTOCLOSE

Autoclose logic takes effect when dead times have expired.

The Autoclose logic checks that all necessary conditions are satisfied before issuing an Autoclose command to the circuit breaker control scheme.

Before a circuit breaker can be closed, it must be healthy (sufficient energy to close, and if necessary re-trip) and it must not be in a lockout condition.

For three-phase Autoreclose, the circuit breaker must be open on all three phases and the appropriate system check conditions must be met. For single-phase Autoreclose, the circuit breaker must be open on that phase.

The Autoclose command is a pulse lasting 100 milliseconds. Another command (***Set CB Close***) to set the circuit breaker to close is asserted as well as the Autoclose command. This signal will remain set either until the end of the Autoreclose cycle, or until the next protection operation. These commands are used to initiate the Reclaim Time logic and the Autoreclose Shot Counter logic.

12.4.12.1 CIRCUIT BREAKER AUTOCLOSE LOGIC DIAGRAM

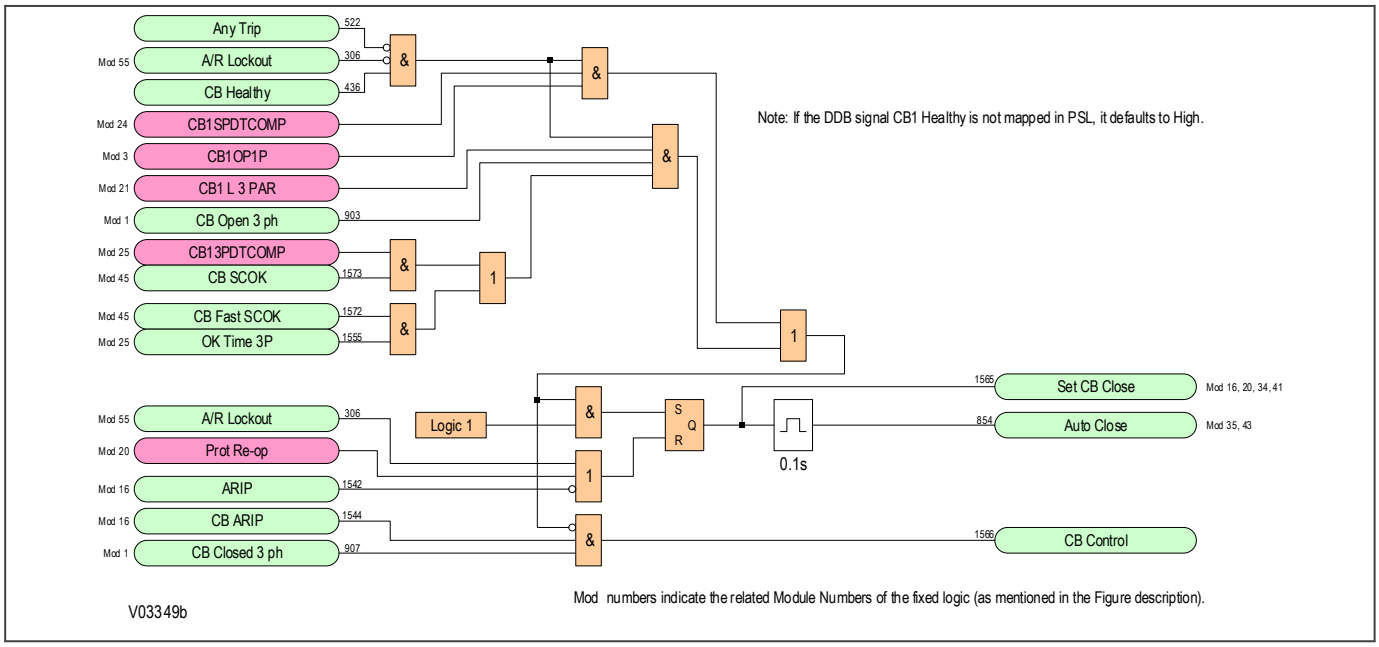


Figure 227: Circuit breaker autoclose logic (module 32)

12.4.13 RECLAIM TIME

If the protection operates again before the reclaim time has expired, the corresponding sequence counter is incremented. At the same time, any “dead time complete” (….DTCOMP) signals are reset and the logic is prepared for the next dead time to start when conditions are suitable. The operation also resets the signal that would set the circuit breaker to close, and stops and resets the reclaim timer. The reclaim time starts again if the signal to set a circuit breaker to close goes high following completion of a dead time in a subsequent Autoreclose cycle. Where the reclaim extend time signal is set, the reclaim time cannot time out and reset the Autoreclose cycle before the time delayed protection has fully operated

If the circuit breaker is closed and has not tripped again when the reclaim time expires, signals are generated to indicate successful Autoreclose. These signals increment the relevant circuit breaker successful Autoreclose shot counters and reset the relevant Autoreclose in progress signal.

The “successful Autoreclose” signals generated from the logic can be reset by various commands and settings options available under *CB CONTROL* menu settings as follows:

If ***Res AROK by UI*** is set to `Enabled`, all the signals can be reset by user interface command ***Reset AROK Ind*** from the *CB CONTROL* menu.

If ***Res AROK by NoAR*** is set to `Enabled`, the signals for each circuit breaker can be reset by temporarily generating an Autoreclose disabled signal according to the logic shown.

If ***Res AROK by Ext*** is set to `Enabled`, the signals can be reset by activation of an external input signal appropriately mapped in the PSL.

If ***Res AROK by TDly*** is set to `Enabled`, the signals are automatically reset after a time delay set in ***AROK Reset Time***.

12.4.13.1 PREPARE RECLAIM INITIATION LOGIC DIAGRAM

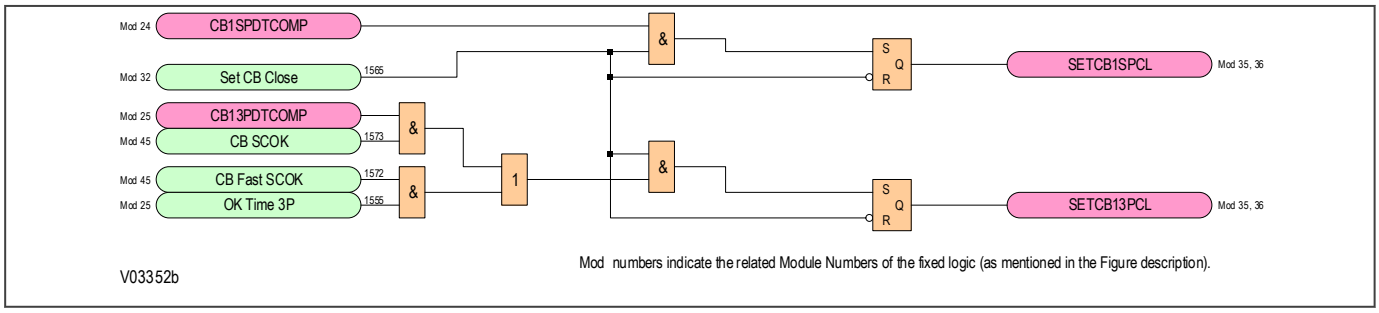


Figure 228: Prepare reclaim initiation logic (module 34)

12.4.13.2 RECLAIM TIME LOGIC DIAGRAM

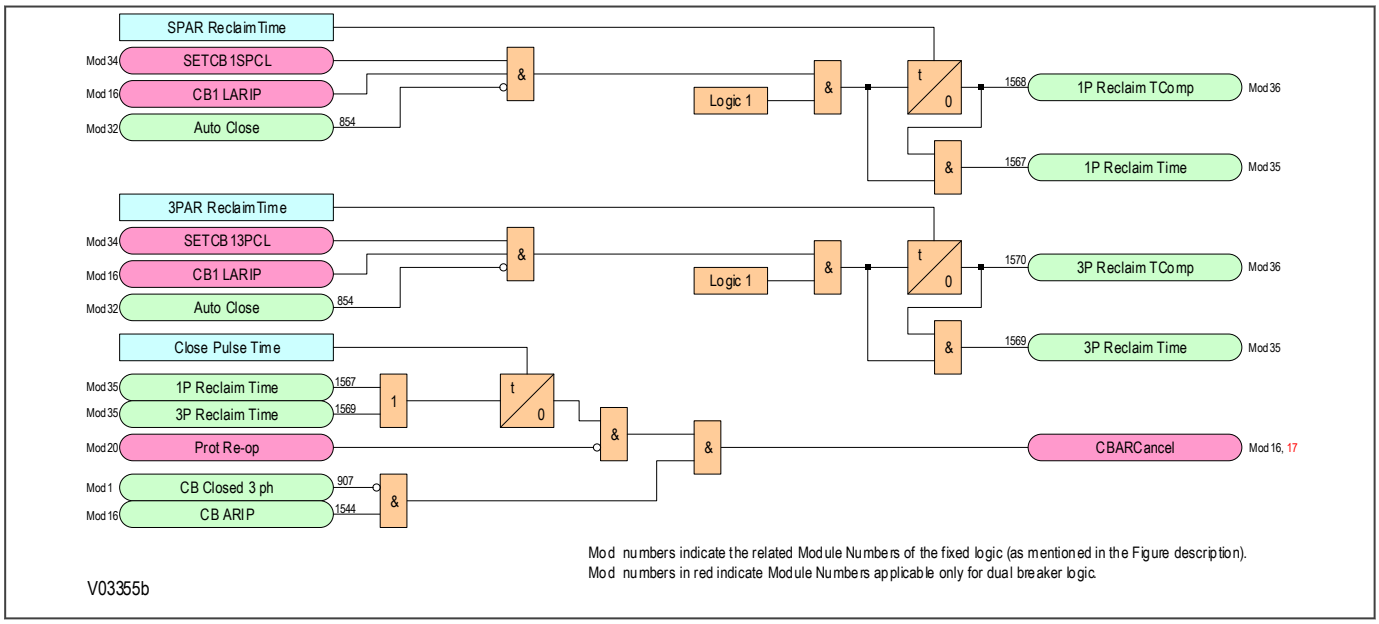


Figure 229: Reclaim time logic (module 35)

12.4.13.3 SUCCESSFUL AUTORECLOSE SIGNALS LOGIC DIAGRAM

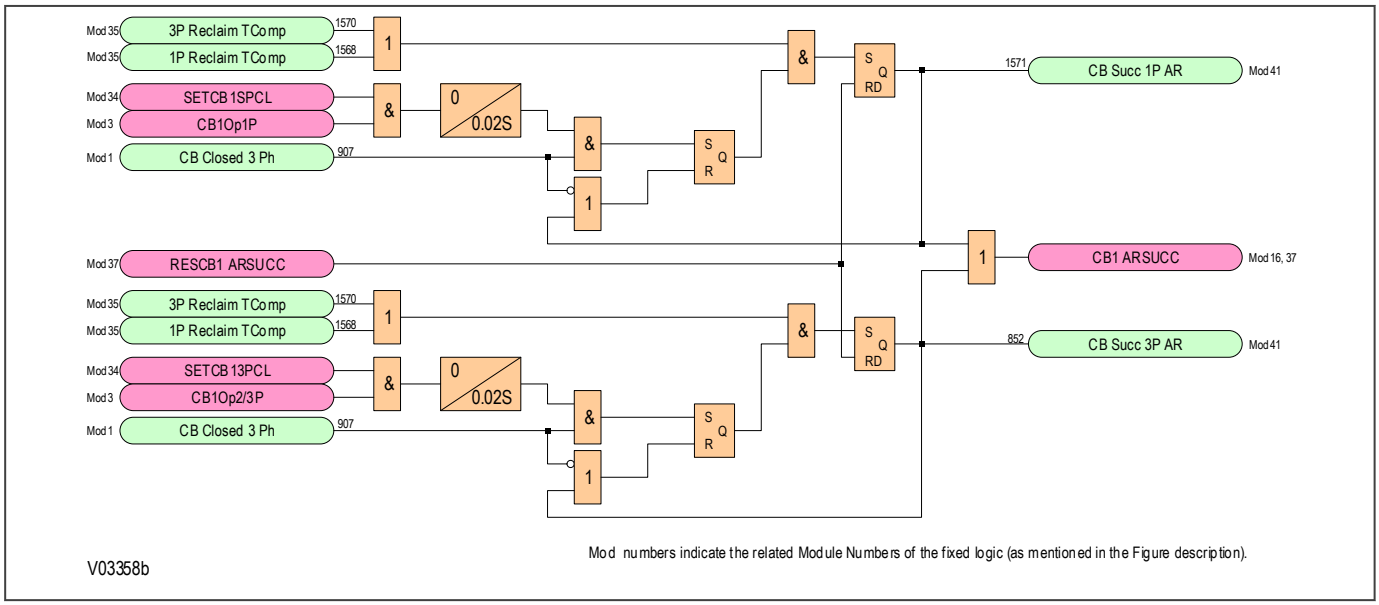


Figure 230: Successful autoreclose signals logic (module 36)

12.4.13.4 AUTORECLOSE RESET SUCCESSFUL INDICATION LOGIC DIAGRAM

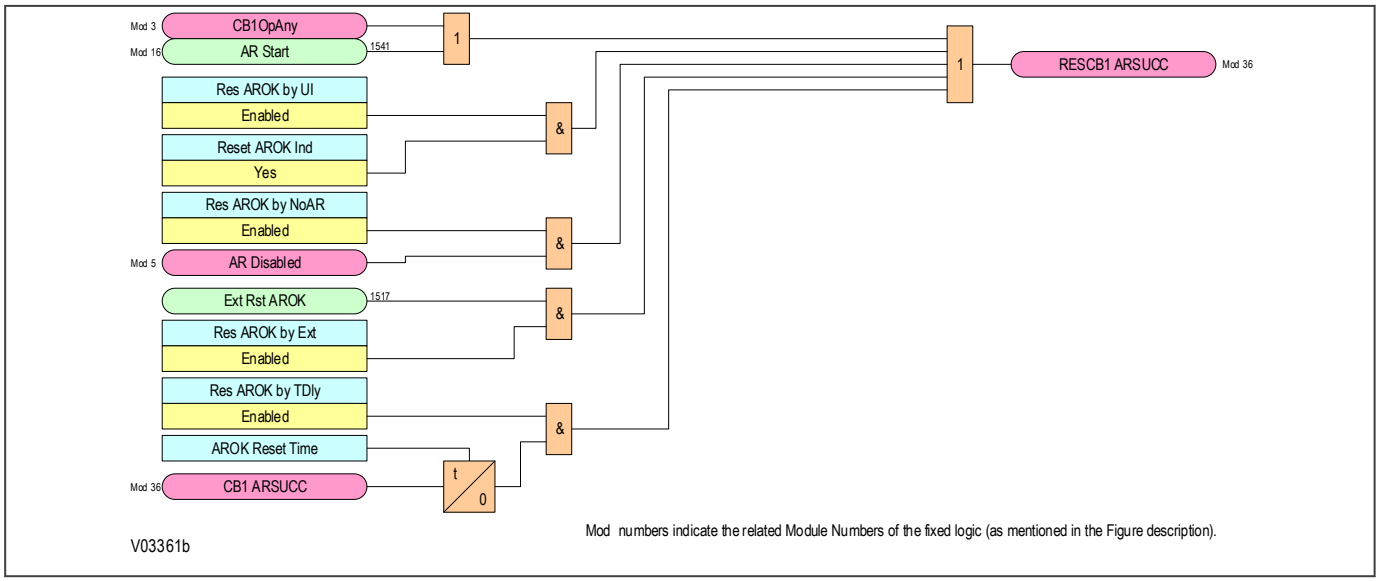


Figure 231: Autoreclose reset successful indication logic (module 37)

12.4.14 CB HEALTHY AND SYSTEM CHECK TIMERS

This logic provides signals to cancel Autoreclose if the circuit breaker is not healthy (for example low gas pressure) or system check conditions are not satisfied (for example required line & bus voltage conditions) when the scheme is ready to close the circuit breaker.

At the completion of a dead time, the logic starts an Autoreclose healthy timer. If a circuit breaker healthy signal becomes high before the Autoreclose healthy time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker healthy signal stays low, then, at the end of the Autoreclose healthy time, a circuit breaker unhealthy alarm is raised. This forces the Autoreclose sequence to be cancelled.

Additionally, at the completion of any three-phase dead time, the logic starts an Autoreclose check synchronism timer. If the circuit breaker synchronism-check OK signal goes high before the time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker synchronism-check OK signal stays low, then when the Autoreclose check synchronism timer expires, an alarm is set to inform that the check synchronism is not satisfied and cancels the Autoreclose cycle.

12.4.14.1 CB HEALTHY AND SYSTEM CHECK TIMERS LOGIC DIAGRAM

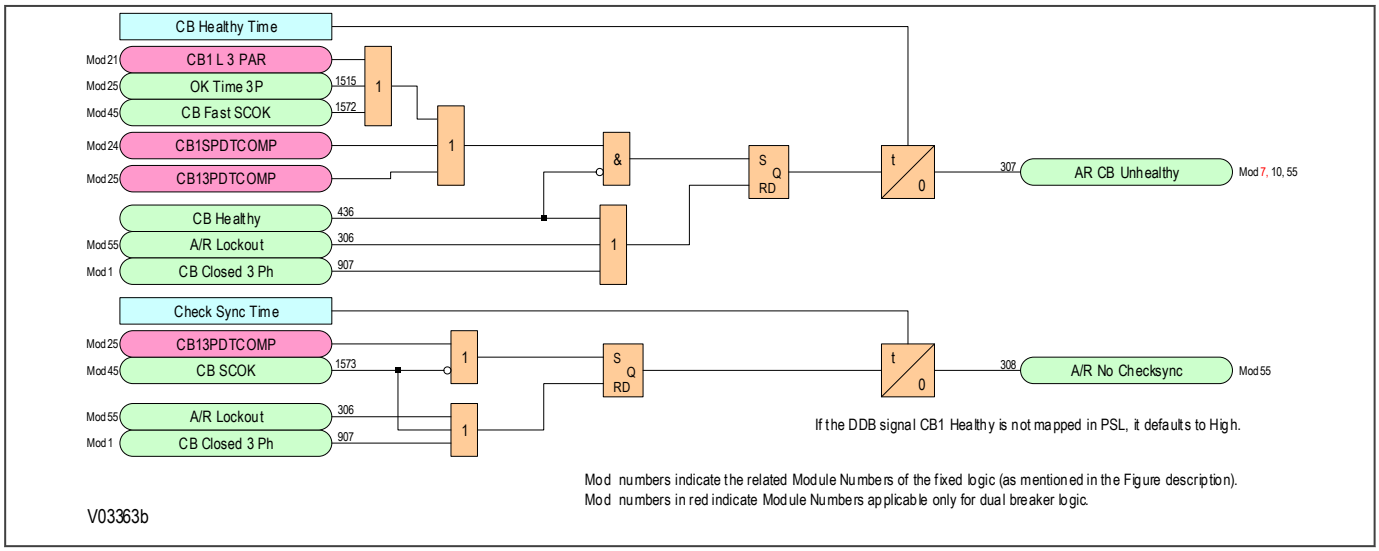


Figure 232: Circuit breaker healthy and system check timers healthy logic (module 39)

12.4.15 AUTORECLOSE SHOT COUNTERS

A number of counters are provided to enable analysis of circuit breaker Autoreclose history. The counters are stored in non-volatile memory, so that the data is maintained even in the event of a failure of the auxiliary supply. The counter values are accessible through the *CB CONTROL* column. The counters can be reset manually, or by activation of an input appropriately mapped in the PSL.

The logic provides the following summary information for each circuit breaker

- Overall total number of shots (Number of Autoreclose attempts)
- Number of successful 1st shot single-phase Autoreclose sequences
- Number of successful 1st shot three-phase Autoreclose sequences
- Number of successful 2nd shot three-phase Autoreclose sequences
- Number of successful 3rd shot three-phase Autoreclose sequences
- Number of successful 4th shot three-phase Autoreclose sequences
- Number of failed Autoreclose cycles which forced a circuit breaker to lockout

12.4.15.1 AUTORECLOSE SHOT COUNTERS LOGIC DIAGRAM

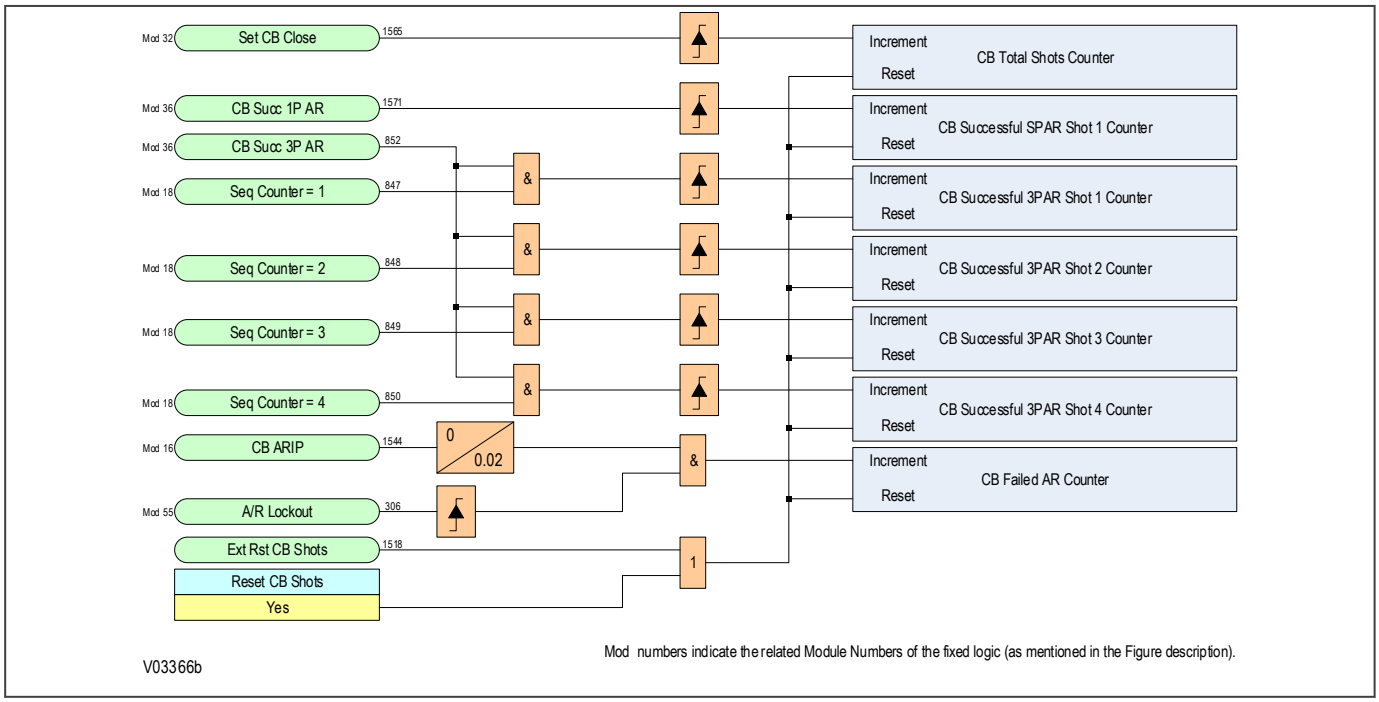


Figure 233: Autoreclose shot counters logic (module 41)

12.4.16 CIRCUIT BREAKER CONTROL

12.4.16.1 CB CONTROL LOGIC DIAGRAM

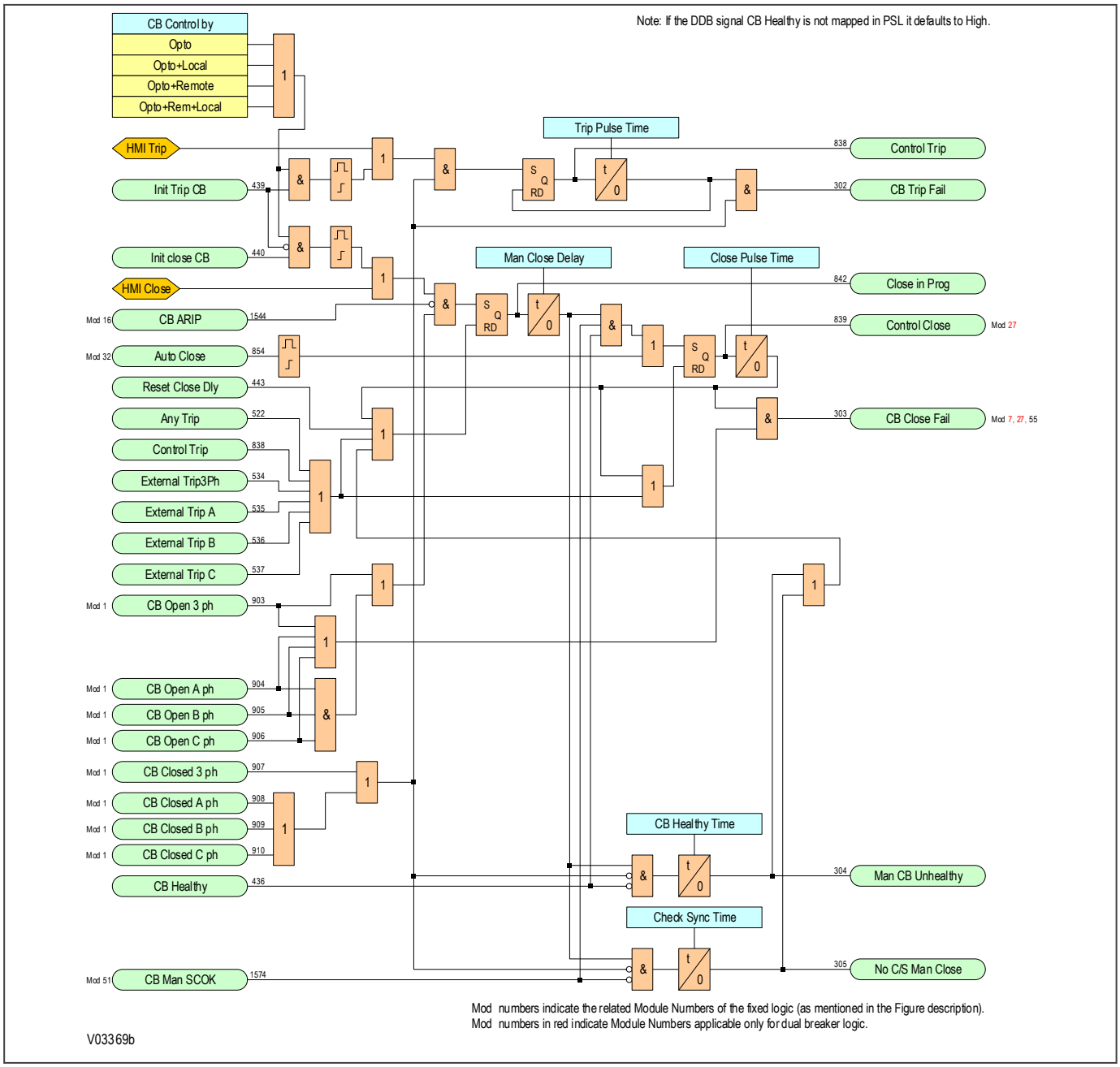


Figure 234: CB control logic (module 43)

12.4.17 CIRCUIT BREAKER TRIP TIME MONITORING

The circuit breaker trip time monitoring logic checks for correct circuit breaker tripping following the issue of a protection trip signal. When the protection trip signal is issued, a timer controlled by the ***Trip Pulse Time*** setting in the *CB CONTROL* column is started.

If the circuit breaker trips correctly the timer resets. If Autoreclose is enabled and the timer resets, the cycle continues. If the circuit breaker fails to trip correctly within the set time, the Autoreclose cycle is forced to lock out and a signal is issued indicating that the circuit breaker failed to trip in response to the protection operation.

12.4.17.1 CB TRIP TIME MONITORING LOGIC DIAGRAM

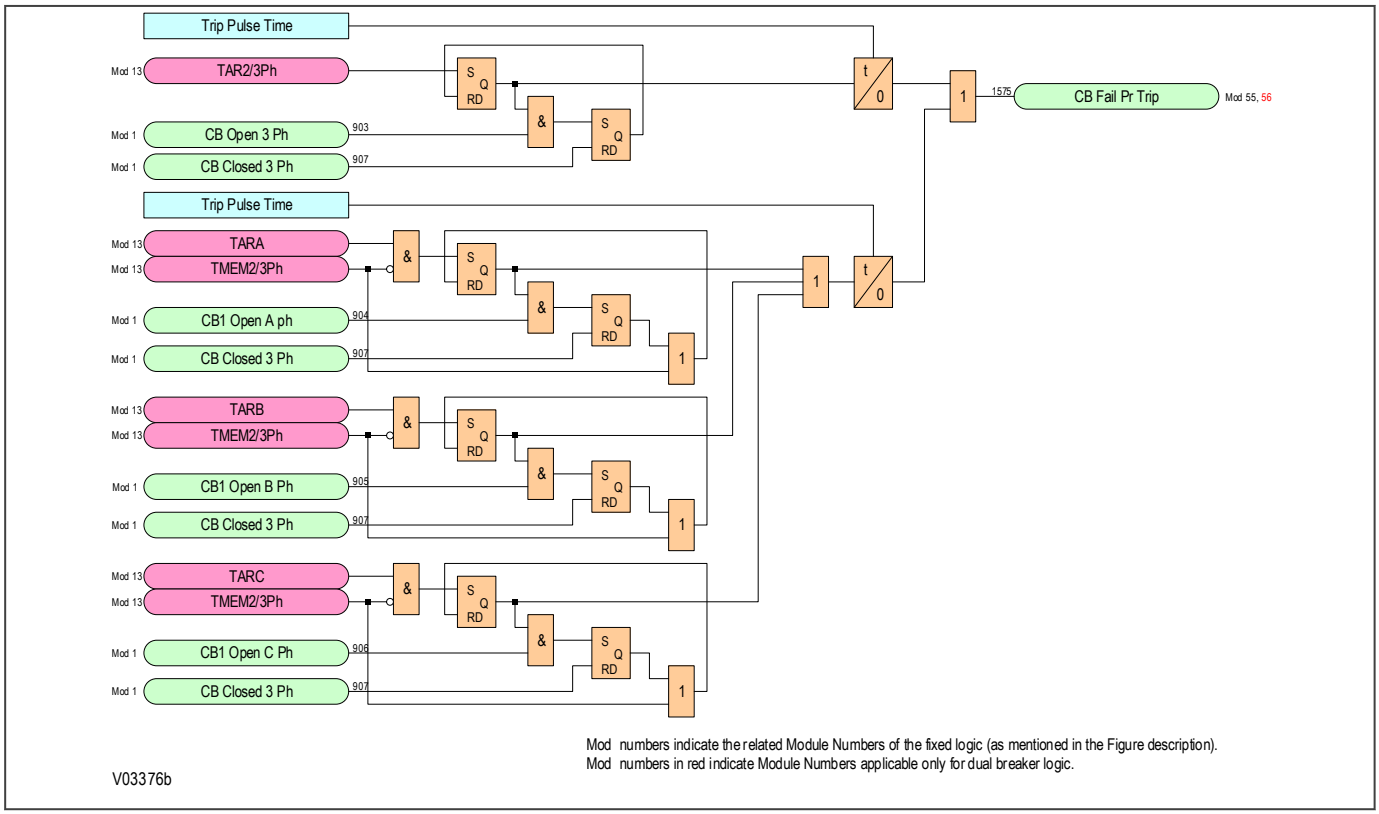


Figure 235: Circuit breaker trip time monitoring logic (module 53)

12.4.18 AUTORECLOSE LOCKOUT

A number of events will cause Autoreclose lockout. If this happens an Autoreclose lockout alarm is raised. In this condition, Autoreclose cannot be initiated until the corresponding lockout has been reset.

The following events force Autoreclose lockout:

- Protection operation during reclaim time. Following the final Autoreclose attempt, if the protection operates during the reclaim time, the AR cycle goes to AR lockout and the Autoreclose function is disabled until the AR lockout condition is reset.
- Persistent fault. A fault is considered persistent if the protection re-operates after the last permitted shot.
- Block Autoreclose. If the block Autoreclose DDB is asserted whilst Autoreclose is in progress, the cycle goes to lockout.
- Protection function selection. Setting ‘Block AR’ against a particular protection function in the AUTORECLOSE column means that operation of the protection will block Autoreclose and force lockout.
- Circuit breaker failure to close. If a circuit breaker fails to close Autoreclose is blocked and forced to lockout.
- Circuit breaker remains open at the end of the reclaim time. An Autoreclose lockout is forced if the circuit breaker is open at the end of the reclaim time.

- Circuit breaker fails to close when the close command is issued.
- Circuit breaker fails to trip correctly.
- Three-phase dead time started by 'line dead' violation. If the line does not go dead within the ***Dead Line Time*** setting, the logic forces the Autoreclose sequence to lockout. Determination of when to start the timer is made in the ***3PDTStart WhenLD*** setting.
- Multi-phase faults. The logic can be set to block Autoreclose either for two-phase or three-phase faults, or to block Autoreclose for three-phase faults only. For this, the setting ***Multi Phase AR*** in the *AUTORECLOSE* column applies.
- Single-phase evolving into multi-phase fault. A discriminating time (***Discrim Time*** in the *AUTORECLOSE* settings) is provided for this feature If, after expiry of the discriminating time, a single-phase fault evolves into a two-phase or three-phase fault, the internal signal 'Evolve Lock' is asserted and the Autoreclose is forced to lockout.

12.4.18.1 CB LOCKOUT LOGIC DIAGRAM

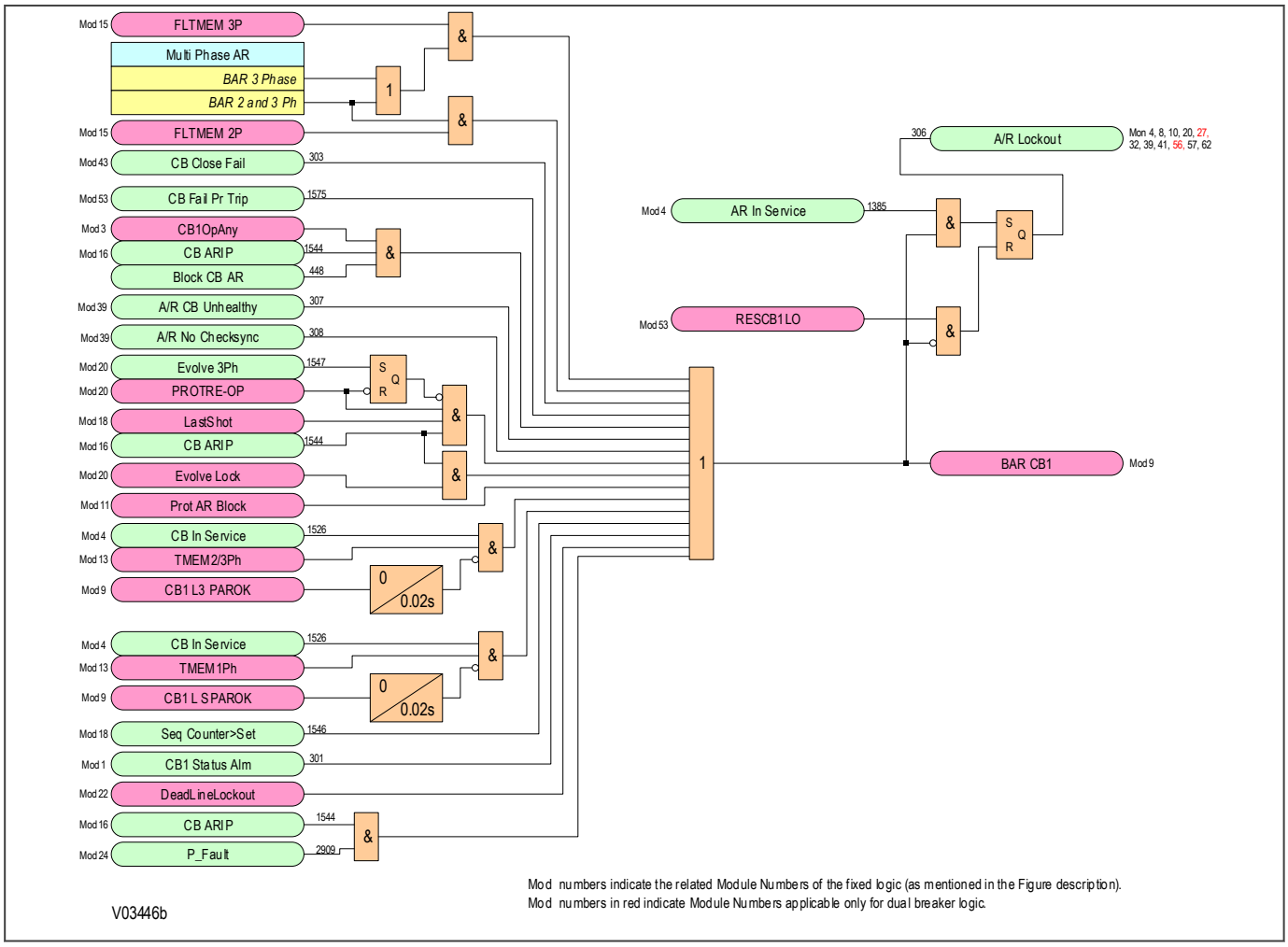


Figure 236: AR lockout logic (module 55)

12.4.19 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to `Enabled`, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to `Enabled`, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to `Enabled`, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to `Enabled`, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is `Enabled`, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

12.4.19.1 RESET CB LOCKOUT LOGIC DIAGRAM

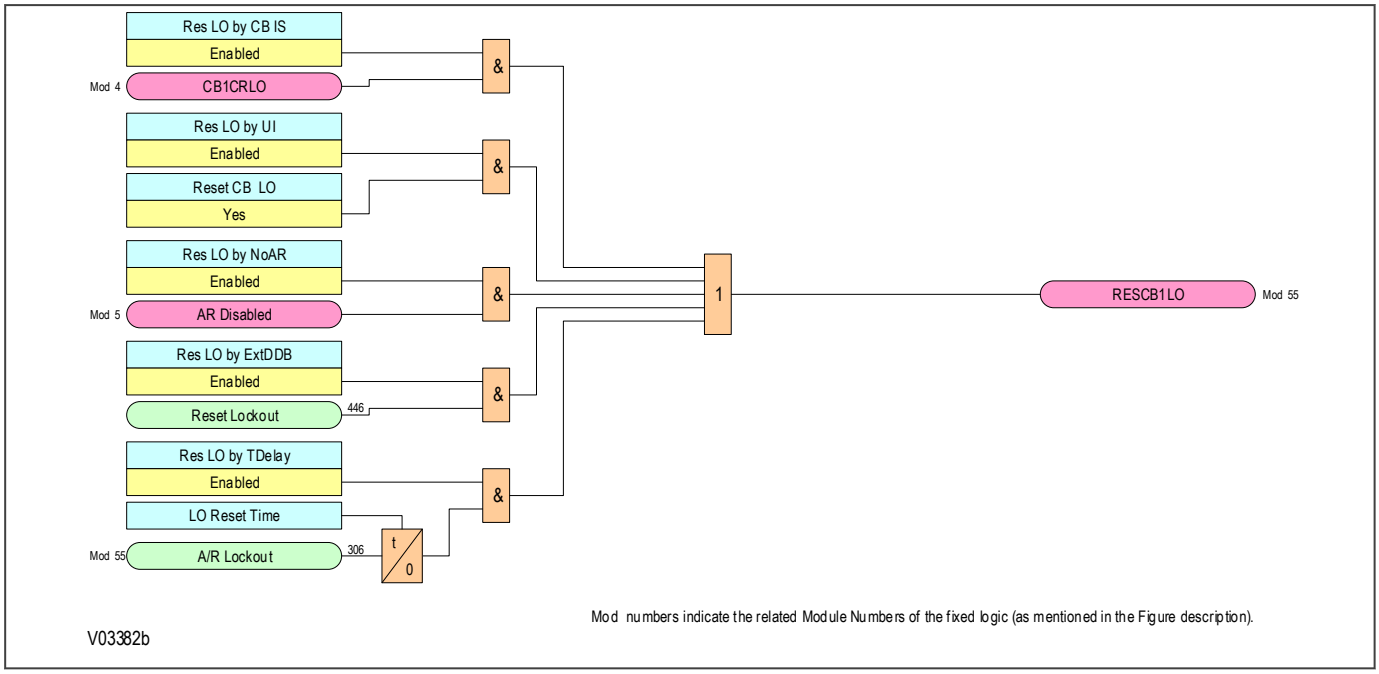


Figure 237: Reset circuit breaker lockout logic (module 57)

12.4.20 POLE DISCREPANCY

In a three-pole CB, certain combinations of poles open and closed are indicative of a problem. The Pole Discrepancy Logic combines an indication of a Pole Discrepancy condition from the CB Monitoring logic with signals from the internal Autoreclose logic to produce a combined Pole Discrepancy indication for the CB.

12.4.20.1 POLE DISCREPANCY LOGIC DIAGRAM

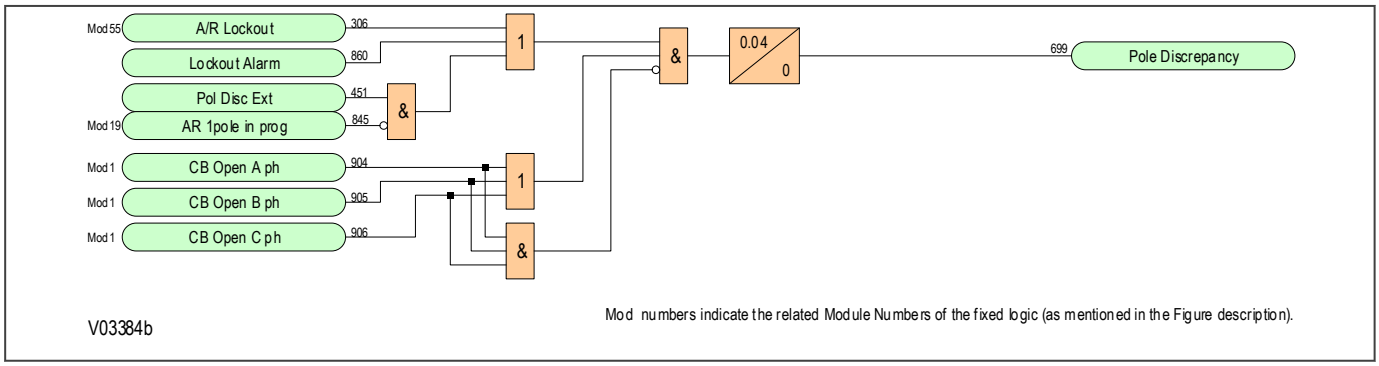


Figure 238: Pole discrepancy logic (module 62)

12.4.21 CIRCUIT BREAKER TRIP CONVERSION

Circuit breakers should only trip single-pole or three-pole. The trip conversion logic ensures that the tripping is either single-pole or three-pole. The trip conversion logic ensures that all conditions that should cause three-pole tripping do so. Indication of the number of phases that caused tripping is provided.

12.4.21.1 CB TRIP CONVERSION LOGIC DIAGRAM

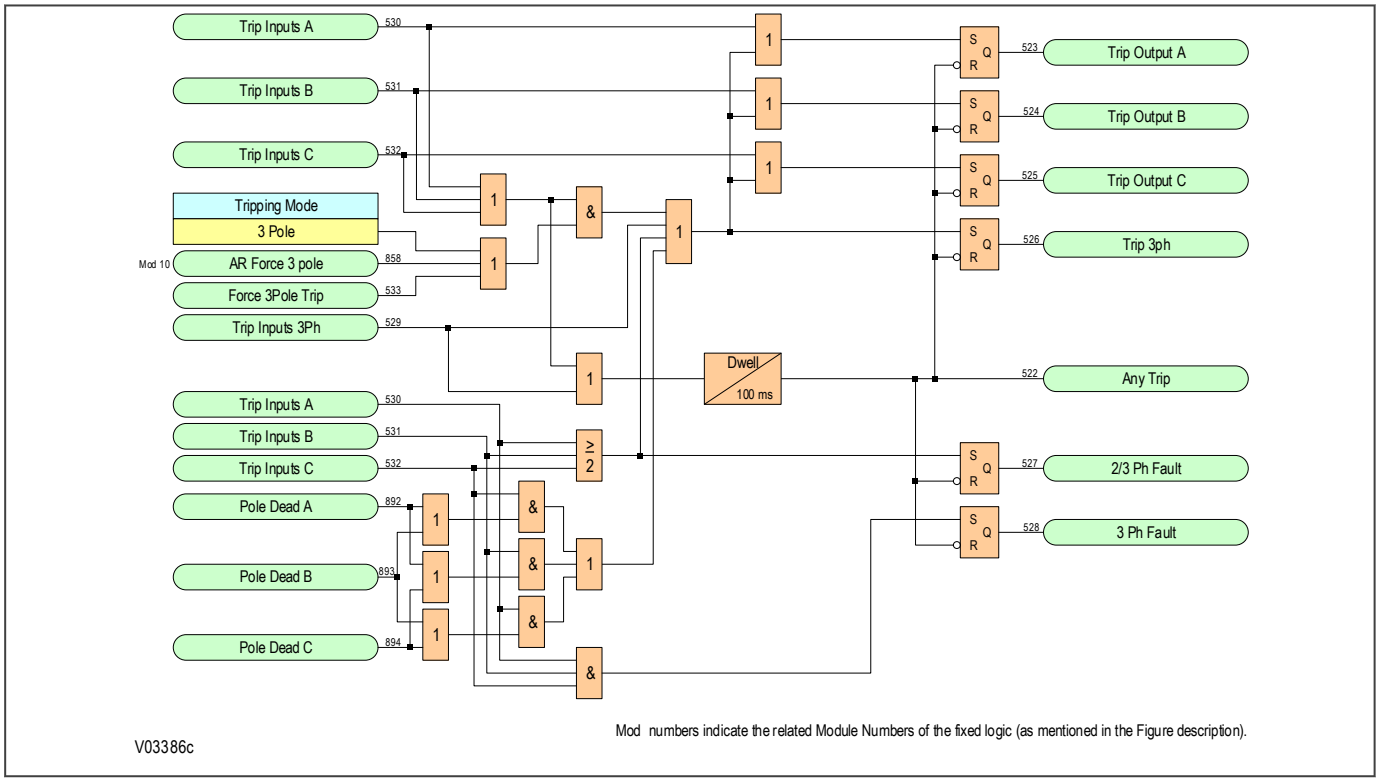


Figure 239: Circuit breaker trip conversion logic (module 63)

12.4.22 MONITOR CHECKS FOR CB CLOSURE

For single-phase Autoreclose neither voltage nor synchronisation checks are needed as synchronising power should be flowing in the two healthy phases. For three-phase Autorelcose, for the first shot (and only the first shot), you can choose to attempt reclosure without performing a synchronisation check. The setting to permit Autoreclose without checking synchronising conditions is ***CB SC Shot 1***.

Otherwise, synchronising checks on voltages, relative frequencies, and relative phase angles are needed to ensure that sympathetic conditions exist before CB closure is attempted.

The following diagrams detail the Monitor Checks for CB closure.

12.4.22.1 VOLTAGE MONITOR FOR CB CLOSURE

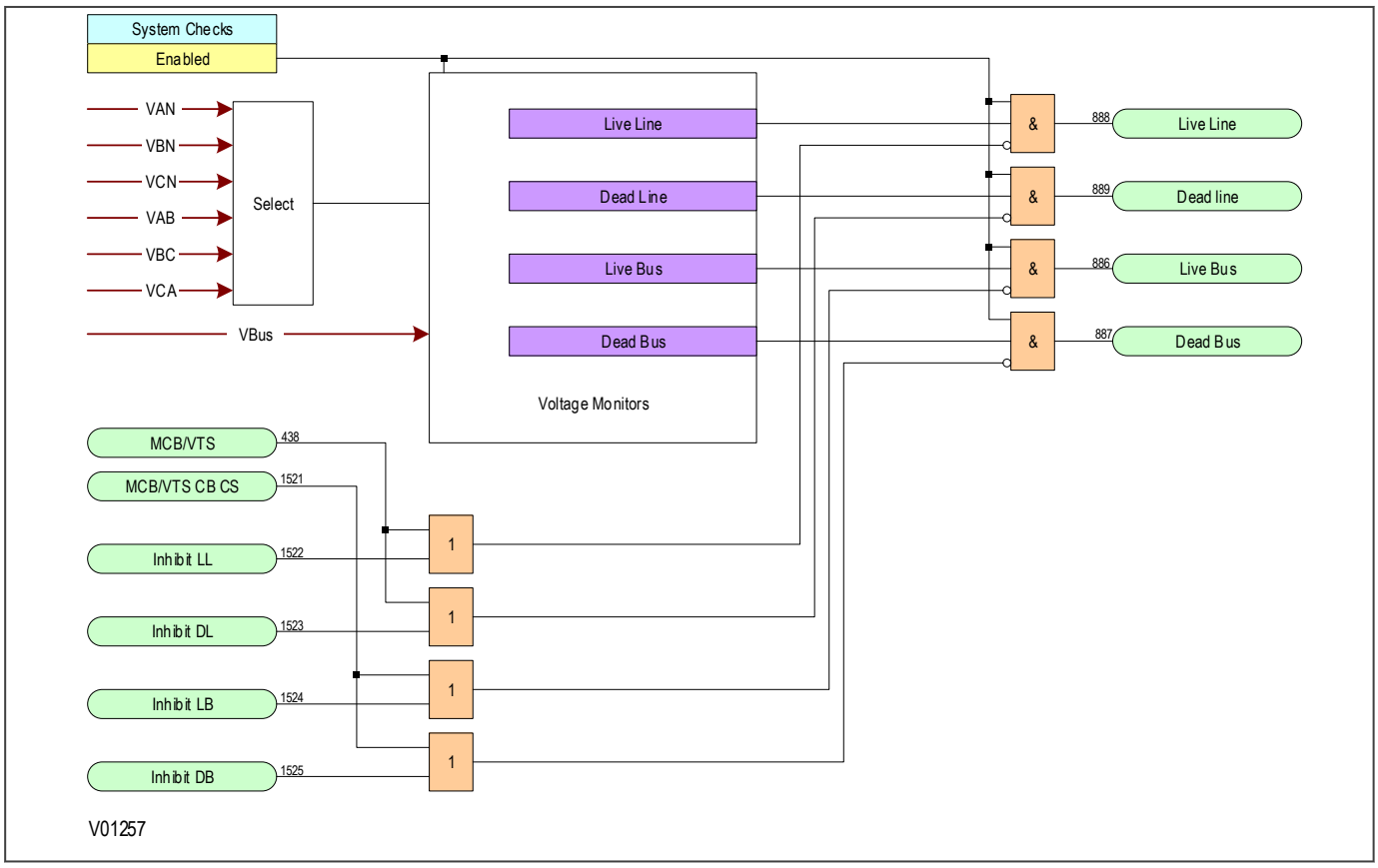


Figure 240: Voltage monitor for CB closure (module 59)

12.4.22.2 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

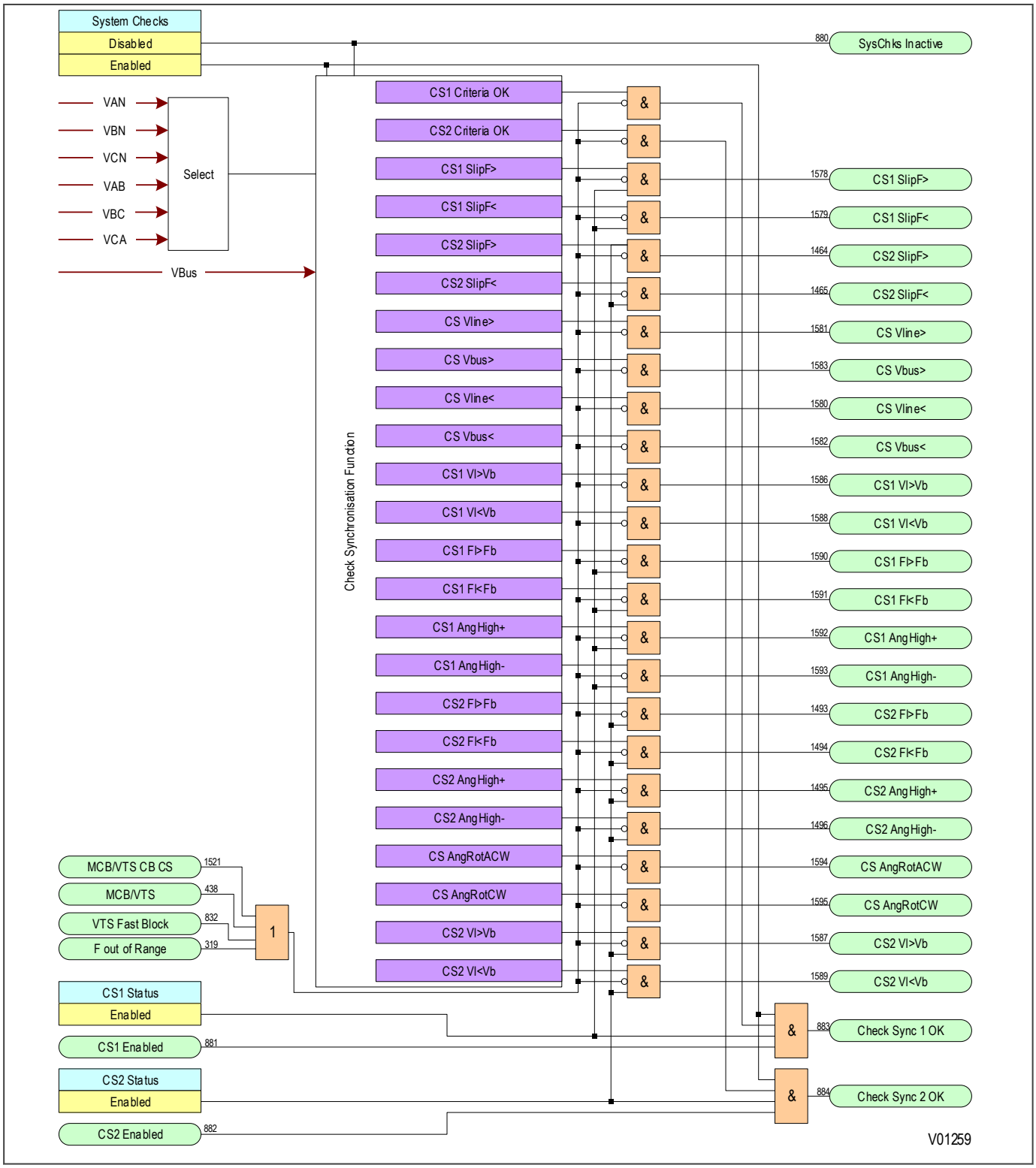


Figure 241: Check synchronisation monitor for CB closure (module 60)

12.4.23 SYNCHRONISATION CHECKS FOR CB CLOSURE

Logical checking of the outputs from the CB closure monitors is performed to generate signals to indicate that it is OK to close circuit breakers.

Signals are provided to indicate that manual CB closure conditions are OK (***CB Man SCOK***), as are signals to indicate that automatic CB closure conditions are OK (***CB SCOK*** and ***CB Fast SCOK***). The ***CB Fast SCOK*** signal allows CB autoreclosure without waiting for the Dead Time to expire.

For single-phase Autoreclose no voltage or synchronism check is required as synchronising power is flowing in the two healthy phases. Three-phase Autoreclose can be performed without checking that voltages are in synchronism for the first shot (and only the first shot). The settings to permit Autoreclose without checking voltage synchronism on the first shot are:

- ***CB1L SC Shot 1*** for circuit breaker 1 as a leader,
- ***CB1F SC Shot 1*** for circuit breaker 1 as a follower,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a leader,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a follower.

When the circuit breaker has closed, the Autoreclose function asserts a DDB signal ***Set CB1 Close***, which indicates that an attempt has been made to close the circuit breaker. At this point, the Reclaim Time starts. If the circuit breaker remains closed after the reclaim timer expires, the Autoreclose cycle is complete, and signals are generated to indicate that Autoreclose was successful. These are:

- ***CB1 Succ 1P AR*** (Single-phase Autoreclose CB1)
- ***CB2 Succ 1P AR*** (Single-phase Autoreclose CB2)
- ***CB1 Succ 3P AR*** (Three-phase Autoreclose CB1)
- ***CB2 Succ 3P AR*** (Three-phase Autoreclose CB2)

These signals increment the relevant circuit breaker successful Autoreclose shot counters, as well as resetting the Autoreclose in progress signal.

The relevant circuit breaker successful Autoreclose shot counters are:

- ***CB1 SUCC SPAR*** (Single-phase Autoreclose CB1)
- CB1 SUCC 3PAR Shot1 (Three-phase Autoreclose CB1, Shot 1)
- CB1 SUCC 3PAR Shot2 (Three-phase Autoreclose CB1, Shot 2)
- CB1 SUCC 3PAR Shot3 (Three-phase Autoreclose CB1, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB1, Shot 4)
- ***CB2 SUCC SPAR*** (Single-phase Autoreclose CB2)
- CB2 SUCC 3PAR Shot1 (Three-phase Autoreclose CB2, Shot 1)
- CB2 SUCC 3PAR Shot2 (Three-phase Autoreclose CB2, Shot 2)
- CB2 SUCC 3PAR Shot3 (Three-phase Autoreclose CB2, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB2, Shot 4)

12.4.23.1 THREE-PHASE AUTORECLOSE SYSTEM CHECK LOGIC DIAGRAM

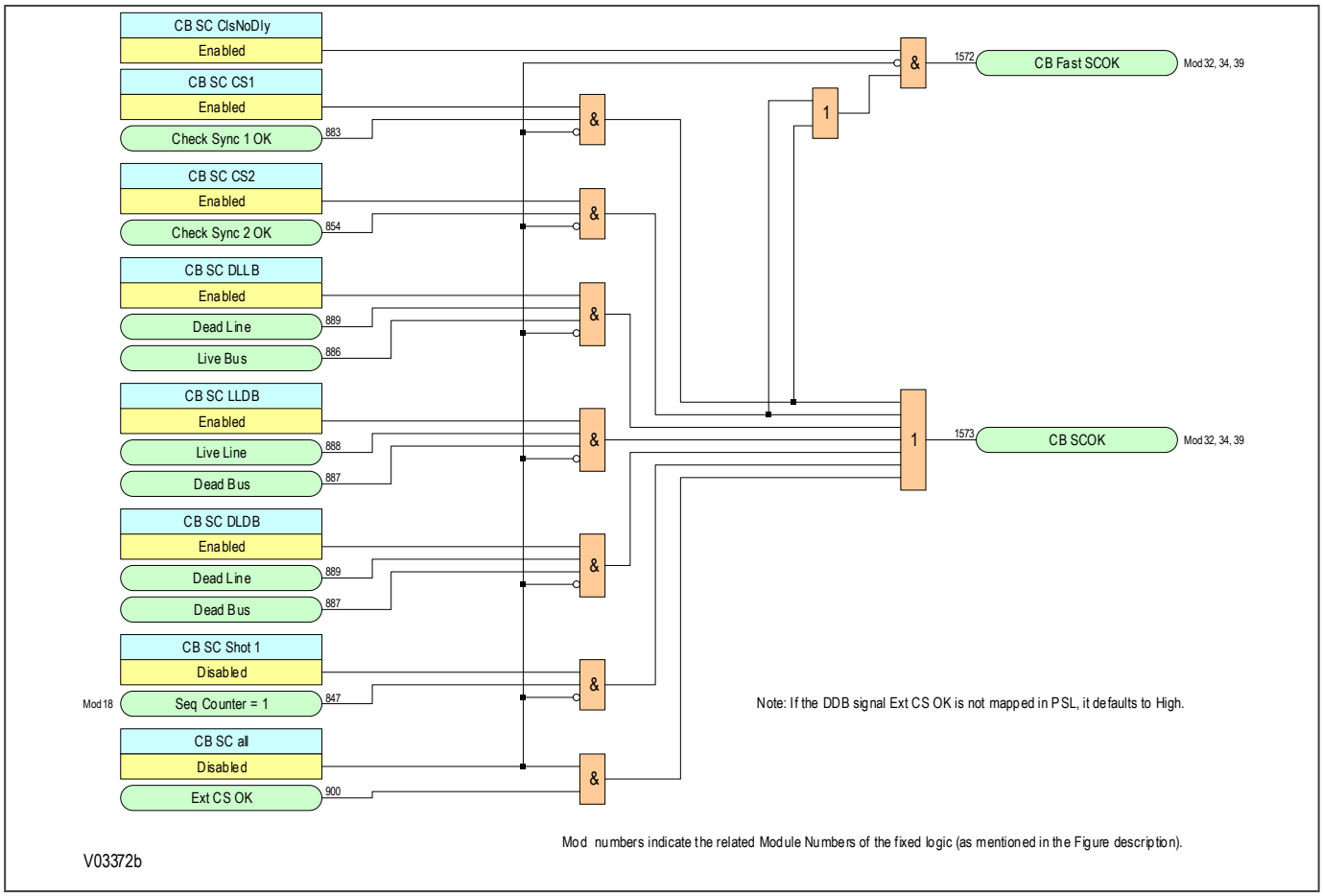


Figure 242: Three-phase autoreclose system check logic (module 45)

12.4.23.2 CB MANUAL CLOSE SYSTEM CHECK LOGIC DIAGRAM

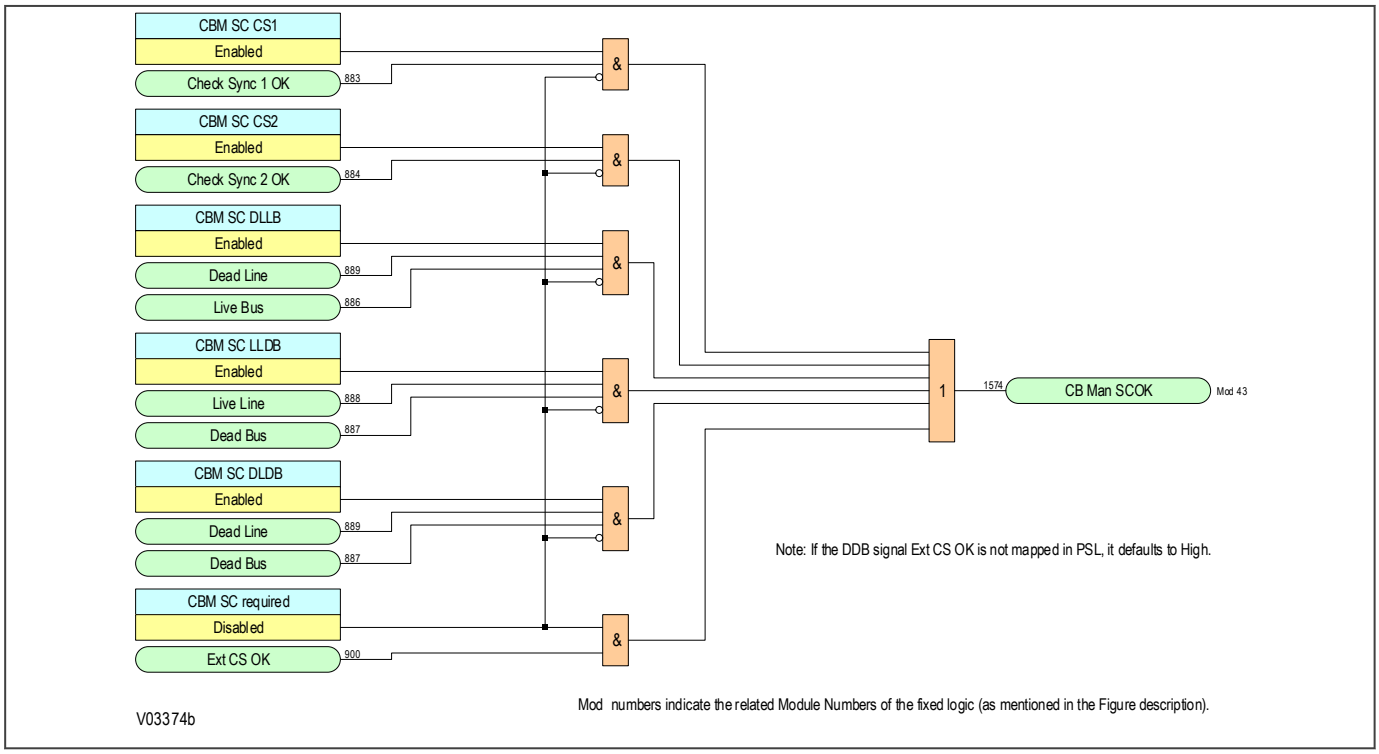


Figure 243: CB manual close system check logic (module 51)

12.5 LOGIC MODULES (DUAL CB)

This section contains a complete set of logic diagrams for dual CB models, which will help to explain the Autoreclose function. Most of the logic diagrams shown are logic modules that comprise the overall Autoreclose system. Some of the diagrams shown are not directly related to Autoreclose functionality, however, they may use some inputs are produce outputs that are used by the Autoreclose system. These diagrams are shown in this section for the sake of completeness.

12.5.1 CIRCUIT BREAKER STATUS MONITOR

The Circuit Breaker State Monitor logic is part of the Monitoring and Control functionality and is fully described in that chapter. The logic diagram is repeated in this section because some of the outputs of this logic module are used as inputs to some of the Autoreclose logic modules.

12.5.1.1 CB STATE MONITOR

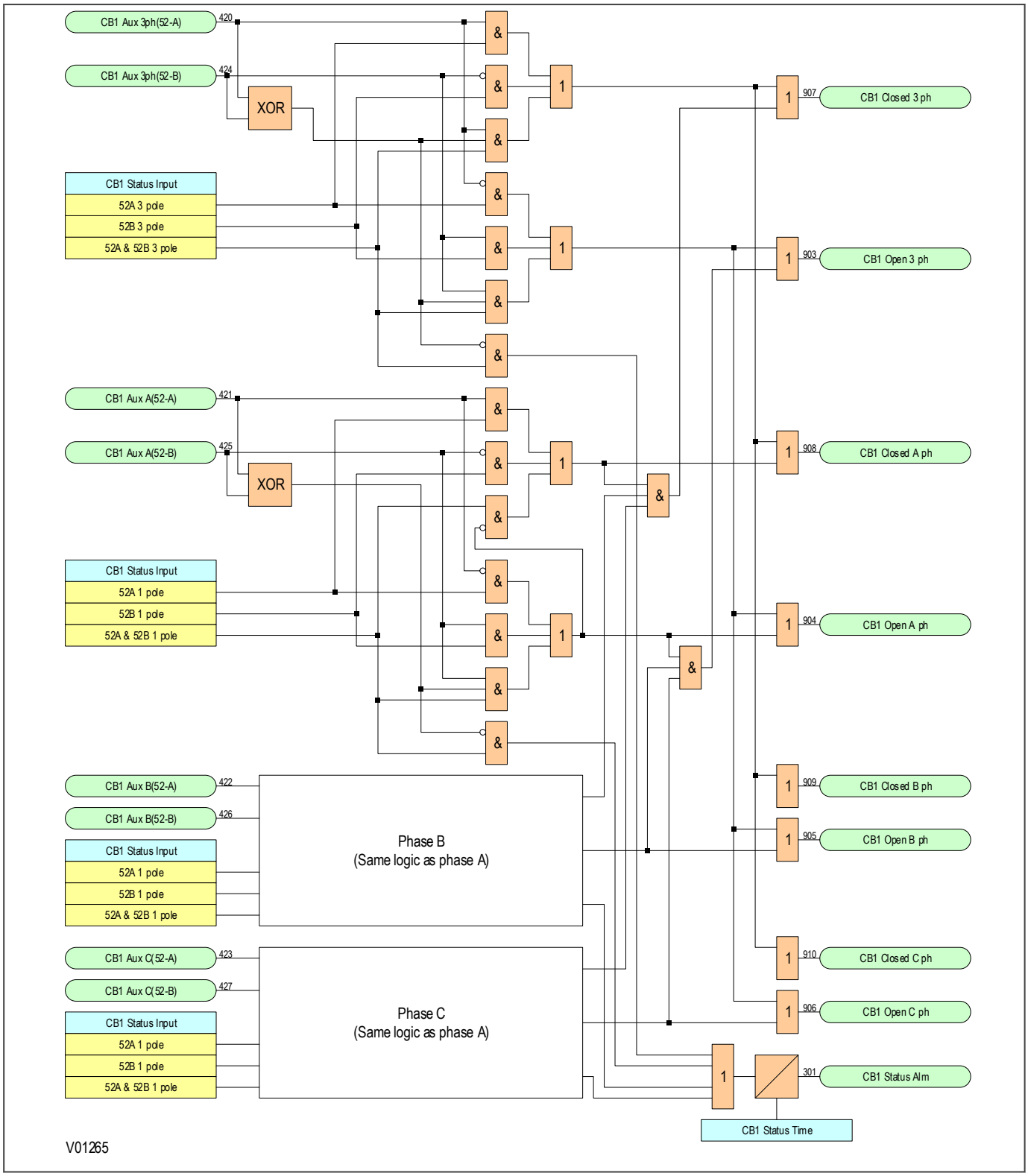


Figure 244: CB state logic (module 1)

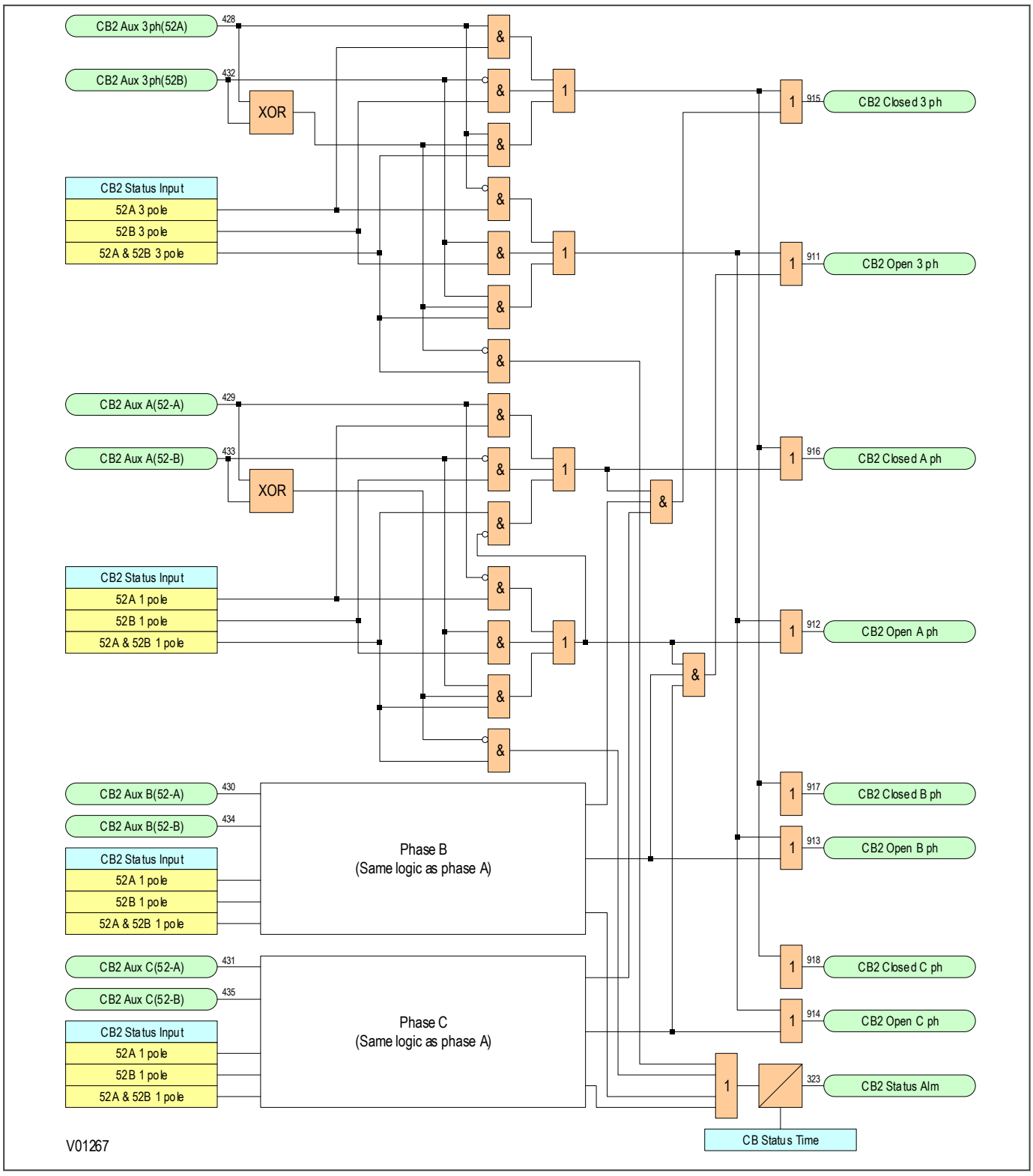


Figure 245: CB state logic (module 2)

12.5.2 CIRCUIT BREAKER OPEN LOGIC

The Circuit Breaker Open logic module produces internal signals indicating the open status of one or more phases. These signals are used by some of the Autoreclose logic modules.

12.5.2.1 CIRCUIT BREAKER OPEN LOGIC DIAGRAM

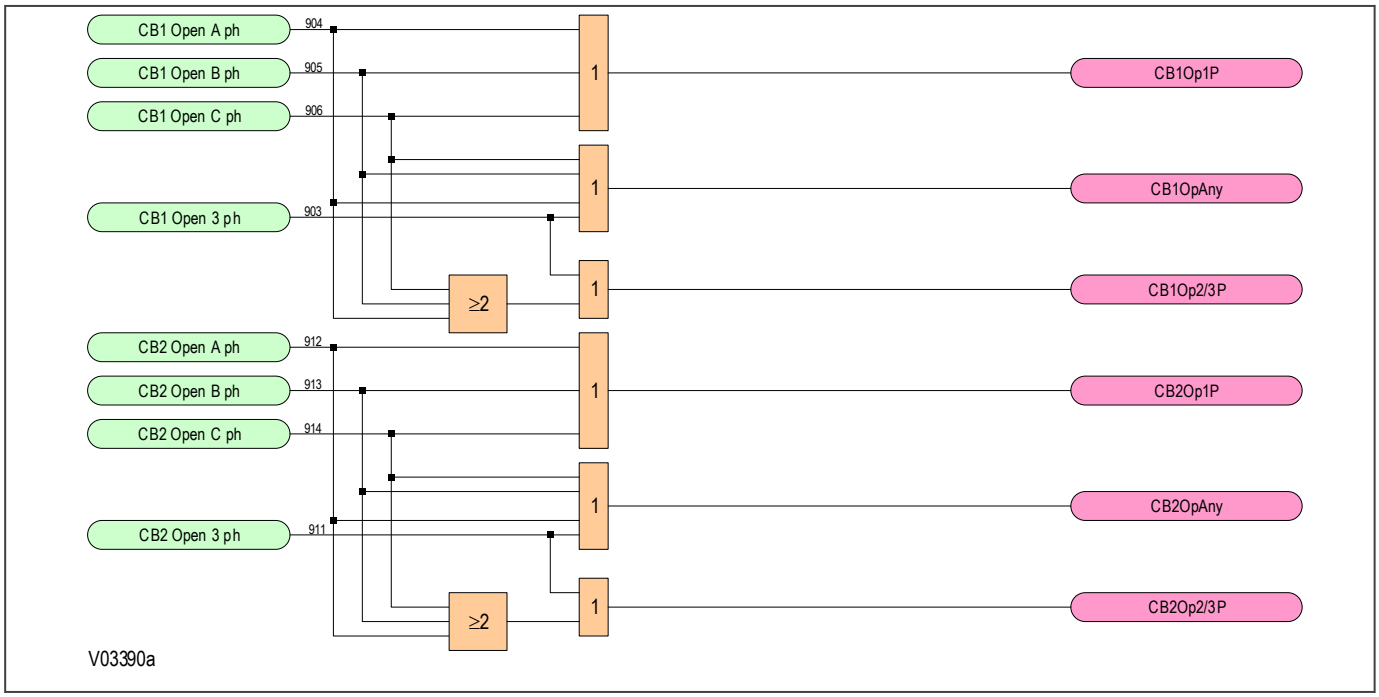


Figure 246: Circuit breaker open logic (module 3)

12.5.3 CIRCUIT BREAKER IN SERVICE LOGIC

For Autoreclose to proceed, a circuit breaker has to be in service when the Autoreclose is initiated. A circuit breaker is considered to be in service if it has been closed for more than the CB IS Time setting.

For applications with fast-acting circuit breaker auxiliary switches, a time delay setting CB IS Memory Time is provided. This is used to ensure correct operation if a delay between the circuit breaker tripping and recognition by the protection, is expected.

When an Autoreclose cycle starts, the “in service” signal for a circuit breaker stays set until the Autoreclose cycle finishes.

The circuit breaker “in service” signal resets if the circuit breaker opens, or if the corresponding Autoreclose in progress (ARIP) signal resets.

12.5.3.1 CIRCUIT BREAKER IN SERVICE LOGIC DIAGRAM

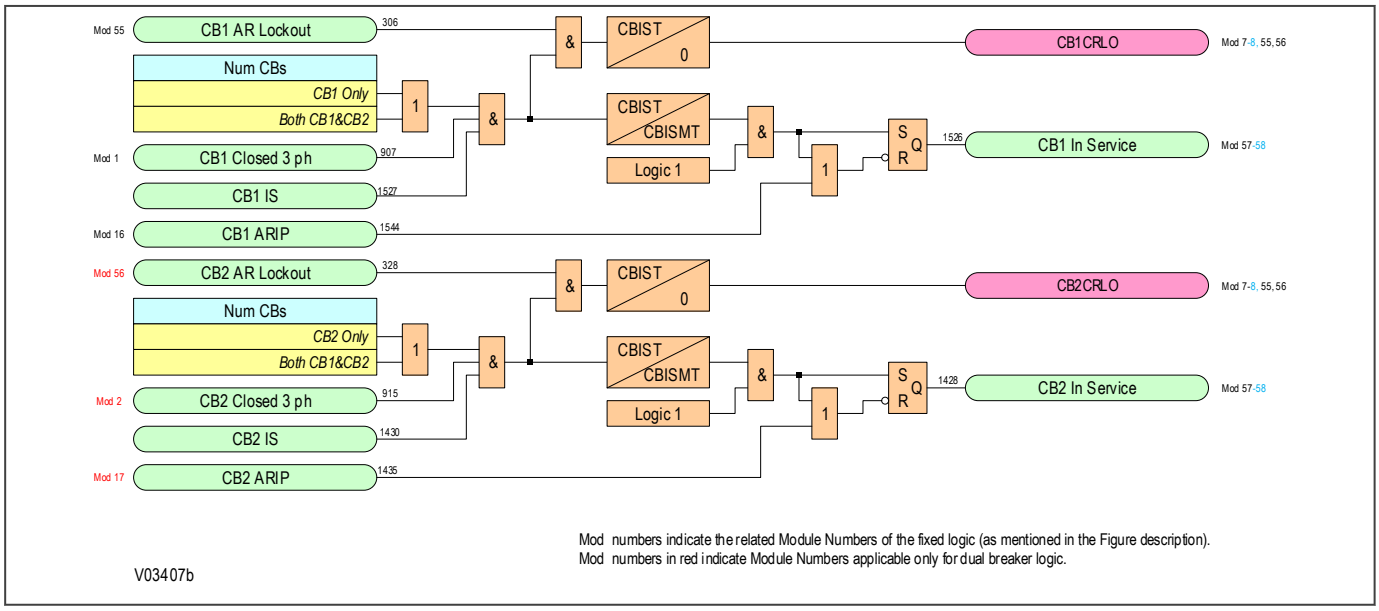


Figure 247: CB in service logic (module 4)

12.5.4 AUTORECLOSE ENABLE LOGIC

The Autoreclose function must be enabled in the *CONFIGURATION* column before it can be brought into service. It can be brought into service by:

- using an opto-input mapped to the ***AR Enable*** DDB signal
- pulsing the DDB signal ***AR On Pulse*** (use ***AR Off Pulse*** to bring it out of service)
- programming a function key on the HMI.
- if applicable, using IEC 60870-5-103 communications

Further validation signals are also required to switch on Autoreclose. These are the DDB signals ***AR Enable CB1*** and ***AR Enable CB2***. Once Autoreclose is in service, the ***AR In Service*** DDB signal is asserted and the ***AR Status*** cell in the *CB CONTROL* column is set accordingly.

12.5.4.1 AUTORECLOSE ENABLE LOGIC DIAGRAM

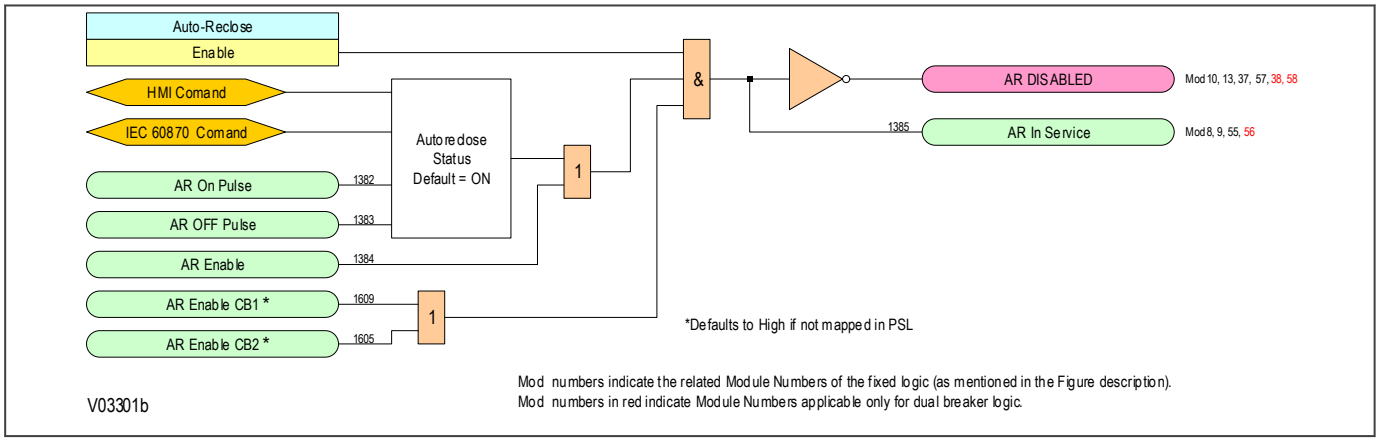


Figure 248: Autoreclose enable logic diagram (module 5)

12.5.5 AUTORECLOSE LEADER/FOLLOWER

You can select either CB1 or CB2 to be the leader, with CB2 or CB1 as the follower respectively.

12.5.5.1 LEADER/FOLLOWER CB SELECTION LOGIC DIAGRAM

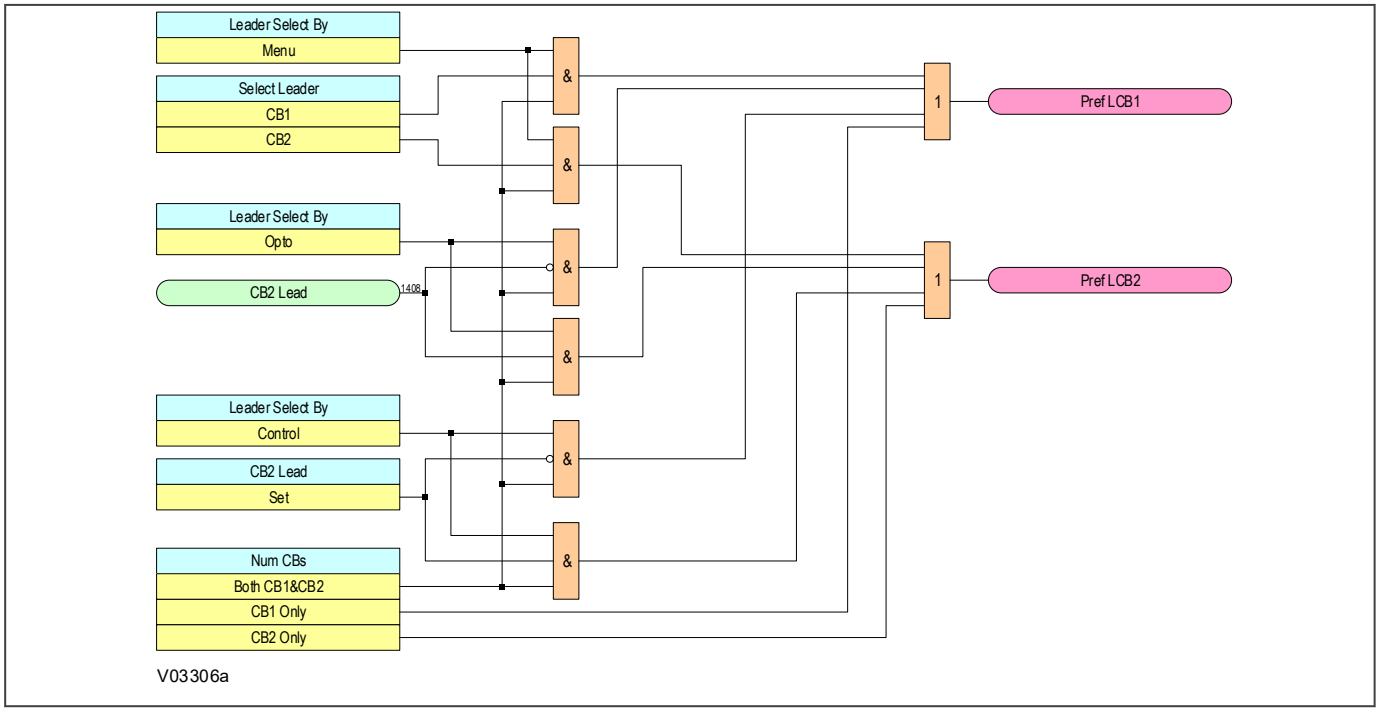


Figure 249: Leader/follower CB selection logic (module 6)

12.5.5.2 LEADER FOLLOWER LOGIC DIAGRAM

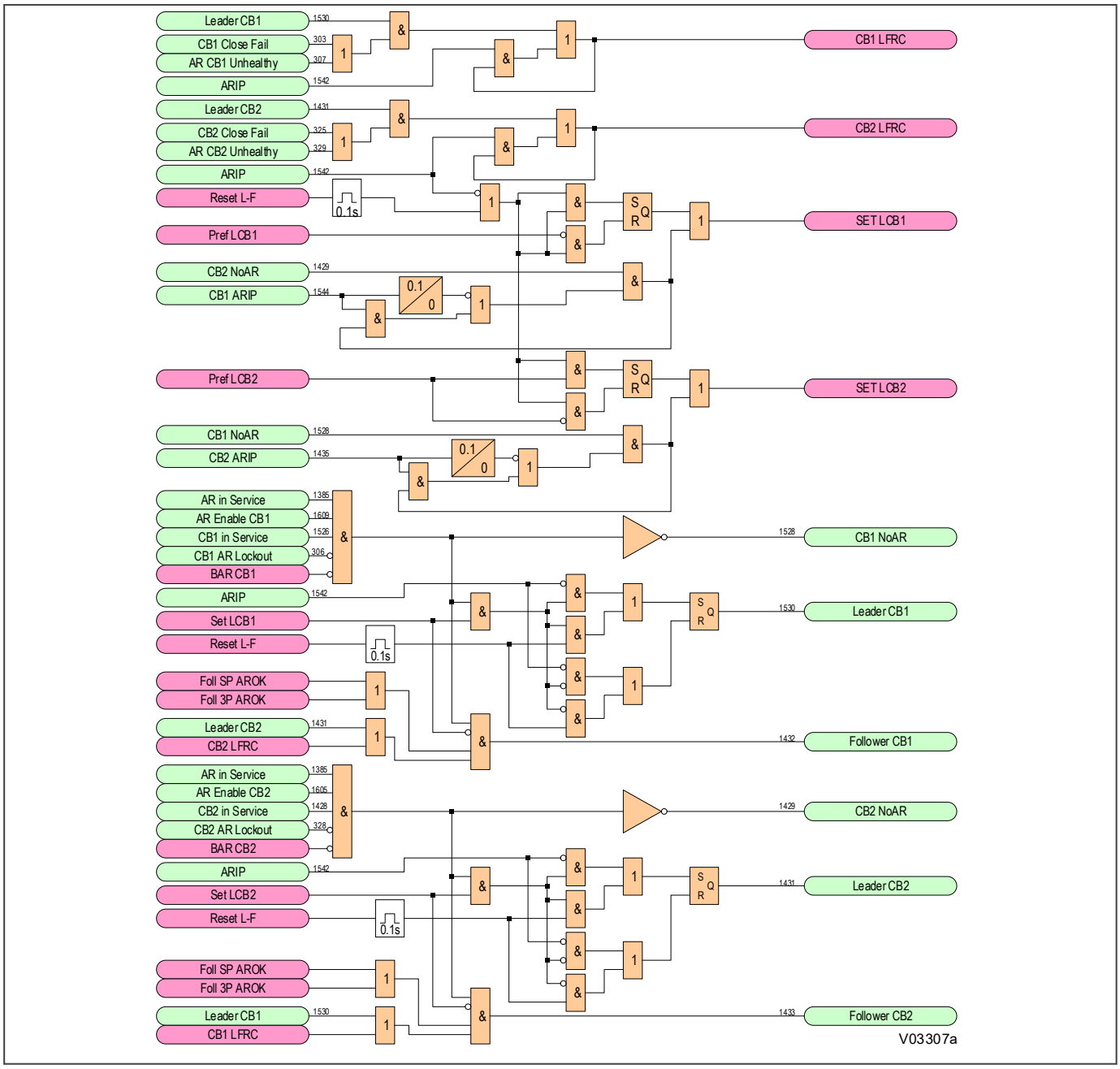


Figure 250: Leader/follower logic (module 7 & 8)

12.5.6 AUTORECLOSE MODES

The device can provide Single-phase and/or Three-phase Autoreclose. The Autoreclose mode is configured by the ***AR Mode*** setting in the *AUTORECLOSE* column. You can choose from:

- Single-phase (`AR 1P`)
- Three-phase (`AR 3P`)
- Single-phase and Three-phase (`AR 1/3P`)
- Controlled by commands from DDB signals that must be mapped to opto-isolated inputs in the PSL (`AR Opto`).

Single-phase Autoreclosing is permitted only for the first shot of an Autoreclose cycle. In a multi-shot Autoreclose cycle the second and subsequent trips will always be three-phase.

For multi-phase faults, you can use the ***Multi Phase AR*** setting in the *AUTORECLOSE* column to configure the following options:

- Allow Autoreclose for all fault types (`Allow Autoclose`)
- Block Autoreclose for 2-phase and 3-phase faults (`BAR 2 and 3 ph`)
- Block Autoreclose for 3-phase faults (`BAR 3 Phase`)

12.5.6.1 SINGLE-PHASE AND THREE-PHASE AUTORECLOSE

This section applies to dual-CB devices. Where there are signals and settings for each of the two circuit breakers, only the first CB (CB1) is shown, to improve clarity and save repetition. Where settings and signals include "CB1", there is a "CB2" equivalent.

Single-phase autoreclose only

If single-phase Autoreclose is enabled, the logic allows only a single shot Autoreclose. For a single-phase fault, the single phase dead timer ***SP AR Dead Time*** starts, and the DDB signal ***CB1 AR 1p Inprog*** is asserted, which indicates that single-phase Autoreclose is in progress. In this case, for a multi-phase fault the logic triggers a three-phase trip and goes to lockout.

Three-phase autoreclose only

During three-phase Autoreclose, for any fault, the three-phase dead timers: ***3P AR DT Shot 1***, ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** are started and the DDB signal is ***CB1 AR 3p InProg*** is asserted, which indicates that three-phase Autoreclose is in progress.

If three-phase only Autoreclose is enabled, the logic forces a three-phase trip by setting the DDB signal ***AR Force CB1 3P*** for any single-phase fault.

Single-phase and three-phase autoreclose

With single-phase and three-phase Autoreclose enabled then, if the first fault is a single-phase fault the single-phase dead time ***SP AR Dead Time*** is started and the single-phase Autoreclose in progress signal is asserted. If the first fault is a multi-phase fault the three phase dead timer ***3P AR DT Shot 1*** is started and the three-phase Autoreclose in progress signal is asserted. If set to allow more than one reclose (***AR Shots*** > 1) then any subsequent faults are converted to three-phase trips by setting the force three-pole tripping signal. The three-phase dead times ***3P AR DT Shot 2***, ***3P AR DT Shot 3*** and ***3P AR DT Shot 4*** (Dead Times 2, 3, 4) are started for the 2nd, 3rd and 4th trips (shots) respectively. The DDB signal ***CB1 AR 3p InProg*** is asserted. If a single-phase fault evolves to a multi-phase fault during the single-phase dead time (***SP AR Dead Time***), single-phase Autoreclose is stopped. The single-phase Autoreclose in progress signal is reset, the three-phase Autoreclose in progress signal is set, and the three-phase dead timer ***3P AR DT Shot 1*** is started.

12.5.6.2 AUTORECLOSE MODES ENABLE LOGIC DIAGRAM

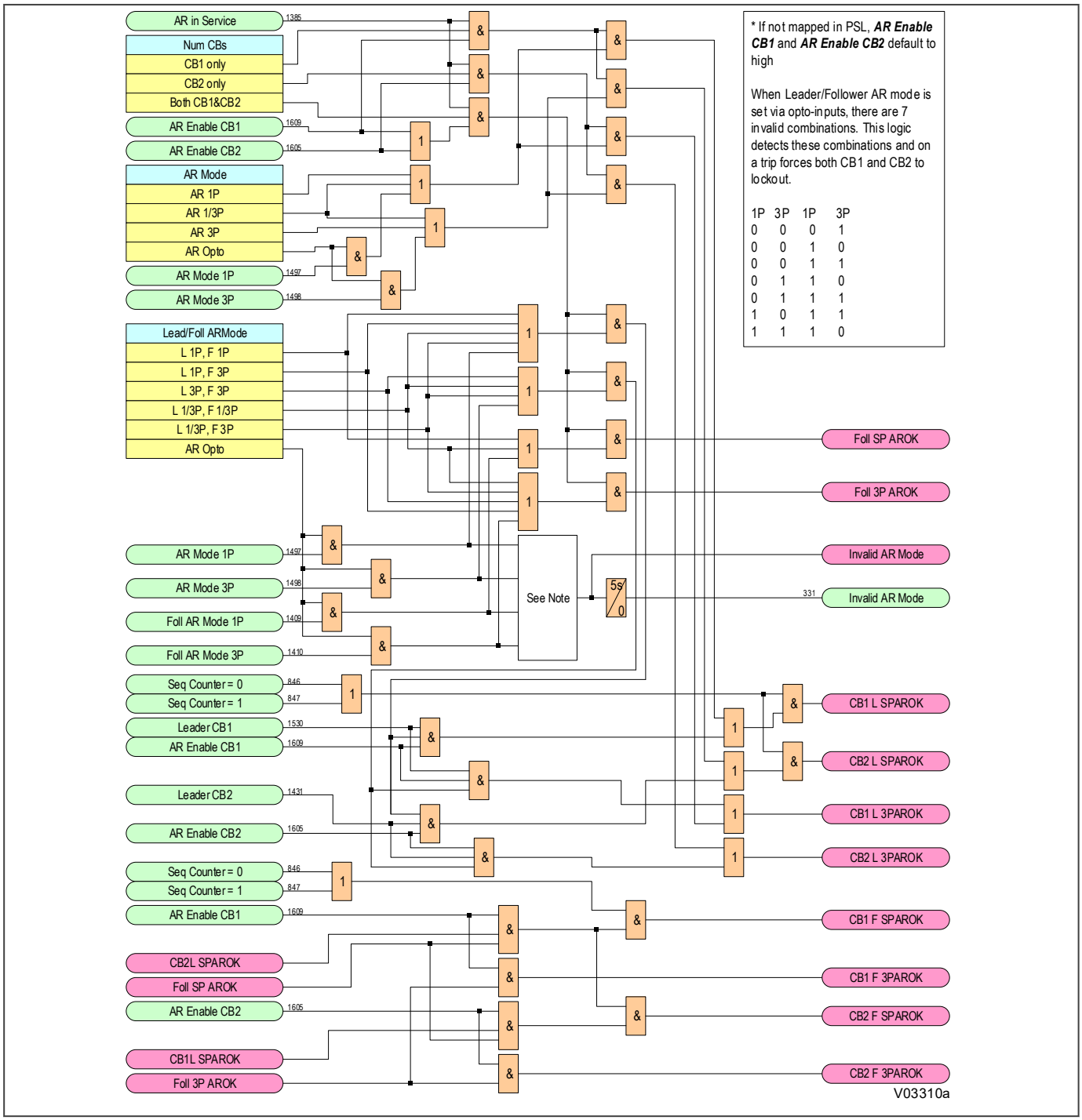


Figure 251: Autoreclose modes enable logic (module 9)

12.5.7 AR FORCE THREE-PHASE TRIP LOGIC

Following single-phase tripping, while the Autoreclose cycle is in progress, and upon resetting of the protection elements, tripping switches to three-phase.

Any protection operations that occur for subsequent faults while the Autoreclose cycle remains in progress will be tripped three-phase.

12.5.7.1 FORCE THREE-PHASE TRIP LOGIC DIAGRAM

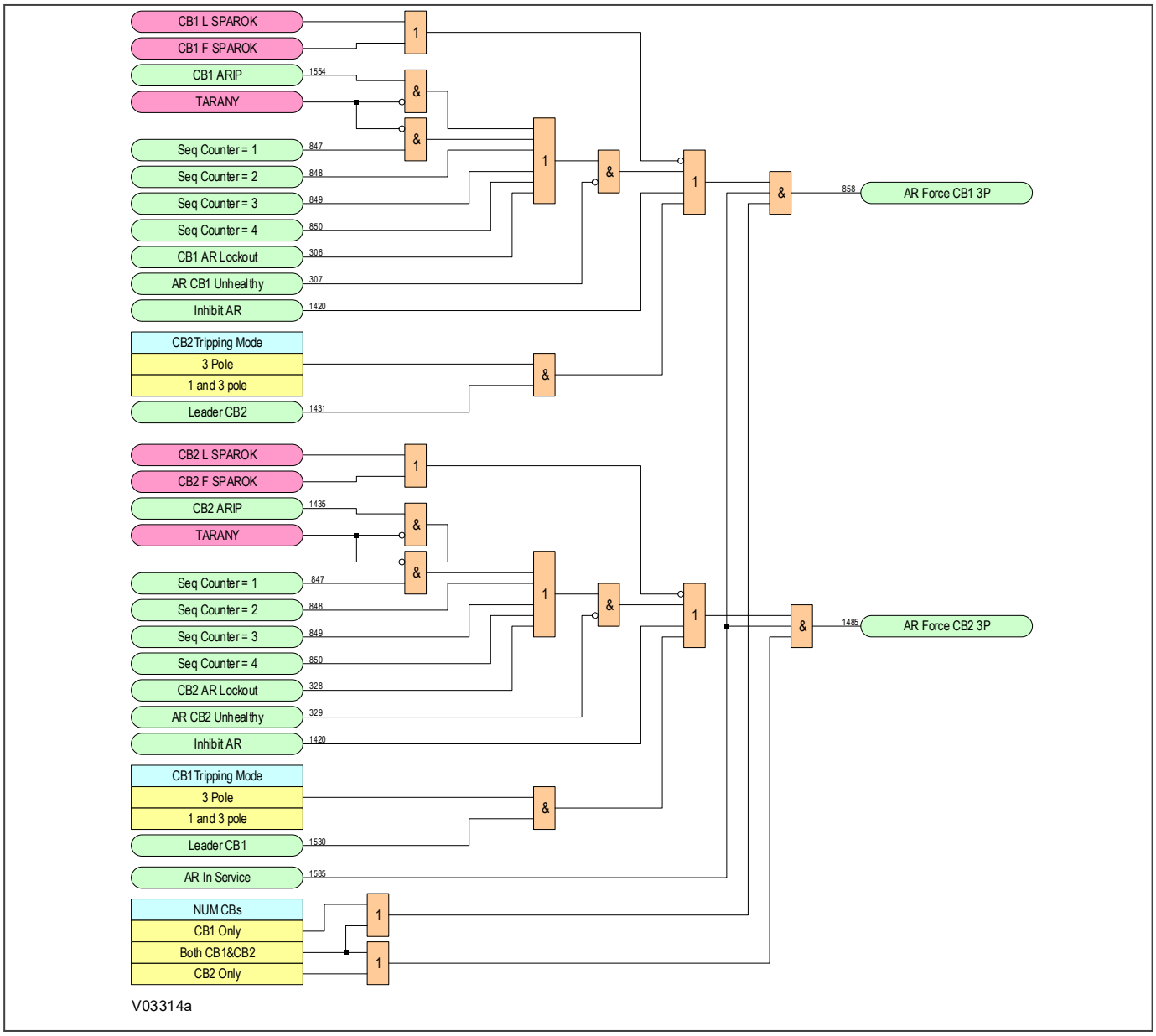


Figure 252: Force three-phase trip logic (module 10)

12.5.8 AUTORECLOSE INITIATION LOGIC

Autoreclose initiation starts Autoreclose for a circuit breaker only if Autoreclose is enabled for the circuit breaker, and the circuit breaker is in service. When an Autoreclose cycle is started, Autoreclose in progress (ARIP) is indicated. The indication remains until the end of the cycle. The end of the cycle is signified by successful Autoreclose, or by lockout.

Autoreclose cycles can be initiated by:

- Protection functions internal to the product
- A Trip Test feature
- External protection equipment
- Evolving fault combinations

Internal protection functions

Many of the protection functions in the product can be programmed to initiate or block Autoreclose. The associated settings are found in the Autoreclose column and the available options are *No Action*, *Initiate AR*, or *Block AR*. If set to *Block AR* operation of the protection function blocks the Autoreclose function and forces a lockout.

Trip test feature

The ***Test Autoreclose*** command cell in the *COMMISSION TESTS* column can be used to initiate an Autoreclose cycle. Each option provides a 100 ms pulse output. There is also a 'No Operation' option to exit the command field without initiating a test.

External protection equipment

Protection operation from a different device can be used to initiate Autoreclose via PSL. By default these external trip input signals are mapped to initiate Autoreclose. These inputs are not mapped to the trip outputs. With appropriate mapping in the PSL, however, the external device can use this product to trip connected circuit breakers.

Evolving fault combinations

The Autoreclose function would normally be initiated by a single condition (such as a single-phase fault). If, however, the system conditions evolve such that other conditions that could initiate Autoreclose, then the dynamics of the Autoreclose logic need to adapt. For example, if a single-phase fault evolves into a multi-phase fault, then the operation of the Autorecloser must consequently adapt. To achieve this signals are generated to indicate conditions such as evolving faults, re-operation of protection, combinations of initiation by internal protection, external protection, or test features, which control the Autoreclose sequencing.

Records of initiating conditions are stored and used to control the sequencing. Initiation can be from a protection function integrated in the product, from external protection and internal sources such as the Autoreclose test function. Initiation can be further qualified by the phases causing the initiation. These conditions are stored in signals that generally feature "MEM"- memory, or "AR" – Autoreclose, in the signal name.

12.5.8.1 AUTORECLOSE INITIATION LOGIC DIAGRAM

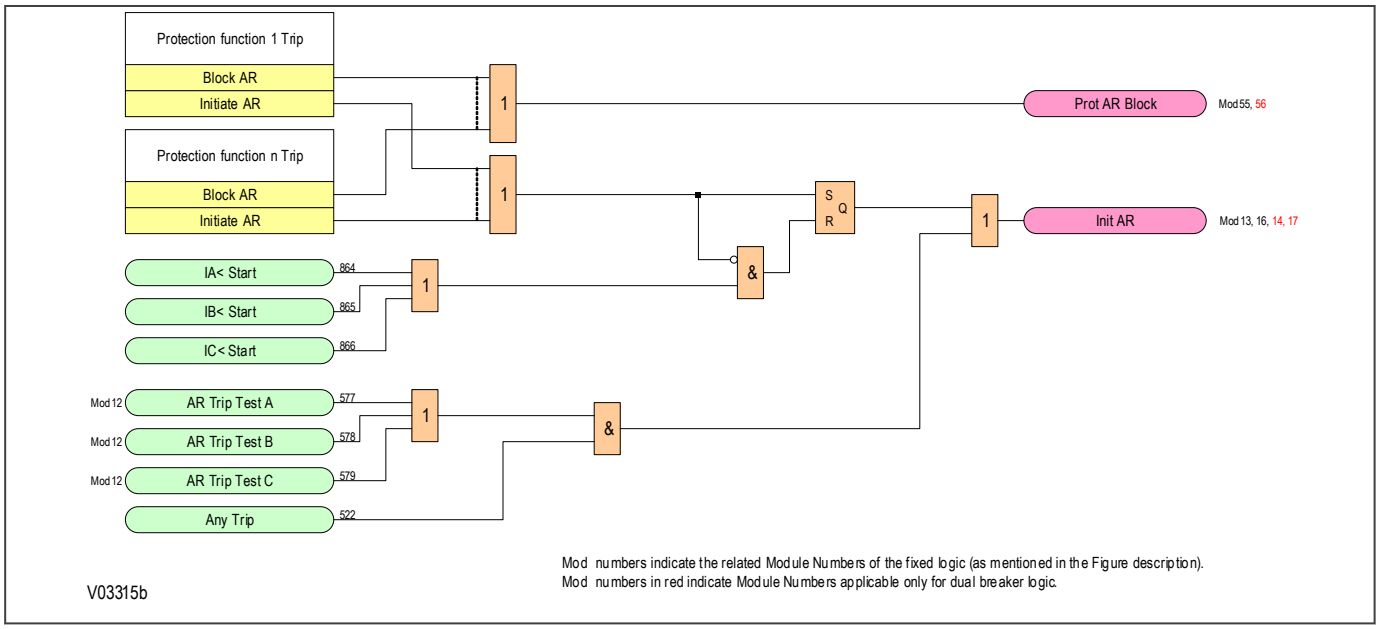


Figure 253: Autoreclose initiation logic (module 11)

12.5.8.2 AUTORECLOSE TRIP TEST LOGIC DIAGRAM

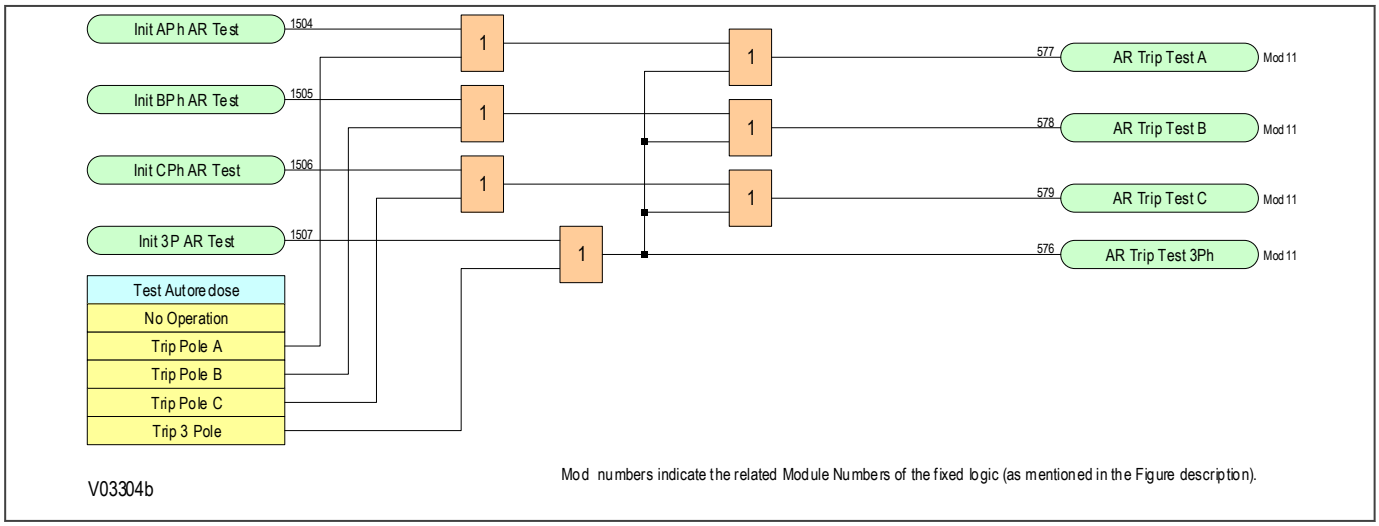


Figure 254: Autoreclose trip test logic (module 12)

12.5.8.3 EXTERNAL TRIP LOGIC DIAGRAM FOR CB1

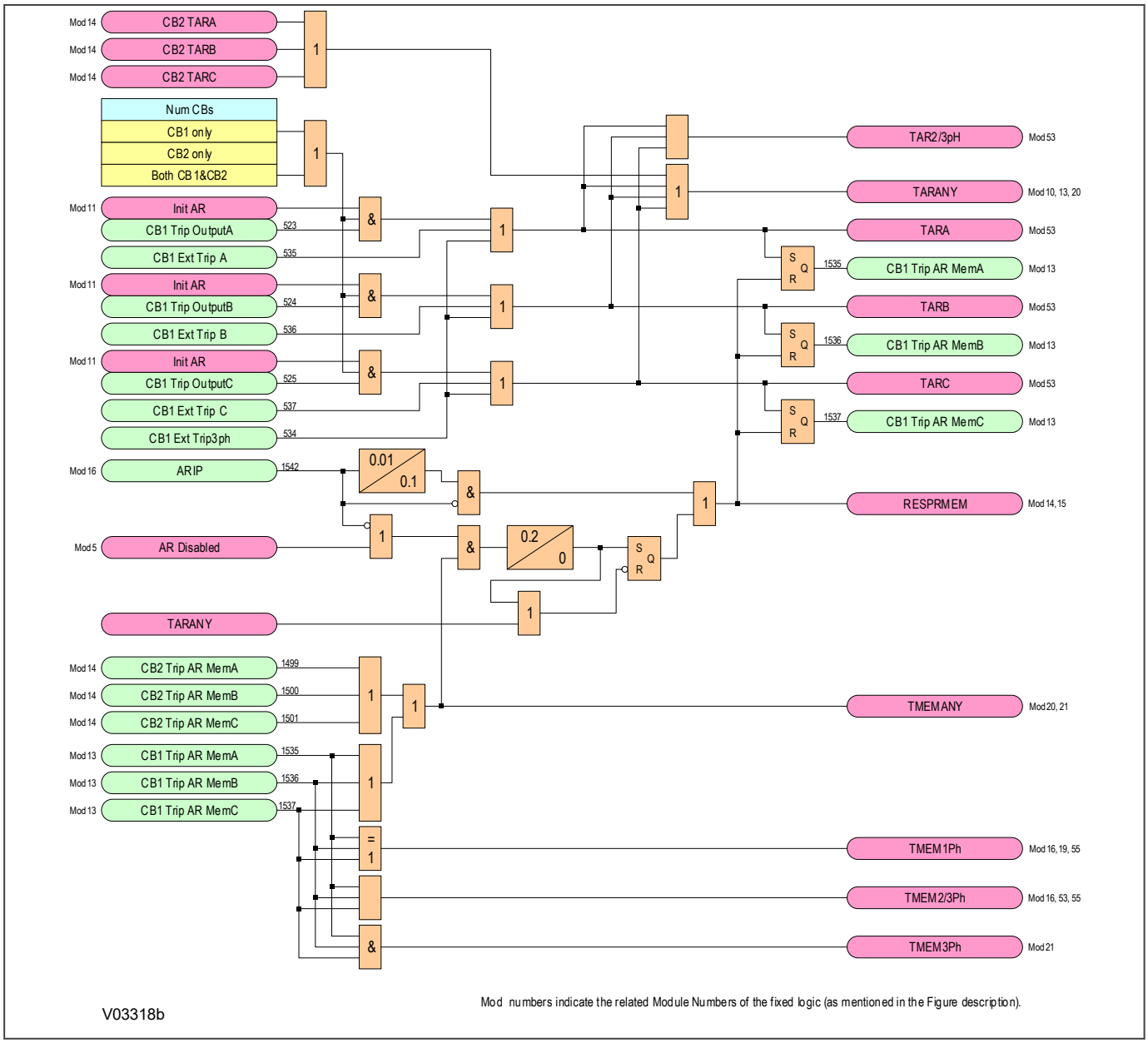


Figure 255: Autoreclose initiation by internal single and three phase trip or external trip for CB1 (module 13)

Note:
For single-phase Autoreclose, these signals must be mapped as shown in the default PSL scheme.

12.5.8.4 EXTERNAL TRIP LOGIC DIAGRAM FOR CB2

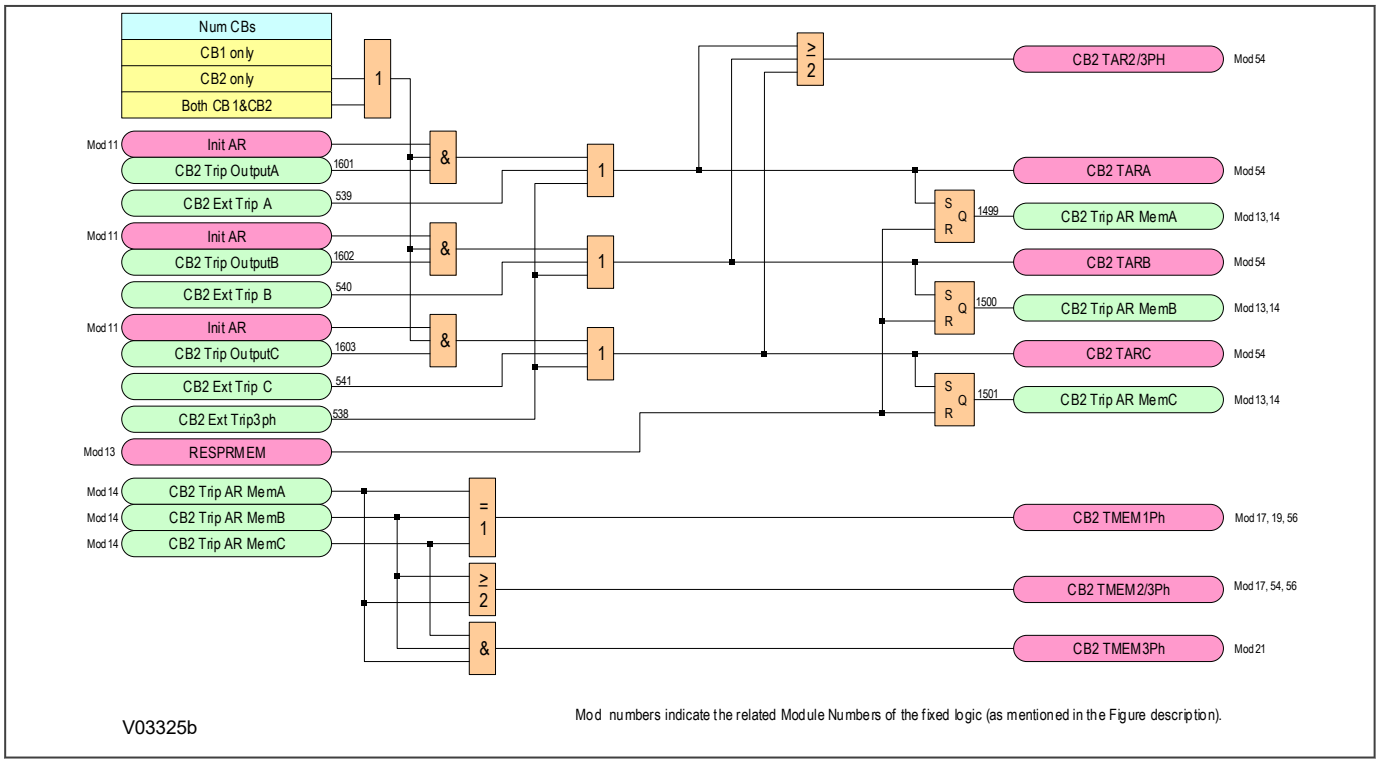


Figure 256: Autoreclose initiation by internal single and three phase trip or external trip for CB2 (module 14)

Note:
For single-phase Autoreclose, these signals must be mapped as shown in the default PSL scheme.

12.5.8.5 PROTECTION REOPERATION AND EVOLVING FAULT LOGIC DIAGRAM

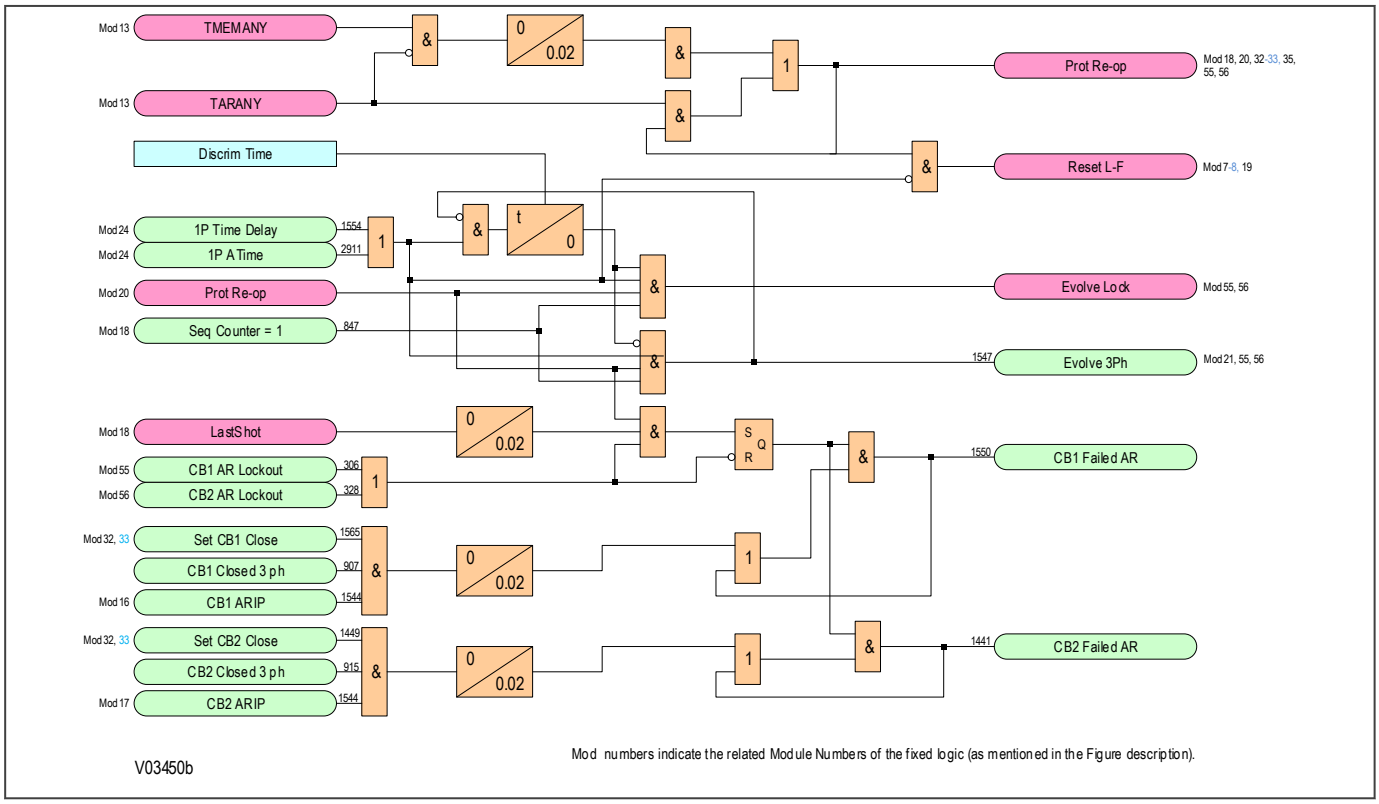


Figure 257: Protection reoperation and evolving fault logic (module 20)

12.5.8.6 FAULT MEMORY LOGIC DIAGRAM

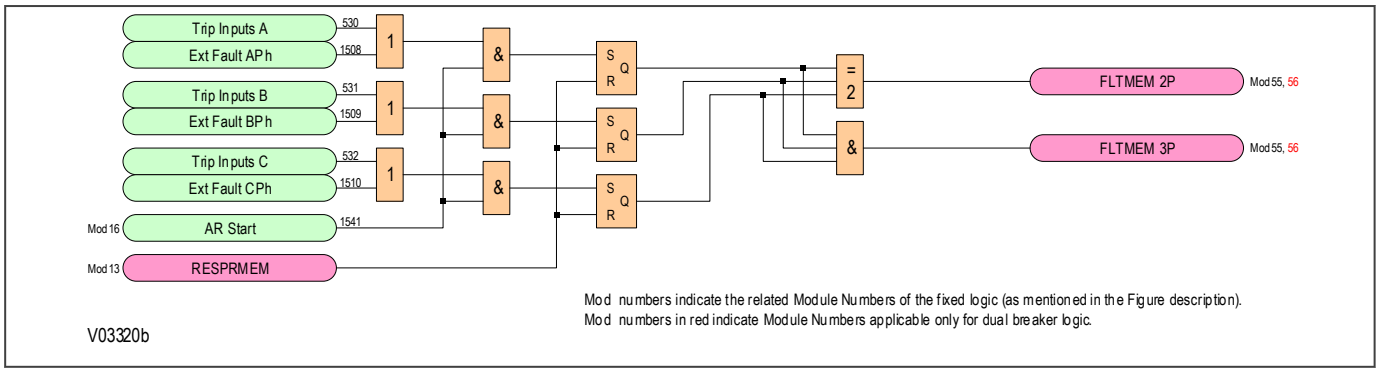


Figure 258: Fault memory logic (module 15)

12.5.9 AUTORECLOSE IN PROGRESS

The AR In Progress module produces various signals to indicate to other modules and functions that an Autoreclose operation is currently in progress.

12.5.9.1 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM FOR CB1

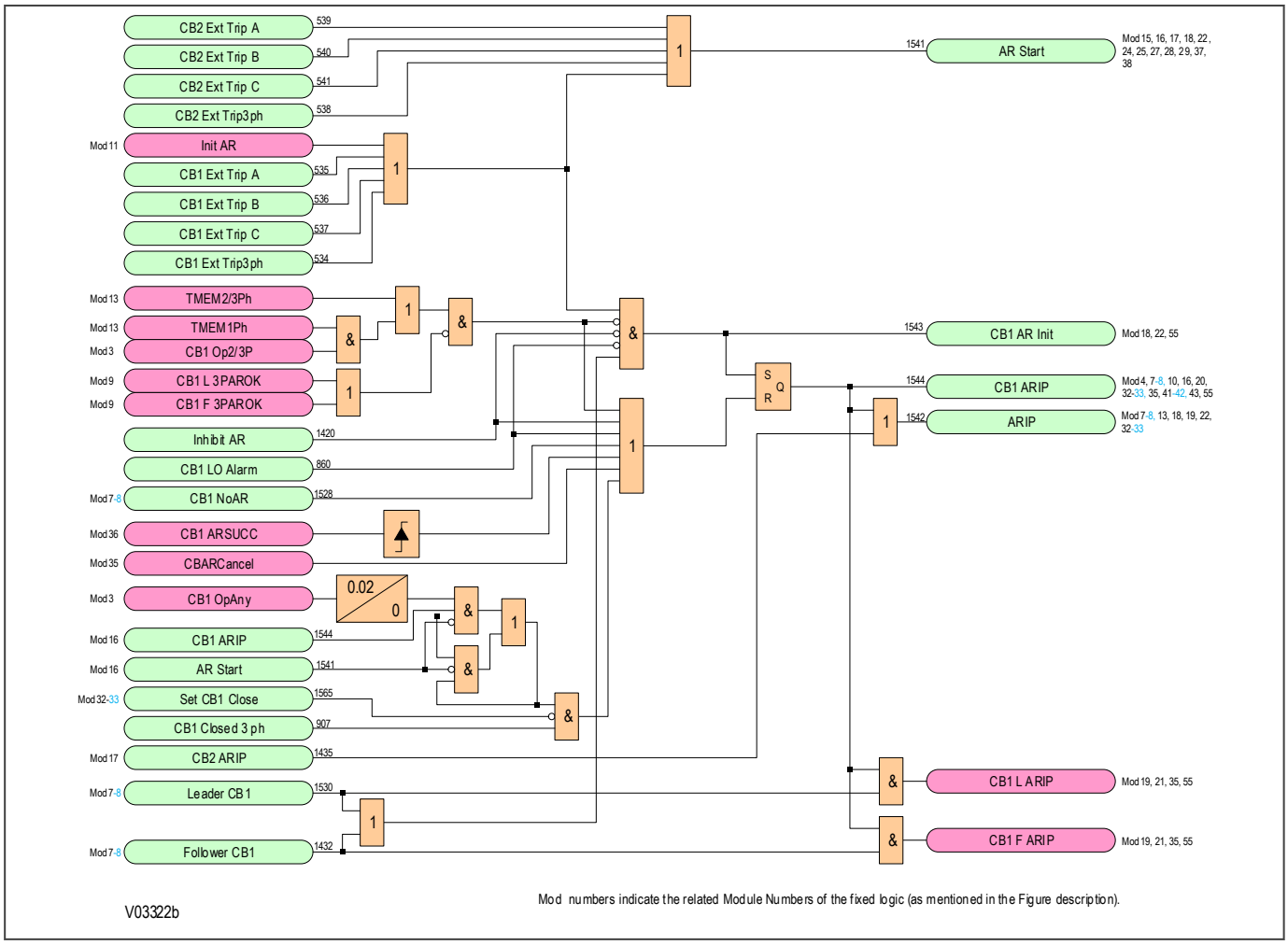


Figure 259: Autoreclose in progress logic for CB1 (module 16)

12.5.9.2 AUTORECLOSE IN PROGRESS LOGIC DIAGRAM FOR CB2

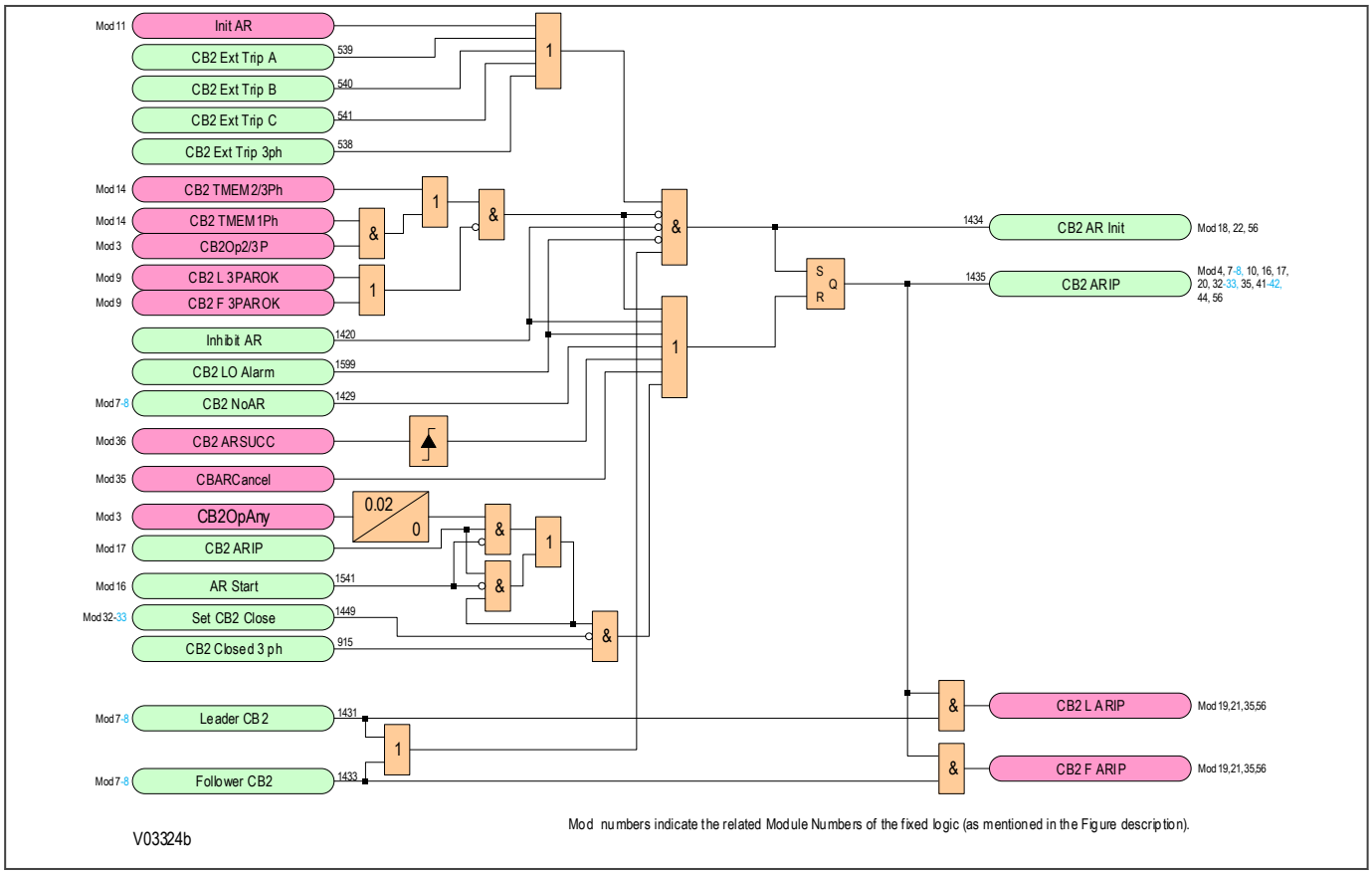


Figure 260: Autoreclose in progress logic for CB2 (module 17)

12.5.10 SEQUENCE COUNTER

The Autoreclose logic includes a counter for counting the number of Autoreclose shots. This is referred to as the sequence counter. The sequence counter has a value of zero if Autoreclose is not in progress. Following a trip, and subsequent Autoreclose initiation, the sequence counter is incremented. The counter provides output signals indicating how many initiation events have occurred in any Autoreclose cycle. These signals are available as user indications and are used in the logic to select the appropriate dead times or, for a persistent fault, force a lockout.

It is possible to skip the first Autoreclose attempt by enabling the ***AR Skip Shot 1*** setting. If this is set, the sequence counter will skip the first Autoreclose attempt (Shot 1) and move to the second (Shot 2) immediately upon Autoreclose initiation. Each time the protection trips the sequence counter is incremented by 1. The Autoreclose logic compares the sequence counter value to the number of Autoreclose shots setting ***AR Shots***. If the counter value exceeds this setting then the Autoreclose is locked out. If Autoreclose is successful, the sequence counter resets to zero.

12.5.10.1 AUTORECLOSE SEQUENCE COUNTER LOGIC DIAGRAM

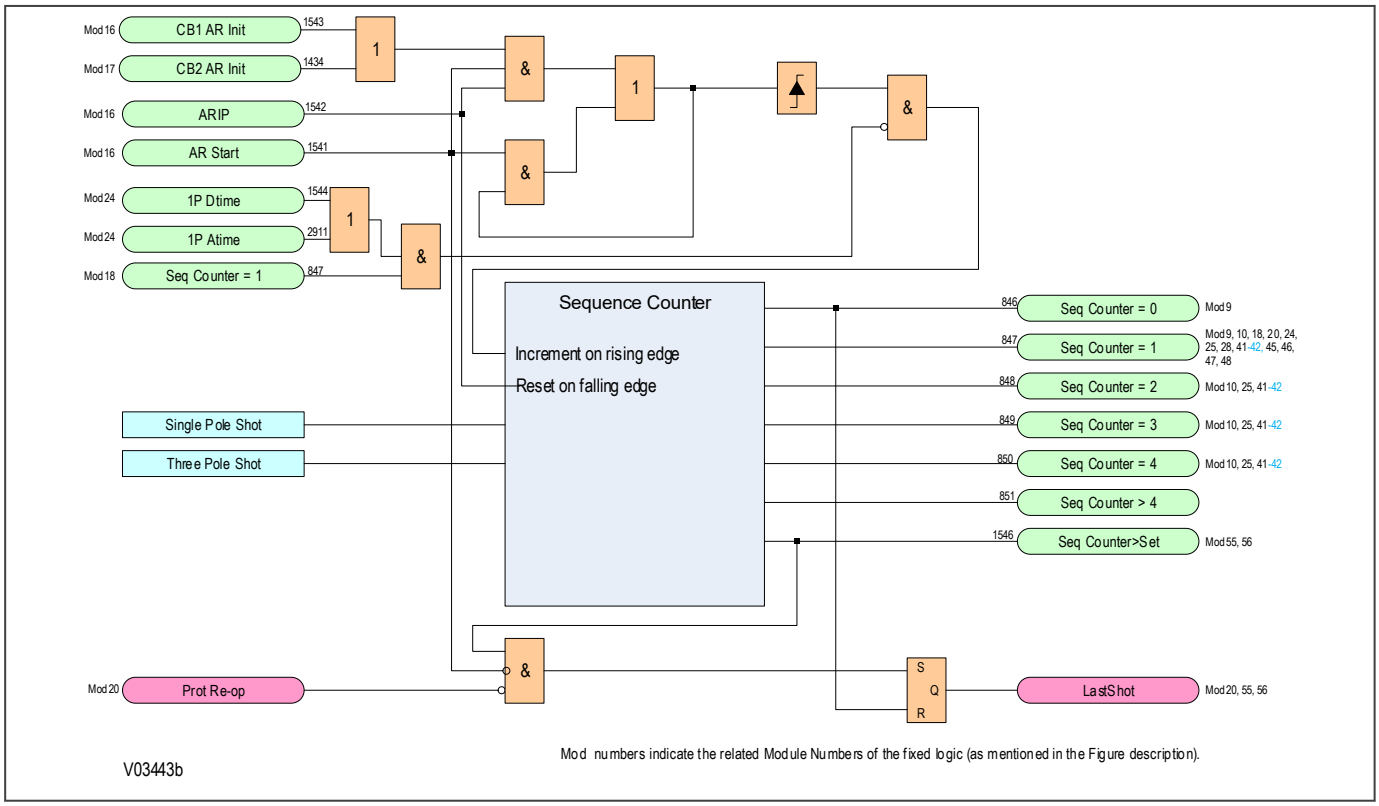


Figure 261: Autoreclose sequence counter logic (module 18)

12.5.11 AUTORECLOSE CYCLE SELECTION

The Autoreclose cycle selection logic is responsible for determining whether the Autoreclose will start as single-phase or three-phase.

12.5.11.1 SINGLE PHASE AUTORECLOSE CYCLE SELECTION LOGIC DIAGRAM

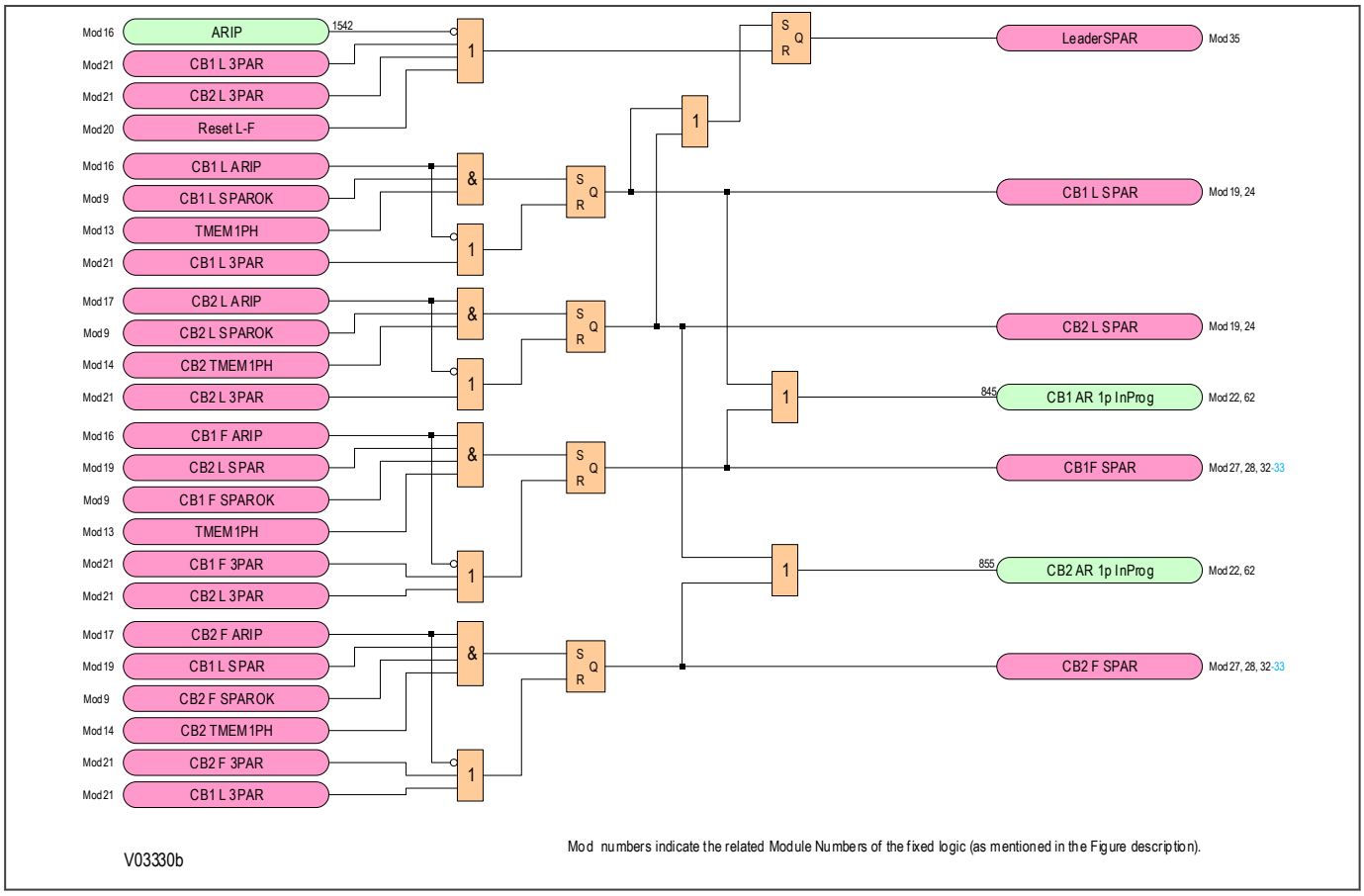


Figure 262: Single-phase autoreclose cycle selection logic (module 19)

12.5.11.2 3-PHASE AUTORECLOSE CYCLE SELECTION

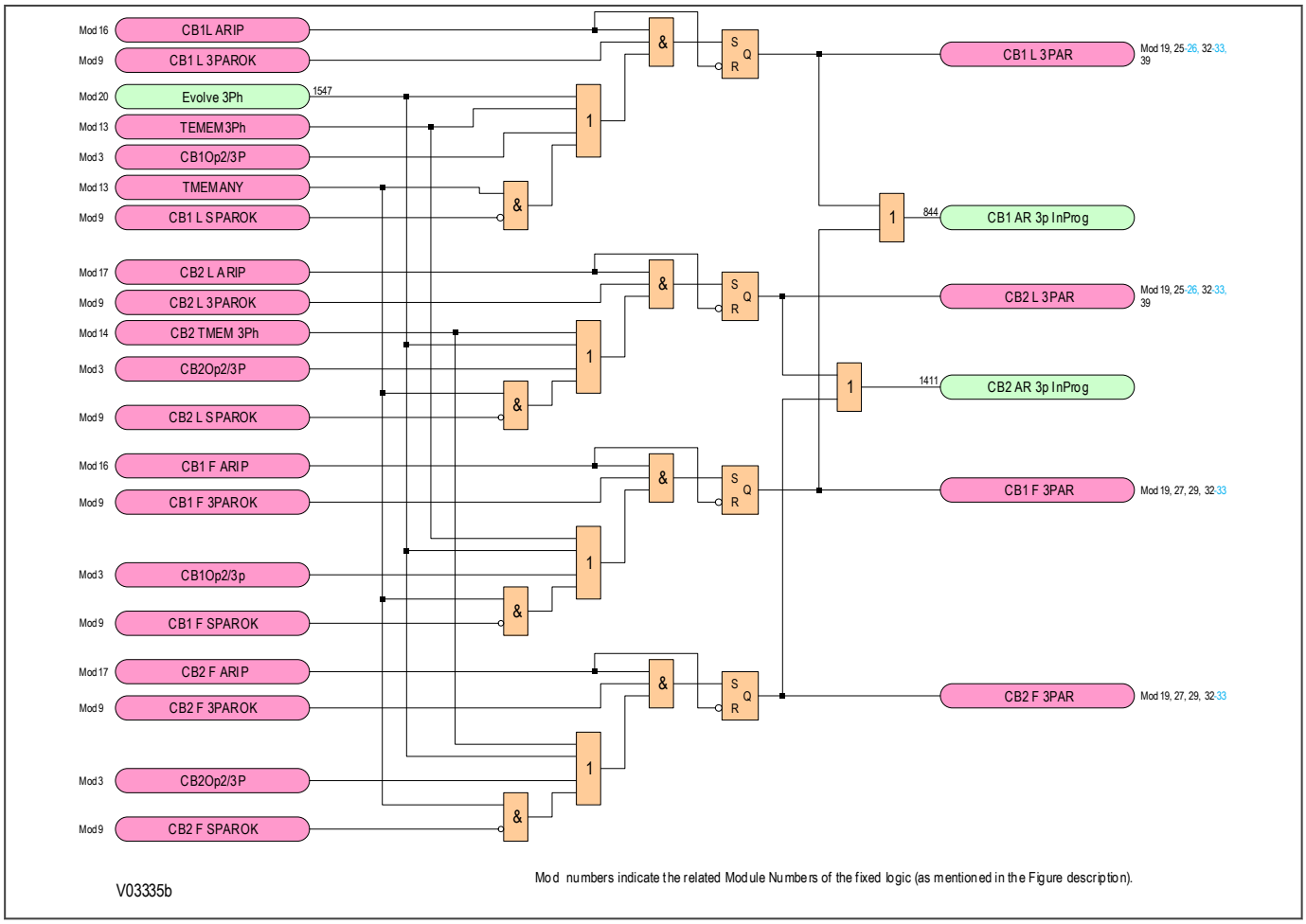


Figure 263: Three-phase autoreclose cycle selection logic (module 21)

12.5.12 DEAD TIME CONTROL

Once an Autoreclose cycle has started, the conditions to enable the dead time to run are determined by the menu settings, the circuit breaker status, the protection status, the nature of the AR cycle (single-phase or three-phase), and the opto-isolated inputs from external sources.

Three settings are involved in controlling the dead time start:

- ***DT Start by Prot***
- ***3PDTStart WhenLD***
- ***DTStart by CB Op***

The ***DT Start by Prot*** determines how the protection action will initiate a dead time. The setting is always visible and has three options `Protection Reset`, `Protection Op` (protection operation), and `Disable` which should be selected if you don't want protection action to start the dead time. These options set the basic conditions for starting the dead time.

Selecting protection operation to start the dead time can, optionally, be qualified by a check that the line is dead.

Selecting protection reset to start the dead time can, optionally, be qualified by a check, that the circuit breaker is open (***DTStart by CB Op***) before starting the dead time. For three-phase tripping applications, there is a further option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time.

If ***DT Start by Prot*** is disabled, the circuit breaker must be open for the dead time to start. For three-phase tripping applications, there is an option to check that the line is dead (***3PDTStart WhenLD***) before starting the dead time. To check that the line is dead, set ***3PDTStart WhenLD*** to `enabled`. To check that the circuit breaker is open, set ***DTStart by CB Op*** to `Enabled`.

12.5.12.1 DEAD TIME START ENABLE LOGIC DIAGRAM

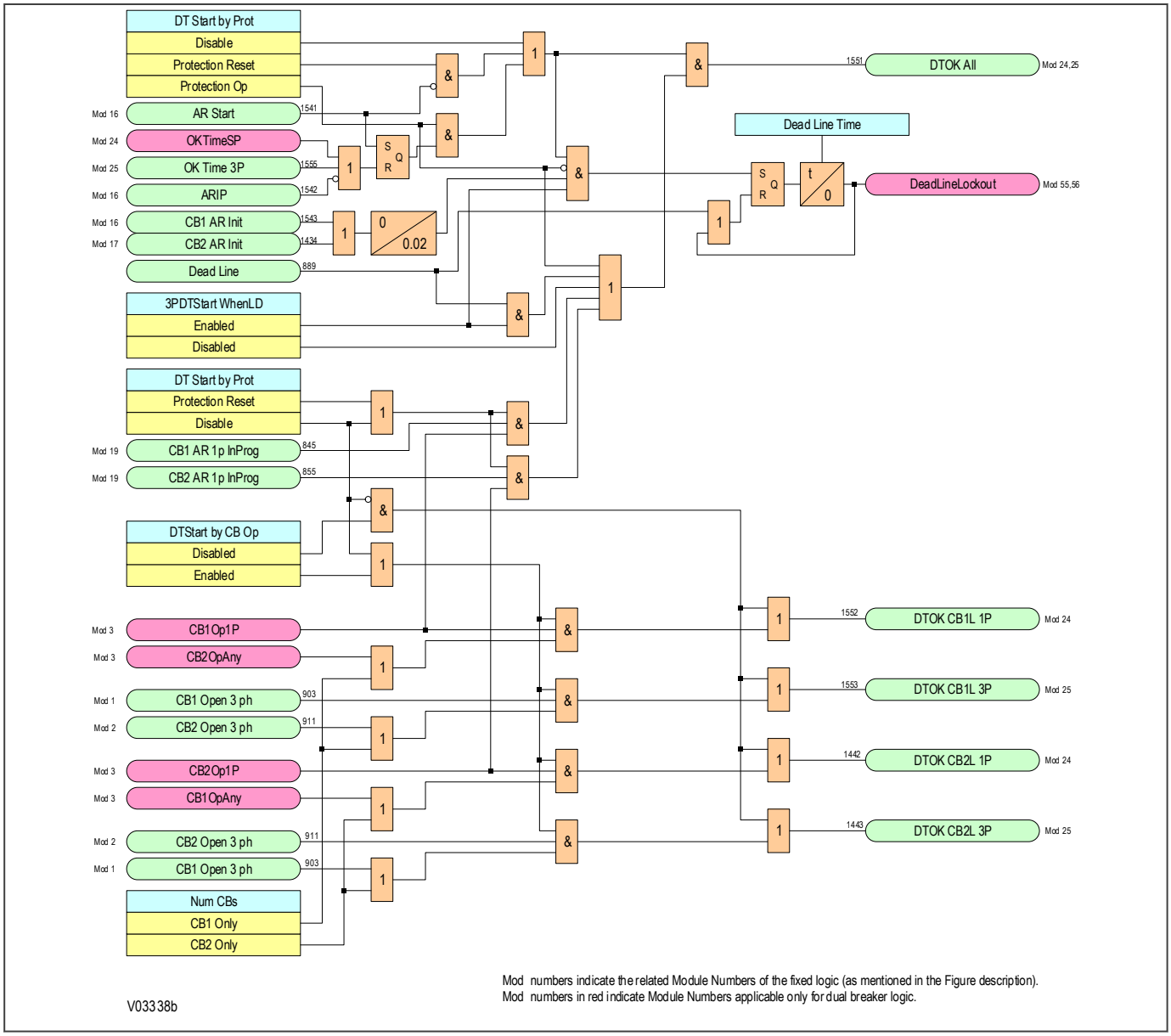


Figure 264: Dead time start enable logic (module 22)

12.5.12.2 SINGLE-PHASE DEAD TIME AND ADAPTIVE AUTORECLOSE (AAR) LOGIC

The autoreclose scheme is adaptive when the ***Adaptive SP AR*** setting is `Enabled`. The adaptive autoreclose is only available for single pole autoreclose applications. When adaptive autoreclose is enable, ***SP AR Dead Time*** is hidden, and two new timer settings are visible: ***SP Min Dead Time*** and ***SP Max Dead Time***. Those two timers are the limits of the single pole dead time.

The Fault Type and Arc Extinction (FTAE) detection algorithm is initiated when the ***Adaptive SP AR*** setting is `Enabled` and the ***OkTimeSP*** signal of the dead time is high, as shown in Module 24.

The breaker open status (***CB Open A PH***/***CB Open B PH*** /***CB Open C PH***) signals are used to identify the single phase to ground fault isolation. The phase voltage information is provided to a six cycle buffer and the δ and |Vs| and derivatives are fed to the ***FTAED*** Module.

The output signals from the ***FTAED*** Module are the ***P_Fault***, ***T_Fault*** and the ***Arc complete*** signals (DDBs: 2909 AAR Perm Flt, 2910 AAR Temp Flt and 2924 AAR Arc Extinct) which indicate a permanent fault detection, transient fault detection and arc extinction.

The ***T_Fault*** signal is high during a transient fault condition and the Arc complete signal is high only after complete de-ionisation of the faulted arc during transient fault conditions. During a permanent fault condition, the ***P_Fault*** output signal of the AAR module is high, and it is routed to the AR lockout logic diagram (Module 55) to stop further autoreclose actions if required.

The ***CB1SPDTCOMP*** and ***CB1SPATCOMP*** signals in Module 24 are inputs to the Circuit Breaker Auto Close Logic Diagram (Module 32). The ***CB1SPDTCOMP*** signal is high in cases where the ***Adaptive SP AR*** is setting is *0* and ***CB1SPATCOMP*** is high in cases where the ***Adaptive SP AR*** setting is *1*.

12.5.12.3 SINGLE-PHASE LEADER DEAD TIME LOGIC DIAGRAM

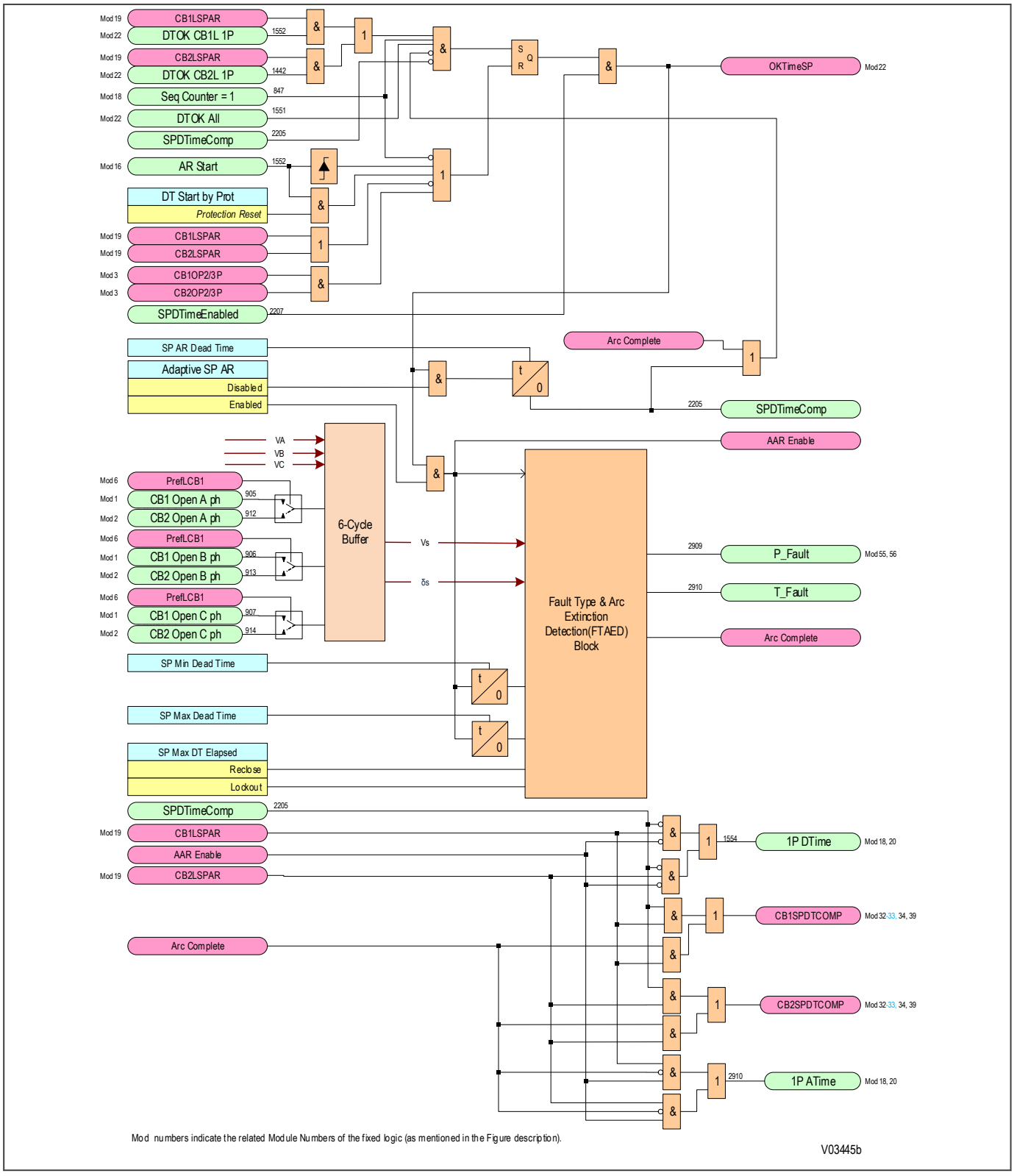


Figure 265: Single-phase leader dead time logic (module 24)

12.5.12.4 3-PHASE LEADER DEAD TIME LOGIC DIAGRAM

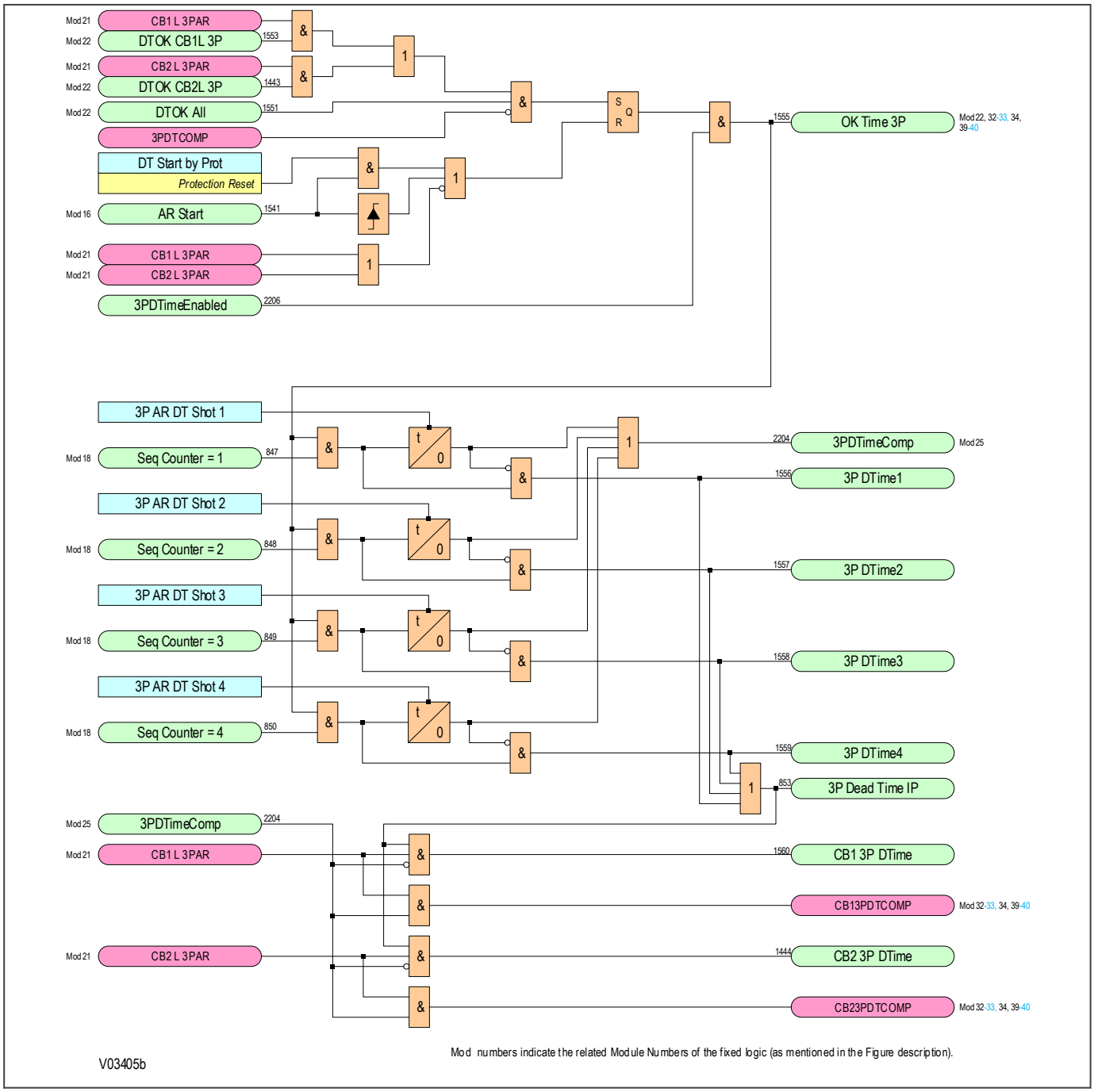


Figure 266: Three-phase leader CB dead time logic (module 25 and module 26)

12.5.12.5 FOLLOWER ENABLE LOGIC DIAGRAM

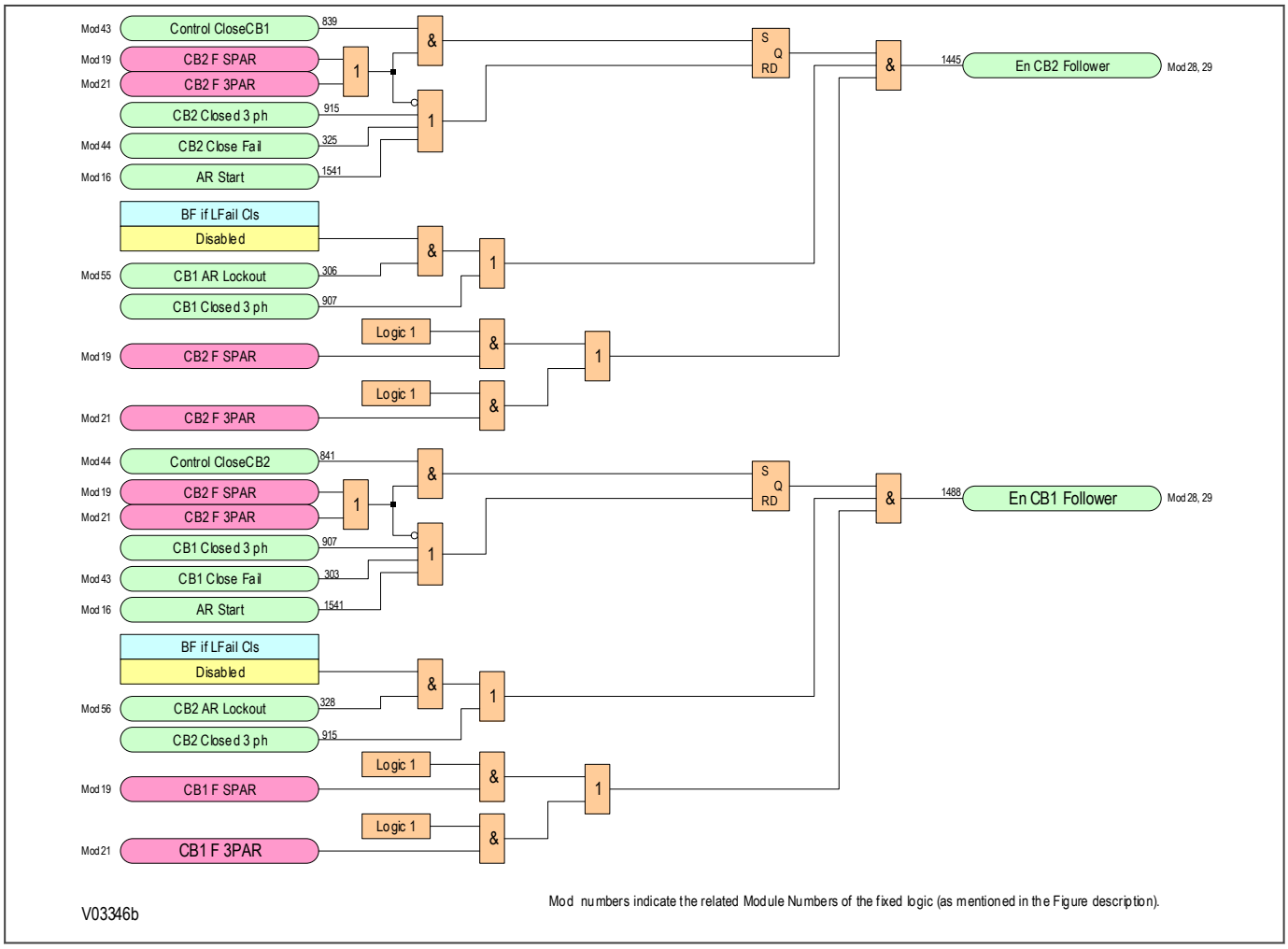


Figure 267: Follower enable logic (module 27)

12.5.12.6 SINGLE-PHASE FOLLOWER TIMING LOGIC DIAGRAM

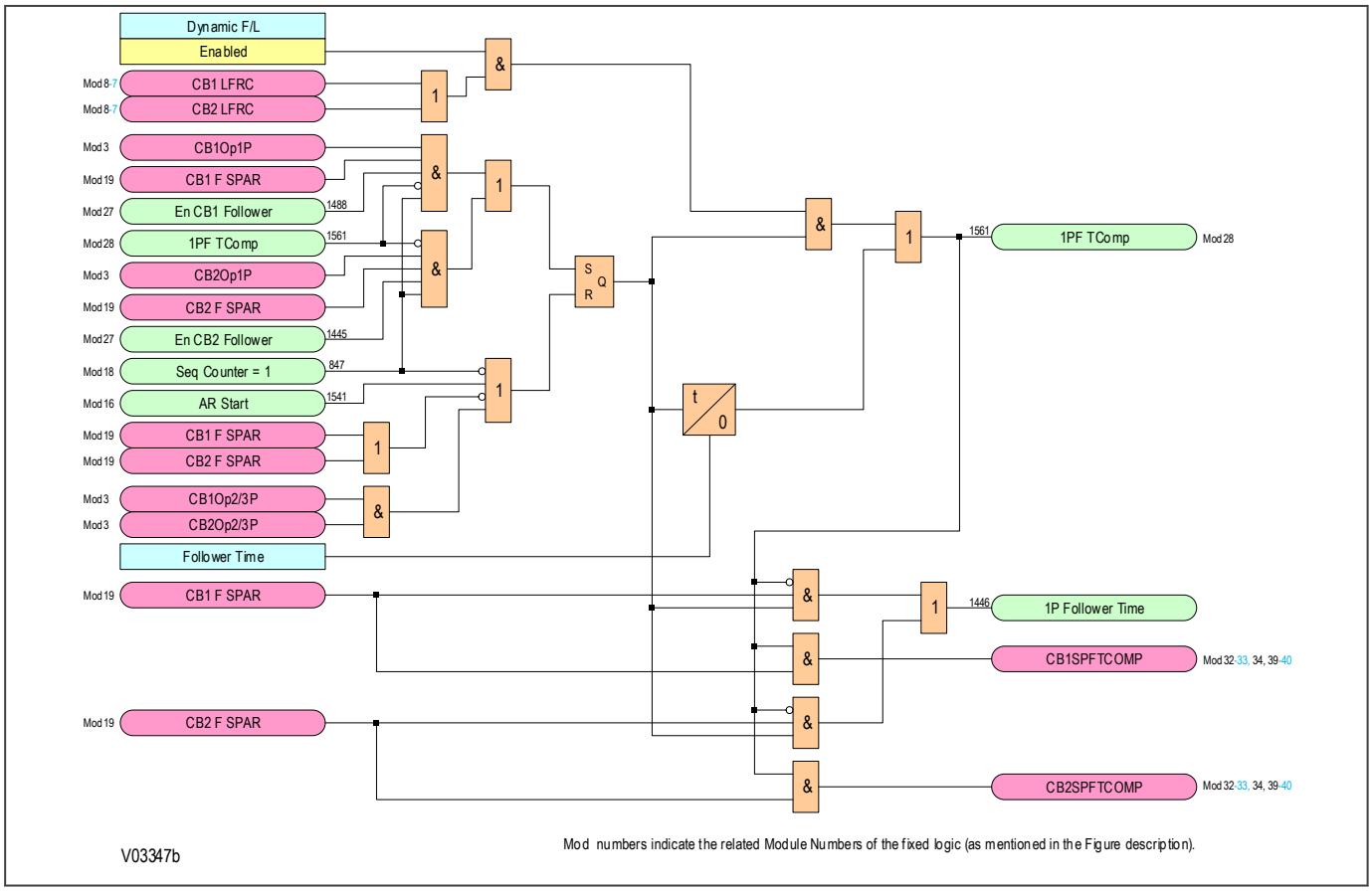


Figure 268: Single-phase follower CB timing logic (module 28)

12.5.12.7 THREE-PHASE FOLLOWER TIMING LOGIC DIAGRAM

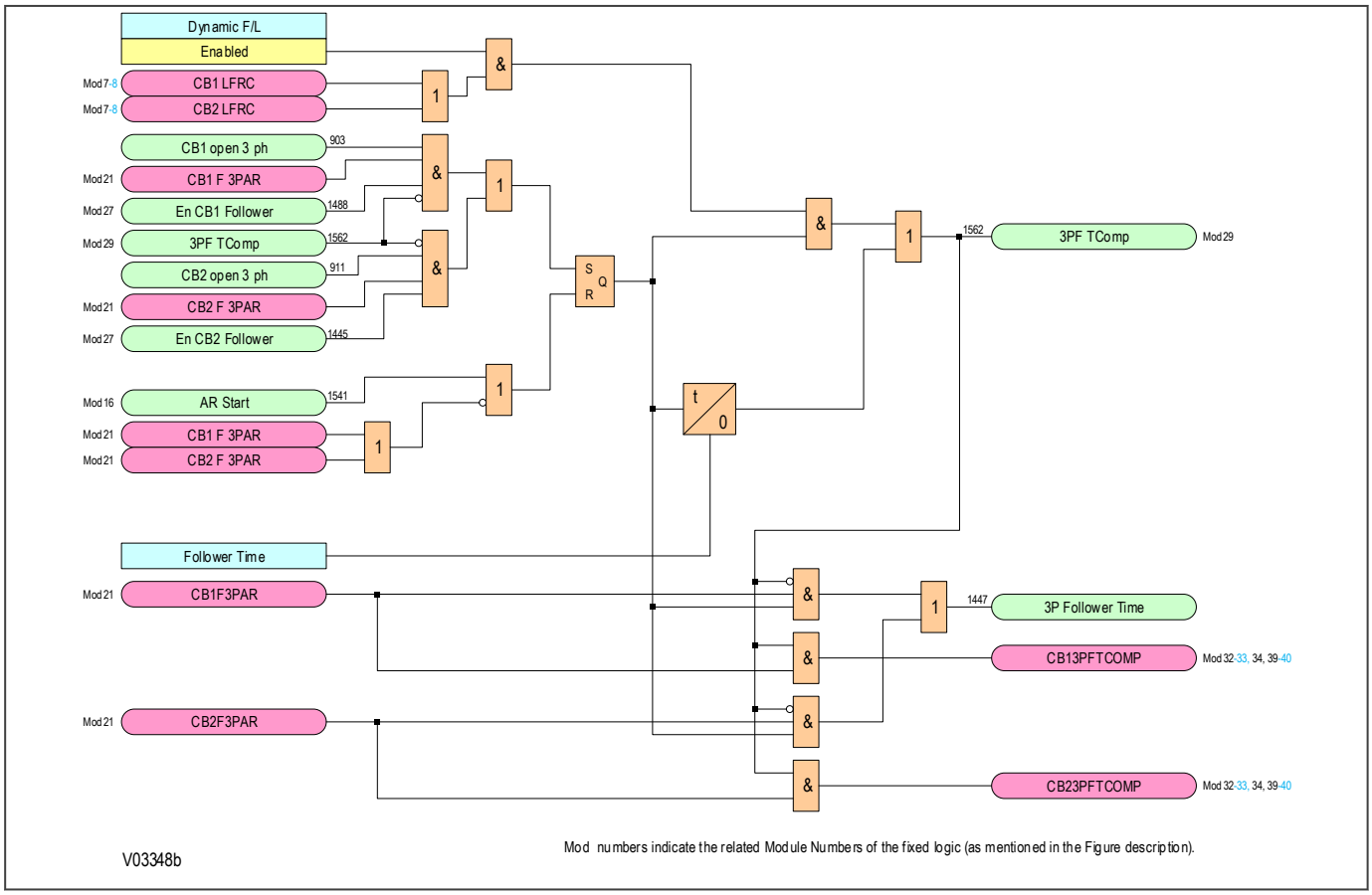


Figure 269: Three-phase follower CB timing logic (module 29)

12.5.13 CIRCUIT BREAKER AUTOCLOSE

Autoclose logic takes effect when dead times have expired.

The Autoclose logic checks that all necessary conditions are satisfied before issuing an Autoclose command to the circuit breaker control scheme.

Before a circuit breaker can be closed, it must be healthy (sufficient energy to close, and if necessary re-trip) and it must not be in a lockout condition.

For three-phase Autoreclose, the circuit breaker must be open on all three phases and the appropriate system check conditions must be met. For single-phase Autoreclose, the circuit breaker must be open on that phase.

The Autoclose command is a pulse lasting 100 milliseconds. Another command (***Set CB Close***) to set the circuit breaker to close is asserted as well as the Autoclose command. This signal will remain set either until the end of the Autoreclose cycle, or until the next protection operation. These commands are used to initiate the Reclaim Time logic and the Autoreclose Shot Counter logic.

12.5.13.1 CIRCUIT BREAKER AUTOCLOSE LOGIC DIAGRAM

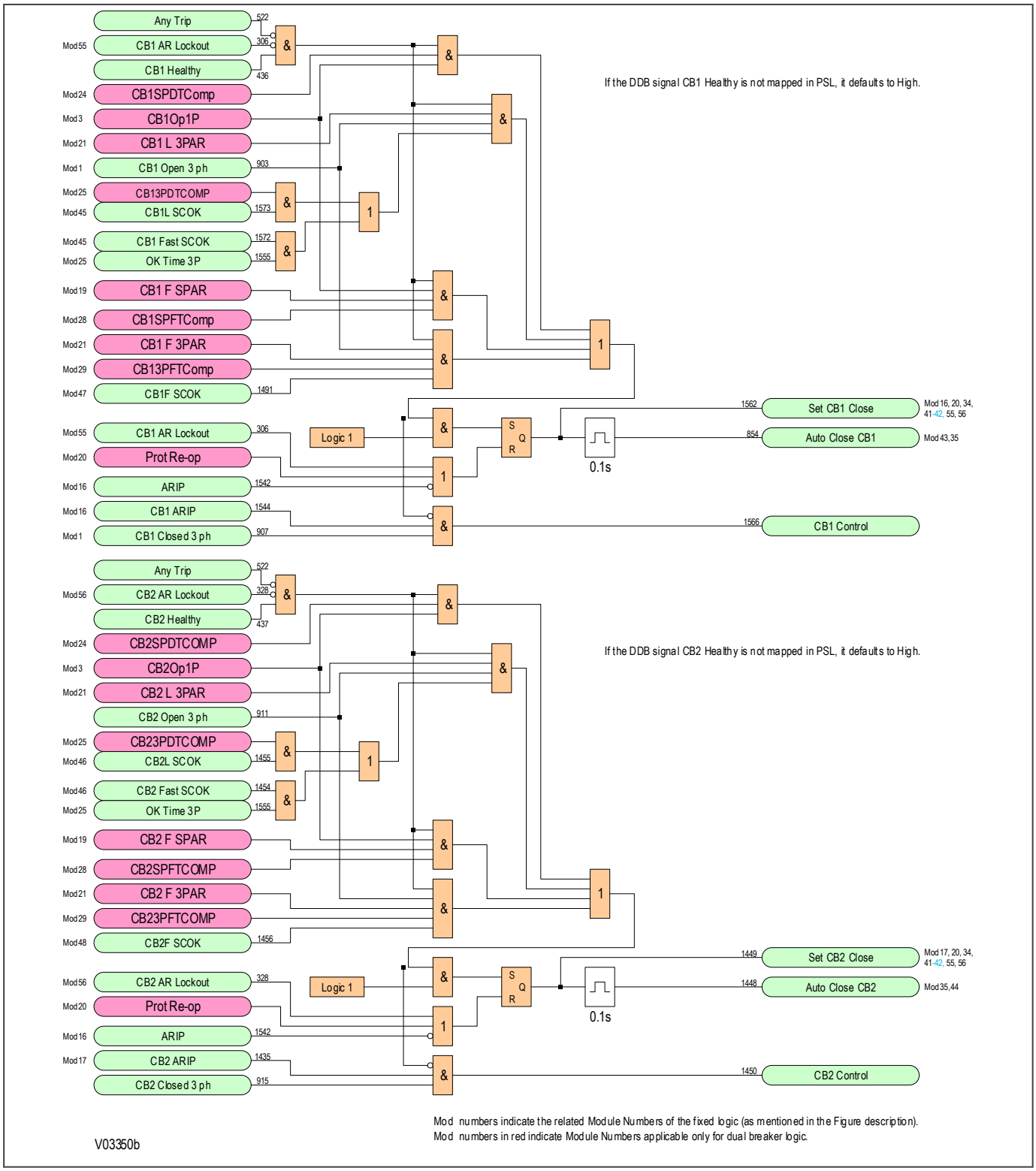


Figure 270: Circuit breaker autoclose logic (modules 32 & 33)

12.5.14 RECLAIM TIME

If the protection operates again before the reclaim time has expired, the corresponding sequence counter is incremented. At the same time, any “dead time complete” (….DTCOMP) signals are reset and the logic is prepared for the next dead time to start when conditions are suitable. The operation also resets the signal that would set the circuit breaker to close, and stops and resets the reclaim timer. The reclaim time starts again if the signal to set a circuit breaker to close goes high following completion of a dead time in a subsequent Autoreclose cycle. Where the reclaim extend time signal is set, the reclaim time cannot time out and reset the Autoreclose cycle before the time delayed protection has fully operated

If the circuit breaker is closed and has not tripped again when the reclaim time expires, signals are generated to indicate successful Autoreclose. These signals increment the relevant circuit breaker successful Autoreclose shot counters and reset the relevant Autoreclose in progress signal.

The “successful Autoreclose” signals generated from the logic can be reset by various commands and settings options available under *CB CONTROL* menu settings as follows:

If ***Res AROK by UI*** is set to `Enabled`, all the signals can be reset by user interface command ***Reset AROK Ind*** from the *CB CONTROL* menu.

If ***Res AROK by NoAR*** is set to `Enabled`, the signals for each circuit breaker can be reset by temporarily generating an Autoreclose disabled signal according to the logic shown.

If ***Res AROK by Ext*** is set to `Enabled`, the signals can be reset by activation of an external input signal appropriately mapped in the PSL.

If ***Res AROK by TDly*** is set to `Enabled`, the signals are automatically reset after a time delay set in ***AROK Reset Time***.

12.5.14.1 PREPARE RECLAIM INITIATION LOGIC DIAGRAM

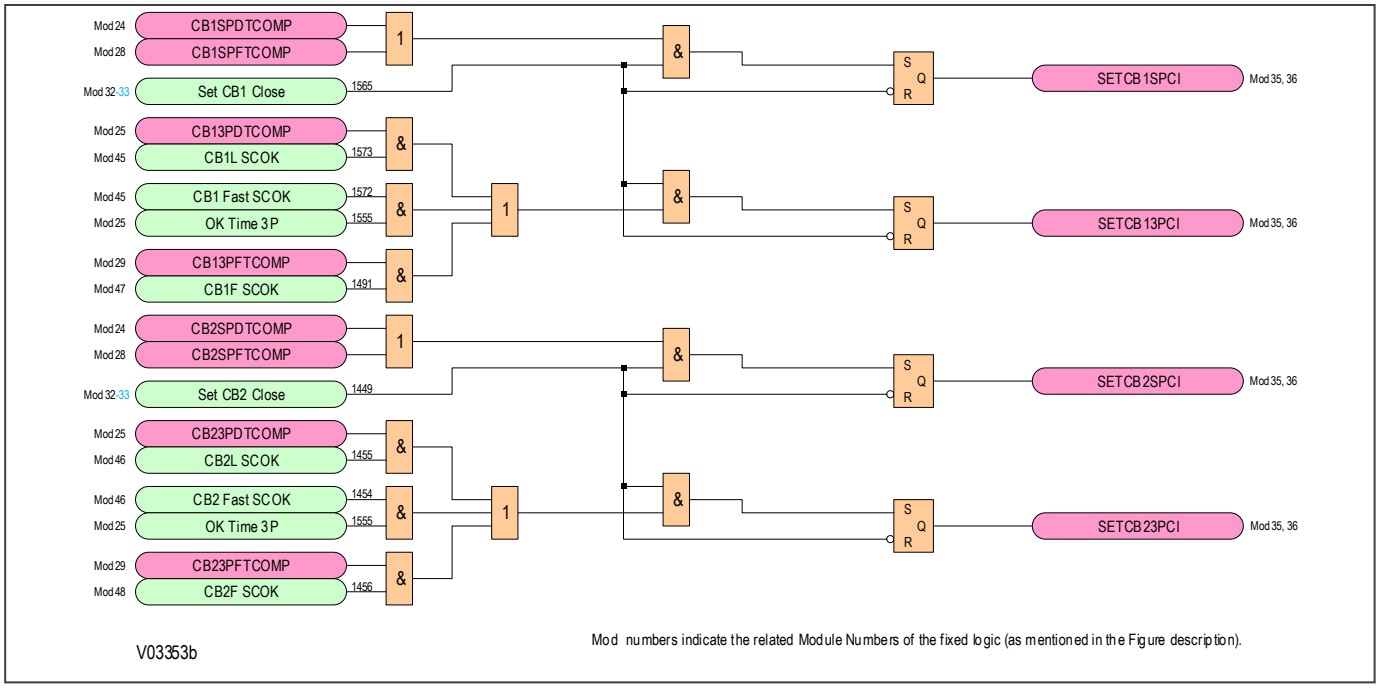


Figure 271: Prepare reclaim initiation logic (module 34)

12.5.14.2 RECLAIM TIME LOGIC DIAGRAM

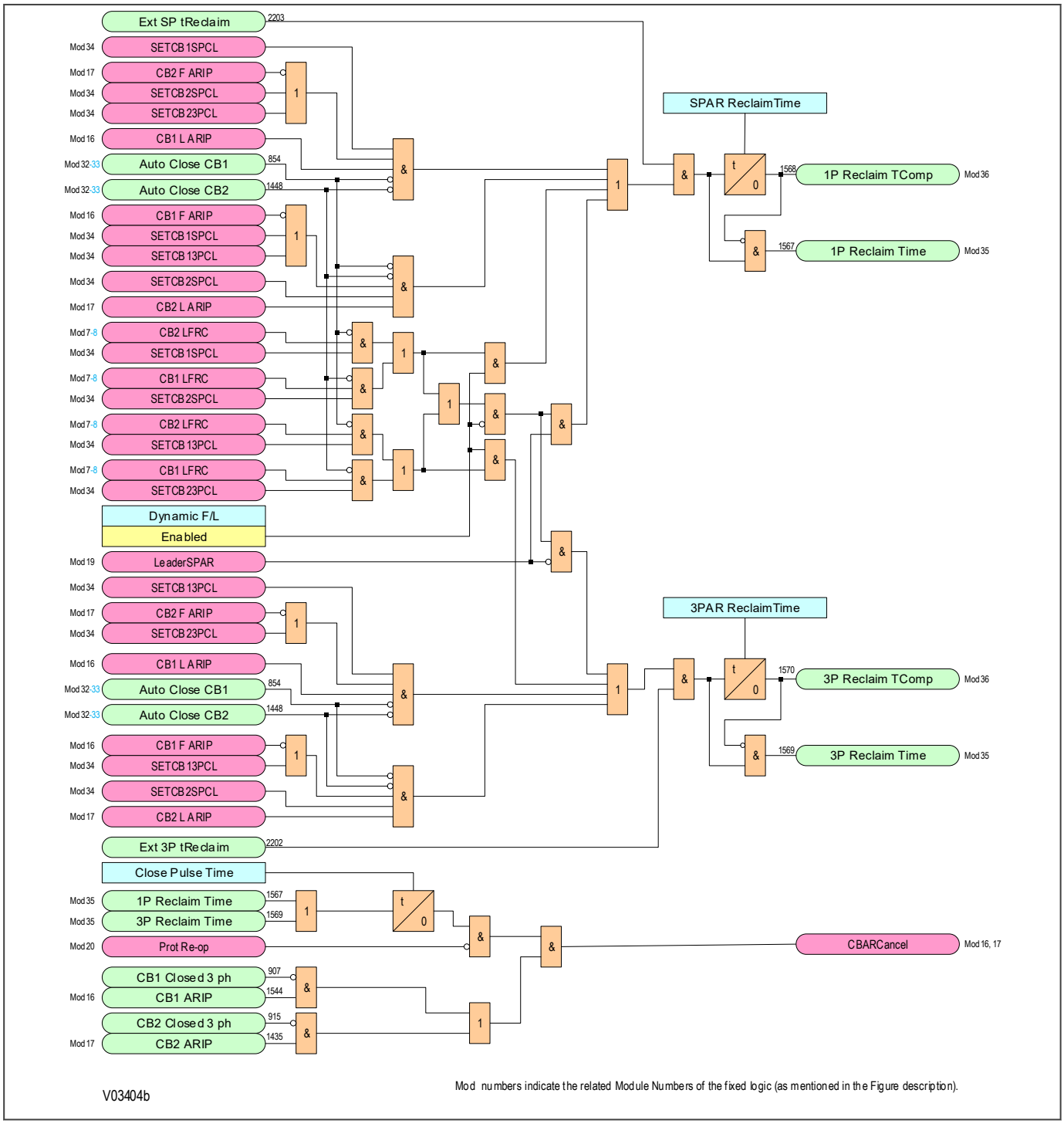


Figure 272: Reclaim time logic (module 35)

12.5.14.3 SUCCESSFUL AUTORECLOSE SIGNALS LOGIC DIAGRAM

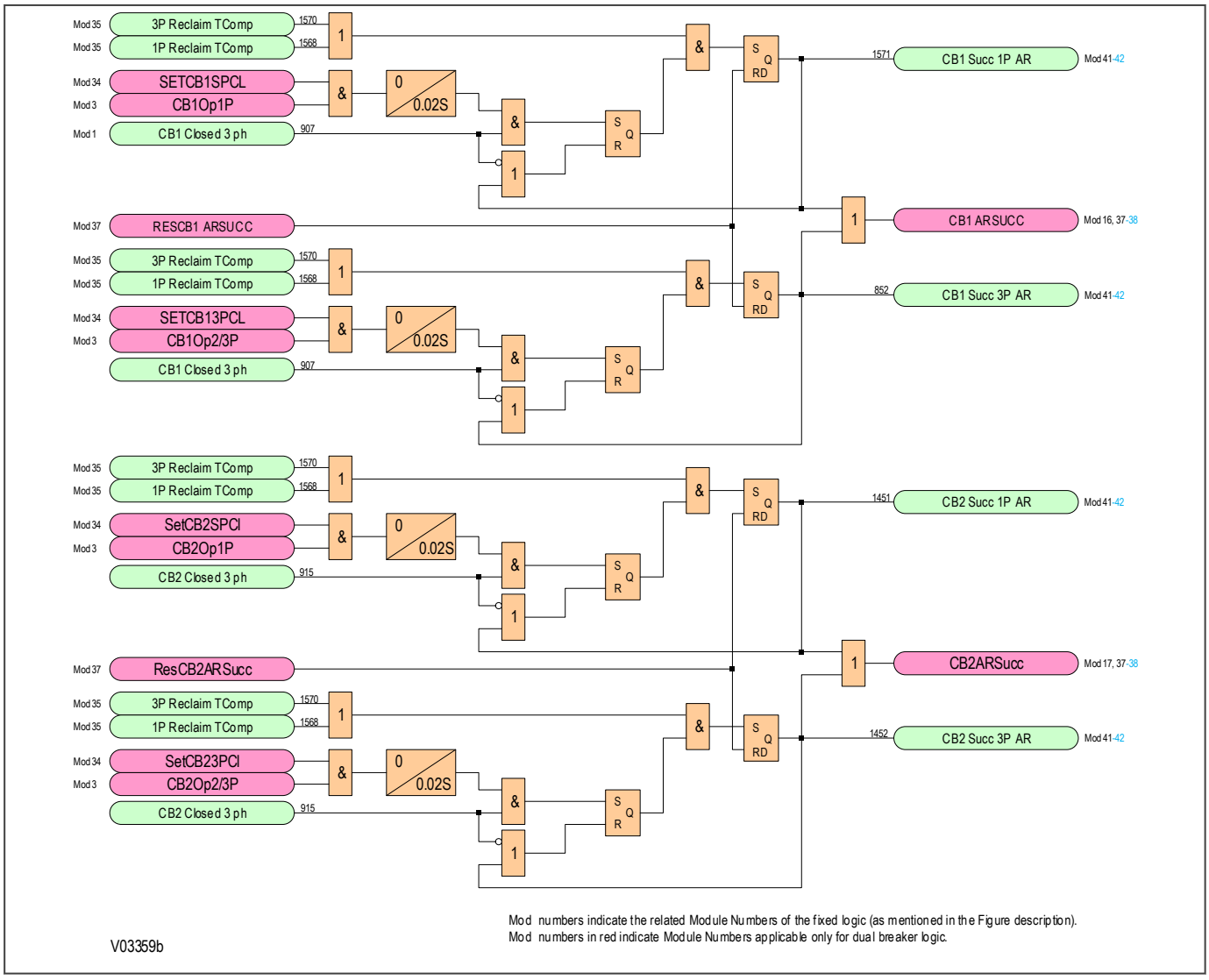


Figure 273: Successful autoreclose signals logic (module 36)

12.5.14.4 AUTORECLOSE RESET SUCCESSFUL INDICATION LOGIC DIAGRAM

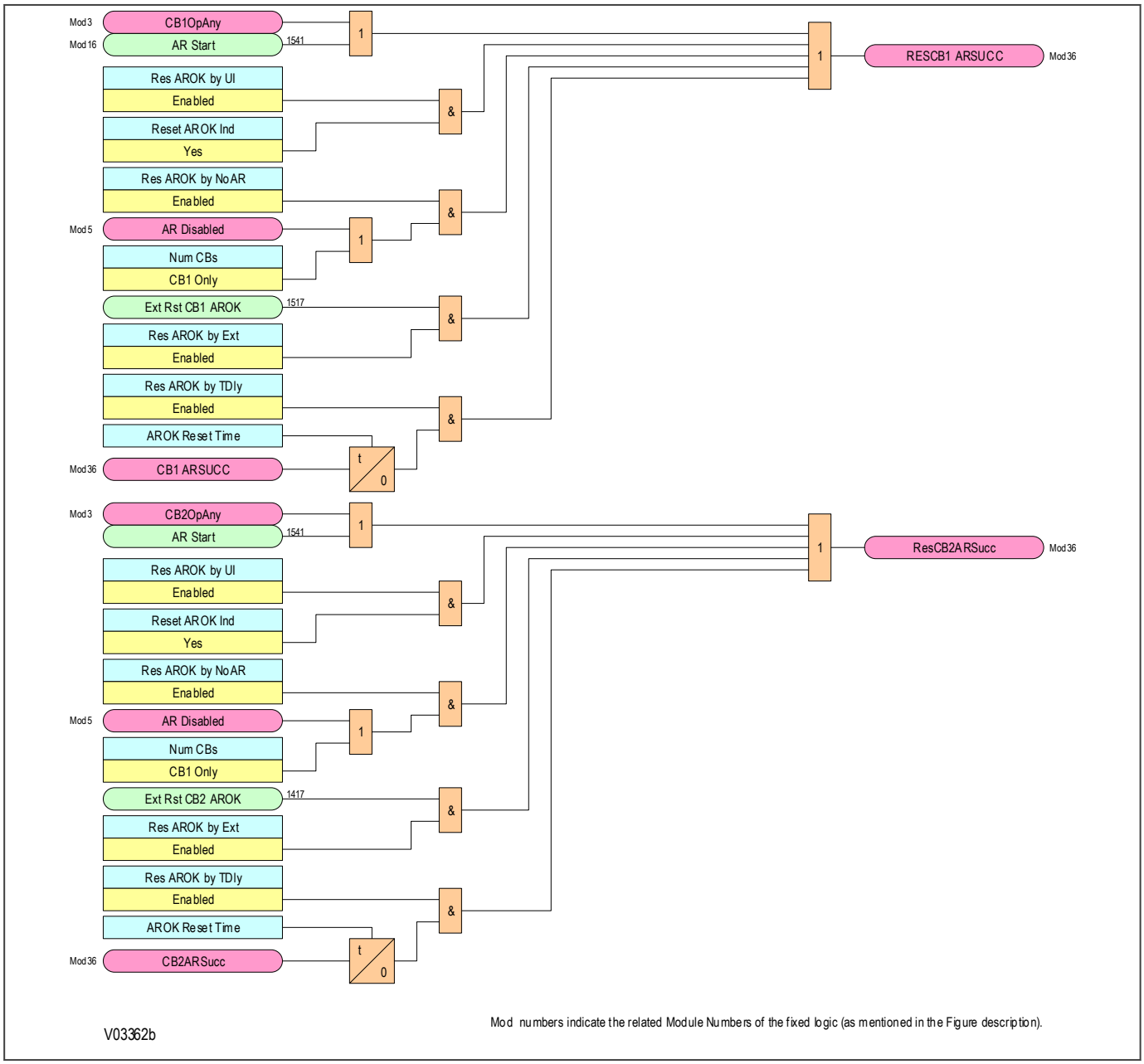


Figure 274: Autoreclose reset successful indication logic (modules 37 & 38)

12.5.15 CB HEALTHY AND SYSTEM CHECK TIMERS

This logic provides signals to cancel Autoreclose if the circuit breaker is not healthy (for example low gas pressure) or system check conditions are not satisfied (for example required line & bus voltage conditions) when the scheme is ready to close the circuit breaker.

At the completion of a dead time, the logic starts an Autoreclose healthy timer. If a circuit breaker healthy signal becomes high before the Autoreclose healthy time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker healthy signal stays low, then, at the end of the Autoreclose healthy time, a circuit breaker unhealthy alarm is raised. This forces the Autoreclose sequence to be cancelled.

Additionally, at the completion of any three-phase dead time, the logic starts an Autoreclose check synchronism timer. If the circuit breaker synchronism-check OK signal goes high before the time is complete, the timer stops and, if all other relevant circuit breaker closing conditions are satisfied, the scheme issues a circuit breaker Autoclose signal. If the circuit breaker synchronism-check OK signal stays low, then when the Autoreclose check synchronism timer expires, an alarm is set to inform that the check synchronism is not satisfied and cancels the Autoreclose cycle.

12.5.15.1 CB HEALTHY AND SYSTEM CHECK TIMERS LOGIC DIAGRAM

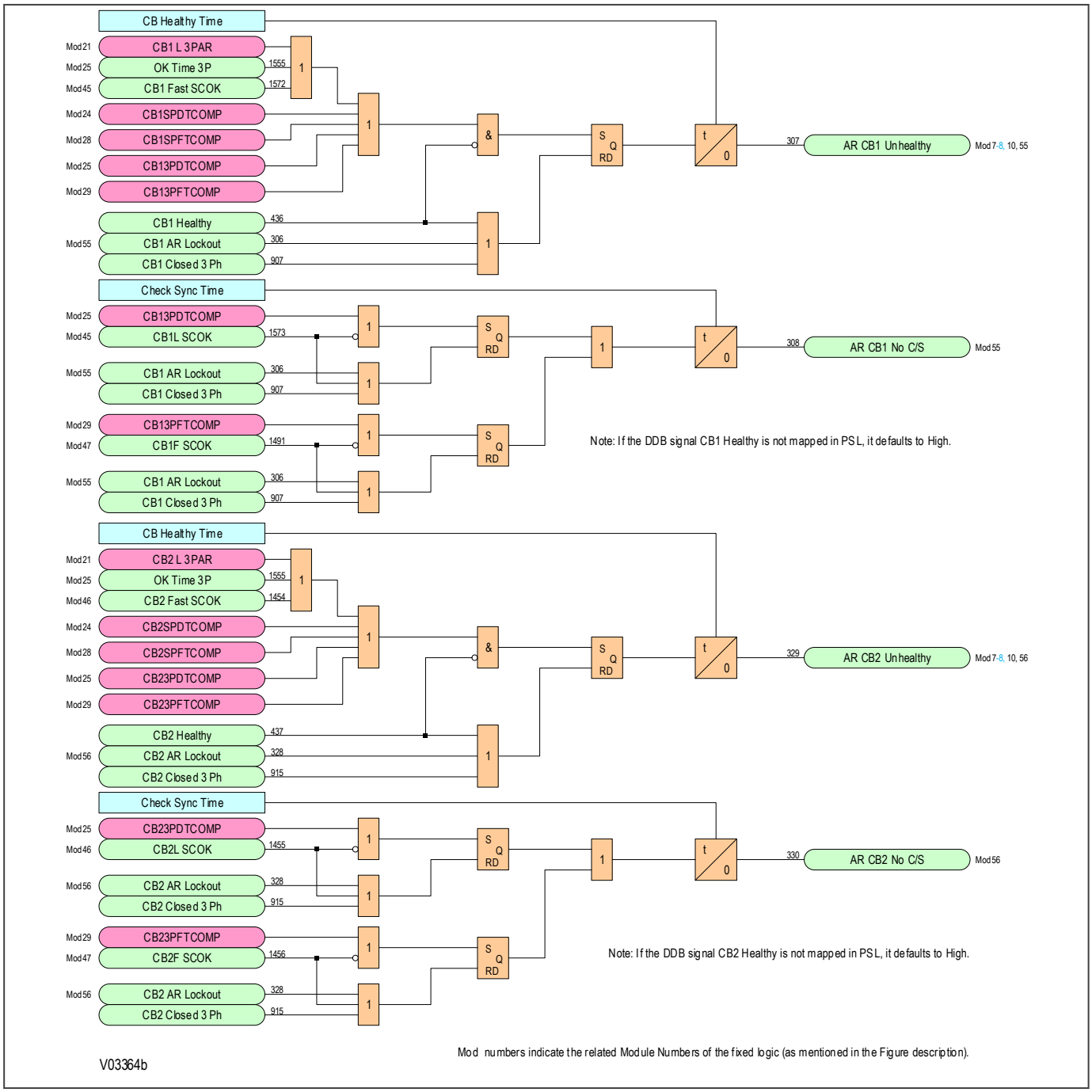


Figure 275: Circuit breaker healthy and system check timers healthy logic (module 38 & 40)

12.5.16 AUTORECLOSE SHOT COUNTERS

A number of counters are provided to enable analysis of circuit breaker Autoreclose history. The counters are stored in non-volatile memory, so that the data is maintained even in the event of a failure of the auxiliary supply. The counter values are accessible through the *CB CONTROL* column. The counters can be reset manually, or by activation of an input appropriately mapped in the PSL.

The logic provides the following summary information for each circuit breaker

- Overall total number of shots (Number of Autoreclose attempts)
- Number of successful 1st shot single-phase Autoreclose sequences
- Number of successful 1st shot three-phase Autoreclose sequences
- Number of successful 2nd shot three-phase Autoreclose sequences
- Number of successful 3rd shot three-phase Autoreclose sequences
- Number of successful 4th shot three-phase Autoreclose sequences
- Number of failed Autoreclose cycles which forced a circuit breaker to lockout

12.5.16.1 AUTORECLOSE SHOT COUNTERS LOGIC DIAGRAM

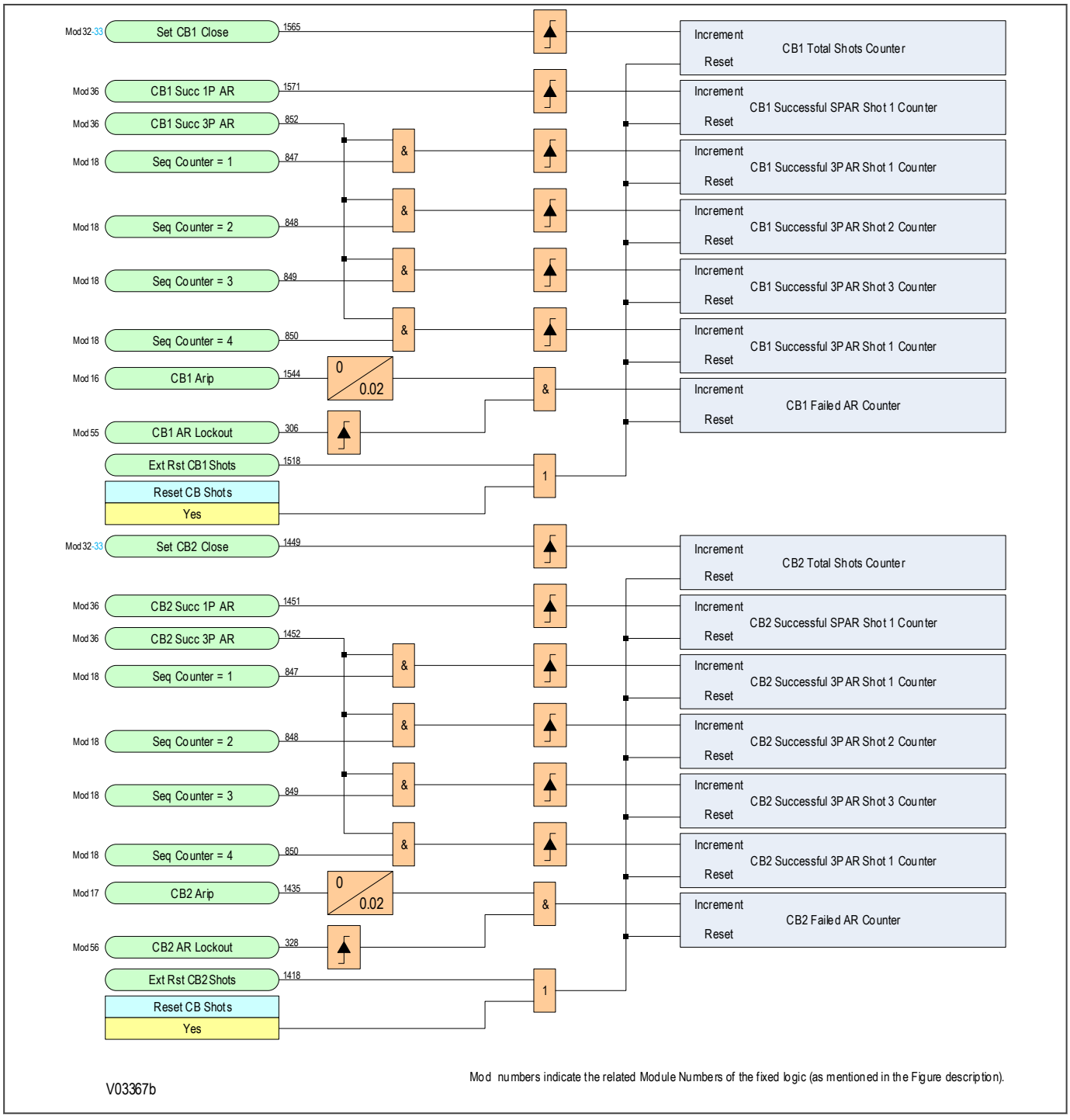


Figure 276: Autoreclose shot counters logic (modules 41 & 42)

12.5.17 CIRCUIT BREAKER CONTROL

12.5.17.1 CB CONTROL LOGIC DIAGRAM

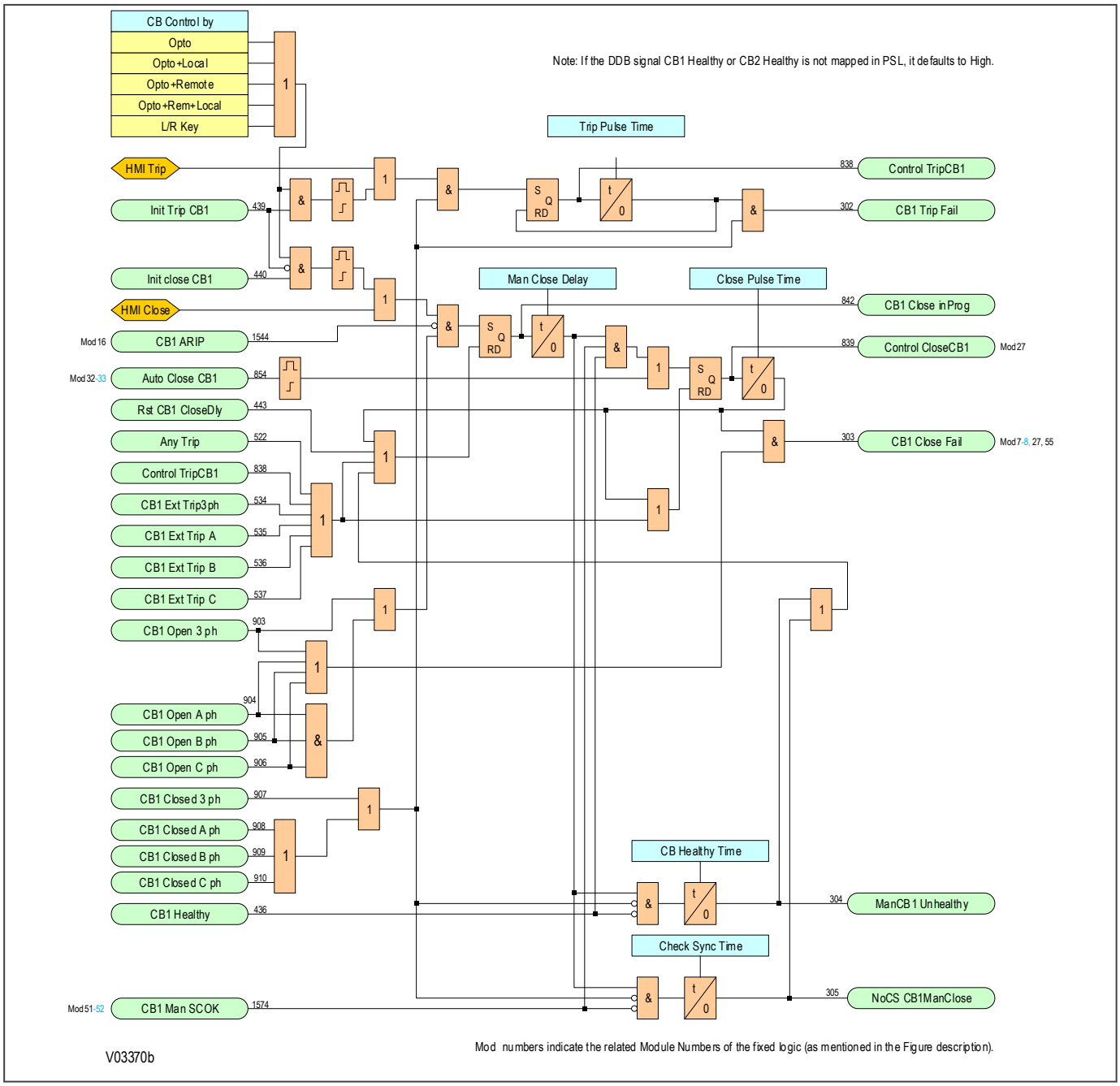


Figure 277: CB1 control logic (module 43)

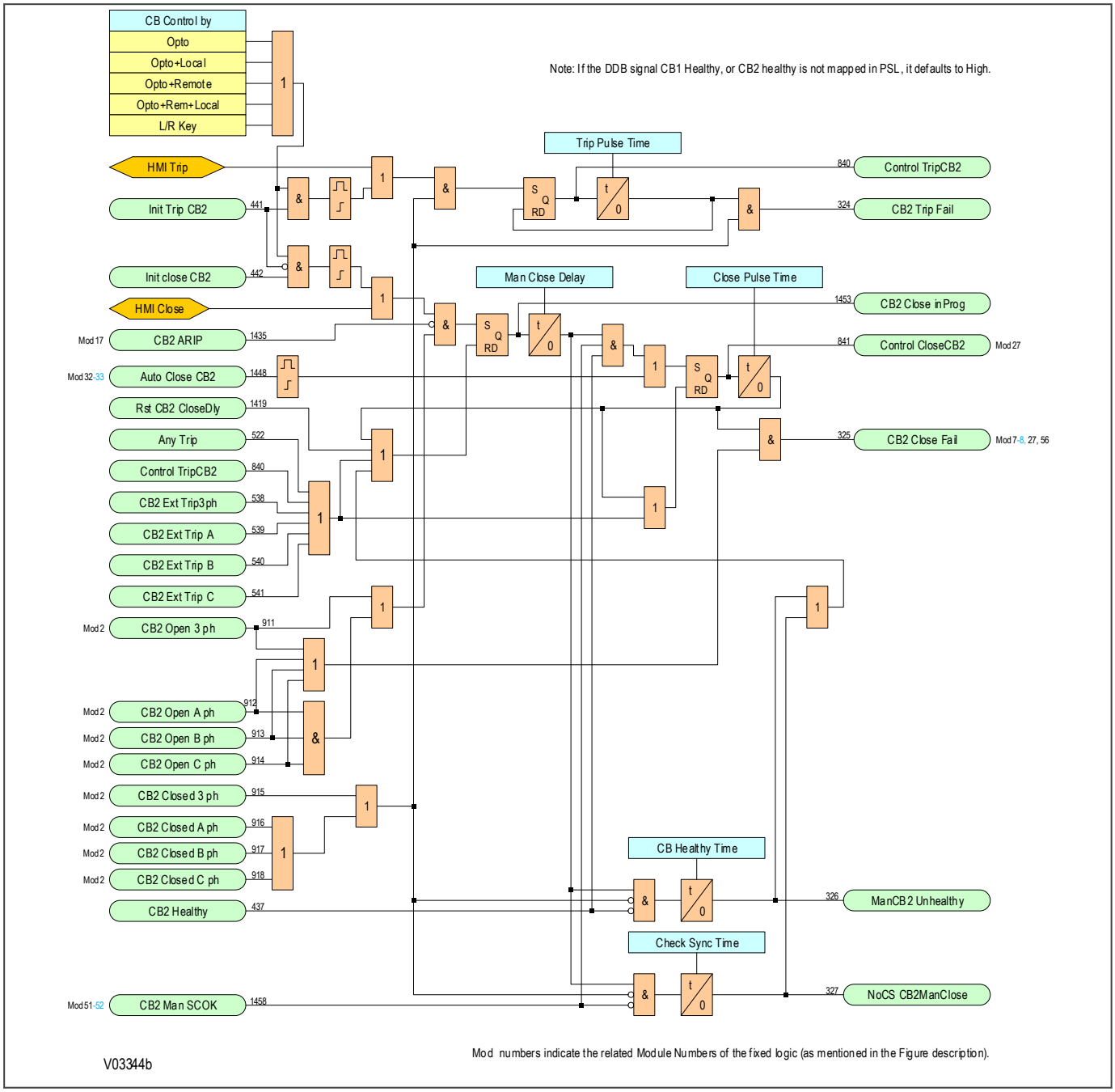


Figure 278: CB2 control logic (module 44)

12.5.18 CIRCUIT BREAKER TRIP TIME MONITORING

The circuit breaker trip time monitoring logic checks for correct circuit breaker tripping following the issue of a protection trip signal. When the protection trip signal is issued, a timer controlled by the ***Trip Pulse Time*** setting in the *CB CONTROL* column is started.

If the circuit breaker trips correctly the timer resets. If Autoreclose is enabled and the timer resets, the cycle continues. If the circuit breaker fails to trip correctly within the set time, the Autoreclose cycle is forced to lock out and a signal is issued indicating that the circuit breaker failed to trip in response to the protection operation.

12.5.18.1 CB TRIP TIME MONITORING LOGIC DIAGRAM

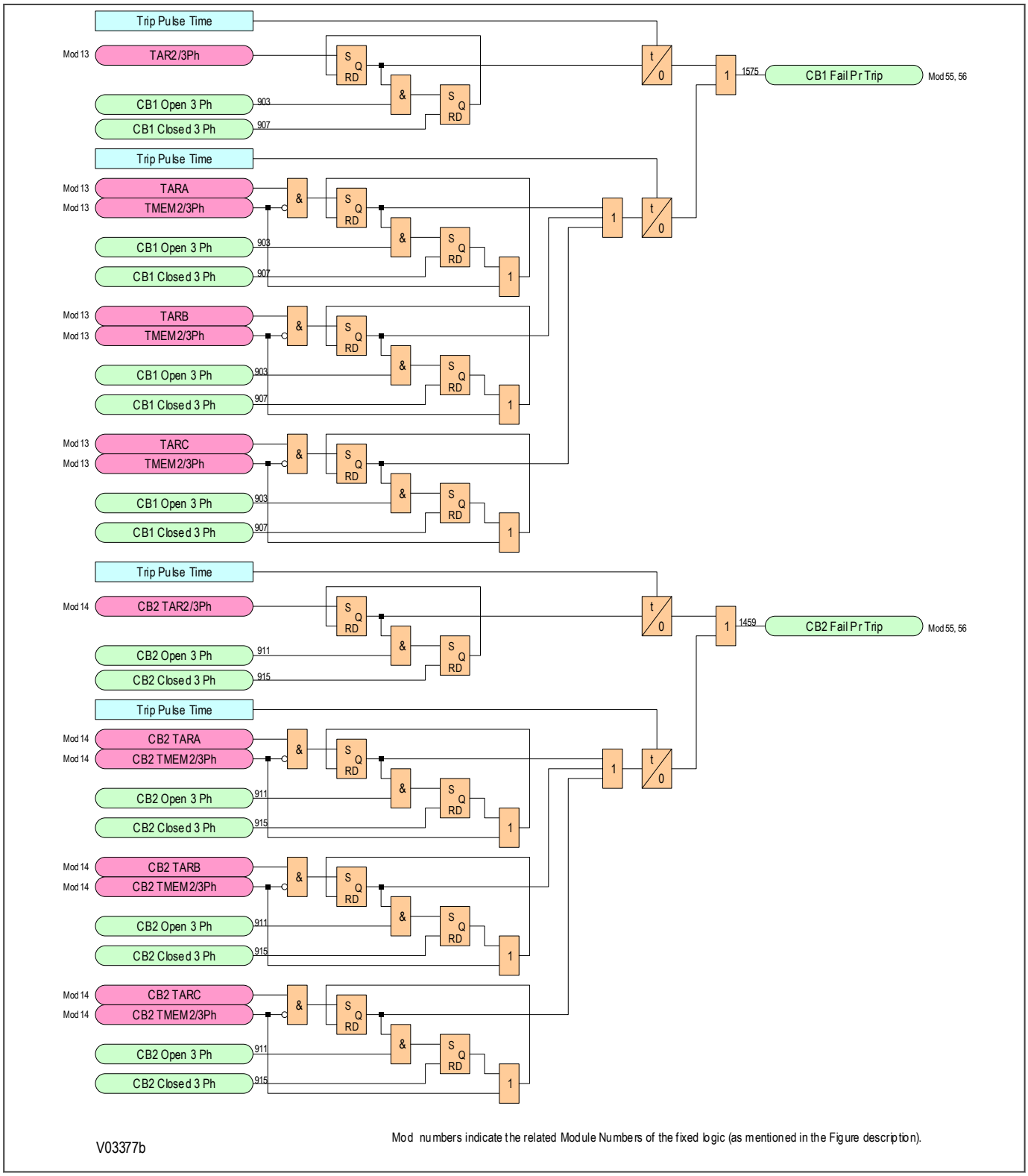


Figure 279: Circuit breaker trip time monitoring logic (modules 53 & 54)

12.5.19 AUTORECLOSE LOCKOUT

A number of events will cause Autoreclose lockout. If this happens an Autoreclose lockout alarm is raised. In this condition, Autoreclose cannot be initiated until the corresponding lockout has been reset.

The following events force Autoreclose lockout:

- Protection operation during reclaim time. Following the final Autoreclose attempt, if the protection operates during the reclaim time, the AR cycle goes to AR lockout and the Autoreclose function is disabled until the AR lockout condition is reset.
- Persistent fault. A fault is considered persistent if the protection re-operates after the last permitted shot.
- Block Autoreclose. If the block Autoreclose DDB is asserted whilst Autoreclose is in progress, the cycle goes to lockout.
- Protection function selection. Setting 'Block AR' against a particular protection function in the AUTORECLOSE column means that operation of the protection will block Autoreclose and force lockout.
- Circuit breaker failure to close. If a circuit breaker fails to close Autoreclose is blocked and forced to lockout.
- Circuit breaker remains open at the end of the reclaim time. An Autoreclose lockout is forced if the circuit breaker is open at the end of the reclaim time.
- Circuit breaker fails to close when the close command is issued.
- Circuit breaker fails to trip correctly.
- Three-phase dead time started by 'line dead' violation. If the line does not go dead within the ***Dead Line Time*** setting, the logic forces the Autoreclose sequence to lockout. Determination of when to start the timer is made in the ***3PDTStart WhenLD*** setting.
- Block Follower if Leader fails to close is set. If the setting ***BF if Lfail Cls*** in the *AUTORECLOSE* column is set to `Enable`, the active Follower circuit breaker will lockout if the Leader circuit breaker fails to reclose.
- Leader/Follower invalid selection using opto-isolated input. If the Leader/Follower Autoreclose mode in the *AUTORECLOSE* settings is set to be selected using the opto-isolated inputs, then if the logic detects an invalid Autoreclose mode combination, it forces both circuit breakers to lockout if a trip occurs.

12.5.19.1 CB LOCKOUT LOGIC DIAGRAM

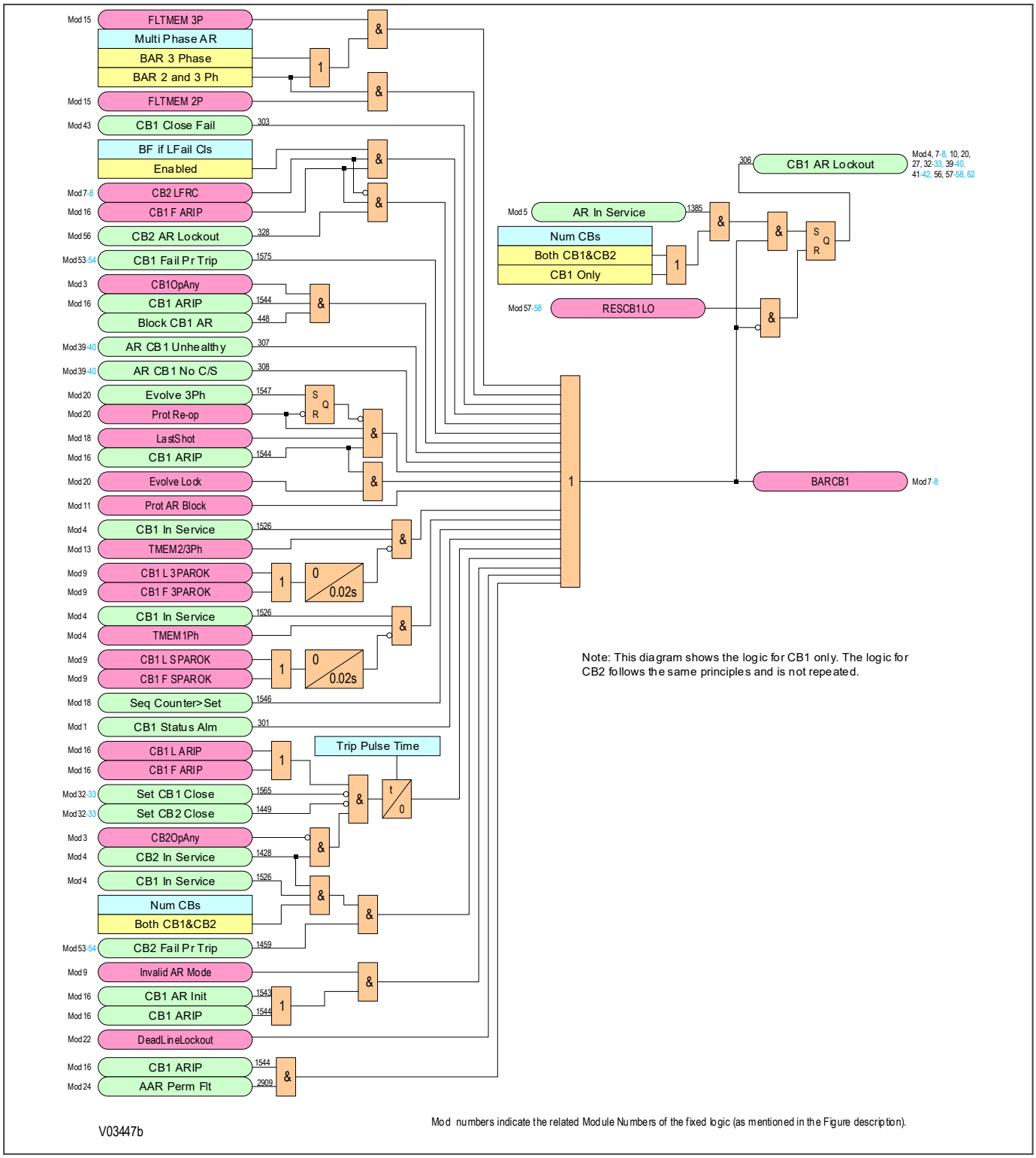


Figure 280: CB1 lockout logic (module 55)

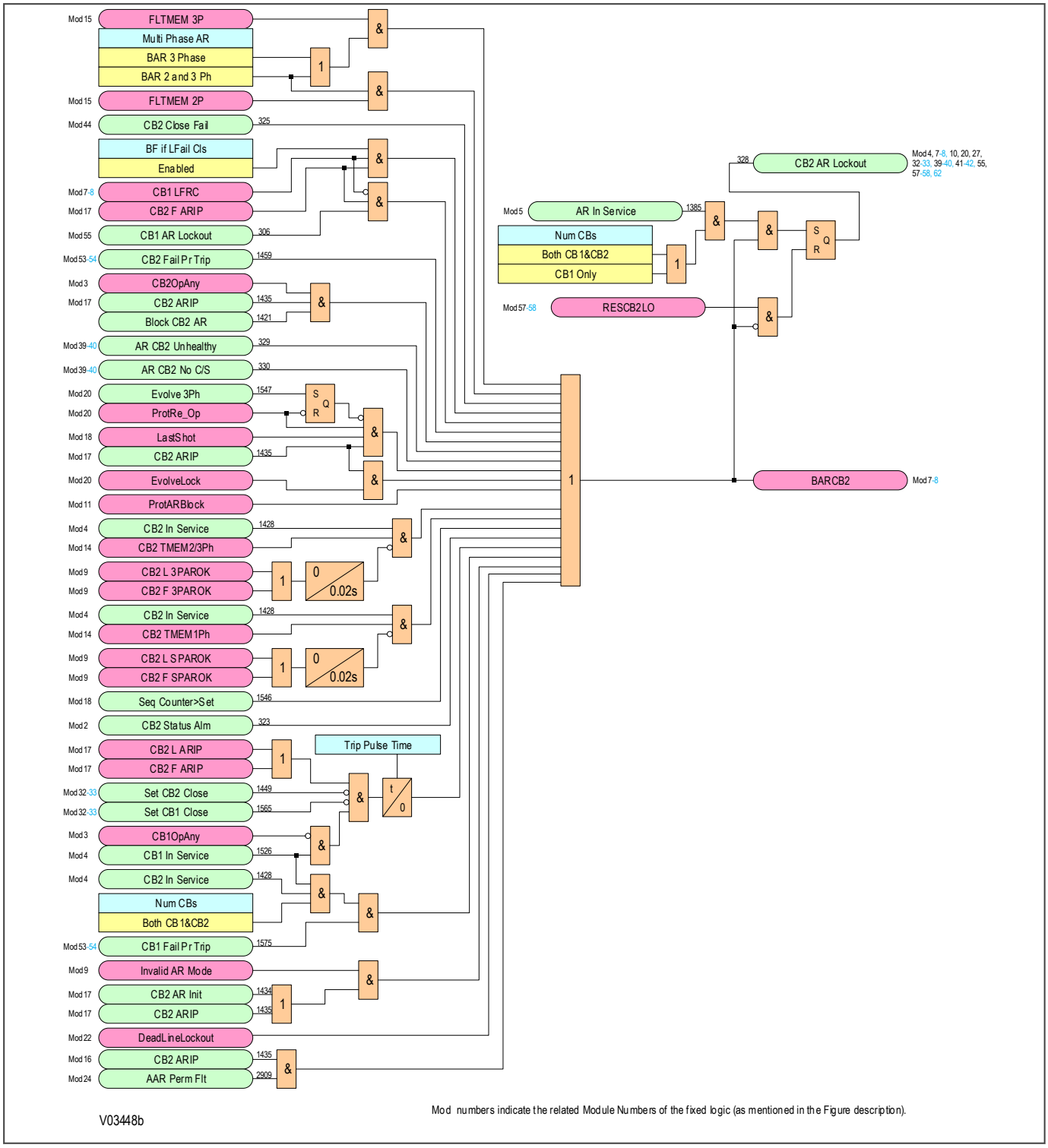


Figure 281: CB2 lockout logic (module 56)

12.5.20 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to `Enabled`, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to `Enabled`, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to `Enabled`, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to `Enabled`, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is `Enabled`, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

12.5.20.1 RESET CB LOCKOUT LOGIC DIAGRAM

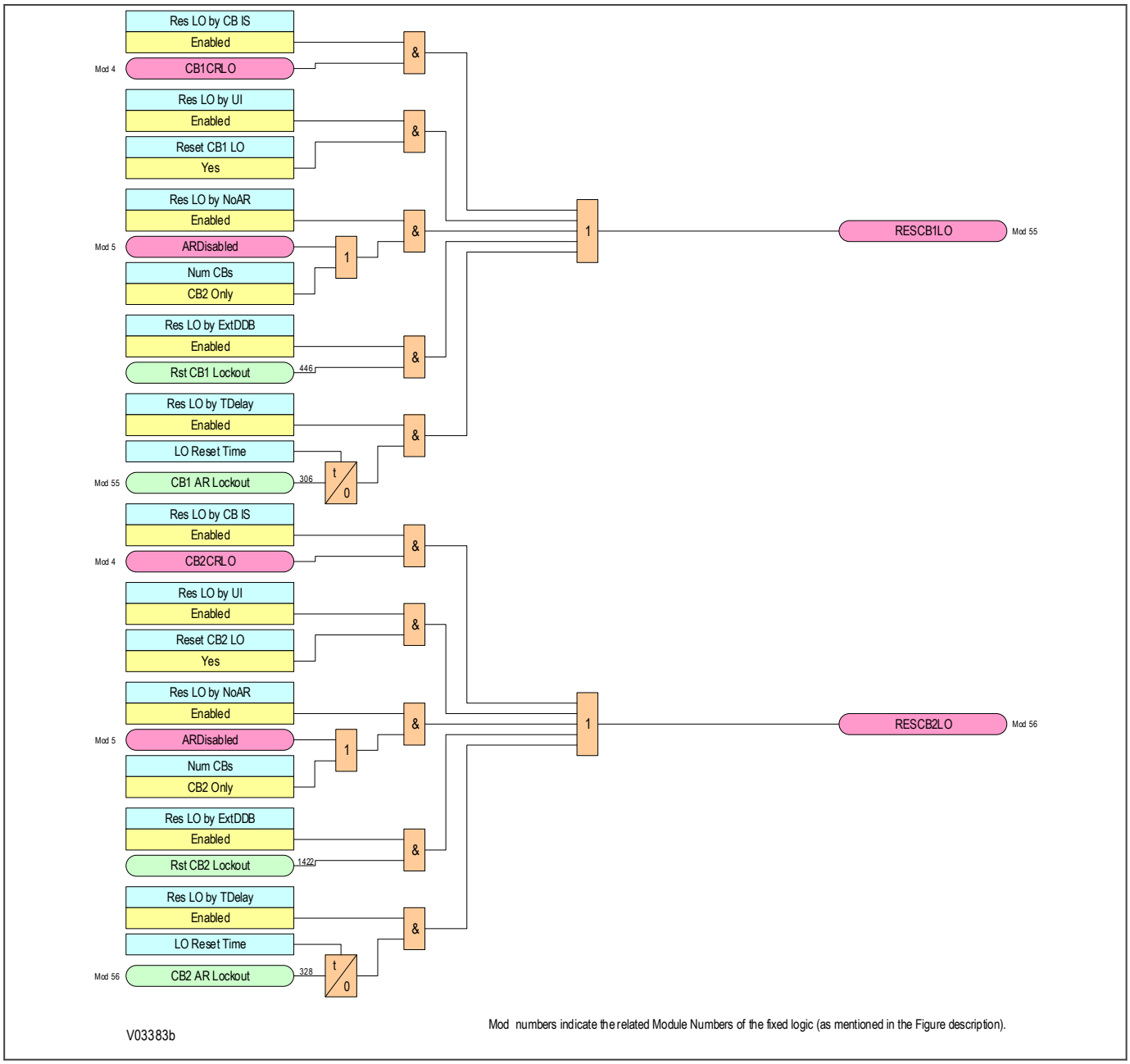


Figure 282: Reset circuit breaker lockout logic (modules 57 & 58)

12.5.21 POLE DISCREPANCY

In a three-pole CB, certain combinations of poles open and closed are indicative of a problem. The Pole Discrepancy Logic combines an indication of a Pole Discrepancy condition from the CB Monitoring logic with signals from the internal Autoreclose logic to produce a combined Pole Discrepancy indication for the CB.

12.5.21.1 POLE DISCREPANCY LOGIC DIAGRAM

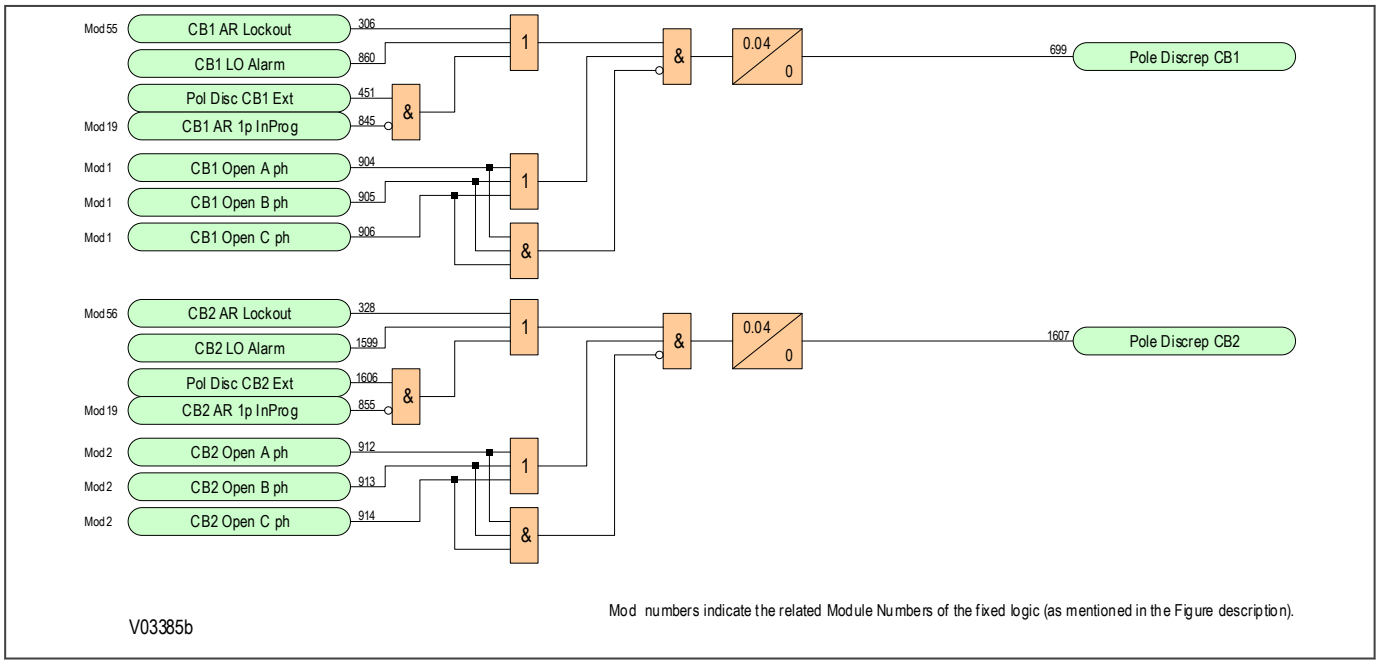


Figure 283: Pole discrepancy logic (module 62)

12.5.22 CIRCUIT BREAKER TRIP CONVERSION

Circuit breakers should only trip single-pole or three-pole. The trip conversion logic ensures that the tripping is either single-pole or three-pole. The trip conversion logic ensures that all conditions that should cause three-pole tripping do so. Indication of the number of phases that caused tripping is provided.

12.5.22.1 CB TRIP CONVERSION LOGIC DIAGRAM

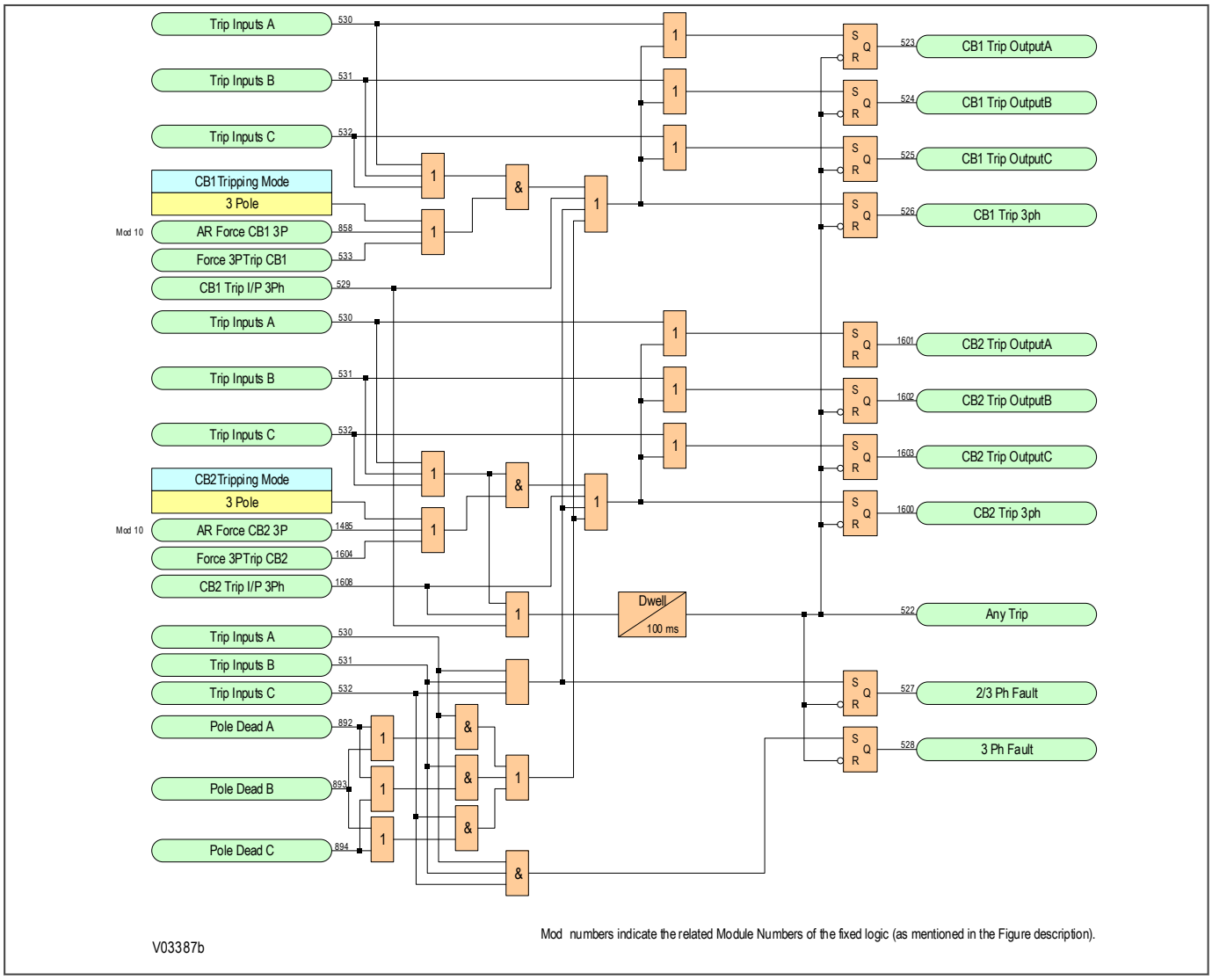


Figure 284: Circuit breaker trip conversion logic (module 63)

12.5.23 MONITOR CHECKS FOR CB CLOSURE

For single-phase Autoreclose neither voltage nor synchronisation checks are needed as synchronising power should be flowing in the two healthy phases. For three-phase Autorelcose, for the first shot (and only the first shot), you can choose to attempt reclosure without performing a synchronisation check. The setting to permit Autoreclose without checking synchronising conditions is ***CB SC Shot 1***.

Otherwise, synchronising checks on voltages, relative frequencies, and relative phase angles are needed to ensure that sympathetic conditions exist before CB closure is attempted.

The following diagrams detail the Monitor Checks for CB closure.

12.5.23.1 VOLTAGE MONITOR FOR CB CLOSURE

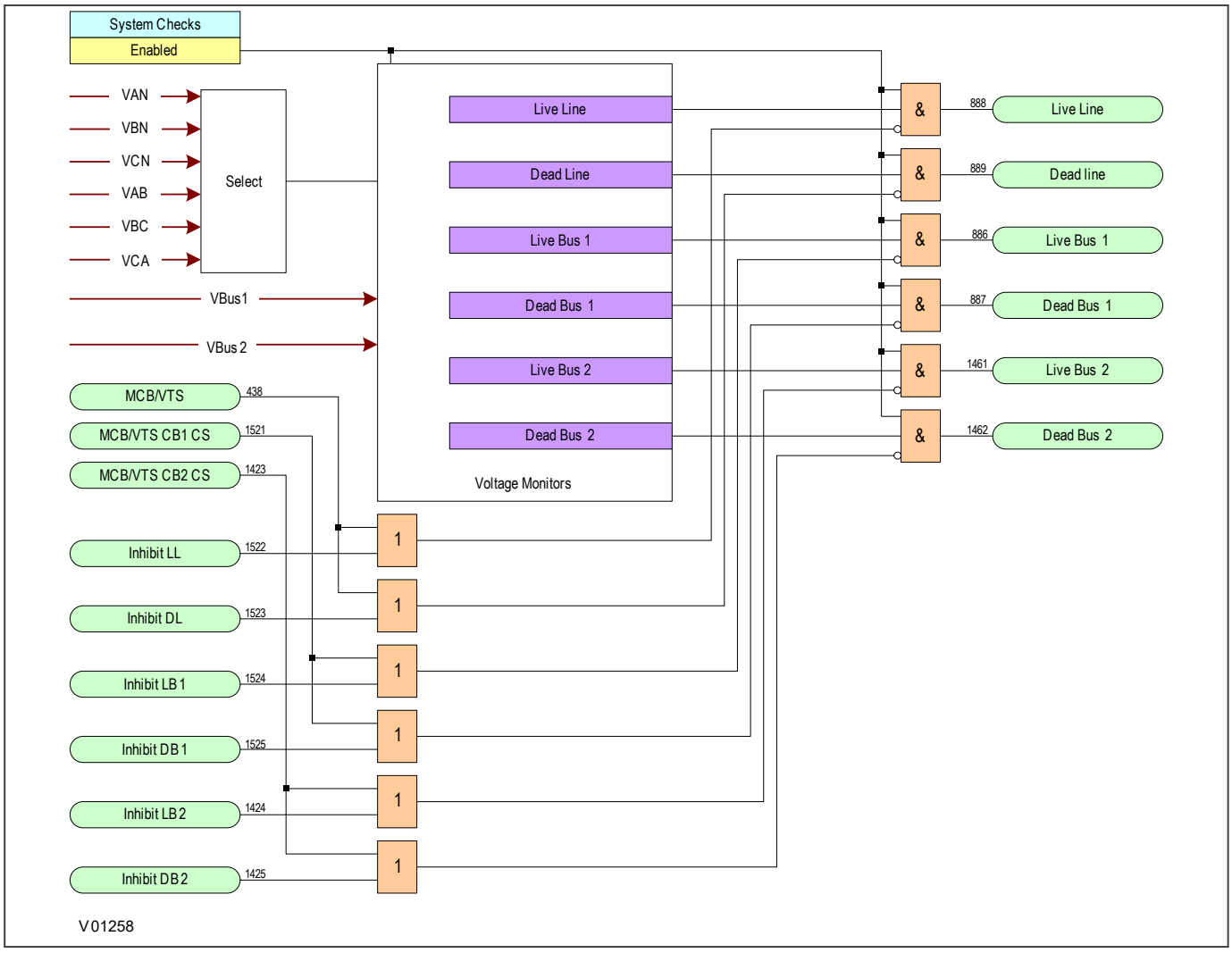


Figure 285: Voltage monitor for CB closure (module 59)

12.5.23.2 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

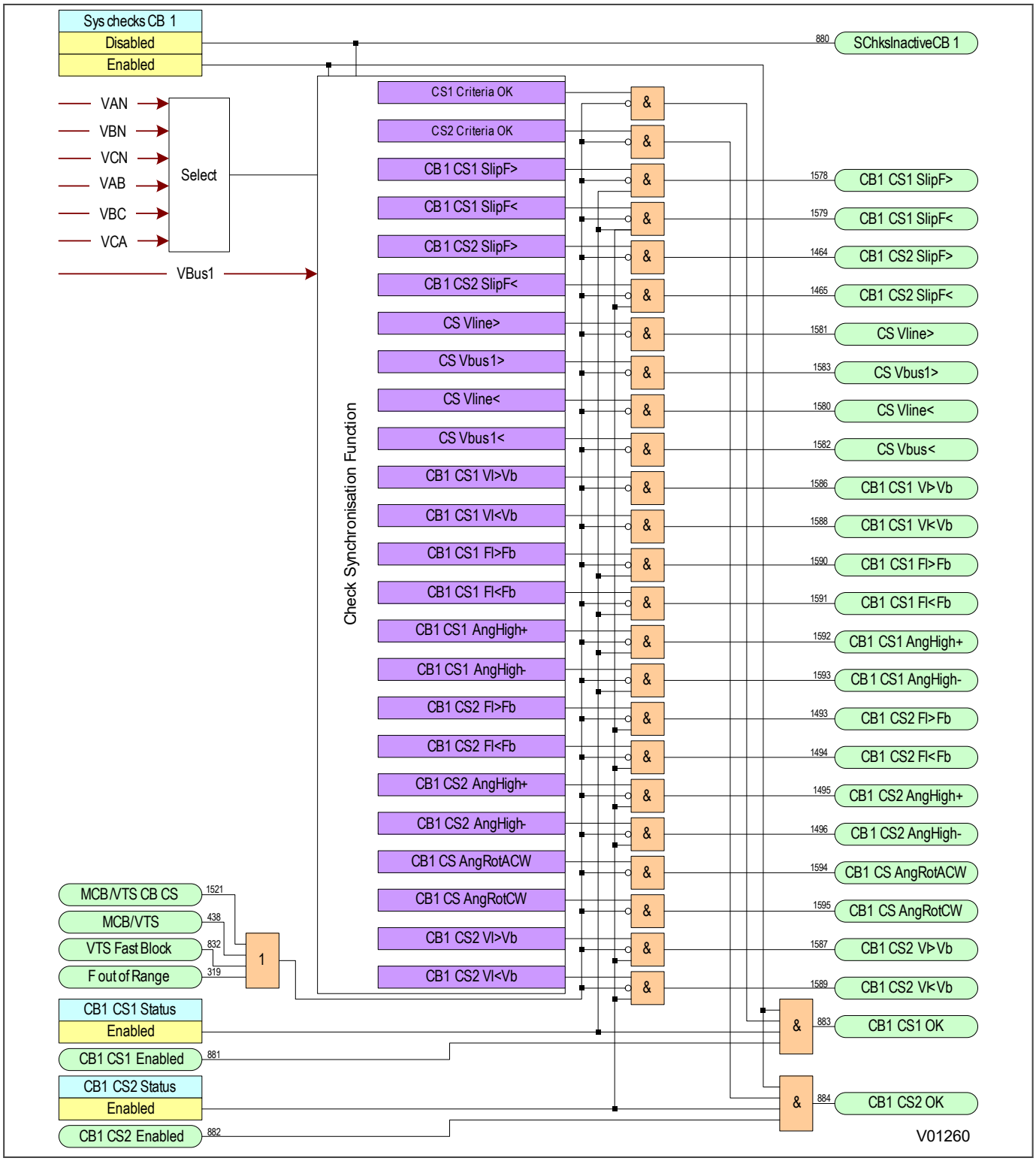


Figure 286: Check synchronisation monitor for CB1 closure (module 60)

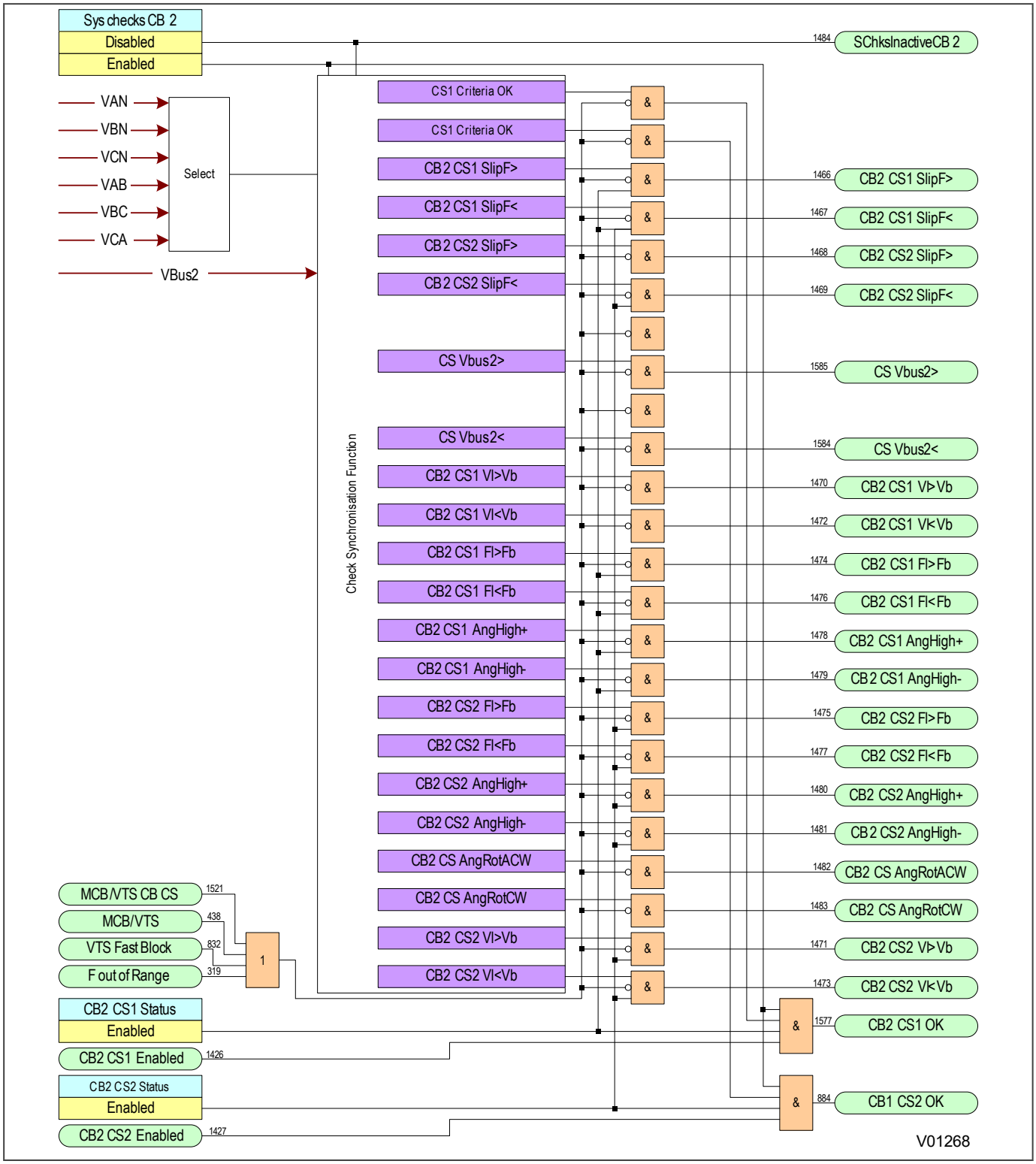


Figure 287: Check synchronisation monitor for CB2 closure (module 61)

12.5.24 SYNCHRONISATION CHECKS FOR CB CLOSURE

Logical checking of the outputs from the CB closure monitors is performed to generate signals to indicate that it is OK to close circuit breakers.

Signals are provided to indicate that manual CB closure conditions are OK (***CB Man SCOK***), as are signals to indicate that automatic CB closure conditions are OK (***CB SCOK*** and ***CB Fast SCOK***). The ***CB Fast SCOK*** signal allows CB autoreclosure without waiting for the Dead Time to expire.

For single-phase Autoreclose no voltage or synchronism check is required as synchronising power is flowing in the two healthy phases. Three-phase Autoreclose can be performed without checking that voltages are in synchronism for the first shot (and only the first shot). The settings to permit Autoreclose without checking voltage synchronism on the first shot are:

- ***CB1L SC Shot 1*** for circuit breaker 1 as a leader,
- ***CB1F SC Shot 1*** for circuit breaker 1 as a follower,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a leader,
- ***CB2L SC Shot 1*** for circuit breaker 2 as a follower.

When the circuit breaker has closed, the Autoreclose function asserts a DDB signal ***Set CB1 Close***, which indicates that an attempt has been made to close the circuit breaker. At this point, the Reclaim Time starts. If the circuit breaker remains closed after the reclaim timer expires, the Autoreclose cycle is complete, and signals are generated to indicate that Autoreclose was successful. These are:

- ***CB1 Succ 1P AR*** (Single-phase Autoreclose CB1)
- ***CB2 Succ 1P AR*** (Single-phase Autoreclose CB2)
- ***CB1 Succ 3P AR*** (Three-phase Autoreclose CB1)
- ***CB2 Succ 3P AR*** (Three-phase Autoreclose CB2)

These signals increment the relevant circuit breaker successful Autoreclose shot counters, as well as resetting the Autoreclose in progress signal.

The relevant circuit breaker successful Autoreclose shot counters are:

- ***CB1 SUCC SPAR*** (Single-phase Autoreclose CB1)
- CB1 SUCC 3PAR Shot1 (Three-phase Autoreclose CB1, Shot 1)
- CB1 SUCC 3PAR Shot2 (Three-phase Autoreclose CB1, Shot 2)
- CB1 SUCC 3PAR Shot3 (Three-phase Autoreclose CB1, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB1, Shot 4)
- ***CB2 SUCC SPAR*** (Single-phase Autoreclose CB2)
- CB2 SUCC 3PAR Shot1 (Three-phase Autoreclose CB2, Shot 1)
- CB2 SUCC 3PAR Shot2 (Three-phase Autoreclose CB2, Shot 2)
- CB2 SUCC 3PAR Shot3 (Three-phase Autoreclose CB2, Shot 3)
- CB1 SUCC 3PAR Shot4 (Three-phase Autoreclose CB2, Shot 4)

12.5.24.1 THREE-PHASE AUTORECLOSE LEADER CHECK LOGIC DIAGRAM

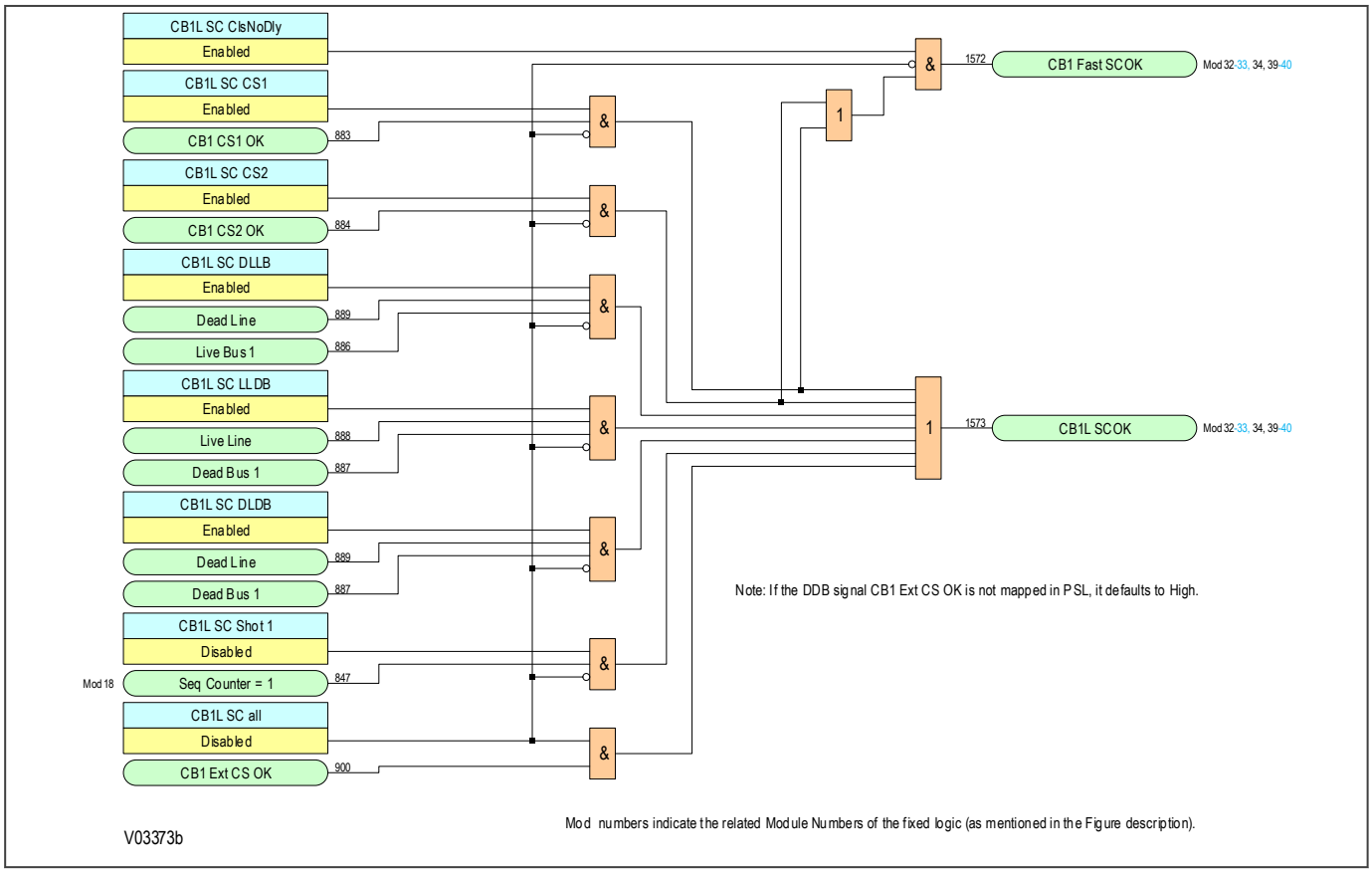


Figure 288: Three-phase AR system check logic for CB1 as leader (module 45)

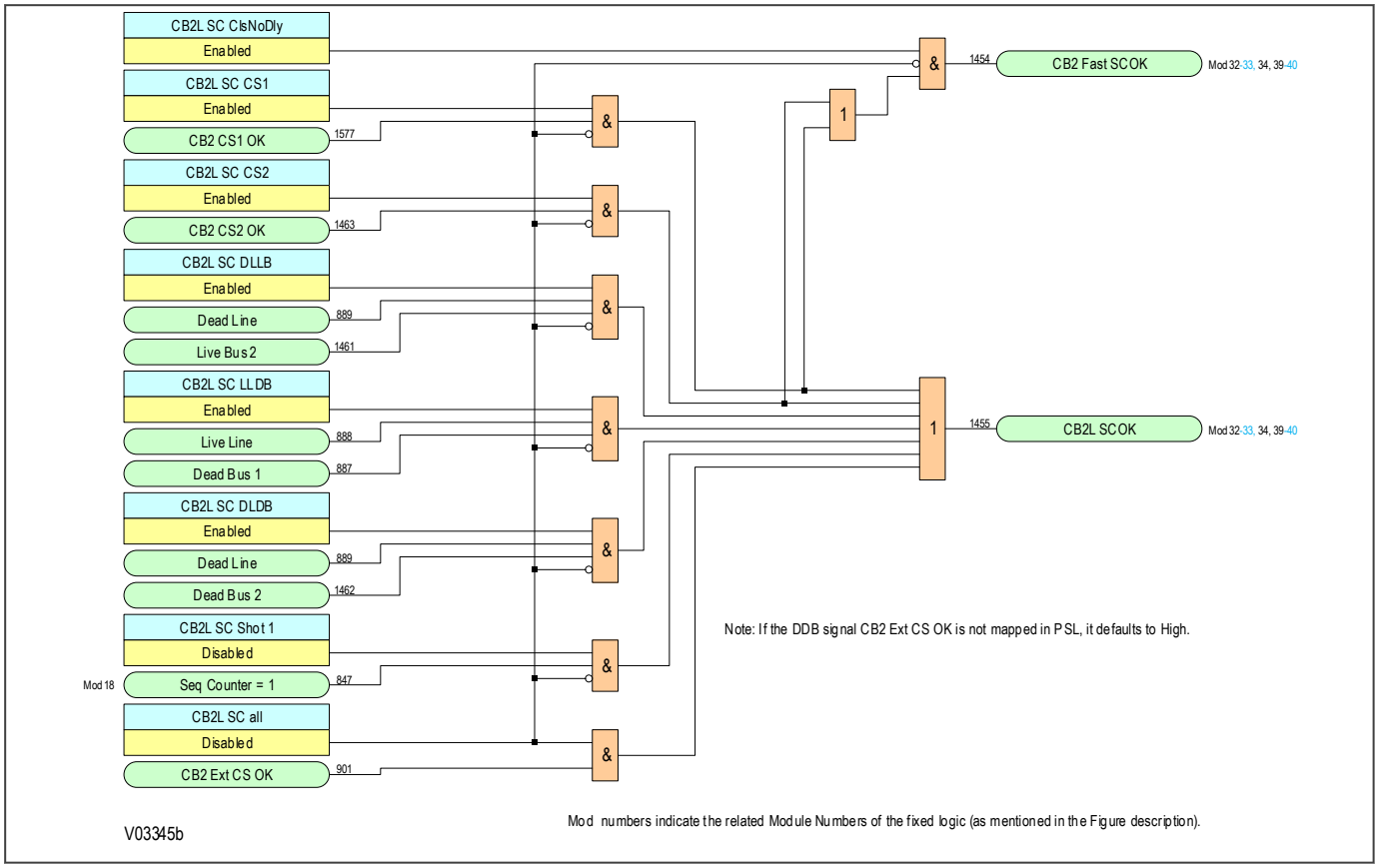


Figure 289: Three-phase AR system check logic for CB2 as leader (module 46)

12.5.24.2 THREE-PHASE AUTORECLOSE FOLLOWER CHECK LOGIC DIAGRAM

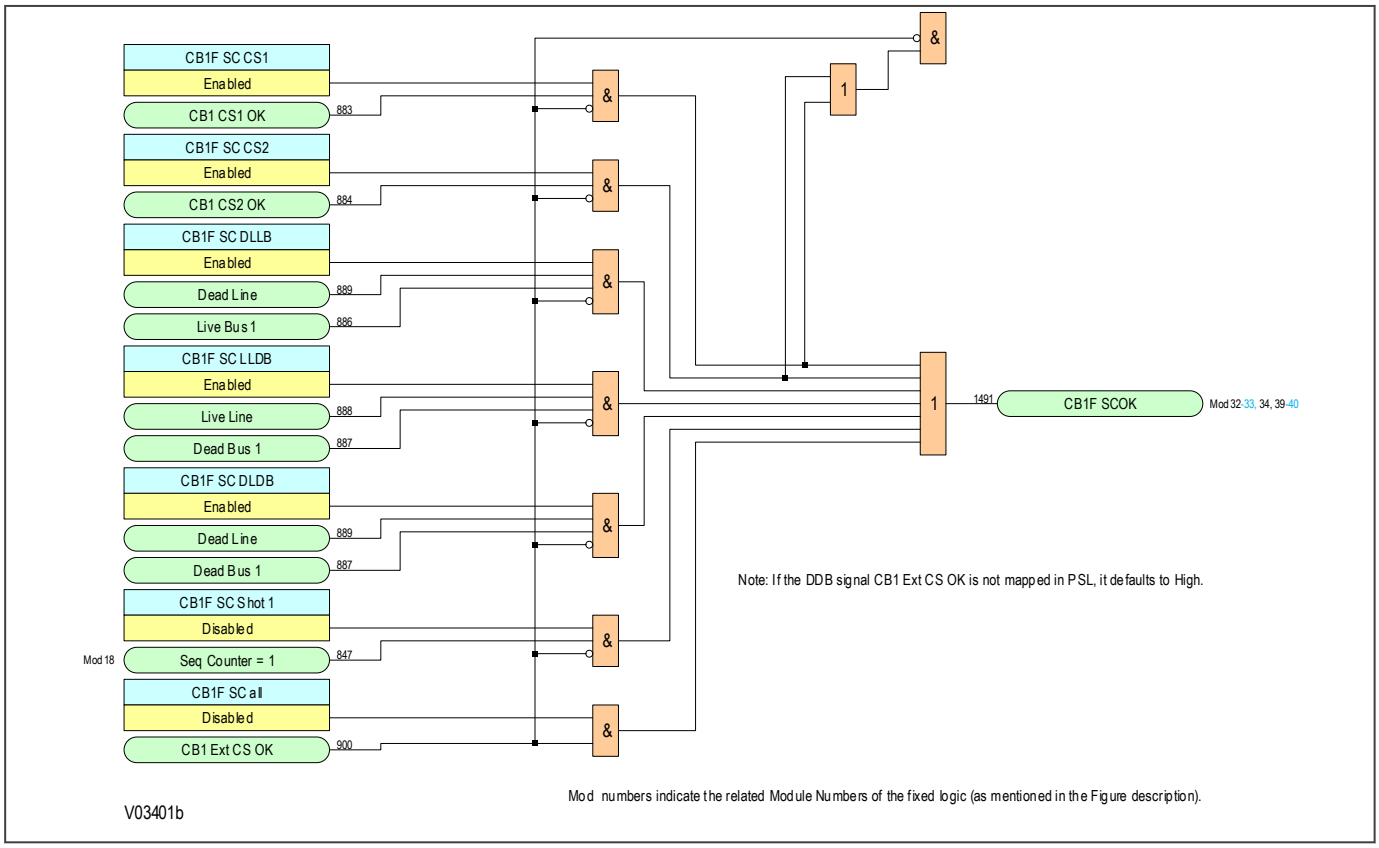


Figure 290: Three-phase AR system check logic for CB1 as follower (module 47)

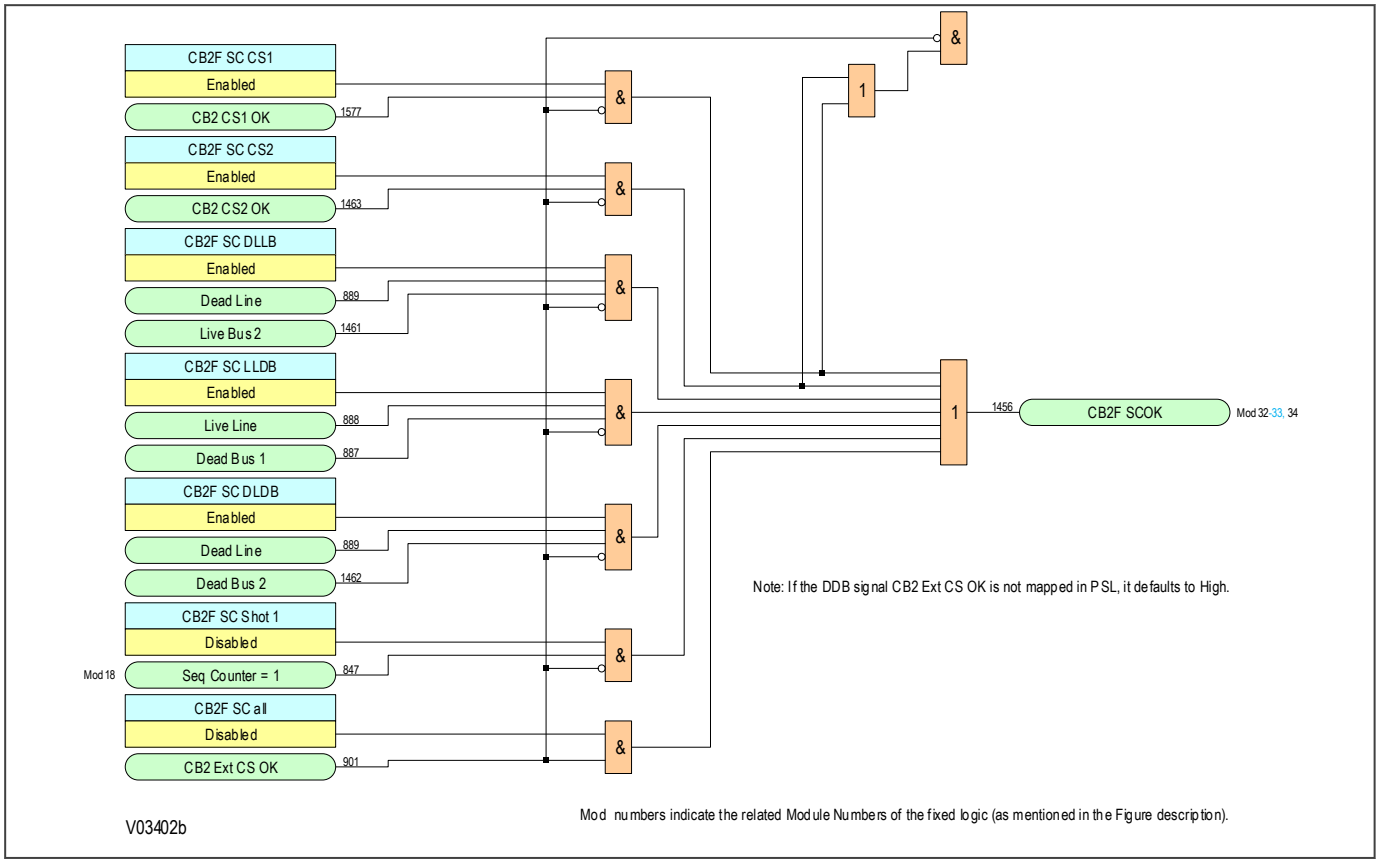
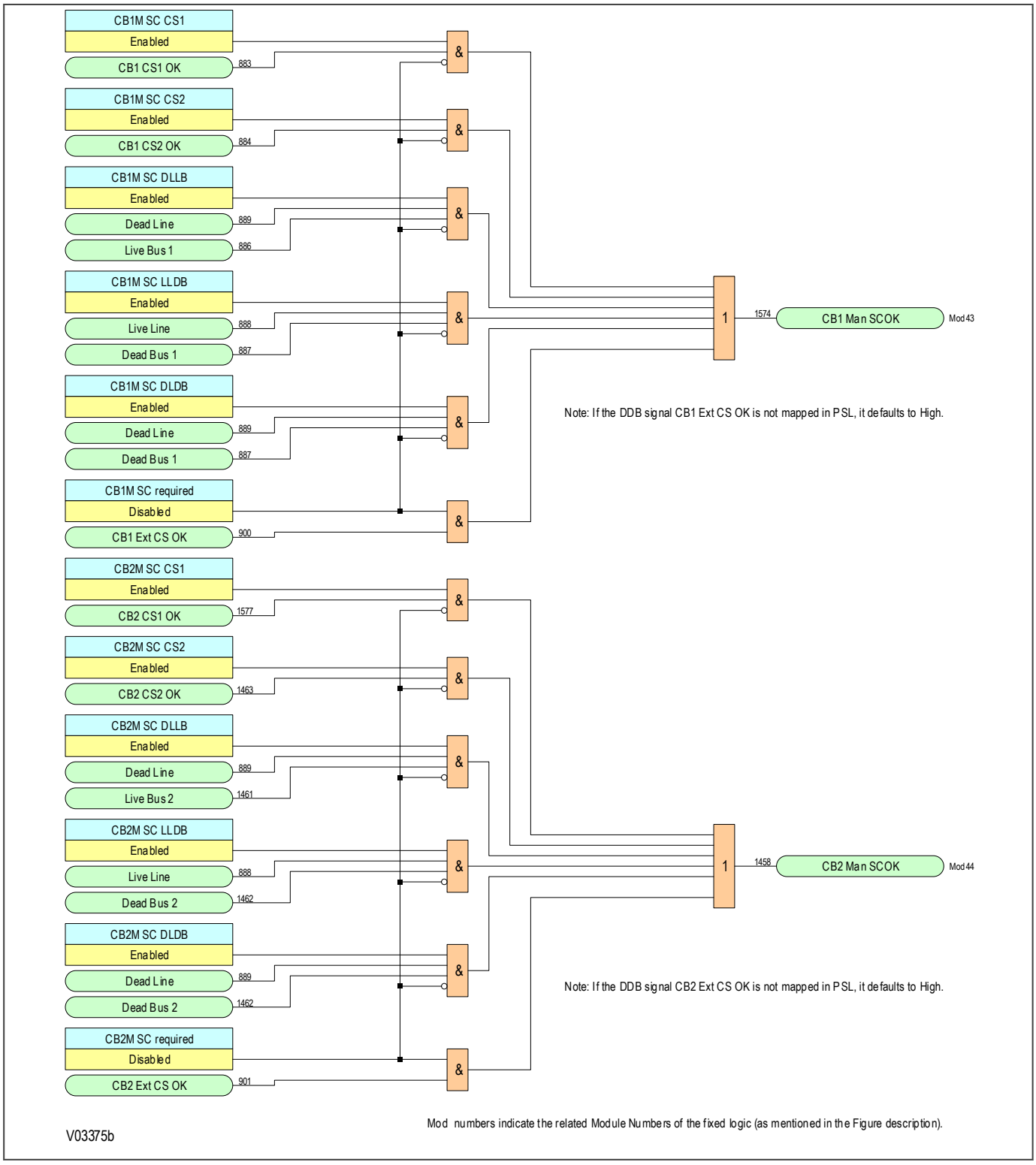


Figure 291: Three-phase AR system check logic for CB2 as follower (module 48)

12.5.24.3 CB MANUAL CLOSE SYSTEM CHECK LOGIC DIAGRAM



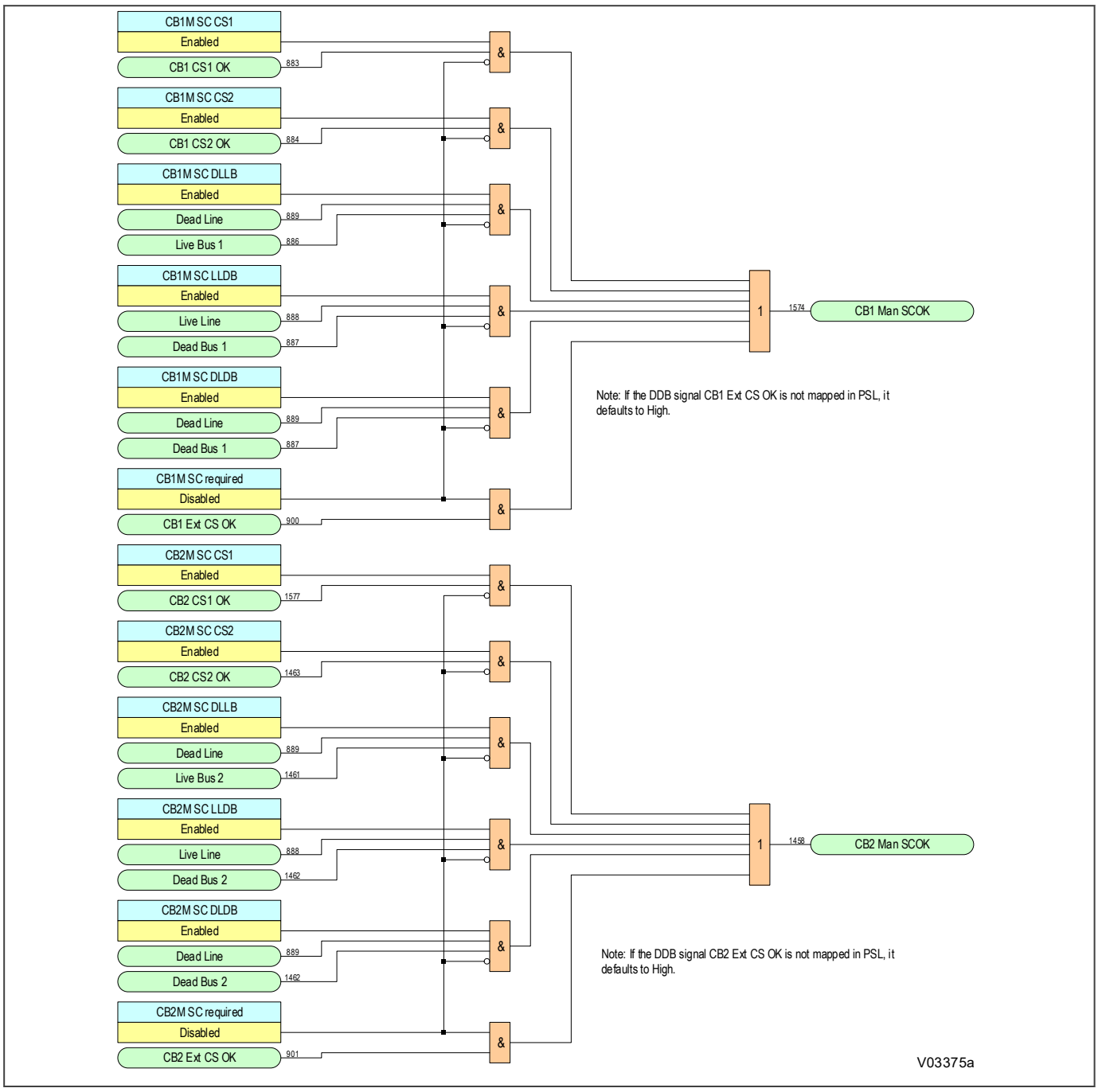


Figure 292: CB manual close system check logic (modules 51 & 52)

12.6 SETTING GUIDELINES

12.6.1 DE-IONISING TIME GUIDANCE

The de-ionisation time of a fault arc depends on several factors such as circuit voltage, conductor spacing, fault current and duration, atmospheric conditions, wind speed and capacitive coupling from adjacent conductors. For this reason it is difficult to estimate the de-ionisation time. Circuit voltage is, generally the most significant factor and experience tells us that typical minimum de-ionising times for a three-phase fault are as follows:

- 66 kV: 100 ms
- 110 kV: 150 ms
- 132 kV: 170 ms
- 220 kV: 280 ms
- 275 kV: 300 ms
- 400 kV: 500 ms

Where single-pole high speed Autoreclose is used, the capacitive current induced between the healthy phases and the faulty phase tends to maintain the arc. This significantly increases the de-ionisation time and hence required dead time.

Single-pole Autoreclose is generally only used at transmission voltages. A typical de-ionisation time at 220 kV may be as high as 560 ms.

12.6.2 DEAD TIMER SETTING GUIDELINES

High speed Autoreclose may need to maintain stability on a network with two or more power sources. For high speed Autoreclose the system disturbance time should be minimised by using fast protection (typically <30 ms) and fast circuit breakers (typically <60 ms). For stability between two sources a system dead time of ≤300 ms may typically be required.

The minimum system dead time (considering just the circuit breaker) is the trip mechanism reset time plus the circuit breaker closing time.

The Autoreclose minimum dead time settings are governed primarily by two factors:

- Time taken for de-ionisation of the fault path
- Circuit breaker characteristics

It is essential that the protection fully resets during the dead time, so that correct time discrimination will be maintained after Autoreclose onto a fault. For high speed Autoreclose instantaneous reset of protection is required.

For highly interconnected systems synchronism is unlikely to be lost by the tripping out of a single line. Here the best policy may be to adopt longer dead times, to allow time for power swings resulting from the fault to settle.

The dead time is normally a fixed time delay but can be can set to adaptive for single-pole autoreclose schemes where it is dependent on the arc extinction time for a transient single-phase fault.

The autoreclose scheme is adaptive when the ***Adaptive SP AR*** setting is `Enabled`. The adaptive autoreclose is only available for single-pole autoreclose applications. The ***SP Min Dead Time*** (0-10s) is the minimum dead time for a single-pole autoreclose. The actual dead time is set to the SP minimum dead time or the time for the secondary arc to extinguish if it is within maximum dead time, whichever is greater. The ***SP Max Dead Time*** (0-10s) is the maximum dead time for single-pole autoreclose. If the secondary arc does not extinguish or it is detected as a permanent fault within the SP maximum dead time, the autoreclose will issue a three-phase trip command and lock out. If a transient fault is detected within the SP maximum dead time, the autoreclose logic will issue a close command to close the open pole. When the AAR dead time exceeds the SP Max Dead Time or there is no output from the AAR logic within the ***SP Max Dead Time***, the output of the autoreclose logic will either reclose or go to A/R lockout based on selection of the ***SP Max Dead Time Elapsed*** – `Reclose`/`Lockout` setting.

12.6.2.1 EXAMPLE DEAD TIME CALCULATION

The following circuit breaker and system characteristics can be used for the minimum dead time calculation:

- a) Circuit breaker Operating time (Trip coil energised to Arc interruption): 50 ms
- b) Circuit breaker Opening + Reset time (Trip coil energised to trip mechanism reset): 200 ms
- c) Protection reset time: < 80 ms
- d) Circuit breaker Closing time (Close command to Contacts make): 85 ms
- e) De-ionisation time (280 ms for 3-phase, or 560 ms for 1-phase)

Three-phase de-ionisation time for 220 kV line is typically 280 ms.

The minimum Autoreclose dead time setting is therefore the greater of:

(a) + (c) = 50 ms + 80 ms = 130 ms, to allow protection reset

(a) + (e) - (d) = 50 ms + 280 ms - 85 ms = 245 ms, to allow de-ionising

In practice a few additional cycles would be added to allow for tolerances, so Dead Time 1 could be set to 300 ms or greater. The overall system dead time is found by adding (d) to the chosen settings then subtracting (a). This gives 335 ms.

A typical de-ionising time value for single-phase trip on a 220 kV line is 560 ms, so the 1 Pole Dead Time could be chosen as 600 ms or greater. The overall system dead time is found by adding (d) to the chosen settings then subtracting (a). This gives 635 ms.

12.6.3 RECLAIM TIME SETTING GUIDELINES

Several factors influence the choice of the reclaim timer, such as:

- Fault incidence/Past experience: Small reclaim times may be required where there is a high incidence of recurrent lightning strikes to prevent unnecessary lockout for transient faults.
- Spring charging time: For high speed Autoreclose the reclaim time may be set longer than the spring charging time. A minimum reclaim time of more than 5s may be needed to allow the circuit breaker time to recover after a trip and close before it can perform another trip-close-trip cycle. This time will depend on the duty (rating) of the circuit breaker. For delayed Autoreclose this may not be needed as the dead time can be extended by an extra circuit breaker healthy check/Autoreclose Inhibit Time window time if there is insufficient energy in the circuit breaker.
- Switchgear Maintenance: Excessive operation resulting from short reclaim times can mean shorter maintenance intervals.

When used in conjunction with distance protection, the Reclaim Time setting is generally set greater than the zone 2 delay.

12.6.4 AUTORECLOSE SHOT COUNTERS

In dual circuit breaker applications, the two circuit breakers are normally arranged to reclose sequentially with one designated the Leader circuit breaker reclosing after a set dead time. If the Leader circuit breaker remains closed after the dead time, the second circuit breaker referred to as the Follower recloses after a further delay, the Follower Time.

The Follower Time is provided to prevent un-necessary operation of the Follower circuit breaker. The Follower Time should be set sufficiently long as to avoid an un-necessary closure of the Follower circuit breaker where conditions are such that it would be required to trip again.

After expiry of the dead time, the Leader circuit breaker will attempt Autoreclose. The minimum value of the Follower time should allow sufficient time for the Autoreclose of the Leader circuit breaker to be considered successful.

An extreme case may be where instantaneous protection is only provided by distance elements and where Autoreclose is onto a dead line with a persistent fault at the remote end of the line.

Local end protection (Time delayed Back up protection, like distance Z2 element) may detect this fault after a time delay (typically > 200 ms). In addition to the delays associated with the back-up protection (typically >200 ms), time must be allowed for the Leader circuit breaker to re-trip (50 - 100 ms), and a safety margin needs to be added so that a minimum Follower time could be around 500 ms.

If the Autoreclose of the Leader circuit breaker is successful, the Follower circuit breaker can be allowed to Autoreclose. Delaying the Autoreclose of the Follower circuit breaker will allow any transients to decay before the switching. If the transient decay figure is known, it can be used to determine a minimum Follower Time value. The larger of the two values can then be used as the minimum Follower Time.

Note:
The Follower circuit breaker should only be reclosed if the system is healthy. In a dual circuit breaker scheme where the system is healthy, the Follower circuit breaker acts more like a bus coupler. In this case there is no need for fast switching and a time delay in excess of 1s is often appropriate. The default Follower time in this product is chosen as 5 s and this can comfortably be applied to most applications.

CHAPTER 13

CB FAIL PROTECTION

13.1 CHAPTER OVERVIEW

The device provides a Circuit Breaker Fail Protection function. This chapter describes the operation of this function including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 439
Circuit Breaker Fail Protection 440
Circuit Breaker Fail Implementation 441
Circuit Breaker Fail Logic 443
Application Notes 449

13.2 CIRCUIT BREAKER FAIL PROTECTION

When a fault occurs, one or more protection devices will operate and issue a trip command to the relevant circuit breakers. Operation of the circuit breaker is essential to isolate the fault and prevent, or at least limit, damage to the power system. For transmission and sub-transmission systems, slow fault clearance can also threaten system stability.

For these reasons, it is common practice to install Circuit Breaker Failure protection (CBF). CBF protection monitors the circuit breaker and establishes whether it has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, the CBF protection will operate, whereby the upstream circuit breakers are back-tripped to ensure that the fault is isolated.

CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

13.3 CIRCUIT BREAKER FAIL IMPLEMENTATION

Circuit Breaker Failure Protection is implemented in the *CB FAIL & P.DEAD* column of the relevant settings group. Independent CB Fail settings are provided for CB1 and CB2 in dual CB versions.

13.3.1 CIRCUIT BREAKER FAIL TIMERS

The circuit breaker failure protection incorporates two timers, ***CB Fail 1 Timer*** and ***CB Fail 2 Timer***, allowing configuration for the following scenarios:

- Simple CBF, where only ***CB Fail 1 Timer*** is enabled. For any protection trip, the **CB Fail 1** ***Timer*** is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, the CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to back-trip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A retripping scheme, plus delayed back-tripping. Here, ***CB Fail 1 Timer*** is used to issue a trip command to a second trip circuit of the same circuit breaker. This requires the circuit breaker to have duplicate circuit breaker trip coils. This mechanism is known as retripping. If retripping fails to open the circuit breaker, a back-trip may be issued following an additional time delay. The back-trip uses ***CB Fail 2 Timer***, which was also started at the instant of the initial protection element trip.

You can configure the CBF elements ***CB Fail 1 Timer*** and ***CBF Fail 2 Timer*** to operate for trips triggered by protection elements within the device. Alternatively you can use an external protection trip by allocating one of the opto-inputs to the ***External Trip*** DDB signal in the PSL.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***NonIProt Rst*** and ***Ext Prot Rst***.

The resetting options are summarised in the following table:

Initiation (Menu Selectable)	CB Fail Timer Reset Mechanism
Current based protection (e.g.50/51/46/21/87)	IA< operates AND IB< operates AND IC< operates AND IN< operates or through Ext Rst DDB in PSL
Sensitive Earth Fault element	ISEF< Operates or Ext Rst SEF DDB
Non-current based protection (e.g. 27/59/81/32L)	Five options are available: - All I< and IN< elements operate or Ext Rst CBF DDB - Protection element reset AND (all I< and IN< elements operate or Ext Rst DDB - CB open (all 3 poles) AND all I< and IN< elements operate
External protection	Five options are available. - All I< and IN< elements operate - External trip reset AND all I< and IN< elements operate - CB open (all 3 poles) AND all I< and IN< elements operate - Prot Reset OR I<: External trip reset OR all I< and IN< elements operate - Rst or CBOp & I<: External trip reset OR Pole Dead AND all I< and IN< elements operate

13.3.2 CIRCUIT BREAKER FAIL INITIATION

If ***ExtTrip Only Ini*** setting is `Disabled`, the CBF protection can be initiated when any internal protection function issues a trip or if an external protection trip occurs. If ***ExtTrip Only Ini*** setting is `Enabled`, then only external protection is allowed to initiate the CBF function. An external protection and internal current-based protections (except SEF protection) initiate the CB Fail function on per-phase basis, while non-current-based protections and SEF initiate CB Fail for all three phases simultaneously.

13.3.3 ZERO CROSSING DETECTION

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is to its saturation point, the higher the subsidence current.

The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the protection clears the fault, the CB Fail function should reset fast to avoid maloperation due to the subsidence current. To compensate for this the device includes a zero-crossing detection algorithm, which ensures that the CB Fail re-trip and back-trip signals are not asserted while subsidence current is flowing. If all the samples within half a cycle are greater than or smaller than 0 A (10 mS for a 50 Hz system), then zero crossing detection is asserted, thereby blocking the operation of the CB Fail function. The zero-crossing detection algorithm is used after the circuit breaker in the primary system has opened ensuring that the only current flowing in the AC secondary circuit is the subsidence current.

13.4 CIRCUIT BREAKER FAIL LOGIC

13.4.1 CIRCUIT BREAKER FAIL LOGIC - PART 1

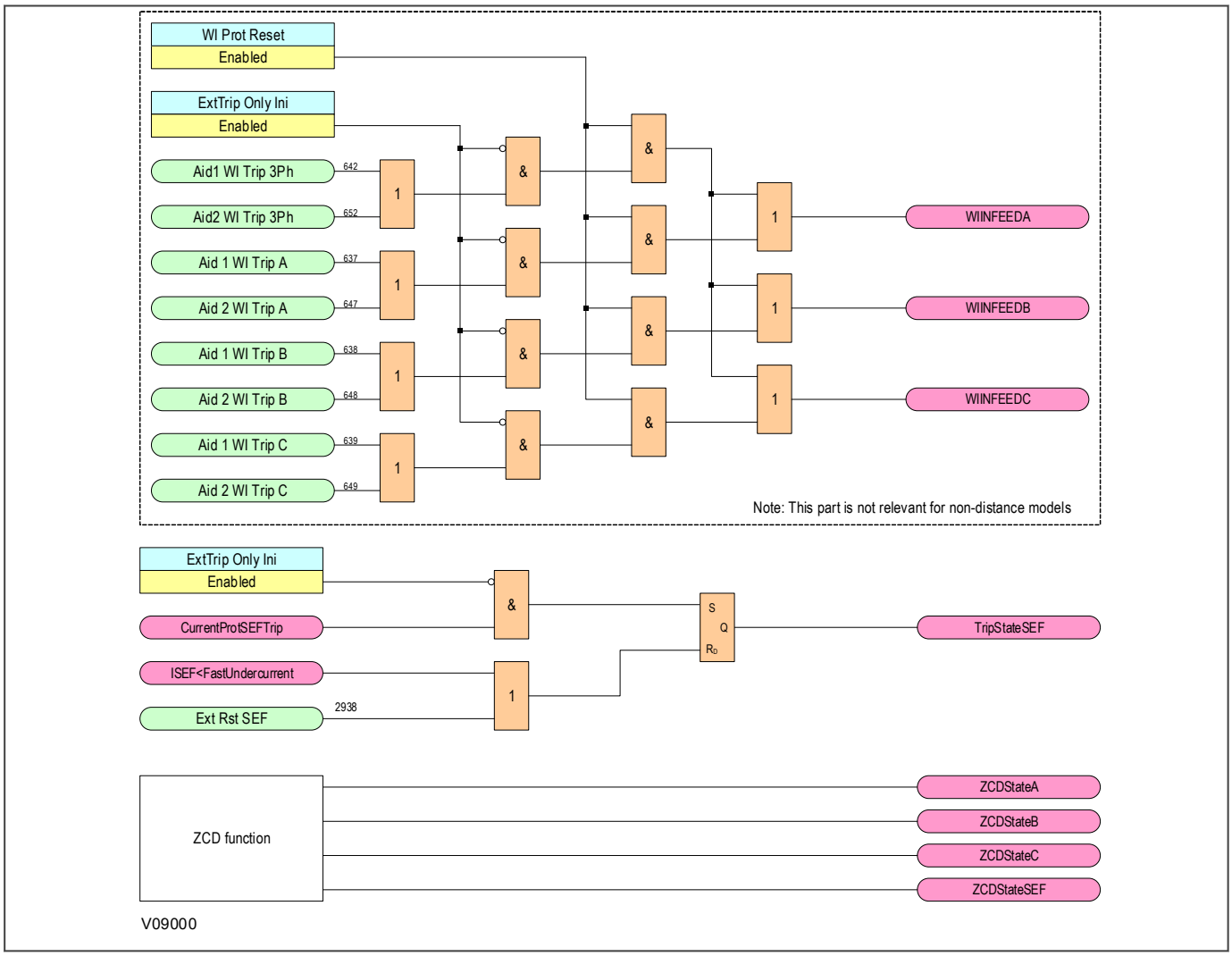


Figure 293: Circuit breaker fail logic - part 1

13.4.2 CIRCUIT BREAKER FAIL LOGIC - PART 2

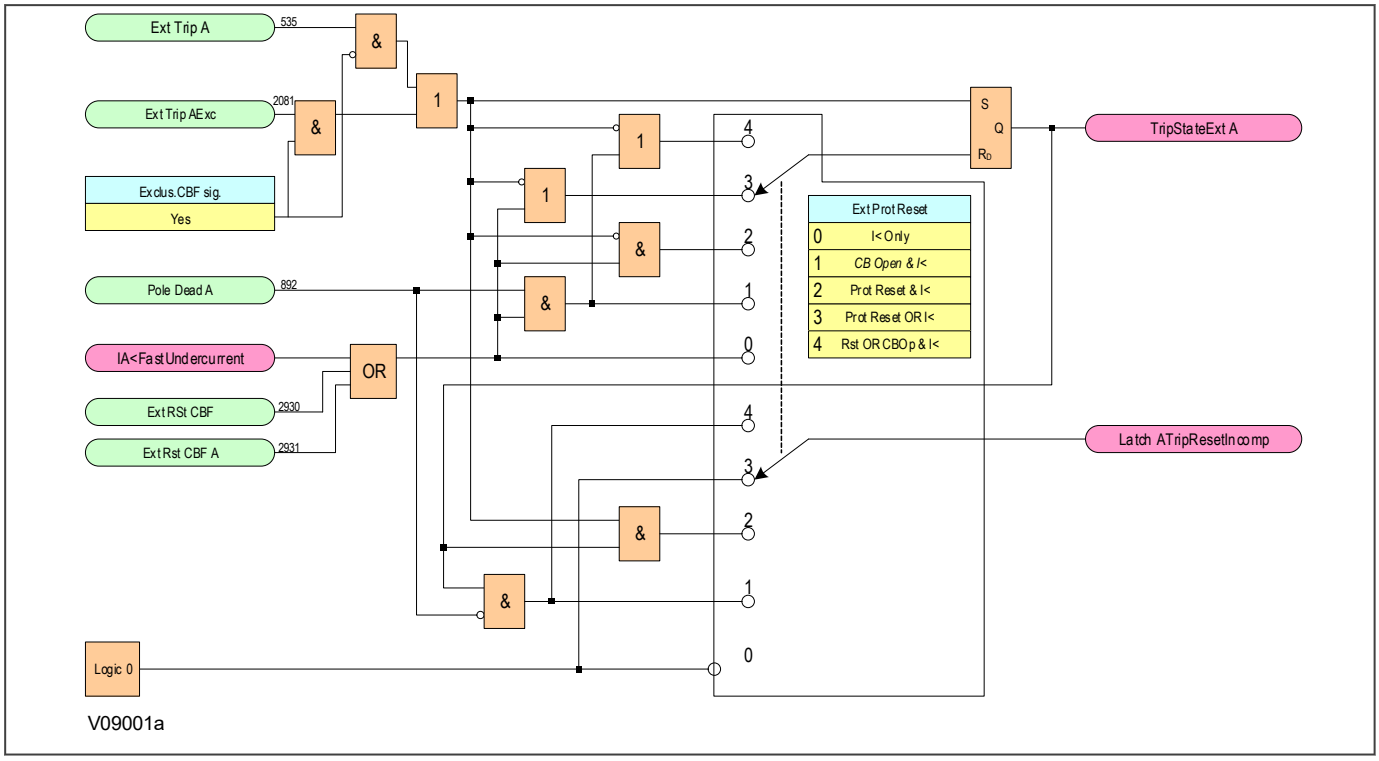


Figure 294: Circuit breaker fail logic - part 2

13.4.3 CIRCUIT BREAKER FAIL LOGIC - PART 2

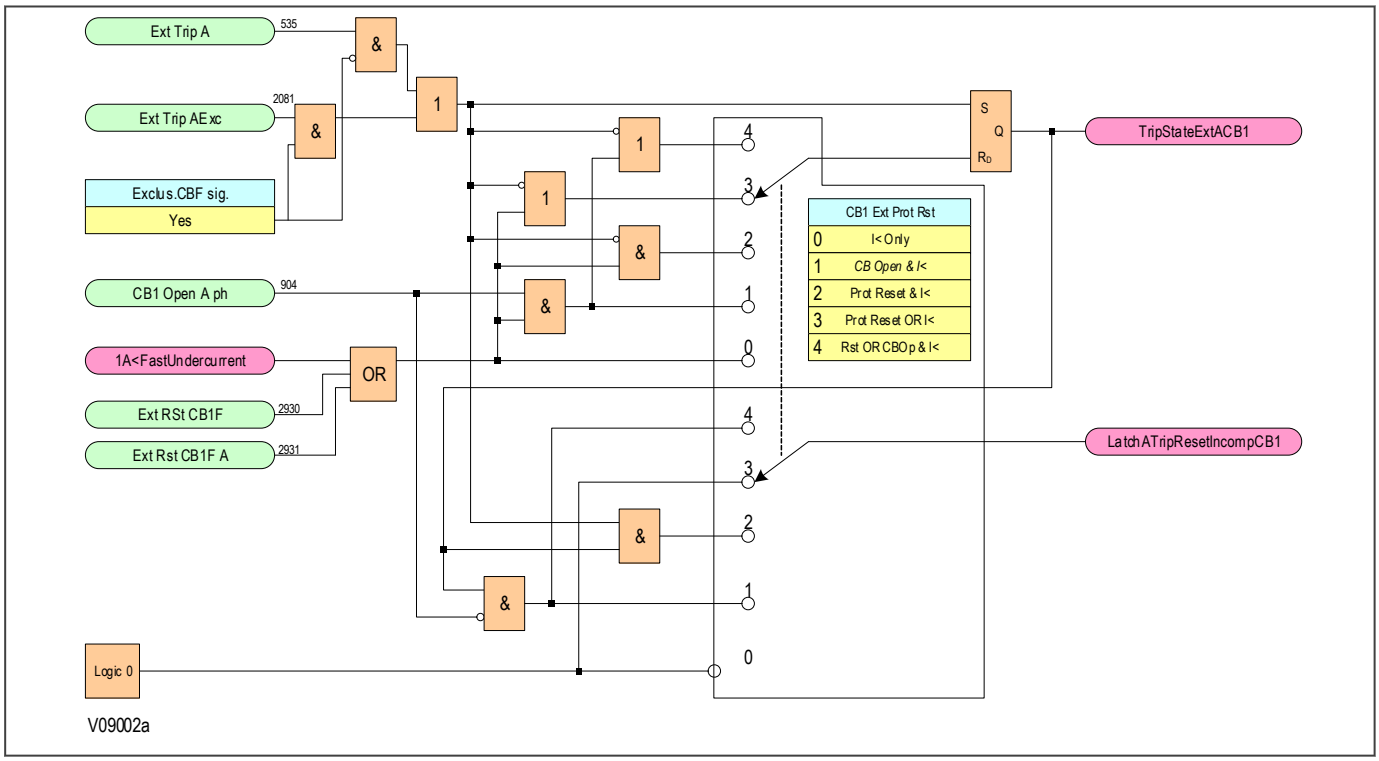


Figure 295: Circuit breaker fail logic - part 2

13.4.4 CIRCUIT BREAKER FAIL LOGIC - PART 3

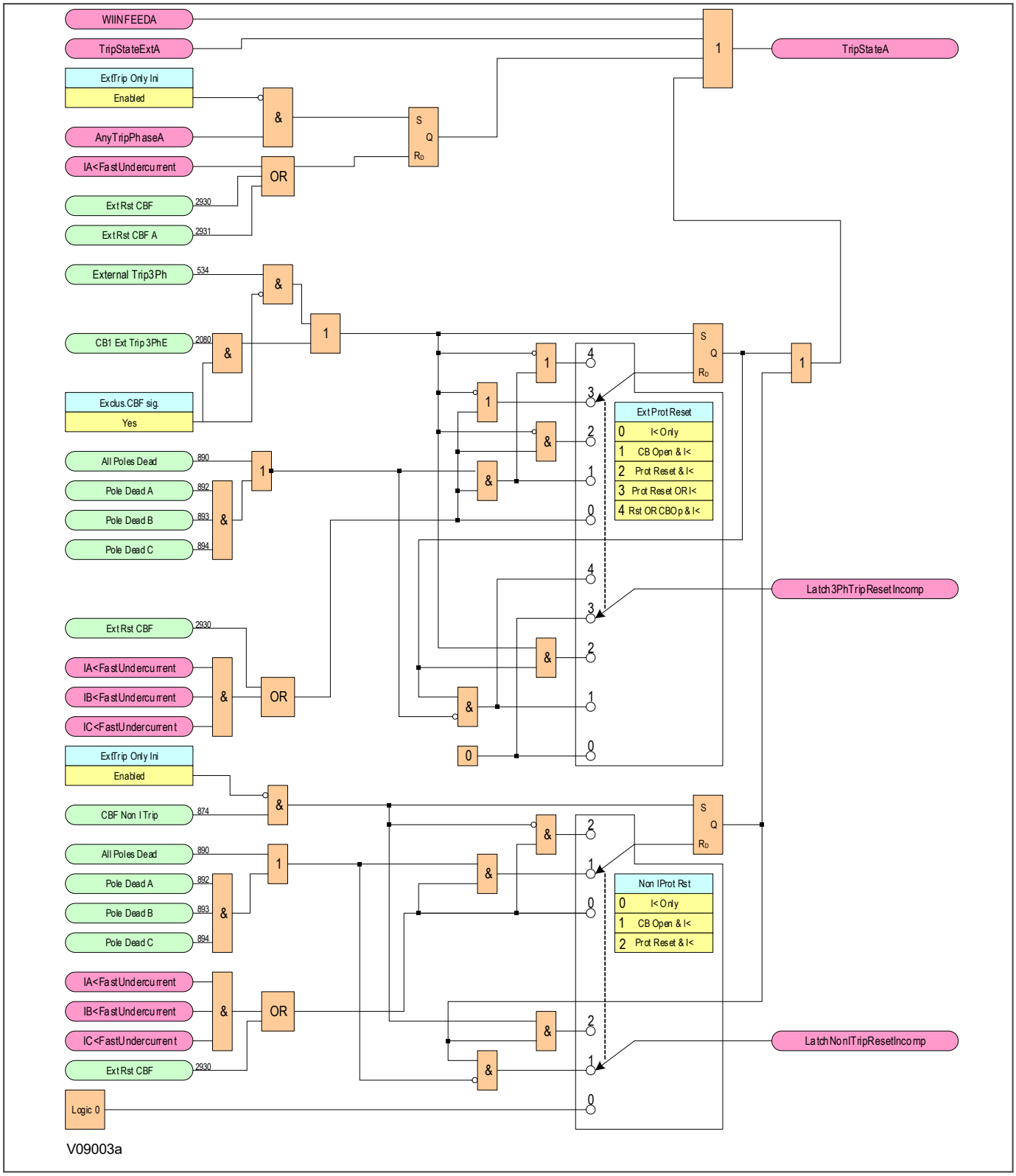


Figure 296: Circuit breaker fail logic - part 3

13.4.5 CIRCUIT BREAKER FAIL LOGIC - PART 3

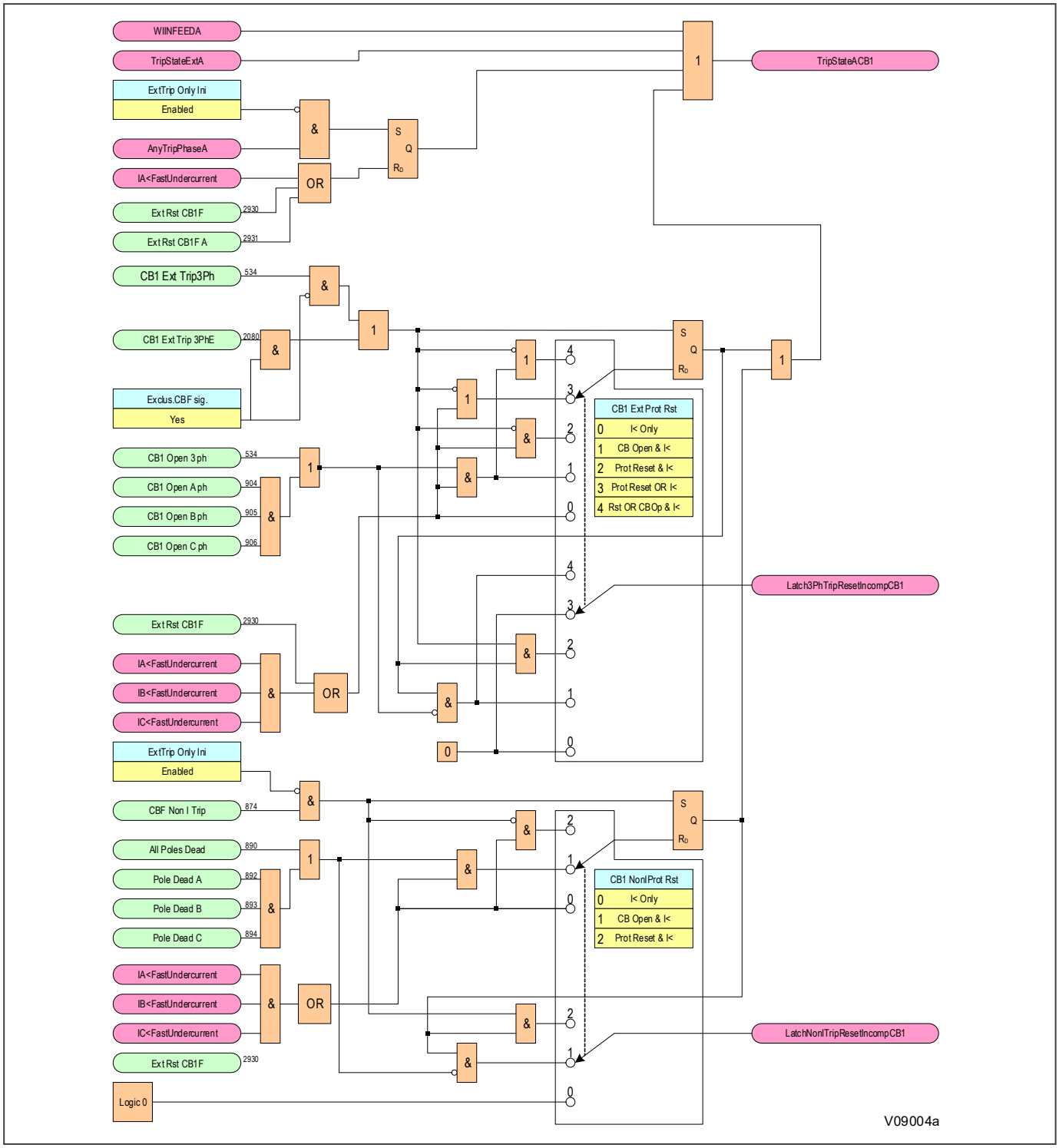


Figure 297: Circuit breaker fail logic - part 3

13.4.6 CIRCUIT BREAKER FAIL LOGIC - PART 4

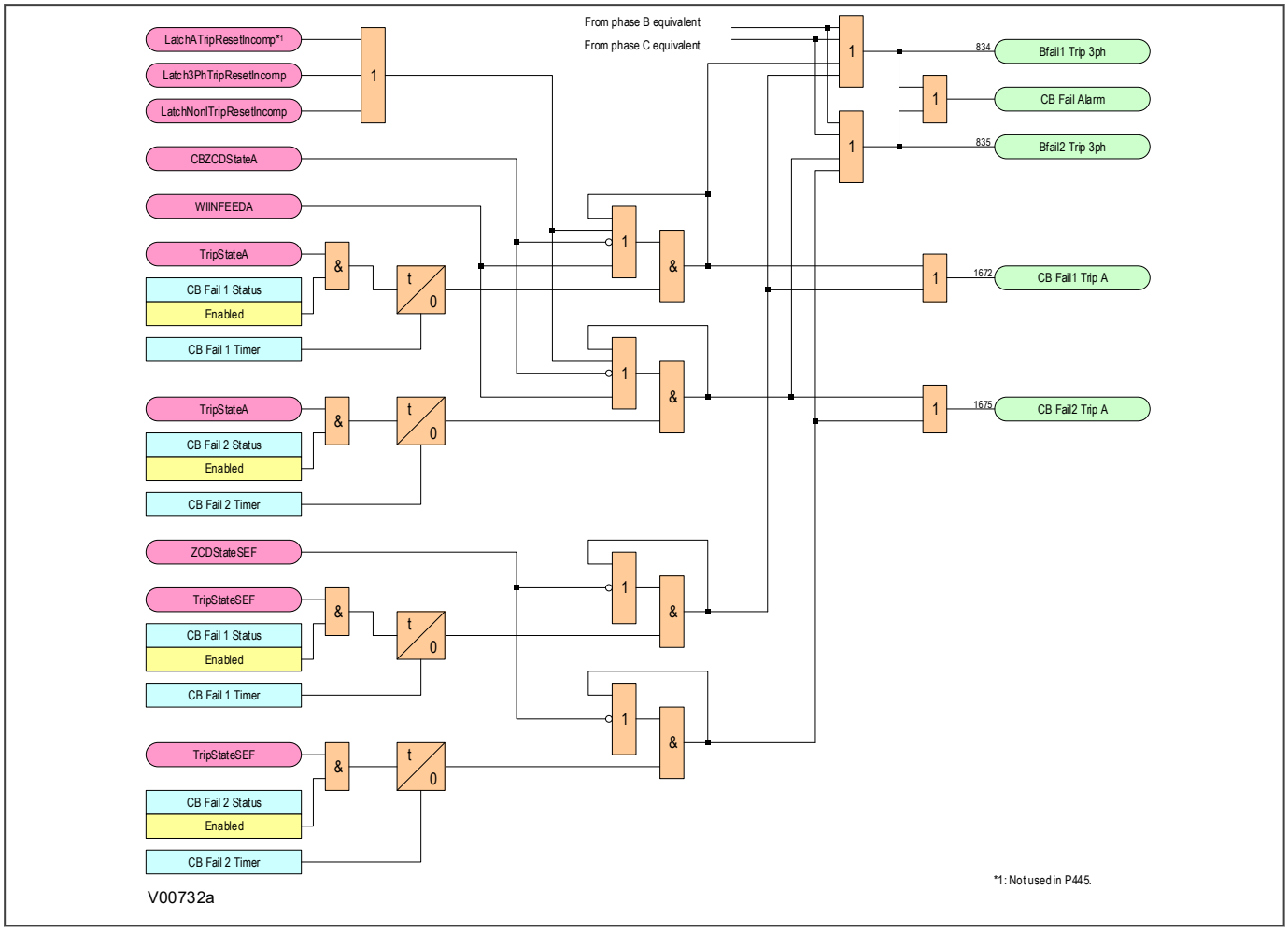


Figure 298: Circuit breaker fail logic - part 4

Note:
This diagram shows only phase-A for a single-CB device. The diagrams for phases B and C follow the same principle and are not repeated here.

13.4.7 CIRCUIT BREAKER FAIL LOGIC - PART 4

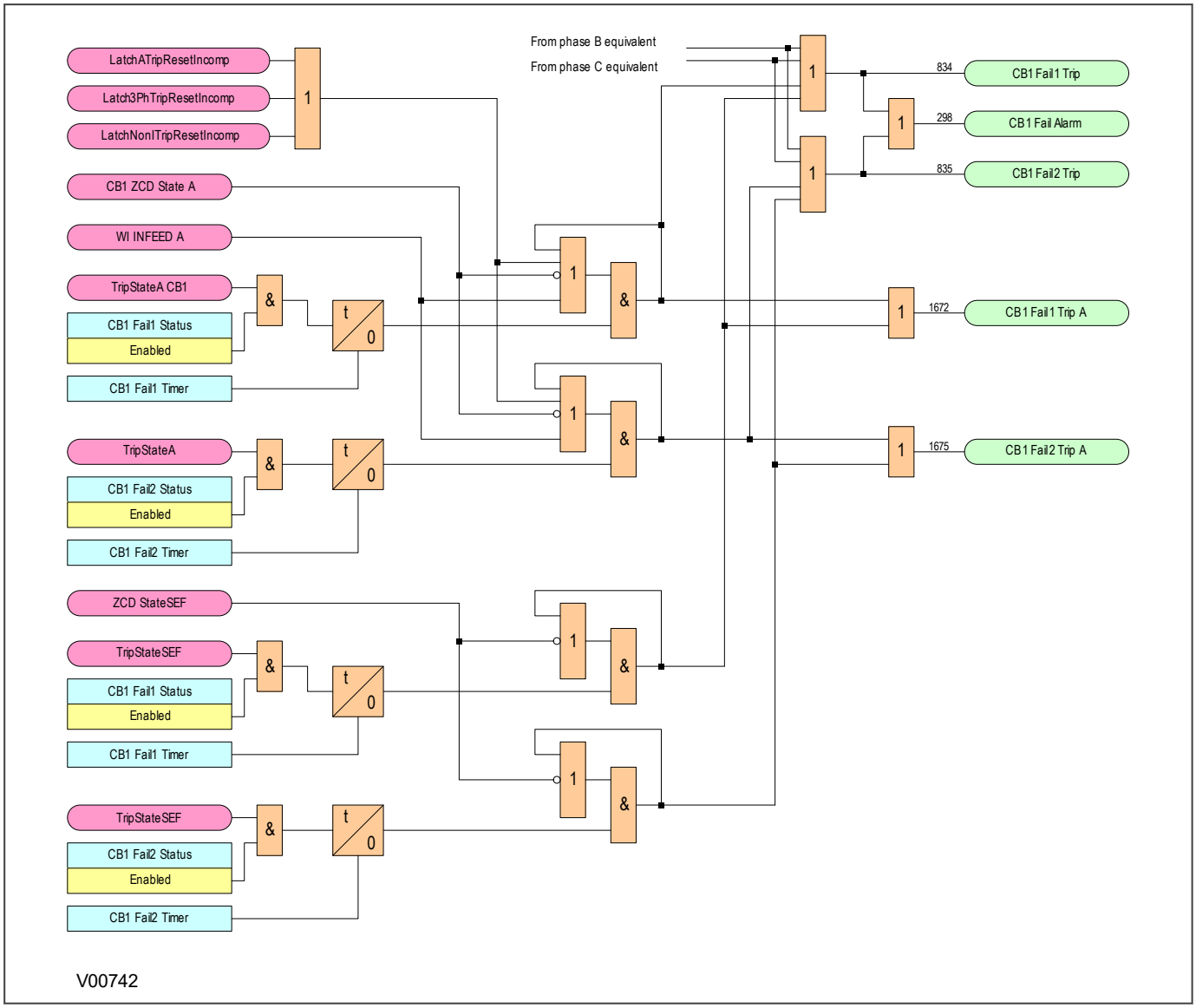


Figure 299: Circuit breaker fail logic - part 4

Note:
This diagram shows only phase-A for the first CB (CB1) of a dual-CB device. The diagrams for phases B and C and for the second CB (CB2) follow the same principle and are not repeated here.

13.5 APPLICATION NOTES

13.5.1 RESET MECHANISMS FOR CB FAIL TIMERS

It is common practise to use low set undercurrent elements to indicate that circuit breaker poles have interrupted the fault or load current. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the device uses operation of undercurrent elements to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting CBF in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. In this case, detecting drop-off of the initiating protection element might be a more reliable method.
- Where distance schemes include Weak Infeed trip logic. The reset of the Weak infeed trip condition should be used in addition to the undercurrent check. ***WI Prot Reset*** should be set to `enabled`.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***Non I Prot Reset*** and ***Ext Prot Reset***.

If the CBF protection is initiated by an external protection trip, then two resetting options ***Prot Reset OR I<*** and ***Rst or CBOp & I<*** are provided. These settings don't necessarily require undercurrent element (I<) operation, as shown in the table below. These options are useful if re-tripping is not implemented, as they allow avoiding back-tripping due to spurious short-time energisation of External Trip opto-inputs.



Warning:
If you are using *Prot Reset OR I<* or *Rst or CBOp & I<*, do not connect the *External Trip* inputs to the Trip Conversion logic inputs in the PSL.

13.5.2 SETTING GUIDELINES (CB FAIL TIMER)

The following timing chart shows the CB Fail timing during normal and CB Fail operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CB Fail back-up trip time delay considers the maximum CB clearing time, the CB Fail reset time plus a safety margin. Typical CB clearing times are 1.5 or 3 cycles. The CB Fail reset time should be short enough to avoid CB Fail back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CB Fail to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit.

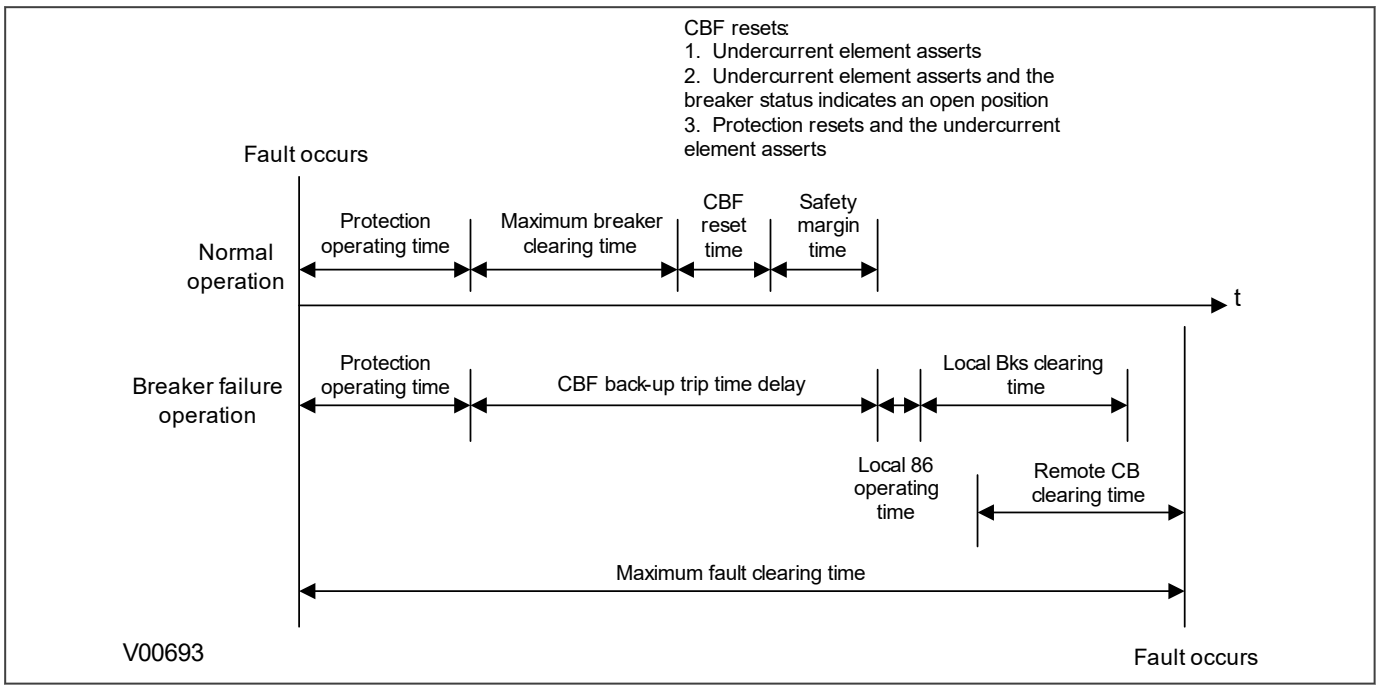


Figure 300: CB fail timing

The following examples consider direct tripping of a 2-cycle circuit breaker. Typical timer settings to use are as follows:

CB Fail Reset Mechanism	tBF Time Delay	Typical Delay For 2 Cycle Circuit Breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Note:
All CB Fail resetting involves the operation of the undercurrent elements. Where element resetting or CB open resetting is used, the undercurrent time setting should still be used if this proves to be the worst case.
Where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.

13.5.3 SETTING GUIDELINES (UNDERCURRENT)

The phase undercurrent settings (I<) must be set less than load current to ensure that I< operation correctly indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20%In. Settings of 5% of In are common for generator CB Fail.

The earth fault undercurrent elements must be set less than the respective trip. For example:

$$IN< = (IN> trip)/2$$

CHAPTER 14

CURRENT PROTECTION FUNCTIONS

14.1 CHAPTER OVERVIEW

The primary purpose of this product is not overcurrent protection. It does however provide a range of current protection functions to be used as backup protection. This chapter assumes you are familiar with overcurrent protection principles and does not provide detailed information here. If you require further information about general overcurrent protection principles, please refer either to GE Vernova's publication, Protection and Automation Application Guide, earlier incarnations of this technical manual, or one of our technical manuals from our P40 Agile Modular distribution range of products such as the P14.

This chapter contains the following sections:

Chapter Overview 452

Phase Fault Overcurrent Protection 453

Negative Sequence Overcurrent Protection 463

Earth Fault Protection 466

Sensitive Earth Fault Protection 471

High Impedance REF 476

Thermal Overload Protection 478

Broken Conductor Protection 482

Transient Earth Fault Detection 484

14.2 PHASE FAULT OVERCURRENT PROTECTION

Phase fault overcurrent protection is provided as a form of back-up protection that could be:

- Permanently disabled
- Permanently enabled
- Enabled only in case of VT fuse/MCB failure
- Enabled only in case of protection communication channel failure
- Enabled if VT fuse/MCB or protection communication channel fail
- Enabled if VT fuse/MCB and protection communication channel fail

In addition, each stage may be inhibited/blocked by a DDB signal.

It should be noted that phase overcurrent protection is phase segregated, but the operation of any phase is mapped to 3 phase tripping in the default PSL.

The VTS element of the IED can be selected to either block the directional element or simply remove the directional control.

14.2.1 IDMT CHARACTERISTICS

There are two basic requirements to consider when designing protection schemes:

- All faults should be cleared as quickly as possible to minimise damage to equipment
- Fault clearance should result in minimum disruption to the electrical power grid.

The second requirement means that the protection scheme should be designed such that only the circuit breaker(s) in the protection zone where the fault occurs, should trip.

These two criteria are actually in conflict with one another, because to satisfy (1), we increase the risk of shutting off healthy parts of the grid, and to satisfy (2) we purposely introduce time delays, which increase the amount of time a fault current will flow. With IDMT protection applied to radial feeders, this problem is exacerbated by the nature of faults in that the protection devices nearest the source, where the fault currents are largest, actually need the longest time delay.

IDMT characteristics are described by operating curves. Traditionally, these were defined by the performance of electromechanical devices. In numerical protection, equations are used to replicate these characteristics so that they can be used to grade with older equipment.

The old electromechanical devices countered this problem somewhat due to their natural operate time v. fault current characteristic, whereby the higher the fault current, the quicker the operate time. The characteristic typical of these electromechanical devices is called Inverse Definite Minimum Time or IDMT for short.

14.2.1.1 IEC 60255 IDMT CURVES

There are four well-known variants of this characteristic:

- Standard Inverse
- Very inverse
- Extremely inverse
- UK Long Time inverse

These equations and corresponding curves governing these characteristics are very well known in the power industry.

Standard inverse

This characteristic is commonly known as the 3/10 characteristic, i.e. at ten times setting current and TMS of 1 the device will operate in 3 seconds.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{0.14}{\left(\frac{I}{I_s}\right)^{0.02} - 1}$$

The standard inverse time characteristic is widely applied at all system voltages – as back up protection on EHV systems and as the main protection on HV and MV distribution systems.

In general, the standard inverse characteristics are used when:

- There are no co-ordination requirements with other types of protective equipment further out on the system, e.g. Fuses, thermal characteristics of transformers, motors etc.
- The fault levels at the near and far ends of the system do not vary significantly.
- There is minimal inrush on cold load pick up. Cold load inrush is that current which occurs when a feeder is energised after a prolonged outage. In general the device cannot be set above this value but the current should decrease below the device setting before the device operates.

The Standard Inverse curve implemented in this device becomes definite time (DT) for input current values above 30 x I_s.

Very inverse

This type of characteristic is normally used to obtain greater time selectivity when the limiting overall time factor is very low, and the fault current at any point does not vary too widely with system conditions. It is particularly suitable, if there is a substantial reduction of fault current as the distance from the power source increases. The steeper inverse curve gives longer time grading intervals. Its operating time is approximately doubled for a reduction in setting from 7 to 4 times the device current setting. This permits the same time multiplier setting for several devices in series.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{13.5}{\left(\frac{I}{I_s}\right) - 1}$$

The Very Inverse curve implemented in this device becomes definite time (DT) for input current values above 30 x I_s.

Extremely inverse

With this characteristic the operating time is approximately inversely proportional to the square of the current. The long operating time of the device at peak values of load current make the device particularly suitable for grading with fuses and also for protection of feeders which are subject to peak currents on switching in, such as feeders supplying refrigerators, pumps, water heaters etc., which remain connected even after a prolonged interruption of supply.

For cases where the generation is practically constant and discrimination with low tripping times is difficult to obtain, because of the low impedance per line section, an extremely inverse device can be very useful since only a small difference of current is necessary to obtain an adequate time difference.

Another application for this device is with auto reclosers in low voltage distribution circuits. As the majority of faults are of a transient nature, the device is set to operate before the normal operating time of the fuse, thus preventing perhaps unnecessary blowing of the fuse.

Upon reclosure, if the fault persists, the recloser locks itself in the closed position and allows the fuse to blow to clear the fault.

The Extremely Inverse curve implemented in this device becomes definite time (DT) for input current values above 20 x I_S.

This characteristic is also widely used for protecting plant against overheating since overheating is usually an I2t function.

This characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{80}{\left(\frac{I}{I_s}\right)^2 - 1}$$

UK long time inverse

This type of characteristic has a long time characteristic and may be used for protection of neutral earthing resistors (which normally have a 30 second rating). The device operating time at 5 times current setting is 30 seconds at a TMS of 1.

This can be defined by:

$$t_{op} = T \frac{120}{\left(\frac{I}{I_s}\right) - 1}$$

In the above equations:

- t_{op} is the operating time
- T is the time multiplier setting
- I is the measured current
- I_S is the current threshold setting

The ratio I/I_S is sometimes defined as ‘M’ or ‘PSM’ (Plug Setting Multiplier).

The Long Time Inverse curve implemented in this device becomes definite time (DT) for input current values above 30 x I_S.

These curves are plotted as follows:

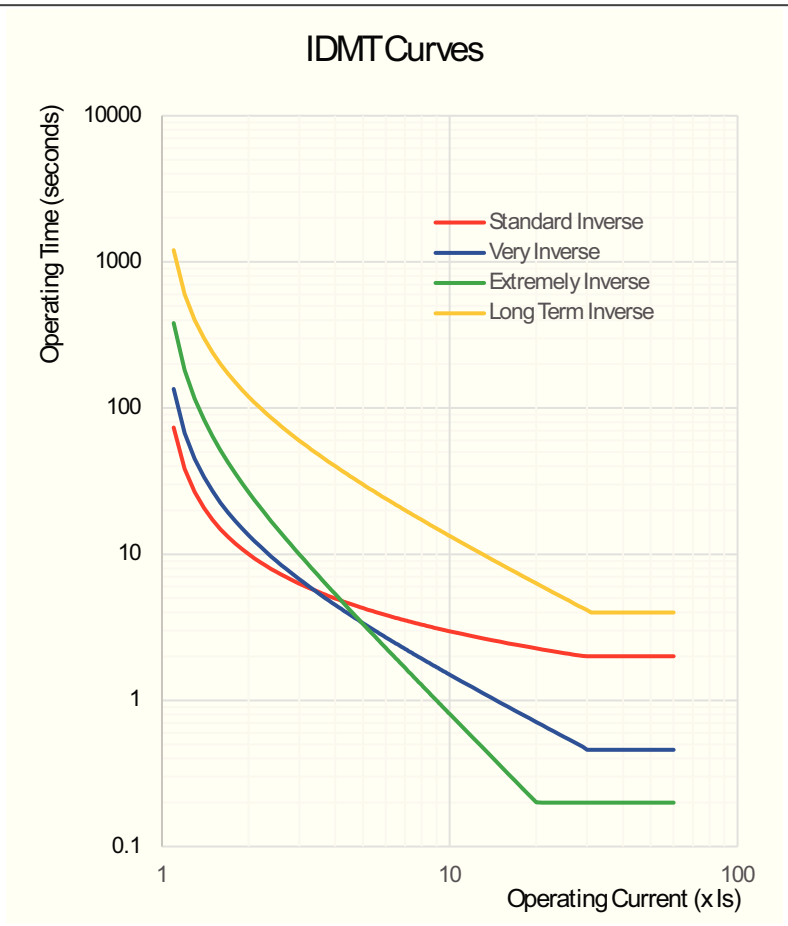


Figure 301: IEC 60255 IDMT curves

14.2.1.2 EUROPEAN STANDARDS

The IEC 60255 IDMT Operate equation is:

$$t_{op} = T\left(\frac{\beta}{M^{\alpha}-1} + L\right) + C$$

and the IEC 60255 IDMT Reset equation is:

$$t_{r} = T\left(\frac{\beta}{1-M^{\alpha}}\right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- T is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/Is)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEC IDMT curves are as follows:

Curve Description	β constant	α constant	L constant
IEC Standard Inverse Operate	0.14	0.02	0
IEC Standard Inverse Reset	8.2	6.45	0
IEC Very Inverse Operate	13.5	1	0
IEC Very Inverse Reset	50.92	2.4	0
IEC Extremely Inverse Operate	80	2	0
IEC Extremely Inverse Reset	44.1	3.03	0
UK Long Time Inverse Operate*	120	1	0

Note:
** When using UK Long Time Inverse, the DT (Definite Time) is always used for the Reset characteristic.*

14.2.1.3 NORTH AMERICAN STANDARDS

The IEEE IDMT Operate equation is:

$$t_{op} = TD\left(\frac{\beta}{M^{\alpha}-1}+L\right)+C$$

and the IEEE IDMT Reset equation is:

$$t_{r} = TD\left(\frac{\beta}{1-M^{\alpha}}\right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- TD is the Time Dial setting
- M is the ratio of the measured current divided by the threshold current (I/I_s)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEEE curves are as follows:

Curve Description	β constant	α constant	L constant
IEEE Moderately Inverse Operate	0.0515	0.02	0.114
IEEE Moderately Inverse Reset	4.85	2	0
IEEE Very Inverse Operate	19.61	2	0.491
IEEE Very Inverse Reset	21.6	2	0
IEEE Extremely Inverse Operate	28.2	2	0.1217
IEEE Extremely Inverse Reset	29.1	2	0
CO8 US Inverse Operate	5.95	2	0.18

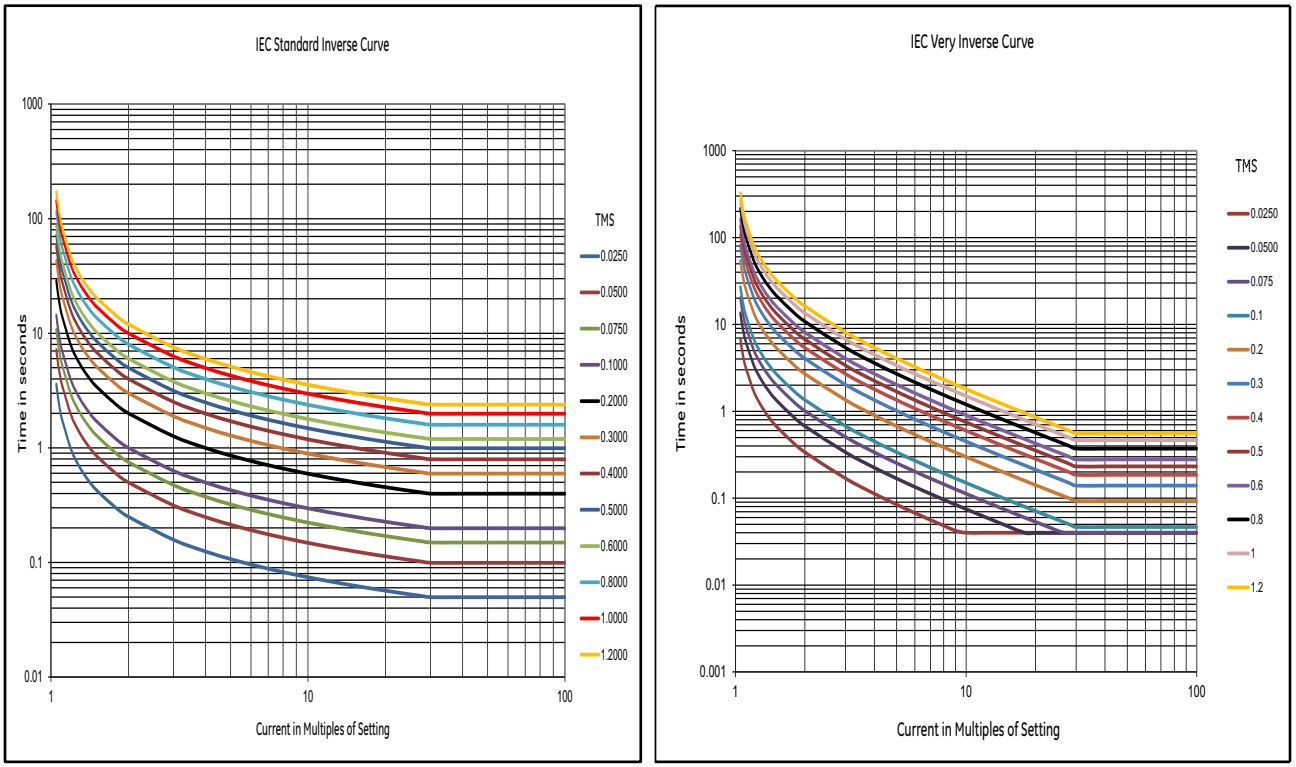
Curve Description	β constant	α constant	L constant
CO8 US Inverse Reset	5.95	2	0
CO2 US Short Time Inverse Operate	0.16758	0.02	0.11858
CO2 US Short Time Inverse Reset	2.261	2	0

The constant values for the ANSI curves are as follows:

Curve Description	β constant	α constant	L constant
ANSI Normally Inverse Operate	8.9341	2.0938	0.17966
ANSI Normally Inverse Reset	9	2	0
ANSI Short Time Inverse Operate	0.03393	1.2969	0.2663
ANSI Short Time Inverse Reset	0.5	2	0
ANSI Long Time Inverse Operate	2.18592	1	5.6143
ANSI Long Time Inverse Reset	15.75	2	0

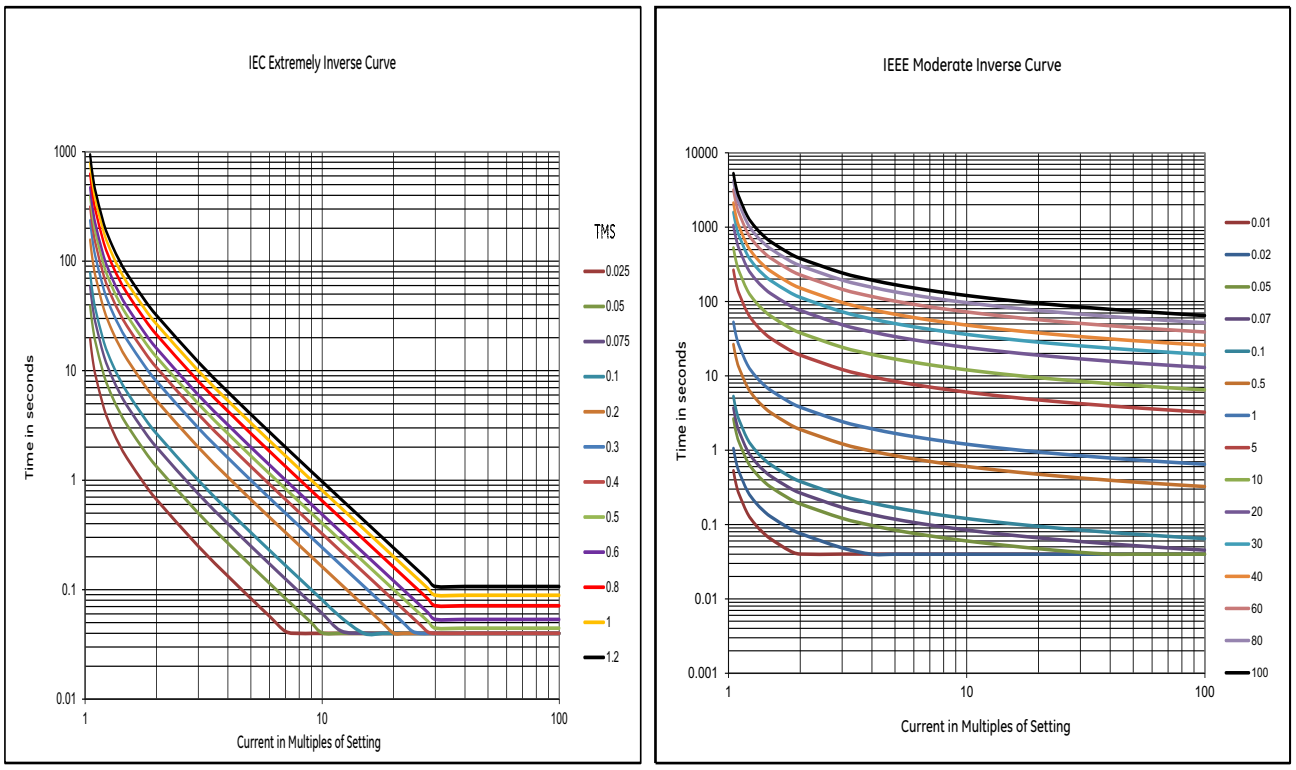
Note:
** When using UK Long Time Inverse or UK Rectifier for the Operate characteristic, DT is always used for the Reset characteristic.*

14.2.1.4 IEC AND IEEE INVERSE CURVES



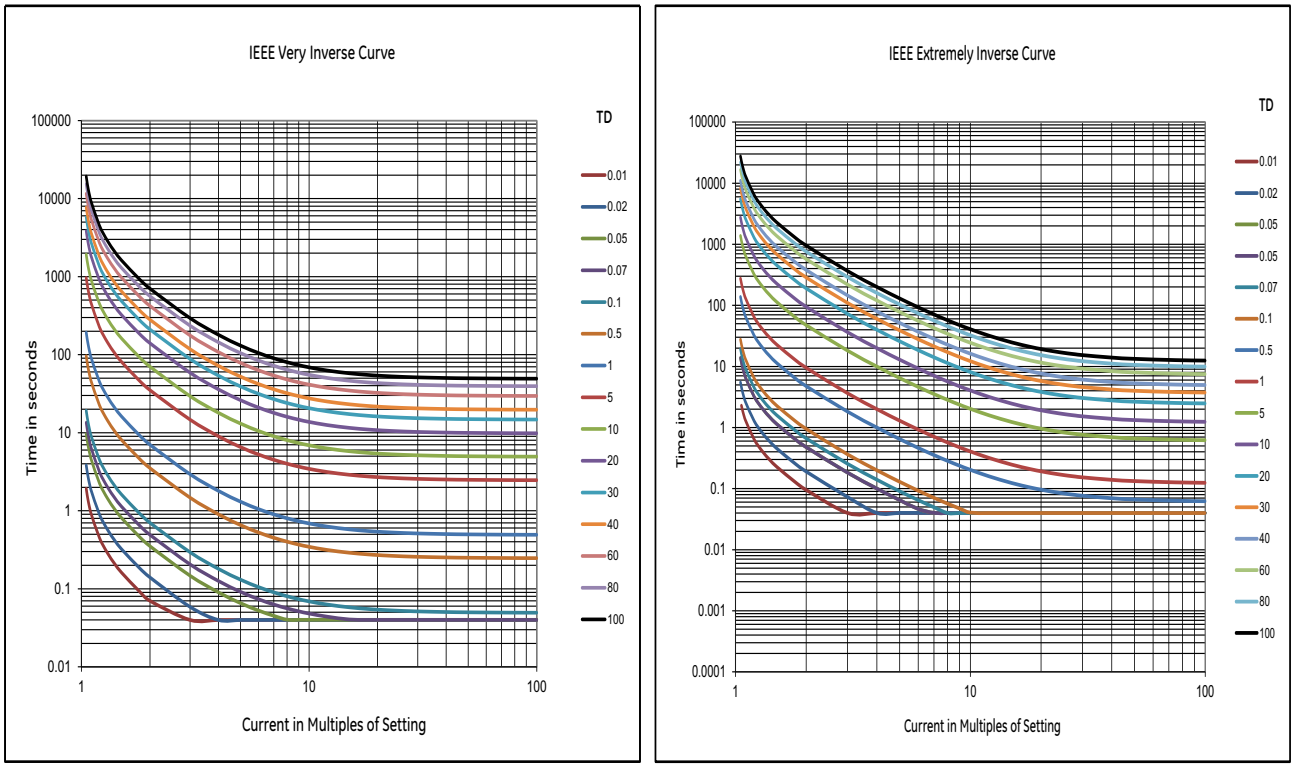
E00757

Figure 302: IEC standard and very inverse curves



E00758

Figure 303: IEC extremely inverse and IEEE moderate inverse curves



E00759

Figure 304: IEEE very and extremely inverse curves

14.2.1.5 DIFFERENCES BETWEEN THE NORTH AMERICAN AND EUROPEAN STANDARDS

The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is used for the IEEE/US curves. The menu is arranged such that if an IEC/UK curve is selected, the ***I> Time Dial*** cell is not visible and vice versa for the TMS setting. For both IEC and IEEE/US type curves, a definite time adder setting is available, which will increase the operating time of the curves by the set value.

14.2.1.6 PROGRAMMABLE CURVES

As well as the standard curves as defined by various countries and standardising bodies, it is possible to program custom curves using the User Programmable Curve Tool, described in the Settings Application Software chapter. This is a user-friendly tool by which you can create curves either by formula or by entering data points. Programmable curves help you to match more closely the withstand characteristics of the electrical equipment than standard curves.

14.2.2 POC IMPLEMENTATION

Phase Overcurrent Protection is configured in the OVERCURRENT column of the relevant settings group.

The product provides four stages of three-phase overcurrent protection, each with independent time delay characteristics. The settings are independent for each stage, but for each stage, the settings apply to all phases.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves based on IEC and IEEE standards
- A range of programmable user-defined curves
- DT (Definite Time) characteristic

This is achieved using the cells:

- ***I>(n) Function*** for the overcurrent operate characteristic
- ***I>(n) Reset Char*** for the overcurrent reset characteristic
- ***I>(n) Usr Rst Char*** for the reset characteristic for user-defined curves

where (n) is the number of the stage.

The IDMT-equipped stages, (1 and 2) also provide a Timer Hold facility. This is configured using the cells ***I>(n) tReset***, where (n) is the number of the stage. This does not apply to IEEE curves.

Stages 3 and 4 have definite time characteristics only.

14.2.3 DIRECTIONAL ELEMENT

If fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Once the direction has been determined the device can decide whether to allow tripping or to block tripping. To determine the direction of a phase overcurrent fault, the device must compare the phase angle of the fault current with that of a known reference quantity. The phase angle of this known reference quantity must be independent of the faulted phase. Typically this will be the line voltage between the other two phases.

The phase fault elements of the IEDs are internally polarised by the quadrature phase-phase voltages, as shown in the table below:

Phase of Protection	Operate Current	Polarising Voltage
A Phase	IA	VBC
B Phase	IB	VCA

Phase of Protection	Operate Current	Polarising Voltage
C Phase	IC	VAB

Under system fault conditions, the fault current vector lags its nominal phase voltage by an angle depending on the system X/R ratio. The IED must therefore operate with maximum sensitivity for currents lying in this region. This is achieved by using the IED characteristic angle (RCA). This is the is the angle by which the current applied to the IED must be displaced from the voltage applied to the IED to obtain maximum sensitivity.

The device provides a setting ***I> Char Angle***, which is set globally for all overcurrent stages. It is possible to set characteristic angles anywhere in the range –95° to +95°.

A directional check is performed based on the following criteria:

Directional forward

$$-90° < (\text{angle(I)} - \text{angle(V)} - \text{RCA}) < 90°$$

Directional reverse

$$-90° > (\text{angle(I)} - \text{angle(V)} - \text{RCA}) > 90°$$

For close up three-phase faults, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the device includes a synchronous polarisation feature that stores the pre-fault voltage information and continues to apply this to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

14.2.4 POC LOGIC

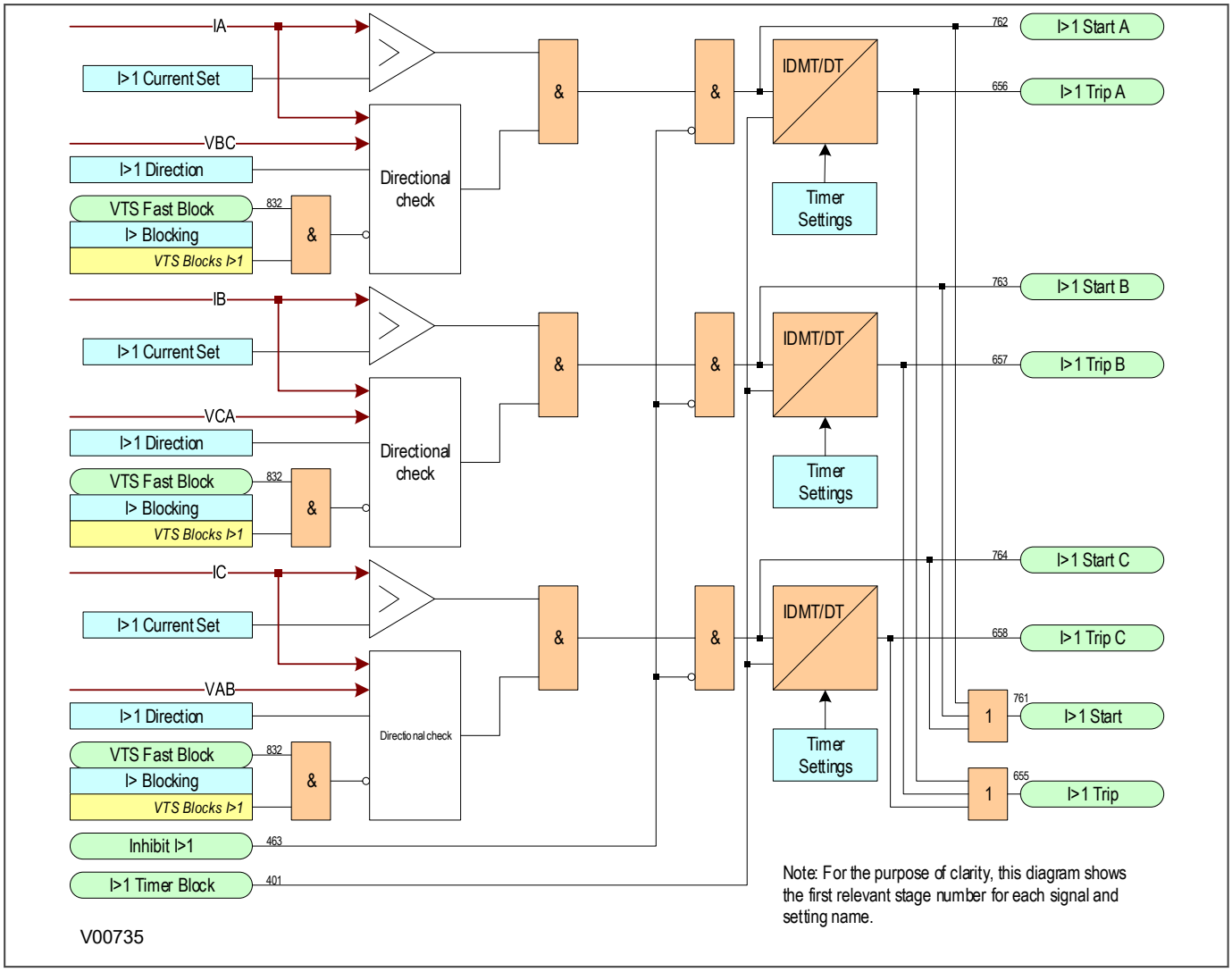


Figure 305: Phase overcurrent protection logic

14.2.5 POC LOGIC

If there is a need to inhibit the overcurrent element during inrush condition, an additional logic as shown below can be created in PSL.

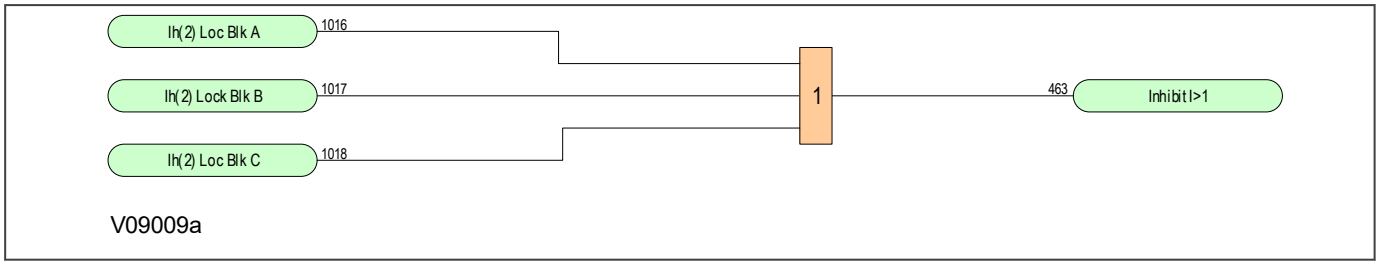


Figure 306: 2nd harmonic block

The settable threshold for 2nd harmonic is available in Supervision/Inrush detection.

14.3 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

When applying standard phase overcurrent protection, the overcurrent elements must be set significantly higher than the maximum load current. This limits the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes. Negative Phase Sequence Overcurrent elements can help in such cases.

Any unbalanced fault condition will produce a negative sequence current component. Therefore, a negative phase sequence overcurrent element can be used for both phase-to-phase and phase-to-earth faults. Negative Phase Sequence Overcurrent protection offers the following advantages:

- Negative phase sequence overcurrent elements are more sensitive to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault element due to the system configuration. For example, an earth fault element applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element may be used to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

14.3.1 NEGATIVE SEQUENCE OVERCURRENT PROTECTION IMPLEMENTATION

Negative Sequence Overcurrent Protection is implemented in the *NEG SEQ O/C* column of the relevant settings group.

The product provides four stages of negative sequence overcurrent protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***I2>(n) Function*** for the overcurrent operate characteristic
- ***I2>(n) Reset Char*** for the overcurrent reset characteristic

where (n) is the number of the stage.

The IDMT-capable stages, (1 and 2) also provide a Timer Hold. This is configured using the cells ***I2>(n) tReset***, where (n) is the number of the stage. This is not applicable for curves based on the IEEE standard.

Stages 3 and 4 have definite time characteristics only.

14.3.2 DIRECTIONAL ELEMENT

Where negative phase sequence current may flow in either direction, directional control should be used.

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. A directional element is available for all of the negative sequence overcurrent stages. This is found in the ***I2> Direction*** cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

A suitable characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (**–V2**), in order to be at the centre of the directional characteristic.

14.3.3 NPSOC LOGIC

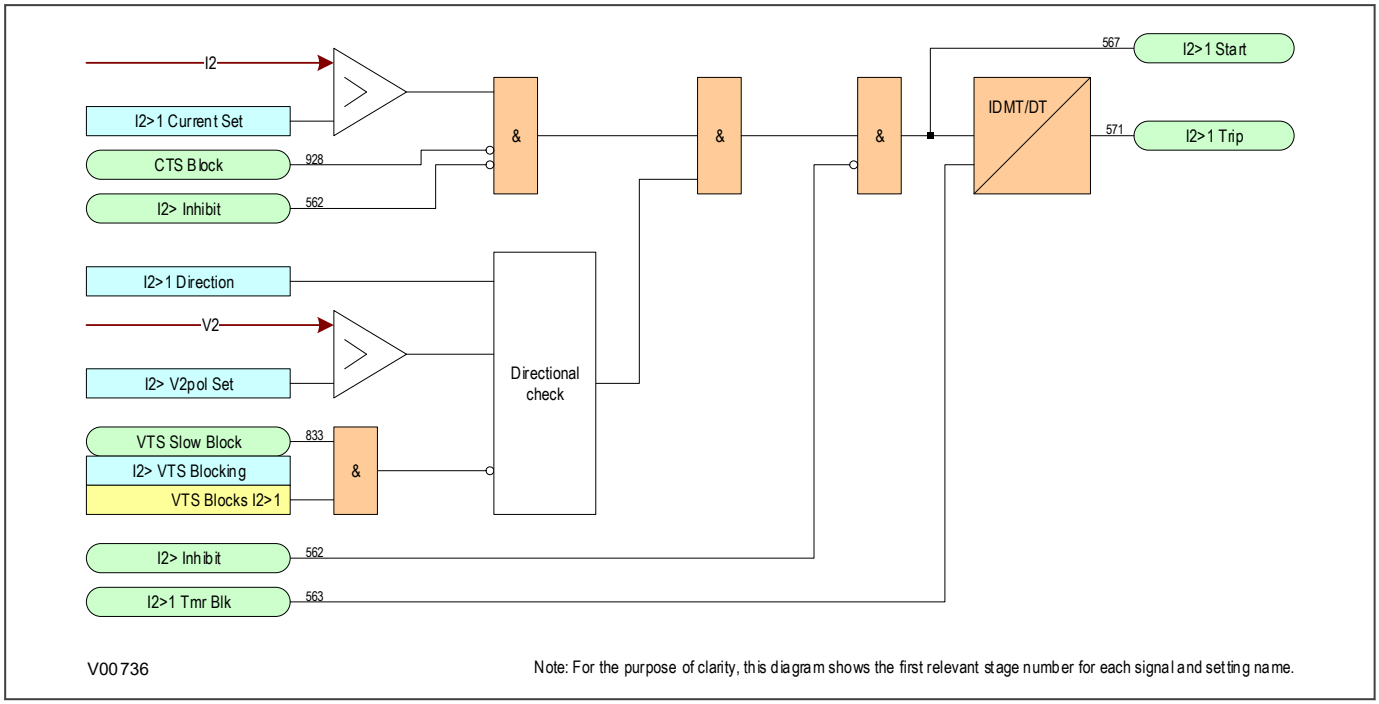


Figure 307: Negative phase sequence overcurrent protection logic

14.3.4 APPLICATION NOTES

14.3.4.1 SETTING GUIDELINES (CURRENT THRESHOLD)

A negative phase sequence element can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-earth or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and earth elements for phase-to-earth and phase-to-phase faults.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load imbalance. This can be set practically at the commissioning stage, making use of the measurement function to display the standing negative phase sequence current. The setting should be at least 20% above this figure.

Where the negative phase sequence element needs to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

14.3.4.2 SETTING GUIDELINES (TIME DELAY)

Correct setting of the time delay for this function is vital. You should also be very aware that this element is applied primarily to provide back-up protection to other protection devices or to provide an alarm. It would therefore normally have a long time delay.

The time delay set must be greater than the operating time of any other protection device (at minimum fault level) that may respond to unbalanced faults such as phase overcurrent elements and earth fault elements.

14.3.4.3 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control of the element should be employed (VT models only).

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the relay characteristic angle (RCA) should be set equal to –60°
- For a distribution system the relay characteristic angle (RCA) should be set equal to –45°

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2> V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

14.4 EARTH FAULT PROTECTION

Earth faults are overcurrent faults where the fault current flows to earth. Earth faults are the most common type of fault.

Earth faults can be measured directly from the system by means of:

- A separate current Transformer (CT) located in a power system earth connection
- A separate Core Balance Current Transformer (CBCT), usually connected to the SEF transformer input
- A residual connection of the three line CTs, where the Earth faults can be derived mathematically by summing the three measured phase currents

Depending on the device model, it will provide one or more of the above means for Earth fault protection.

14.4.1 EARTH FAULT PROTECTION IMPLEMENTATION

Earth fault protection is implemented in the *EARTH FAULT* column of the relevant settings group. The element uses quantities derived internally from summing the three-phase currents.

The product provides four stages of Earth Fault protection with independent time delay characteristics, for each *EARTH FAULT* column.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells:

- ***IN>(n) Function*** for the overcurrent operate characteristics
- ***IN>(n) Reset Char*** for the overcurrent reset characteristic

where (n) is the number of the stage.

Stages 1 and 2 provide a Timer Hold facility. This is configured using the cells ***IN>(n) tReset***

Stages 3 and 4 can have definite time characteristics only.

Earth fault Overcurrent IN> can be set to:

- Permanently disabled
- Permanently enabled
- Enabled only if VT fuse/MCB fails
- Enabled only if protection communication channel fails
- Enabled if VT fuse/MCB or protection communication channel fail
- Enabled if VT fuse/MCB and protection communication channel fail

Each stage can be individually inhibited with a DDB signal ***Inhibit IN>(n)***, where n is the stage number.

14.4.2 IDG CURVE

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

$$t_{op} = 5.8 - 1.35 log_e \left(\frac{I}{IN > Setting} \right)$$

where:

t_{op} is the operating time

I is the measured current

IN> Setting is an adjustable setting, which defines the start point of the characteristic

Note:
Although the start point of the characteristic is defined by the "IN>" setting, the actual current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

Note:
When using an IDG Operate characteristic, DT is always used with a value of zero for the Rest characteristic.

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

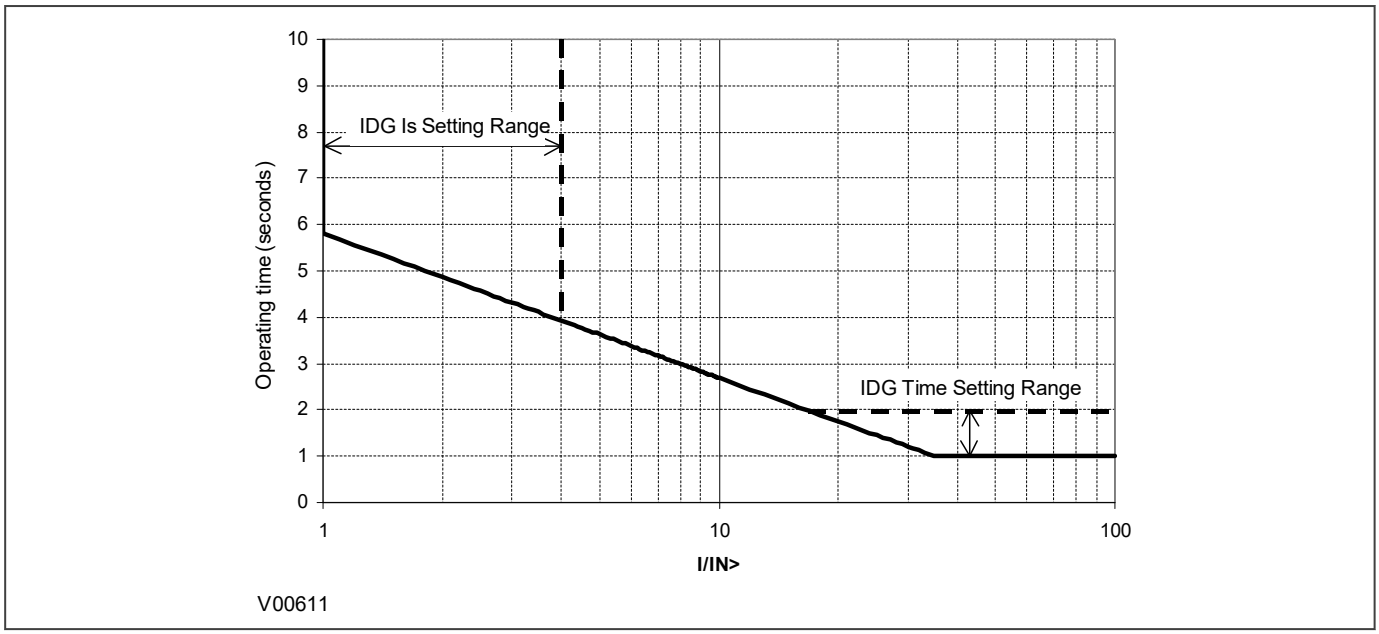


Figure 308: IDG characteristic

14.4.3 DIRECTIONAL ELEMENT

If Earth fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Typical systems that require such protection are parallel feeders and ring main systems.

A directional element is available for all of the Earth Fault stages. These are found in the direction setting cells for the relevant stage. They can be set to non-directional, directional forward, or directional reverse.

Directional control can be blocked by the VTS element if required.

For standard earth fault protection, two options are available for polarisation; Residual Voltage (zero sequence) or Negative Sequence.

14.4.3.1 RESIDUAL VOLTAGE POLARISATION

With earth fault protection, the polarising signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise directional earth fault

elements. This is known as Zero Sequence Voltage polarisation, Residual Voltage polarisation or Neutral Displacement Voltage (NVD) polarisation.

Small levels of residual voltage could be present under normal system conditions due to system imbalances, VT inaccuracies, device tolerances etc. For this reason, the device includes a user settable threshold (***IN> VNPol set***), which must be exceeded in order for the DEF function to become operational. The residual voltage measurement provided in the *MEASUREMENTS 1* column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note:
Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the "-Vres" quantity. This 180° phase shift is automatically introduced within the device.

The directional criteria with residual voltage polarisation is given below:

- Directional forward: -90° < (angle(IN) - angle(VN + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(IN) - angle(VN + 180°) - RCA) > 90°

14.4.3.2 NEGATIVE SEQUENCE POLARISATION

In some applications, the use of residual voltage polarisation may not be possible to achieve or it can be problematic. For example, a suitable type of VT may be unavailable, or an HV/EHV parallel line application may present problems with zero sequence mutual coupling.

In such situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarisation. This method determines the fault direction by comparing the NPS voltage with the NPS current. The operating quantity, however, is still residual current.

This can be used for both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells ***IN> V2pol set*** and ***IN> I2pol set*** respectively.

Negative phase sequence polarising is not recommended for impedance earthed systems regardless of the type of VT feeding the device. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance to negligible levels. If this voltage is less than 0.5 volts the device will stop providing directionalisation.

The directional criteria with negative sequence polarisation is given below:

- Directional forward: -90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

14.4.4 EARTH FAULT PROTECTION LOGIC

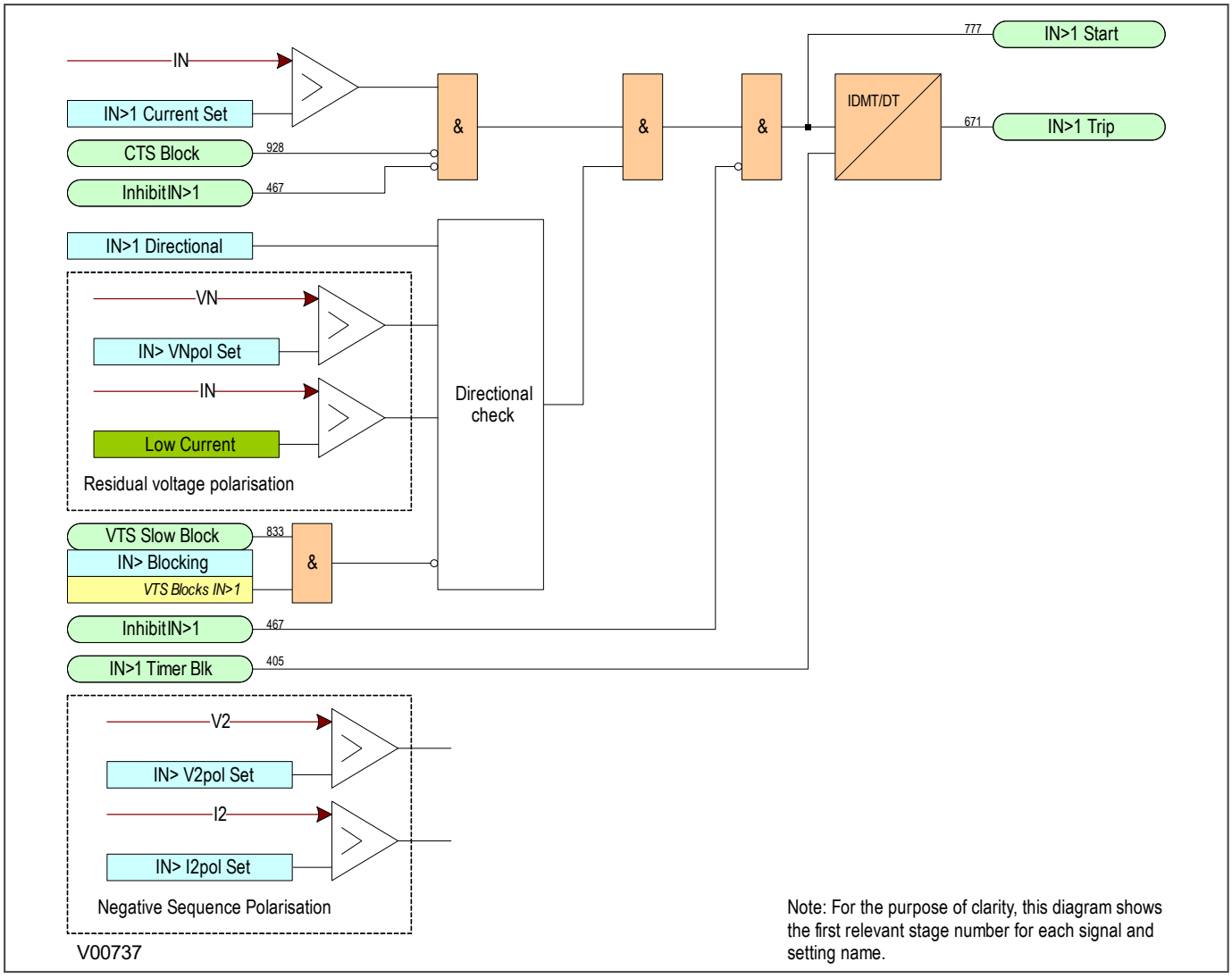


Figure 309: Earth fault protection logic

14.4.5 APPLICATION NOTES

14.4.5.1 RESIDUAL VOLTAGE POLARISATION SETTING GUIDELINES

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies, IED tolerances etc. Hence, the IED includes a user settable threshold (***IN> VNPol Set***) which must be exceeded in order for the DEF function to be operational. In practice, the typical zero sequence voltage on a healthy system can be as high as 1% (i.e. 3% residual), and the VT error could be 1% per phase. A setting between 1% and 4% is therefore typical. The residual voltage measurement may assist in determining the required threshold setting during commissioning, as this will indicate the level of standing residual voltage present.

14.4.5.2 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

With directional earth faults, the residual current under fault conditions lies at an angle lagging the polarising voltage. Hence, negative RCA settings are required for DEF applications. This is set in the cell ***I> Char Angle*** in the relevant earth fault menu.

We recommend the following RCA settings:

- Resistance earthed systems: 0°
- Distribution systems (solidly earthed): -45°
- Transmission systems (solidly earthed): -60°

14.5 SENSITIVE EARTH FAULT PROTECTION

With some earth faults, the fault current flowing to earth is limited by either intentional resistance (as is the case with some HV systems) or unintentional resistance (e.g. in very dry conditions and where the substrate is high resistance, such as sand or rock).

To provide protection in such cases, it is necessary to provide an earth fault protection system with a setting that is considerably lower than for normal line protection. Such sensitivity cannot be provided with conventional CTs, therefore the SEF input would normally be fed from a core balance current transformer (CBCT) mounted around the three phases of the feeder cable. The SEF transformer should be a special measurement class transformer.

14.5.1 SEF PROTECTION IMPLEMENTATION

The product provides four stages of SEF protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***ISEF>(n) Function*** for the overcurrent operate characteristic
- ***ISEF>(n) Reset Chr*** for the overcurrent reset characteristic

where (n) is the number of the stage.

Stages 1 and 2 also provide a Timer Hold facility. This is configured using the cells ***ISEF>(n) tReset***.

Stages 3 and 4 have definite time characteristics only.

Each stage can be individually inhibited with a DDB signal Inhibit ISEF>(n), where n is the stage number.

14.5.2 EPATR B CURVE

The EPATR B curve is commonly used for time-delayed Sensitive Earth Fault protection in certain markets. This curve is only available in the Sensitive Earth Fault protection stages 1 and 2. It is based on primary current settings, employing a SEF CT ratio of 100:1 A.

The EPATR_B curve has 3 separate segments defined in terms of the primary current. It is defined as follows:

Segment	Primary Current Range Based on 100A:1A CT Ratio	Current/Time Characteristic
1	ISEF = 0.5A to 6.0A	t = 432 x TMS/ISEF 0.655 secs
2	ISEF = 6.0A to 200A	t = 800 x TMS/ISEF secs
3	ISEF above 200A	t = 4 x TMS secs

where TMS (time multiplier setting) is 0.025 - 1.2 in steps of 0.025.

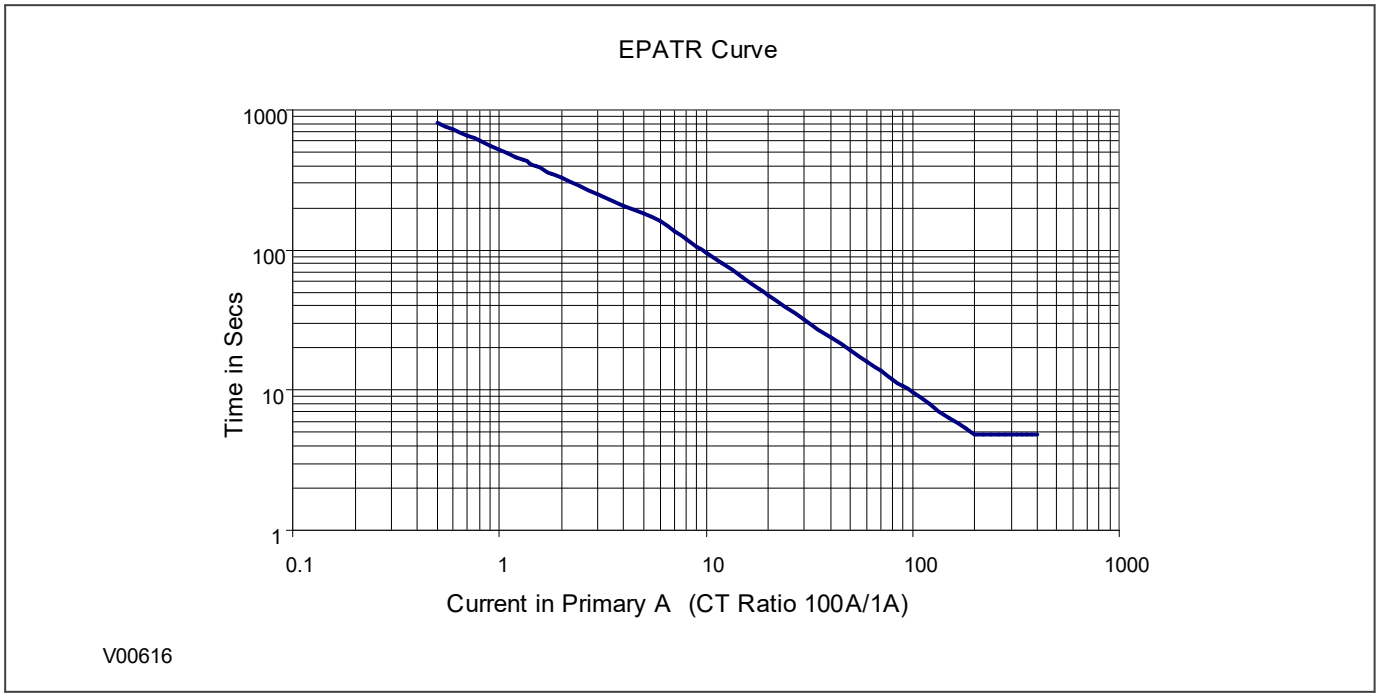


Figure 310: EPATR B characteristic shown for TMS = 1.0

14.5.3 SENSITIVE EARTH FAULT PROTECTION LOGIC

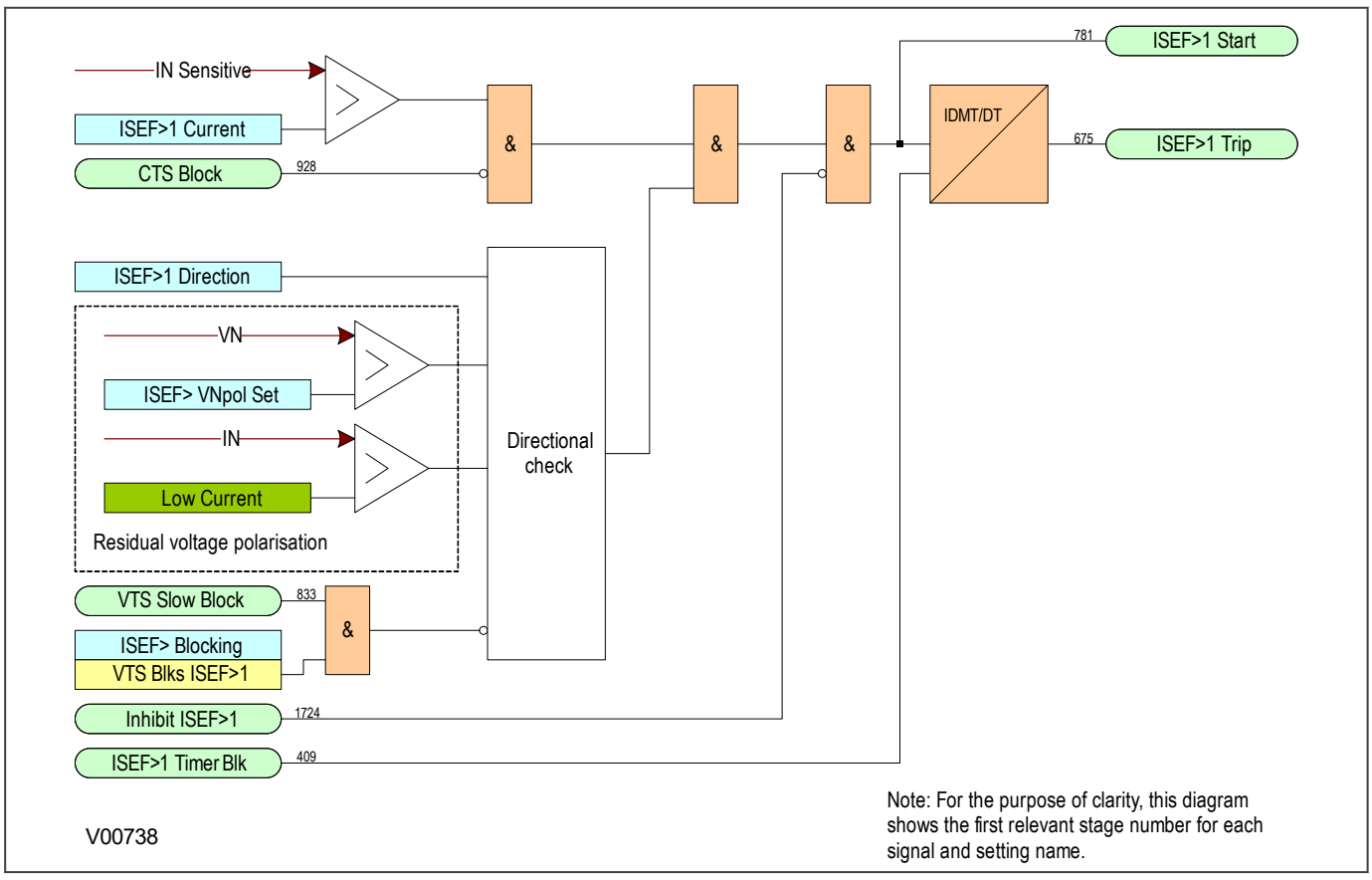


Figure 311: Sensitive earth fault protection logic

14.5.4 APPLICATION NOTES

14.5.4.1 INSULATED SYSTEMS

When insulated systems are used, it is not possible to detect faults using standard earth fault protection. It is possible to use a residual overvoltage device to achieve this, but even with this method full discrimination is not possible. Fully discriminative earth fault protection on this type of system can only be achieved by using a SEF (Sensitive Earth Fault) element. This type of protection detects the resultant imbalance in the system charging currents that occurs under earth fault conditions. A core balanced CT must be used for this application. This eliminates the possibility of spill current that may arise from slight mismatches between residually connected line CTs. It also enables a much lower CT ratio to be applied, thereby allowing the required protection sensitivity to be more easily achieved.

The following diagram shows an insulated system with a C-phase fault.

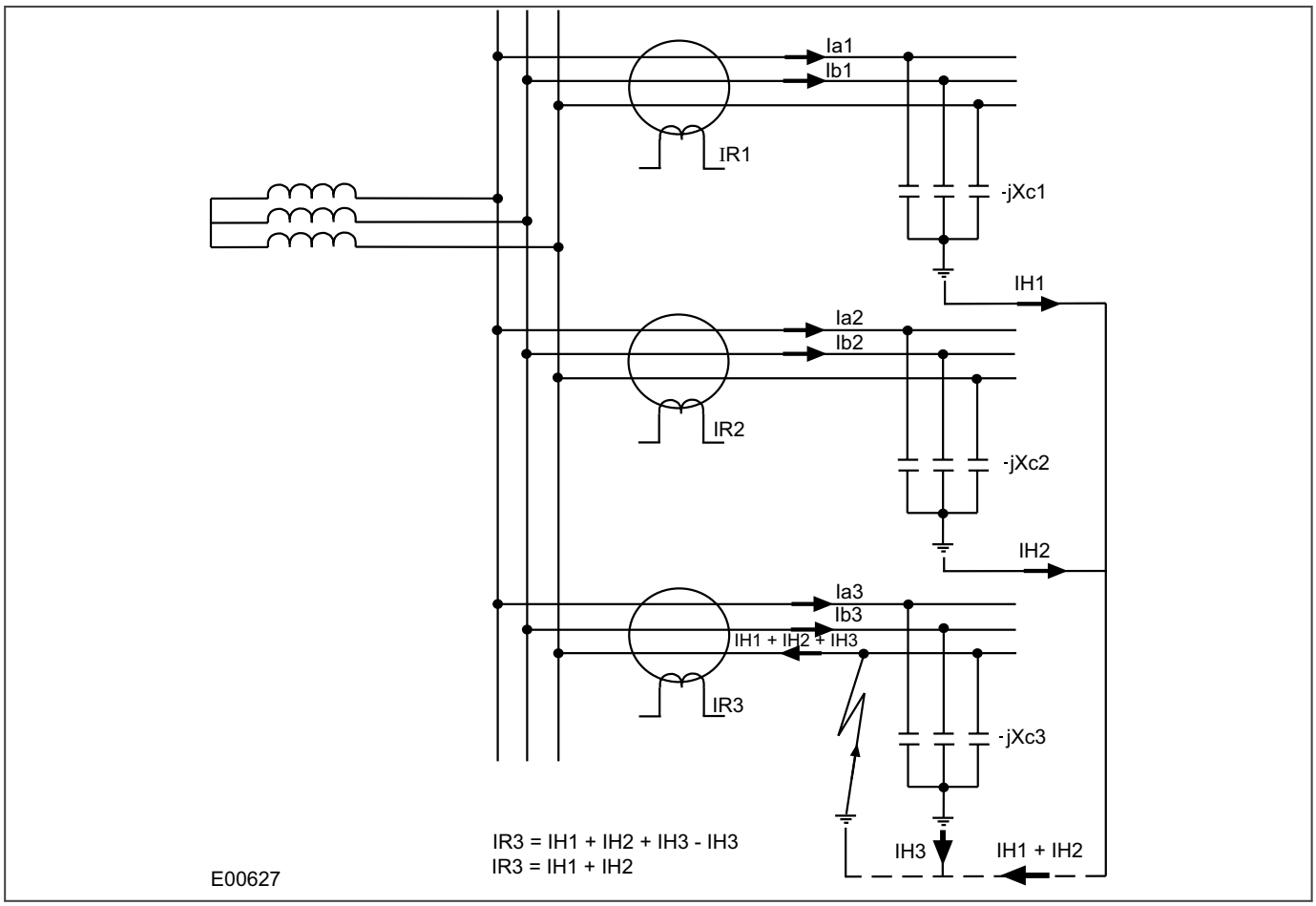


Figure 312: Current distribution in an insulated system with C phase fault

The protection elements on the healthy feeder see the charging current imbalance for their own feeder. The protection element on the faulted feeder, however, sees the charging current from the rest of the system (IH1 and IH2 in this case). Its own feeder's charging current (IH3) is cancelled out.

With reference to the associated vector diagram, it can be seen that the C-phase to earth fault causes the voltages on the healthy phases to rise by a factor of √3. The A-phase charging current (Ia1), leads the resultant A phase voltage by 90°. Likewise, the B-phase charging current leads the resultant Vb by 90°.

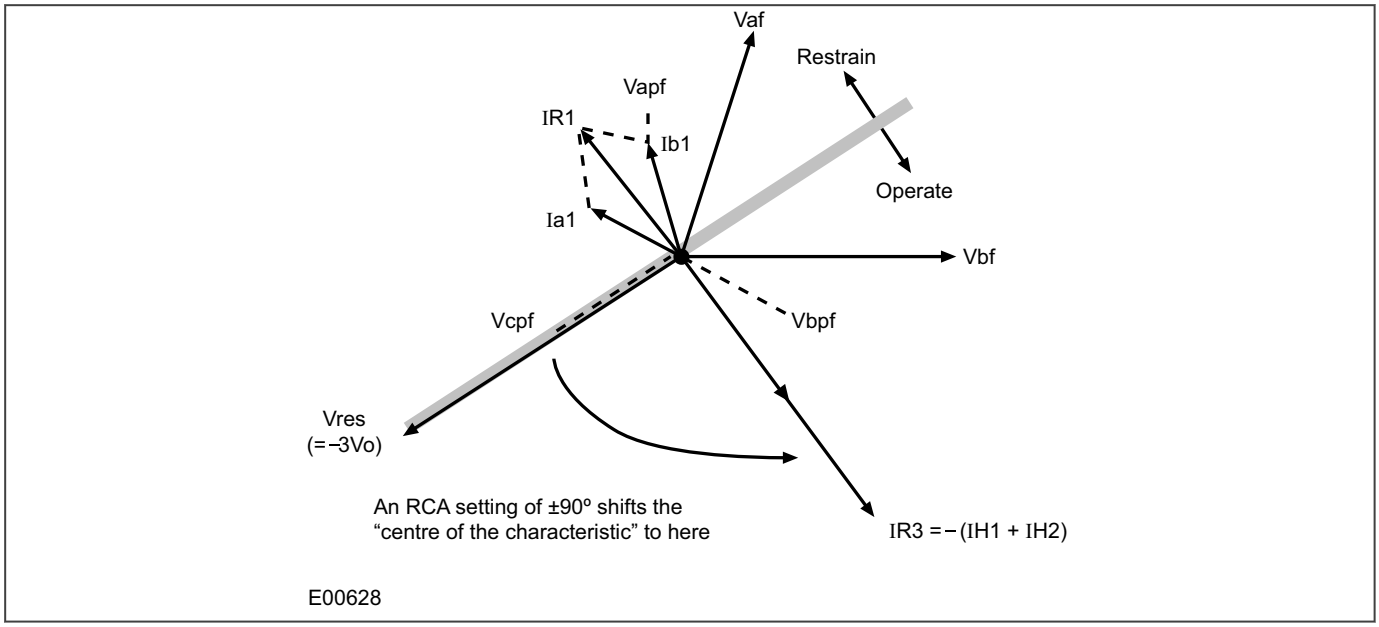


Figure 313: Phasor diagrams for insulated system with C phase fault

The current imbalance detected by a core balanced current transformer on the healthy feeders is the vector addition of Ia1 and Ib1. This gives a residual current which lags the polarising voltage (–3Vo) by 90°. As the healthy phase voltages have risen by a factor of √3, the charging currents on these phases are also √3 times larger than their steady state values. Therefore, the magnitude of the residual current IR1, is equal to 3 times the steady state per phase charging current.

The phasor diagram indicates that the residual currents on the healthy and faulted feeders (IR1 and IR3 respectively) are in anti-phase. A directional element (if available) could therefore be used to provide discriminative earth fault protection.

If the polarising is shifted through +90°, the residual current seen by the device on the faulted feeder will lie within the operate region of the directional characteristic and the current on the healthy feeders will fall within the restrain region.

The required characteristic angle setting for the SEF element when applied to insulated systems, is +90°. This is for the case when the protection is connected such that its direction of current flow for operation is from the source busbar towards the feeder. If the forward direction for operation were set such that it is from the feeder into the busbar, then a –90° RCA would be required.

Note:
Discrimination can be provided without the need for directional control. This can only be achieved, however, if it is possible to set the IED in excess of the charging current of the protected feeder and below the charging current for the rest of the system.

14.5.4.2 SETTING GUIDELINES (INSULATED SYSTEMS)

The residual current on the faulted feeder is equal to the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the per phase value. Therefore, the total imbalance current is equal to three times the per phase charging current of the rest of the system. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the remaining system. Practically though, the required setting may well be determined on site, where suitable settings can be adopted based on practically obtained results.

When using a core-balanced transformer, care must be taken in the positioning of the CT with respect to the earthing of the cable sheath:

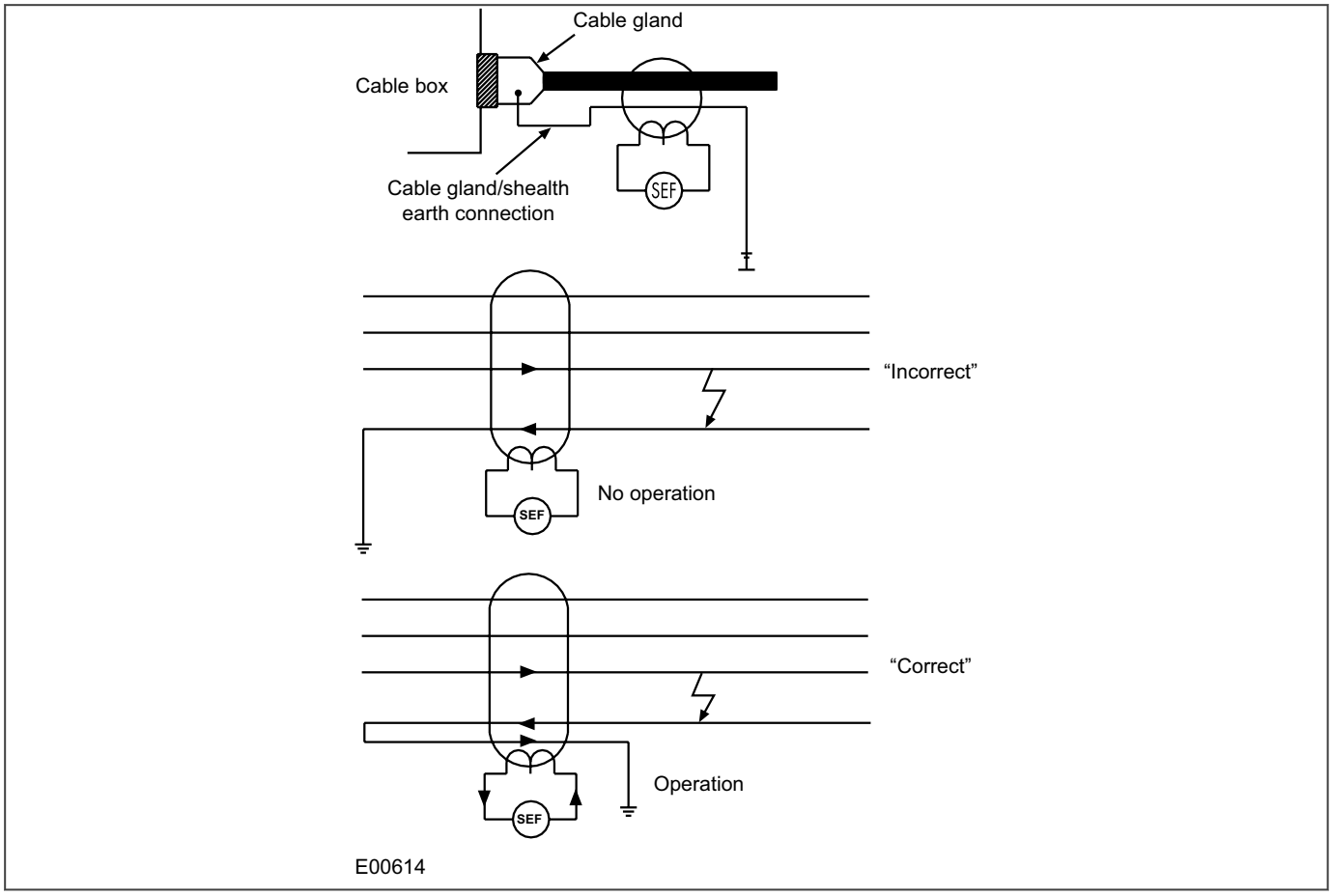


Figure 314: Positioning of core balance current transformers

If the cable sheath is terminated at the cable gland and directly earthed at that point, a cable fault (from phase to sheath) will not result in any unbalanced current in the core balance CT. Therefore, prior to earthing, the connection must be brought back through the CBCT and earthed on the feeder side. This then ensures correct device operation during earth fault conditions.

14.6 HIGH IMPEDANCE REF

The device provides a high impedance restricted earth fault protection function. An external resistor is required to provide stability in the presence of saturated line current transformers. Current transformer supervision signals do not block the high impedance REF protection. The appropriate logic must be configured in PSL to block the high impedance REF when any of the above signals is asserted.

14.6.1 HIGH IMPEDANCE REF PRINCIPLE

This scheme is very sensitive and can protect against low levels of fault current, typical of winding faults.

High Impedance REF protection is based on the differential principle. It works on the circulating current principle as shown in the following diagram.

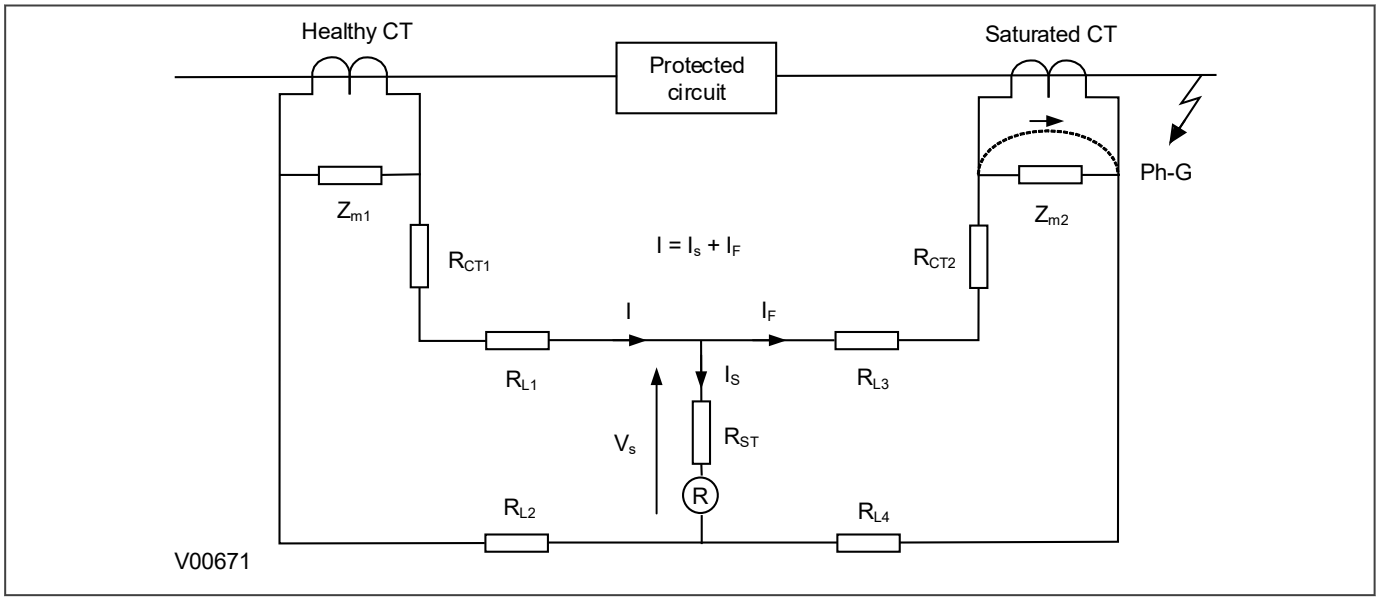


Figure 315: High impedance REF principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in imbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the device will be less than the setting, therefore maintaining stability during external faults.

Voltage across REF element $V_s = I_F (R_{CT2} + R_{L3} + R_{L4})$

Stabilising resistor $R_{ST} = V_s/I_s - R_R$

where:

- I_F = maximum secondary through fault current
- R_R = device burden
- R_{CT} = CT secondary winding resistance
- R_{L2} and R_{L3} = Resistances of leads from the device to the current transformer
- R_{ST} = Stabilising resistor

High Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED are as follows:

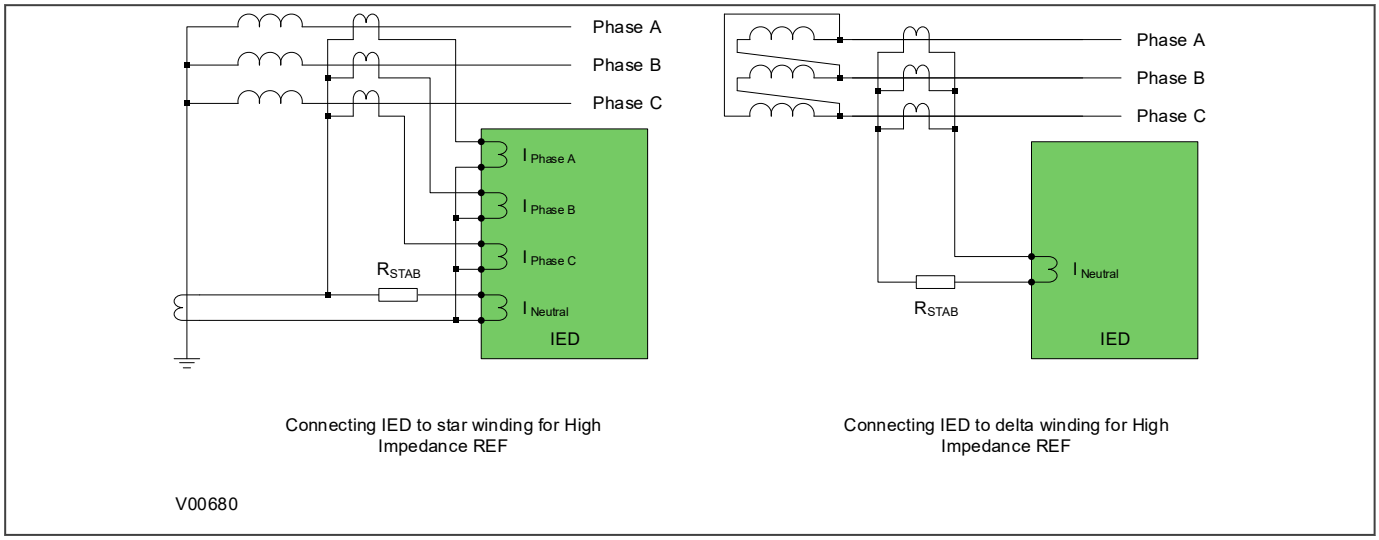


Figure 316: High impedance REF connection

14.7 THERMAL OVERLOAD PROTECTION

The heat generated within an item of plant is the resistive loss. The thermal time characteristic is therefore based on the equation I^2Rt. Over-temperature conditions occur when currents in excess of their maximum rating are allowed to flow for a period of time.

Temperature changes during heating follow exponential time constants. The device provides two characteristics for thermal overload protection; a single time constant characteristic and a dual time constant characteristic. You select these according to the application.

14.7.1 SINGLE TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect cables, dry type transformers and capacitor banks.

The single constant thermal characteristic is given by the equation:

$$t = -\tau \log_e \left[\frac{I^2 - \left(KI_{FLC}\right)^2}{I^2 - I_p{}^2} \right]$$

where:

- t = time to trip, following application of the overload current I
- τ = heating and cooling time constant of the protected plant
- I = largest phase current
- I_{FLC} full load current rating (the Thermal Trip setting)
- K = a constant with the value of 1.05
- I_p = steady state pre-loading before application of the overload

14.7.2 DUAL TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect equipment such as oil-filled transformers with natural air cooling. The thermal model is similar to that with the single time constant, except that two timer constants must be set.

For marginal overloading, heat will flow from the windings into the bulk of the insulating oil. Therefore, at low current, the replica curve is dominated by the long time constant for the oil. This provides protection against a general rise in oil temperature.

For severe overloading, heat accumulates in the transformer windings, with little opportunity for dissipation into the surrounding insulating oil. Therefore at high current levels, the replica curve is dominated by the short time constant for the windings. This provides protection against hot spots developing within the transformer windings.

Overall, the dual time constant characteristic serves to protect the winding insulation from ageing and to minimise gas production by overheated oil. Note however that the thermal model does not compensate for the effects of ambient temperature change.

The dual time constant thermal characteristic is given by the equation:

$$0.4e^{(-t/\tau_1)} + 0.6e^{(-t/\tau_2)} = \left[\frac{I^2 - \left(KI_{FLC}\right)^2}{I^2 - I_p{}^2} \right]$$

where:

- τ_1 = heating and cooling time constant of the transformer windings
- τ_2 = heating and cooling time constant of the insulating oil

14.7.3 THERMAL OVERLOAD PROTECTION IMPLEMENTATION

The device incorporates a current-based thermal characteristic, using Fourier based load current to model heating and cooling of the protected plant. The element can be set with both alarm and trip stages.

Thermal Overload Protection is implemented in the *THERMAL OVERLOAD* column of the relevant settings group.

This column contains the settings for the characteristic type, the alarm and trip thresholds and the time constants.

14.7.4 THERMAL OVERLOAD PROTECTION LOGIC

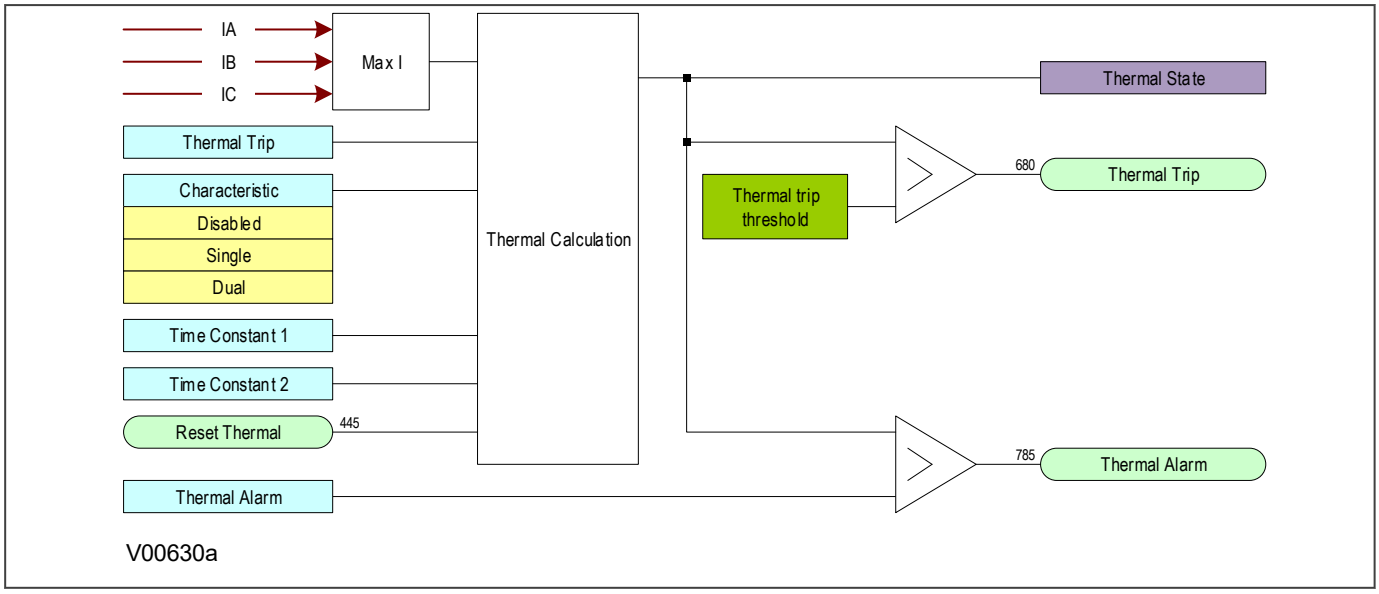


Figure 317: Thermal overload protection logic

The magnitudes of the three phase input currents are compared and the largest magnitude is taken as the input to the thermal overload function. If this current exceeds the thermal trip threshold setting a start condition is asserted.

The Start signal is applied to the chosen thermal characteristic module, which has three outputs signals; alarm trip and thermal state measurement. The thermal state measurement is made available in one of the *MEASUREMENTS* columns.

The thermal state can be reset by either a digital signal (Opto, GOOSE, InterMiCOM), if assigned to this function using programmable scheme logic or the HMI panel menu.

14.7.5 APPLICATION NOTES

14.7.5.1 SETTING GUIDELINES FOR DUAL TIME CONSTANT CHARACTERISTIC

The easiest way of solving the dual time constant thermal equation is to express the current in terms of time and to use a spreadsheet to calculate the current for a series of increasing operating times using the following equation, then plotting a graph.

$$I = \sqrt{\frac{0.4I_p^{\,2}.e^{(-t/\tau 1)} + 0.6I_p^{\,2}.e^{(-t/\tau 2)} - k^2.I_{FLC}^{\,2}}{0.4e^{(-t/\tau 1)} + 0.6e^{(-t/\tau 2)} - 1}}$$

	A	B	C	D	E	F
1						
2	**Time constant 1 =**		**300**	seconds		
3	**Time constant 2 =**		**7200**	seconds		
4	**Pre-overload current Ip =**		**0.9**	per unit		
5	**Full load current =**		**1**	Amps		
6						
7	**OP Time (t)**	**Overload current (I)**				
8	1	14.40852032				
9	1.5	11.7805774				
10	2	10.21617905				
11	2.5	9.150045407				
12	3	8.364131776				
13	3.5	7.754150044				
14	4	7.263123888				
15	4.5	6.856949012				

Figures based on equation

E00728

Figure 318: Spreadsheet calculation for dual time constant thermal characteristic

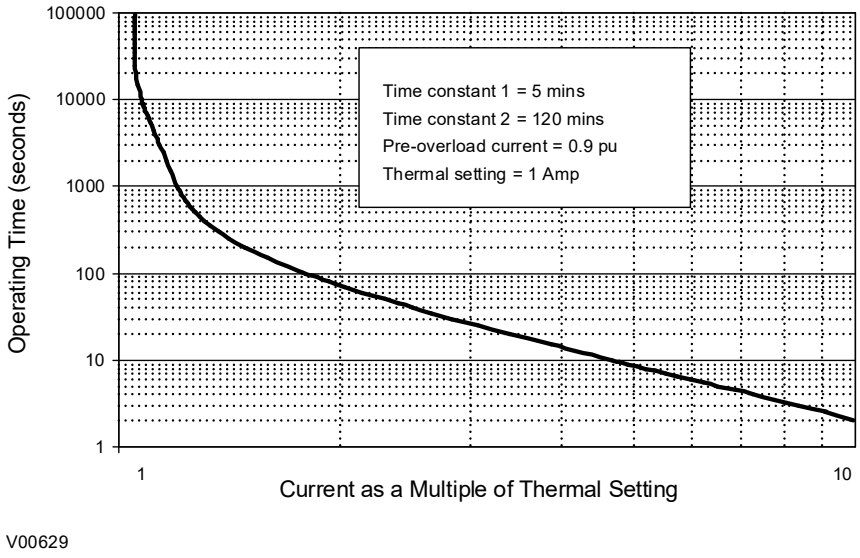


Figure 319: Dual time constant thermal characteristic

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the transformer item/CT ratio.

For an oil-filled transformer with rating 400 to 1600 kVA, the approximate time constants are:

- τ_1 = 5 minutes
- τ_2 = 120 minutes

An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be "Thermal Alarm" = 70% of thermal capacity.

Note:
The thermal time constants given in the above tables are typical only. Reference should always be made to the plant manufacturer for accurate information.

14.7.5.2 SETTING GUIDELINES FOR SINGLE TIME CONSTANT CHARACTERISTIC

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from hot or cold.

The thermal time constant characteristic may be rewritten as:

$$e^{(-t/\tau)} = \left[\frac{\theta - \theta_p}{\theta - 1}\right]$$

where:

- θ = thermal state = $I^2/K^2I_{FLC}^2$
- θ_p = pre-fault thermal state = $I_p^2/K^2I_{FLC}^2$
- I_p is the pre-fault thermal state
- I_{FLC} is the full load current

Note:
A current of 105%Is (KI_{FLC}) has to be applied for several time constants to cause a thermal state measurement of 100%.

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

The following tables show the approximate time constant in minutes, for different cable rated voltages with various conductor cross-sectional areas, and other plant equipment.

Area mm^2	6 - 11kV	22 kV	33 kV	66 kV
25 - 50	10 minutes	15 minutes	40 minutes	–
70 - 120	15 minutes	25 minutes	40 minutes	60 minutes
150	25 minutes	40 minutes	40 minutes	60 minutes
185	25 minutes	40 minutes	60 minutes	60 minutes
240	40 minutes	40 minutes	60 minutes	60 minutes
300	40 minutes	60 minutes	60 minutes	90 minutes

Plant Type	Time Constant (Minutes)
Dry-type transformer <400 kVA	40
Dry-type transformers 400 - 800 kVA	60 - 90
Air-core reactors	40
Capacitor banks	10
Overhead lines with cross section > 100 mm^2	10
Overhead lines	10
Busbars	60

14.8 BROKEN CONDUCTOR PROTECTION

One type of unbalanced fault is the 'Series' or 'Open Circuit' fault. This type of fault can arise from, among other things, broken conductors. Series faults do not cause an increase in phase current and so cannot be detected by overcurrent protection. However, they do produce an imbalance, resulting in negative phase sequence current, which can be detected.

It is possible to apply a negative phase sequence overcurrent element to detect broken conductors. However, on a lightly loaded line, the negative sequence current resulting from a series fault condition may be very close to, or less than, the full load steady state imbalance arising from CT errors and load imbalances, making it very difficult to distinguish. A regular negative sequence element would therefore not work at low load levels. To overcome this, the device incorporates a special Broken Conductor protection element.

The Broken Conductor element measures the ratio of negative to positive phase sequence current (I2/I1). This ratio is approximately constant with variations in load current, therefore making it more sensitive to series faults than standard negative sequence protection.

14.8.1 BROKEN CONDUCTOR PROTECTION IMPLEMENTATION

Broken Conductor protection is implemented in the *BROKEN CONDUCTOR* column of the relevant settings group.

This column contains the settings to enable the function, for the pickup threshold and the time delay.

14.8.2 BROKEN CONDUCTOR PROTECTION LOGIC

The ratio of I_2/I_1 is calculated and compared with the threshold setting. If the threshold is exceeded, the delay timer is initiated. The CTS block signal is used to block the operation of the delay timer.

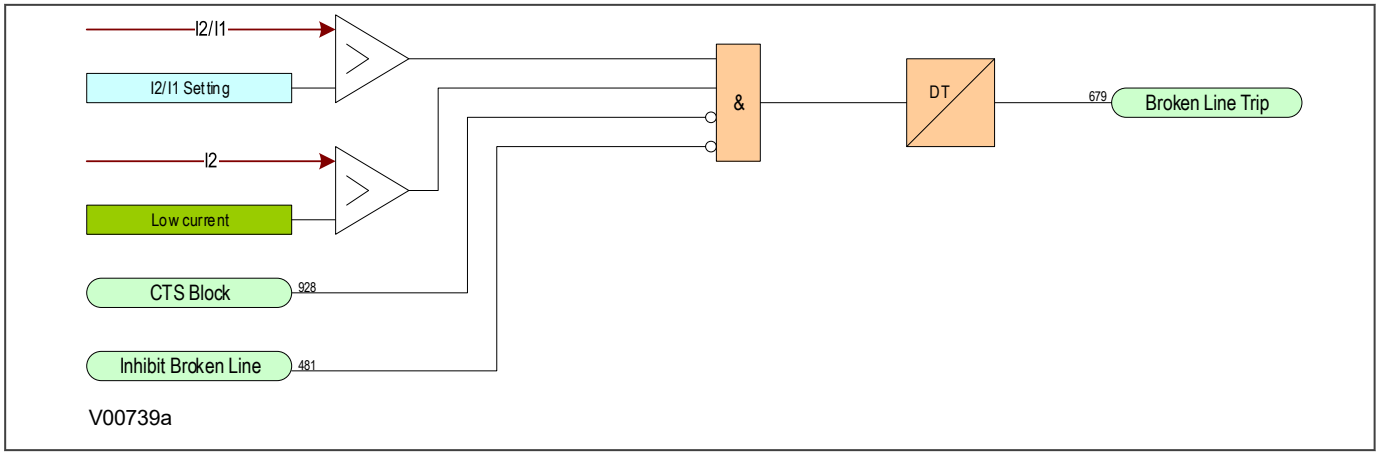


Figure 320: Broken conductor logic

14.8.3 APPLICATION NOTES

14.8.3.1 SETTING GUIDELINES

For a broken conductor affecting a single point earthed power system, there will be little zero sequence current flow and the ratio of I_2/I_1 that flows in the protected circuit will approach 100%. In the case of a multiple earthed power system (assuming equal impedance's in each sequence network), the ratio I_2/I_1 will be 50%.

In practise, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for.

Note:
A minimum value of 8% negative phase sequence current is required for successful operation.

Since sensitive settings have been employed, we can expect that the element will operate for any unbalanced condition occurring on the system (for example, during a single pole autoreclose cycle). For this reason, a long time delay is necessary to ensure co-ordination with other protection devices. A 60 second time delay setting may be typical.

The following example was recorded by an IED during commissioning:

$$I_{\text{full load}} = 500\text{A}$$

$$I_2 = 50\text{A}$$

therefore the quiescent I_2/I_1 ratio = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical: Therefore set:

$$I_2/I_1 = 0.2$$

In a double circuit (parallel line) application, using a 40% setting will ensure that the broken conductor protection will operate only for the circuit that is affected. A setting of 0.4 results in no pick-up for the parallel healthy circuit.

Set I_2/I_1 Time Delay = 60 s to allow adequate time for short circuit fault clearance by time delayed protections.

14.9 TRANSIENT EARTH FAULT DETECTION

Some distribution systems run completely insulated from earth. Such systems are called unearthed systems. The advantage of an unearthed system is that a single phase to earth fault does not cause an earth fault current to flow. This means the whole system remains operational and the supply is not interrupted. The system must be designed to withstand high transient and steady state overvoltages, however, and so its use is generally restricted to low and medium voltage distribution systems.

When there is an earth fault in an unearthed 3-phase system, the voltage of the faulted phase is reduced to the earth potential. This causes the phase voltage in the other two phases to increase, which causes a significant charging current between the phase-to-earth capacitances. This can cause arcing at the fault location. Many systems use a Petersen coil to compensate for this, thus eliminating the arcing problem. Such systems are called compensated networks. The network is earthed with an inductive reactor, where its reactance is made nominally equal to the total system capacitance to earth. Under this condition, a single-phase earth fault does not result in any steady state earth fault current.

The introduction of a Petersen coil introduces major difficulties when it comes to determining the direction of the fault. This is because the faulted line current is the sum of the inductive current introduced by the Petersen coil and the capacitive current of the line, which are in anti-phase with each other. If they are equal in magnitude, the current in the faulted line is zero. If the inductive current is larger than capacitance current, the direction of the faulted line current will appear to be in the same direction as that of the healthy line.

Standard directionalising techniques used by conventional feeder protection devices are not adequate for this scenario, therefore we need a different method for determining the direction of the fault. Two commonly used methods are the First Half Wave method and the Residual Active Power method.

First half wave method

The initial transient wave, generated at the fault point travels towards the bus along the faulted line, until it reaches the healthy line. For forward faults the high frequency fault voltage and current components are in opposite directions during the first half wave, whereas for reverse faults, they are in phase. This fact can be used to determine the fault direction. This method, however, is subject to the following disadvantages:

- The time duration of the characteristic is very short, in most cases not more than 3 ms. Because of this, it requires a high sampling frequency (3000Hz or even higher)
- It requires an analogue high pass filter, necessitating special hardware
- It is affected by the fault inception angle. For example, when the fault inception angle is 0°, there are no initial travelling waves.

Residual active power method

Residual Active power, which is sometimes used to detect the instance of a fault can also in some cases be used for detecting the fault direction. Although the capacitive currents can be compensated by an inductive current generated by a Petersen coil, the active (instantaneous) current can never be compensated for and this is still opposite to that of the healthy line. This fact can also be used to directionalise the fault.

For a forward directional fault, the zero-sequence active power is the power loss of Petersen’s coil, which is negative. For a reverse fault, the zero-sequence active power is the power loss of the transmission line, which is positive. This method, however, is subject to the following disadvantages:

- The zero-sequence active power will be very small in magnitude for a reverse directional fault. Its value depends on the power loss of transmission line.
- The zero-sequence active power may be too small in magnitude to be detected for a forward directional fault. Its value depends on the power loss of Petersen coil.
- High resolution CTs are required

Due to the low magnitude of measured values, reliability is compromised

This product does not use the above techniques for directionalisation. This product uses an innovative patented technique called Transient Reactive Power method to determine the fault direction of an earth fault in a compensated network.

14.9.1 TRANSIENT EARTH FAULT DETECTION IMPLEMENTATION

Transient Earth Fault Detection (TEFD) in this device comprises three modules:

- Transient Earth Fault Detection module (TEF)
- Fault Type Detector (FTD)
- Direction Detector (DD)

> *Note:*
> *In this product, TEFD is implemented for 50Hz only.*

14.9.1.1 TRANSIENT EARTH FAULT DETECTOR

To establish if there is an earth fault on the system somewhere is straightforward. A simple residual overvoltage comparison can determine this. Therefore, a ***TEF> Start*** signal is produced by comparing the neutral voltage with a threshold voltage set by ***TEF VN> Start*** in the *TEF DETECTION* column. The difficulty comes with establishing the type of fault and its direction.

14.9.1.2 FAULT TYPE DETECTOR

The FTD uses a Fundamental analysis (FA) technique to establish whether the fault is an intermittent fault or a steady state faults. For Transient Earth Fault Detection, the detector counts the Residual Voltage bursts within a specified time window. With some clever signal processing the detector module creates pulses by comparing the bursts with a settable threshold, then counts these pulses. If the number of pulses equals or exceeds the number specified by the ***FTD> Fault Count*** setting, within the time window specified by ***FTD> Time Window***, the fault is deemed to be intermittent and the ***TEF> Intermit DDB*** signal is asserted. If there are fewer pulses than this number, this indicates either a disturbance or a permanent fault. To establish which, we need to look at the RMS value of the residual voltage.

If there are fewer pulses than specified and the RMS value does not drop below setting within the specified time window, the fault is deemed to be permanent. In this case the ***TEF> Steady*** DDB signal is asserted.

If there are fewer pulses than specified and the RMS value does drop below setting, this indicates that a disturbance has been detected but it is not a fault. In this case, the ***TEF> Steady*** DDB signal is not asserted.

The user can map the signals ***TEF>Steady***, ***TEF>Intermit***, ***TEF>DIR FWD*** or ***TEF> DIR REV*** to the TEF Alarm Logic DDB to generate a TEF Alarm.

The inputs to this module are:

- The residual voltage
- ***FTD> VN*** (defines the threshold which converts the residual voltage burst into a pulse
- ***FTD> Time Window*** (defines the time window - default is 2 seconds)
- ***FTD> Fault Count*** (defines the fault count)

The FTD outputs two signals to indicate whether the fault is steady state or intermittent.

14.9.1.3 DIRECTION DETECTOR

The Direction Detector (DD) uses a patented technique based on Transient Reactive Power (TRP) to establish the direction of the fault. Unlike traditional methods, this TRP method does not require high resolution CTs or special analogue filtering hardware and is therefore cheaper to implement.

It can be shown that the residual voltage and residual current components can be reliably used as discriminative criteria between a faulty and healthy feeder at 220Hz.

The admittance response of a healthy distributed feeder is shown below using a Pi model:

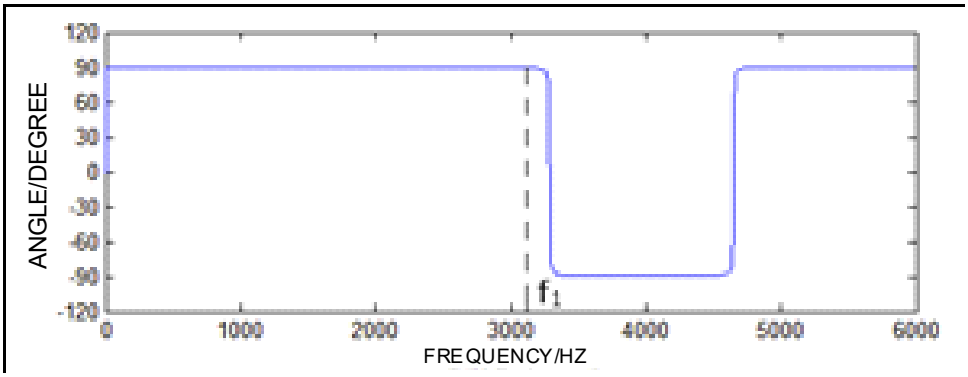


Figure 321: Healthy line response

In the above figure, the phase response of the admittance is consistent at 90o up to frequency f1 (approximately 3000Hz). For a compensated faulty feeder, the admittance response is shown below using a Pi model:

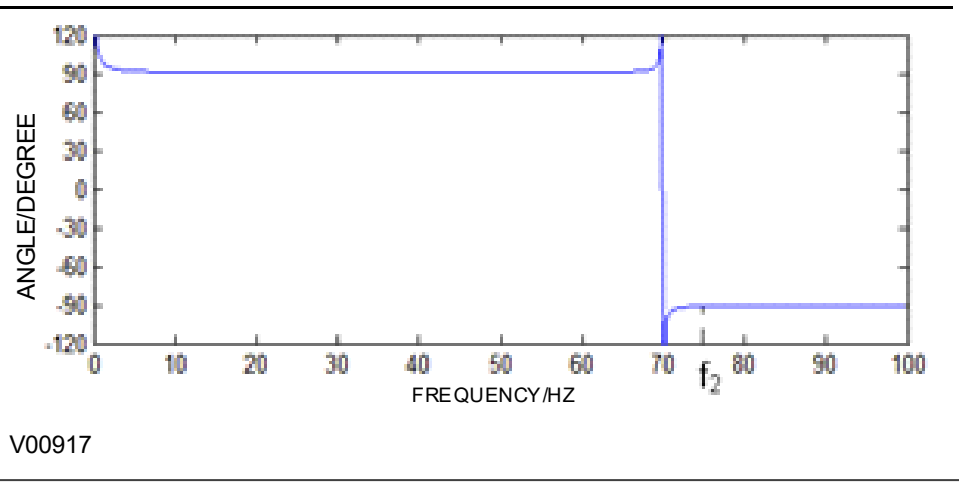


Figure 322: Faulty line response

We can observe that the phase angle (and thus, the reactive power flow) changes from 90o to -90o at frequencies higher than f2. Based on the above, we have clear direction discrimination between a healthy and faulted feeder at any frequency between f2 and f1 approximately.

> *Note:*
> *The resonant frequency in the above system is 70Hz. For a perfectly compensated system, this will be 50Hz.*

MiCOM devices use an anti-aliasing band pass filter with cut-off frequency of 150Hz. Furthermore, at 220Hz the post-filter magnitude is approximately 0.5pu, and at 330Hz, it is less than 0.2pu. To avoid any integer harmonics, and to avoid severely attenuated quantities due to the filter, we have chosen 220Hz as the most suitable frequency for direction determination.

In the forward direction, the residual voltage leads the residual current by 90°, and in the reverse direction the residual voltage lags the residual current by 90°. These criteria can be used to directionalise the fault.

The residual voltage (Vres) after passing through the bandpass filter tuned to 220 Hz, has 90° added to its phase. The residual current (Ires) is also passed through a 220 Hz bandpass filter, but no phase shift is applied. The resulting components which we shall call VH1 and IH2 are therefore in antiphase with each other for forward faults and in phase if the forward line is not faulted.

The VH1 and IH2 components are passed through a sign filter and multiplied to create a reactive power component in the range of -1 to +1. This is the transient reactive power Q_{tran}. If $Q_{tran} > 0$, then there forward line is healthy. If $Q_{tran} < 0$, then the forward line is faulty.

There are two modes of operation for the direction detector; Standard and Advanced. Standard mode is used in most cases and is described here. Advanced mode is for special applications that deviate from the standard model of two or more geographically close feeders outgoing from a power transformer. The following default settings are recommended for majority of applications:

- Dir>Vnf Thresh 8.000 V
- Dir>Inf Thresh 50.00 mA
- Dir>Qn Thresh 100.0e-3
- Dir>Qr Thresh 40.00e-3

When ***TEF>Dir Mod*** is set to ***Advance***, the following settings become visible:

- ***Dir>Qs Thresh*** 50.00e-3
- ***Qn Smooth fct*** 20.00e-3
- ***Operate.Cycles*** 6

Here, Qs is an integration of Q_n, with the window of integration being the first ***Operate cycles*** setting after the start signal is triggered. Q_s is used as a further discriminative directional feature if direction cannot be determined by Q_n only. Q_S is calculated by the following formula:

$$Q_S = \int_{(t=0)}^{(t=K*T)} (Q_{N(t)})$$

Where ‘K’ is the setting Operate Cycles. Operate Cycles affects Qs only.

Qn Smooth fact is a smoothing factor for consecutive Qn values which prevents sudden changes in the value of Qn. The calculated new value of Qn is:

new_valueQn = old_value*(1-smoothing_factor)+ new_value*smoothing_factor.

It is important to note that all settings for the TGFD function, including those at 220Hz, can be set based on 50Hz nominal secondary values. This is because the gain of the 220Hz transient filter is 1.

The inputs to this module are:

- The residual voltage
- The residual current
- ***Dir> Vnf Thresh*** (defines the threshold for the residual voltage sign filter).
- ***Dir> Inf Thresh*** (defines the threshold for the residual current sign filter

The DD outputs two signals to indicate a forward fault and a reverse fault

Sign filter thresholds

The ***Dir> Vnf Thresh*** setting is used to get the sign of instantaneous voltage value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

The ***Dir> Inf Thresh*** setting is used to get the sign of instantaneous current value by sign filter. If the input value is larger than Vnf, the output is +1. If the input value is less than -1*Vnf, the output is -1. Otherwise the output is 0.

Q_{tran} thresholds

The setting ***Dir>Qn Thresh*** is the forward direction Q_{tran} threshold calculated from the quantised Vnf and Inf values.

The setting ***Dir>Qr*** is the reverse direction Q_{trans} threshold calculated from the quantised Vnf and Inf values.

The following DDBs are also available:

Timer Block: used to inhibit the TEF function and reset all associated DDBs

Reset TEF: can be configured as a user-defined manual reset alarms

TEF Alarm Output: This is the main TEF alarm that can be mapped to a relay output for a trip

14.9.2 TRANSIENT EARTH FAULT DETECTION LOGIC

14.9.2.1 TRANSIENT EARTH FAULT DETECTION LOGIC OVERVIEW

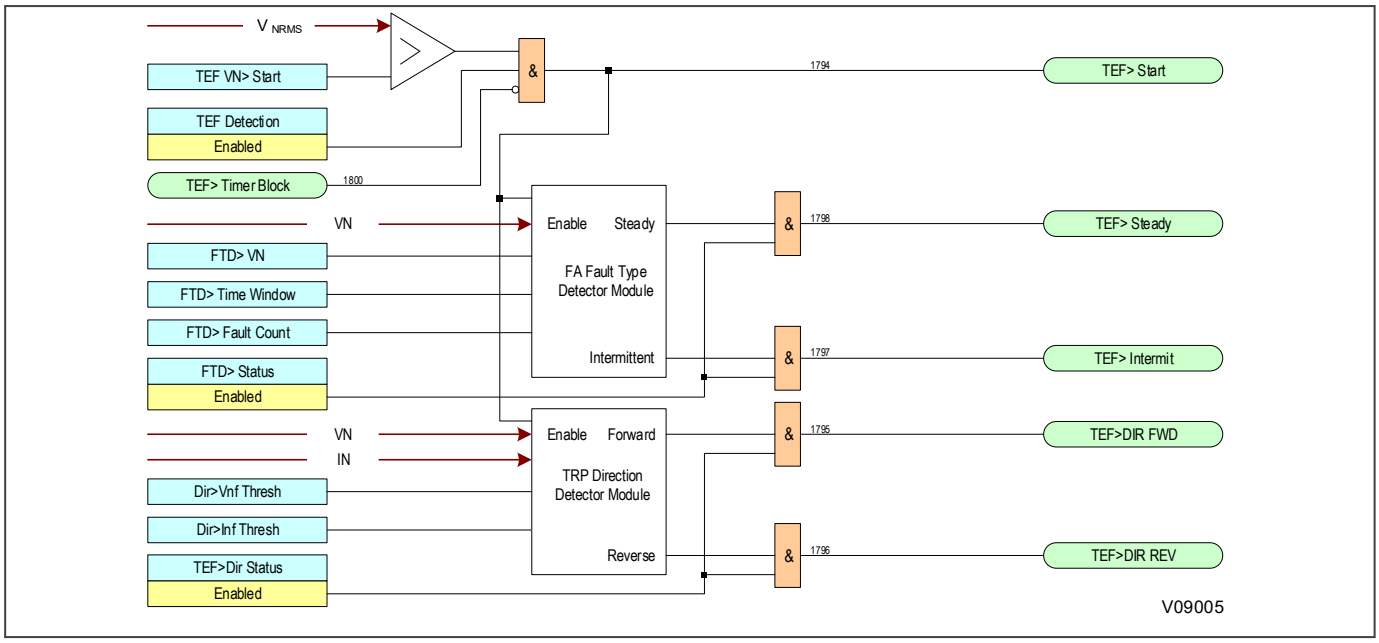


Figure 323: Transient earth fault logic overview

14.9.2.2 FAULT TYPE DETECTOR LOGIC

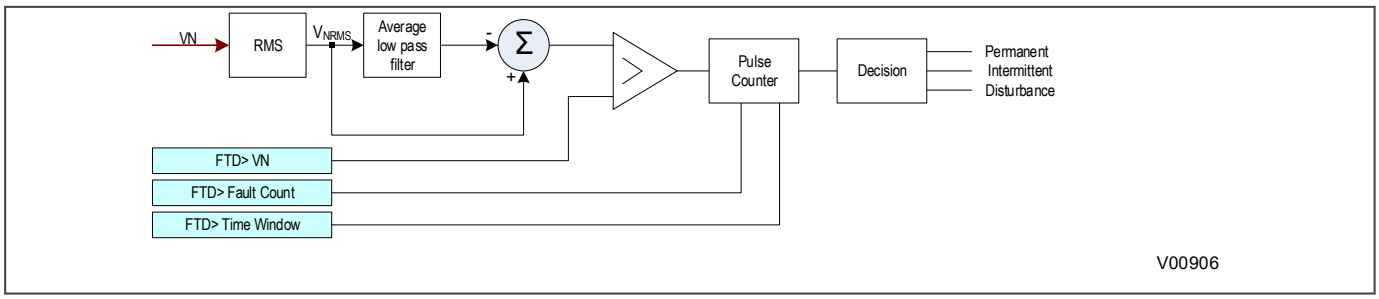


Figure 324: Fault type detector logic

14.9.2.3 DIRECTION DETECTOR LOGIC - STANDARD MODE

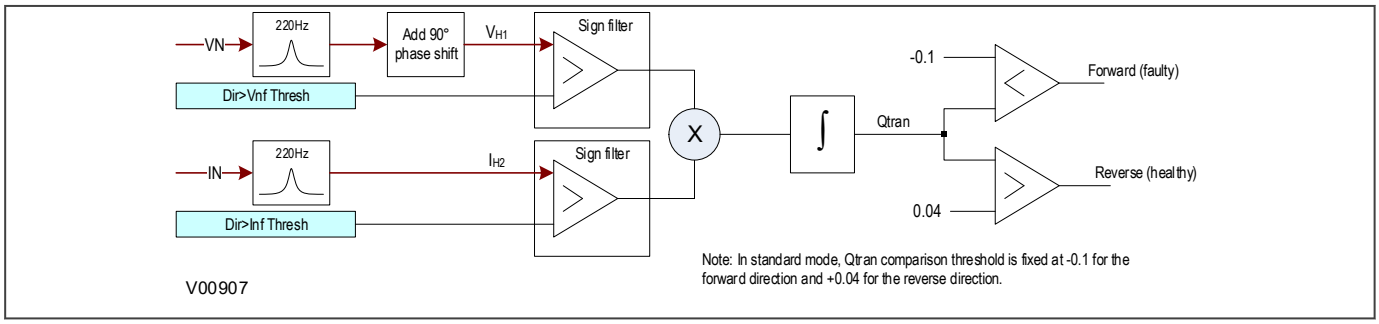


Figure 325: Direction detector logic - standard mode

14.9.2.4 TRANSIENT EARTH FAULT DETECTION OUTPUT ALARM LOGIC

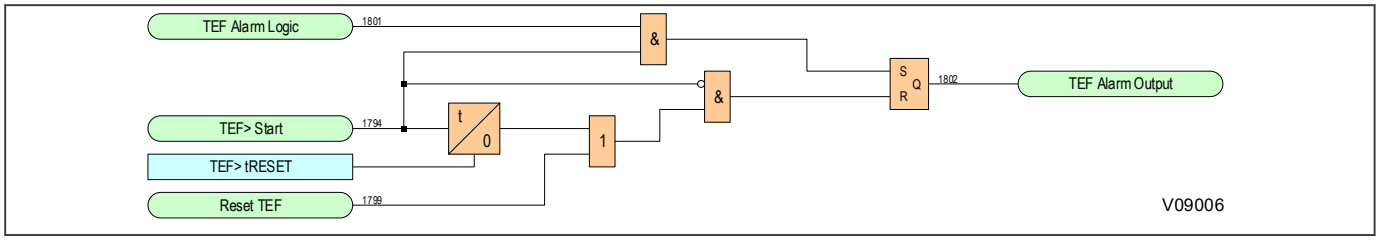


Figure 326: TEFD output alarm logic

14.9.2.5 APPLICATION NOTES

14.9.2.5.1 TRANSIENT EARTH FAULT DETECTION: ACTIVE POWER CHECK

A preventive measure should be taken in cases when devices are located at the extremities of a radial system, where the charging current component reduces the further the device is from the source, and the active component remains small but constant. In these cases, the transient active current component can be comparable to the transient reactive current during the directional check of the TEFD algorithm.

To ensure correct directionality for all fault positions and system configurations (radial, ring or meshed), the TEFD algorithm shall be supplemented with an additional element - 'Active Power Check'. This scheme ensures the correct directional decision is raised regardless of residual active power levels present in the system at the time of the fault. Sensitive Directional Earth Fault (SDEF) with Active Power Check shall be applied in parallel with the TEFD algorithm.

The combined logic for the TEFD and SDEF is shown in Figure below. A 'Forward START' (shown as a name modified User Alarm) signal is raised when either TEFD FWD or SDEF FWD signals are active. However, 'Forward START' is inhibited if the SDEF REV signal is ever active. This ensures SDEF takes priority if there is enough residual active power during a fault condition. For cases where the residual active power is low, the TEFD algorithm provides the directional decision.

An additional 100ms delay is included to delay the start conditions, thus ensuring the SDEF protection is not adversely affected by the initial fault transient. The TEFD logic is unaffected by the additional timer as its directional decision is latched for a minimum of 200ms after fault inception.

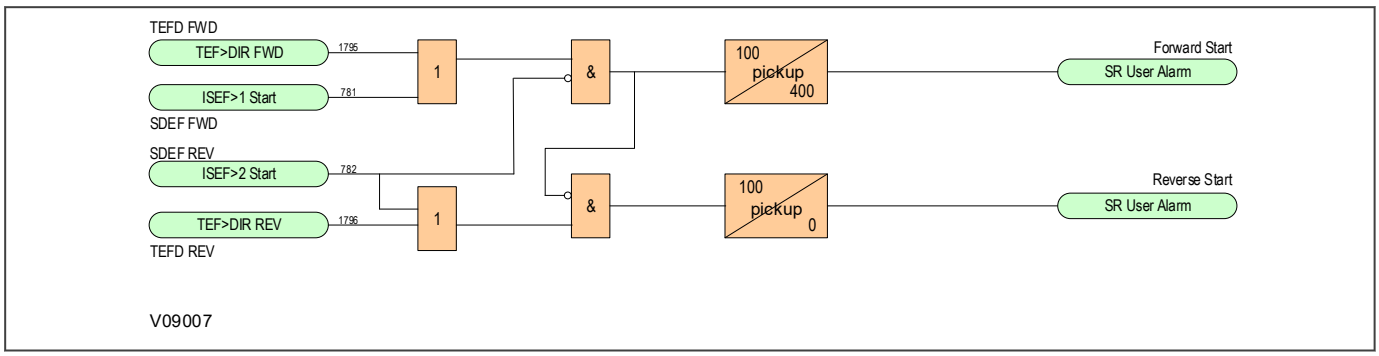


Figure 327: Combined TEFD and SDEF start PSL logic

CHAPTER 15

VOLTAGE PROTECTION FUNCTIONS

15.1 CHAPTER OVERVIEW

The device provides a wide range of voltage protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 492
Undervoltage Protection 493
Overvoltage Protection 496
Compensated Overvoltage 499
Residual Overvoltage Protection 501

15.2 UNDERVOLTAGE PROTECTION

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Undervoltage conditions can be related to increased loads, whereby the supply voltage will decrease in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an undervoltage condition, which must be cleared.
- If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping by means of an undervoltage element is required.
- Faults occurring on the power system result in a reduction in voltage of the faulty phases. The proportion by which the voltage decreases is dependent on the type of fault, method of system earthing and its location. Consequently, co-ordination with other voltage and current-based protection devices is essential in order to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be necessary to isolate each of the outgoing circuits, such that when supply voltage is restored, the load is not connected. Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This can be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions that last longer than a pre-determined time.

15.2.1 UNDERVOLTAGE PROTECTION IMPLEMENTATION

Undervoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Undervoltage parameters are contained within the sub-heading *UNDERVOLTAGE*.

The product provides two stages of Undervoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V<1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage (***V<(n) Voltage Set***)

The undervoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V< Measur't Mode*** cell.

There is no Timer Hold facility for Undervoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V<2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V< Operate Mode*** cell for each stage.

15.2.2 UNDERVOLTAGE PROTECTION LOGIC

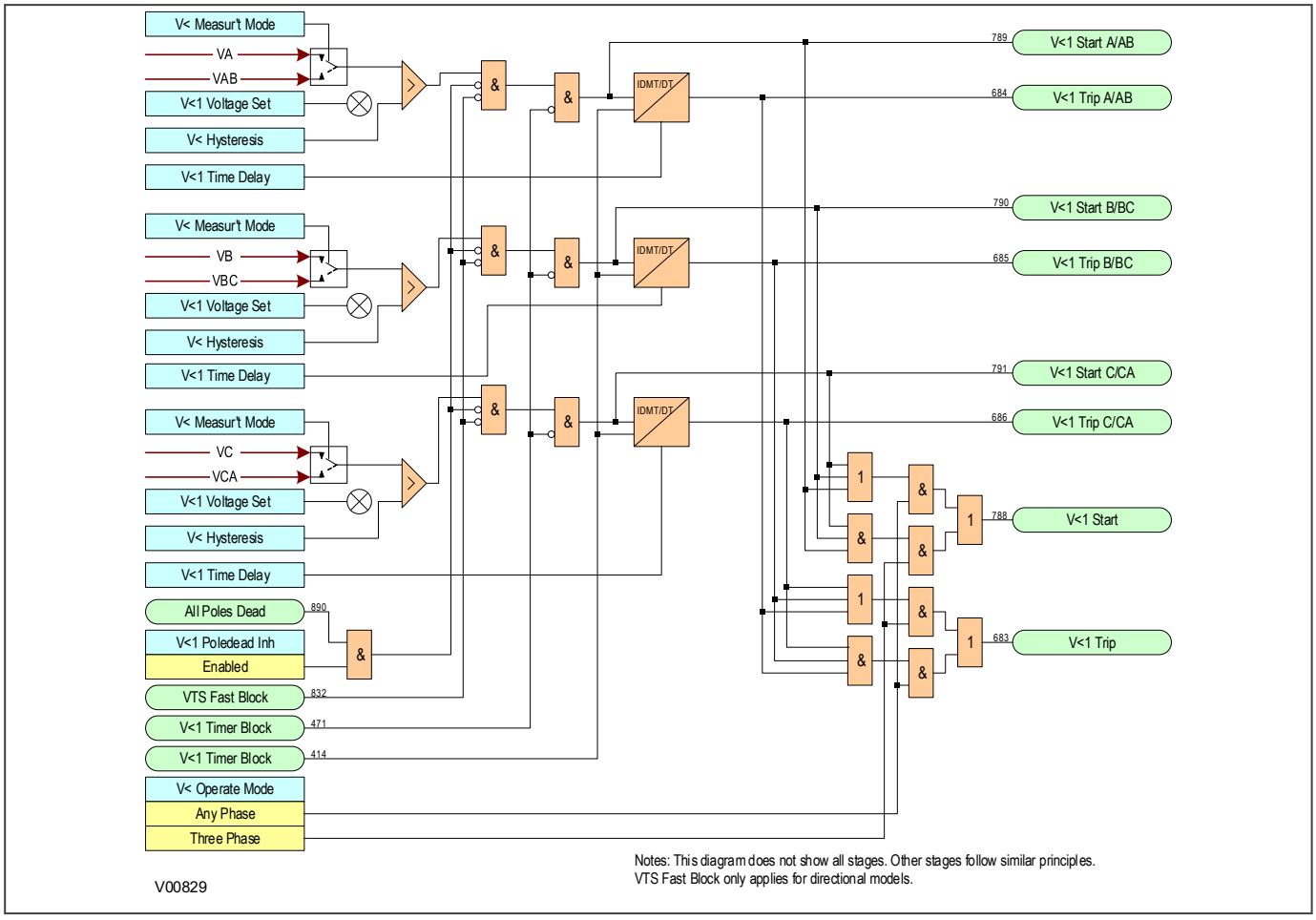


Figure 328: Undervoltage - single and three phase tripping mode (single stage)

The Undervoltage protection function detects when the voltage magnitude for a certain stage falls short of a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal and an ***All Poles Dead*** signal. This ***Start*** signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the undervoltage timer block signal (***V<(n) Timer Block***). For each stage, there are three Phase undervoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V<(n) Start***), which can be be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V< Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V< Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

In some cases, we do not want the undervoltage element to trip; for example, when the protected feeder is de-energised, or the circuit breaker is opened, an undervoltage condition would obviously be detected, but we would not want to start protection. To cater for this, an ***All Poles Dead*** signal blocks the ***Start*** signal for each phase. This is controlled by the ***V<Poledead Inh*** cell, which is included for each of the stages. If the cell is enabled, the relevant stage will be blocked by the integrated pole dead logic. This logic produces an output when it detects either an open circuit breaker via auxiliary contacts feeding the opto-inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***V< Hysteresis*** setting. For example, where the ***V<Hysteresis*** default setting is *2*, relay pick-up will be at set voltage and drop-off will be at 102% of set voltage.

15.2.3 APPLICATION NOTES

15.2.3.1 UNDERVOLTAGE SETTING GUIDELINES

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case you should select phase-to-phase voltage measurement, as this quantity is less affected by single-phase voltage dips due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependent on the system in question but typical healthy system voltage excursions may be in the order of 10% of nominal value.

The same applies to the time setting. The required time delay is dependent on the time for which the system is able to withstand a reduced voltage.

If motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

15.3 OVERVOLTAGE PROTECTION

Overvoltage conditions are generally related to loss of load conditions, whereby the supply voltage increases in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an overvoltage condition which must be cleared.

Note:
During earth fault conditions on a power system there may be an increase in the healthy phase voltages. Ideally, the system should be designed to withstand such overvoltages for a defined period of time.

15.3.1 OVERVOLTAGE PROTECTION IMPLEMENTATION

Overvoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Overvoltage parameters are contained within the sub-heading *OVERVOLTAGE*.

The product provides two stages of overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V>1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage setting voltage (***V>(n) Voltage Set***)

The overvoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V> Measur't Mode*** cell.

There is no Timer Hold facility for Overvoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V>2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V> Operate Mode*** cell for each stage.

15.3.2 OVERVOLTAGE PROTECTION LOGIC

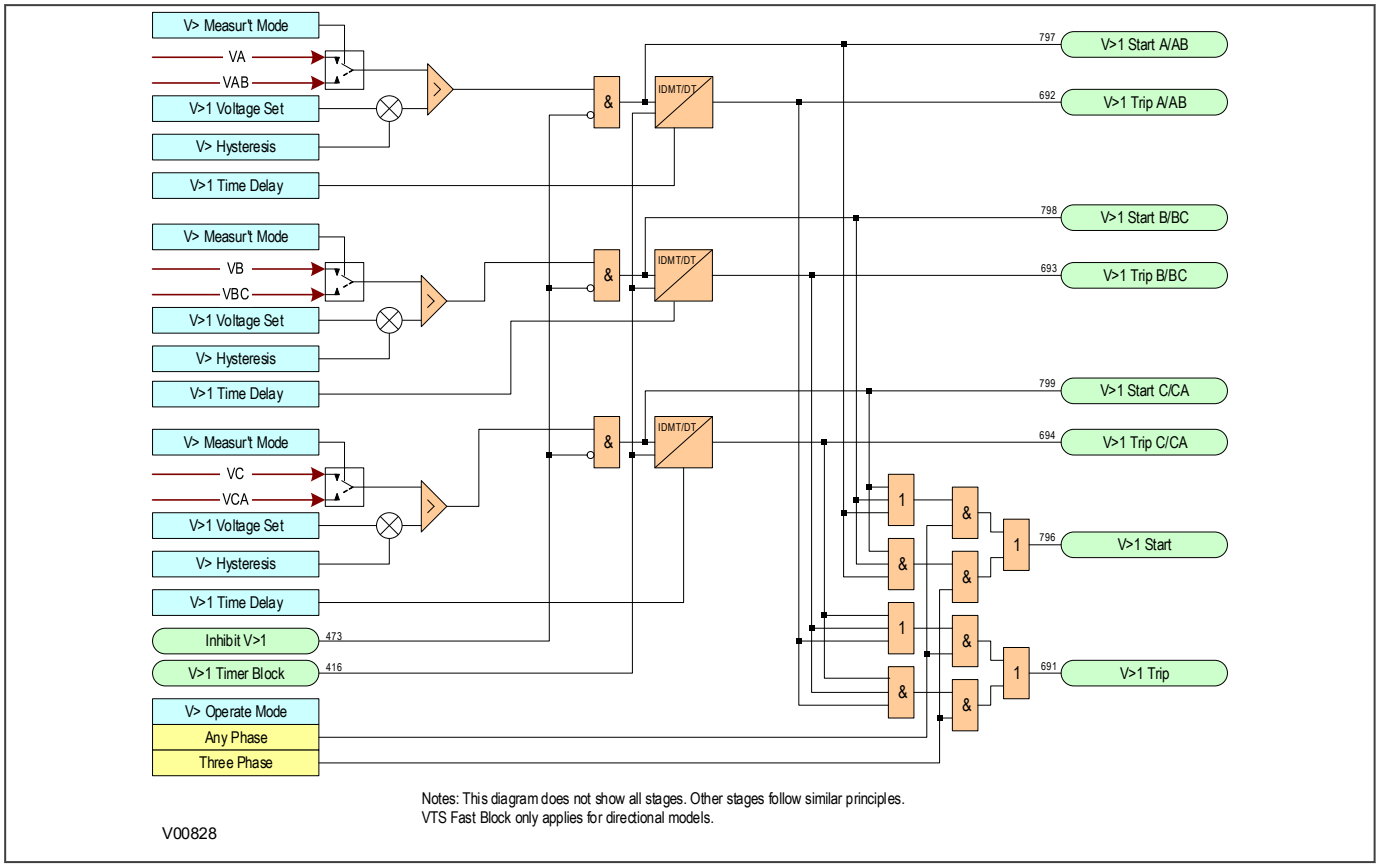


Figure 329: Overvoltage - single and three phase tripping mode (single stage)

The Overvoltage protection function detects when the voltage magnitude for a certain stage exceeds a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal. This start signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the overvoltage timer block signal (***V>(n) Timer Block***). For each stage, there are three Phase overvoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V>(n) Start***), which can then be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V> Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V> Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***V> Hysteresis*** setting. For example, where the ***V>Hysteresis*** default setting is 2, relay pick-up will be at set voltage and drop-off will be at 98% of set voltage.

15.3.3 APPLICATION NOTES

15.3.3.1 OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

15.4 COMPENSATED OVERVOLTAGE

The Compensated Overvoltage function calculates the positive sequence voltage at the remote terminal using the positive sequence local current and voltage and the line impedance and susceptance. This can be used on long transmission lines where Ferranti Overvoltages can develop under remote circuit breaker open conditions.

15.4.1 COMPENSATED OVERVOLTAGE IMPLEMENTATION

The Compensated overvoltage protection function can be set in the *VOLT PROTECTION* column under the sub heading COMP OVERVOLTAGE. The remote voltage is calculated using line impedance settings and the line charging admittance in the *LINE PARAMETERS* column.

The IED uses the [A,B,C,D] transmission line equivalent model given the following parameters:

- Total Impedance Z = $z\angle\theta$ ohms
- Total Susceptance Y = $y\angle -90°$
- Line Length l

The remote voltage is calculated using the following equations:

$$\begin{bmatrix} \bar{V}r \\ \bar{I}r \end{bmatrix} = \begin{bmatrix} D & -C \\ -BA & \end{bmatrix} \times \begin{bmatrix} \bar{V}s \\ \bar{I}s \end{bmatrix}$$

where

- V_r is the voltage at the receiving end
- I_r is the current at the receiving end
- V_s is the measured voltage at the sending end
- I_s is the measured current at the sending end
- A= D = cosh(y.l)
- B = Z_c.sinh(y.l)
- C = Y_c.sinh(y.l)
- y.l = $\sqrt{}$(Z.Y)
- Z_c = 1/Y_c = $\sqrt{}$(Z/Y)
- Y = total line capacitive charging susceptance
- Z_c = characteristic impedance of the line (surge impedance)

There are two stages to provide both alarm and trip stages where required. Both stages can be set independently.

Stage 1 can be set to `IDMT`, `DT` or `Disabled`, in the ***V1>1 Cmp Funct*** cell. Stage 2 is DT only and is enabled or disabled in the ***V1>2 Cmp Status*** cell.

The IDMT characteristic on the first stage is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t =Operating time in seconds
- M = Remote Calculated voltage / IED setting voltage

15.4.2 COMPENSATED OVERVOLTAGE LOGIC

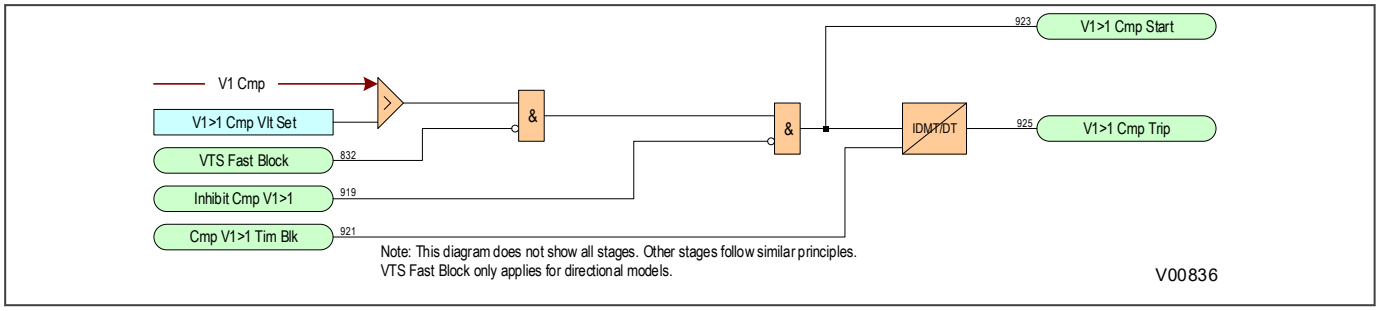


Figure 330: Compensated overvoltage logic

The Compensated Overvoltage module (***V1 Cmp***) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***V1>(n) Cmp Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***V1> (n) Cmp Trip*** signal which is used to drive the tripping output relay.

Voltage drop-off threshold, defined as a percentage of set voltage, may be adjusted via the ***Cp V Hysteresis*** setting. For example, where the ***Cp V Hysteresis*** default setting is *2*, relay pick-up will be at set voltage and drop-off will be at 98% of set voltage.

15.4.3 APPLICATION NOTES

15.4.3.1 COMPENSATED OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

15.5 RESIDUAL OVERVOLTAGE PROTECTION

On a healthy three-phase power system, the sum of the three-phase to earth voltages is nominally zero, as it is the vector sum of three balanced vectors displaced from each other by 120°. However, when an earth fault occurs on the primary system, this balance is upset and a residual voltage is produced. This condition causes a rise in the neutral voltage with respect to earth. Consequently this type of protection is also commonly referred to as 'Neutral Voltage Displacement' or NVD for short.

This residual voltage may be derived (from the phase voltages) or measured (from a measurement class open delta VT). Derived values will normally only be used where the model does not support measured functionality (a dedicated measurement class VT). If a measurement class VT is used to produce a measured Residual Voltage, it cannot be used for other features such as Check Synchronisation.

This offers an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balanced current transformers on each feeder may be either impractical, or uneconomic, or for providing earth fault protection for devices with no current transformers.

15.5.1 RESIDUAL OVERVOLTAGE PROTECTION IMPLEMENTATION

Residual Overvoltage Protection is implemented in the *RESIDUAL O/V NVD* column of the relevant settings group.

Some applications require more than one stage. For example an insulated system may require an alarm stage and a trip stage. It is common in such a case for the system to be designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The product provides two stages of Derived Residual Overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K= Time multiplier setting
- t = Operating time in seconds
- M = Derived residual voltage setting voltage (***VN> Voltage Set***)

You set this using the ***VN>1 Function*** setting.

Stage 1 also provides a Timer Hold facility.

Stage 2 can have definite time characteristics only. This is set in the ***VN>2 status*** cell

The device derives the residual voltage internally from the three-phase voltage inputs supplied from either a 5-limb VT or three single-phase VTs. These types of VT design provide a path for the residual flux and consequently permit the device to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. Three-limb VTs have no path for residual flux and are therefore unsuitable for this type of protection.

15.5.2 RESIDUAL OVERVOLTAGE LOGIC

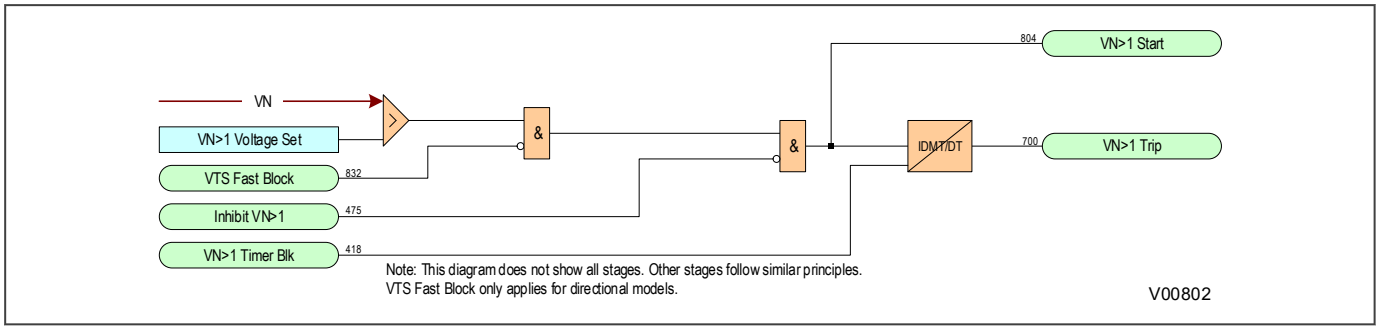


Figure 331: Residual overvoltage logic

The Residual Overvoltage module (VN>) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***VN>(n) Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***VN> (n) Trip*** signal which is used to drive the tripping output relay.

15.5.3 APPLICATION NOTES

15.5.3.1 CALCULATION FOR SOLIDLY EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

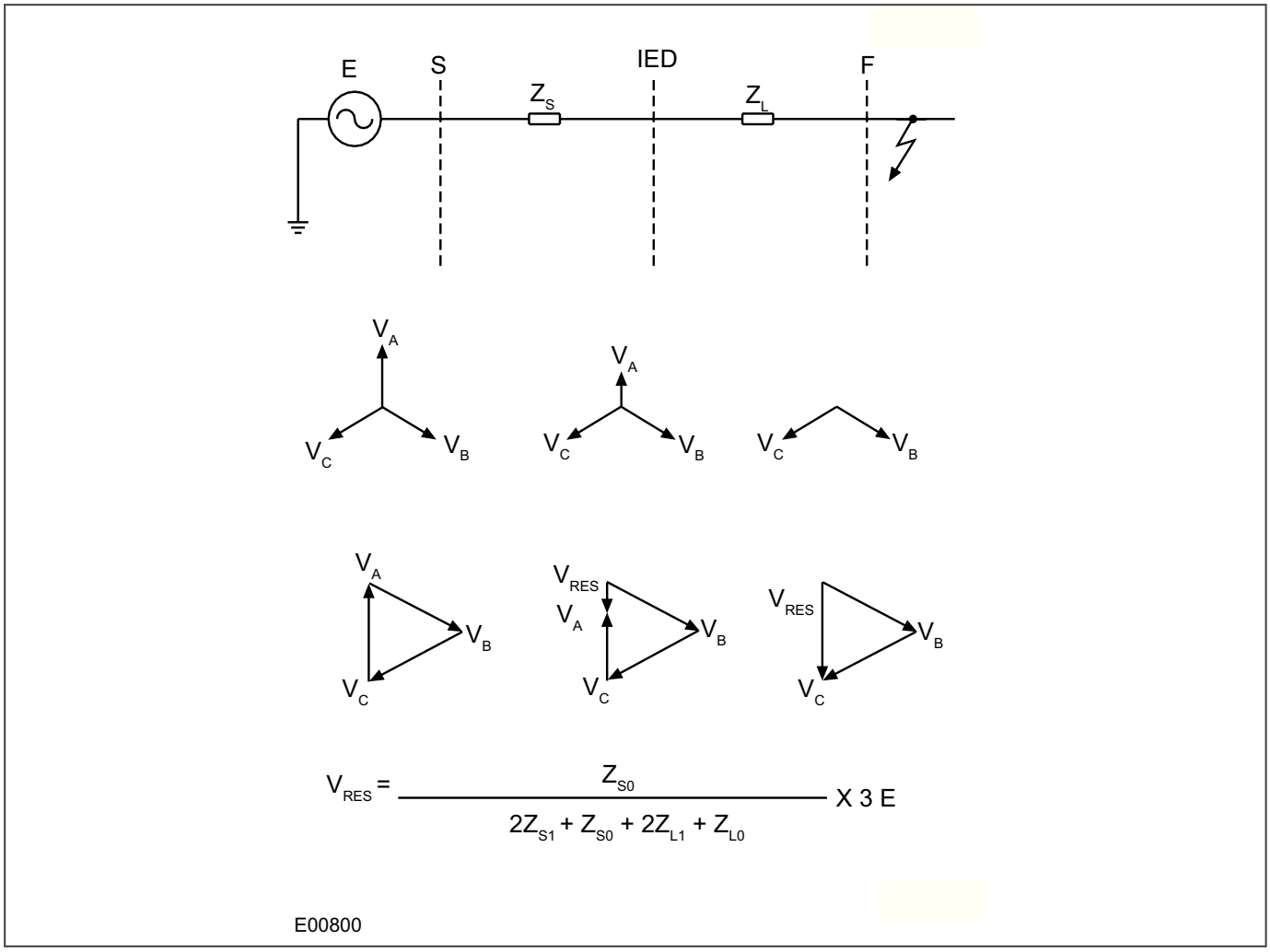


Figure 332: Residual voltage for a solidly earthed system

As can be seen from the above diagram, the residual voltage measured on a solidly earthed system is solely dependent on the ratio of source impedance behind the protection to the line impedance in front of the protection, up to the point of fault. For a remote fault far away, the Z_S/Z_L: ratio will be small, resulting in a correspondingly small residual voltage. Therefore, the protection only operates for faults up to a certain distance along the system. The maximum distance depends on the device setting.

15.5.3.2 CALCULATION FOR IMPEDANCE EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

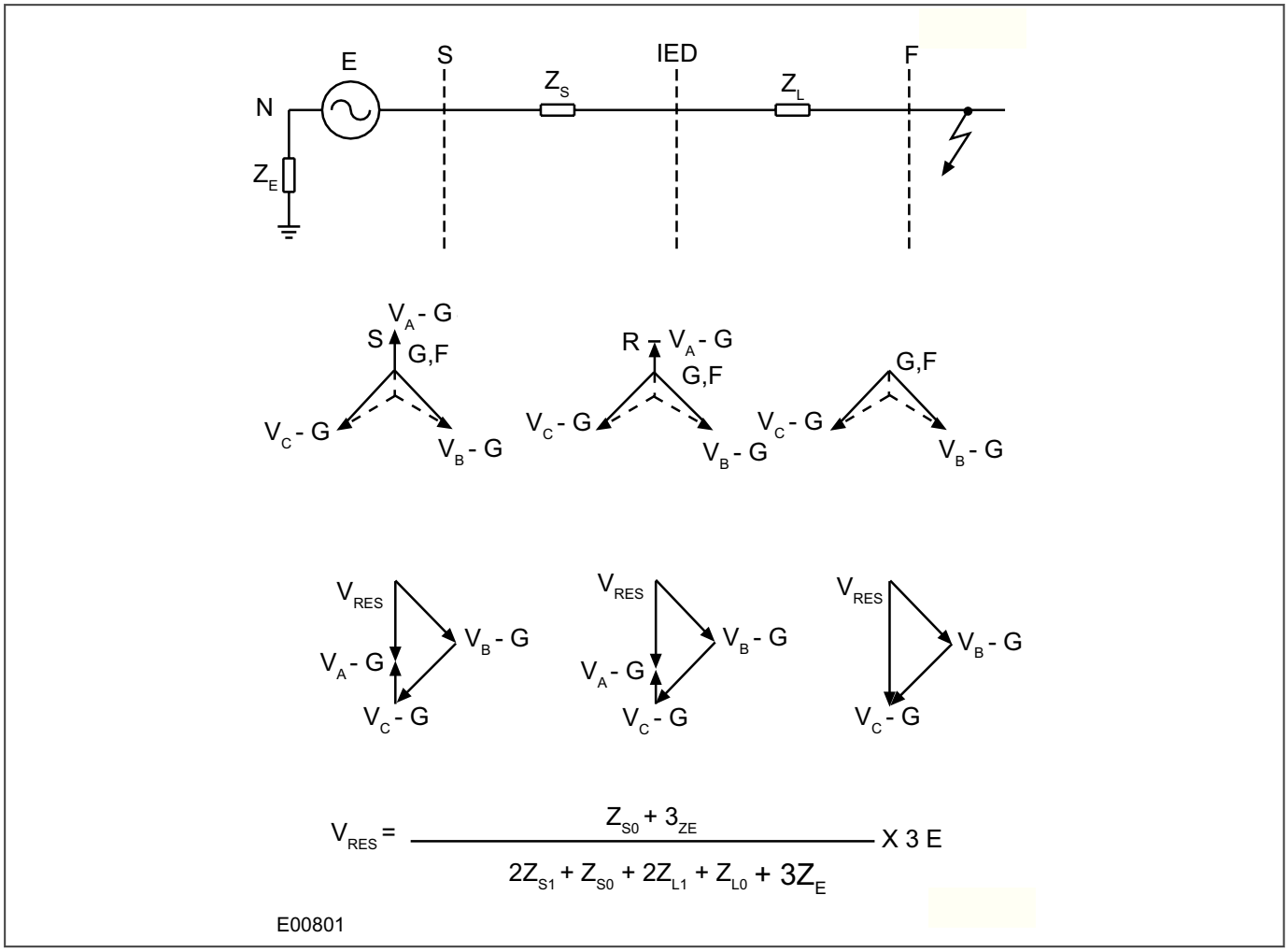


Figure 333: Residual voltage for an impedance earthed system

An impedance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

15.5.3.3 SETTING GUIDELINES

The voltage setting applied to the elements is dependent on the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependent on the method of system earthing employed.

Also, you must ensure that the protection setting is set above any standing level of residual voltage that is present on the system.

CHAPTER 16

FREQUENCY PROTECTION FUNCTIONS

16.1 CHAPTER OVERVIEW

The device provides a range of frequency protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 506

Frequency Protection 507

Independent R.O.C.O.F Protection 510

16.2 FREQUENCY PROTECTION

Power generation and utilisation needs to be well balanced in any industrial, distribution or transmission network. These electrical networks are dynamic entities, with continually varying loads and supplies, which are continually affecting the system frequency. Increased loading reduces the system frequency and generation needs to be increased to maintain the frequency of the supply. Conversely decreased loading increases the system frequency and generation needs to be reduced. Sudden fluctuations in load can cause rapid changes in frequency, which need to be dealt with quickly.

Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse, which has dire consequences.

Normally, generators are rated for a particular band of frequency. Operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken. This type of protection can be used for operator alarms or turbine trips in case of severe frequency decay.

Clearly a range of methods is required to ensure system frequency stability. The frequency protection in this device provides both underfrequency and overfrequency protection.

Frequency Protection is implemented in the *FREQ PROTECTION* column of the relevant settings group.

16.2.1 UNDERFREQUENCY PROTECTION

A reduced system frequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the capacity of the generators in that particular subsystem. Industrial plants that are dependent on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

Many types of industrial loads have limited tolerances on the operating frequency and running speeds (e.g. synchronous motors). Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may damage equipment and even lead to blackouts. It is therefore essential to provide protection for underfrequency conditions.

16.2.1.1 UNDERFREQUENCY PROTECTION IMPLEMENTATION

Simple underfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 4 stages of underfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F<1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F<1 Setting***: defines the frequency pickup setting
- ***F<1 Time Delay***: sets the time delay

16.2.1.2 UNDERFREQUENCY PROTECTION LOGIC

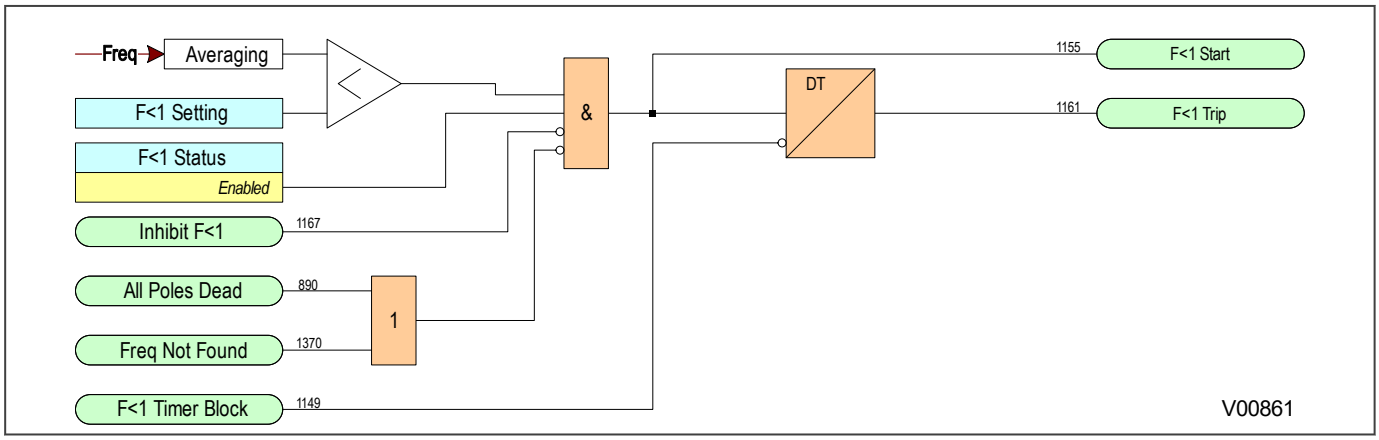


Figure 334: Underfrequency logic (single stage)

If the frequency is below the setting and not blocked the DT timer is started. If the frequency cannot be determined, the function is blocked.

16.2.1.3 APPLICATION NOTES

16.2.1.3.1 SETTING GUIDELINES

In order to minimise the effects of underfrequency, a multi-stage load shedding scheme may be used with the plant loads prioritised and grouped. During an underfrequency condition, the load groups are disconnected sequentially, with the highest priority group being the last one to be disconnected.

The effectiveness of each load shedding stage depends on the proportion of power deficiency it represents. If the load shedding stage is too small compared with the prevailing generation deficiency, then there may be no improvement in the frequency. This should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. These should not be excessive as this could jeopardise system stability. Time delay settings of 5 - 20 s are typical.

The protection function should be set so that declared frequency-time limits for the generating set are not infringed. Typically, a 10% underfrequency condition should be continuously sustainable.

16.2.2 OVERFREQUENCY PROTECTION

An increased system frequency arises when the mechanical power input to a generator exceeds the electrical power output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such conditions, the governor would normally respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Overfrequency protection is required as a backup to cater for cases where the reaction of the control equipment is too slow.

16.2.2.1 OVERFREQUENCY PROTECTION IMPLEMENTATION

Simple overfrequency Protection is configured in the *FREQ PROTECTION* column of the relevant settings group.

The device provides 2 stages of overfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F>1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F>1 Setting***: defines the frequency pickup setting
- ***F>1 Time Delay***: sets the time delay

16.2.2.2 OVERFREQUENCY PROTECTION LOGIC

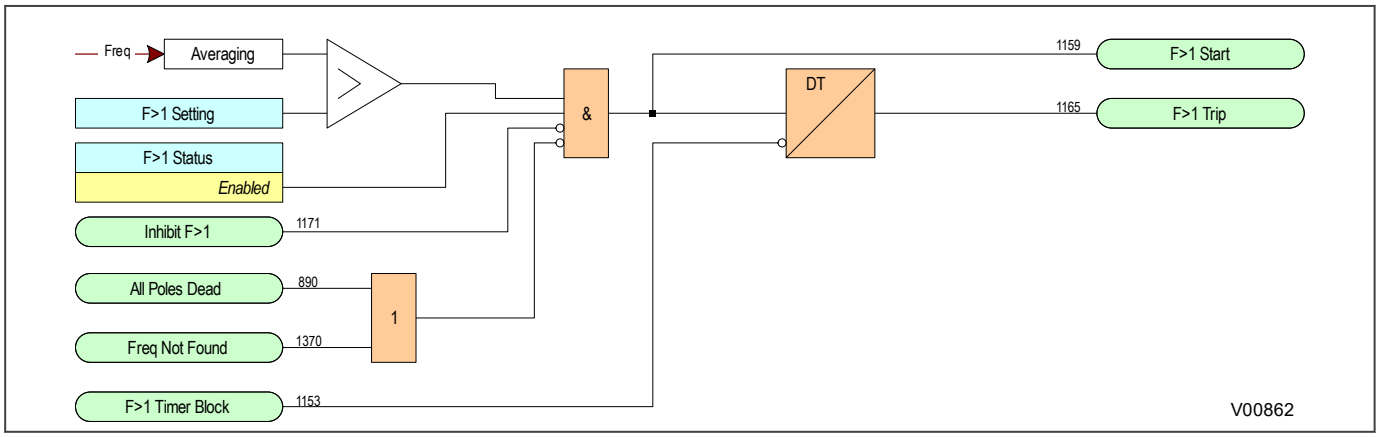


Figure 335: Overfrequency logic (single stage)

If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out, the trip is produced. If the frequency cannot be determined, the function is blocked.

16.2.2.3 APPLICATION NOTES

16.2.2.3.1 SETTING GUIDELINES

Following changes on the network caused by faults or other operational requirements, it is possible that various subsystems will be formed within the power network. It is likely that these subsystems will suffer from a generation/ load imbalance. The "islands" where generation exceeds the existing load will be subject to overfrequency conditions. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element can be suitably set to sense this contingency.

16.3 INDEPENDENT R.O.C.O.F PROTECTION

Where there are very large loads, imbalances may occur that result in rapid decline in system frequency. The situation could be so bad that shedding one or two stages of load is unlikely to stop this rapid frequency decline. In such a situation, standard underfrequency protection will normally have to be supplemented with protection that responds to the rate of change of frequency. An element is therefore required which identifies the high rate of decline of frequency, and adapts the load shedding scheme accordingly.

Such protection can identify frequency variations occurring close to nominal frequency thereby providing early warning of a developing frequency problem. The element can also be used as an alarm to warn operators of unusually high system frequency variations.

16.3.1 INDEPENDENT R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides four independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***df/dt Avg.Cycles*** calculates the rate of change of frequency over a fixed period of several cycles.
- ***df/dt>1 Status***: determines whether the stage is for falling or rising frequency conditions
- ***df/dt>1 Setting***: defines the rate of change of frequency pickup setting
- ***df/dt>1 Time***: sets the time delay
- ***df/dt>1 Dir'n***: sets the direction of change you wish to check (positive, negative, or both)

In addition, start, trip and timer block DDB signals are available for each stage, as well as an inhibit signal to inhibit all four stages.

Note:
It is recommended to only use df/dt settings <8Hz/s to maintain the claimed performance accuracy for pick-up and operating time, and to ensure the relay is within the frequency operating range, 45-65Hz.

16.3.2 INDEPENDENT R.O.C.O.F PROTECTION LOGIC

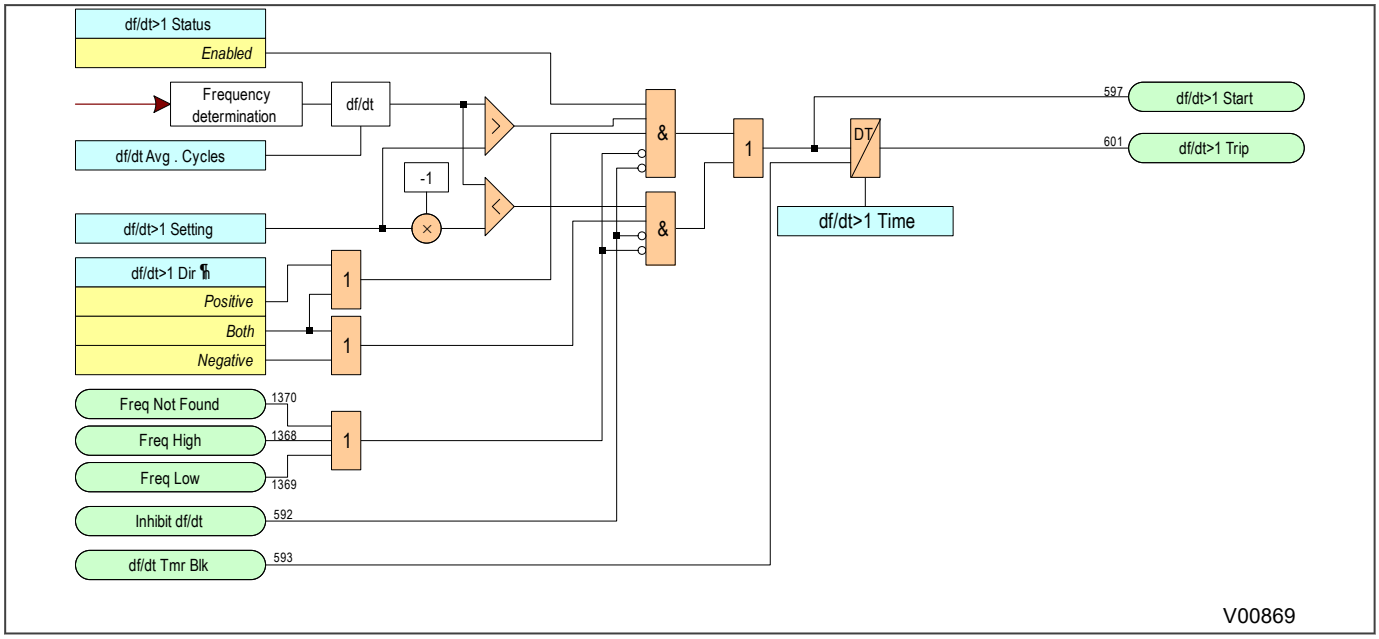


Figure 336: Rate of change of frequency logic (single stage)

CHAPTER 17

POWER PROTECTION FUNCTIONS

17.1 CHAPTER OVERVIEW

Power protection is used for protecting generators. Although the main function of this device is for feeder applications, it can also be used as a cost effective alternative for protecting small distributed generators, typically less than 2 MW.

This chapter contains the following sections:

Chapter Overview 513

Overpower Protection 514

Underpower Protection 517

17.2 OVERPOWER PROTECTION

With Overpower, we should consider two distinct conditions: Forward Overpower and Reverse Overpower.

A forward overpower condition occurs when the system load becomes excessive. A generator is rated to supply a certain amount of power and if it attempts to supply power to the system greater than its rated capacity, it could be damaged. Therefore overpower protection in the forward direction can be used as an overload indication. It can also be used as back-up protection for failure of governor and control equipment. Generally the Overpower protection element would be set above the maximum power rating of the machine.

A reverse overpower condition occurs if the generator prime mover fails. When this happens, the power system may supply power to the generator, causing it to motor. This reversal of power flow due to loss of prime mover can be very damaging and it is important to be able to detect this with a Reverse Overpower element.

17.2.1 OVERPOWER PROTECTION IMPLEMENTATION

Overpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group.

The Power Protection elements provide 4 stages of directional power for both active and reactive power, any of which can be configured as Overpower by selecting the `Over` value in the ***Power1 Function*** (or other stage) setting. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power and single phase power measurements (based on A, B and/or C phases) as the energising quantities. A Start condition occurs when two consecutive measurements exceed the setting threshold. A trip condition occurs if the Start condition is present for the set time delay. This can be inhibited by the VTS Slow Block and Pole Dead logic if desired.

The Start and Trip timer resets if the power falls below the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

17.2.2 OVERPOWER LOGIC

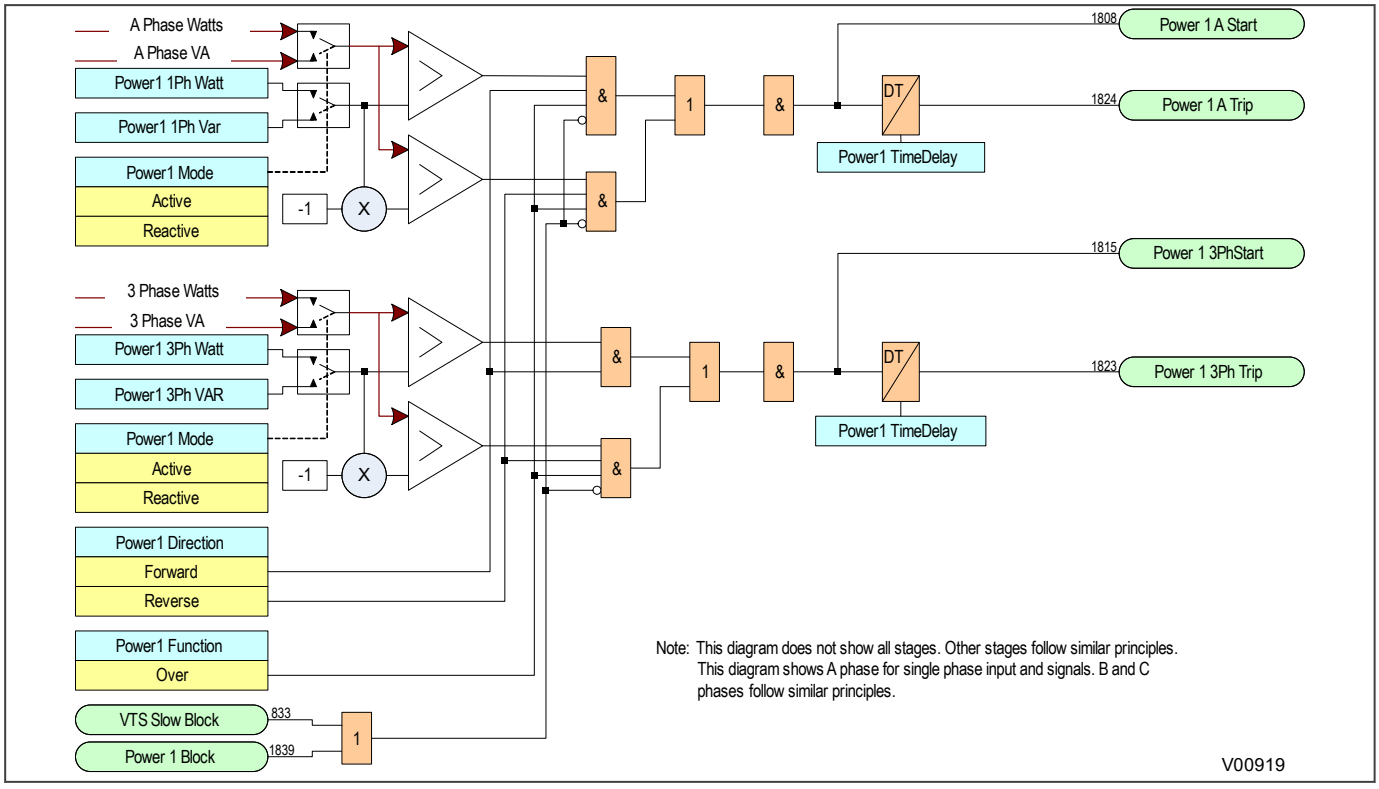


Figure 337: Overpower logic

17.2.3 APPLICATION NOTES

17.2.3.1 FORWARD OVERPOWER SETTING GUIDELINES

The relevant power threshold settings should be set greater than the full load rated power.

The operating mode should be set to Forward.

A time delay setting, ***Power1 TimeDelay*** (or other stage) should be applied. This setting is dependant on the application. The delay on the reset timer, ***Power1 tRESET*** (or other stage) setting, would normally be set to zero.

17.2.3.2 REVERSE POWER CONSIDERATIONS

A generator is expected to supply power to the connected system in normal operation. If the generator prime mover fails, it will begin to take motoring power from the power system (if the power system to which it is connected has other generating sources). The consequences of this reversal of power and the level of power drawn from the power system will be dependent on the type of prime mover.

Prime Mover	Motoring Power	Possible Damage (Percentage Rating)
Diesel Engine	5% - 25%	Risk of fire or explosion from unburned fuel
Motoring level depends on compression ratio and cylinder bore stiffness. Rapid disconnection is required to limit power loss and risk of damage.		
Gas Turbine	10% - 15% (Split-shaft) >50% (Single-shaft)	With some gear-driven sets, damage may arise due to reverse torque on gear teeth.
Compressor load on single shaft machines leads to a high motoring power compared to split-shaft machines. Rapid disconnection is required to limit power loss or damage.		
Hydraulic Turbines	0.2 - >2% (Blades out of water) >2.0% (Blades in water)	Blade and runner damage may occur with a long period of motoring
Power is low when blades are above tail-race water level. Hydraulic flow detection devices are often the main means of detecting loss of drive. Automatic disconnection is recommended for unattended operation.		
Steam Turbines	0.5% - 3% (Condensing sets) 3% - 6% (Non-condensing sets)	Thermal stress damage may be inflicted on low-pressure turbine blades when steam flow is not available to dissipate losses due to air resistance.
Damage may occur rapidly with non-condensing sets or when vacuum is lost with condensing sets. Reverse power protection may be used as a secondary method of detection and might only be used to raise an alarm.		

In some applications, the level of reverse power in the case of prime mover failure may fluctuate. This may be the case for a failed diesel engine. To prevent cyclic initiation and reset of the main trip timer, an adjustable reset time delay is provided. You will need to set this time delay longer than the period for which the reverse power could fall below the power setting. This setting needs to be taken into account when setting the main trip time delay.

Note:
A delay in excess of half the period of any system power swings could result in operation of the reverse power protection during swings.

17.2.3.3 REVERSE OVERPOWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a reverse power stage by setting the ***Power1 Direction*** (or other stage) cell to `Reverse`.

The relevant power threshold settings should be set to less than 50% of the motoring power.

The operating mode should be set to Reverse.

The reverse power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation.

A time delay setting, of approximately 5 s would be typically applied.

The delay on the reset timer, ***Power1 tRESET*** (or other stage), would normally be set to zero.

When settings of greater than zero are used for the reset time delay, the pick-up time delay setting may need to be increased to ensure that false tripping does not result in the event of a stable power swinging event.

Reverse overpower protection can also be used for loss of mains applications. If the distributed generator is connected to the grid but not allowed to export power to the grid, it is possible to use reverse power detection to switch off the generator. In this case, the threshold setting should be set to a sensitive value, typically less than 2% of the rated power. It should also be time-delayed to prevent false trips or alarms being given during power system disturbances, or following synchronisation. A typical time delay is 5 seconds.

17.3 UNDERPOWER PROTECTION

Although the Underpower protection is directional and can be configured as forward or reverse, the most common application is for Low Forward Power protection.

When a machine is generating and the circuit breaker connecting the generator to the system is tripped, the electrical load on the generator is cut off. This could lead to overspeeding of the generator if the mechanical input power is not reduced quickly. Large turbo-alternators, with low-inertia rotor designs, do not have a high over speed tolerance. Trapped steam in a turbine, downstream of a valve that has just closed, can rapidly lead to over speed. To reduce the risk of over speed damage, it may be desirable to interlock tripping of the circuit breaker and the mechanical input with a low forward power check. This ensures that the generator circuit breaker is opened only after the mechanical input to the prime mover has been removed, and the output power has reduced enough such that overspeeding is unlikely. This delay in tripping the circuit breaker may be acceptable for non-urgent protection trips (e.g. stator earth fault protection for a high impedance earthed generator). For urgent trips however (e.g. stator current differential protection), this Low Forward Power interlock should not be used.

17.3.1 UNDERPOWER PROTECTION IMPLEMENTATION

Underpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group..

The Power Protection element provides 4 stages of directional power for both active and reactive power, any of which can be configured as Underpower by selecting the `Under` value in the ***Power1 Function*** (or other stage) setting. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power or single phase power measurements (based on A, B or/and or C phases) as the energising quantity. A start condition occurs when two consecutive measurements fall below the setting threshold. A trip condition occurs if the start condition is present for the set trip time. This can be inhibited by the VTS slow block and pole dead logic if desired.

The Start and Trip timer resets if the power exceeds the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

17.3.2 UNDERPOWER LOGIC

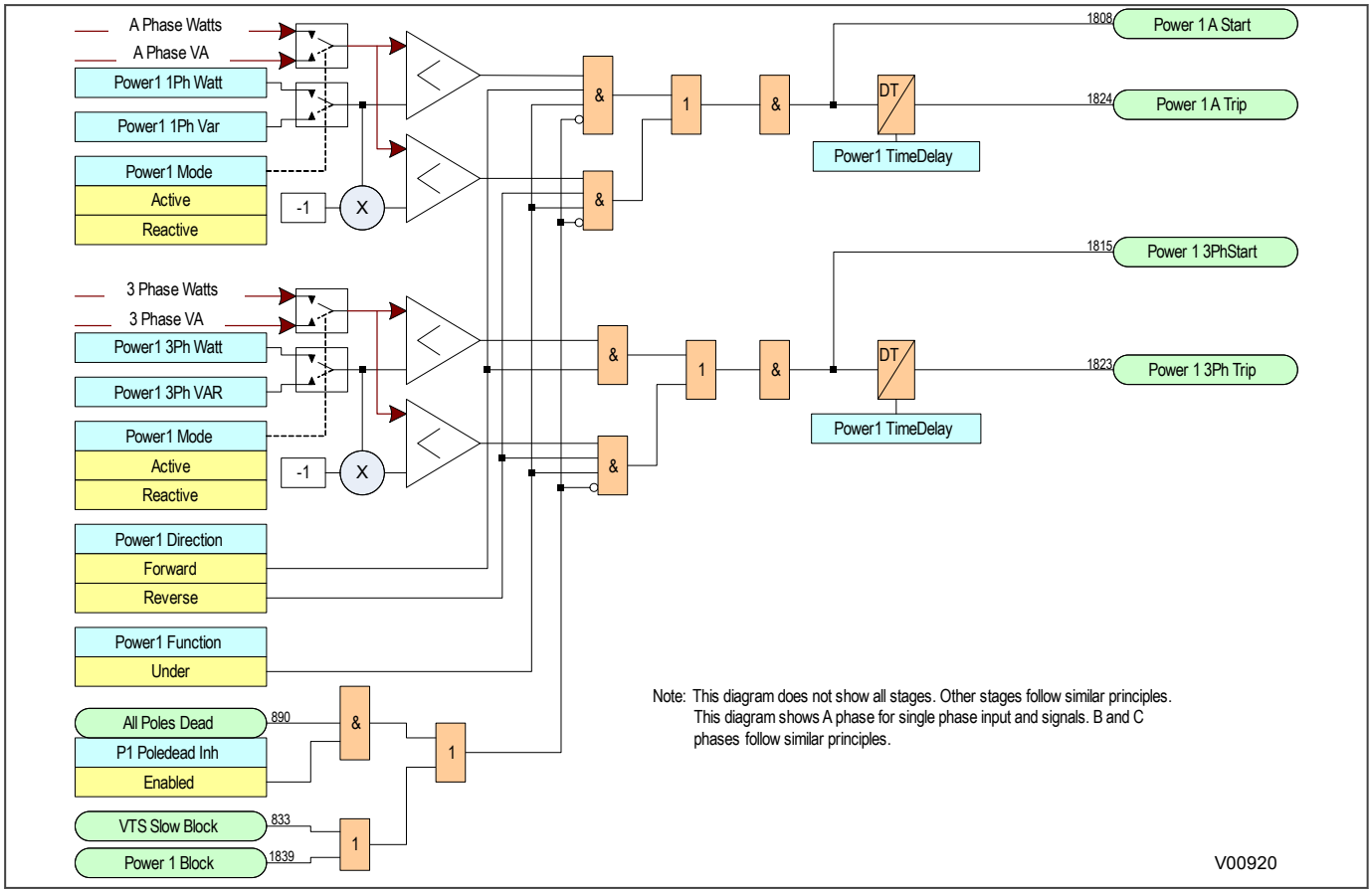


Figure 338: Underpower logic

17.3.3 APPLICATION NOTES

17.3.3.1 LOW FORWARD POWER CONSIDERATIONS

The Low Forward Power protection can be arranged to interlock 'non-urgent' protection tripping using the Flexlogic Equation Editor. It can also be arranged to provide a contact for external interlocking of manual tripping. To prevent unwanted alarms and flags, a Low Forward Power protection element can be disabled when the circuit breaker is opened via Pole Dead logic.

The Low Forward Power protection can also be used to provide loss of load protection when a machine is motoring. It can be used for example to protect a machine which is pumping from becoming unprimed, or to stop a motor in the event of a failure in the mechanical transmission.

A typical application would be for pump storage generators operating in the motoring mode, where there is a need to prevent the machine becoming unprimed which can cause blade and runner damage. During motoring conditions, it is typical for the protection to switch to another setting group with the low forward power enabled and correctly set and the protection operating mode set to `Reverse`.

A low forward power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

17.3.3.2 LOW FORWARD POWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a forward power stage by setting the ***Power1 Direction*** (or other stage) cell to `Forward`.

When required for interlocking of non-urgent tripping applications, the threshold setting of the low forward power protection function should be less than 50% of the power level that could result in a dangerous overspeed condition on loss of electrical loading.

When required for loss of load applications, the threshold setting of the low forward power protection function, is system dependent, however, it is typically set to 10 - 20% below the minimum load. The operating mode should be set to operate for the direction of the load current, which would typically be reverse for a pump storage machine application where *Forward* is the Generating direction and *Reverse* is the motoring direction.

For interlocking non-urgent trip applications the time delay associated with the low forward power protection function could be set to zero. However, some delay is desirable so that permission for a non-urgent electrical trip is not given in the event of power fluctuations arising from sudden steam valve/throttle closure. A typical time delay is 2 seconds.

For loss of load applications the pick-up time delay is application dependent but is normally set in excess of the time between motor starting and the load being established. Where rated power cannot be reached during starting (for example where the motor is started with no load connected) and the required protection operating time is less than the time for load to be established then it will be necessary to inhibit the power protection during this period. This can be done in the PSL using AND logic and a pulse timer triggered from the motor starting to block the power protection for the required time.

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse power protection function, should be set to a sensitive value, typically <2% of the rated power.

The low forward power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation. A time delay setting, of 5 s should be applied typically.

The delay on the reset timers would normally be set to zero.

To prevent unwanted alarms and flags, the protection element can be disabled when the circuit breaker is open via Pole Dead logic.

17.3.3.3 REACTIVE POWER PROTECTION

Some applications provide underexcitation protection using negative reactive power elements. This is popular for synchronous motors and small generators.

A reverse reactive power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

Setting guidelines

Each stage of power protection can be selected to operate as a reverse reactive power stage by selecting the ***Power1 Function*** (or other stage) cell to *Over* and the ***Power1 Direction*** (or other stage) cell to *Reverse*.

The power threshold setting of the negative reactance power protection, ***Power1 3Ph VAr*** or ***Power1 1Ph VAr*** (or other stage) should be set to supervise the steady state and dynamic stability limits for under excitation protection. The following figure shows an example of the typical settings, Q1 and Q2.

The disadvantage of this method is that the measurement is not very sensitive during low voltage operation of the generator. The reactive power elements can be blocked in the PSL from an undervoltage start signal if this is a problem. This method is less secure than the impedance method and so is often used just to alarm.

If the static limit characteristic Q1 is exceeded, the voltage regulator must first have the opportunity of increasing the excitation. For this reason, a time delayed trip of typically 5-10s is used ***Power1 TimeDelay*** (or other stage). A shorter delay of 0.5s can be used for Q2.

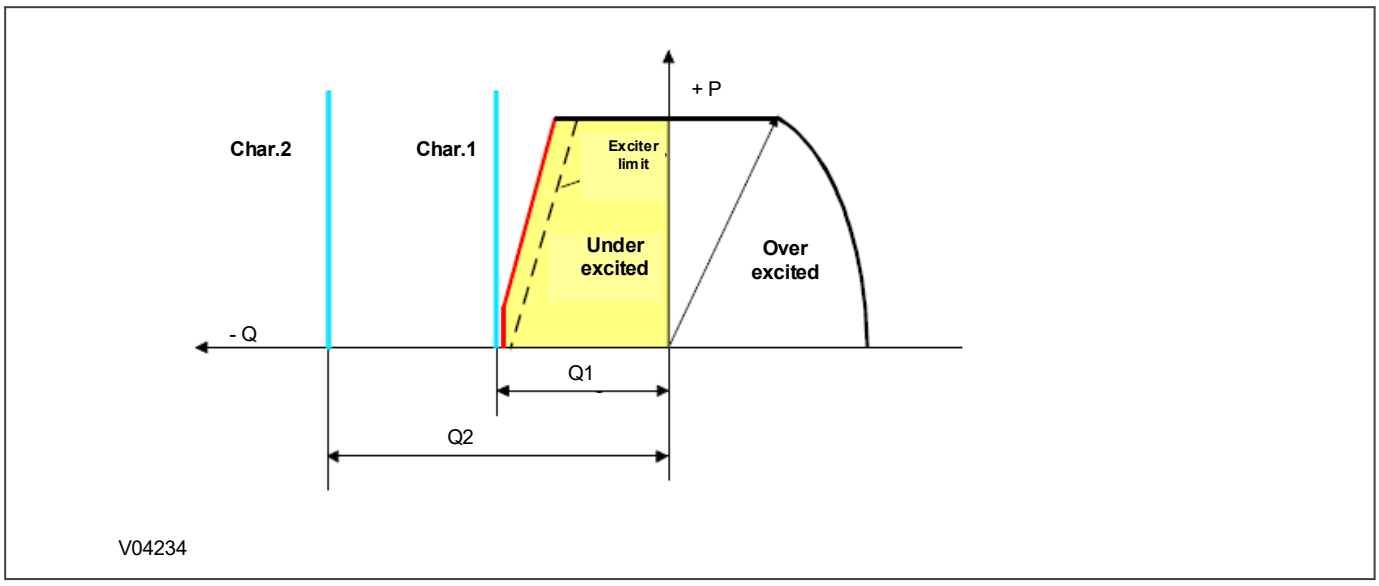


Figure 339: Reactive power protection for underexcitation protection

$Q1 = VN^2/Xd$

$Q2 > = 2\ VN^2/Xd$

Where:

VN = Machine nominal voltage

Xd = Generator direct-axis synchronous reactance in ohms

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse reactive power protection function, ***Power1 3Ph VAr*** or ***Power1 1Ph VAr*** (or other stage), should be set to a suitable value, typically <2% of the rated reactive power. The reverse reactive power protection function should be time-delayed, to prevent false trips or alarms being given during power system disturbances or following synchronisation, a typical time delay is 5 s.

CHAPTER 18

CURRENT TRANSFORMER REQUIREMENTS

18.1 CHAPTER OVERVIEW

This chapter contains the following sections:

Chapter Overview 522
Recommended CT Classes 523
Current Differential Requirements 524
Distance Protection Requirements 526
Determining Vk for IEEE C-class CT 527
Worked Examples 528

18.2 RECOMMENDED CT CLASSES

You can use Class X current transformers with a knee point voltage greater or equal to that calculated. You can also use class 5P protection CT. These have a knee-point voltage equivalent, which can be approximated from the following calculations:

$$V_k = (VA \times ALF)/I_n + (R_{CT} \times ALF \times I_n)$$

where:

- V_k = Knee-point voltage
- VA = Voltampere burden rating
- ALF = Accuracy limit factor
- I_n = CT nominal secondary current
- R_{CT} = CT resistance

18.3 CURRENT DIFFERENTIAL REQUIREMENTS

Performance of line current differential protection is heavily dependent upon the integrity of the signals obtained from the associated line current transformers. A major influence on CT performance is knee-point voltage value (V_K) since CT errors increase significantly when this value is exceeded.

The V_K value of a CT relates to how much flux its magnetic core can support and is influenced by the CT size and class rating. We strongly recommend class X or class 5P Current Transformers for line current differential protection. In addition, we recommend that the compliance with minimum V_K requirements is reviewed before confirming suitability of the protection.

General Applications

Methods used to check V_K compliance vary according to anticipated levels of pre-fault remanent CT flux.

For most applications, heavy pre-fault CT core saturation is not envisaged and so, to avoid oversizing the CTs, a conservative approach can be taken. To ensure that pre-fault flux-remanence in the CT magnetic core is accounted for in the evaluation of V_K, the magnetic flux is pre-aligned in the core before application of faults for V_K evaluation. A spreadsheet (accessible through the link below) allows different scenarios to be modelled to provide a convenient evaluation of CT knee-point voltage requirements (V_K).

CT Knee-point Calculations

Note:
The CT knee point calculations in the embedded spreadsheet are based upon the following default settings: Phase Is1 set to 0.2In, Phase Is2 set to 2.0In, Phase k1 set to 30%, Phase k2 set to 150%, Ktransient set to 200%, Is1 Restraint set to 4.0In and Phase Time Delay set to 0 seconds.

If using Adobe Acrobat Reader, click on the button below to open the spreadsheet.

This manual must be opened with a PDF viewer capable of opening attachments, such as Adobe Acrobat Reader or Nitro PDF. If using Nitro PDF, attachments are shown in the attachment pane. To show or hide the attachments pane, look in the sidebar and click the attachments tab.

Note:
An Open File dialogue box may open with a warning message about potential harm from programs, macros or viruses. The file supplied does not contain any harmful content and may be safely opened.

Applications Requiring Adherence to NGTS 3.24.18

For applications where heavy pre-fault CT core saturation might be predicted, a more rigorous approach may be appropriate. In this scenario, conjunctive testing is used to determine the required V_K. This method involves simulating 3 polarised faults to force CT flux levels into saturation before evaluating combined CT and differential protection performance. Typically resulting in the specification of larger CTs, the minimum V_K requirement is determined as:

$$V_k \geq KI_n(R_{CT} + 2R_L)$$

where:

- V_k = Required IEC knee point voltage
- K = Dimensioning factor

- I_n = CT nominal secondary current
- R_{CT} = CT resistance
- R_L = One-way lead impedance from CT to relay
- K is a constant depending on the maximum value of through fault current for stability (I_f), and the Primary system X/R ratio

Determination of K with transient bias disabled

For IEDs with the settings: Is1 = 20%, Is2 = 2In, k1 = 30%, k2 = 150% and for (I_f x X/R) ≤ 1000 (2-end applications):

K must have the value 65 or as calculated by: K = 40 + (0.07(I_f x X/R)), whichever the highest.

For higher (I_f x X/R) up to 2600, K = 107

For IEDs with the settings: Is1 = 20%, Is2 = 2In, k1 = 30%, k2 = 100% and for (I_f x X/R) ≤ 600 (3-end applications):

K must have the value 65 or as calculated by: K = 40 + (0.35(I_f x X/R))

For higher (I_f x X/R) up to 2600, K = 256

Determination of K with transient bias enabled

For IEDs with the settings: Is1 = 20%, Is2 = 2 In, k1 = 30%, k2 = 150% (2-end applications):

K = (1.42I_f + 53.7)(6.06E-03 x X/R + 0.515)

For IEDs with the settings: Is1 = 20%, Is2 = 2 In, k1 = 30%, k2 = 100% (3-end applications):

K = (7.47 x I_f + 77.8)(8.19E-03 x X/R + 0.345)

This is valid for I_f ≤ 50 pu and X/R ≤ 80

18.4 DISTANCE PROTECTION REQUIREMENTS

Zone 1 Reach Point Accuracy (RPA)

$$V_k \geq K_{RPA\ x}\ I_{fZ1\ x}\ (1+ X/R)(R_{CT} + R_L)$$

where:

- V_k = Required CT knee point voltage (volts)
- I_{fZ1} = Maximum secondary phase fault current at Zone 1 reach point (A)
- X/R = Primary system reactance/resistance ratio
- R_{CT} = CT secondary winding resistance
- R_L = Single lead resistance from CT to IED
- K_{RPA} = Fixed dimensioning factor:
  - = 0.6 for all overhead line applications, or where sub-cycle tripping times are required for Zone 1 element
  - = 0.35 for power cable applications, where sub-cycle tripping times are not required for Zone 1 element

Zone 1 close-up fault operation

An additional calculation must be performed for all cables and lines where the source impedance ratio (SIR) may be less than SIR = 2.

$$V_k \geq K_{max\ x}\ I_{fmax\ x}\ (R_{CT} + R_L)$$

where:

K_{max} = Fixed dimensioning factor = 1.4

I_{fmax} = Maximum secondary phase fault current

Then, the highest of the two calculated knee points must be used.

> *Note:*
> *It is not necessary to repeat the calculation for earth faults, as the phase reach calculation is the worst-case for CT dimensioning.*

18.5 DETERMINING VK FOR IEEE C-CLASS CT

Where IEEE standards are used to specify CTs, the C class voltage rating can be checked to determine the equivalent V_k (knee point voltage according to IEC).

The equivalence formula is:

$$V_k = 1.05(\text{C rating in volts}) + 100R_{CT}$$

18.6 WORKED EXAMPLES

The power system and the line parameters used in these examples are as follows:

- Single circuit operation between Green Valley and Blue River
- System voltage = 230 kV
- System frequency = 50 Hz
- System grounding = solid
- CT ratio = 1200/1
- Line length = 100 km
- Line positive sequence impedance Z1 = 0.089 + j 0.476 ohm per km
- Bus fault level = 40 kA
- Primary time constant = 120 ms

Important notes to be considered

- For calculating the CT requirements, the bus bar short time symmetrical fault rating should be considered as the bus fault level.
- If only indicative X/R ratios are available, the circuit breaker's DC breaking capacity is used to derive the primary time constant and therefore the primary system X/R. It is derived from the circuit breaker manufacturer's practical primary time constants. These vary between 50 ms (66 kV and 132 kV breakers) and 120 ms (220 kV and 400 kV breakers). 150 ms is a practical figure for generator circuit breakers.
- Current differential: Both If and X/R are to be calculated for a through fault
- Distance Zone1 reach point case: Both If and X/R are to be calculated for a fault at Zone1 reach point

18.6.1 CALCULATION OF PRIMARY X/R RATIO

Primary X/R up to the Green Valley busbar:

$= 2\pi f \times \text{primary time constant}$

$= 2\pi \times 50 \times 0.12 = 37.7$

18.6.2 CALCULATION OF SOURCE IMPEDANCE

Source impedance magnitude:

$= 230\ \text{kV}/(1.732 \times 40\ \text{kA}) = 3.32\ \text{ohms}$

Source angle:

$= \tan^{-1}(37.7) = 88.48°$

Hence:

$Zs = 0.088 + j3.317$

18.6.3 CALCULATION OF FULL LINE IMPEDANCE

Z1:

$= 0.089 + j0.476\ \text{ohms/km}$

Z_L:

$= 8.9 + j47.6 = 48.42\ \text{ohms angle}\ 79.4°$

18.6.4 CALCULATION OF TOTAL IMPEDANCE UP TO REMOTE BUSBAR

$Z_T = Z_S + Z_L$:

= 8.988+ j50.917 ohms =51.7 ohms angle 80°

18.6.5 CALCULATION OF THROUGH FAULT X/R RATIO

$X/R_{\text{through}} = 50.917/8.988 = 5.66$

18.6.6 CALCULATION OF THROUGH FAULT CURRENT

$I_{f\,\text{through}} = 230\text{kV}/(1.732 \times 51.7) = 2568.5$ A primary = 2.14 A secondary

18.6.7 CALCULATION OF LINE IMPEDANCE TO ZONE 1 REACH POINT

$Z_{\text{zone 1}} = 0.8ZL = 7.12 + j\,38.08 = 38.73$ ohms angle 79.4°

18.6.8 CALCULATION OF TOTAL IMPEDANCE TO ZONE 1 REACH POINT

$Z_{T\,\text{zone 1}} = Z_S + Z\ \text{zone 1} = 7.208 + j\,41.397 = 42.019$ ohms angle 80°

18.6.9 CALCULATION OF X/R TO ZONE 1 REACH POINT

$X/R_{\text{zone 1}} = 41.397/7.208 = 5.74$

18.6.10 CALCULATION OF FAULT CURRENT TO ZONE 1 REACH POINT

$I_{f\,\text{zone 1}} = 230\text{kV}/(1.732 \times 42.019) = 3160.34$ A primary = 2.63 A secondary

18.6.11 CALCULATION OF VK FOR CURRENT DIFFERENTIAL PROTECTION

Transient bias disabled, with k2 set to 150%

$I_{f\,\text{through}} \times X/R_{\text{through}} = 2.14 \times 5.66 = 12.11$

As this is less than 1000, we use the highest of K = 65 or K = 40 + (0.07(I_f x X/R))

Hence in this example we use K = 65. Therefore:

We know that $V_k \geq KI_n(R_{CT} + 2R_L)$, therefore

$V_k \geq 65(R_{CT} + 2R_L)$

Transient bias enabled, with k2 set to 150%

K = (1.42 x 2.14 + 53.7)(6.06E-03 x 5.66 + 0.515) = 31.2, therefore

$V_k \geq 31.2(R_{CT} + 2R_L)$

18.6.12 CALCULATION OF VK FOR DISTANCE ZONE 1 REACH POINT

Using: $V_k \geq K_{RPA} \times I_{fZ1} \times (1 + X/R)(R_{CT} + R_L)$

$V_k > 0.6 \times 2.63 \times (1 + 5.74)(R_{CT} + R_L)$, therefore:

$V_k > 10.65(R_{CT} + R_L)$

18.6.13 CALCULATION OF VK FOR DISTANCE ZONE 1 CLOSE-UP FAULT

SIR = Z_s/Z_{zone1} =3.32/38.73, which is less than 2, so we need to calculate Vk.

Close-up fault current = 40kA primary, = 33.33A secondary

$V_k \geq K_{max} \times I_{fmax\ x} (R_{CT} + R_L)$

$V_k > 1.4 \times 33.3 \times (R_{CT} + R_L)$, therefore:

$V_k > 46.67(R_{CT} + R_L)$

18.6.14 CALCULATION OF VK FOR DISTANCE TIME DELAYED ZONES

$V_k > I_f(R_{CT} + R_L)$

$V_k > I_{fthrough} \times (R_{CT} + R_L)$, therefore:

$V_k > 2.14(R_{CT} + R_L)$

CHAPTER 19

MONITORING AND CONTROL

19.1 CHAPTER OVERVIEW

As well as providing a range of protection functions, the product includes comprehensive monitoring and control functionality.

This chapter contains the following sections:

Chapter Overview 532
Event Records 533
Disturbance Recorder 537
Measurements 538
CB Condition Monitoring 546
CB State Monitoring 560
Circuit Breaker Control 565
Pole Dead Function 572
System Checks 574
Switch Status and Control 585
Test Mode 590
IEC 61850 Control Authority 591

19.2 EVENT RECORDS

GE Vernova devices record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

The event records are detailed in the *VIEW RECORDS* column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

If viewing the event with the settings application software, simply open the extracted event file. All the events are displayed chronologically. Each event is summarised with a time stamp obtained from the ***Time & Date*** cell) and a short description relating to the event obtained from the ***Event Text*** cell). You can expand the details of the event by clicking on the **+** icon to the left of the time stamp.

The following table shows the correlation between the fields in the setting application software's event viewer and the cells in the menu database.

Field in Event Viewer	Equivalent Cell in Menu DB	Cell Reference	User Settable?
Left hand column header	VIEW RECORDS → Time & Date	01 03	No
Right hand column header	VIEW RECORDS → Event Text	01 04	No
Description	SYSTEM DATA → Description	00 04	Yes
Plant reference	SYSTEM DATA → Plant Reference	00 05	Yes
Model number	SYSTEM DATA → Model Number	00 06	No
Address	Displays the Courier address relating to the event	N/A	No
Event type	VIEW RECORDS → Menu Cell Ref	01 02	No
Event Value	VIEW RECORDS → Event Value	01 05	No
Evt Unique Id	VIEW RECORDS → Evt Unique ID	01 FE	No

The device is capable of storing up to 5000 time tagged event records.

In addition to the event log, there are two logs which contain duplicates of the last 10 maintenance records and the last 100 fault records. The purpose of this is to provide convenient access to the most recent fault and maintenance events.

19.2.1 EVENT TYPES

There are several different types of event:

- Opto-input events (Change of state of opto-input)
- Contact events (Change of state of output relay contact)
- Alarm events
- Fault record events
- Standard events
- Security events

Standard events are further sub-categorised internally to include different pieces of information. These are:

- Protection events (starts and trips)
- Maintenance record events
- Platform events

Note:
The first event in the list (event 0) is the most recent event to have occurred.

19.2.1.1 OPTO-INPUT EVENTS

If one or more of the opto-inputs has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all opto-inputs. You can tell which opto-input has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Logic Inputs #` where # is the batch number of the opto-inputs. This is '1', for the first batch of opto-inputs and '2' for the second batch of opto-inputs (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the opto-inputs, where the Least Significant Bit (LSB), on the right corresponds to the first opto-input `Input L1`.

The same information is also shown in the ***Opto I/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

19.2.1.2 CONTACT EVENTS

If one or more of the output relays (also known as output contacts) has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all output relays. You can tell which output relay has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Output Contacts #` where # is the batch number of the output relay contacts. This is '1', for the first batch of output contacts and '2' for the second batch of output contacts (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the output relays, where the LSB (on the right) corresponds to the first output contact `Output R1`.

The same information is also shown in the ***Relay O/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

19.2.1.3 ALARM EVENTS

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event.

The description of this event type, as shown in the ***Event Text*** cell is cell dependent on the type of alarm and will be one of those shown in the following tables, followed by `OFF` or `ON`.

The event value shown in the ***Event Value*** cell for this type of event is a 32 bit binary string. There are one or more banks 32 bit registers, depending on the device model. These contain all the alarm types and their logic states (`ON` or `OFF`).

The same information is also shown in the ***Alarm Status (n)*** cells in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

19.2.1.4 FAULT RECORD EVENTS

An event record is created for every fault the IED detects. This is also known as a fault record.

The event type description shown in the ***Event Text*** cell for this type of event is always `Fault Recorded`.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the ***Select Fault*** setting, where fault number 0 is the latest fault.

A fault record is triggered by the ***Fault REC TRIG*** signal DDB, which is assigned in the PSL. The fault recorder records the values of all parameters associated with the fault for the duration of the fault. These parameters are stored in separate Courier cells, which become visible depending on the type of fault.

The fault recorder stops recording only when:

The Start signal is reset AND the undercurrent is ON OR the Trip signal is reset, as shown below:

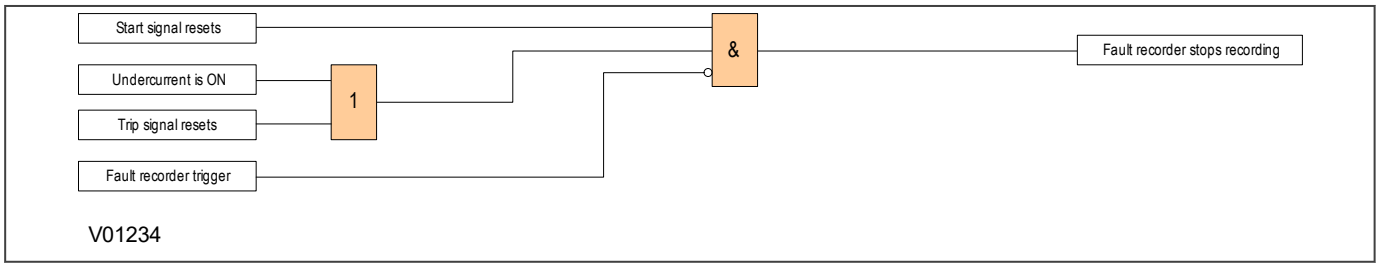


Figure 340: Fault recorder stop conditions

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The timestamp assigned to the fault record event corresponds to the time when the fault recorder stops.

Note:
We recommend that you do not set the triggering contact to latching. This is because if you use a latching contact, the fault record would not be generated until the contact has been fully reset.

19.2.1.5 MAINTENANCE EVENTS

Internal failures detected by the self-test procedures are logged as maintenance records. Maintenance records are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is always `Maint Recorded`.

The ***Event Value*** cell also provides a unique binary code.

The IED contains a separate register containing the latest maintenance records. This provides a convenient way of viewing the latest maintenance records and saves searching through the event log. You access these fault records using the ***Select Maint*** setting.

The maintenance record has a number of extra menu cells relating to the maintenance event. These parameters are ***Maint Text***, ***Maint Type*** and ***Maint Data***. They contain details about the maintenance event selected with the ***Select Maint*** cell.

19.2.1.6 PROTECTION EVENTS

The IED logs protection starts and trips as individual events. Protection events are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is dependent on the protection event that occurred. Each time a protection event occurs, a DDB signal changes state. It is the name of this DDB signal followed by 'ON' or 'OFF' that appears in the ***Event Text*** cell.

The ***Event Value*** cell for this type of event is a 32 bit binary string representing the state of the relevant DDB signals. These binary strings can also be viewed in the *COMMISSION TESTS* column in the relevant DDB batch cells.

Not all DDB signals can generate an event. Those that can are listed in the *RECORD CONTROL* column. In this column, you can set which DDBs generate events.

19.2.1.7 SECURITY EVENTS

An event record is generated each time a setting that requires an access level is executed.

The event type description shown in the ***Event Text*** cell displays the type of change.

19.2.1.8 PLATFORM EVENTS

Platform events are special types of standard events.

The event type description shown in the ***Event Text*** cell displays the type of change.

19.3 DISTURBANCE RECORDER

The disturbance recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals. The digital signals may be inputs, outputs, or internal DDB signals. The disturbance records can be extracted using the disturbance record viewer in the settings application software. The disturbance record file can also be stored in the COMTRADE format. This allows the use of other packages to view the recorded data.

The integral disturbance recorder has an area of memory specifically set aside for storing disturbance records. The number of records that can be stored is dependent on the recording duration. The minimum duration is 0.1 s and the maximum duration is 10.5 s.

When the available memory is exhausted, the oldest records are overwritten by the newest ones.

Each disturbance record consists of a number of analogue data channels and digital data channels. The relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities.

The fault recording times are set by a combination of the ***Duration*** and ***Trigger Position*** cells. The ***Duration*** cell sets the overall recording time and the ***Trigger Position*** cell sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

With the ***Trigger Mode*** set to *Single*, if further triggers occurs whilst a recording is taking place, the recorder will ignore the trigger. However, with the ***Trigger Mode*** set to *Extended*, the post trigger timer will be reset to zero, extending the recording time.

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

You may choose any of the digital channels to trigger the disturbance recorder on either a low to high or a high to low transition, via the ***Input Trigger*** cell. The default settings are such that any dedicated trip output contacts will trigger the recorder.

It is not possible to view the disturbance records locally via the front panel LCD. You must extract these using suitable setting application software such as MiCOM S1 Agile.

19.4 MEASUREMENTS

19.4.1 MEASURED QUANTITIES

The device measures directly and calculates a number of system quantities, which are updated every second. You can view these values in the relevant MEASUREMENT columns or with the Measurement Viewer in the settings application software. Depending on the model, the device may measure and display some or more of the following quantities:

- Measured and calculated analogue current and voltage values
- Power and energy quantities
- Peak, fixed and rolling demand values
- Frequency measurements
- Thermal measurements
- Teleprotection channel measurements

19.4.2 MEASUREMENT SETUP

You can define the way measurements are set up and displayed using the *MEASURE'T SETUP* column and the measurements are shown in the relevant MEASUREMENTS tables.

19.4.3 FAULT LOCATOR

Some models provide fault location functionality. It is possible to identify the fault location by measuring the fault voltage and current magnitude and phases and presenting this information to a Fault Locator function. The fault locator is triggered whenever a fault record is generated, and the subsequent fault location data is included as part of the fault record. This information is also displayed in the ***Fault Location*** cell in the *VIEW RECORDS* column. This cell will display the fault location in metres, miles ohms or percentage, depending on the chosen units in the ***Fault Location*** cell of the *MEASURE'T SETUP* column.

The Fault Locator uses pre-fault and post-fault analogue input signals to calculate the fault location. The result is included it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record.

When applied to parallel circuits, mutual flux coupling can alter the impedance seen by the fault locator. The coupling contains positive, negative and zero sequence components. In practise the positive and negative sequence coupling is insignificant. The effect on the fault locator of the zero sequence mutual coupling can be eliminated using the mutual compensation feature provided.

19.4.3.1 FAULT LOCATOR OPERATION

The fault locator uses an algorithmic method to provide a distance to fault location feature with metering capabilities. The data input to the algorithm is filtered using established digital signal processing techniques.

The data processed by the algorithm is first acquired by performing analogue to digital conversion on signals provided by the device's internal analogue bus and then performing the necessary calculations.

The metering values are continuously calculated, regularly updated and passed to the relays processor when requested.

Acquired data is written to a buffer until a fault condition is notified by the processor. This input buffer data is held pending the fault calculation and input data is redirected to an alternative buffer.

The fault calculation is initiated by a signal from the relay main processor. When the fault calculation is complete the output information is stored in non-volatile memory and made available to the processor for display on the relay front panel.

Where parallel circuits are hung on opposite sides of a route of towers, mutual flux coupling alters the impedance seen by the fault locator. In practice the positive and negative sequence coupling is insignificant and the effect on

the fault locator of the zero sequence mutual coupling can be eliminated by using the mutual compensation feature provided.

It should be noted that in devices fitted with both a ***DEF*** element and a fault locator, the mutual compensation current input terminals are shared with the ***DEF*** zero sequence current polarising input. And so, ***DEF*** zero sequence current polarising cannot be used at the same time as fault locator mutual compensation.

The fault locator is optional on the underground cable version of the device, where it is recommended that it is used for metering purposes only (see the Metering section, below) as fault location accuracy cannot be relied upon for this application.

19.4.3.2 EARTH FAULT BASIC THEORY

A two-machine equivalent circuit of a faulted power system is shown in the figure below:

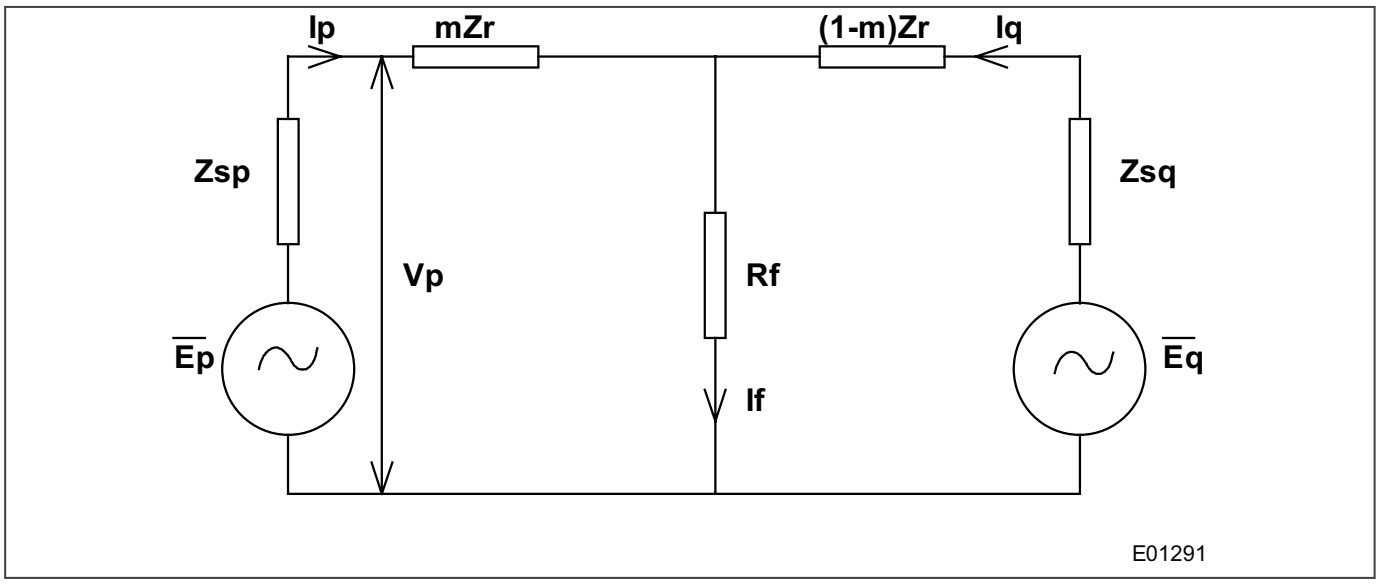


Figure 341: Two machine equivalent circuit

From the above figure:

$$Vp = mIpZr + IfRf$$

This equation shows that the calculation of m, the distance to fault, based on measurements of Vp and Ip at the local relay terminals is distorted by the IfRf term. This term is related to the current infeed from the remote terminal and cannot be readily measured. However its effect can be minimised as follows:

The real and imaginary components of these vectors (with respect to an arbitrary vector reference) vary with time as:

$$|Vp|[\cos(\omega t + s) + j\sin(\omega t + s)] = m|Zr|\,|Ip|\,[\cos(\omega t + e) + j\sin(\omega tt + e)] + Rf\,|If|\,[\cos(\omega t + d) + j\sin(\omega t + d)].$$

where:

d is the angle of the fault current.

s is the angle of Vp.

e is the angle of IpZr.

By evaluating equation *Vp = mIpZr + IfRf* at the instant in time when the fault current passes through zero and considering only the real components, then the Rf |If| term becomes zero i.e. t = ((π/2)-d)/ ω and the equation simplifies to:

$$|Vp|\cos(((\pi/2)-d) + s) = m\,|Zr|\,|Ip|\,\cos(((\pi/2)-d) + e)$$

Therefore, the fault location m can be calculated if the angle of the fault current d is known.

Estimating d the phase of the fault current If:

The fault vector If is obtained from an algorithm which uses superimposed currents, that is, the change of currents following the instant of fault.

Superimposed currents are indicated with an apostrophe (').

The sequence diagram for superimposed currents for an A-G fault is shown in the figure below:

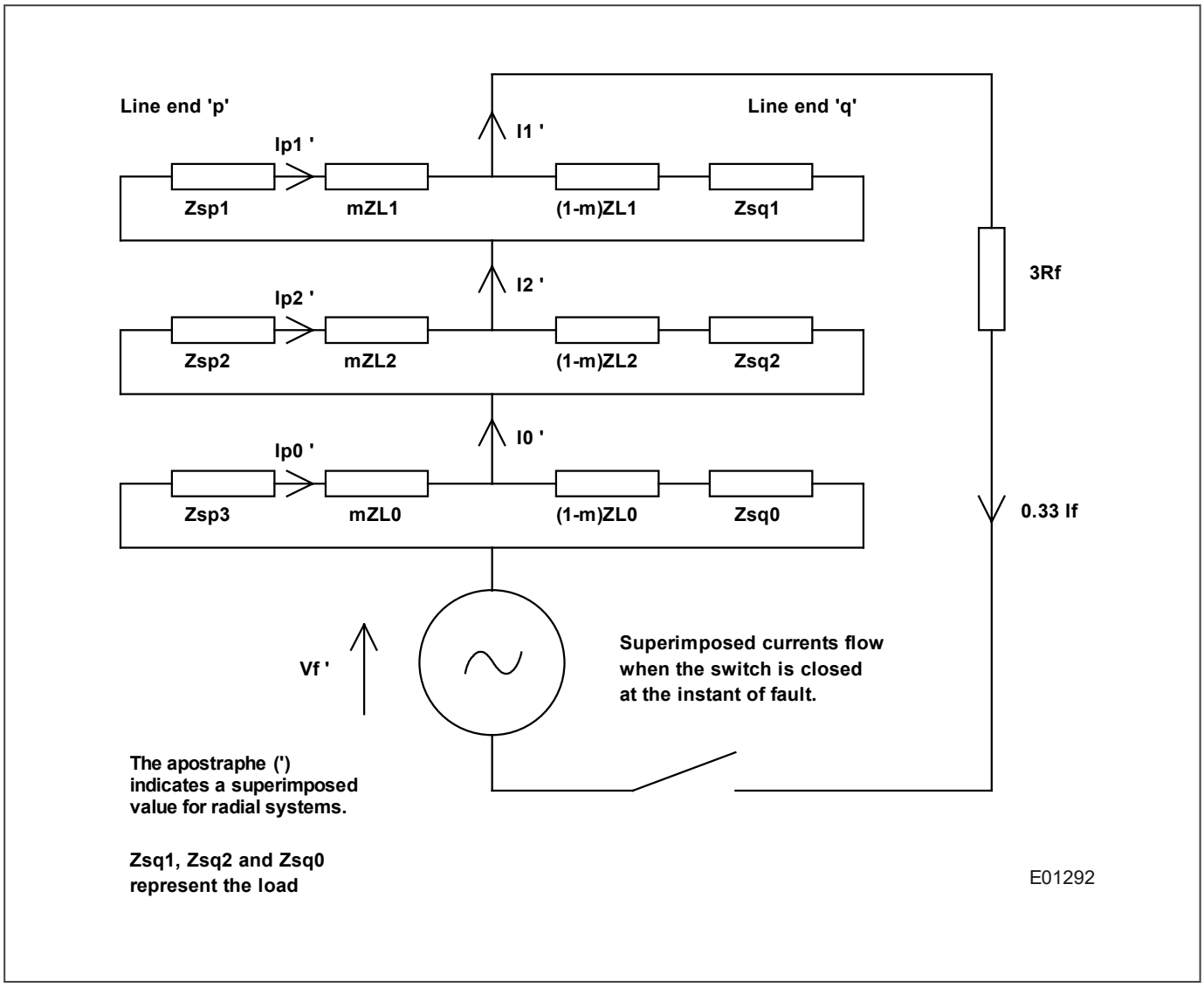


Figure 342: Superimposed symmetrical component sequence for A - N fault

For an A phase to earth fault:

$$0.33If = I1' = I2' = I0'$$

from which:

$$0.66If = I1' + I2'$$

$$= Ip1'D1 + Ip2'D2$$

where:

$$D1 = I1' / Ip1' \text{ and } D2 = I2' / Ip2'$$

and:

D2 approximately = D1 (assuming that the power system source and line positive and negative sequence impedances are approximately equal)

therefore:

$$0.66If = D1(Ip1' + Ip2')$$

also:

$$Ip' = Ip1' + Ip2' + Ip0'$$

therefore:

$$Ip1' + Ip2' = Ip' - Ip0'$$

from the equations above:

$$0.66If = D1\ (Ip' - Ip0')$$

Hence:

$$\text{angle } If = \text{angle } D1 + \text{angle } (Ip' - Ip0')$$

where:

D1 = A SCALAR factor - assuming that the power system is homogeneous
$= (Zsp1 + Zl1 + Zsq1) / ((1-m)Zl1 + Zsq1)$

The angle of D1 depends upon the fault position but for the purposes of this algorithm this angle is assumed to be zero.

Thus:

$$\text{angle } If = d = \text{angle } (Ip' - Ip0')$$

The equation above, shows that the phase angle of the fault current d can be estimated from the superimposed phase and neutral currents measured at the relay terminals.

therefore for an earth fault:

$$|If|(\cos(d) + j\sin(d))$$
$$= kD1(Ip'-Ip0')$$
$$= kD1[(Ia(fault) - Ia(prefault))$$
$$- 0.33(In(fault) - In(prefault))]$$

where:

k is a scalar factor and d is the required phase angle of If at the instant of time that the faulted vectors are calculated.

similarly, for a phase to phase fault:

$$|If|\ (\cos(d) + j\sin(d)) = kD1[(Ia(fault) - Ia(prefault))- (Ib(fault) - Ib(prefault))]$$

Thus, using the calculated pre-fault and faulted vectors the fault locator is able to calculate the angle of the fault current vector d at the instant of time that the faulted vectors are calculated.

19.4.3.3 DATA ACQUISITION AND BUFFER PROCESSING

The fault locator stores the sampled data within a 12 cycle cyclic buffer at a resolution of 48 samples per cycle. When the fault recorder is triggered the data in the buffer is frozen such that the buffer contains 6 cycles of pre-trigger data and 6 cycles of post-trigger data. Fault calculation commences shortly after this trigger point.

The trigger for the fault recorder is user selectable via the programmable scheme logic.

The fault locator can store data for up to four faults. This ensures that fault location can be calculated for all shots on a typical multiple reclose sequence.

19.4.3.4 FAULTED PHASE SELECTION

Phase selection is derived from the superimposed current phase selector.

Phase selection and fault location calculations can only be made if the current change exceeds 5% In.

19.4.3.5 FAULTED PHASE CALCULATION

The fault location calculation works by:

1. First obtaining the vectors
2. Selecting the faulted phase(s)
3. Estimating the phase of the fault current If for the faulted phase(s)
4. Solving the below equation for the fault location m at the instant of time where f = 0

$$Vp = mIpZr + IfRf$$

19.4.3.6 DISTANCE TO FAULT CALCULATION

Replica impedance Zr

The fault location calculation needs vectors derived from the line voltage (Vp) and from the relay's "replica impedance" voltage (IpZr) under fault conditions. The replica impedance is derived from the relay settings and is effectively set to the same value as the total line impedance. i.e.

$$Zr = Zline / \theta\ line + Zresidual / / \theta\ residual$$

This "replica impedance" is modified using the mutual compensation factor when the mutual compensation feature is used. i.e.

$$Zr = Zline / \theta\ line + Zresidual / / \theta\ residual + Zmutual / / \theta\ mutual$$

Where :

$$Zresidual = kZN*Zline$$
$$Zmutual = kZm*Zline$$

The fault location calculation

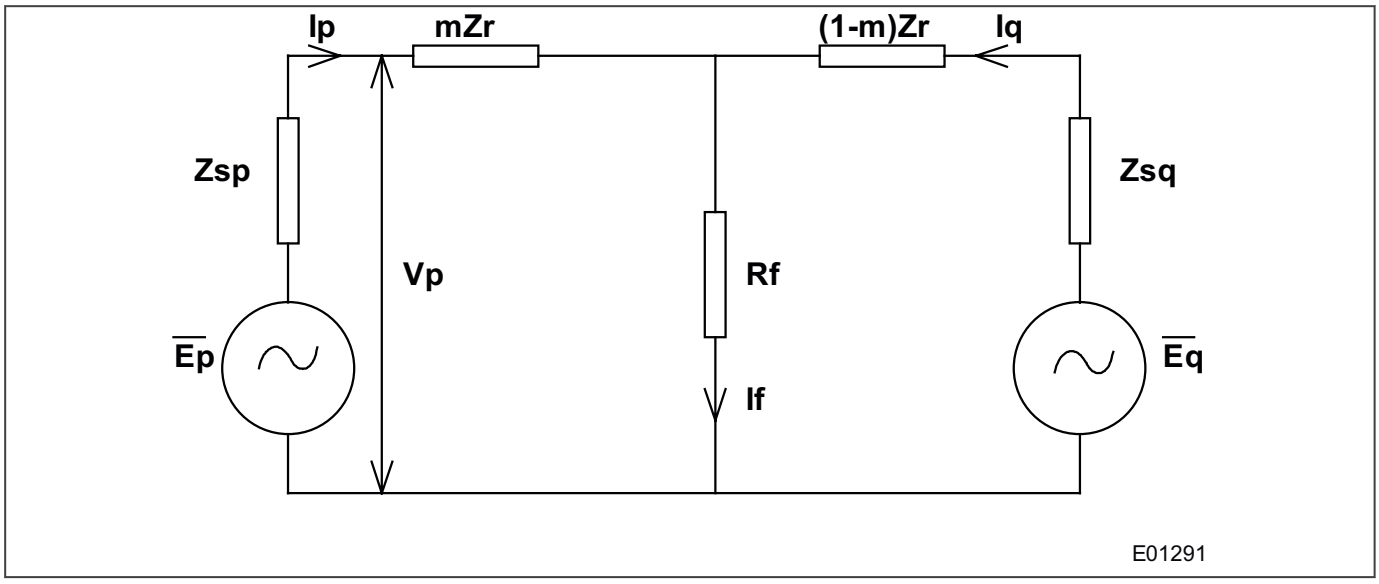


Figure 343: Two machine equivalent circuit

Fault location equation:

$$Vp = mIpZr + IfRf$$

Referring to the figure and equation, above.

The fault location calculation works by:

1. First obtaining the vectors to satisfy the above equation for the fault type specified by the phase selector.
2. Then estimating the phase of the fault current If.
3. Finally solving the above equation for the fault location m at the instant of time where If = 0.

Obtaining the vectors

Different sets of vectors are chosen depending on the type of fault identified by the phase selection algorithm. The calculation using fault location equation, above is applied for either a phase to earth fault or a phase to phase fault.

Thus, for a A phase to earth fault:

$$IpZr = Ia\ (Zline / \theta\ line) + In\ (Zresidual / / \theta\ residual)$$

and

$$Vp = VA$$

And for a A phase to B phase fault:

$$IpZr = Ia\ (\ Zline / \theta\ line\ ) - Ib\ (Zline / \theta\ line)$$

and

$$Vp = VA - VB$$

The calculation for an earth fault (A phase to earth fault equation, above) is modified when mutual compensation is used :

$$IpZr = Ia\ (Zline / \theta\ line) + In(Zresidual / / \theta\ residual\ ) + Im(Zmutual / / \theta\ mutual)$$

Solving the equation for the fault location

As the sine wave of If passes through zero, the instantaneous values of the sine waves Vp and □p can be used to solve the below equation for the fault location m. (The term IfRf being zero).

$$Vp = mIpZr + IfRf$$

This is determined by shifting the calculated vectors of Vp and IpZr by the angle (90° - angle of fault current) and then dividing the real component of Vp by the real component of IpZr. (See figure, below).

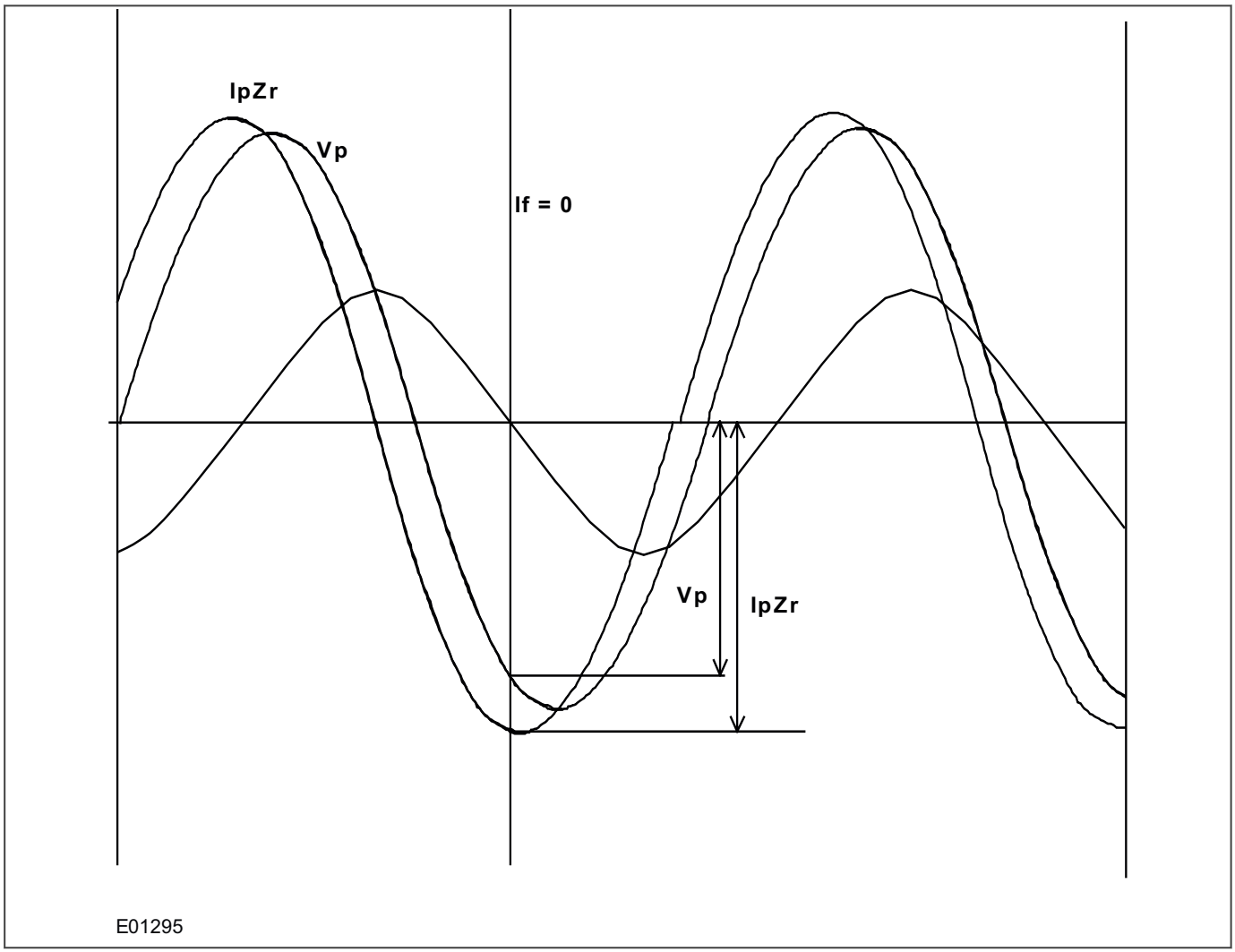


Figure 344: Fault locator selection of fault current zero

i.e.:

Phase advanced vector Vp

$$= |Vp| [\cos(s) + j\sin(s)] * [\sin(d) + j\cos(d)]$$

$$= |Vp| [-\sin(s-d) + j\cos(s-d)]$$

Phase advanced vector IpZr

$$= ||pZr| [\cos(e) + j\sin(e)] * [\sin(d) + j\cos(d)]$$

$$= ||pZr| [-\sin(e-d) + j\cos(e-d)]$$

Therefore, from equation 1:

$$m = Vp \div (Ip * Zr) \text{ at } If = 0$$

$$= Vp \sin(s-d)/(IpZr * \sin(e-d))$$

Where:

d = Angle of fault current If

s = Angle of Vp

e = Angle of IpZr

Thus, the relay evaluates m which is the fault location as a percentage of the fault locator line impedance setting and then calculates the output fault location by multiplying this by the line length setting. When calculated the fault location can be found in the fault record under the *VIEW RECORDS* column in the ***Fault Location*** cells. Distance to fault is available in kilometers, miles, impedance or percentage of line length.

19.4.3.7 MUTUAL COMPENSATION

Analysis of a ground fault on one circuit of a parallel over-head line shows that a fault locator positioned at one end of the faulty line will tend to over-reach while that at the other end will tend to under-reach. In cases of long lines with high mutual inductance, mutual zero sequence compensation can be used to improve the fault locator accuracy. The compensation is achieved by taking an input to the relay from the residual circuit of the current transformers in the parallel line.

Mutual compensation is available as needed by some protection functions as well as by the fault locator.

19.4.3.8 METERING

The metering calculations are continuously performed using the same fourier technique used by the fault locator. The results of these calculations are continuously updated and can be viewed using the relay user interface.

19.4.4 OPTO-INPUT TIME STAMPING

Each opto-input sample is time stamped within a tolerance of +/- 1 ms with respect to the Real Time Clock. These time stamps are used for the opto event logs and for the disturbance recording. The device needs to be synchronised accurately to an external clock source such as an IRIG-B signal or a master clock signal provided in the relevant data protocol.

For both the filtered and unfiltered opto-inputs, the time stamp of an opto-input change event is the sampling time at which the change of state occurred. If multiple opto-inputs change state at the same sampling interval, these state changes are reported as a single event.

19.5 CB CONDITION MONITORING

The device records various statistics related to each circuit breaker trip operation, allowing an accurate assessment of the circuit breaker condition to be determined. These statistics are available in the *CB CONDITION* column. The menu cells are register values only and cannot be set directly. They may be reset, however, during maintenance. The statistics monitored are:

- Total Current Broken: A register stores the total amount of current that the CB has broken is stored in an accumulator, giving at any time a measure of the total amount of current that the CB has broken since the value was last reset.
- Number of CB operations: A counter registers the number of CB trips that have been performed for each phase, giving at any time the total number of trips that the CB has performed since the value was last reset.
- CB Operate Time: A register stores the total amount of time the CB has transitioned from closed to open is stored in an accumulator, giving at any time a measure of the total time that the CB has spent tripping since the values was last reset.
- Excessive Fault Frequency: A counter registers the number of CB trips that have been performed for all phases, giving at any time the total number of trips performed since the value was last reset.

These statistics are available in the *CB CONDITION* column. The menu cells are register values only and cannot be set directly. They may be reset, however, during maintenance.

> *Note:*
> *When in Commissioning test mode the CB condition monitoring registers are not updated.*

Circuit breaker lockout, can be caused by the following circuit breaker condition monitoring functions:

- Maintenance lockout
- Excessive fault frequency lockout
- Broken current lockout

If the circuit breaker is locked out, the logic generates a lockout alarm

19.5.1 BROKEN CURRENT ACCUMULATOR

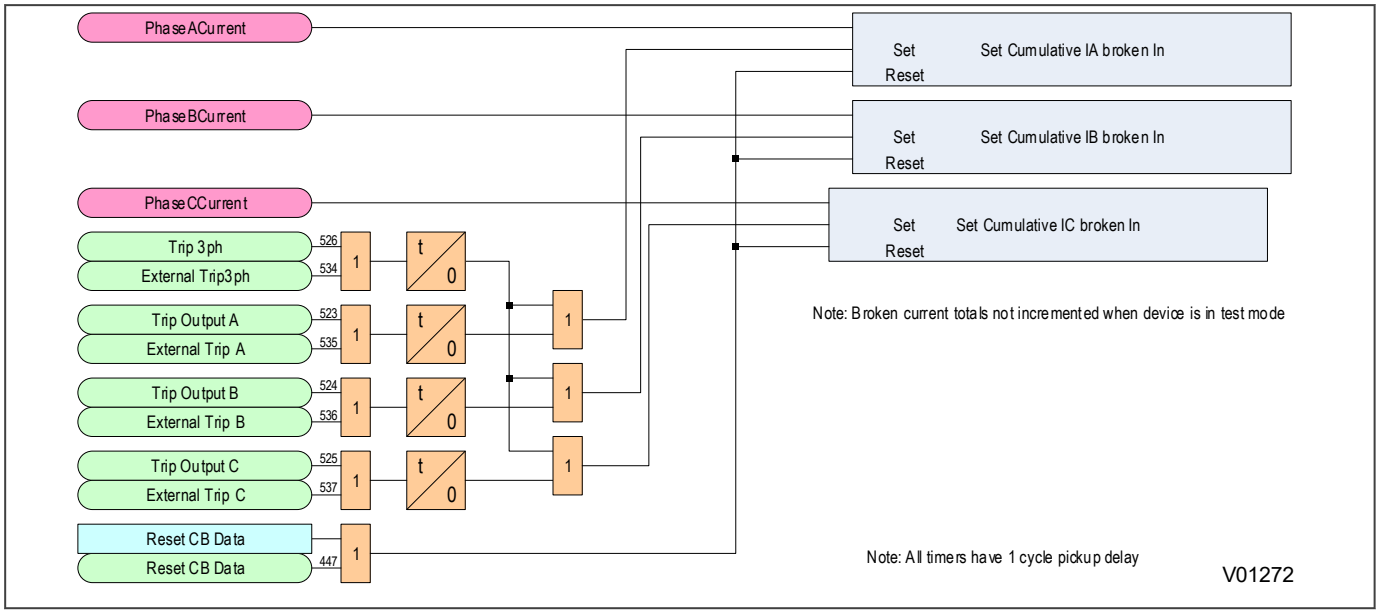


Figure 345: Broken current accumulator logic

19.5.2 BROKEN CURRENT ACCUMULATOR

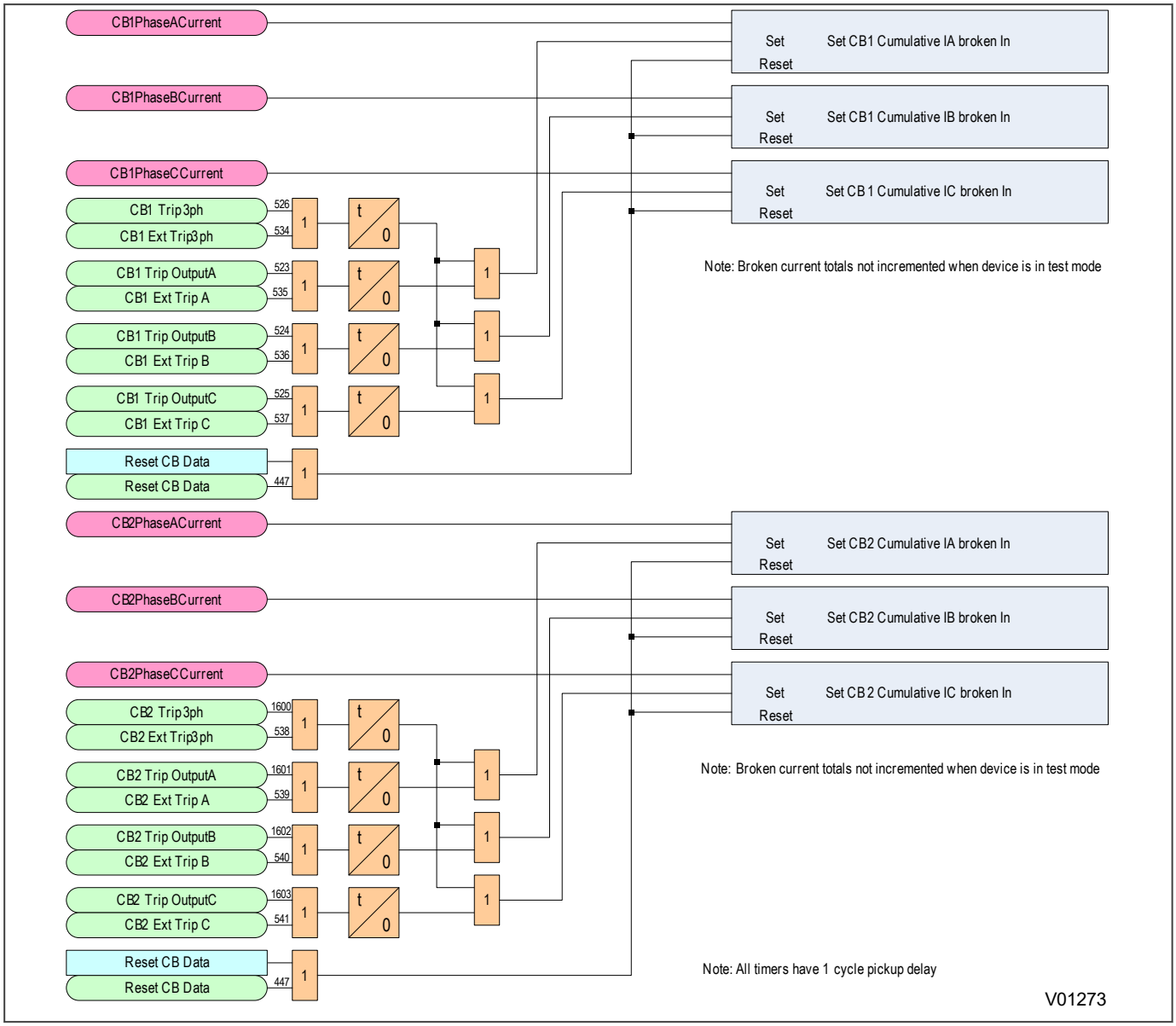


Figure 346: Broken current accumulator logic

19.5.3 CB TRIP COUNTER

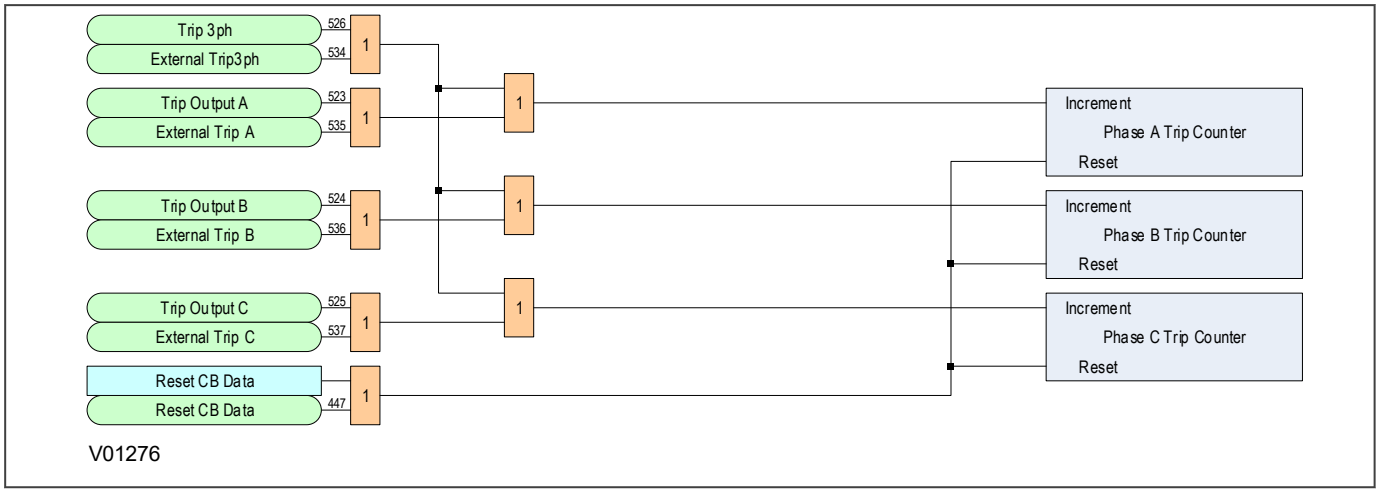


Figure 347: CB trip counter logic

19.5.4 CB TRIP COUNTER

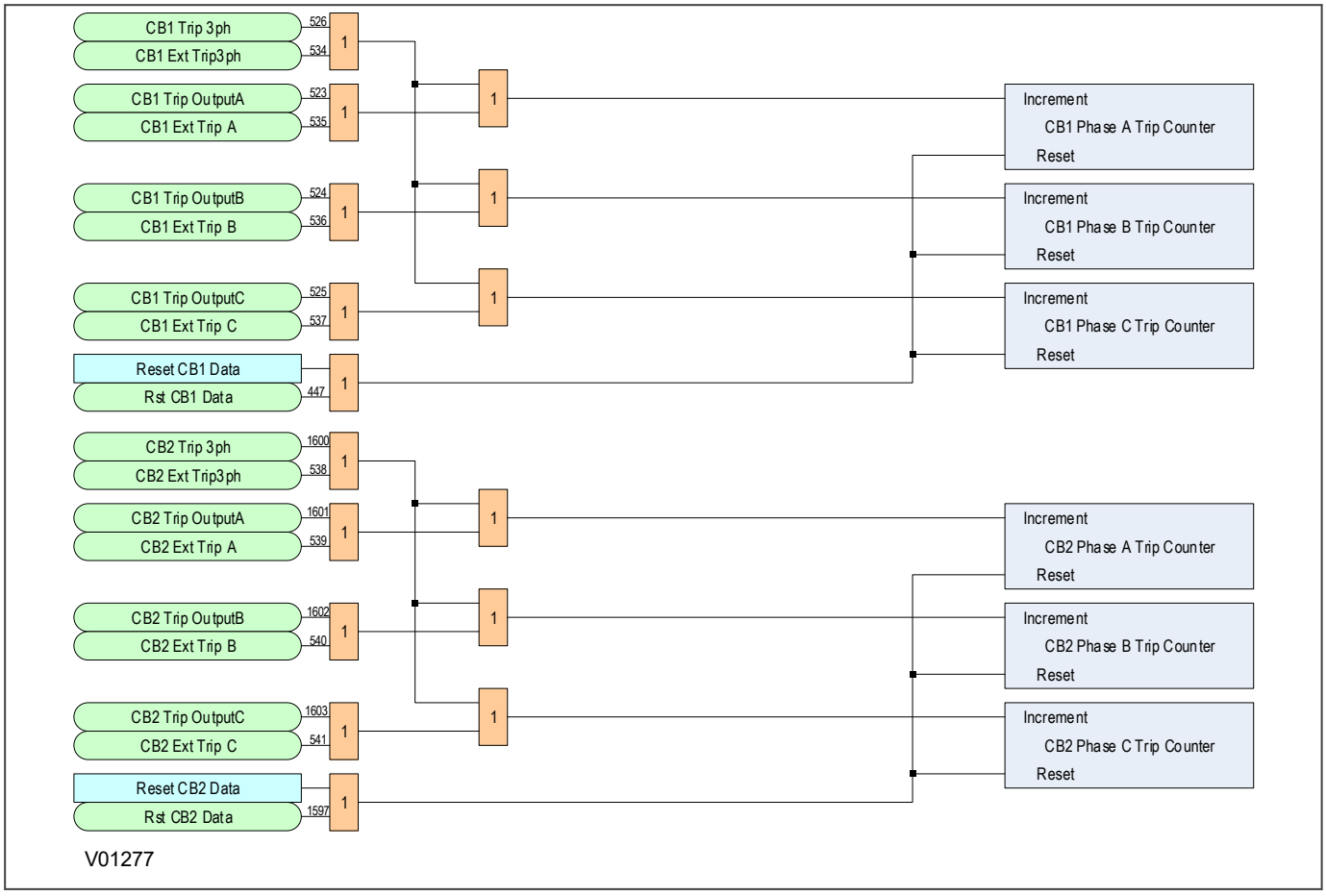


Figure 348: CB trip counter logic

19.5.5 CB OPERATING TIME ACCUMULATOR

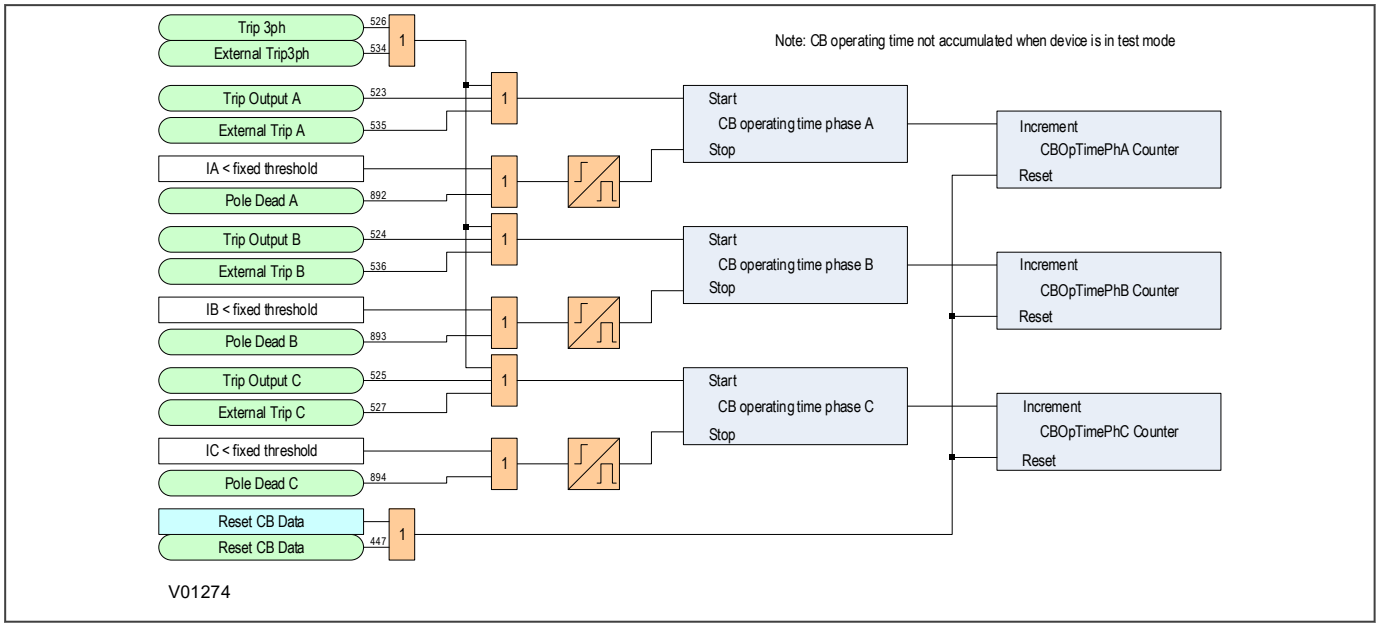


Figure 349: Operating time accumulator

19.5.6 CB OPERATING TIME ACCUMULATOR

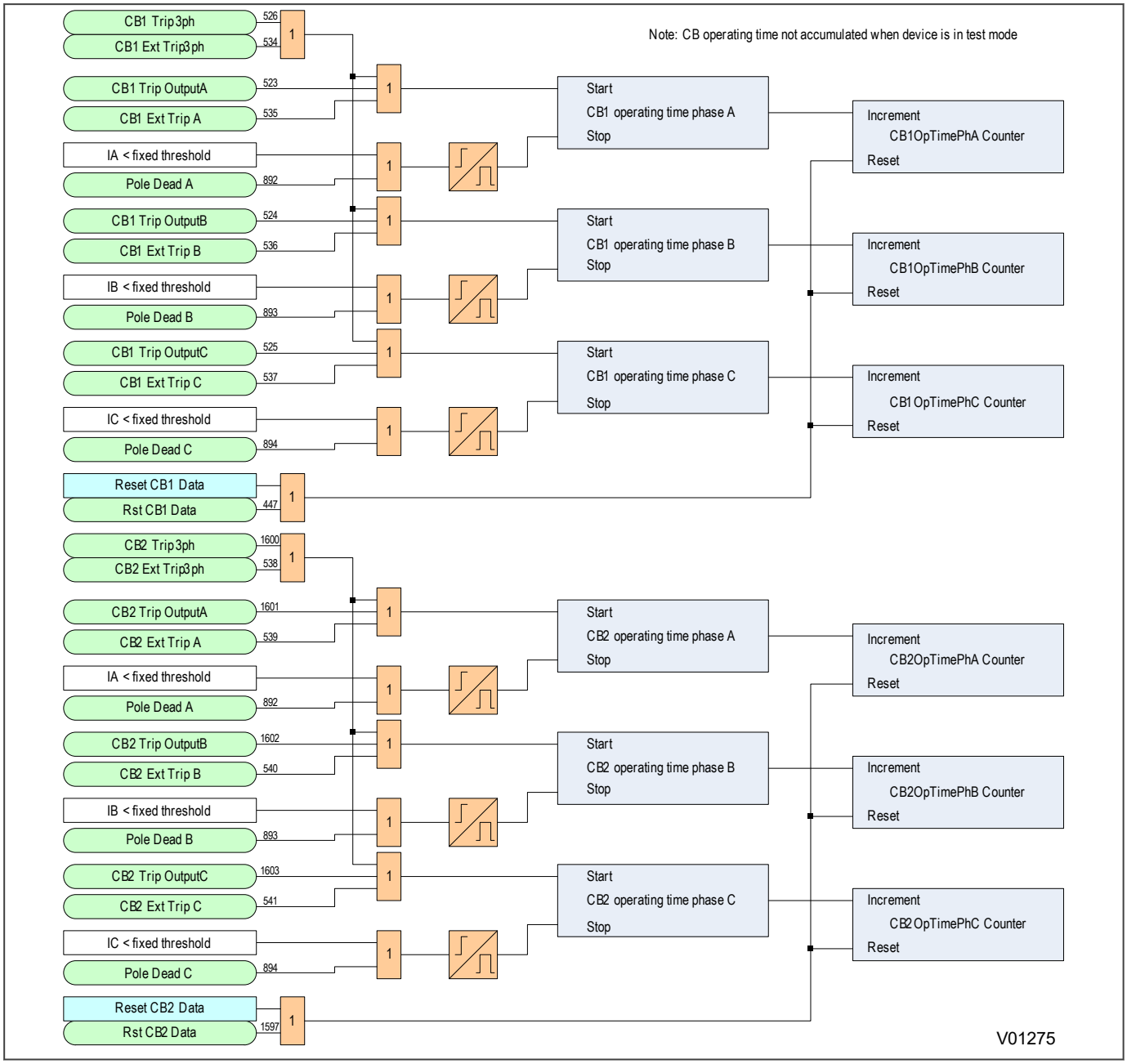


Figure 350: Operating time accumulator

19.5.7 EXCESSIVE FAULT FREQUENCY COUNTER

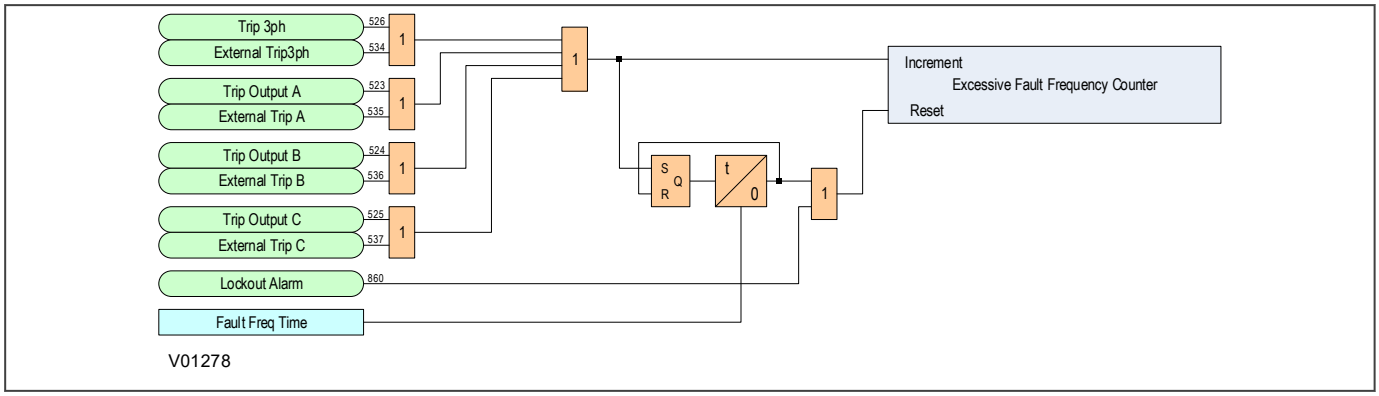


Figure 351: Excessive fault frequency logic

19.5.8 EXCESSIVE FAULT FREQUENCY COUNTER

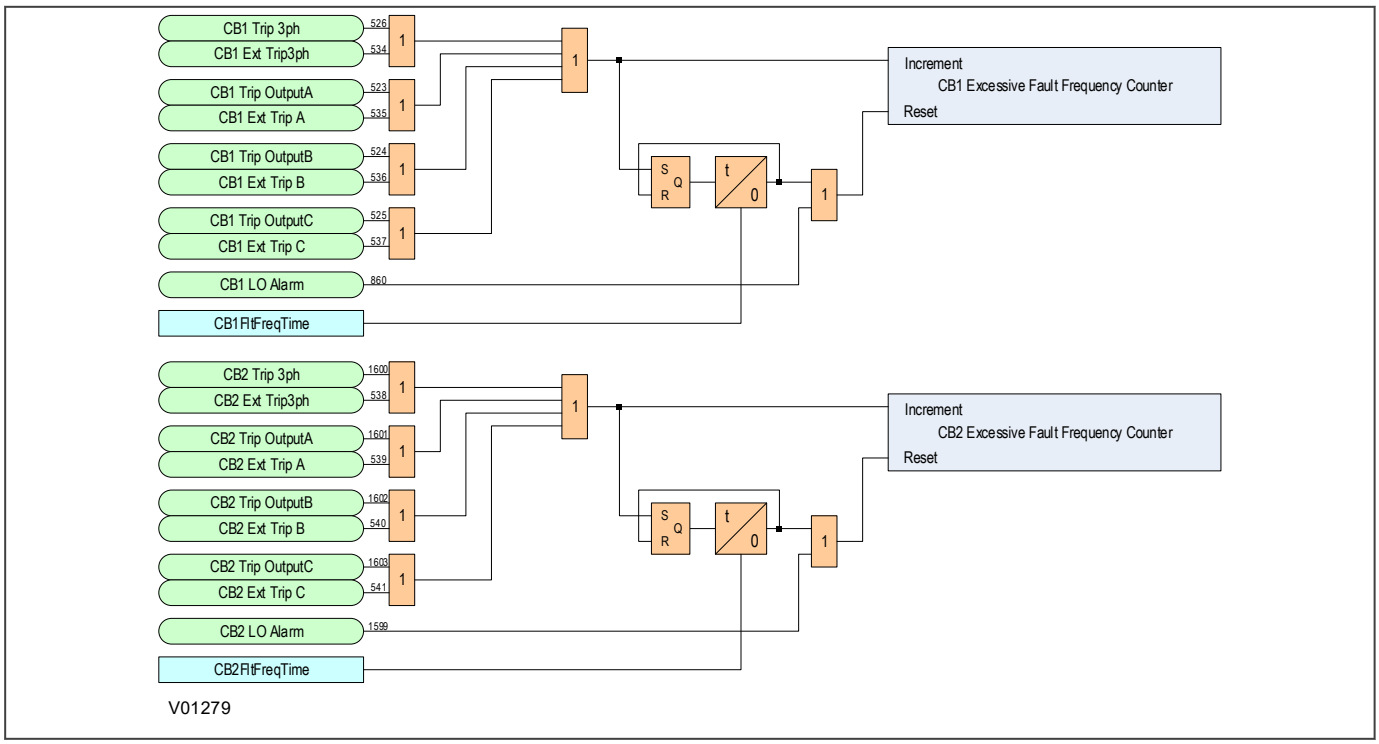


Figure 352: Excessive fault frequency logic

19.5.9 RESET LOCKOUT ALARM

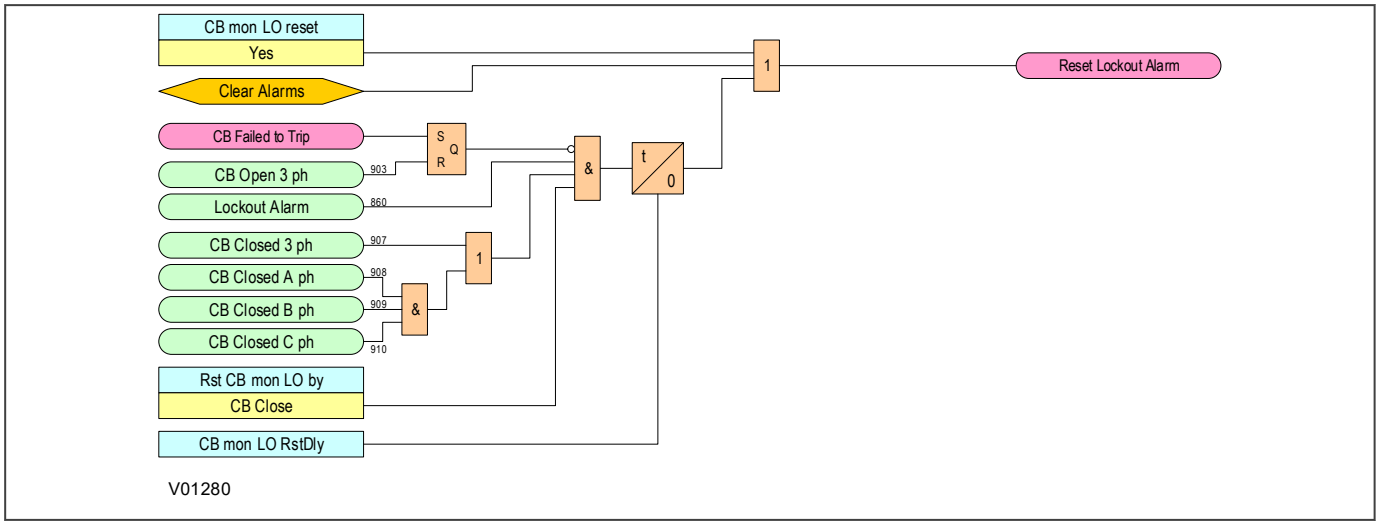


Figure 353: Reset lockout alarm logic

19.5.10 RESET LOCKOUT ALARM

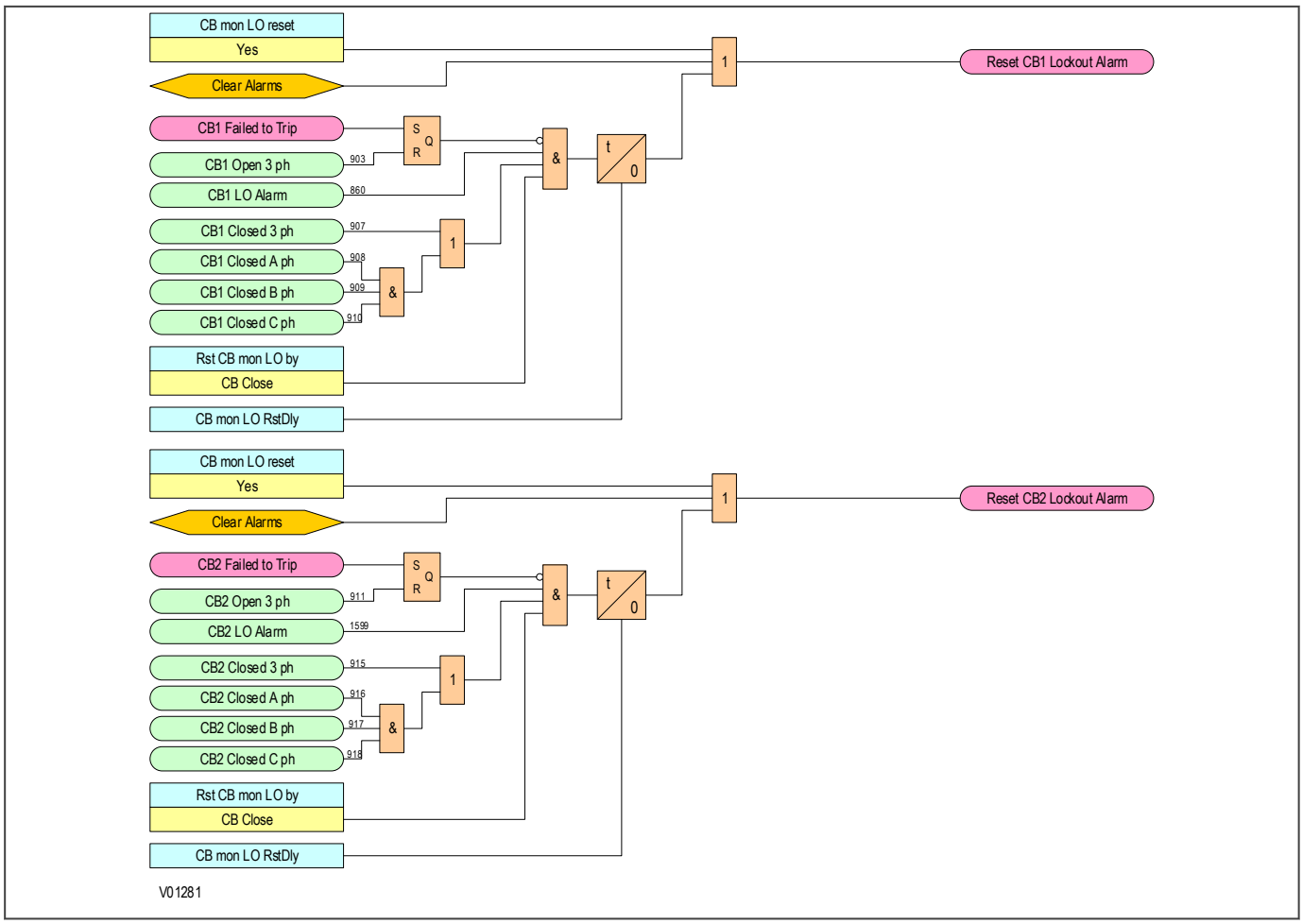


Figure 354: Reset lockout alarm logic

19.5.11 CB CONDITION MONITORING LOGIC

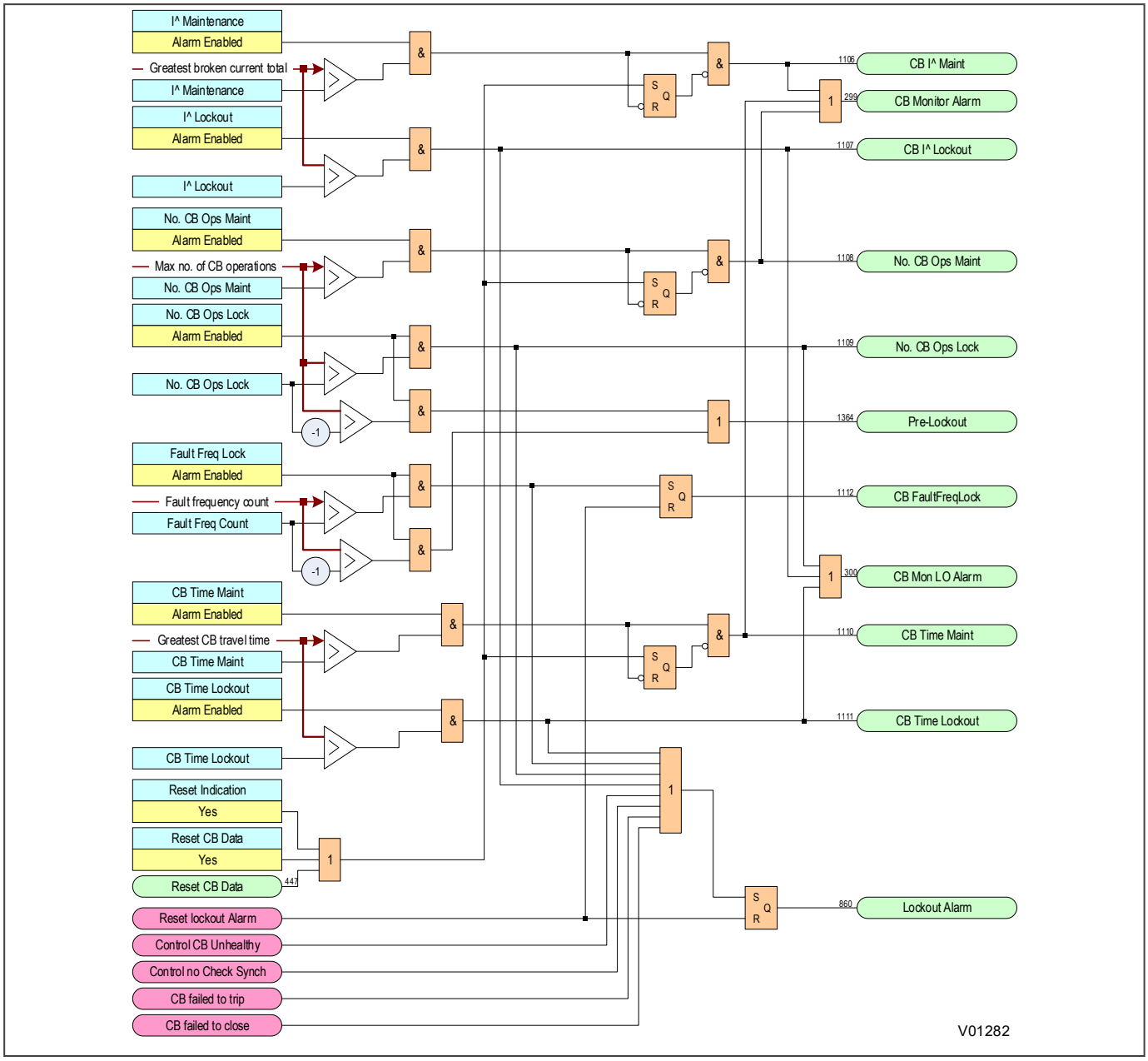


Figure 355: CB condition monitoring logic

19.5.12 CB CONDITION MONITORING LOGIC

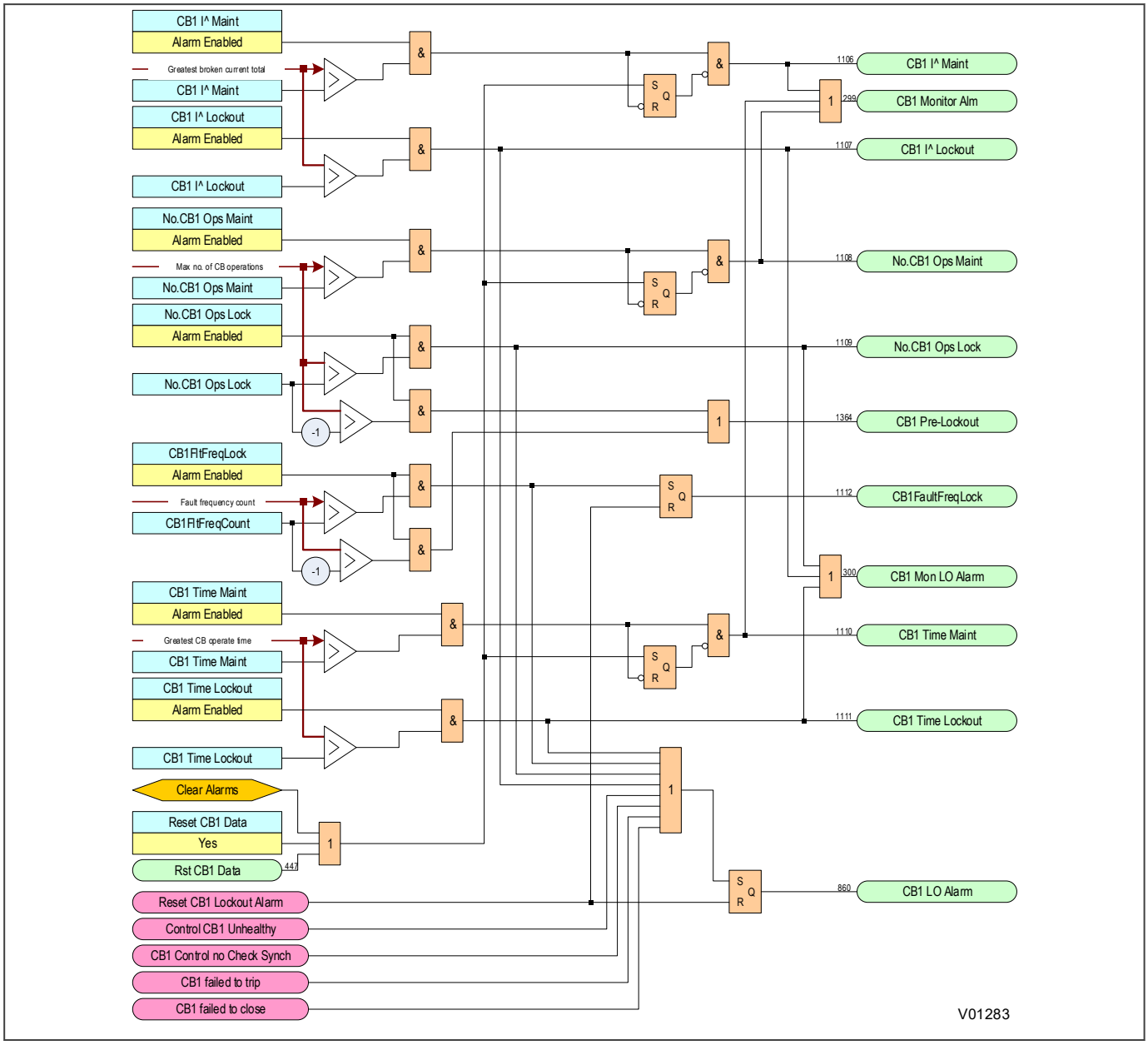


Figure 356: CB1 condition monitoring logic

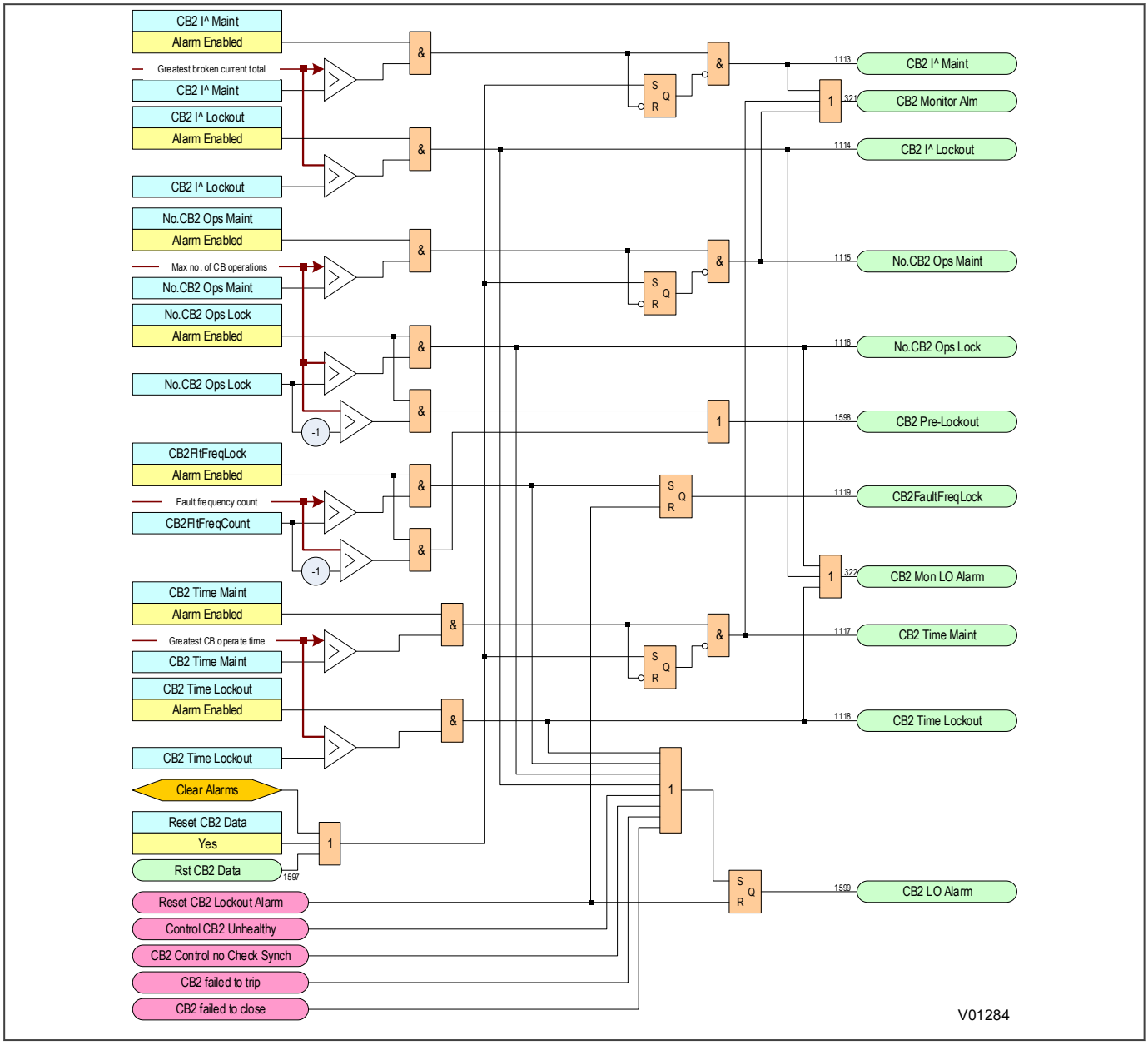


Figure 357: CB2 condition monitoring logic

19.5.13 RESET CIRCUIT BREAKER LOCKOUT

Lockout conditions caused by the circuit breaker condition monitoring functions can be reset according to the condition of the ***Rst CB mon LO*** by setting found in the *CB CONTROL* column. There are two options; `CB Close` and `User interface`.

If set to `CB Close`, a timer setting, ***CB mon LO RstDly***, becomes visible. When the circuit breaker closes, the ***CB mon LO RstDly*** time starts. The lockout is reset when the timer expires.

If set to `User Interface` then a command, ***CB mon LO reset***, becomes visible. This command can be used to reset the lockout from a user interface.

An Autoreclose lockout generates an Autoreclose lockout alarm. Autoreclose lockout conditions can be reset by various commands and setting options found under the *CB CONTROL* column.

If ***Res LO by CB IS*** is set to *Enabled*, a lockout is reset if the circuit breaker is successfully closed manually. For this, the circuit breaker must remain closed long enough so that it enters the “In Service” state.

If ***Res LO by UI*** is set to *Enabled*, the circuit breaker lockout can be reset from a user interface using the reset circuit breaker lockout command in the *CB CONTROL* column.

If ***Res LO by NoAR*** is set to *Enabled*, the circuit breaker lockout can be reset by temporarily generating an ***AR disabled*** signal.

If ***Res LO by TDelay*** is set to *Enabled*, the circuit breaker lockout is automatically reset after a time delay set in the ***LO Reset Time*** setting.

If ***Res LO by ExtDDB*** is *Enabled*, the circuit breaker lockout can be reset by activation of an external input mapped in the PSL to the relevant reset lockout DDB signal.

19.5.13.1 RESET CB LOCKOUT LOGIC DIAGRAM

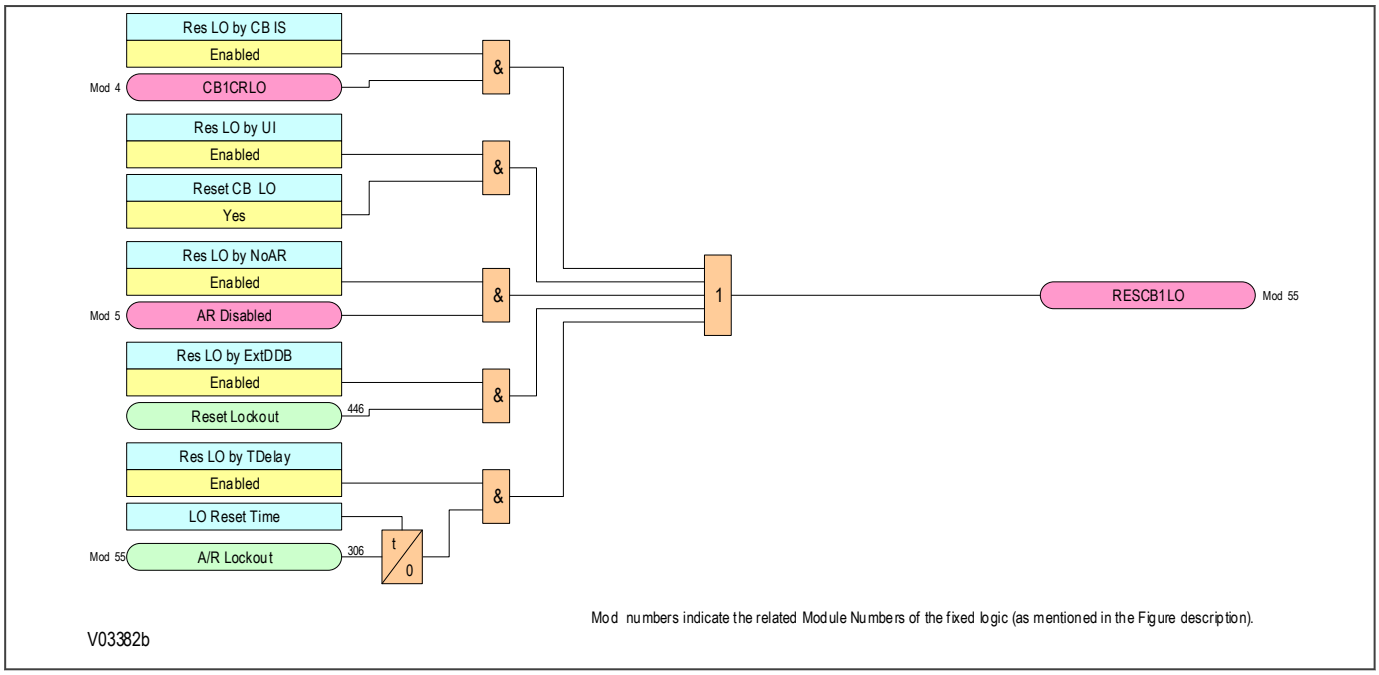


Figure 358: Reset circuit breaker lockout logic (module 57)

19.5.13.2 RESET CB LOCKOUT LOGIC DIAGRAM

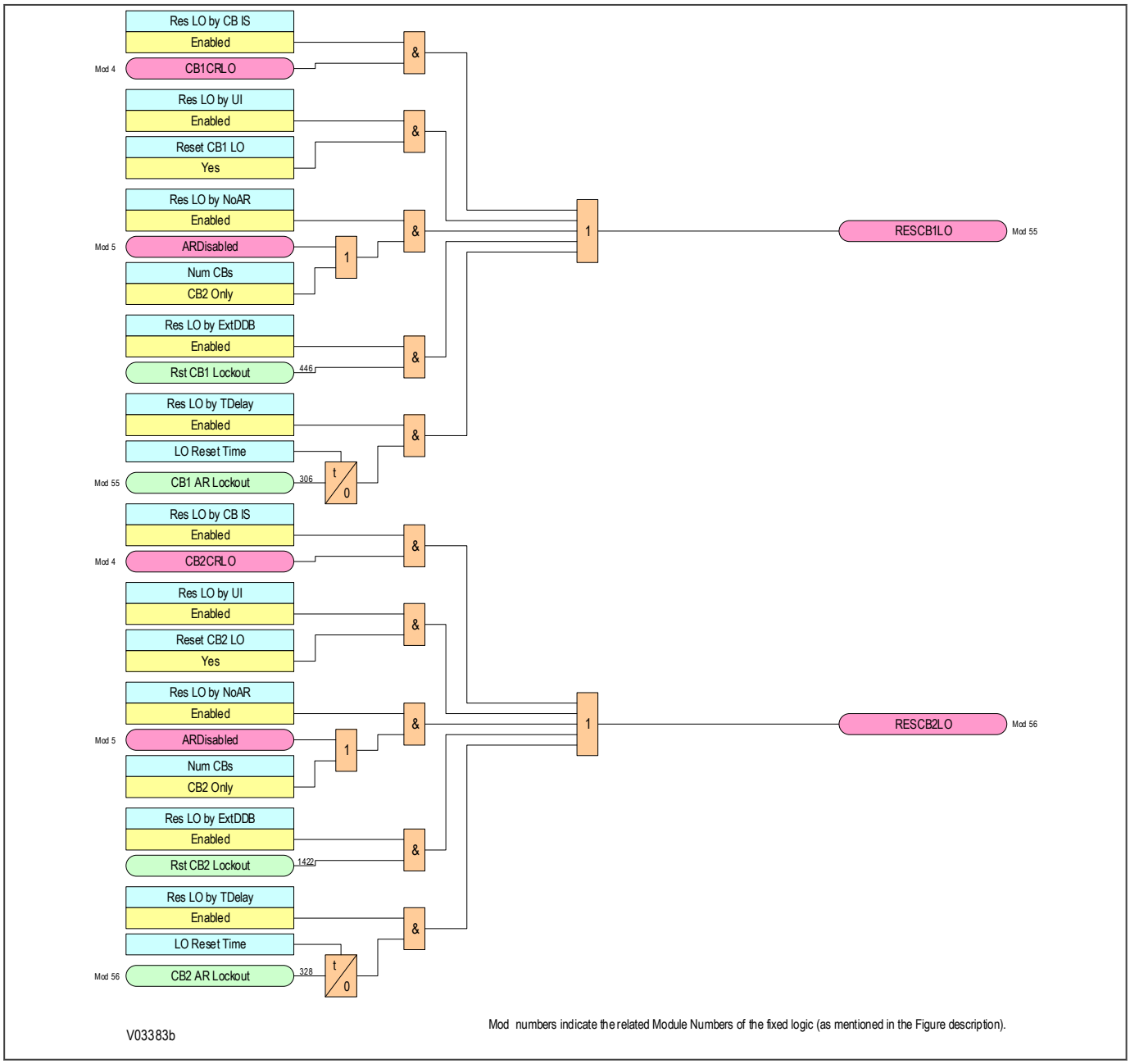


Figure 359: Reset circuit breaker lockout logic (modules 57 & 58)

19.5.14 APPLICATION NOTES

19.5.14.1 SETTING THE THRESHOLDS FOR THE TOTAL BROKEN CURRENT

Where power lines use oil circuit breakers (OCBs), changing of the oil accounts for a significant proportion of the switchgear maintenance costs. Often, oil changes are performed after a fixed number of CB fault operations. However, this may result in premature maintenance where fault currents tend to be low, because oil degradation may be slower than would normally be expected. The Total Current Accumulator (I^ counter) cumulatively stores the total value of the current broken by the circuit breaker providing a more accurate assessment of the circuit breaker condition.

The dielectric withstand of the oil generally decreases as a function of I^2t, where 'I' is the broken fault current and 't' is the arcing time within the interrupter tank. The arcing time cannot be determined accurately, but is generally dependent on the type of circuit breaker being used. Instead, you set a factor (***Broken I^***) with a value between 1 and 2, depending on the circuit breaker.

Most circuit breakers would have this value set to '2', but for some types of circuit breaker, especially those operating on higher voltage systems, a value of 2 may be too high. In such applications ***Broken I^*** may be set lower, typically 1.4 or 1.5.

The setting range for ***Broken I^*** is variable between 1.0 and 2.0 in 0.1 steps.

Note:
Any maintenance program must be fully compliant with the switchgear manufacturer's instructions.

19.5.14.2 SETTING THE THRESHOLDS FOR THE NUMBER OF OPERATIONS

Every circuit breaker operation results in some degree of wear for its components. Therefore routine maintenance, such as oiling of mechanisms, may be based on the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventative maintenance is due. Should maintenance not be carried out, the device can be set to lockout the autoreclose function on reaching a second operations threshold (***No. CB ops Lock***). This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Some circuit breakers, such as oil circuit breakers (OCBs) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonising of the oil, degrading its dielectric properties. The maintenance alarm threshold (setting ***No. CB Ops Maint***) may be set to indicate the requirement for oil dielectric testing, or for more comprehensive maintenance. Again, the lockout threshold ***No. CB Ops Lock*** may be set to disable autoreclosure when repeated further fault interruptions could not be guaranteed. This minimises the risk of oil fires or explosion.

19.5.14.3 SETTING THE THRESHOLDS FOR THE OPERATING TIME

Slow CB operation indicates the need for mechanism maintenance. Alarm and lockout thresholds (***CB Time Maint*** and ***CB Time Lockout***) are provided to enforce this. They can be set in the range of 5 to 500 ms. This time relates to the interrupting time of the circuit breaker.

19.5.14.4 SETTING THE THRESHOLDS FOR EXCESSSIVE FAULT FREQUENCY

Persistent faults will generally cause autoreclose lockout, with subsequent maintenance attention. Intermittent faults such as clashing vegetation may repeat outside of any reclaim time, and the common cause might never be investigated. For this reason it is possible to set a frequent operations counter, which allows the number of operations ***Fault Freq Count*** over a set time period ***Fault Freq Time*** to be monitored. A separate alarm and lockout threshold can be set.

19.6 CB STATE MONITORING

CB State monitoring is used to verify the open or closed state of a circuit breaker. Most circuit breakers have auxiliary contacts through which they transmit their status (open or closed) to control equipment such as IEDs. These auxiliary contacts are known as:

- 52A for contacts that follow the state of the CB
- 52B for contacts that are in opposition to the state of the CB

This device can be set to monitor both of these types of circuit breaker state indication. If the state is unknown for some reason, an alarm can be raised.

Some CBs provide both sets of contacts. If this is the case, these contacts will normally be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5 s ***CB Status Time*** time delay. An output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

In the CB CONTROL column there is a setting called ***CB Status Input***. This cell can be set at one of the following four options:

- None
- 52A
- 52B
- Both 52A and 52B

Where *None* is selected no CB status is available. Where only 52A is used on its own then the device will assume a 52B signal opposite to the 52A signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52B is used. If both 52A and 52B are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table:

Auxiliary Contact Position		CB State Detected	Action
52A	52B		
Open	Closed	Breaker open	Circuit breaker healthy
Closed	Open	Breaker closed	Circuit breaker healthy
Closed	Closed	CB failure	Alarm raised if the condition persists for greater than 5 s
Open	Open	State unknown	Alarm raised if the condition persists for greater than 5 s. ***CB State Detected*** becomes ***CB Failure***.

In the internal logic of the P40, the breaker position used in the algorithm is considered to be open when the **CB State Detected is Breaker Open**. In all other cases, the breaker position is considered to be closed. Therefore, during operation of the circuit breaker, if the condition '52A=52B=0' or '52A=52B=1' is encountered, the circuit breaker is considered to be closed.

The Circuit Breaker status can be monitored in the serial and Ethernet data protocols. For example, IEC 60870-5-103, DNP 3.0 and IEC 61850.

IEC 60870-5-103 protocol: The CB status can be monitored from individual private information numbers.

DNP 3.0 protocol: The CB status can be monitored from individual Binary Inputs.

IEC 61850 protocol: The CB status can be monitored in ‘XCBR’ Logical Node(s).

19.6.1 CB STATE MONITOR LOGIC DIAGRAM

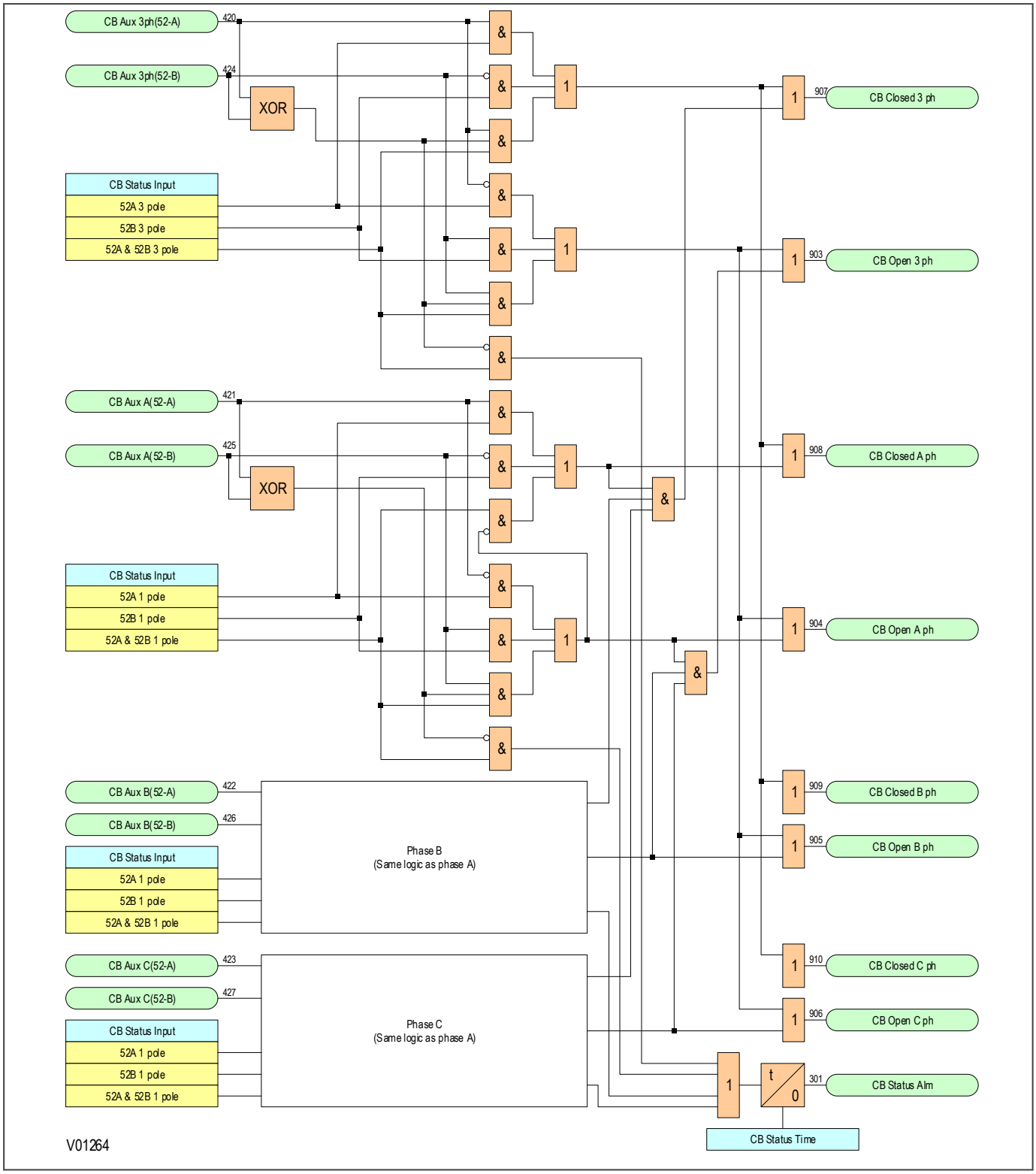


Figure 360: CB state monitor logic (module 1)

19.6.2 CB STATE MONITOR

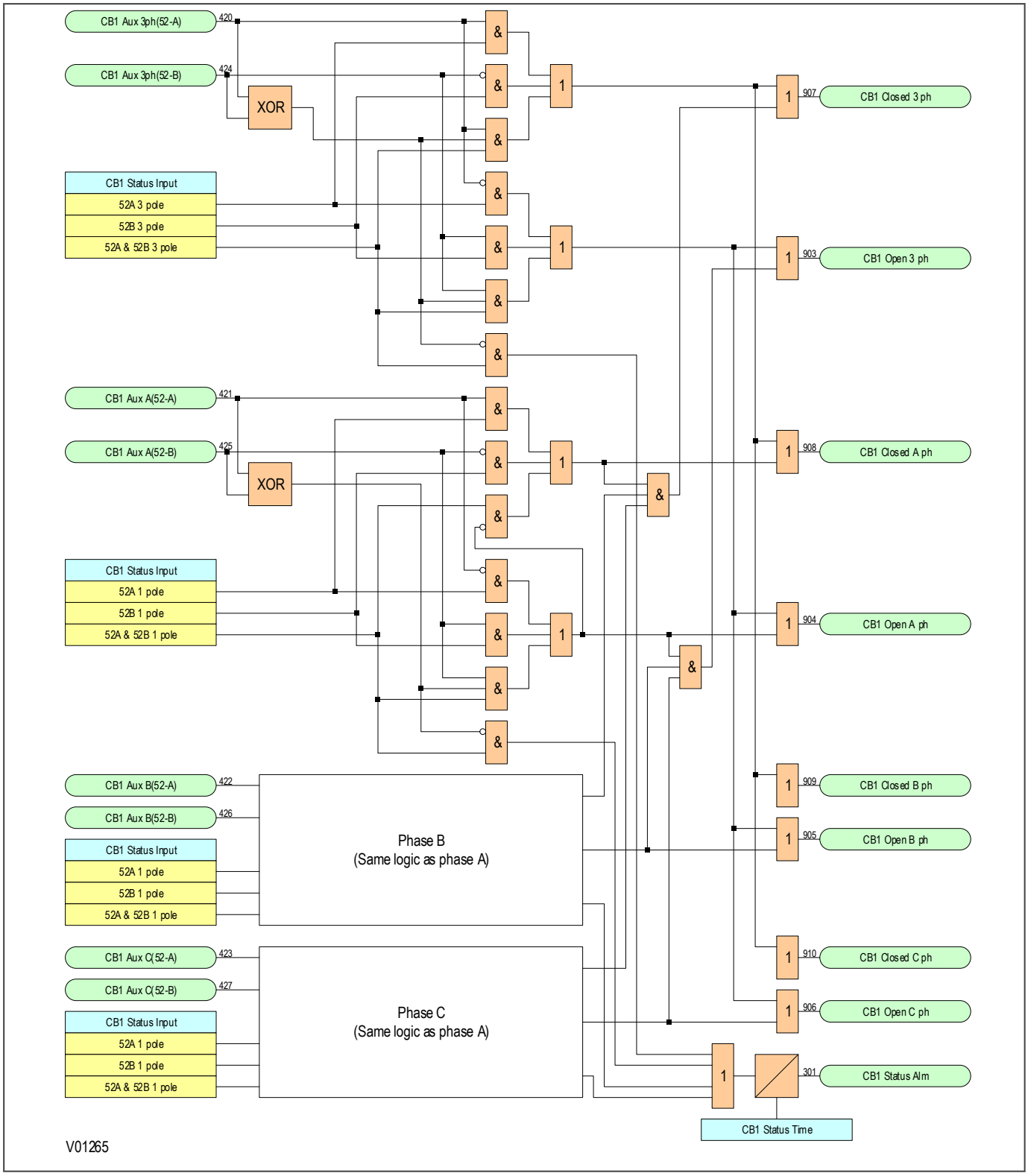


Figure 361: CB state logic (module 1)

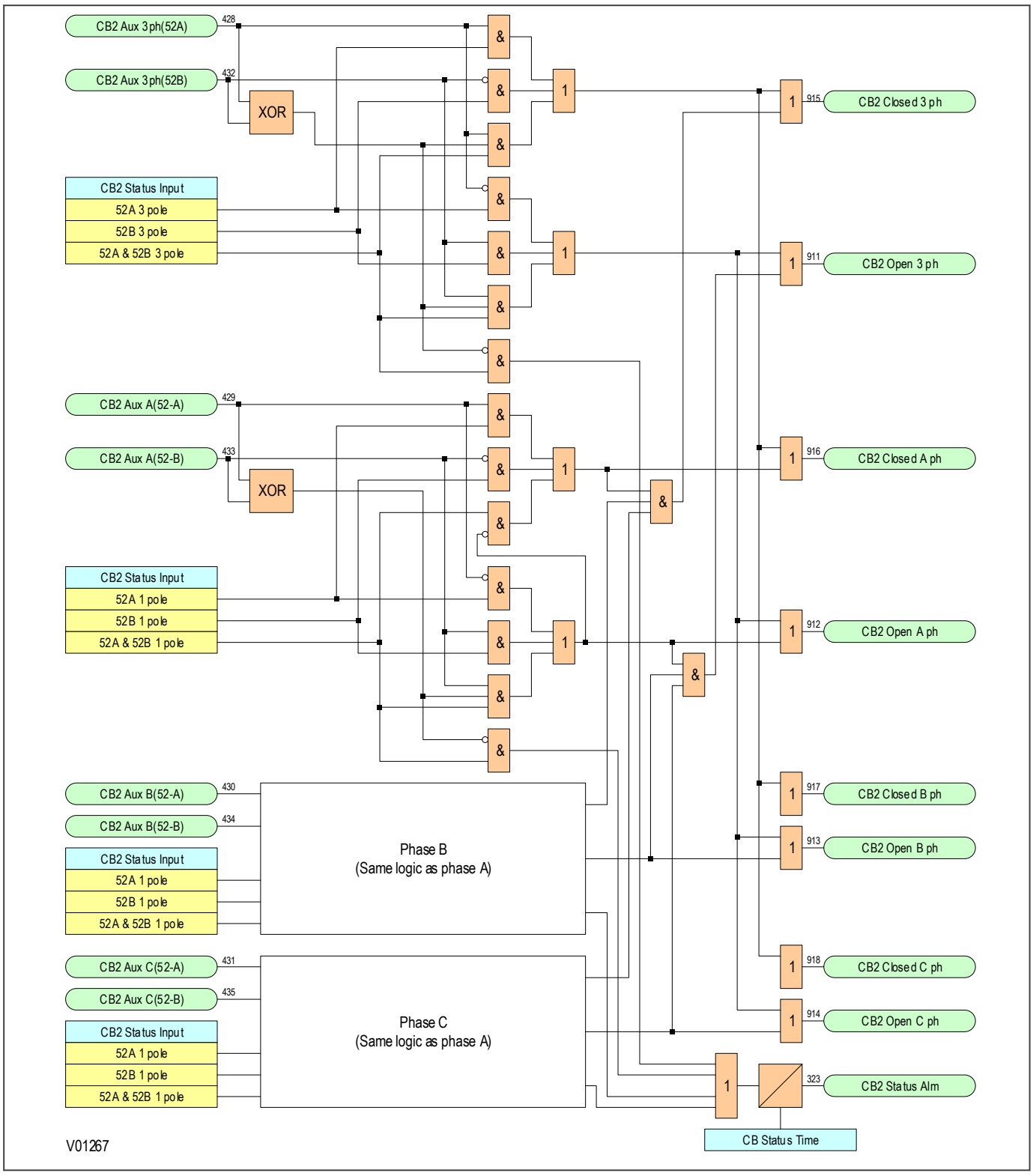


Figure 362: CB state logic (module 2)

19.7 CIRCUIT BREAKER CONTROL

Although some circuit breakers do not provide auxiliary contacts, most provide auxiliary contacts to reflect the state of the circuit breaker. These are:

- CBs with 52A contacts (where the auxiliary contact follows the state of the CB)
- CBs with 52B contacts (where the auxiliary contact is in the opposite state from the state of the CB)
- CBs with both 52A and 52B contacts

Circuit Breaker control is only possible if the circuit breaker in question provides auxiliary contacts. The ***CB Status Input*** cell in the *CB CONTROL* column must be set to the type of circuit breaker. If no CB auxiliary contacts are available then this cell should be set to `None`, and no CB control will be possible.

The ***CB control by*** cell is used to enable or disable local control options, remote control options, and combinations of both.

The output contact can be set to operate following a time delay defined by the setting ***Man Close Delay***. One reason for this delay is to give personnel time to safely move away from the circuit breaker following a CB close command.

The control close cycle can be cancelled at any time before the output contact operates by any appropriate trip signal, or by activating the ***Reset Close Dly*** DDB signal.

The length of the trip and close control pulses can be set via the ***Trip Pulse Time*** and **Close Pulse Time** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

The ***Reset Lockout by*** setting is used to enable or disable the resetting of lockout automatically from a manual close after the time set by ***Man Close RstDly***.

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) an alarm is generated after the relevant trip or close pulses have expired. These alarms can be viewed on the LCD display, remotely, or can be assigned to output contacts using the programmable scheme logic (PSL).

Note:
*The **CB Healthy Time** and **Sys Check time** set under this menu section are applicable to manual circuit breaker operations only. These settings are duplicated in the AUTORECLOSE menu for autoreclose applications.*

The ***Lockout Reset*** and ***Reset Lockout by*** settings are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example) and autoreclose lockouts.

The device includes the following options for control of a single circuit breaker:

- The IED menu (local control)
- The CB Open/Close keys and the SLD on the graphical HMI
- The opto-inputs (local control)
- SCADA communication (remote control)

19.7.1 CB CONTROL USING THE IED MENU

You can control manual trips and closes with the ***CB Trip/Close*** command in the *SYSTEM DATA* column. This can be set to `No Operation`, `Trip`, or `Close` accordingly.

For this to work you have to set the ***CB control by*** cell to option 1 `Local`, option 3 `Local + Remote`, option 5 `Opto+Local`, option 7 `Opto+Local+Remote` or option 8 `L&R Key` in the *CB CONTROL* column.

19.7.2 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

19.7.2.1 CIRCUIT BREAKER CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the circuit breaker selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the ***CB Control by*** setting is selected, to option 1 `Local`, option 3 `Local+Remote`, option 5 `Opto+local`, option 7 `Opto+Rem+local` or option 8 `L/R Key` in the *CB CONTROL* column users are allowed to use the Trip and Close Key on the front panel to operate the CB.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***CB control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is green and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is red and the REMOTE mode is selected. ***The L/R Key Status*** DDB status is stored in non-volatile memory, so that it's status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant which you require to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the Open or Close key to operate

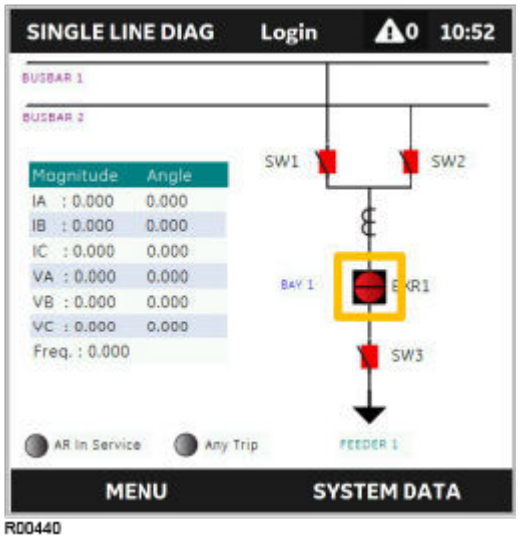


Figure 363: HMI SLD display

For the Circuit Breaker Commands from HMI, additional checks are done:

If the CB is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "Control by" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "Control by" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "Control by" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - In Remote Control".

If the associated local DDB is set to local, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

19.7.3 CB CONTROL USING THE OPTO-INPUTS

Certain applications may require the use of push buttons or other external signals to control the various CB control operations. It is possible to connect such push buttons and signals to opto-inputs and map these to the relevant DDB signals.

For this to work, you have to set the ***CB control by*** cell to option 4 *opto*, option 5 *Opto+Local*, option 6 *Opto +Remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

19.7.4 REMOTE CB CONTROL

Remote CB control can be achieved from some of the serial and Ethernet data protocols, or by using the MiCOM S1 Agile settings application software.

For this to work, you have to set the ***CB control by*** cell to option 2 *Remote*, option 3 *Local+Remote*, option 6 *Opto+remote*, option 7 *Opto+Rem+local* or option 8 *L/R Key* in the *CB CONTROL* column.

We recommend that you allocate separate relay output contacts for remote CB control and protection tripping. This allows you to select the control outputs using a simple local/remote selector switch as shown below. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

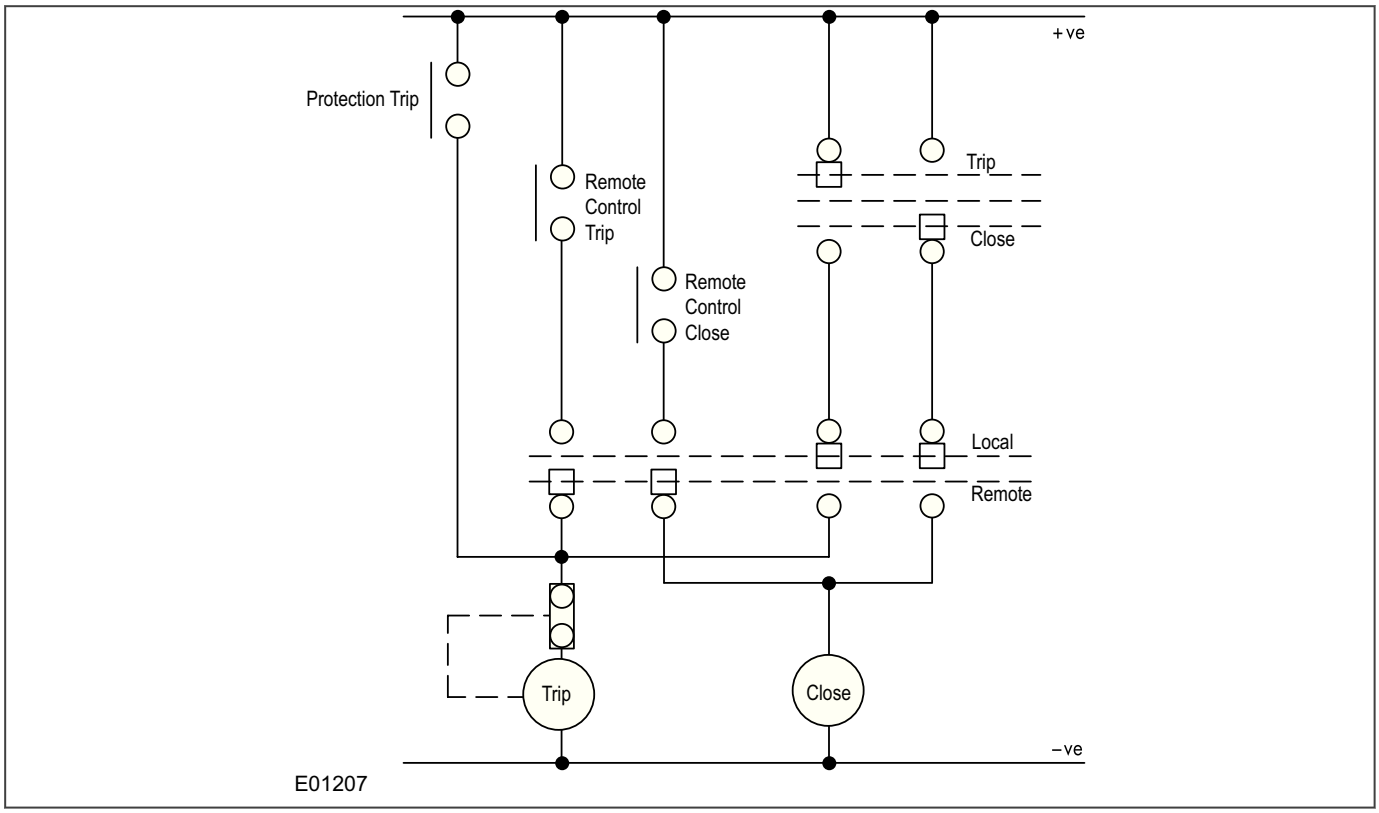


Figure 364: Remote control of circuit breaker

DNP 3.0 protocol: The CB and switch positions can be controlled from Binary Outputs/Control Relay Output Blocks.

IEC 61850 protocol: The CB and switch positions can be controlled in the ‘CSWI’ Logical Node that is linked to the ‘XCBR’ Circuit Breaker Logical Node and 'XSWI' switch Logical Nodes. For Control Authority as per IEC 61850, it is necessary to select ***CB Control by*** cell as option 8 *L/R Key*.

19.7.5 CB HEALTHY CHECK

A CB Healthy check is available if required. This facility accepts an input to one of the opto-inputs to indicate that the breaker is capable of closing (e.g. that it is fully charged). A time delay can be set with the setting ***CB Healthy Time***. If the CB does not indicate a healthy condition within the time period following a Close command, the device will lockout and alarm.

19.7.6 SYNCHRONISATION CHECK

Where the check synchronism function is set, this can be enabled to supervise manual circuit breaker Close commands. A circuit breaker Close command will only be issued if the Check Synchronisation criteria are satisfied. A time delay can be set with the setting ***Sys Check time.*** If the Check Synchronisation criteria are not satisfied within the time period following a Close command the device will lockout and alarm.

19.7.7 CB CONTROL AR IMPLICATIONS

An ***Auto Close CB*** signal from the Auto-close logic bypasses the ***Man Close Delay*** time, and the ***CB Close*** output operates immediately to close the circuit breaker.

If Autoreclose is used it may be desirable to block its operation when performing a manual close. In general, the majority of faults following a manual closure are permanent faults and it is undesirable to allow automatic reclosure.

To ensure that Autoreclose is not initiated for a manual circuit breaker closure on to a pre-existing fault, the ***CB IS Time*** (circuit breaker in service time) setting in the *AUTORECLOSE* menu should be set for the desired time window. This setting ensures that Autoreclose initiation is inhibited for a period equal to setting ***CB IS Time*** following a manual circuit breaker closure. If a protection operation occurs during the inhibit period, Autoreclose is not initiated.

Following manual circuit breaker closure, if either a single phase or a three phase fault occur, the circuit breaker is tripped three phase, but Autoreclose is not locked out for this condition.

19.7.8 CB CONTROL LOGIC DIAGRAM

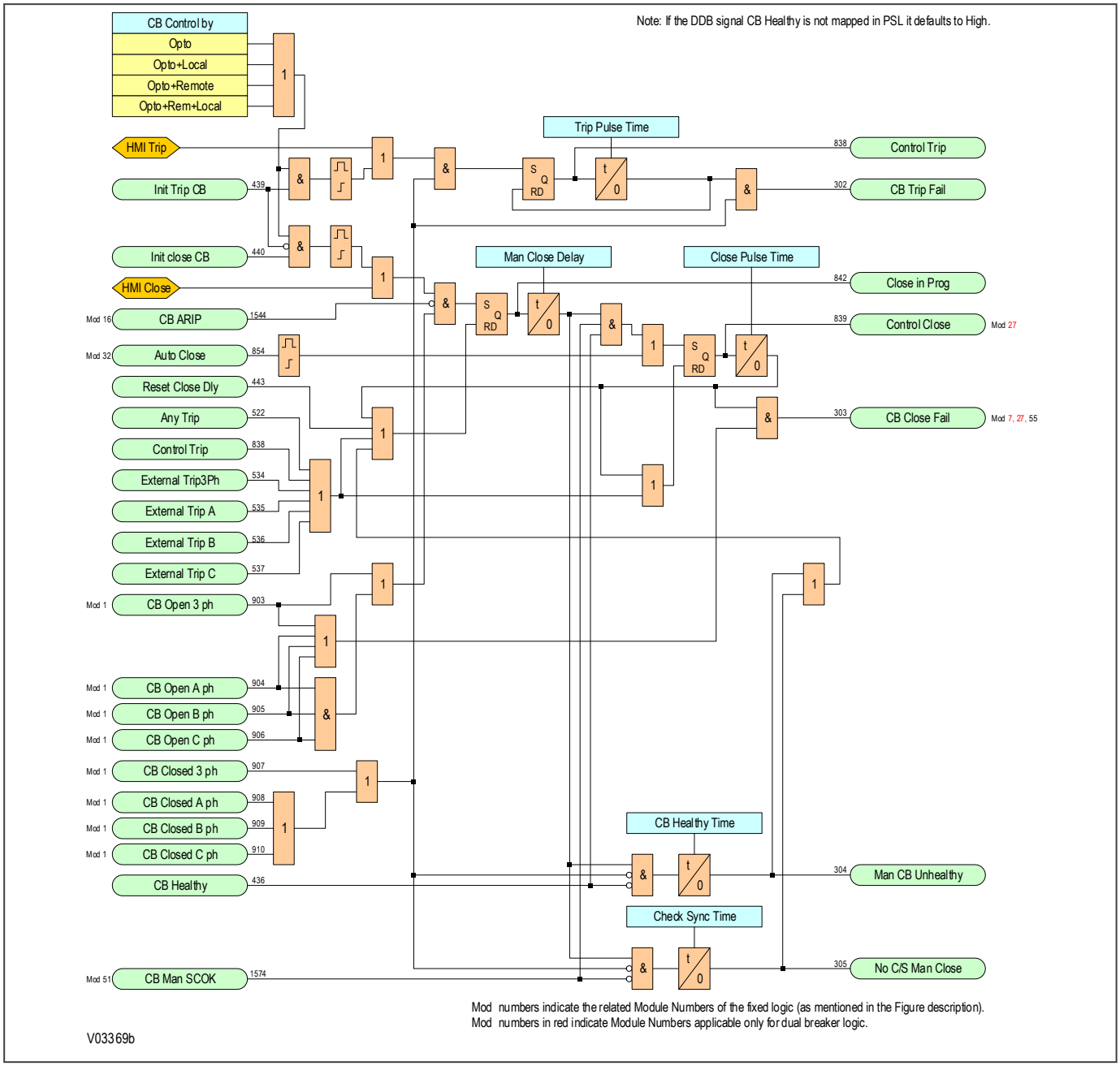


Figure 365: CB control logic (module 43)

19.7.9 CB CONTROL LOGIC DIAGRAM

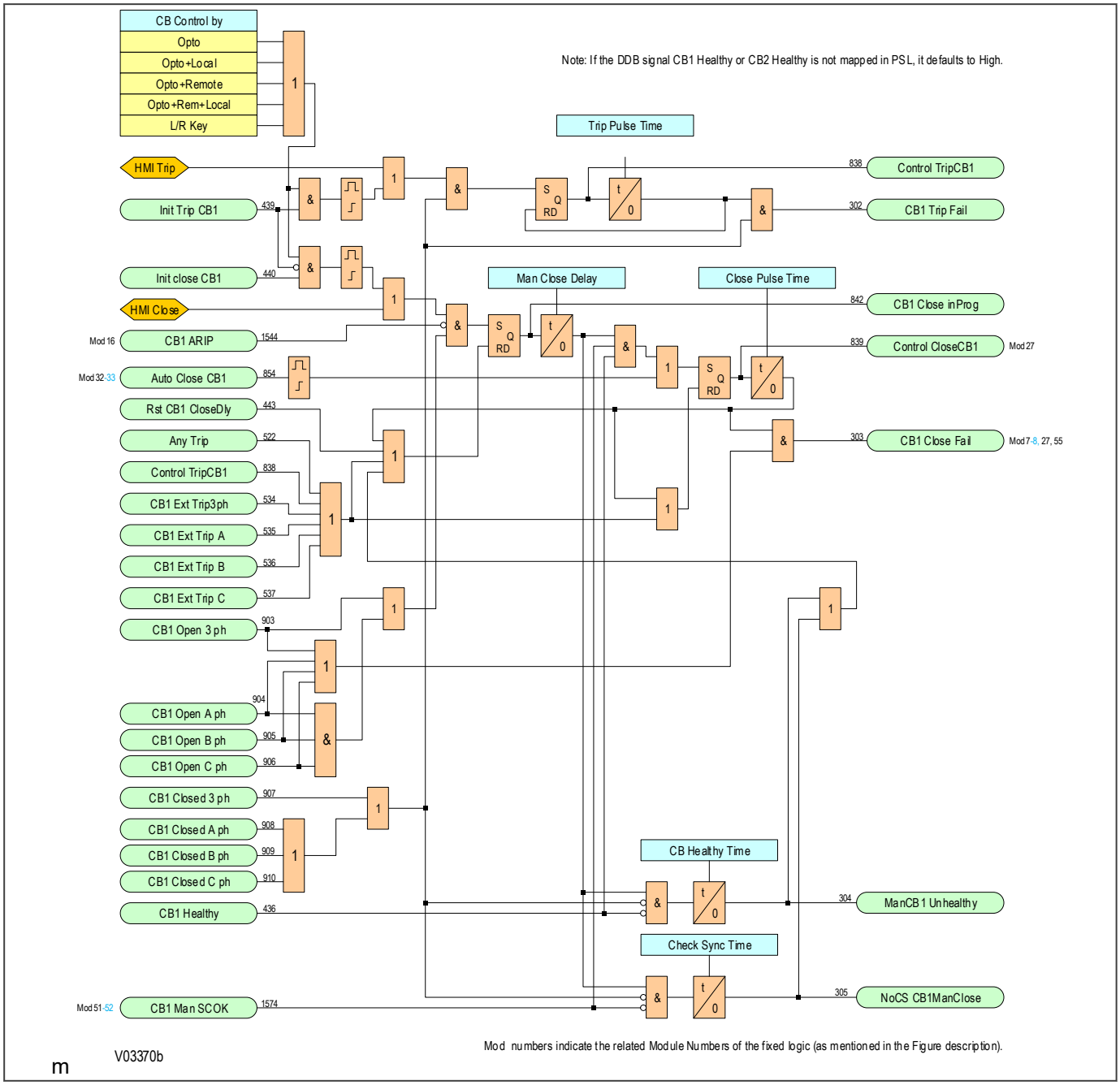


Figure 366: CB1 control logic (module 43)

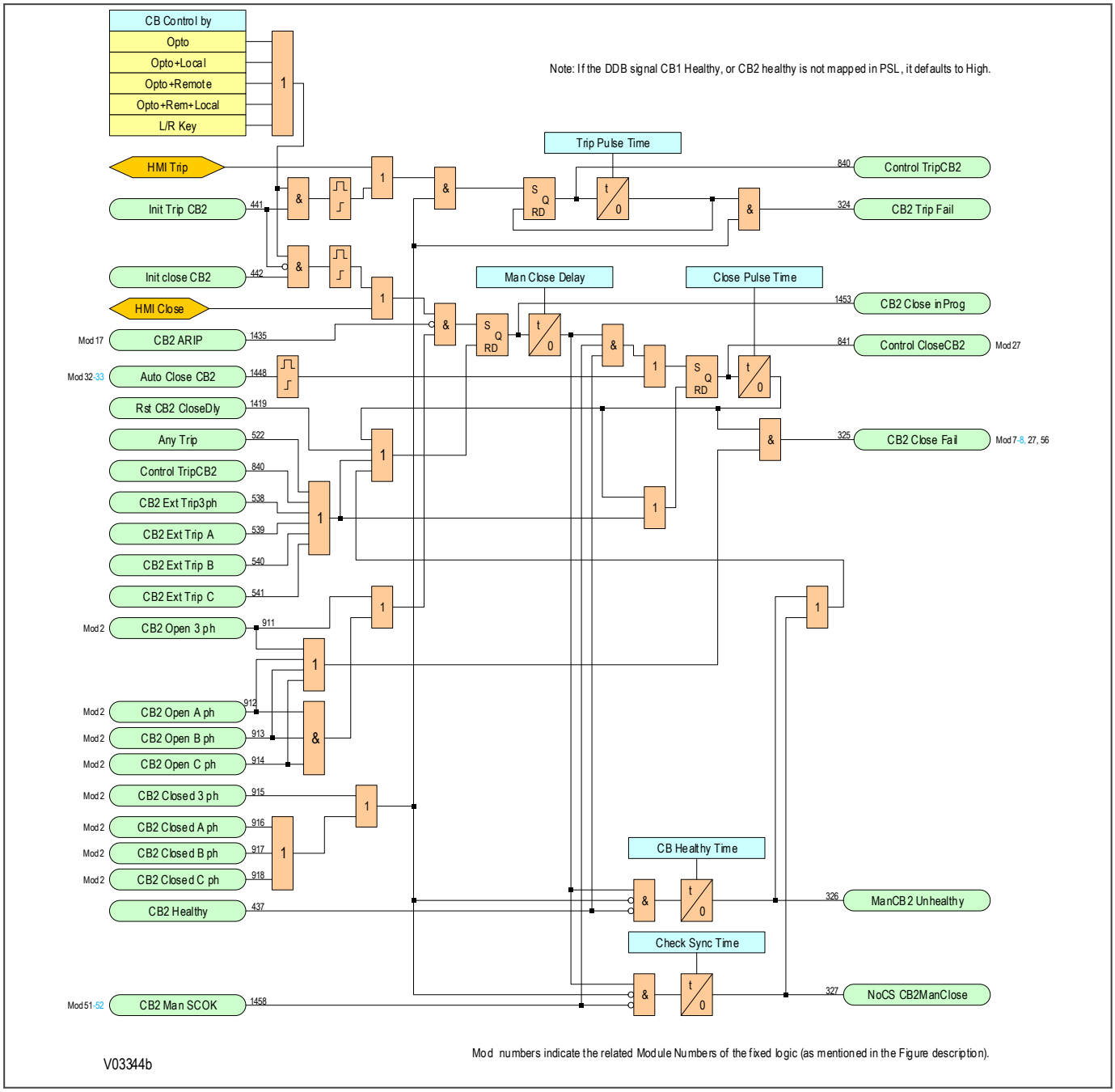


Figure 367: CB2 control logic (module 44)

19.8 POLE DEAD FUNCTION

The Pole Dead Logic is used to determine and indicate that one or more phases of the line are not energised. A Pole Dead condition is determined either by measuring:

- the line currents and/or voltages, or
- by monitoring the status of the circuit breaker auxiliary contacts, as shown by dedicated DDB signals.

It can also be used to block operation of underfrequency and undervoltage elements where applicable.

19.8.1 POLE DEAD LOGIC

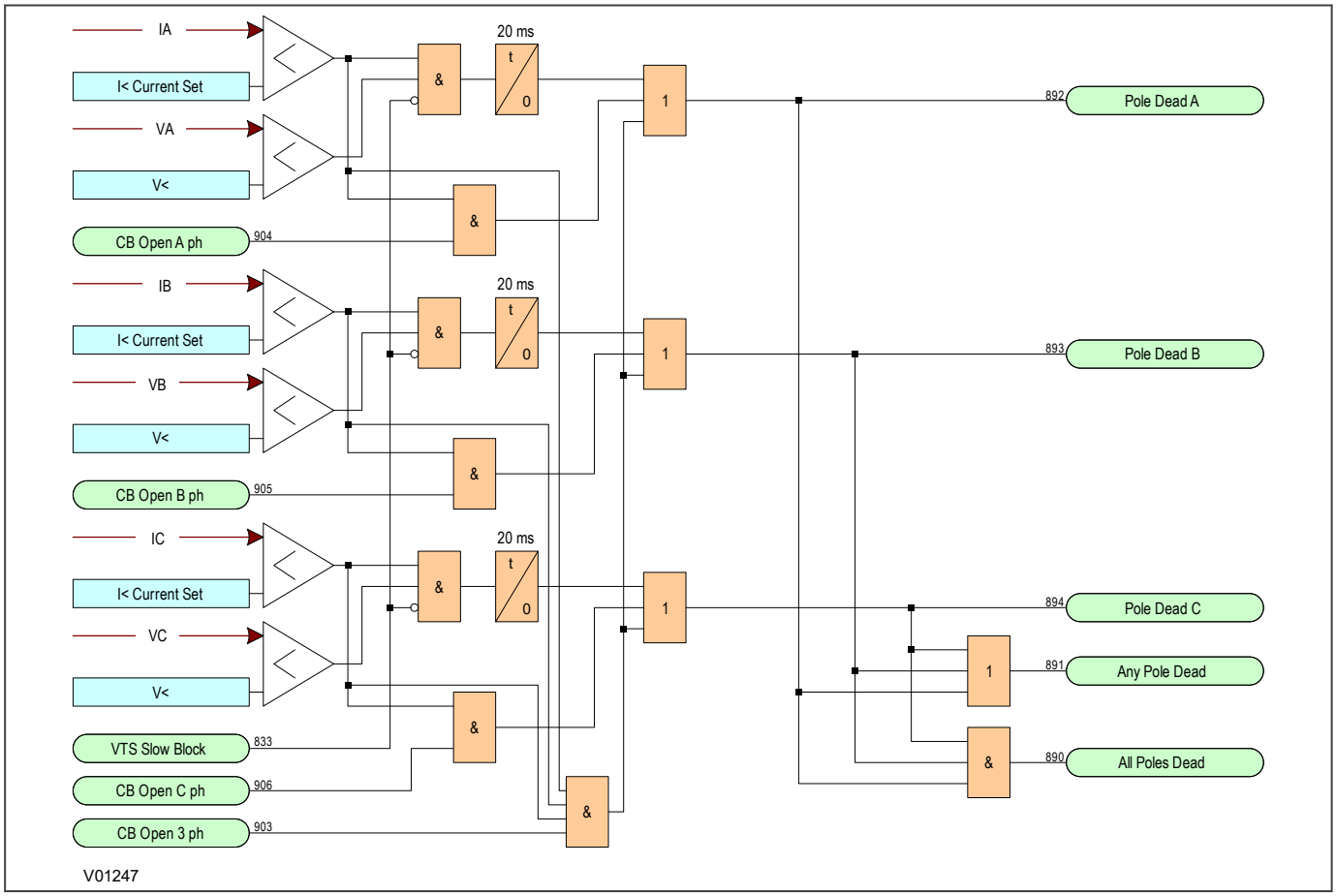


Figure 368: Pole dead logic

If both the line current and voltage values fall below a certain threshold, or a CB Open condition is asserted from the state control logic, the device initiates a Pole Dead condition. The current and voltage thresholds can be set with the ***I< Current Set*** and the ***V< settings*** respectively, in the *CBFAIL&P.DEAD* column.

If one or more poles are dead, the device indicates which phase is dead and asserts the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal is accompanied by the ***All Poles Dead*** signal.

If the VT fails, a ***VTS Slow Block*** signal is taken from the VTS logic to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds.

Note:
If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the IED for a correct pole dead indication.

19.8.2 POLE DEAD LOGIC

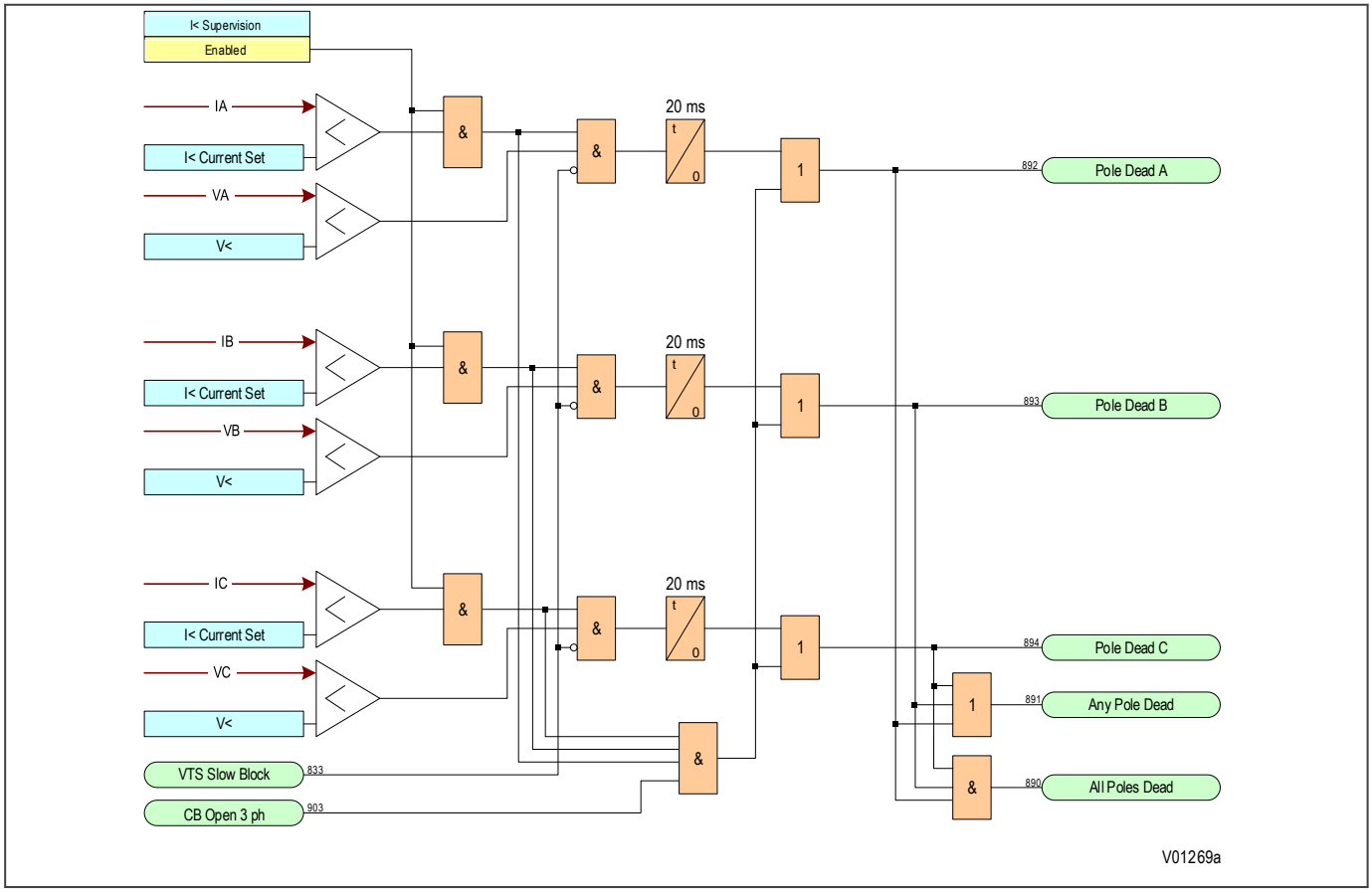


Figure 369: Pole dead logic

If both the line current and voltage values fall below a certain threshold, or a CB Open condition is asserted from the state control logic, the device initiates a Pole Dead condition. The current and voltage thresholds can be set with the ***I< Current Set*** and the ***V< settings*** respectively, in the *CBFAIL&P.DEAD* column.

If one or more poles are dead, the device indicates which phase is dead and asserts the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal is accompanied by the ***All Poles Dead*** signal.

If the VT fails, a ***VTS Slow Block*** signal is taken from the VTS logic to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds.

Note:
If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the IED for a correct pole dead indication.

19.9 SYSTEM CHECKS

In some situations it is possible for both "bus" and "line" sides of a circuit breaker to be live when a circuit breaker is open - for example at the ends of a feeder that has a power source at each end. Therefore, it is normally necessary to check that the network conditions on both sides are suitable, before closing the circuit breaker. This applies to both manual circuit breaker closing and autoreclosing. If a circuit breaker is closed when the line and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to connected machines.

The System Checks functionality involves monitoring the voltages on both sides of a circuit breaker, and if both sides are live, performing a synchronisation check to determine whether any differences in voltage magnitude, phase angle or frequency are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration, and for autoreclosing, on the selected autoreclose program. For example, on a feeder with delayed autoreclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing. The second line end circuit breaker now sees a live bus and a live line.

If there is a parallel connection between the ends of the tripped feeder the frequencies will be the same, but any increased impedance could cause the phase angle between the two voltages to increase. Therefore just before closing the second circuit breaker, it may be necessary to perform a synchronisation check, to ensure that the phase angle between the two voltages has not increased to a level that would cause unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism altogether and the frequency at one end could "slip" relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line-end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

19.9.1 SYSTEM CHECKS IMPLEMENTATION

The System Checks function provides *Live/Dead Voltage Monitoring*, two stages of *Check Synchronisation* and *System Split* indication.

The System Checks function is enabled or disabled by the ***System Checks*** setting in the *CONFIGURATION* column. If ***System Checks*** is disabled, the *SYSTEM CHECKS* menu becomes invisible, and a ***SysChks Inactive*** DDB signal is set.

The System Checks functionality can also be enabled or disabled by the ***System Checks*** setting in the *SYSTEM CHECKS* column. For the Systems Checks functionality to be enabled, both the ***System Checks*** setting in the *CONFIGURATION* column AND the ***System Checks*** setting in the *SYSTEM CHECKS* column must be enabled. For the System Checks functionality to be disabled, either the ***System Checks*** setting in the *CONFIGURATION* column OR the ***System Checks*** setting in the *SYSTEM CHECKS* column must be enabled. In the latter case, the ***SysChks Inactive*** DDB signal is set.

The system Checks functionality can also be enabled or disabled individually for each circuit breaker by the ***System Checks CB1*** and ***System Checks CB2*** settings in the *SYSTEM CHECKS* column. For the Systems Checks functionality to be enabled, both the ***System Checks*** setting in the *CONFIGURATION* column AND the relevant setting (***System Checks CB1*** and/or ***System Checks CB2***) in the *SYSTEM CHECKS* column must be enabled. For the System Checks functionality to be disabled, either the ***System Checks*** setting in the *CONFIGURATION* column OR the relevant setting (***System Checks CB1*** and/or ***System Checks CB2***) in the *SYSTEM CHECKS* column must be enabled. In the latter case, the ***SysChks Inactive*** DDB signal is set.

19.9.1.1 VT CONNECTIONS

The device provides inputs for a three-phase "Main VT" and at least one single-phase VT for check synchronisation. Depending on the primary system arrangement, the Main VT may be located on either the line-side of the busbar-side of the circuit breaker, with the Check Sync VT on the other. Normally, the Main VT is located on the line-side (as per the default setting), but this is not always the case. For this reason, a setting is provided where you can define this. This is the ***Main VT Location*** setting, which is found in the *CT AND VT RATIOS* column.

The Check Sync VT may be connected to one of the phase-to-phase voltages or phase-to-neutral voltages. This needs to be defined using the ***CS Input*** setting in the *CT AND VT RATIOS* column. Options are, A-B, B-C, C-A, A-N, B-N, or C-N.

19.9.1.2 VOLTAGE MONITORING

The settings in the *VOLTAGE MONITORS* sub-heading in the *SYSTEM CHECKS* column allow you to define the threshold at which a voltage is considered live, and a threshold at which the voltage is considered dead. These thresholds apply to both line and bus sides. If the measured voltage falls below the ***Dead Voltage*** setting, a DDB signal is generated (***Dead Bus***, or ***Dead Line***, depending on which side is being measured). If the measured voltage exceeds the ***Live Voltage*** setting, a DDB signal is generated (***Live Bus***, or ***Live Line***, depending on which side is being measured).

19.9.1.3 CHECK SYNCHRONISATION

The device provides two stages of Check Synchronisation. The first stage (CS1) is intended for use in synchronous systems. This means, where the frequencies and phase angles of both sides are compared and if the difference is within set limits, the circuit breaker is allowed to close. The second stage (CS2) is similar to stage, but has an additional adaptive setting. The second stage CS2 is intended for use in asynchronous systems, i.e. where the two sides are out of synchronism and one frequency is slipping continuously with respect to another. If the closing time of the circuit breaker is known, the CB Close command can be issued at a definite point in the cycle such that the CB closes at the point when both sides are in phase.

In situations where it is possible for the voltages on either side of a circuit breaker to be either synchronous or asynchronous, both CS1 and CS2 can be enabled to provide a CB Close signal if either set of permitted closing conditions is satisfied.

Each stage can also be set to inhibit circuit breaker closing if selected blocking conditions such as overvoltage, undervoltage or excessive voltage magnitude difference are detected. CS2 requires the phase angle difference to be decreasing in magnitude before permitting the circuit breaker to close. CS2 has an optional “Adaptive” closing feature, which issues the permissive close signal when the predicted phase angle difference immediately prior to the instant of circuit breaker main contacts closing (i.e. after CB Close time) is as close as practicable to zero.

Slip frequency is the rate of change of phase between each side of the circuit breaker, which is measured by the difference between the voltage signals on either side of the circuit breaker.

Having two system synchronism check stages available allows the circuit breaker closing to be enabled under different system conditions (for example, low slip / moderate phase angle, or moderate slip / small phase angle).

The settings specific to Check Synchronisation are found under the sub-heading *CHECK SYNC* in the *SYSTEM CHECKS* column. The only difference between the CS1 settings and the CS2 settings is that CS2 has a ***CS2 Adaptive*** setting for predictive closure of CB.

The settings specific to Check Synchronisation are found under the sub-heading *CHECK SYNC* in the *SYSTEM CHECKS* column. The only difference between the CS1 settings and the CS2 settings is that CS2 has settings for predictive closure of each CB (***CB1 CS2 Adaptive*** and ***CB2 CS2 Adaptive***).

19.9.1.4 CHECK SYNCRONISATION VECTOR DIAGRAM

The following vector diagram represents the conditions for the System Check functionality. The Dead Volts setting is represented as a circle around the origin whose radius is equal to the maximum voltage magnitude, whereby the voltage can be considered dead. The nominal line voltage magnitude is represented by a circle around the origin

whose radius is equal to the nominal line voltage magnitude. The minimum voltage magnitude at which the system can be considered as Live, is the magnitude difference between the bus and line voltages.

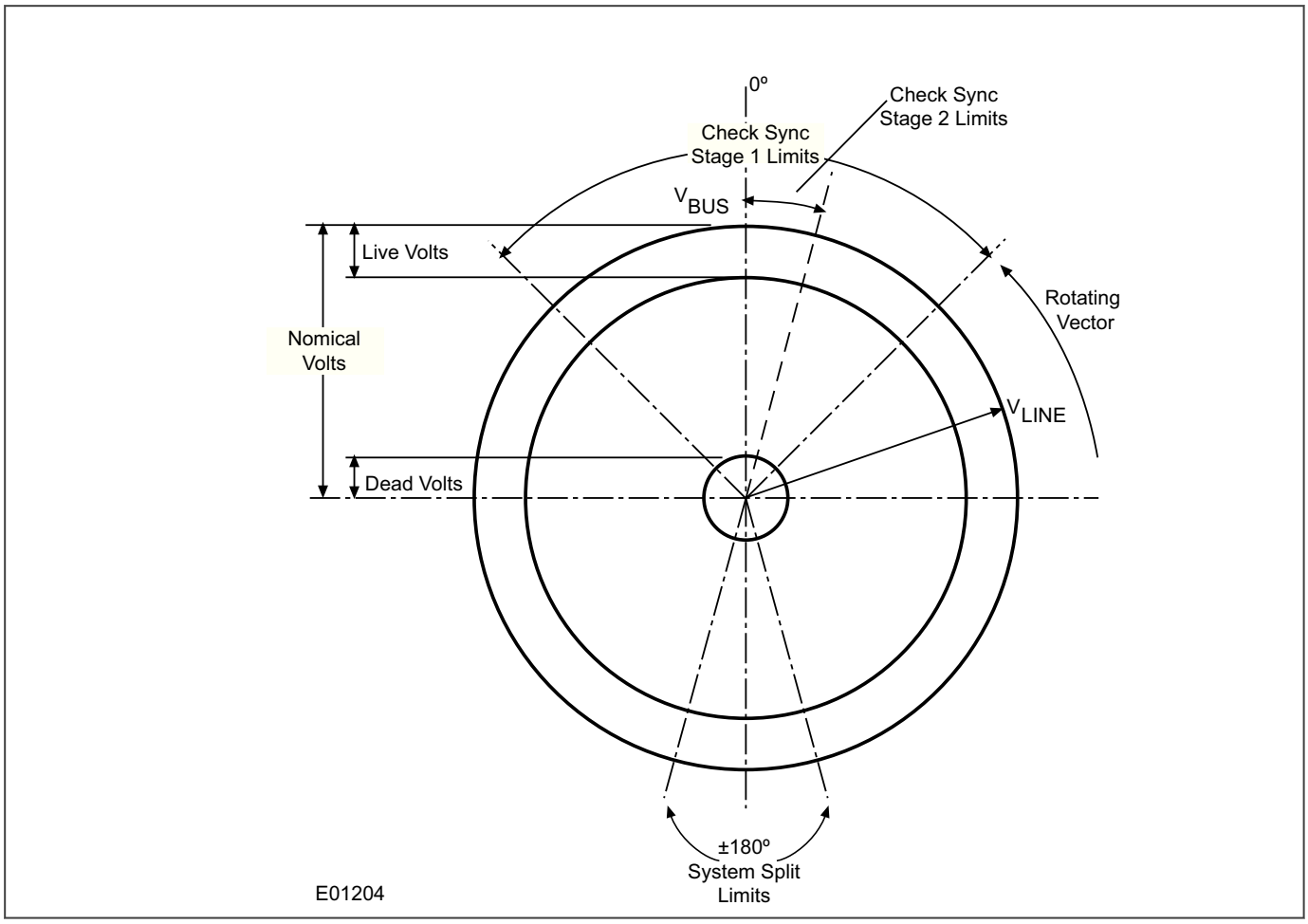


Figure 370: Check synchronisation vector

19.9.1.5 SYSTEM SPLIT

If the line side and bus side are of the same frequency (i.e. in synchronism) but have a large phase angle between them (180° +/- the set limits), the system is said to be 'Split'. If this is the case, the device will detect this and issue an alarm signal indicating this.

The settings specific to System Split functionality are found under the sub-heading *SYSTEM SPLIT* in the *SYSTEM CHECKS* column.

19.9.2 VOLTAGE MONITOR FOR CB CLOSURE

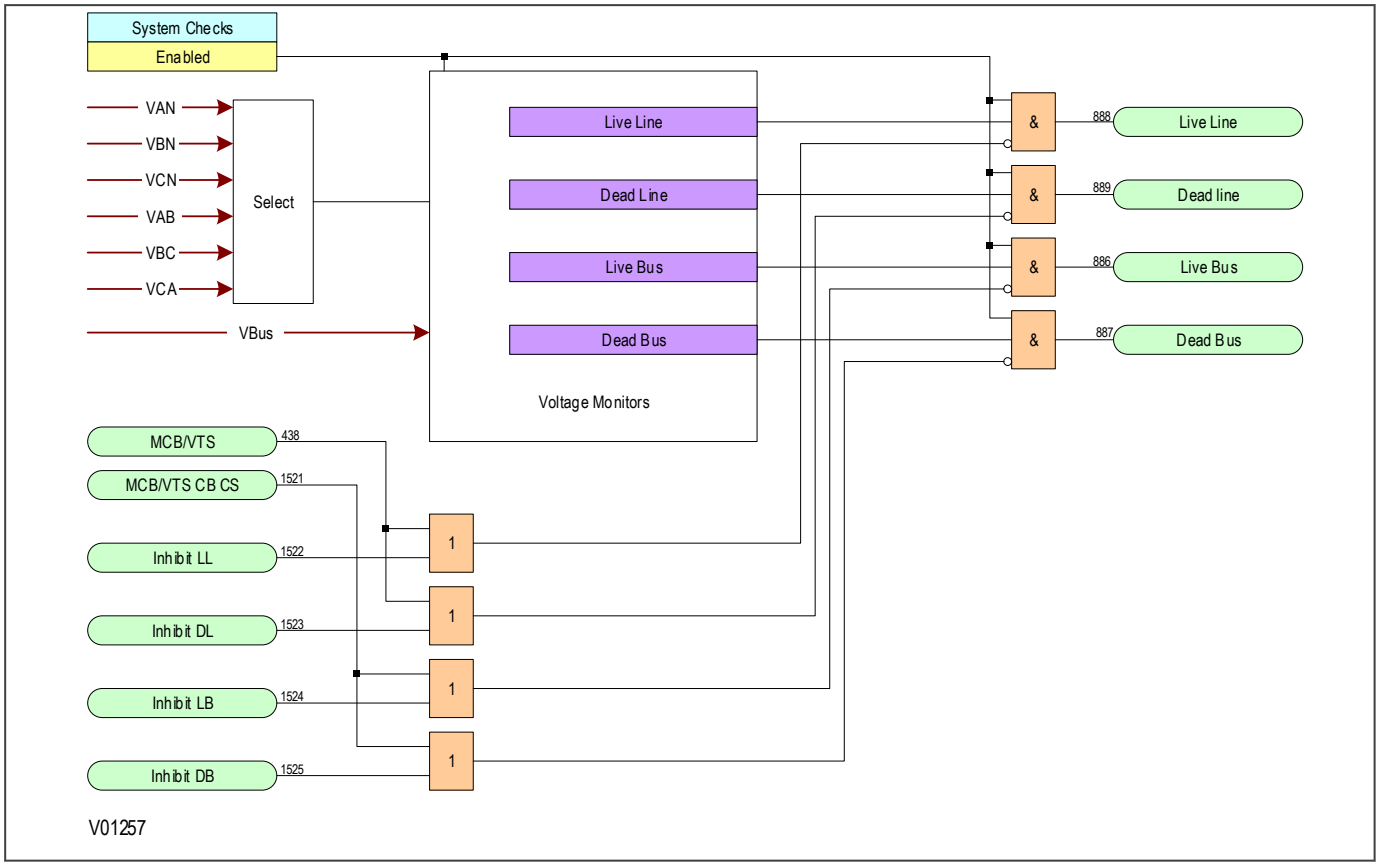


Figure 371: Voltage monitor for CB closure (module 59)

19.9.3 VOLTAGE MONITOR FOR CB CLOSURE

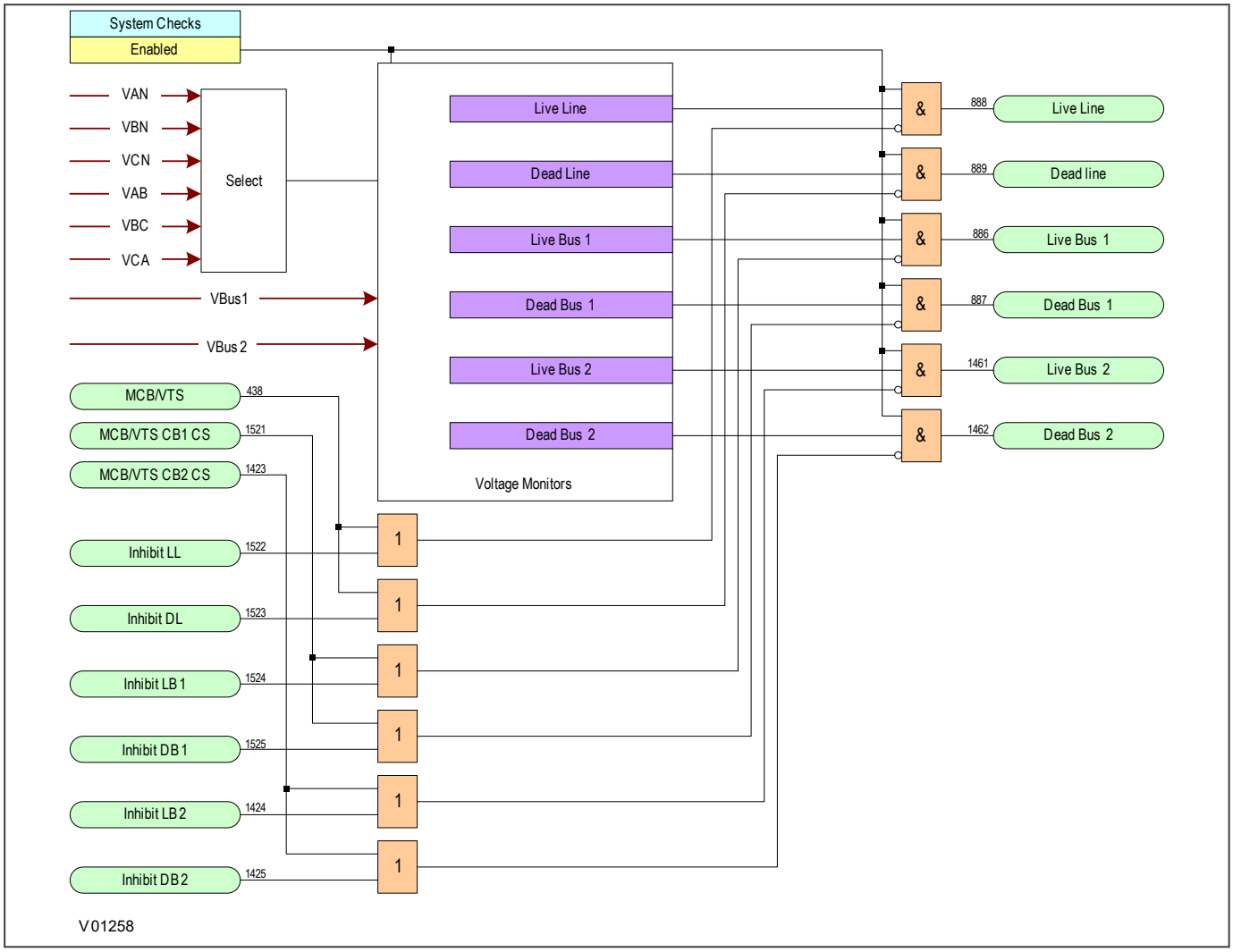


Figure 372: Voltage monitor for CB closure (module 59)

19.9.4 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

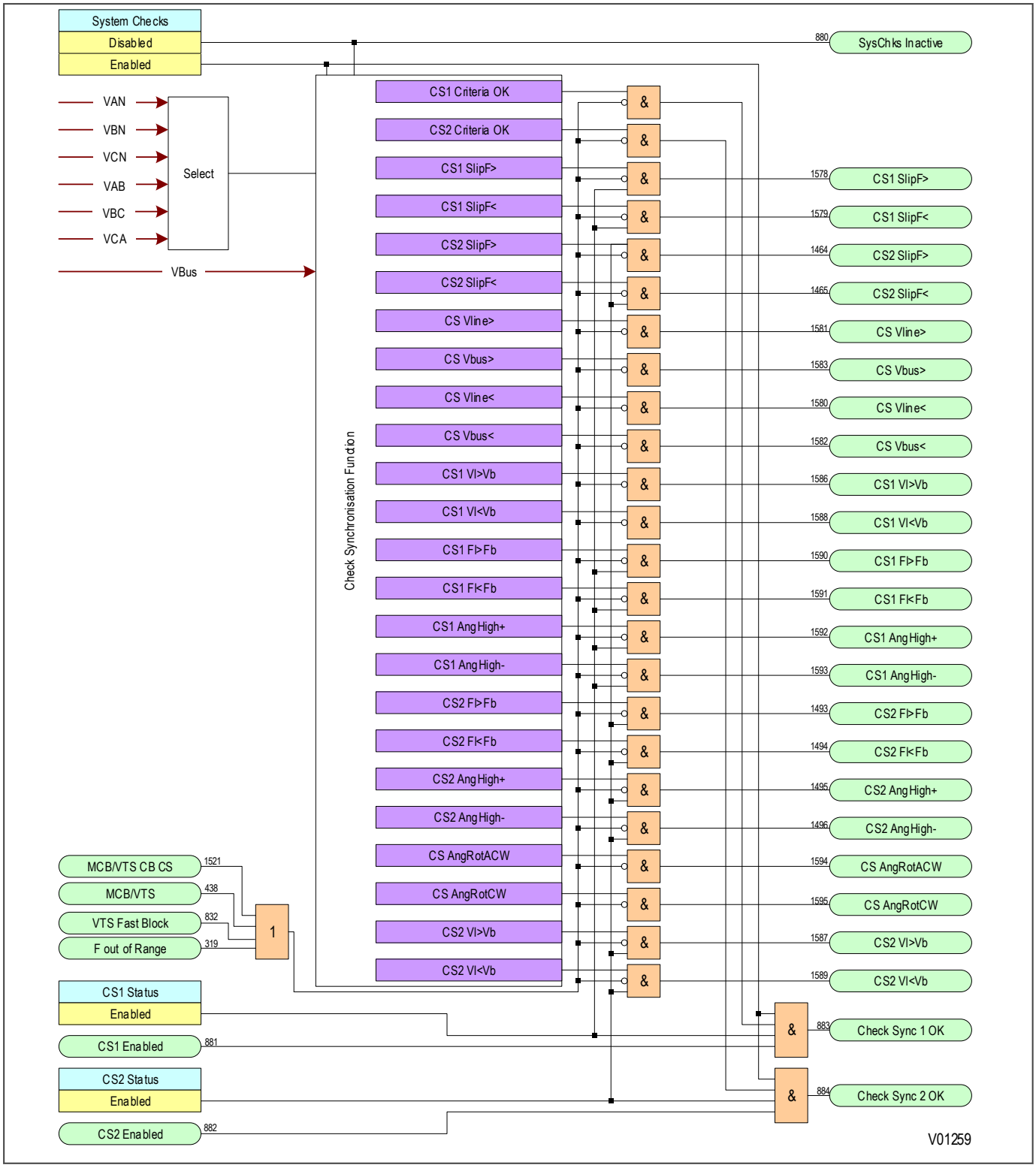


Figure 373: Check synchronisation monitor for CB closure (module 60)

19.9.5 CHECK SYNCHRONISATION MONITOR FOR CB CLOSURE

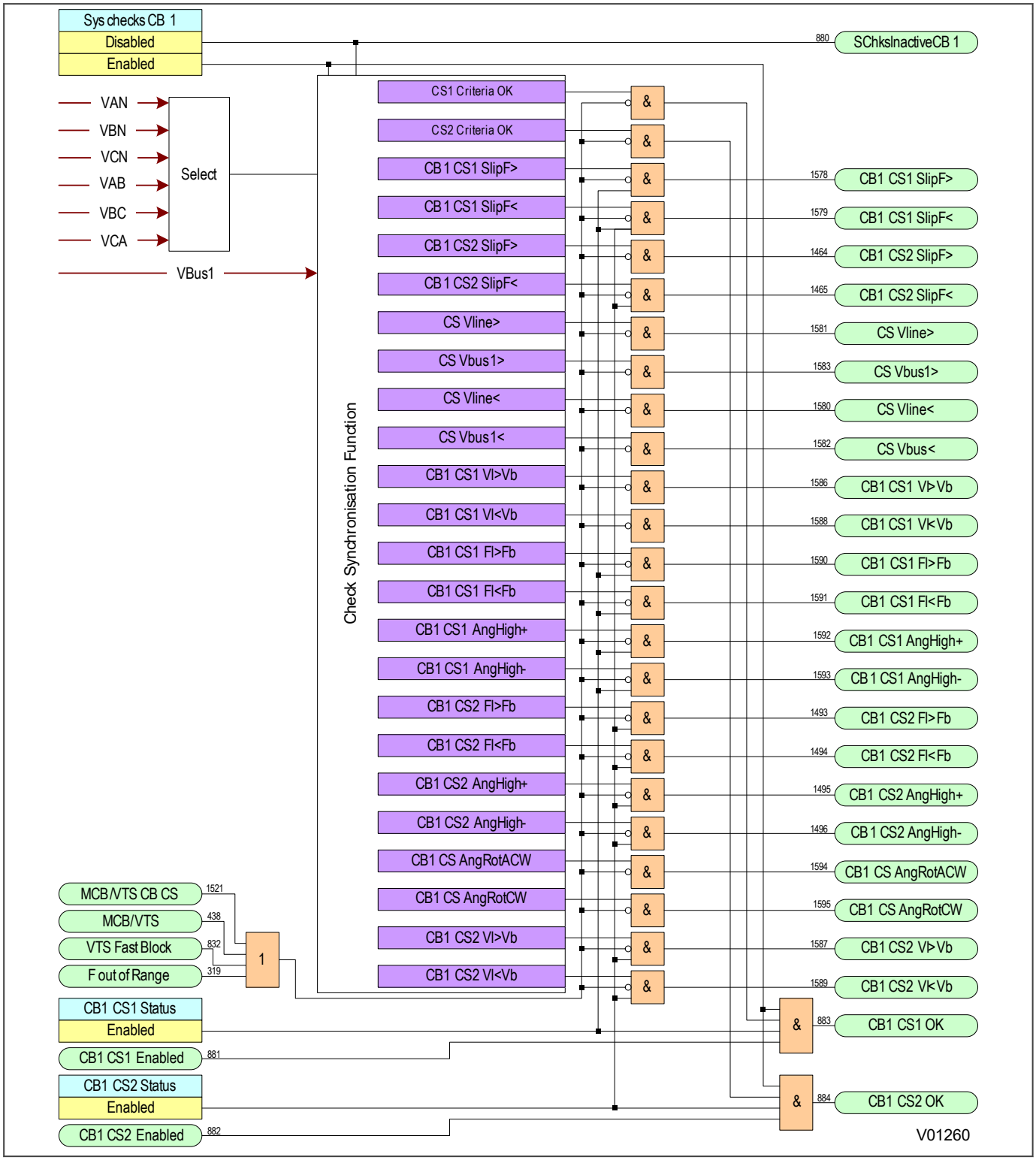


Figure 374: Check synchronisation monitor for CB1 closure (module 60)

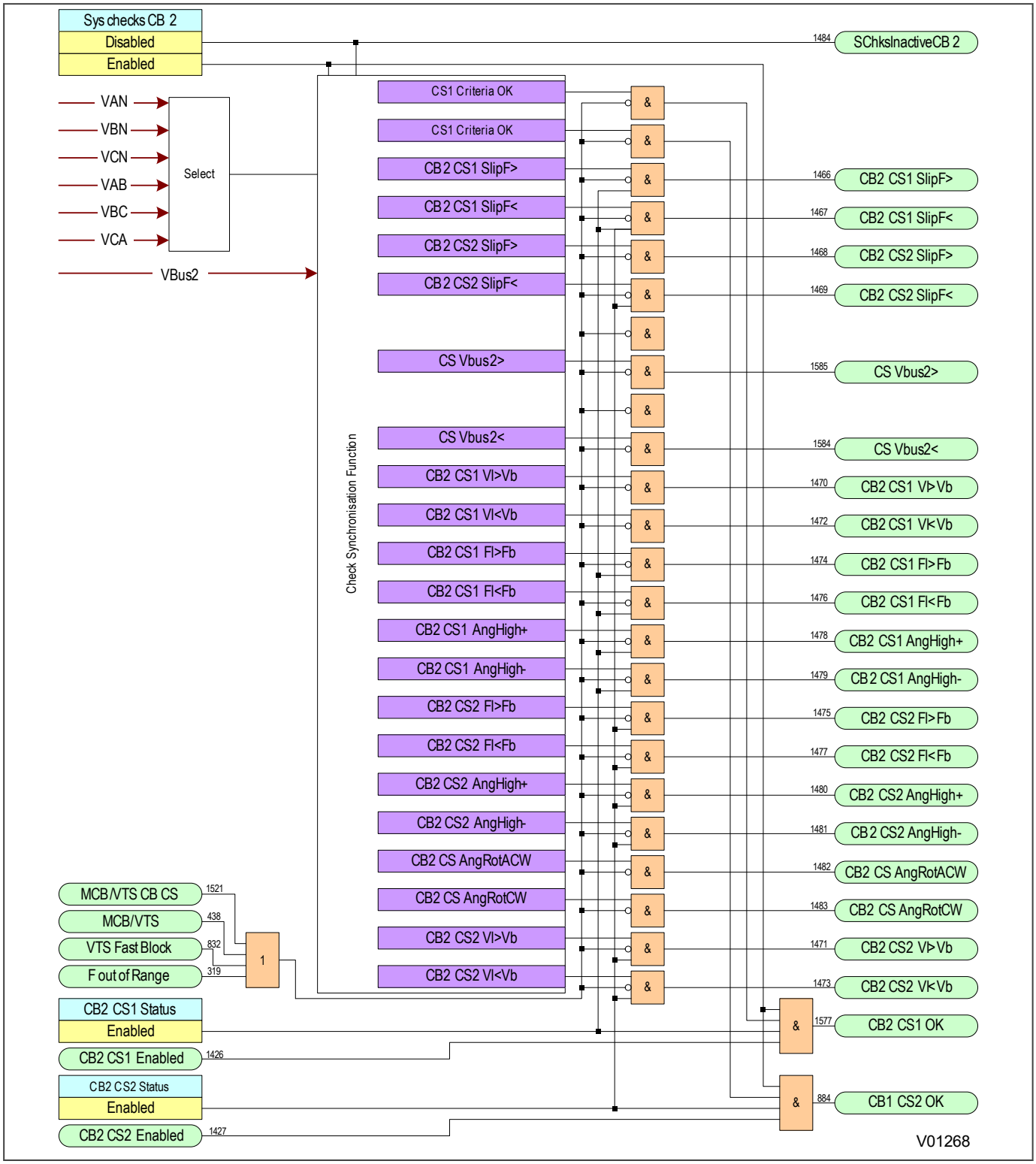


Figure 375: Check synchronisation monitor for CB2 closure (module 61)

19.9.6 SYSTEM CHECK LOGIC

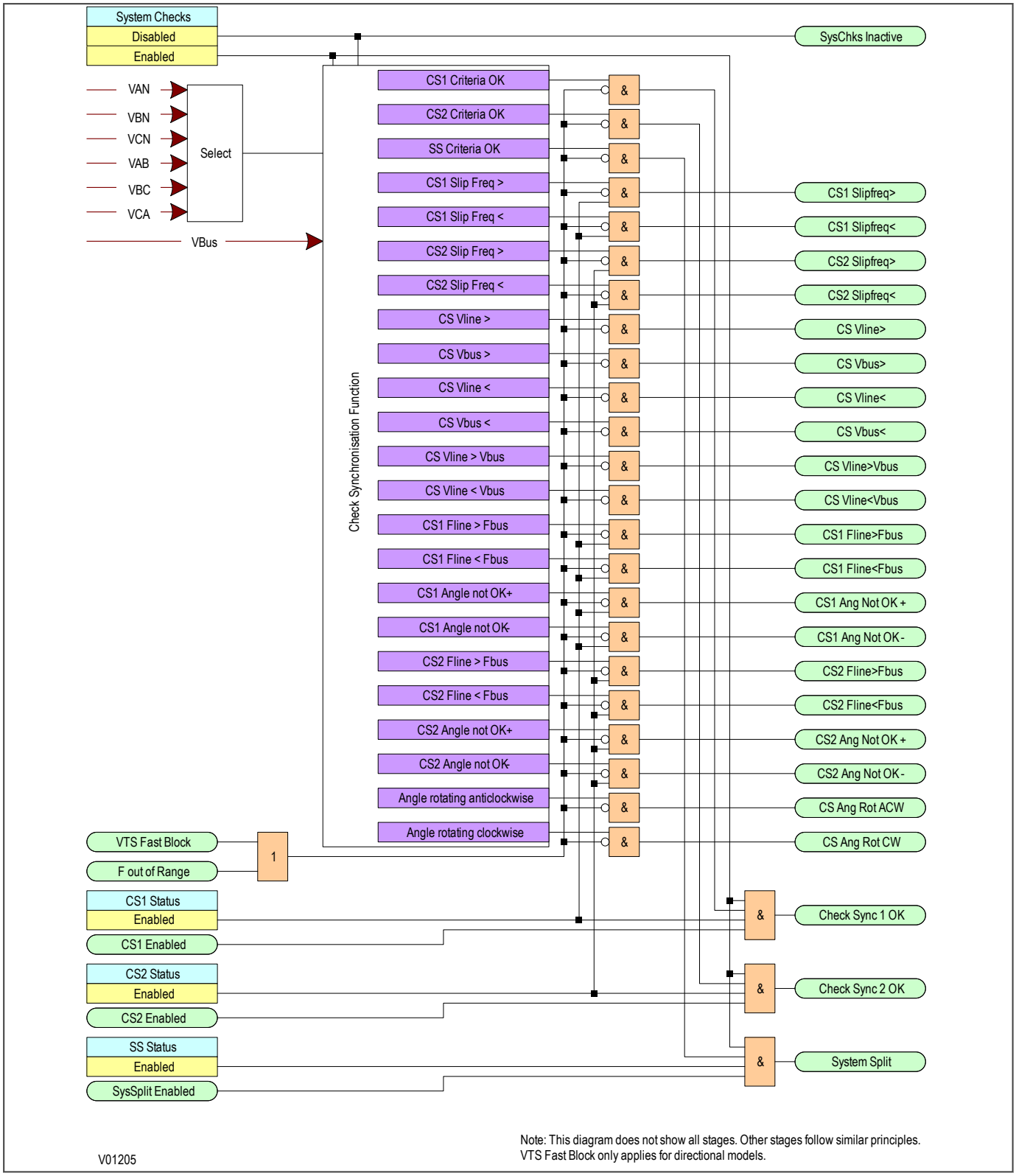


Figure 376: System check logic

19.9.7 SYSTEM CHECK PSL

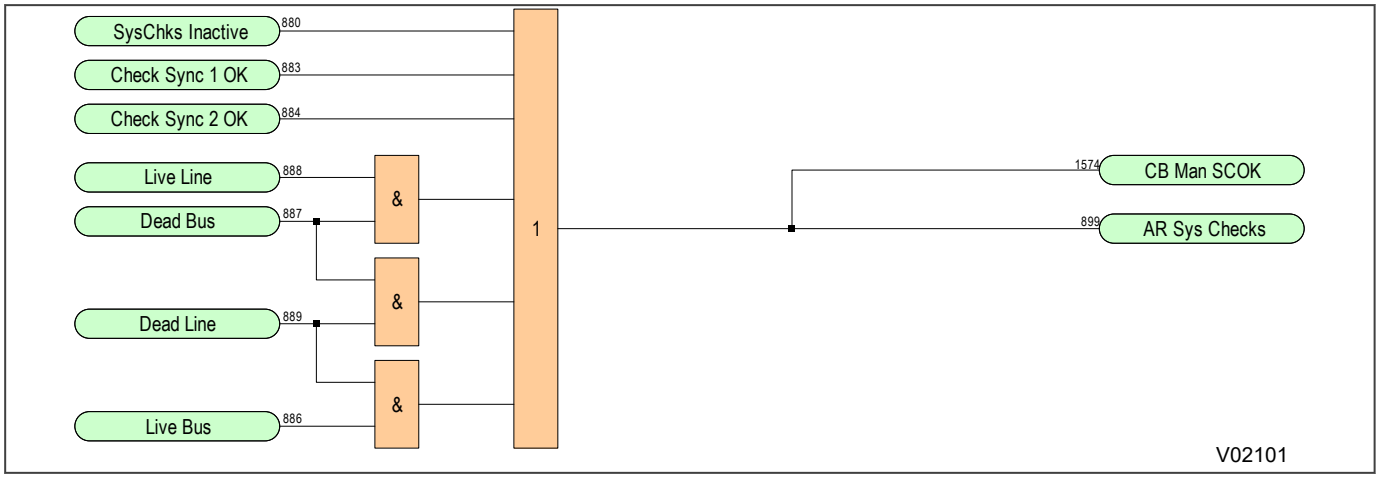


Figure 377: System check PSL

19.9.8 APPLICATION NOTES

19.9.8.1 USE OF CHECK SYNC 2 AND SYSTEM SPLIT

Check Sync 2 (CS2) and System Split functions are included for situations where the maximum permitted slip frequency and phase angle for synchronism checks can change due to adverse system conditions. A typical application is on a closely interconnected system, where synchronism is normally retained when a feeder is tripped. But under some circumstances, with parallel interconnections out of service, the feeder ends can drift out of synchronism when the feeder is tripped. Depending on the system and machine characteristics, the conditions for safe circuit breaker closing could be, for example:

Condition 1: For synchronised systems, with zero or very small slip:

- Slip <50 mHz; phase angle <30°

Condition 2: For unsynchronised systems, with significant slip:

- Slip < 250 mHz; phase angle <10° and decreasing

By enabling both CS1 and CS2, the device can be configured to allow CB closure if either of the two conditions is detected.

For manual circuit breaker closing with synchronism check, some utilities might prefer to arrange the logic to check initially for condition 1 only. However, if a System Split is detected before the condition 1 parameters are satisfied, the device will switch to checking for condition 2 parameters instead, based on the assumption that a significant degree of slip must be present when system split conditions are detected. This can be arranged by suitable PSL logic, using the System Check DDB signals.

19.9.8.2 PREDICTIVE CLOSURE OF CIRCUIT BREAKER

The ***CS2 Adaptive*** setting compensates for the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 65 Hz.

19.9.8.3 PREDICTIVE CLOSURE OF CIRCUIT BREAKERS

The ***CB1 CS2 Adaptive*** and ***CB1 CS2 Adaptive*** settings compensate for the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 65 Hz.

19.9.8.4 VOLTAGE AND PHASE ANGLE CORRECTION

For the Check Synchronisation function, the device needs to convert measured secondary voltages into primary voltages. In some applications, VTs either side of the circuit breaker may have different VT Ratios. In such cases, a magnitude correction factor is required.

There are some applications where the main VT is on the HV side of a transformer and the Check Sync VT is on the LV side, or vice-versa. If the vector group of the transformer is not "0", the voltages are not in phase, so phase correction is also necessary.

The correction factors are as follows and are located in the *CT AND VT RATIOS* column:

- C/S V kSM, where kSM is the voltage correction factor.
- C/S Phase kSA, where kSA is the angle correction factor.

Assuming C/S input setting is A-N, then:

The line and bus voltage magnitudes are matched if $V_{a\ sec} = V_{cs\ sec}$ x C/S V kSA

The line and bus voltage angles are matched if $\angle V_{a\ sec} = \angle V_{cs\ sec}$ + C/S Phase kSA

The following application scenarios show where the voltage and angular correction factors are applied to match different VT ratios:

Scenario	Physical Ratios (ph-N Values)				Setting Ratios				CS Correction Factors	
	Main VT Ratio		CS VT Ratio		Main VT Ratio (ph-ph) Always		CS VT Ratio		kSM	kSA
	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)		
1	220/√3	110/√3	132/√3	100/√3	220	110	132	100	1.1	30º
2	220/√3	110/√3	220/√3	110	220	110	127	110	0.577	0º
3	220/√3	110/√3	220/√3	110/3	220	110	381	110	1.732	0º

19.10 SWITCH STATUS AND CONTROL

All P54 products support Switch Status and Control for up to 8 switchgear elements. This is available for IEC60870-5-103 and IEC61850 protocols. The device is able to monitor the status of and control up to eight switches. The types of switch that can be controlled are:

- Load Break switch
- Disconnector
- Earthing SwitchP54
- High Speed Earthing Switch

Consider the following feeder bay:

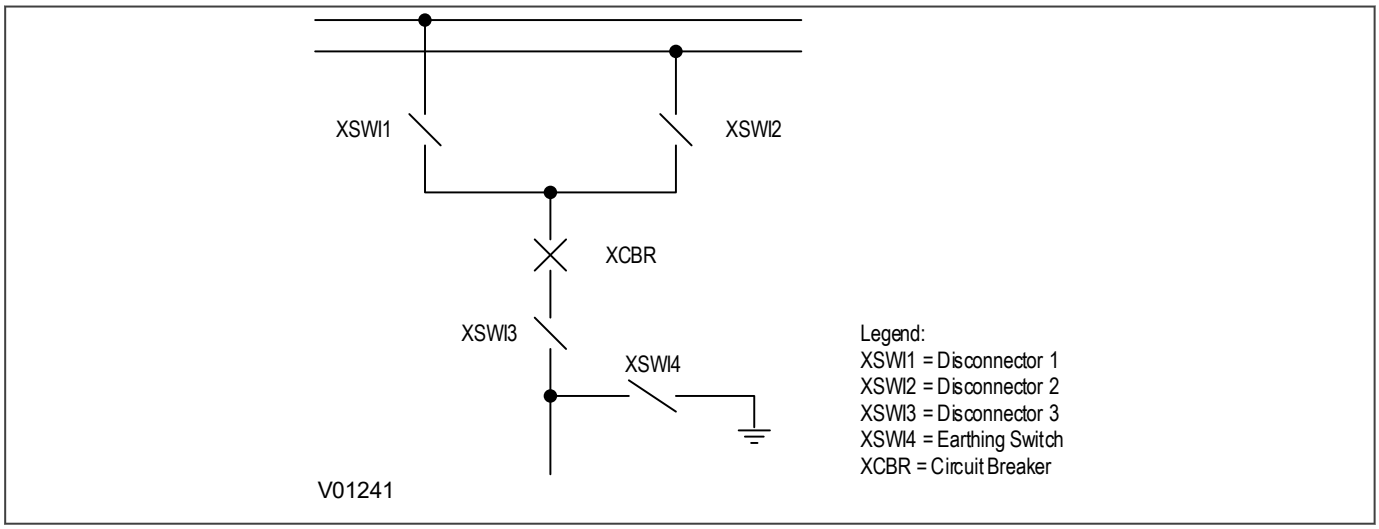


Figure 378: Representation of typical feeder bay

This bay shows four switches of the type LN XSWI and one circuit breaker of type LN XCBR. In this example, the switches XSWI1 – XSWI3 are disconnectors and XCSWI4 is an earthing switch.

For the device to be able to control the switches, the switches must provide auxiliary contacts to indicate the switch status. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers.

There are eight sets of settings in the *SWITCH CONTROL* column, which allow you to set up the Switch control, one set for each switch. These settings are as follows:

SWITCH1 Type

This setting defines the type of switch. It can be a load breaking switch, a disconnector, an earthing switch or a high speed earthing switch.

SWI1 Status Inpt

This setting defines the type of auxiliary contacts that will be used for the control logic. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers. "A" contacts match the status of the primary contacts, whilst "B" contacts are of the opposite polarity.

SWI1 Control by

This setting determines how the switch is to be controlled. This can be Local (using the device directly) remote (using a communications link), or both.

SWI1Trip/Close

This is a command t o directly trip or close the switch.

SWI1 Trp Puls T and ***SWI1 Cls Puls T***

These settings allow you to control the width of the open and close pulses.

SWI1 Sta Alrm T

This setting allows you to define the duration of wait timer before the device raises a status alarm.

SWI1 Trp Fail T and ***SWI1 Cls Fail T***

These settings allow you to control the delay of the open and close alarms when the final switch status is not in line with expected status.

SWI1 Operations

This is a data cell, which displays the number of switch operations that have taken place. It is an accumulator, which you can reset using the ***Reset SWI1 Data*** setting

Reset SWI1 Data

This setting resets the switch monitoring data.

Note:
Settings for switch 1 are shown, but settings for all other switch elements are the same.

IEC 61850 protocol: The Switch position can be controlled in the 'CSWI' Logical Node that is linked to the 'XSWI' Switch Logical Node. For Control Authority as per IEC 61850, it is necessary to select ***SWx Control by*** cell as option 4 L/R Key.

19.10.1 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

19.10.2 SWITCH CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the switches selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the Switch Control by setting is selected to option 1 *LOCAL*, option 3 `Local+Remote` or option 4 `L/R Key` in the SWITCH CONTROL column, users are allowed to use the Open and Close Key on the front panel to operate the SWITCH.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***Switch Control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is green and the REMOTE mode is selected. The **L/R Key Status** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant you want to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the OPEN or CLOSE key to operate

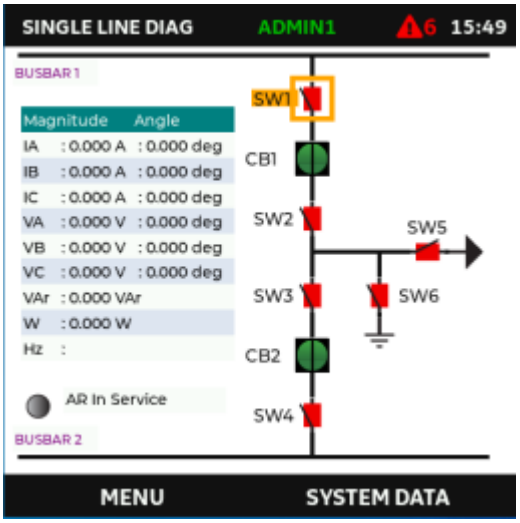


Figure 379: HMI SLD display

For the Switch Commands from HMI, these additional checks are done:

If the Switch is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "***Control by***" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - In Remote Control."

If the associated local DDB is set to local, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

19.10.3 SWITCH CONTROL LOGIC

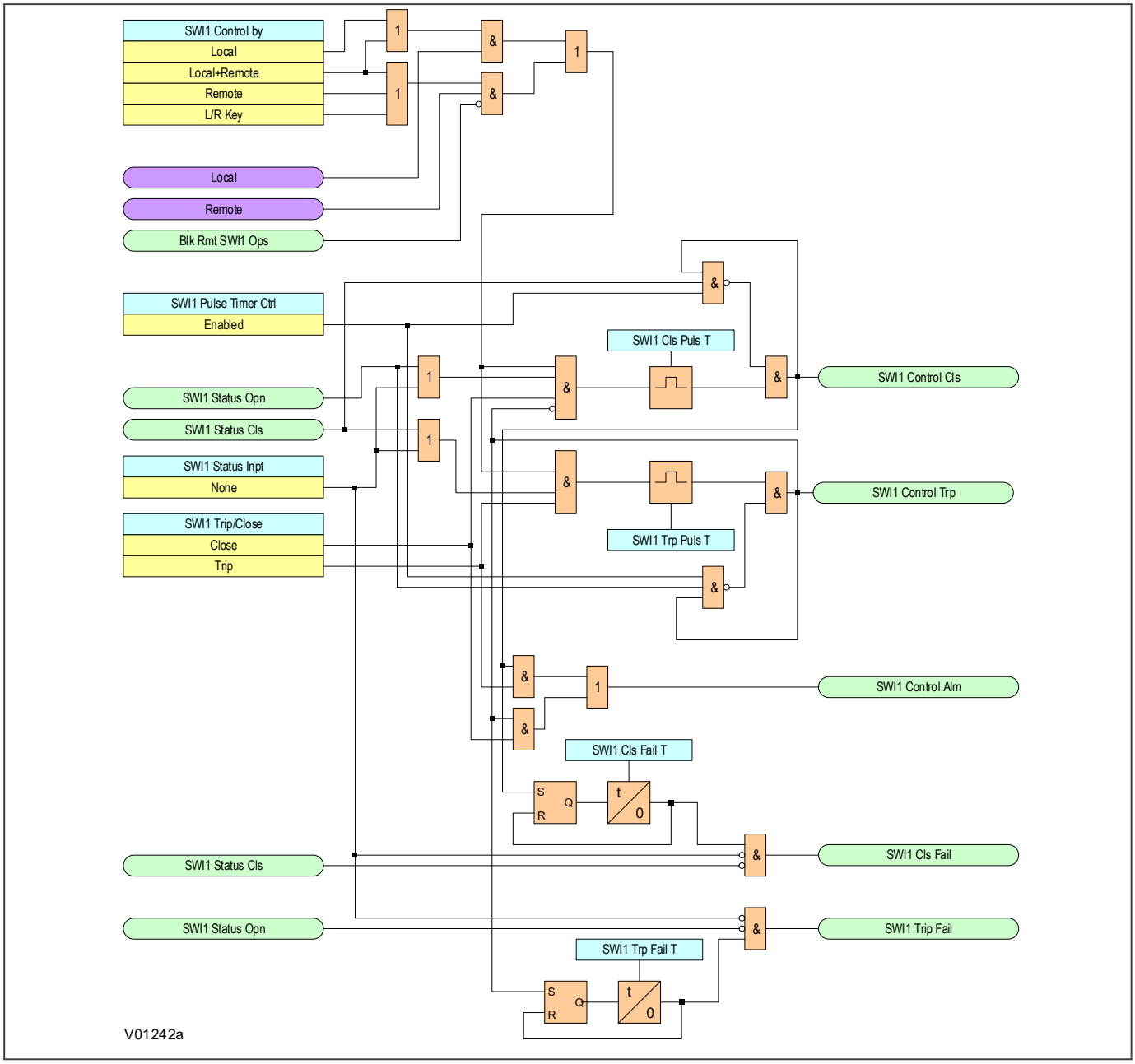


Figure 380: Switch control logic

19.10.4 SWITCH STATUS LOGIC

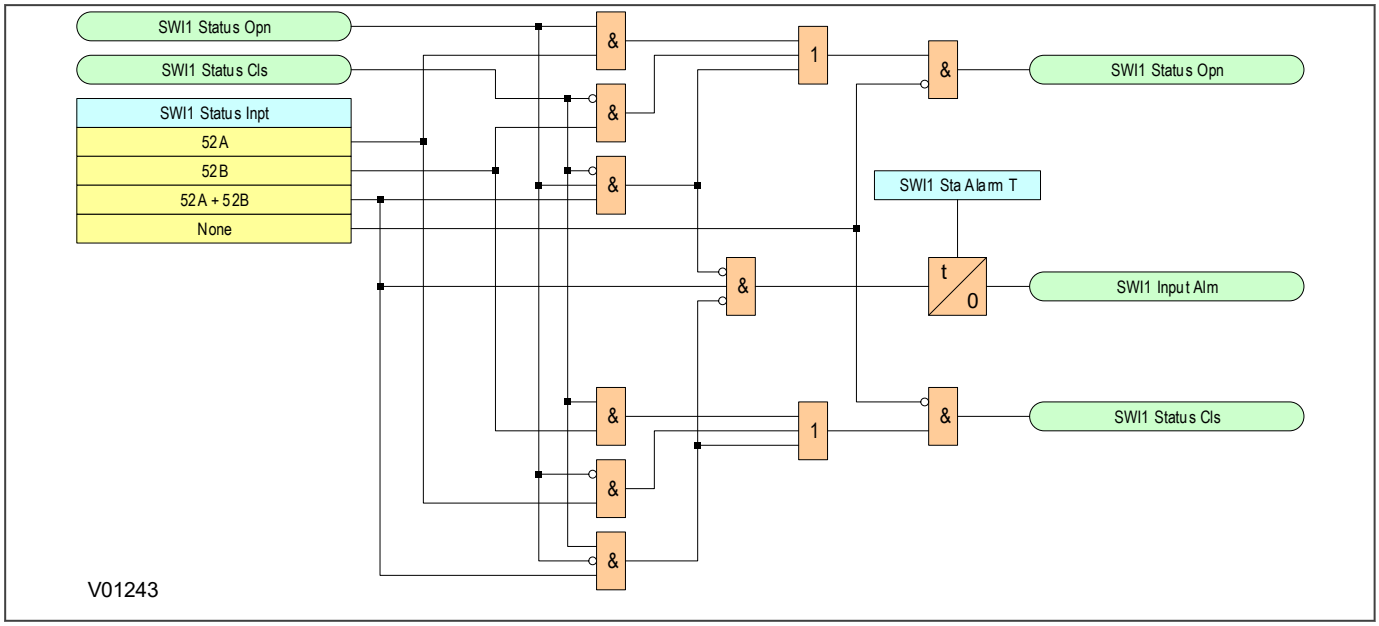


Figure 381: Switch status logic

19.11 TEST MODE

The behaviour of the IED is dependant on if it is in normal operation or in one of the Test Modes. This is reflected in some of the data that can be monitored and affects the allowed control operations, particularly using the IEC 61850 protocol.

The mode of operation is set using the ***IED Test Mode*** cell under the *COMMISSION TESTS* column. See the Commissioning Instructions chapter for more information.

When the IED is in either ***Test*** or ***Contacts Blocked*** mode, IEC 61850 status and measurement data will be transmitted with its quality parameter set to ***test***, so that the receiver understands that they have been issued by a device under test and can respond accordingly.

When the IED is in either ***Test*** or ***Contacts Blocked*** mode, the IED only responds to IEC 61850 MMS controls from the client with the 'test' flag set (with the exception of controls on System/LLN0.Mod).

You can select the mode of operation of the P40 IED by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column
- Using an IEC 61850 MMS control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the P40 IED behaviour under the different modes:

IED Test Mode Setting	IEC 61850 Mod	Result
Disabled	on	• Normal IED behaviour • IED only responds to incoming GOOSE and SV messages with quality q.test = false
Test	test	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are still active • IEC 61850 message outputs have 'quality' q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true
Contacts Blocked	test/blocked	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are disabled • IEC 61850 message outputs have quality q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

19.12 IEC 61850 CONTROL AUTHORITY

Within the substation, control commands to the primary equipment, such as the breaker or disconnect/earth switches can be originated from one of four levels: Device, Bay, Station or Remote.

Device: Controls are issued manually at the device in the yard/GIS. Any commands from remote locations are not accepted. For this to happen the XCBR/XSWI.Loc object should be True. For P40 devices, the XCBR/XSWI.Loc is mapped to these DDBs, where applicable:

DDB No.	DDB Name	Description
2186	LocKey Local	This DDB signal indicates that the IED is in local status
2187	SW1 Local	This DDB signal indicates that the switch 1 is in local status
2188	SW2 Local	This DDB signal indicates that the switch 2 is in local status
2189	SW3 Local	This DDB signal indicates that the switch 3 is in local status
2190	SW4 Local	This DDB signal indicates that the switch 4 is in local status
2191	SW5 Local	This DDB signal indicates that the switch 5 is in local status
2192	SW6 Local	This DDB signal indicates that the switch 6 is in local status
2193	SW7 Local	This DDB signal indicates that the switch 7 is in local status
2194	SW8 Local	This DDB signal indicates that the switch 8 is in local status
2195	CB1 Local	This DDB signal indicates that the CB1 is in local status
2196	CB2 Local	This DDB signal indicates that the CB2 is in local status
2197	CB3 Local	This DDB signal indicates that the CB3 is in local status
2198	CB4 Local	This DDB signal indicates that the CB4 is in local status
2199	CB5 Local	This DDB signal indicates that the CB4 is in local status

If the DDBs associated are not connected, the default is False which facilitates remote operations.

Bay: The commands are issued from the HMI of the P40. The P40 has a dedicated L/R Button for selection in the front face.

Key	Description	Function
	Local/Remote key	To select between local and remote operating modes.

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is Red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is Green and the REMOTE mode is selected. The ***L/R Key Status*** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

Bay Level controls are possible from the HMI if the ***L/R Key Status*** is in Local. When L/R Key is in Local the IEC 61850 Signal, System\LLN0.Loc is set as True. When L/R Key is in Remote, and a control action is attempted, the User will be advised with a pop-up message of "Command Unavailable - in remote".

To facilitate integration of the IED into a wired Local/Remote control switch in a panel, an additional DDB L/R Key has been provided.

This is modelled into IEC 61850 System\LLN0.LocKey. The data object LocKey represents the status of a physical key switch and allows taking over the control authority, if the DDB is wired. If the DDB is used, and is set to 1, the IED Local/Remote (System\LLN0.Loc) automatically changes to Local. At this stage, it is not possible to change the

IED L/R Key to remote. If the DDB is set to 0, the IED L/R does not automatically change to Remote. If necessary, a user action is required to change the control authority to Remote.

Station/Remote: Station level commands are those originating from either the substation gateway or from the station HMI. Remote commands are from the remote Network Control Center (NCC).

The data object LocSta modelled in System\LLN0 shows the control authority at station level. If LocSta=True, control authority is at station level and control from remote is disabled. If LocSta=False, control commands are allowed from remote, e.g. network control center (NCC).

P40 devices also support the concept of Multiple Level Control authority. This is done via a dedicated datapoint in System\LLN0 known as MltLev. If true, authority control from multiple levels is allowed, otherwise no other control level is allowed.

Under certain operational conditions, such as during maintenance, it is necessary to block commands from one or more of these levels. The local/remote control feature (described in IEC 61850 7-4: Annex B) allows users to enable or disable control authority from one or more of the three levels, as illustrated in the tables below:

IEC 61850 commands originating from the various levels are differentiated using the Origin.OrCat attribute value in the IEC 61850 command.

If the control command is rejected by the P40 IED due to control authority check, the AddCause - Blocked-by-switching-hierarchy will be shown in the IEC 61850 Client.

Control Authority for Other Controllable Objects								
Device	Switch	Bay Control			Manual Control at Front Panel	Command From		
		Mode of Switching Authority for Local Control	Local Control Behaviour	Control Authority at Station Level		OrCat		
LLN0.Loc Key	XCBR.Loc XWI.Loc	LLN0.Mlt Lev	CSWI.Loc	CSWI.Loc Sta		Bay	Station	Remote
T	n.a.	F	n.a.	n.a.	AA	NA	NA	NA
F	T	F	T	n.a.	AA	NA	NA	NA
F	T	F	F	n.a.	NA	NA	NA	NA
F	F	F	T	n.a.	AA	NA	NA	NA
F	F	F	F	T	NA	NA	AA	NA
F	F	F	F	F	NA	NA	NA	AA
T	n.a.	T	n.a.	n.a.	AA	NA	NA	NA
F	T	T	T	n.a.	AA	NA	NA	NA
F	T	T	F	n.a.	NA	NA	NA	NA
F	F	T	T	n.a.	AA	NA	NA	NA
F	F	T	F	T	NA	AA	AA	NA
F	F	T	F	F	NA	AA	AA	AA

n.a. - Not Applicable
AA - Always Allowed
NA - Not Allowed

In addition to the CB/Switches, P40 devices follow the concept of Control Authority for other commands executed via IEC 61850. These include:

- Control Inputs
- Reset of Trip LED
- Enable/Disable of Protection, Check Sync and Auto Recloser
- Reset of demands and thermal measurements

Control Authority for Other Controllable Objects							
Device	Bay Control			Manual Control at Front Panel	Command From		
	Mode of Switching Authority for Local Control	Local Control Behaviour	Control Authority at Station Level		OrCat		
LLN0.Loc Key	LLN0.Mlt Lev	LLN0.Loc	LLN0.Loc Sta		Bay	Station	Remote
T	F	n.a.	n.a.	AA	NA	NA	NA
F	F	T	n.a.	AA	NA	NA	NA
F	F	F	T	AA	NA	AA	NA
F	F	F	F	AA	NA	NA	AA
T	T	n.a.	n.a.	AA	NA	NA	NA
F	T	T	n.a.	AA	NA	NA	NA
F	T	F	T	AA	AA	AA	NA
F	T	F	F	AA	AA	AA	AA
n.a. - Not Applicable AA - Always Allowed NA - Not Allowed							

IEC 61850 based control authority can be visualised from the P40 HMI.

This is under the COMMISSION TESTS Menu, under IEC 61850 Control Sub Menu:

Menu Text	Description	Min	Max	Default	Controllable
Multiple Level	Used to enable/disable the 'multi level control authority' feature for breaker/switch and other controls	Disabled	Enabled	Disabled	Yes
Station Level	Used to get control command of station authority from IEC 61850 Client	Disabled	Enabled	Disabled	No
Device Level	Used to show the IED local/remote status	Local	Remote	Local	No

Multiple Level Control Authority can be selected either via an IEC 61850 MMS Command or via selection from the menu item shown above.

Note:
The Control Authority only works if the Protocol is IEC 61850. For Legacy Protocols, the existing control mechanism remains.

Note:
For Control Authority for CB/Switches, it is mandatory to select the option of L/R for CB/Switches if IEC 61850 is used.

CHAPTER 20

SUPERVISION

20.1 CHAPTER OVERVIEW

This chapter describes the supervison functions.

This chapter contains the following sections:

Chapter Overview 595
Current Differential Supervision 596
Voltage Transformer Supervision 606
Current Transformer Supervision 610
Trip Circuit Supervision 616

20.2 CURRENT DIFFERENTIAL SUPERVISION

Current Differential protection of transmission lines or distribution feeders requires communication of measured values of currents between terminals so that a comparison of current entering and leaving the protected zone can be made. To determine the health of the protected zone, the current values received from a remote terminal must be synchronised to locally acquired values. One method of achieving this is the so called 'Ping-Pong' method. For this method to work, there is a requirement that the time taken for signals communicated from one terminal to another (the propagation delay time) is equal to the time taken for signals to be communicated between the same devices in the opposite direction. This is an assumption that is valid for many applications and which has been widely applied. In some applications however, the communications symmetry may be violated either temporarily or permanently. If the requirement is violated, the Ping-Pong method cannot work correctly and maloperation may occur. Some products in this range can use a Global Positioning Satellite (GPS) input signal to provide a precise timing signal that can be used to synchronise the alignment of the current values. This allows the protection to work in applications where the communications paths may not be symmetrical. If there is no GPS synchronisation signal available or its performance becomes severely degraded, a technique based on the Ping-Pong method is employed to maintain the Current Differential protection. Unfortunately, with this compromised GPS synchronisation technique, as well as with the standard Ping-Pong technique, switching of communications paths can lead to miscalculation of bias and differential currents which could lead to maloperation. To help prevent this a number of supervision checks can be applied to Current Differential protection that is not GPS synchronised. These are:

- Current Differential Starter Supervision (Permit Current Differential)
- Switched Communications Paths Supervision
- Communications Asymmetry Supervision.

20.2.1 CURRENT DIFFERENTIAL STARTER SUPERVISION

An unexpected communications asymmetry condition can cause an apparent rise in the differential current. This causes a condition that could be interpreted as a three-phase (balanced) fault condition. Positive sequence current components are apparent in normally operating systems. A balanced fault will increase the magnitude of these positive sequence components. Any increase resulting from a communications asymmetry will be modest. However, a real three-phase fault will generally cause the magnitude of the positive sequence components to increase far more than an asymmetric communication condition would. The measurement of positive sequence current components can therefore be used to supervise Current Differential protection for balanced fault conditions.

Unbalanced faults always produce negative sequence current components. Negative sequence current components can therefore be used to supervise Current Differential protection for unbalanced fault conditions.

The components that implement this supervision are called Starter Elements. Both positive-sequence current (I1) and negative-sequence current (I2) are derived. For both I1 and I2, there are two types of starter element for each sequence component; fixed threshold and rate-of-change threshold (delta). There are four Starter Elements in all:

- ***Start I1 low***
- ***Delta I1 low***
- ***Start I2 low***
- ***Delta I2 low***

Which starter elements are used and in which combination depend on the specific application and customer requirements. The device provides complete flexibility, allowing you to use each of them individually or in combination with one another using PSL.

The starter element settings are located in the *CURRENT DIFF* column. You can choose to enable, or disable them, or select ***Idiff Permit*** (discussed later). They are disabled by default.

If a starter element picks up, the associated DDB signal is asserted. These can be used to block the current differential protection. These DDB signals are:

- ***I1 Lo Start*** (Positive phase-sequence fixed threshold start)
- ***Del I1 Lo Start*** (Rate-of-change of positive phase-sequence current)
- ***I2 Lo Start*** (Negative phase-sequence fixed threshold start)
- ***Del I2 Lo Start*** (Rate-of-change of negative phase-sequence current)

If elements are set to *Disabled*, then the DDB signals cannot be asserted.

If elements are set to *Enabled*, then the DDB signals will be asserted if appropriate conditions are met. This will allow you to use PSL to customize supervision of Current Differential protection operation. These signals do not directly affect the operation of the Current Differential function. In order to directly influence the operation of the current differential function you need to set one or more of the starter elements to *Idiff Permit*.

If elements are set to *Idiff Permit*, then the DDB Start signals will also be asserted if the appropriate conditions are met, so you can use the PSL to customise supervision of Current Differential protection operation. In addition however, if any one or more elements are set to *IDiff Permit*, then fixed internal logic is employed to produce an internal signal (Permit CDiff) that supervises the Current Differential protection by either inhibiting it or permitting it.

20.2.1.1 CURRENT DIFFERENTIAL STARTER SUPERVISION LOGIC

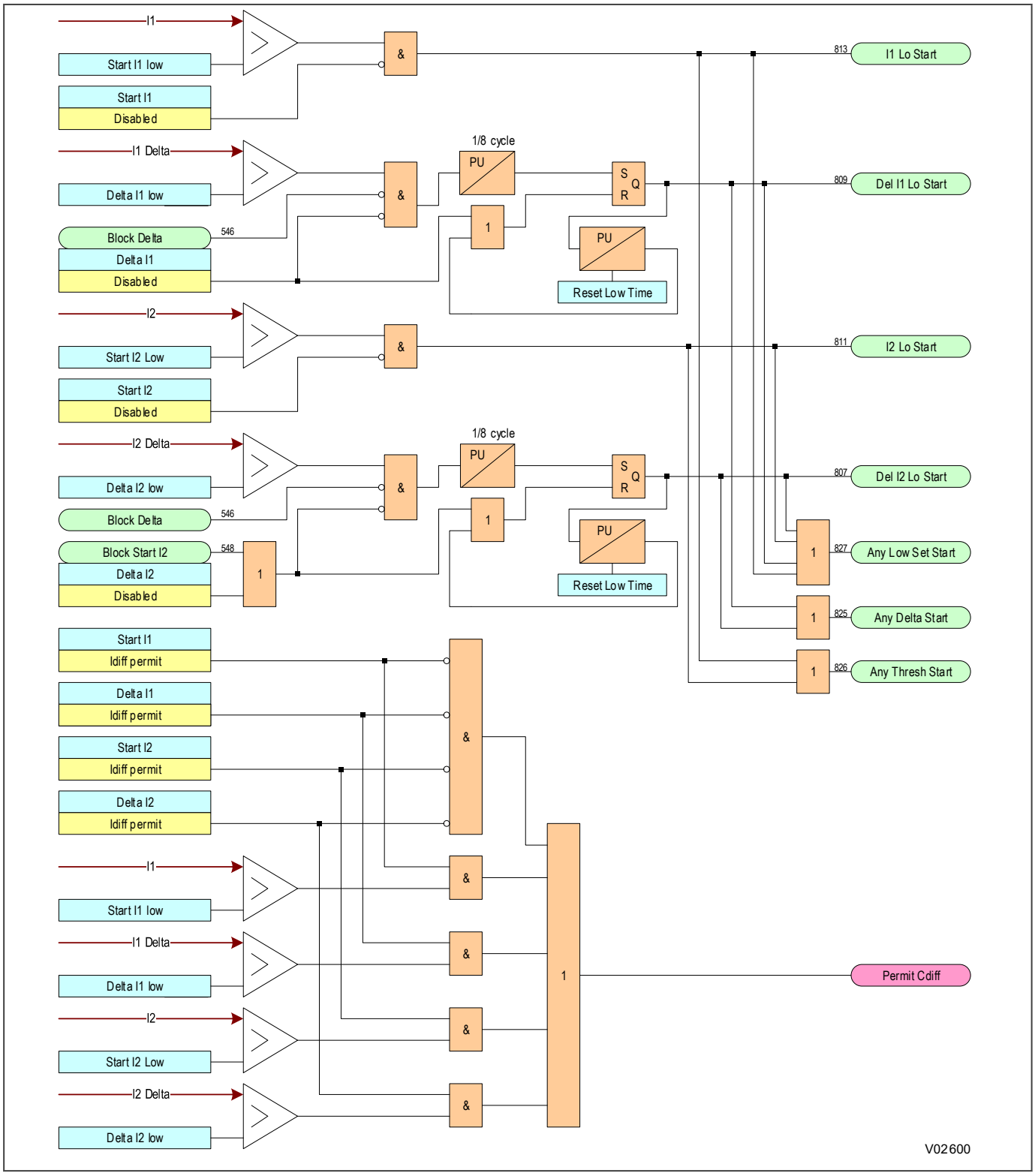


Figure 382: Current differential starter supervision logic

20.2.1.2 START AND DELTA ISEF

There is also an extra supervision available only in case of single phase to ground faults. It is located under the *STARTERS* within the *CURRENT DIFF* column. This function works using measured earth current fed into the ***IN SENSITIVE*** current transformer of the relay CT (SEF CT).

There are two elements associated to this function:

- ***Start Isef***
- ***Delta Isef***

This function is completely different to the I1 and I2 starters. It is necessary to enable at all relay ends of the line protected for this function to work correctly.

Start Isef and ***Delta Isef*** elements can be set to `Enabled` or `Disabled`. If both elements are set to `Disabled`, The line differential protection completely ignores this check and DDB signals ***Start Isef Low*** and ***Delta Isef Low*** cannot be asserted.

If one or both elements are set to `Enabled`, all multiphase faults ignore this check, and single phase to ground faults are only allowed to issue a differential trip if the threshold of the differential element has been exceeded or a differential intertrip has been received and the threshold of ***Start Isef*** or ***Delta Isef*** has been exceeded. DDB signals, ***Start Isef Low*** and ***Delta Isef Low*** will be asserted if appropriate conditions are met.

Start Isef supervision should be set above the maximum unbalanced current expected in the protected circuit. This could happen during maximum load condition. A margin of 20% above that value is recommended to take account of the accuracy of the element and the measurement.

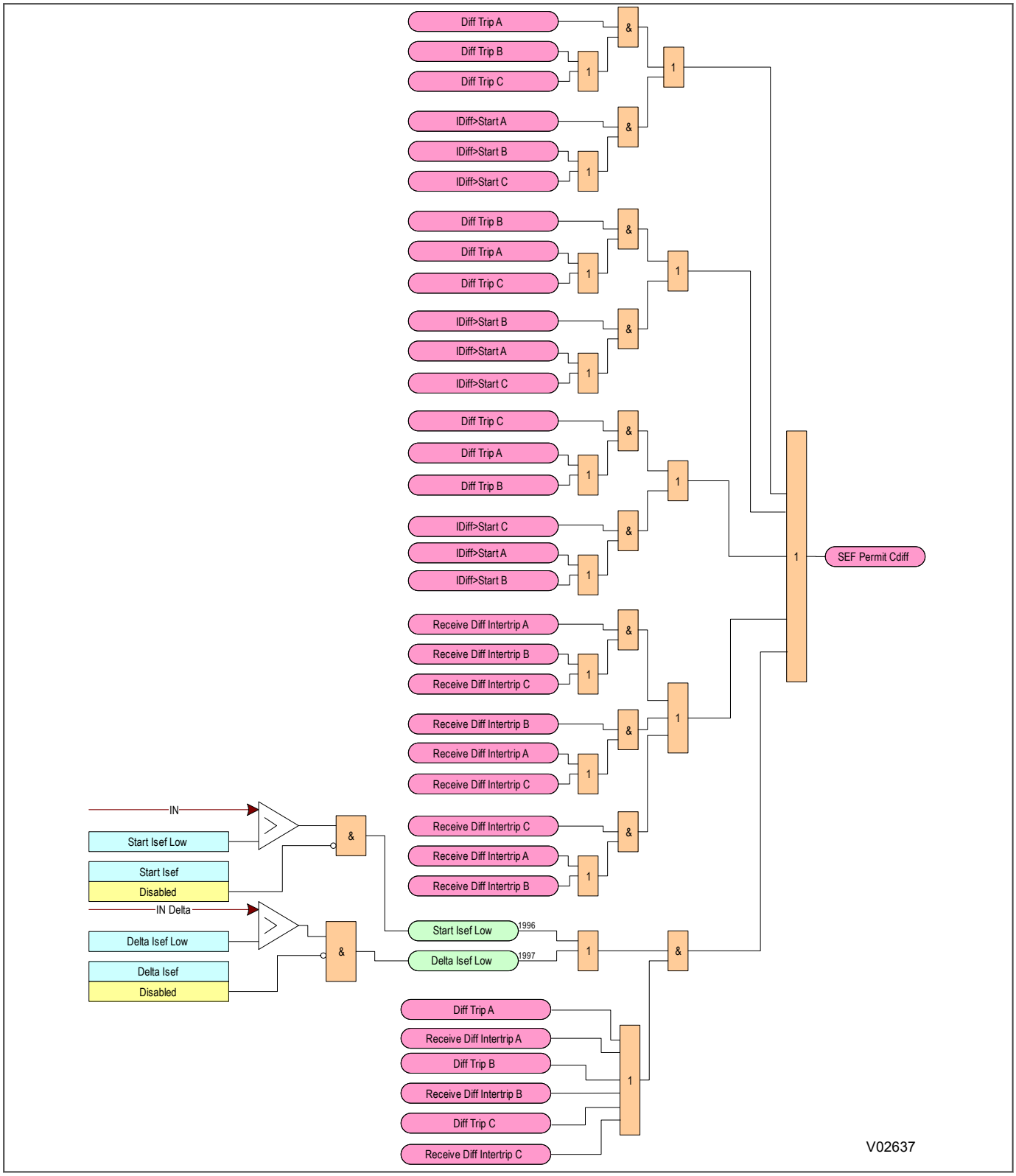


Figure 383: SEF allow logic

20.2.1.3 CURRENT DIFFERENTIAL START LOGIC

The Permit Cdiff internal signal interacts with the Current Differential function to control the Current Differential start signals. The following figure shows how this is achieved for the line differential currents. The same principle applies to neutral differential current.

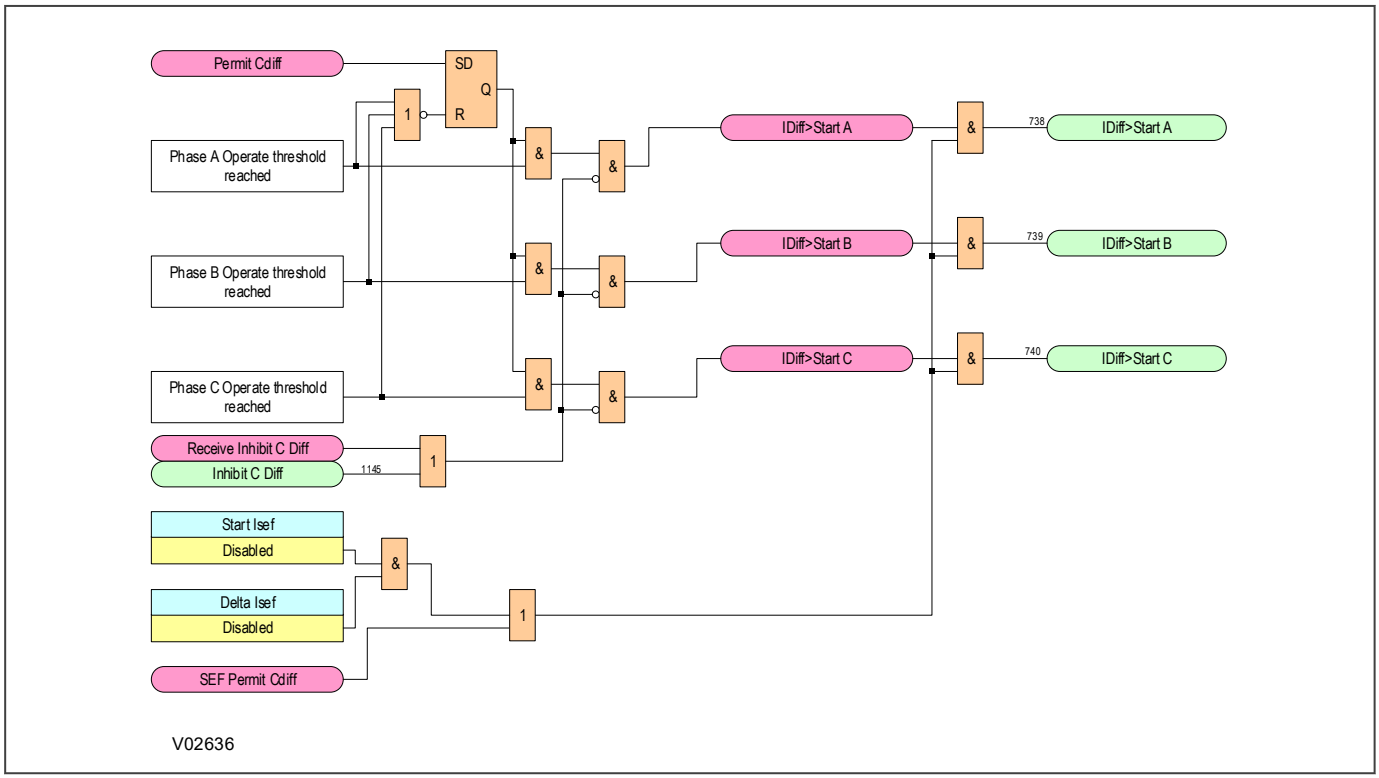


Figure 384: Current differential function start logic

20.2.2 SWITCHED COMMUNICATION PATH SUPERVISION

A feature is included in this product to supervise the operation of the Current Differential protection in the event of communications paths being switched. The Ping-Pong method of time alignment requires symmetry of communications paths. The absolute value of propagation delay is not important, but the symmetry is. Many telecommunication systems feature self-healing mechanisms so that if a particular link fails, the integrity of the system can be maintained by re-routing of traffic via unaffected links. Careful system management can ensure that the reconfiguration of the system to bypass the failed link can respect the communications symmetry requirements. Whilst the reconfiguration is in progress, however, there may be a temporary violation of the symmetry requirements. The Switched Communications Paths Supervision function protects against incorrect tripping during the period of transient symmetry violation.

The settings for the Switched Communications Paths Supervision reside in the *PROT COMMS/IM64* column.

The Current Differential protection continually monitors the communications propagation delay time. With reference to the following figure, if the differences between 2 successive calculated propagation times exceed the ***Comm Delay Tol*** setting in the *PROT COMMS/ IM64* column, then the operating characteristic is modified from the blue line to the red line.

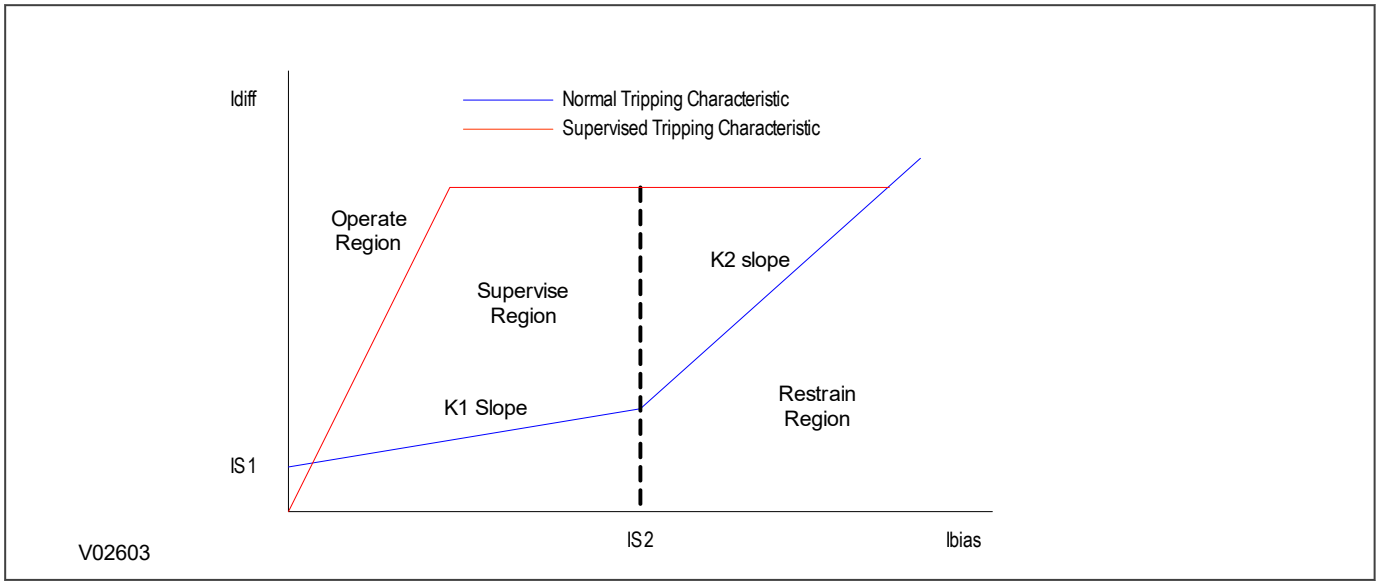


Figure 385: Switched communication path supervision

The change to the characteristic is determined by two timers (***Char Mod Time***, and ***Char Mod RstTime***) found in the *PROT COMMS/IM64* column. These timers start when the switched communication path condition is recognised. These timers define how long the modification to the tripping characteristics is applied for. A communications delay alarm (***Comm Delay Alarm***) is also raised at the same time.

When the ***Comm Delay Tol*** setting has been exceeded for two consecutive calculations, the K1 slope is increased to 200%. When the 200% slope reaches the IS2 setting, the characteristic tracks a horizontal line until it meets with the K2 slope which the characteristic then follows.

The characteristic normally returns to normal when the ***Char Mod Time*** expires, but a mechanism is provided to accelerate the reset if system conditions permit by using an additional timer ***Char Mod RstTime*** which is set to a value less than the ***Char Mod Time***.

The ***Char Mod RstTime*** can be enabled or disabled. If it is enabled, then it starts when the ***Char Mod Time*** starts. If the ***Char Mod RstTime*** has expired, but the ***Char Mod Time*** is still running, AND IF the bias current is above 5% In, AND IF the differential current is below 10% of bias current on all phases, then the ***Char Mod Time*** is reset and the characteristic returns to normal. If these conditions are not met, then the characteristic remains increased for the duration of the ***Char Mod Time***. The ***Char Mod RstTime*** should be set greater than the minimum switching delay expected, and less than the ***Char Mod Time***.

We don't recommend it, but If you don't want the tripping characteristic to be changed during communications switching operations, you should set ***Char Mod Time*** to 0.

20.2.3 COMMUNICATIONS ASYMMETRY SUPERVISION

The settings for this function reside under the *DIFF SUPERVISON* sub-heading of the *SUPERVISION* column.

The Communications Asymmetry Supervision function is included to supervise the Current Differential protection on applications where communications path switching is expected. It is particularly intended to identify a situation where communications switching has occurred and the communications has been re-established onto paths where the symmetry requirements are not fully respected, but where the arising apparent differential current is insufficient to cause tripping. It is usually used to indicate that the telecommunications network is not configured as expected. It can also be used to block operation of the Current Differential protection until the issue has been resolved. If the communications paths between a pair of devices are running on different paths, the protection will calculate an apparent differential current even though the currents entering and leaving the protected zone balance. If this pseudo-differential current exceeds the criteria for tripping, maloperation will occur. If the level is less, it can be assumed to be caused by asymmetric communications paths and the restraint characteristic can be changed to

prevent tripping should the effect of increasing load current with communications asymmetry take the apparent differential current above the operate threshold.

Referring to the Switched Communication Path Supervision feature, if communication switching takes place, the Current Differential protection will detect a propagation delay change and invoke a temporary increase in the tripping threshold for a period set in the ***Char Mod Time*** setting column. When the timer expires, the standard characteristic is restored. Whilst the timer is active, the differential protection will be stable for asymmetric communication paths but if the asymmetry persists when the characteristic switches back, the protection might trip. Using the current differential supervision feature, the condition can be detected and maloperation can be prevented.

The function superimposes a second dual slope characteristic (defined by the settings ***IDiff Isup1*** and ***IDiff Isup2*** and ***Phase k1*** slope of the current differential protection) onto the standard operating characteristic as shown in the figure below:

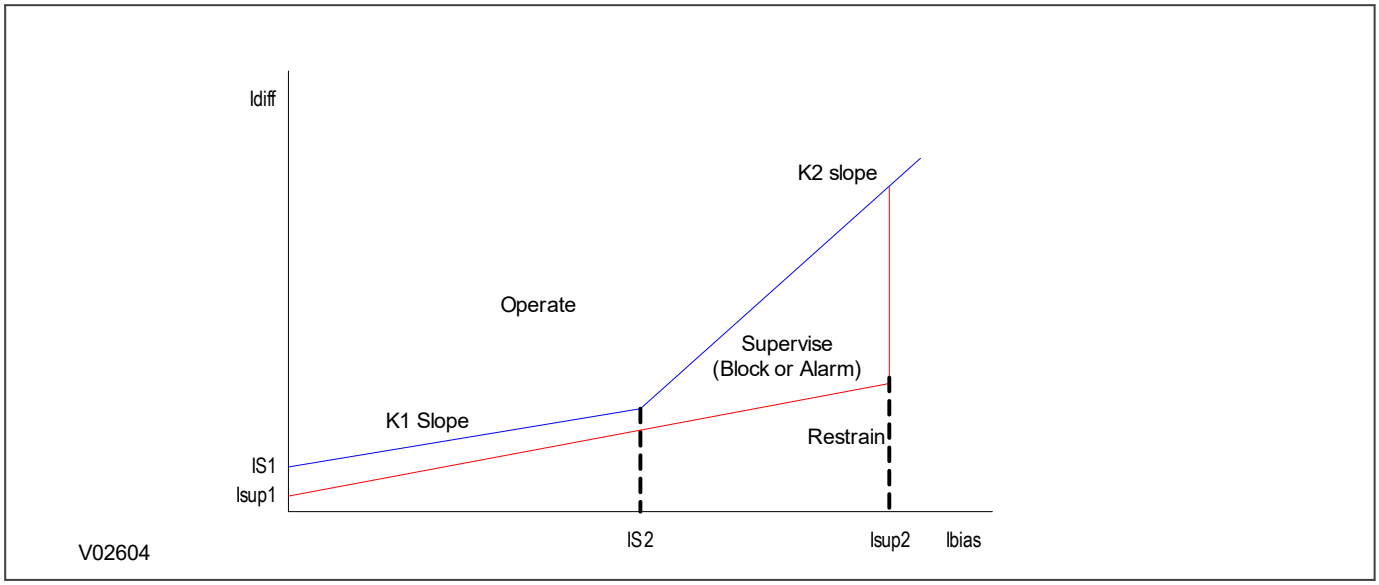


Figure 386: Communication asymmetry supervision

If you choose to use the function, we recommend that you set the pickup value of the differential supervision function (***IDiff Isup1***) be set at 80% of the ***Is1*** setting and the ***IDiff Isup2*** setting to 200% of ***Is2***. The delay between the condition being recognised and the alarm being raised is determined by the ***Idiff Sup TDelay*** setting.

Note:
Idiff Sup TDelay *must always be set greater than the value set in* ***Char Mod time****.*

20.2.4 GPS SYNCHRONISATION SUPERVISION

You can enable or disable GPS syncrhonisation supervision using the ***GPS Sync*** setting in the *PROT COMMS/ IM64* column. It is disabled by default. There are three options with which you can enable the GPS synchronisation. Each provides a different approach to supervising the Current Differential protection should the GPS synchronisation signal become corrupt or unavailable. The three options available are:

- *GPS -> Standard*
- *GPS -> Inhibit*
- *GPS -> Restrain*

If the GPS signal is available, terminals will be synchronised, and the communications paths propagation delay times (tp1 and tp2) will be continuously calculated and retained by each terminal. Should there be a failure of the GPS input, the synchronisation might be lost and the product will adapt its operation according to the chosen ***GPS Sync*** setting as explained below.

GPS Standard

If *GPS -> Standard* is selected, the time alignment of the current data is performed by using the values of propagation delay times (tp1, tp2) that were calculated and stored prior to the GPS failure. Each terminal continues to measure the overall propagation delay (tp1+tp2). If the overall propagation delay remains unchanged, the differential protection will continue to use the stored values until the GPS synchronisation is restored.

A communications delay tolerance setting (***Comm Delay Tol***) is provided. If the overall propagation delay changes but by an amount less than this setting, the differential protection will continue to use the stored values of tp1 and tp2 until GPS synchronisation is restored. If the overall propagation delay changes by an amount more than this setting, the differential protection will be blocked until GPS synchronisation is restored.

GPS Inhibit

With *GPS -> Inhibit* selected, if the propagation delay times are equal when the GPS synchronisation is lost, the product reverts to the ping-pong method of time alignment. If the propagation delays are not equal when the GPS signal is lost, the product performs in the same way as if *GPS -> Standard* had been selected, using the stored propagation delay times.

If the propagation delay changes by more than the ***Comm Delay Tol*** setting, the differential protection is blocked until GPS synchronisation is restored.

GPS Restrain

If *GPS -> Restrain* is selected in the ***GPS Sync*** setting, the supervision applied to the Current Differential function is the same as that for Switched Communications Paths Supervision described previously, and based on increasing the bias quantity if path switching is detected.

In this case, if GPS has failed, and if the difference between successive propagation delay time measurements exceeds the user settable ***Comm Delay Tol*** value, the device asserts the ***Comm Delay Alarm*** DDB signal and initiates the temporary change in the bias characteristic managed by the ***Char Mod Time*** and ***Char Mod RstTime*** settings.

20.2.4.1 PROPOGATION DELAY MANAGEMENT

When GPS synchronisation is used, there are some settings that are provided to control the behaviour of the product according to the propagation delay times between terminals. These are described, together with some related settings in the table below:

Setting	Description
Prop Delay Equal	This applies if the device is using GPS synchronisation. If the GPS signal is lost and there is a switch in the protection communications network, the differential protection is inhibited. When the GPS is restored, the differential protection will return to service. Using this setting you can return the differential protection to service in the absence of the GPS signal. Before activating this setting you must be sure that the communication receiver and transmitter path delays (go and return) are equal, otherwise false tripping may occur. The setting is invisible when GPS Sync is disabled.
Prop Delay Stats	This setting enables (activates) or disables (turns off) the alarms of Maximum propagation delay time described by the ***MaxCh1 PropDelay*** and ***MaxCh2 PropDelay*** settings
MaxCh1 PropDelay	When the protection communications are enabled, the overall propagation delay divided by 2 is calculated for channel 1. The maximum value is determined and displayed in the *MEASUREMENTS 4* column. The value is compared against the ***MaxCh1 PropDelay*** setting. If the setting is exceeded, an alarm ***MaxCh1 PropDelay*** DDB is raised.
MaxCh2 PropDelay	When the protection communications are enabled, and where used, the overall propagation delay divided by 2 is calculated for channel 2. The maximum value is determined and displayed in the *MEASUREMENTS 4* column. The value is compared against the ***MaxCh2 PropDelay*** setting. If the setting is exceeded, an alarm ***MaxCh2 PropDelay*** DDB is raised.
TxRx Delay Stats	This is used to enable (activate) or disable (turn off) the alarms of absolute difference between the Transmission and Reception propagation delay. This setting is not visible if GPS Sync is disabled.

Setting	Description
MaxCh1 Tx-RxTime	When Current Diff is enabled and if GPS Sync is not disabled, the absolute difference between the Transmission and Reception propagation delay on channel 1 is calculated. The maximum value is displayed in the *MEASUREMENTS 4* column. The value is compared against the ***MaxCh1 Tx-RxTime*** setting. If the setting is exceeded, an alarm, ***MaxCh1 Tx-RxTime*** DDB is raised.
MaxCh2 Tx-RxTime	When Current Diff is enabled and if GPS Sync is not disabled, if channel 2 is used, the absolute difference between the Transmission and Reception propagation delay is calculated. The maximum value is displayed in the *MEASUREMENTS 4* column. The value is compared against the ***MaxCh2 Tx-RxTime*** setting. If the setting is exceeded, an alarm, ***MaxCh2 Tx-RxTime*** DDB is raised.
GPS Fail Timer	This sets the time delay after which the GPS Alarm signal is asserted following a loss of GPS signal or by initiation by the GPS transient fail alarm function described by the setting GPS Trans Fail.
GPS Trans Fail	To enable (activate) or disable (turn off) the transient GPS Fail alarm function described by the GPS Trans Count and GPS Trans Timer settings.
GPS Trans Count	Sets the count for the number of failed GPS signals which must be exceeded in the GPS Trans Timer setting window after which the GPS Fail Timer is initiated.
GPS Trans Timer	Sets the rolling time window in which the GPS Trans Count must be exceeded after which the GPS Fail Timer is initiated.

20.3 VOLTAGE TRANSFORMER SUPERVISION

The Voltage Transformer Supervision (VTS) function is used to detect failure of the AC voltage inputs to the protection. This may be caused by voltage transformer faults, overloading, or faults on the wiring, which usually results in one or more of the voltage transformer fuses blowing.

If there is a failure of the AC voltage input, the IED could misinterpret this as a failure of the actual phase voltages on the power system, which could result in unnecessary tripping of a circuit breaker.

The VTS logic is designed to prevent such a situation by detecting voltage input failures, which are NOT caused by power system phase voltage failure, and automatically blocking associated voltage dependent protection elements. A time-delayed alarm output is available to warn of a VTS condition.

The following scenarios are possible with respect to the failure of the VT inputs.

- Loss of one or two-phase voltages
- Loss of all three-phase voltages under load conditions
- Absence of three-phase voltages upon line energisation

20.3.1 LOSS OF ONE OR TWO PHASE VOLTAGES

If the power system voltages are healthy, no Negative Phase Sequence (NPS) current will be present. If however, one or two of the AC voltage inputs are missing, there will be Negative Phase Sequence voltage present, even if the actual power system phase voltages are healthy. VTS works by detecting Negative Phase Sequence (NPS) voltage without the presence of Negative Phase Sequence current. So if there is NPS voltage present, but no NPS current, it is certain that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

The Negative Sequence VTS Element is blocked by the ***Any Pole Dead*** DDB signal during ***SP AR Dead Time***. The resetting of the blocking signal is delayed by 240 ms after an ***Any Pole Dead*** condition disappears.

20.3.2 LOSS OF ALL THREE PHASE VOLTAGES

If all three voltage inputs are lost, there will be no Negative Phase Sequence quantities present, but the device will see that there is no voltage input. If this is caused by a power system failure, there will be a step change in the phase currents. However, if this is not caused by a power system failure, there will be no change in any of the phase currents. So if there is no measured voltage on any of the three phases and there is no change in any of the phase currents, this indicates that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation.

To avoid blocking VTS due to changing load condition, the superimposed current signal can only prevent operation of the VTS during the time window of 40 ms following the voltage collapse.

20.3.3 ABSENCE OF ALL THREE PHASE VOLTAGES ON LINE ENERGISATION

On line energisation there should be a change in the phase currents as a result of loading or line charging current. Under this condition we need an alternative method of detecting three-phase VT failure.

If there is no measured voltage on all three phases during line energisation, two conditions might apply:

- A three-phase VT failure
- A three-phase fault.

The first condition would require VTS to block the voltage-dependent functions.

In the second condition, voltage dependent functions should not be blocked, as tripping is required.

To differentiate between these two conditions an overcurrent level detector is used (***VTS I> Inhibit***). This prevents a VTS block from being issued in case of a genuine fault. This overcurrent level detector is only enabled for 240 ms following line energisation (based on an ***All Poles Dead*** signal drop off). It must still be set below any three-phase fault along the line.

If the line is closed where a three-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

20.3.4 VTS IMPLEMENTATION

VTS is implemented in the *SUPERVISION* column of the relevant settings group.

The following settings are relevant for VT Supervision:

- ***VTS Mode***: determines the mode of operation (Measured + MCB, Measured Only, MCB Only)
- ***VTS Status***: determines whether the VTS Operate output will be a blocking output or an alarm indication only
- ***VTS Reset Mode***: determines whether the Reset is to be manual or automatic
- ***VTS Time Delay***: determines the operating time delay
- ***VTS I> Inhibit***: inhibits VTS operation in the case of a phase overcurrent fault
- ***VTS I2> Inhibit***: inhibits VTS operation in the case of a negative sequence overcurrent fault

For faults with I2 less than the setting ***VTS I2 Inhibit***, VTS will be active and block the associated functions if sufficient V2 is measured. VTS is only enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions.

Thresholds

The negative sequence thresholds used by the element are:

- V2 = 10 V (fixed)
- I2 = 0.05 to 0.5 In settable (default 0.05 In).

The phase voltage level detectors are:

- Drop off = 10 V (fixed)
- Pickup = 30 V (fixed)

The sensitivity of the superimposed current elements is fixed at 0.1 In.

Fuse fail

The device includes a setting (***VT Connected***) in the *CT AND VT RATIOS* column, which determines whether there are voltage transformers connected to it. If set to `No`, this setting has no effect.

If set to `No` it causes the VTS logic to set the ***VTS Slow Block*** and ***VTS Fast Block*** DDBs, but not raise any alarms. It also disables the VTS function. This prevents the pole dead logic working incorrectly if there is no voltage or current. It also blocks the distance, under voltage and other voltage-dependant functions. However, it does not affect the CB open part of the logic.

A VTS condition can be raised by a mini circuit breaker (MCB) status input, by internal logic using IED measurement, or both. The setting ***VTS Mode*** is used to select the method of indicating VT failure.

20.3.5 VTS LOGIC

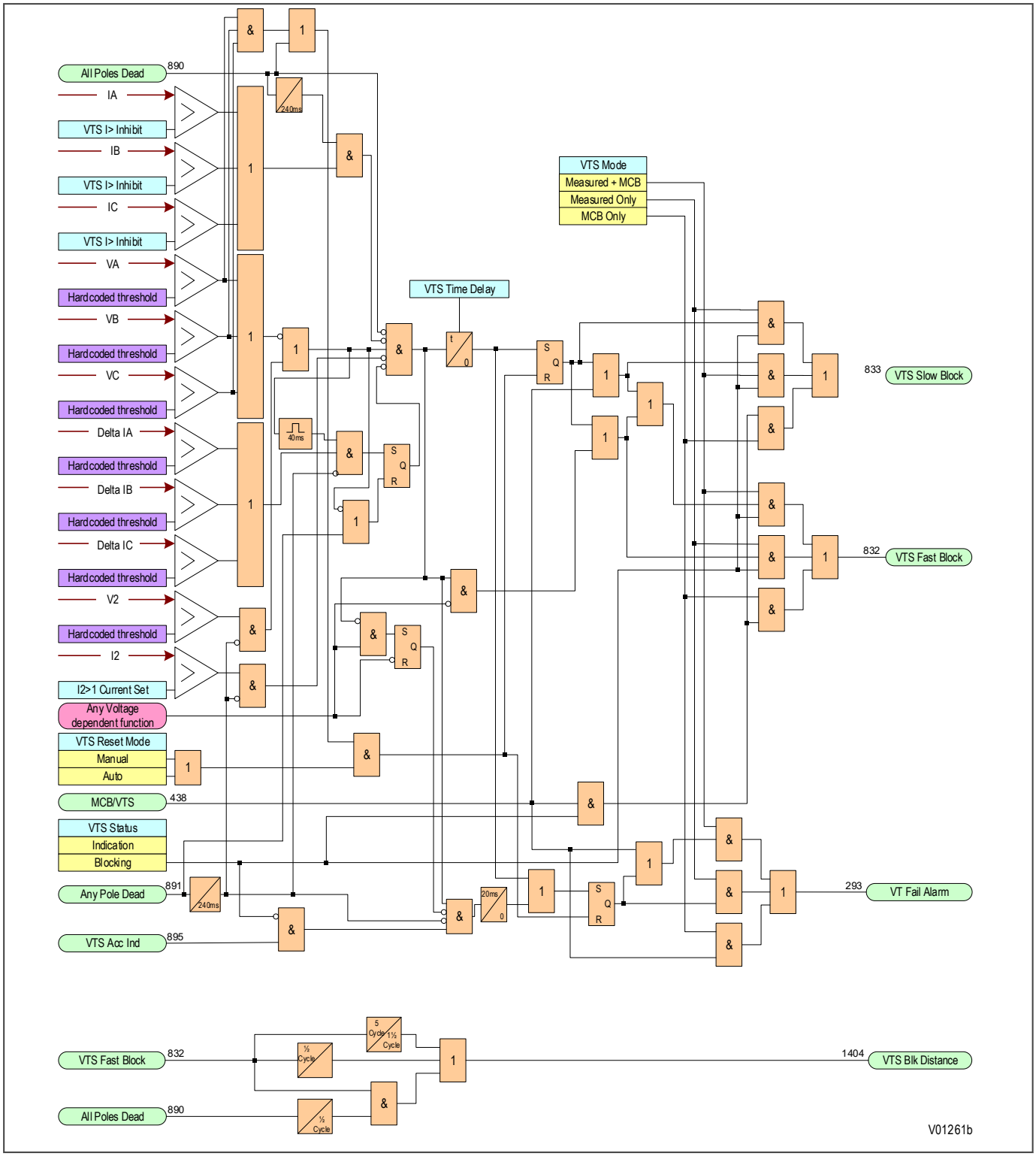


Figure 387: VTS logic

The IED may respond as follows, on operation of any VTS element:

- VTS set to provide alarm indication only
- Optional blocking of voltage-dependent protection elements
- Optional conversion of directional overcurrent elements to non-directional protection (by setting the relevant current protection status cells to *Enabled VTS*. In this case, the directional setting cells are automatically set to *non-directional*.)

The ***VTS I> Inhibit*** or ***VTS I2> Inhibit*** elements are used to override a VTS block if a fault occurs that could trigger the VTS logic. However, once the VTS block is set, subsequent system faults must not override the block. Therefore the VTS block is latched after a settable time delay (***VTS Time Delay***). Once the signal has latched, there are two methods of resetting. The first is manually using the front panel HMI, or remote communications (if the VTS condition has been removed). The second is in Auto mode, by restoring the 3 phase voltages above the phase level detector settings mentioned previously.

VTS Status can be set to *Disabled*, *Blocking* or *Indication*. If ***VTS Status*** is set to *Blocking*, a VTS condition will block operation of the relevant protection elements. In this case, a VTS indication is given after the ***VTS Time Delay*** has expired. If it is set to *Indication*, their is a risk of maloperation because protection elements are not blocked. In this case the VTS indication is given before the ***VTS Time Delay*** expires, if a trip signal is given (in this case a signal from the VTS acceleration logic is used as an input).

This scheme also operates correctly under very low load or even no load conditions. To achieve this, it uses a combination of time delayed signals derived from the DDB signals ***VTS Fast Block*** and ***All Poles Dead***, to generate the distance blocking DDB signal called ***VTS Blk Distance.***

Note:
*All non-distance voltage-dependent elements are blocked by the **VTS Fast Block** DDB.*

If a miniature circuit breaker (MCB) is used to protect the voltage transformer output circuits, MCB auxiliary contacts can be used to indicate a three-phase output disconnection. It is possible for the VTS logic to operate correctly without this input, but this facility has been provided to maintain compatibility with some practises. Energising an opto-isolated input assigned to the ***MCB/VTS*** provides the necessary block.

The VTS function is inhibited if:

- An ***All Poles Dead*** DDB signal is present
- Any phase overcurrent condition exists
- A Negative Phase Sequence current exists
- If the phase current changes over the period of 1 cycle

20.4 CURRENT TRANSFORMER SUPERVISION

The Current Transformer Supervision function (CTS) is used to detect failure of the AC current inputs to the protection. This may be caused by internal current transformer faults, overloading, or faults on the wiring. If there is a failure of the AC current input, the protection could misinterpret this as a failure of the actual phase currents on the power system, which could result in maloperation. Also, an open circuit in the AC current circuits can cause dangerous CT secondary voltages to be generated.

The IED has two methods of providing Current Transformer Supervision (CTS); differential and standard. The differential method uses the ratio between positive and negative sequence currents to determine CT failure. This method is not voltage dependant and relies on channel communications to declare a CTS condition.

The standard method relies on local measurements of zero sequence currents and voltages. You select the method according to the application. Both methods can be applied individually or in parallel.

The ***CTS Mode*** setting in the *SUPERVISION* column is used to set the method. The options are:

- Disabled
- Standard
- Idiff
- Idiff + Std

The ***CTS Reset Mode*** setting determines whether the CTS will reset automatically or will need manual intervention.

20.4.1 DIFFERENTIAL CTS

Differential CTS does not need any local voltage measurements to determine a CTS condition. It is based on measurement of the ratio of negative sequence current to positive sequence current (I2/I1) at all line ends. When this ratio is small (theoretically zero), one of four possible conditions apply:

- The system is unloaded (both I2 and I1 are zero)
- The system is loaded but balanced (I2 is zero)
- The system has a three phase fault present (I2 is zero)
- There is a genuine 3 phase CT problem (unlikely, but if this is the case it would probably develop from a single or two phase condition)

If the ratio is non-zero, we can assume one of two conditions are present:

- The system has an unbalanced fault (both I2 and I1 are non-zero)
- There is a 1 or 2 phase CT problem (both I2 and I1 are non-zero)

Measurement at a single end cannot provide any more information than this. However, if the ratio is calculated at all ends and compared, the device can make a decision based on the following criteria:

- If the ratio is non-zero at more than two ends, it is almost certainly a genuine fault condition and so the CT supervision is prevented from operating.
- If the ratio is non-zero at one end, there is a chance of either a CT problem or a single-end fed fault condition.

A second criterion looks to see whether the differential system is loaded or not. For this purpose the device looks at the positive sequence current I1. If load current is detected at one-end only, the device assumes that this is an internal fault condition and prevents CTS operation. However, if load current is detected at two or more ends, this indicates CT failure, so CTS operation is allowed.

There are two modes of operation, *Indication* and *Restrain*. You determine the mode of operation with the ***CTS Status*** setting. In *Indication* mode, a CTS alarm is raised but there is no effect on tripping. In *Restrain* mode, the differential protection is blocked for 20 ms after CT failure detection, then the Current Differential threshold setting is raised above the load current.

For correct operation of the scheme, Differential CTS must be enabled at each end of the protected zone.

20.4.2 DIFFERENTIAL CTS LOGIC

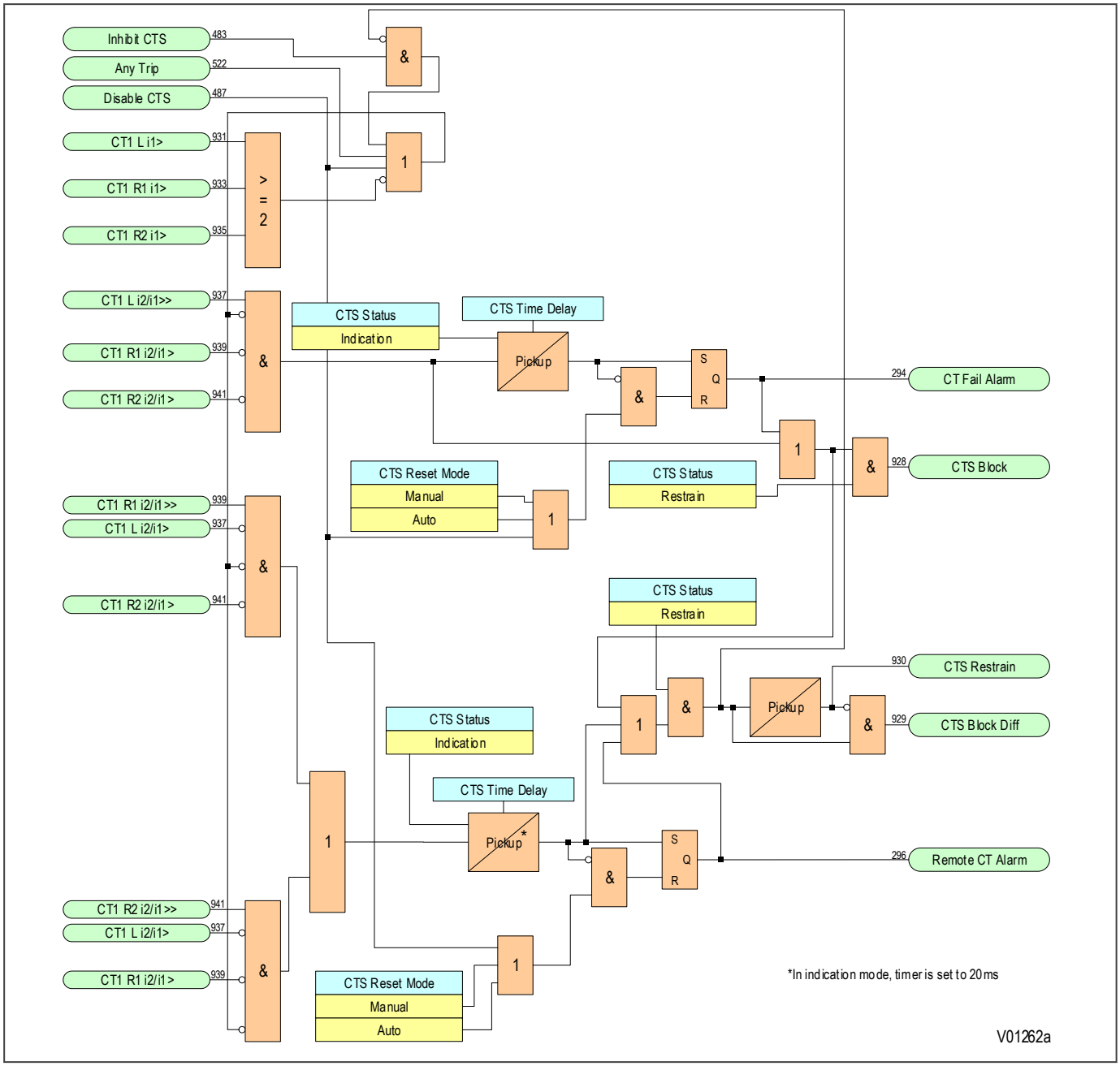


Figure 388: 'Differential' CT supervision logic

20.4.3 DIFFERENTIAL CTS LOGIC

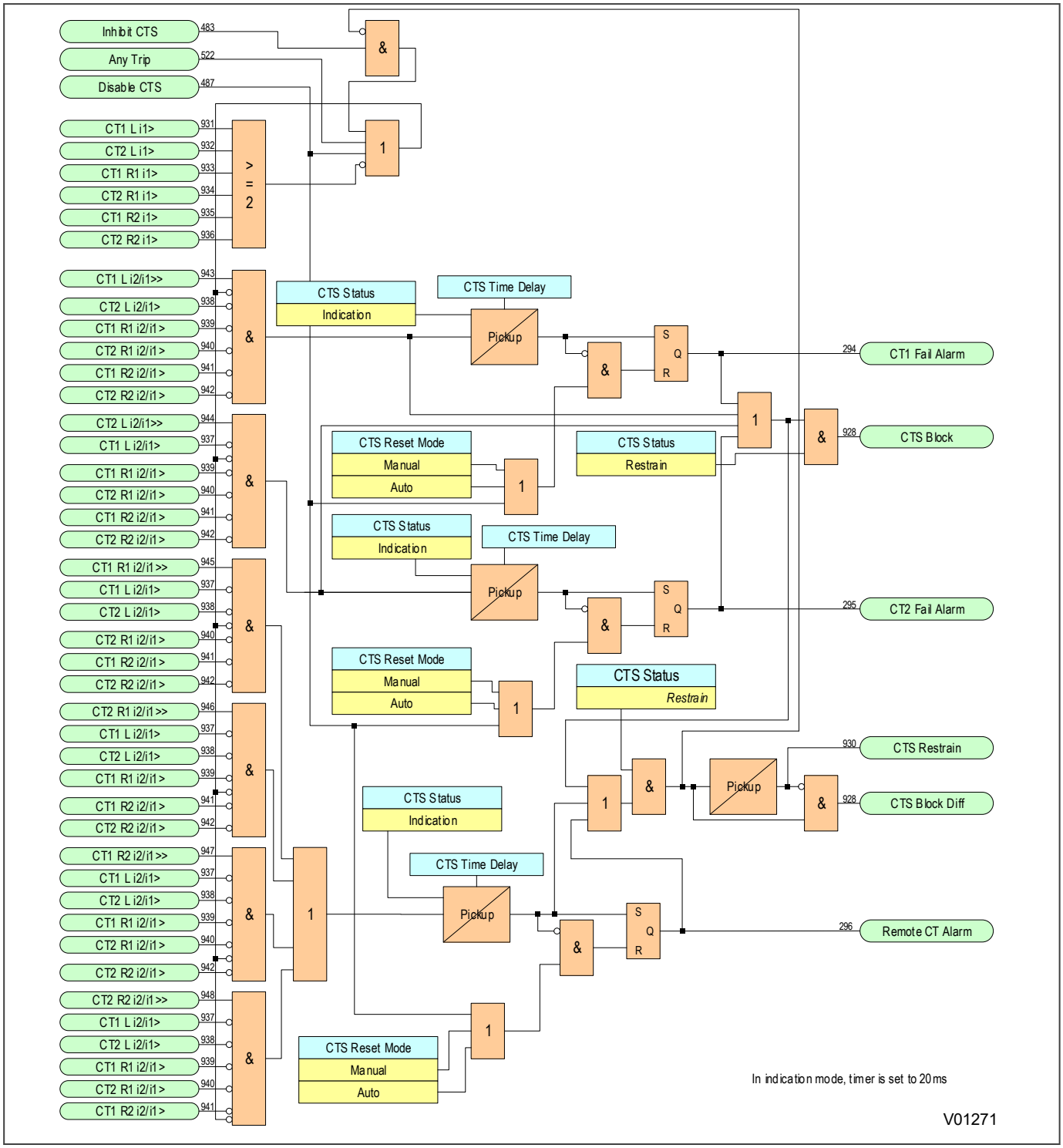


Figure 389: Differential CTS (dual-CB)

20.4.4 STANDARD CTS IMPLEMENTATION

If the power system currents are healthy, no zero sequence voltage are derived. However, if one or more of the AC current inputs are missing, a zero sequence current would be derived, even if the actual power system phase

currents are healthy. Standard CTS works by detecting a derived zero sequence current where there is no corresponding derived zero sequence voltage.

The voltage transformer connection used must be able to refer zero sequence voltages from the primary to the secondary side. Therefore, this element should only be enabled where the VT is of a five-limb construction, or comprises three single-phase units with the primary star point earthed.

The CTS function is implemented in the *SUPERVISION* column of the relevant settings group, under the sub-heading *CT SUPERVISION*.

The following settings are relevant for CT Supervision:

- ***CTS Status***: to disable or enable CTS
- ***CTS VN< Inhibit***: inhibits CTS if the zero sequence voltage exceeds this setting
- ***CTS IN> Set***: determines the level of zero sequence current
- ***CTS Time Delay***: determines the operating time delay

20.4.5 STANDARD CTS LOGIC

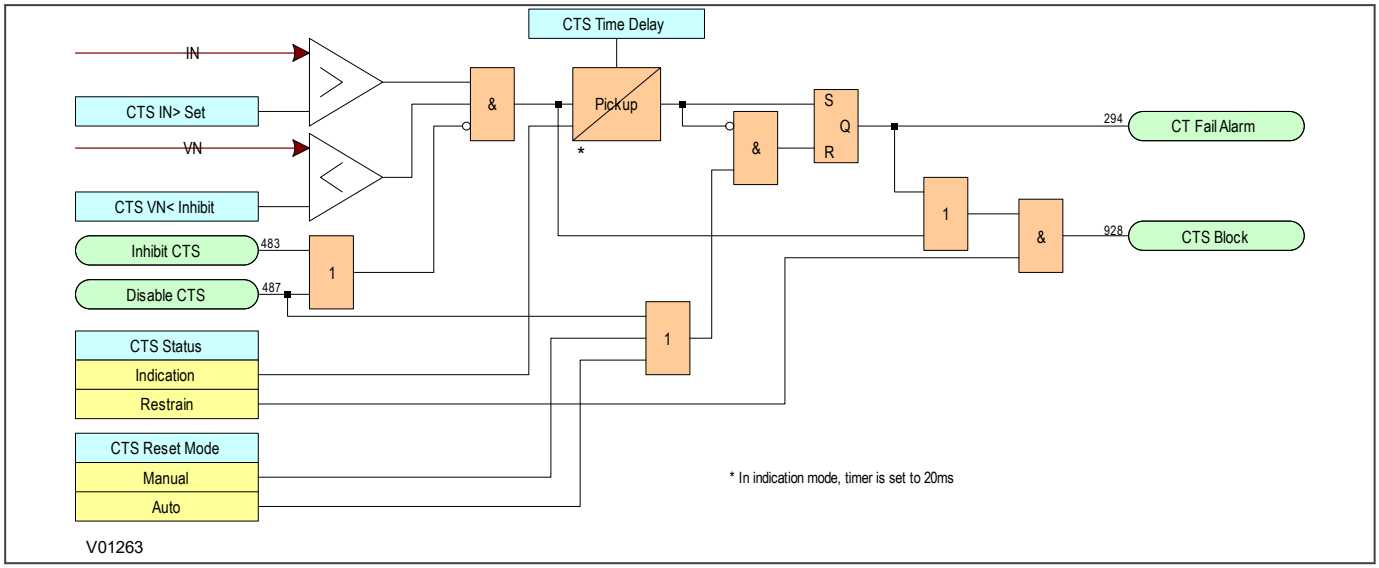


Figure 390: 'Standard' CT supervision logic

20.4.6 STANDARD CTS LOGIC

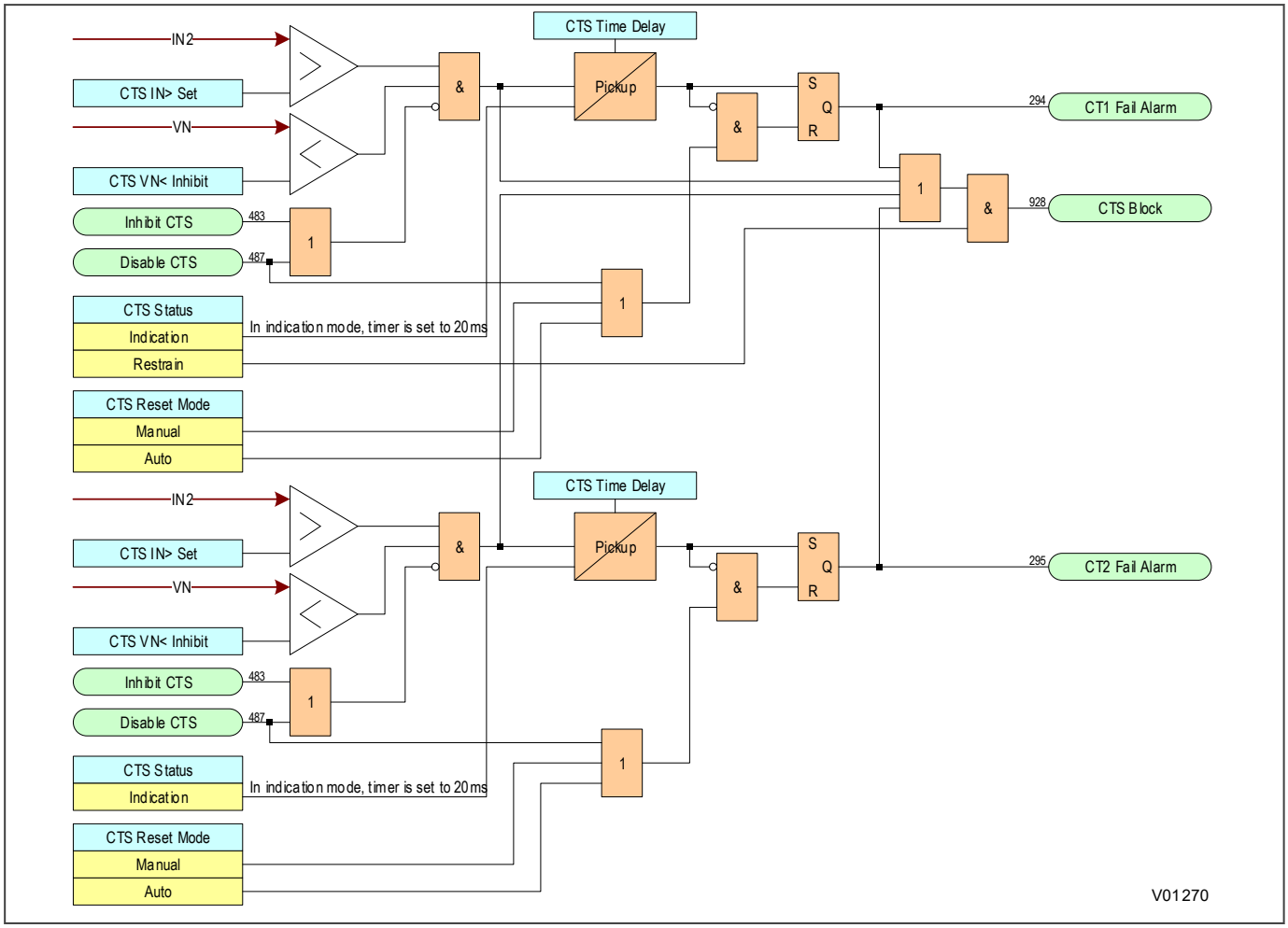


Figure 391: Standard CTS

20.4.7 CTS BLOCKING

Both the standard and differential CTS methods block protection elements operating from derived quantities, such as Broken conductor, derived earth fault and negative sequence overcurrent. Measured quantities such as DEF can be selectively blocked by designing an appropriate PSL scheme.

Differential CTS can be used to restrain the differential protection if required.

20.4.8 APPLICATION NOTES

20.4.8.1 SETTING GUIDELINES

The residual voltage setting, ***CTS VN< Inhibit*** and the residual current setting, ***CTS IN> Set***, should be set to avoid unwanted operation during healthy system conditions. For example:

- ***CTS VN< Inhibit*** should be set to 120% of the maximum steady state residual voltage.
- ***CTS IN> Set*** will typically be set below minimum load current.
- ***CTS Time Delay*** is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent protection elements being blocked during fault conditions.

20.4.8.2 DIFFERENTIAL CTS SETTING GUIDELINES

The ***Phase Is1 CTS*** setting must be set above the phase current of the maximum load transfer expected, normally at 1.2 In. This setting defines the minimum pick-up level of the current differential protection once the current transformer supervision CTS is detected.

The ***CTS i1>*** setting, once exceeded, indicates that the circuit is loaded. A default setting of 0.1 In is considered suitable for most applications, but could be lowered in case of oversized CTs.

The ***CTS i2/i1>*** setting should be in excess of the worst unbalanced load expected in the circuit under normal operation. It is recommended to read out the values of i2 and i1 in the *MEASUREMENTS 1* column and set the ratio above 5% of the actual ratio.

The ***CTS i2/i1>>*** setting should be kept at the default setting (40% In). If the ratio i2/i1 exceeds the value of this setting at only one end, the CT failure is declared.

Note:
The minimum generated i2/i1 ratio will be 50% (case of one CT secondary phase lead being lost), and therefore a setting of 40% is considered appropriate to guarantee sufficient operating speed.

20.5 TRIP CIRCUIT SUPERVISION

In most protection schemes, the trip circuit extends beyond the IED enclosure and passes through components such as links, relay contacts, auxiliary switches and other terminal boards. Such complex arrangements may require dedicated schemes for their supervision.

There are two distinctly separate parts to the trip circuit; the trip path, and the trip coil. The trip path is the path between the IED enclosure and the CB cubicle. This path contains ancillary components such as cables, fuses and connectors. A break in this path is possible, so it is desirable to supervise this trip path and to raise an alarm if a break should appear in this path.

The trip coil itself is also part of the overall trip circuit, and it is also possible for the trip coil to develop an open-circuit fault.

This product supports a number of trip circuit supervision (TCS) schemes.

20.5.1 TRIP CIRCUIT SUPERVISION SCHEME 1

This scheme provides supervision of the trip coil with the CB open or closed, however, it does not provide supervision of the trip path whilst the breaker is open. The CB status can be monitored when a self-reset trip contact is used. However, this scheme is incompatible with latched trip contacts, as a latched contact will short out the opto-input for a time exceeding the recommended Delayed Drop-off (DDO) timer setting of 400 ms, and therefore does not support CB status monitoring. If you require CB status monitoring, further opto-inputs must be used.

Note:
A 52a CB auxiliary contact follows the CB position. A 52b auxiliary contact is the opposite.

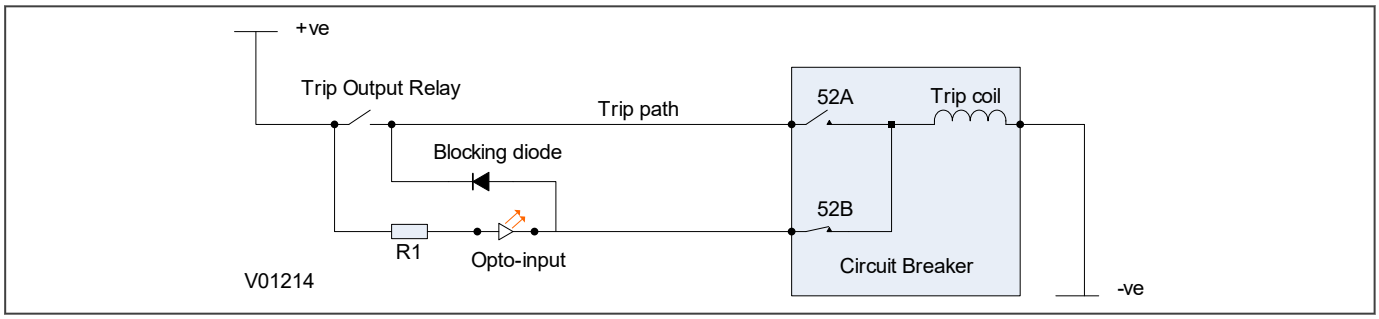


Figure 392: TCS scheme 1

When the CB is closed, supervision current passes through the opto-input, blocking diode and trip coil. When the CB is open, supervision current flows through the opto-input and into the trip coil via the 52b auxiliary contact. This means that *Trip Coil* supervision is provided when the CB is either closed or open, however *Trip Path* supervision is only provided when the CB is closed. No supervision of the trip path is provided whilst the CB is open (pre-closing supervision). Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

20.5.1.1 RESISTOR VALUES

The supervision current is a lot less than the current required by the trip coil to trip a CB. The opto-input limits this supervision current to less than 10 mA. If the opto-input were to be short-circuited however, it could be possible for the supervision current to reach a level that could trip the CB. For this reason, a resistor R1 is often used to limit the current in the event of a short-circuited opto-input. This limits the current to less than 60mA. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 (ohms)
48/54	24/27	1.2k
110/125	48/54	2.7k
220/250	110/125	5.2k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

20.5.1.2 PSL FOR TCS SCHEME 1

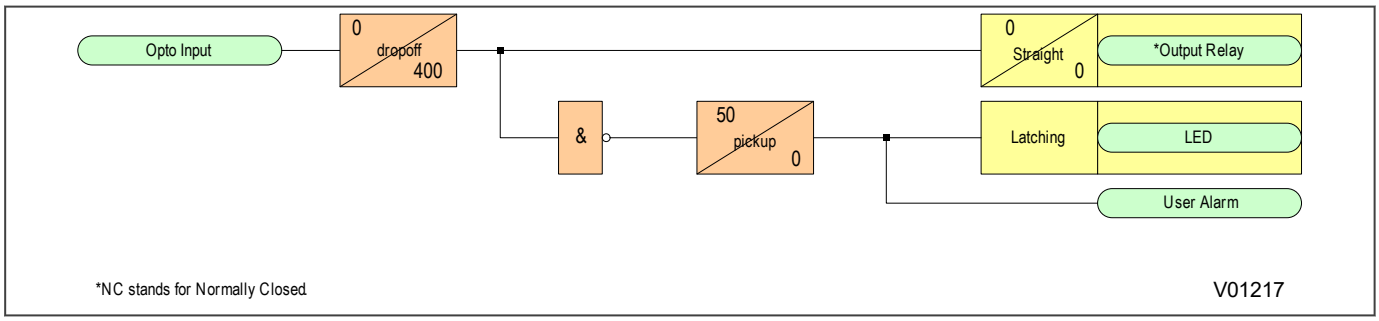


Figure 393: PSL for TCS scheme 1

The opto-input can be used to drive a Normally Closed Output Relay, which in turn can be used to drive alarm equipment. The signal can also be inverted to drive a latching programmable LED and a user alarm DDB signal.

The DDO timer operates as soon as the opto-input is energised, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto-input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the power up time, following a voltage supply interruption.

20.5.2 TRIP CIRCUIT SUPERVISION SCHEME 2

This scheme provides supervision of the trip coil with the breaker open or closed but does not provide pre-closing supervision of the trip path. However, using two opto-inputs allows the IED to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning one opto-input to the 52a contact and another opto-input to the 52b contact. Provided the ***CB Status*** setting in the *CB CONTROL* column is set to `Both 52A and 52B`, the IED will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

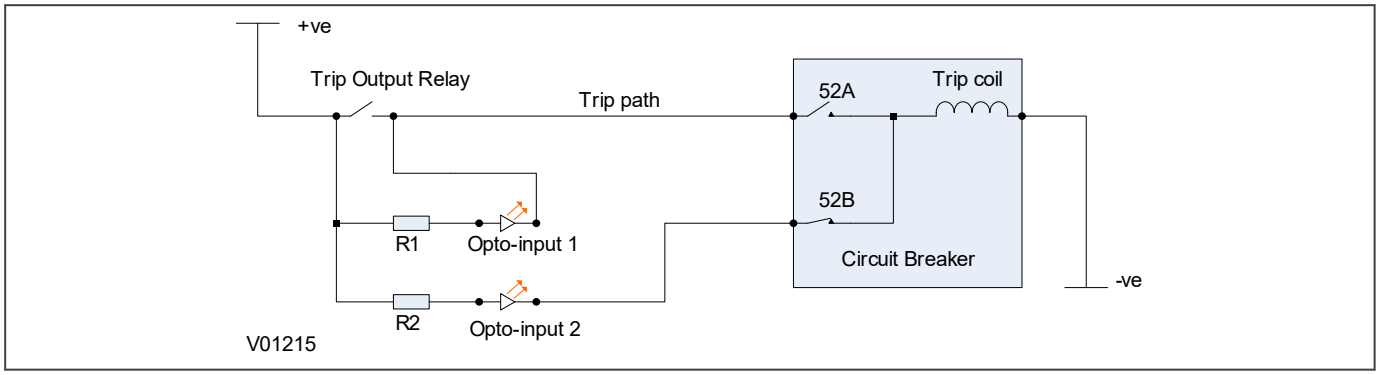


Figure 394: TCS scheme 2

When the breaker is closed, supervision current passes through opto input 1 and the trip coil. When the breaker is open current flows through opto input 2 and the trip coil. No supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

20.5.2.1 RESISTOR VALUES

Optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto-input is shorted. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 and R2 (ohms)
48/54	24/27	1.2k
110/125	48/54	2.7k
220/250	110/125	5.2k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

20.5.2.2 PSL FOR TCS SCHEME 2

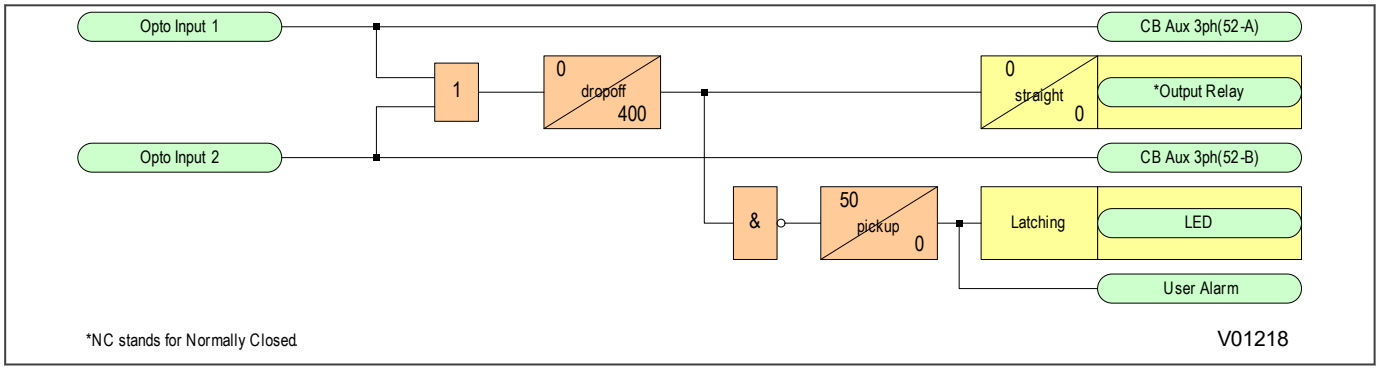


Figure 395: PSL for TCS scheme 2

In TCS scheme 2, both opto-inputs must be low before a trip circuit fail alarm is given.

20.5.3 TRIP CIRCUIT SUPERVISION SCHEME 3

TCS Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed. It provides pre-closing supervision of the trip path. Since only one opto-input is used, this scheme is not compatible with latched trip contacts. If you require CB status monitoring, further opto-inputs must be used.

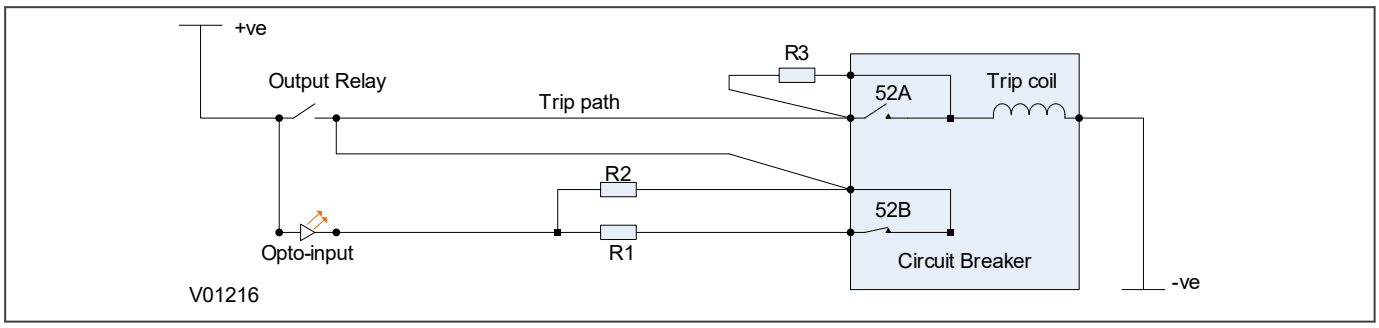


Figure 396: TCS scheme 3

When the CB is closed, supervision current passes through the opto-input, resistor R2 and the trip coil. When the CB is open, current flows through the opto-input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. The supervision current is maintained through the trip path with the breaker in either state, therefore providing pre-closing supervision.

20.5.3.1 RESISTOR VALUES

Resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes. This scheme is dependent upon the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)
48/54	24/27	1.2k	600
110/250	48/54	2.7k	1.2k
220/250	110/125	5.0k	2.5k



Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

20.5.3.2 PSL FOR TCS SCHEME 3

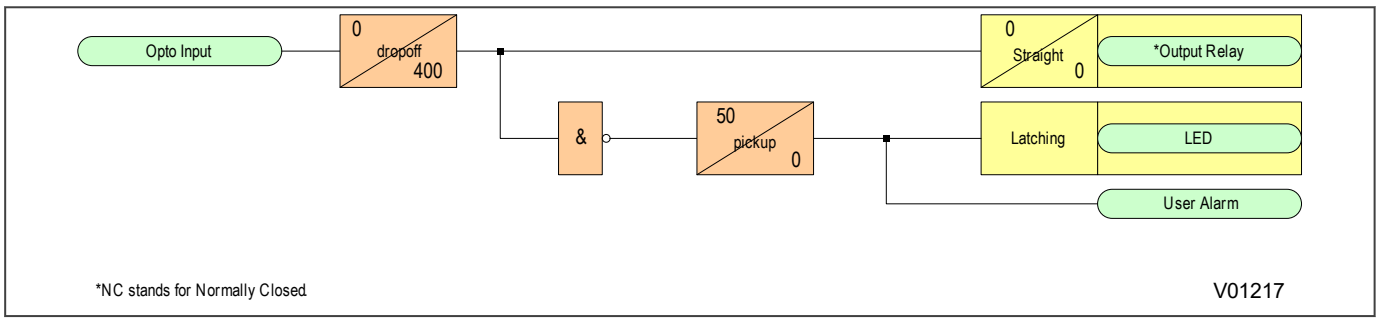


Figure 397: PSL for TCS scheme 3

CHAPTER 21

DIGITAL I/O AND PSL CONFIGURATION

21.1 CHAPTER OVERVIEW

This chapter introduces the PSL (Programmable Scheme Logic) Editor, and describes the configuration of the digital inputs and outputs. It provides an outline of scheme logic concepts and the PSL Editor. This is followed by details about allocation of the digital inputs and outputs, which require the use of the PSL Editor. A separate "Settings Application Software" document is available that gives a comprehensive description of the PSL, but enough information is provided in this chapter to allow you to allocate the principal digital inputs and outputs.

This chapter contains the following sections:

Chapter Overview 621
Configuring Digital Inputs and Outputs 622
Scheme Logic 623
Configuring the Opto-Inputs 625
Assigning the Output Relays 626
Fixed Function LEDs 627
Configuring Programmable LEDs 628
Function Keys 630
Control Inputs 631
User Alarms 632

21.2 CONFIGURING DIGITAL INPUTS AND OUTPUTS

Configuration of the digital inputs and outputs in this product is very flexible. You can use a combination of settings and programmable logic to customise them to your application. You can access some of the settings using the keypad on the front panel, but you will need a computer running the settings application software to fully interrogate and configure the properties of the digital inputs and outputs.

The settings application software includes an application called the PSL Editor (Programmable Scheme Logic Editor). The PSL Editor lets you allocate inputs and outputs according to your specific application. It also allows you to apply attributes to some of the signals such as a drop-off delay for an output contact.

In this product, digital inputs and outputs that are configurable are:

- Optically isolated digital inputs (opto-inputs). These can be used to monitor the status of associated plant.
- Output relays. These can be used for purposes such as initiating the tripping of circuit breakers, providing alarm signals, etc..
- Programmable LEDs. The number and colour of the programmable LEDs varies according to the particular product being applied.
- Function keys and associated LED indications. These are not provided on all products, but where they are, each function key has an associated tri-colour LED.
- IEC 61850 GOOSE inputs and outputs. These are only provided on products that have been specified for connection to an IEC61850 system, and the details of the GOOSE are presented in the documentation on IEC61850.
- InterMiCOM inputs and outputs. These are not used by all products. If your product is equipped with an InterMiCOM feature, you will find details of allocation and configuration in the chapter dedicated to the InterMiCOM function.

21.3 SCHEME LOGIC

The product is supplied with pre-loaded Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL).

The Scheme Logic is a functional module within the IED, through which all mapping of inputs to outputs is handled. The scheme logic can be split into two parts; the Fixed Scheme Logic (FSL) and the Programmable Scheme Logic (PSL). It is built around a concept called the digital data bus (DDB). The DDB encompasses all of the digital signals (DDBs) which are used in the FSL and PSL. The DDBs included digital inputs, outputs, and internal signals.

The FSL is logic that has been hard-coded in the product. It is fundamental to correct interaction between various protection and/or control elements. It is fixed and cannot be changed.

The PSL gives you a facility to develop custom schemes to suit your application if the factory-programmed default PSL schemes do not meet your needs. Default PSL schemes are programmed before the product leaves the factory. These default PSL schemes have been designed to suit typical applications and if these schemes suit your requirements, you do not need to take any action. However, if you want to change the input-output mappings, or to implement custom scheme logic, you can change these, or create new PSL schemes using the PSL editor.

The PSL consists of components such as logic gates and timers, which combine and condition DDB signals.

The logic gates can be programmed to perform a range of different logic functions. The number of inputs to a logic gate are not limited. The timers can be used either to create a programmable delay or to condition the logic outputs. Output contacts and programmable LEDs have dedicated conditioners.

The PSL logic is event driven. Only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This minimises the amount of processing time used by the PSL ensuring industry leading performance.

The following diagram shows how the scheme logic interacts with the rest of the IED.

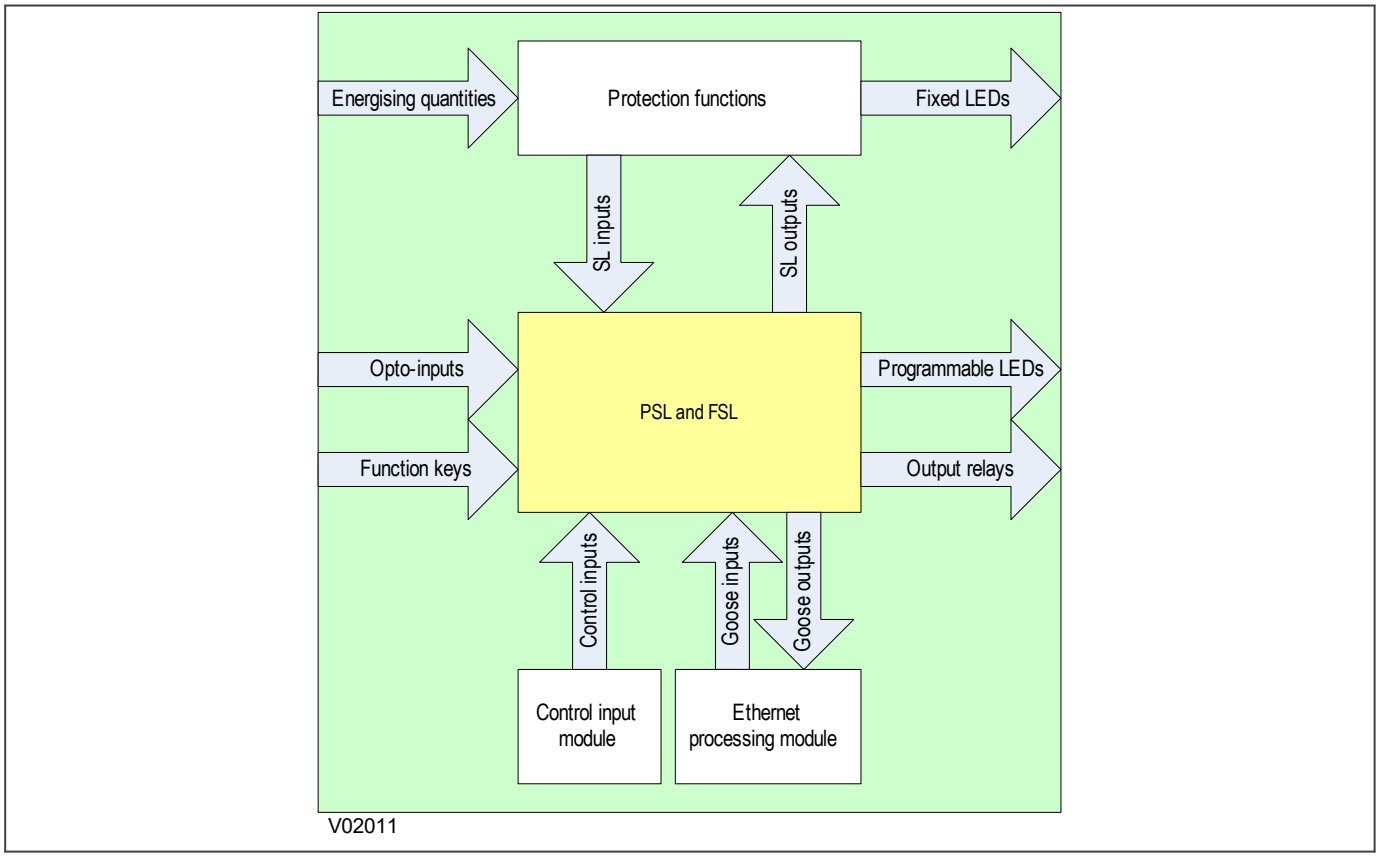


Figure 398: Scheme logic interfaces

21.3.1 PSL EDITOR

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised logic to qualify how the product manages its response to system conditions. The IED's digital inputs are combined with internally generated digital signals using logic gates, timers, and conditioners. The resultant signals are then mapped to digital outputs signals including output relays and LEDs.

The PSL Editor is a tool in the settings application software that allows you to create and edit scheme logic diagrams. You can use the default scheme logic which has been designed to suit most applications, but if it does not suit your application you can change it. If you create a different scheme logic with the software, you need to upload it to the device to apply it.

21.3.2 PSL SCHEMES

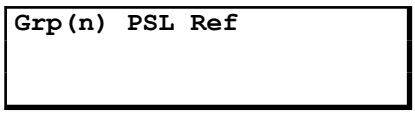
Your product is shipped with default scheme files. These can be used without modification for most applications, or you can choose to use them as a starting point to design your own scheme. You can also create a new scheme from scratch. To create a new scheme, or to modify an existing scheme, you will need to launch the settings application software. You then need to open an existing PSL file, or create a new one, for the particular product that you are using, and then open a PSL file. If you want to create a new PSL file, you should select **File** then **New** then **Blank scheme...** This action opens a default file appropriate for the device in question, but deletes the diagram components from the default file to leave an empty diagram with configuration information loaded. To open an existing file, or a default file, simply double-click on it.

21.3.3 PSL SCHEME VERSION CONTROL

To help you keep track of the PSL loaded into products, a version control feature is included. The user interface contains a *PSL DATA* column, which can be used to track PSL modifications. A total of 12 cells are contained in the *PSL DATA* column; 3 for each setting group.

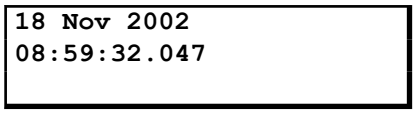
Grp(n) PSL Ref: When downloading a PSL scheme to an IED, you will be prompted to enter the relevant group number and a reference identifier. The first 32 characters of the reference identifier are displayed in this cell. The horizontal cursor keys can scroll through the 32 characters as the LCD display only displays 16 characters.

Example:



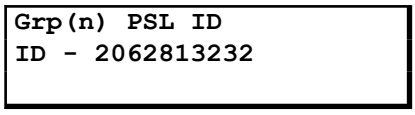
Date/time: This cell displays the date and time when the PSL scheme was downloaded to the IED.

Example:



Grp(n) PSL ID: This cell displays a unique ID number for the downloaded PSL scheme.

Example:



21.4 CONFIGURING THE OPTO-INPUTS

The number of optically isolated status inputs (opto-inputs) depends on the specific model supplied. The use of the inputs will depend on the application, and their allocation is defined in the programmable scheme logic (PSL). In addition to the PSL assignment, you also need to specify the expected input voltage. Generally, all opto-inputs will share the same input voltage range, but if different voltage ranges are being used, this device can accommodate them.

In the *OPTO CONFIG* column there is a global nominal voltage setting. If all opto-inputs are going to be energised from the same voltage range, you select the appropriate value in the setting. If you select `Custom` in the setting, then the cells ***Opto Input 1***, ***Opto Input 2***, etc. become visible. You use these cells to set the voltage ranges for each individual opto-input.

Within the *OPTO CONFIG* column there are also settings to control the filtering applied to the inputs, as well as the pick-up/drop-off characteristic.

The filter control setting provides a bit string with a bit associated with all opto-inputs. Setting the bit to '1' means that a half-cycle filter is applied to the inputs. This helps to prevent incorrect operation in the event of power system frequency interference on the wiring. Setting the field to '0' removes the filter and provides for faster operation.

The ***Characteristic*** setting is a single setting that applies to all the opto-inputs. It is used to set the pick-up/drop-off ratios of the input signals. As standard it is set to 80% pick-up and 60% drop-off, but you can change it to other available thresholds if that suits your operational requirements.

21.5 ASSIGNING THE OUTPUT RELAYS

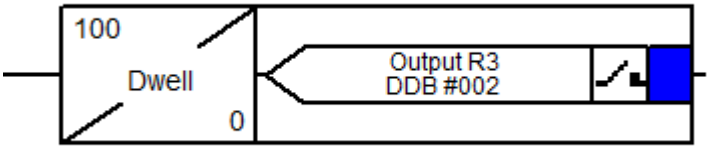
Relay contact action is controlled using the PSL. DDB signals are mapped in the PSL and drive the output relays. The driving of an output relay is controlled by means of a relay output conditioner. Several choices are available for how output relay contacts are conditioned. For example, you can choose whether operation of an output relay contact is latched, has delay on pick-up, or has a delay on drop-off. You make this choice in the **Contact Properties** window associated with the output relay conditioner.

To map an output relay in the PSL you should use the Contact Conditioner button in the toolbar to import it. You then condition it according to your needs. The output of the conditioner respects the attributes you have assigned.

The toolbar button for a Contact Conditioner looks like this:



The PSL contribution that it delivers looks like this:



Note:
Contact Conditioners are only available if they have not all been used. In some default PSL schemes, all Contact Conditioners might have been used. If that is the case, and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the relay outputs. The button looks like this:



This is the "Contact Signal" button. It allows you to put replica instances of a conditioned output relay into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

21.6 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

21.6.1 TRIP LED LOGIC

When a trip occurs, the trip LED is illuminated. It is possible to reset this with a number of ways:

- Directly with a reset command (by pressing the Clear Key)
- With a reset logic input
- With self-resetting logic

You enable the automatic self-resetting with the ***Sys Fn Links*** cell in the *SYSTEM DATA* column. A '0' disables self resetting and a '1' enables self resetting.

The reset occurs when the circuit is reclosed and the ***Any Pole Dead*** signal has been reset for three seconds providing the ***Any Start*** signal is inactive. The reset is prevented if the ***Any Start*** signal is active after the breaker closes.

The Trip LED logic is as follows:

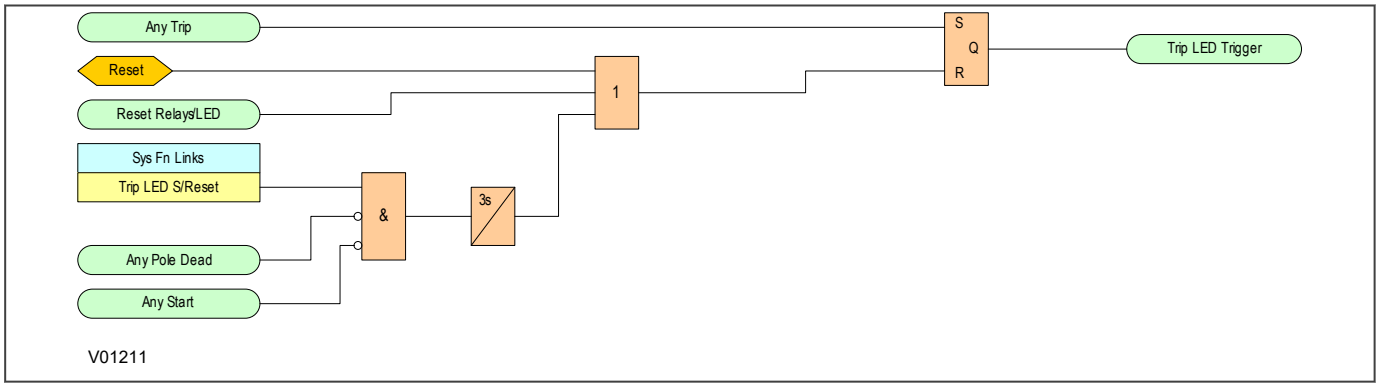


Figure 399: Trip LED logic

21.7 CONFIGURING PROGRAMMABLE LEDS

There are three types of programmable LED signals which vary according to the model being used. These are:

- Single-colour programmable LED. These are red when illuminated.
- Tri-colour programmable LED. These can be illuminated red, green, or amber.
- Tri-colour programmable LED associated with a Function Key. These can be illuminated red, green, or amber.

DDB signals are mapped in the PSL and used to illuminate the LEDs. For single-coloured programmable LEDs there is one DDB signal per LED. For tri-coloured LEDs there are two DDB signals associated with the LED. Asserting ***LED # Grn*** will illuminate the LED green. Asserting ***LED # Red*** will illuminate the LED red. Asserting both DDB signals will illuminate the LED amber.

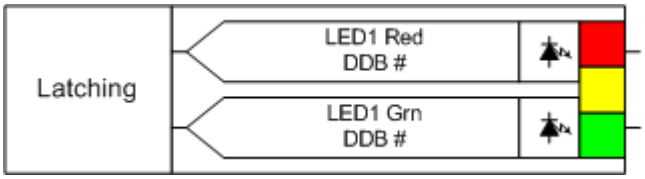
The illumination of an LED is controlled by means of a conditioner. Using the conditioner, you can decide whether the LEDs reflect the real-time state of the DDB signals, or whether illumination is latched pending user intervention.

To map an LED in the PSL you should use the LED Conditioner button in the toolbar to import it. You then condition it according to your needs. The output(s) of the conditioner respect the attribute you have assigned.

The toolbar button for a tri-colour LED looks like this:



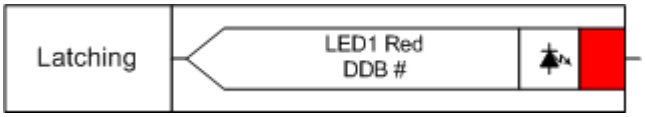
The PSL contribution that it delivers looks like this:



The toolbar button for a single-colour LED looks like this:



The PSL contribution that it delivers looks like this.



Note:
LED Conditioners are only available if they have not all been used up, and in some default PSL schemes they might be. If that is the case and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the LEDs. For a tri-coloured LED the button looks like this:



For a single-colour LED it looks like this: 

It is the "LED Signal" button. It allows you to put replica instances of a conditioned LED into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

Note:
All LED DDB signals are always shown in the PSL Editor. However, the actual number of LEDs depends on the device hardware. For example, if a small 20TE device has only 4 programmable LEDs, LEDs 5-8 will not take effect even if they are mapped in the PSL.

21.8 FUNCTION KEYS

For most models, a number of programmable function keys are available. This allows you to assign function keys to control functionality via the programmable scheme logic (PSL). Each function key is associated with a programmable tri-colour LED, which you can program to give the desired indication on activation of the function key.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are found in the *FUNCTION KEYS* column.

Each function key is associated with a DDB signal as shown in the DDB table. You can map these DDB signals to any function available in the PSL.

The ***Fn Key Status*** cell displays the status (energised or de-energised) of the function keys by means of a binary string, where each bit represents a function key starting with bit 0 for function key 1.

Each function key has three settings associated with it, as shown:

- ***Fn Key (n)***, which enables or disables the function key
- ***Fn Key (n) Mode***, which allows you to configure the key as toggled or normal
- ***Fn Key (n) label***, which allows you to define the function key text that is displayed

The ***Fn Key (n)*** cell is used to enable (unlock) or disable (unlock) the function key signals in PSL. The Lock setting has been provided to prevent further activation on subsequent key presses. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

When the ***Fn Key (n) Mode*** cell is set to `Toggle`, the function key DDB signal output will remain in the set state until a reset command is given. In the `Normal` mode, the function key DDB signal will remain energised for as long as the function key is pressed and will then reset automatically. In this mode, a minimum pulse duration can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The ***Fn Key Label*** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of all function keys are recorded in non-volatile memory. In case of auxiliary supply interruption their status will be maintained.

Note:
All function key DDB signals are always shown in the PSL Editor. However, the actual number of function keys depends on the device hardware. For example, if a small 20TE device has no function keys, the function key DDBs mapped in the PSL will not take effect.

21.9 CONTROL INPUTS

The control inputs are software switches, which can be set or reset locally or remotely. These inputs can be used to trigger any PSL function to which they are connected. There are three setting columns associated with the control inputs: *CONTROL INPUTS*, *CTRL I/P CONFIG* and *CTRL I/P LABELS*. These are listed in the Settings and Records appendix at the end of this manual.

21.10 USER ALARMS

User Alarms can be operated from an opto input or a control input using the PSL. They are useful for giving an alarm led and message on the LCD display, and an alarm indication via the communications of an external condition - for example: trip circuit supervision alarm, and temperature alarm etc. In the ***USER ALARMS*** menu, the ***Manual Reset*** 32 bit binary string (0 self-reset, 1 manual reset) can be used to set the operating mode of the user alarms to self or manual reset. The ***User Alarm 1-32*** labels in the ***USER ALARMS*** menu column are used to individually label each user alarm. The text is restricted to 16 characters.

CHAPTER 22

FIBRE TELEPROTECTION

22.1 CHAPTER OVERVIEW

This chapter provides information about the fibre-optic communication mechanism,which is used to provide unit schemes and general-purpose teleprotection signalling for protection of transmission lines and distribution feeders. The feature is called Fibre Teleprotection.

This chapter contains the following sections:

Chapter Overview 634

Protection Signalling Introduction 635

Fibre Teleprotection Implementation 637

IM64 Logic 647

Application Notes 649

22.2 PROTECTION SIGNALLING INTRODUCTION

Unit protection schemes can be formed by several IEDs located remotely from each other and some distance protection schemes. Such unit protection schemes need communication between each location to achieve a unit protection function. This communication is known as protection signalling or teleprotection. Communications facilities are also needed when remote circuit breakers need to be operated due to a local event. This communication is known as intertripping.

The communication messages involved may be quite simple, involving instructions for the receiving device to take some defined action (trip, block, etc.), or it may be the passing of measured data in some form from one device to another (as in a unit protection scheme).

Various types of communication links are available for protection signalling, for example:

- Private pilot wires installed by the utility
- Pilot wires or channels rented from a communications company
- Carrier channels at high frequencies over the power lines
- Radio channels at very high or ultra high frequencies
- Optical fibres

Whether or not a particular link is used depends on factors such as the availability of an appropriate communication network, the distance between protection relaying points, the terrain over which the power network is constructed, as well as cost.

Protection signalling is used to implement unit protection schemes, provide teleprotection commands, or implement intertripping between circuit breakers.

22.2.1 UNIT PROTECTION SCHEMES

Phase comparison and current differential schemes use signalling to convey information concerning the relaying quantity - phase angle of current and phase and magnitude of current respectively - between local and remote relaying points. Comparison of local and remote signals provides the basis for both fault detection and discrimination of the schemes.

22.2.2 TELEPROTECTION COMMANDS

Some Protection schemes use signalling to convey commands between local and remote relaying points. Receipt of the information is used to aid or speed up clearance of faults within a protected zone or to prevent tripping from faults outside a protected zone.

Teleprotection systems are often referred to by their mode of operation, or the role of the teleprotection command in the system.

Three types of teleprotection command are commonly encountered, direct tripping, permissive tripping and blocking schemes.

Direct tripping

In direct tripping applications (also known as intertripping), signals are sent directly to the master trip relay. Receipt of the command causes circuit breaker operation. The method of communication must be reliable and secure because any signal detected at the receiving end causes a trip of the circuit at that end. The communications system must be designed so that interference on the communication circuit does not cause spurious trips. If a spurious trip occurs, the primary system might be unnecessarily isolated.

Permissive tripping

Permissive trip commands are always monitored by a protection relay. The circuit breaker is tripped when receipt of the command coincides with a ‘start’ condition being detected by the protection relay at the receiving end responding to a system fault. Requirements for the communications channel are less onerous than for direct

tripping schemes, since receipt of an incorrect signal must coincide with a ‘start’ of the receiving end protection for a trip operation to take place. The intention of these schemes is to speed up tripping for faults occurring within the protected zone.

Blocking scheme

Blocking commands are initiated by a protection element that detects faults external to the protected zone. Detection of an external fault at the local end of a protected circuit results in a blocking signal being transmitted to the remote end. At the remote end, receipt of the blocking signal prevents the remote end protection operating if it had detected the external fault. Loss of the communications channel is less serious for this scheme than in others as loss of the channel does not result in a failure to trip when required. However, the risk of a spurious trip is higher.

22.2.3 TRANSMISSION MEDIA AND INTERFERENCE

The transmission media that provide the communication links involved in protection signalling can be:

- Private pilots
- Rented pilots or channels
- Power line carrier
- Radio
- Optical fibres

Historically, pilot wires and channels (discontinuous pilot wires with isolation transformers or repeaters along the route between signalling points) have been the most widely used due to their availability, followed by Power Line Carrier Communications (PLCC) techniques and radio. In recent years, fibre-optic systems have become the usual choice for new installations, primarily due to their complete immunity from electrical interference. The use of fibre-optic cables also greatly increases the number of communication channels available for each physical fibre connection and thus enables more comprehensive monitoring of the power system to be achieved by the provision of a large number of communication channels.

22.3 FIBRE TELEPROTECTION IMPLEMENTATION

The Fibre Teleprotection interface is an integral part of the Current Differential protection implementation for this product. It provides the communications necessary for the Current Differential protection schemes as well as intertripping command signalling which can be freely allocated to realise protection schemes such as Permissive and Blocking schemes.

If Current Differential protection is enabled, Fibre Teleprotection is enabled automatically. If you choose to disable the Current Differential protection, you can still use the Fibre Teleprotection feature for teleprotection command signalling. To do this you must enable the InterMiCOM 64 setting in the CONFIGURATION column. This setting will only be visible if Current Differential protection is disabled.

If you enable Fibre Teleprotection but have current differential protection disabled, the *CURRENT DIFF* column will be invisible. To re-enable Current Differential protection you must first set the ***InterMiCOM 64*** setting in the *CONFIGURATION* column to disabled. Enabling Current Differential protection will then automatically enable Fibre Teleprotection and the ***InterMiCOM 64*** setting in the *CONFIGURATION* column will disappear.

Each product can have up to 2 fibre-optic communications channels for teleprotection signalling. A range of different fibre-optic interfaces are available to provide:

- Direct fibre connections between devices with a number of options available to suit different requirements
- Indirect connections using the industry standard IEEE C37.94. Fibre-optic connections are made between the product and telecommunications equipment that supports industry standard fibre-optic interfaces (IEEE C37.94). The telecommunications equipment provides the end-to-end service.
- Fibre-optic connection in conjunction with proprietary auxiliary interface units to provide connection to standard electrical telecommunications interfaces (G.703, V.35, X.21). With this indirect connection method, the telecommunications equipment provides the end-to-end service.

Signals to be communicated between devices are constructed into packets (sometimes called telegrams). These packets include addressing, timing, and error checking information as well as teleprotection commands and data, and are transmitted between terminals at frequent regular intervals. Upon reception, they are checked for integrity before the contents are used.

Allocation of teleprotection commands is realised with mappings between InterMiCOM 64 signals and internal DDB logic signals using the product's the Programmable Scheme Logic (PSL).

22.3.1 SETTING UP THE IM64 SCHEME

To use the fibre teleprotection features in this product, you will need to configure the protection signalling scheme. The protection signalling scheme is defined by the number of connected terminals, together with the communications links between them.

Products can have either 1 physical fibre teleprotection channel, or two. Products with 1 physical fibre teleprotection channel can be used to connect two products together into a scheme. Products with 2 physical fibre teleprotection channels can be used to connect three products together into a scheme, or they can be used to connect two products together into a scheme with dual communications channels to provide communications redundancy (hot standby) in the event of a single communications channel failure.

For products with 2 physical fibre teleprotection channels use the ***Scheme Setup*** setting in the *PROT COMMS/ IM64* column. The choices are `3 Terminal`, `2 Terminal` (only physical Ch1 is used), and `Dual Redundant` (two terminals with two interconnecting channels).

The physical connections are labelled as Ch1 and Ch2.

In a two-terminal scheme, channel 1 of one device should always connect to channel 1 of the other device. For a two-terminal scheme with dual redundant communications, it follows that channel 2 of one device should connect to channel 2 of the other.

In a three terminal scheme, channel 1 of one device should always connect to channel 2 of another device as shown in the figure below.

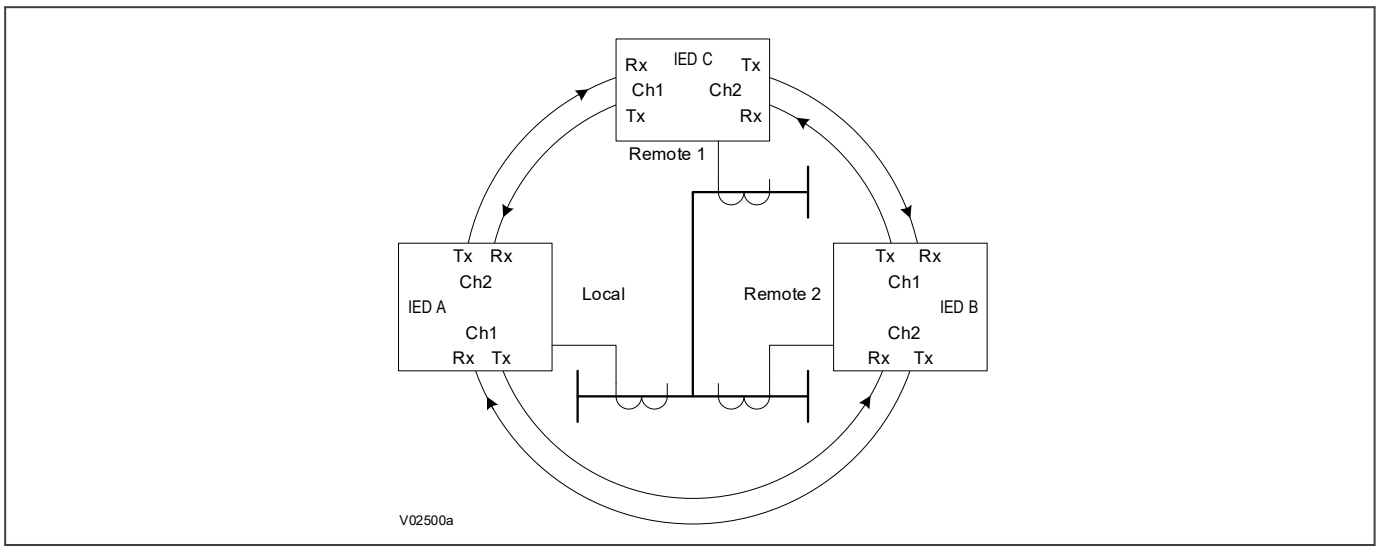


Figure 400: Fibre teleprotection connections for a three-terminal scheme

22.3.1.1 FIBRE TELEPROTECTION SCHEME TERMINAL ADDRESSING

In Fibre Teleprotection schemes, commands are packaged together with other important data for transmission over communications channels to the other devices. The packages of information are generally called ‘messages’. These messages are created for a specific destination where they will be acted upon to realise the overall scheme protection. It is critical that they are only used by the intended device. Making the correct channel connections may not always ensure that the messages get to the correct destination; there may be a possibility that communication paths may become cross-connected or looped back during telecommunications network switching operations. To avoid incorrect scheme operation, extra security is needed to ensure that messages are acted upon only by their intended recipient. This is achieved by means of an address field in the messages. The address field is used to individually match connected devices. A transmitting device includes the address of the intended recipient in the message. If the receiving device matches the address, the message will be used. If it does not match, it is discarded.

The address field is an 8-bit (or 32-bit*) field in the message . It can carry any 8-bit (or 32-bit*) value, but certain values have been chosen for maximum security. For convenience they have been arranged into 32 groups. All devices in a scheme must share the same group. For addressing, the different devices are referenced as ‘A’, ‘B’, and ‘C’ for three-terminal schemes. Their addresses should recognise the referencing.

So for a two-terminal scheme, if one device has the address set to ‘5-A’ the other should have the address to ‘5-B’.

Similarly, in a three-terminal scheme if one device has address ‘1-A’, the other devices would have addresses ‘1-B’ and ‘1-C’. The address is set using the address setting in the *PROT COMMS/IM64* column.

*If the ***Extended IM64*** mode is `Enabled`.

Note:
*In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

Note:
A universal address (0-0) is used as default. If this is used all products use the same address ‘0-0’. This is primarily intended to help test the product before it goes into service. We strongly recommend not to use 0-0 in service since any communications switching or loopback condition will not be detected and may cause false tripping.

Note:
For a three-terminal scheme, the A, B, and C parts of the address group should match the figure shown earlier for a triangulated scheme where device A has address A, device B has address B, and device C has address C.

22.3.1.2 SETTING UP IM64

In this product, the feature that manages the fibre teleprotection command signals is called InterMiCOM 64 (or IM64). IM64 is suitable for the exchange of all teleprotection command types.

Up to 2 banks of teleprotection command signals (IM64 signals) are provided. Each bank provides 8 (or 32*) duplex command signals. That means that each bank assigns 8 bits (or 32 bits*) for IM64 input signals and 8 bits (or 32 bits*) for IM64 output signals. Each bank is associated with a logical channel (referred to as Ch1 or Ch2 in the internal logic). Each logical channel associates with a physical communications channel (labelled Ch1 or Ch2 at the physical connection point). The association of logical channels to physical channels varies according to specific scheme configurations.

*If the ***Extended IM64*** mode is `Enabled`.

Note:
*In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

Action of each IM64 input signal is managed by attributes defined by three settings associated with it. These are set in the *PROT COMMS/IM64* column and are of the form:

- ***IM 1 Cmd Type*** (command type)
- ***IM 1 FallBackMode*** (fallback modes)
- ***IM 1 DefaultValue*** (default values)

The settings shown above are for bit 1 only

The IM64 command type settings set the teleprotection type. `Permissive` satisfies the security requirements of a permissive application, as well as the speed needed for a blocking scheme. For direct tripping applications, set it to `Direct`.

The IM64fallback settings determine the behaviour of an input under communications failure conditions. You can choose either to latch the state of the last good command received, or to revert to a default state. If you set the fallback mode to `Default` you will need to set the default state to your requirement (either 1 or 0).

The attributes assigned to bit n of an IM64 input apply to that bit in both logical channels. For example, if ***IM4 DefaultValue*** is chosen as `1` then the default value for bit 4 in logical channel 1 (IM64 Ch1 Input 4) will be the same for bit 4 in logical channel 2 (IM64 Ch2 Input 4), and will take the value 1.

22.3.1.3 TWO-TERMINAL IM64 OPERATION

The protection signalling connection requirement for products operating as a Two Terminal scheme is that the Physical Channels labelled as Ch1 should be connected together. That means that the local Ch1 Tx connects to the remote Ch1 Rx, and the local Ch1 Rx connects to the remote Ch1 Tx. Physical Channel 2 (Ch2) connectors may be fitted, but they are not used.

With current differential protection enabled

Only the 8-bits (or 32-bits*) of Logical Channel 1 (Ch1) are used, and they are all assigned to Physical Channel 1, so 8 (or 32*) duplex commands (IM64 Ch1 bits 1-8, or 1-32-bits*) can be communicated between terminals. The command bits are packaged with the Current Differential signals and use Ch1 Physical Channels.

With current differential protection disabled

The 8-bits (or 32-bits*) of both Logical Channels (Ch1 and Ch2) are used. The bits of both Logical Channels are all assigned to Physical Channel 1, so 16 (or 64) duplex commands (IM64 Ch1 bits 1-8 (1-32*) and IM64 Ch2 bits 1-8 (1-32*) can be communicated between terminals in IM64 messages using Ch1 Physical Channels.

*If the ***Extended IM64*** mode is `Enabled`.

Note:
*In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

22.3.1.4 DUAL REDUNDANT TWO-TERMINAL IM64 OPERATION

The protection signalling connection requirement for products operating as a Dual Redundant (Hot Standby) scheme is that the Physical Channels labelled as Ch1 should be connected together and the Physical Channels labelled as Ch2 should be connected together. That means that the local Ch1 Tx connects to the remote Ch1 Rx, the local Ch1 Rx connects to the remote Ch1 Tx, the local Ch2 Tx connects to the remote Ch2 Rx, and the local Ch2 Rx connects to the remote Ch2 Tx.

With current differential protection enabled

The 8 bits (or 32 bits*) of both Logical Channels (Ch1 and Ch2) are available, Logical Channel 1 is assigned to Physical Channel 1, and Logical Channel 2 is assigned to Physical Channel 2, so 16 (or 64*) duplex commands are potentially available.

To implement a true redundancy scheme, however, signals on Logical Channel 2 should be assigned identically to those on Logical Channel 1. Upon reception, the matched bits should be logically ‘OR’ed when mapped in the PSL.

In this application the command bits are packaged with the Current Differential signals. Current Differential protection and the IM64 signalling will be maintained in the event of a single communication channel failure.

With current differential protection disabled

The 8 bits (or 32 bits*) of both Logical Channels (Ch1 and Ch2) are used. The bits of both Logical Channels are all assigned both to Physical Channel 1 and to Physical Channel 2, so that 16 duplex commands (IM64 Ch1 bits 1-8 and IM64 Ch2 bits 1-8) can be communicated between terminals in IM64 messages with full redundancy of both Logical Channels in the event of failure of either Physical Channel.

*If the ***Extended IM64*** mode is `Enabled`.

Note:
*In the PROT COMMS/ IM64 column, **Extended IM64** mode is only available when the **Comms Mode** is set to either, `128 kbits/s` or `IEEE C37.94`. When the **Comms Mode** is set to `IEEE C37.94`, **Ch1 N*64 kbits/s** and **Ch2 N*64 kbits/s** settings are available and should be set to a minimum of `2`.*

22.3.1.5 THREE-TERMINAL IM64 OPERATION

The protection signalling connection requirement for products operating as a Three Terminal scheme is that Physical Channels labelled as Ch1 should be connected to Physical Channels labelled as Ch2 . That means that a local Ch1 Tx connects to a remote Ch2 Rx, and the corresponding Ch1 Rx and Ch2 Tx are connected together as shown in the earlier figure (Fibre Teleprotection Connections for a Three Terminal Scheme).

With current differential protection enabled

8 (or 32*) IM64 Fibre Teleprotection Commands can be transferred between pairs of terminals. Integrity of the Current Differential protection and the IM64 schemes can be maintained in the event of a communications link

failure by reverting to a master-slave-slave configuration where the terminal with healthy communications with the other terminals makes the tripping decision and sends intertrip commands to the other two. The master can also send 8 (or 32*) IM64 teleprotection commands to the remote terminals. The same commands are sent to both terminals .

In this IM64 application, the 8 bits (or 32 bits*) of both Logical Channels (Ch1 and Ch2) are available, Logical Channel 1 is assigned to Physical Channel 1, and Logical Channel 2 is assigned to Physical Channel 2. To implement a true redundancy scheme that will work correctly, the same IM64 bit assignments should be made at all three terminals and the signals on Logical Channel 2 should be assigned identically to those on Logical Channel 1. Upon reception, the matched bits should be logically ‘OR’ed when mapped in the PSL.

In this application the command bits are packaged with the Current Differential signals. Current Differential protection and the IM64 signalling will be maintained in the event of a single communication channel failure.

With current differential protection disabled

This Three Terminal scheme uses a triangulation approach and is designed to function if a communications link between two terminals is not present or is degraded. 8 duplex teleprotection commands are available between any pair of terminals even if one communication channel fails.

Logical Channel 1 is associated with Physical Channel 1, and Logical Channel 2 is associated with Physical Channel 2.

Consider a Three terminal scheme where the terminals are referenced as Local, Remote1, and Remote2. Remote 1 correlates to Ch1, and Remote 2 correlates to Ch2. The Local terminal will send the commands that it wants Remote 1 to act on to both Remote 1 and Remote 2. Upon receipt, Remote 1 acts upon the commands that the Local terminal wants it to use. Remote 1 also packages the commands that it wants Remote 2 to use, together with a copy of the commands that Local wants Remote 2 to use, and also the commands it wants Local to use. Remote 1 sends the message to Remote2. Remote 2 acts similarly. The same process occurs in the opposite direction around the ring, so in the event of a single channel failure, and if all terminals have the same mappings for the 8 (or 32*) IM64 bits integrity will be maintained for all 8 (or 32*) duplex commands between connected terminals.

In a triangulated scheme, at each terminal, Logical Channel 1 commands are assigned to Physical Channel 1, and Logical Channel 2 commands are assigned to Physical Channel 2. At each terminal, the eight IM64 commands transmitted on Physical Channel 1 are intended for the device connected as its Remote 1, and the eight IM64 commands transmitted on Channel 2 are intended for the device connected as its Remote 2. So, 8 (or 32*) full-duplex commands are available between any two terminals. Each device transmits both channels of eight IM64 commands to the connected devices. At the Remote 1 device, the eight Channel 1 IM64 commands are used directly by the receiving device which passes through the 8 (or 32*) Channel 2 IM64 commands to the remote 2 device. All three devices in the scheme perform similarly, ensuring that, so long as one device is able to communicate with the other two, scheme integrity is maintained.

*If the ***Extended IM64*** mode is `Enabled`.

> *Note:*
> *In the PROT COMMS/ IM64 column,* ***Extended IM64*** *mode is only available when the* ***Comms Mode*** *is set to either,* `128 kbits/s` *or* `IEEE C37.94`*. When the* ***Comms Mode*** *is set to* `IEEE C37.94`*,* ***Ch1 N*64 kbits/s*** *and* ***Ch2 N*64 kbits/s*** *settings are available and should be set to a minimum of* `2`*.*

This Chain topology (normally invoked when a communication link fails) can be used to save cost in a three-terminal scheme. This is because two legs are cheaper to install than full triangulation implementation. Also if a suitable communication link is not available between two of the line ends, it may be the only option. If a Chain topology is used, or one link in a fully triangulated scheme is lost, the operating delay of the teleprotection commands increases by approximately 7 ms, plus the communications channel signalling delay, due to the extended path length and additional processing.

22.3.1.6 PHYSICAL CONNECTION

The protection communications into and out of the products are fibre-optic. Connections are made using BFOC/2.5 connectors (BFOC/2.5 connectors are commonly referred to as “ST” connectors where “ST” is a registered trademark of AT&T).

According to application, different fibre-optic interfaces are available described in the following table:

Wavelength of Light (nm)	Fibre Type	Maximum Transmission Distance (km)
850	Multi-mode	1
1300	Multi-mode	50
1300	Single-mode	100
1550	Single-mode	130

Connections are made using appropriate fibre-optic cables terminated with BFOC/2.5 connectors. The transmitter of one device (for example Tx1) is connected to the receiver of another (Rx1 or Rx2 according to the scheme set-up)

Products can be supplied with the following fibre-optic channel arrangements:

Ch 1	Ch2
850 nm	850 nm
1300 nm multi-mode	Not fitted
1300 nm multi-mode	1300 nm multi-mode
1300 nm single-mode	Not fitted
1300 nm single-mode	1300 nm single-mode
1550 nm single-mode	Not fitted
1550 nm single-mode	1550 nm single-mode
850 nm	1300 nm multi-mode
850 nm	1300 nm single-mode
850 nm	1550 nm single-mode
1300 nm multi-mode	850 nm
1300 nm single-mode	850 nm
1550 nm single-mode	850 nm

22.3.1.6.1 DIRECT CONNECTION

If you are using direct fibre connections you need to set the ***Scheme Setup*** settings and you are advised to change the ***Address*** setting from the default. You find these settings in the PROT *COMMS/IM64* columns. You should not need to use any of the other settings that would be applicable if using shared links and/or interfacing units.

22.3.1.6.2 INDIRECT CONNECTION

For 850nm communications links where the connection is not direct fibre, a number of options are available to interface with standard telecommunications equipment. These are:

- Fibre connection to telecommunications equipment supporting the IEEE C37.94 interface
- Connection to G.703, V.35 or X.21 electrical circuits using auxiliary P59x interface units

P59x interface unit options are:

- P591 - Fiber optic proprietary relay protocol or IEEE C37.94 (1 to 12 x 64kbps channels auto configurable), depending on ordering option to electrical signal G.703 (co-directional) (64 Kbit/s or 2 Mbit/s, depending on ordering option)
- P592 - Fiber optic to electrical signal V.35
- P593 - Fiber optic proprietary relay protocol or IEEE C37.94 (12 x 64kbps channels only), depending on ordering option to electrical signal X.21 (64 Kbit/s or 768kbps, depending on ordering option)

Note:
*When the relay is set to 32bit InterMiCOM64 application mode (**Extended IM64** setting `Enabled`), the relay is not compatible with P592. Please contact GE Vernova for G.703, V.35 or X.21 electrical circuit converter.*

P59x interface units are housed in 10TE wide, 4U high cases. They provide optical-electrical conversion. The optical characteristics match those of the 850nm interface on the protection device. When used, you need one unit for each transmitter/receiver pair. That means one unit at each end of each communications channel as demonstrated in the figure below.

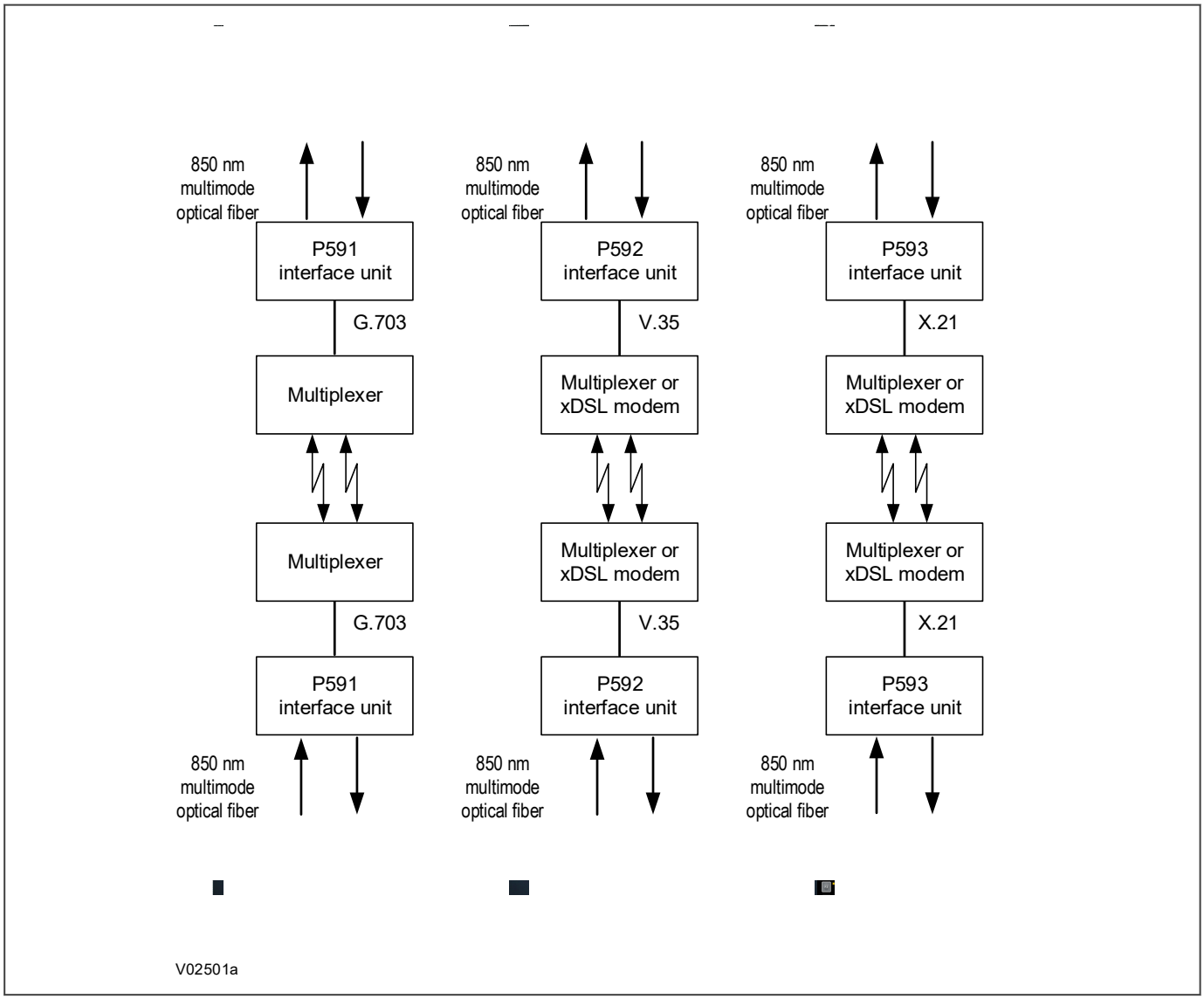


Figure 401: Interfacing to PCM multiplexers

Note:
P59x interface units should be mounted as close as possible to the telecommunications equipment to minimise interference on the electrical connections.

22.3.1.6.2.1 INDIRECT CONNECTION - FIBRE (IEEE C37.94)

An 850 nm fibre-optic interface can connect directly to a multiplexer supporting the IEEE C37.94 standard. 850 nm multi-mode optical fibres, either 50/125 μm or 62.5/125 μm are suitable. BFOC/2.5 type fibre optic connectors are used.

Note:
To use this configuration, you need to set ***Comms Mode*** *to 'IEEE C37.94'. You then need to remove the power supply from the product and then re-apply the power. The setting is now effective. If 'IEEE C37.94' is used, it applies to both communication channels.*

The IEEE C37.94 standard defines an N*64 kbits/s selection, where N is a number between 1 and 12 and selects the channel used in the multiplexer. The value of N is set on a per channel basis by setting ***Ch1 N*64kbits/s*** (and ***Ch2 N*64kbits/s*** where applicable) to N (1 to 12). For convenience an auto-detect setting is provided, if using the ***Extended IM64*** mode, and therefore 128Kb/s, then a minimum of 2 slots will need to be configured. Setting to `Auto` means that the device will automatically determine which multiplexer channel to use.

22.3.1.6.2.2 INDIRECT CONNECTION - ELECTRICAL CIRCUITS

P591, P592, P593 interface units are housed in 10TE wide, 4U high cases. They provide optical-electrical conversion allowing the protection to be used with telecommunications equipment providing interfaces to the ITU-T recommendations G,703, V.35 and X.21 respectively. The optical characteristics of the P59x devices match those of the 850 nm interface on the protection device. When used, you need one unit for each transmitter/receiver pair. That means one unit at each end of each communications channel. The P59x devices should be mounted as close as possible to the telecommunications equipment to minimise interference on the electrical connections.

A detailed description of the devices can be found in the P59x Technical Manual.

The P59x range supports the following electrical connections:

- X.21: Connection at 64 kbps or C37.94 is supported.
- V.35: Connection at 64 kbps or 56 kbps is supported.
- G.703: The data rate (baud rate) is 64 kbps or C37.94 up to 12 x 64 kbps, but connection can be made at either 64 kbps or 2 Mbps.

When P59x units are used in the communications channel of the protection scheme, the following must be set:

- Comms Mode
- Baud Rate Chn (n = 1 or 2)
- Clock Source Chn (n = 1 or 2)

You should set the Comms Mode setting to S`tandard` or `C37.94`, and you should match the Baud Rate to the channel data rate.

For V.35, you should set the Clock Source to `External` for a multiplexer network which is supplying a master clock signal, or to `Internal` for a multiplexer network recovering signal timing from the equipment (clock recovery). For G.703 and X.21, you always set the clock source to E`xternal`.

Note:
When you are using C37.94 between the IED and the P591, you must set one of the converters as a master and the other as a slave.

22.3.2 COMMUNICATIONS SUPERVISION

Since electrical power systems are generally required to operate continuously, it follows that the applied protection must do the same. If the protection uses communications, it must supervise these communications to take appropriate action should they become degraded or lost.

IM64 provides the necessary communications supervision.

There are seven settings associated with the IM64 protection signalling communications supervision which are listed below and described in the settings table:

- Comm Fail Timer
- Comm Fail Mode
- Channel Timeout
- IM Msg Alarm Lvl
- Prop Delay Stats
- MaxCh 1 PropDelay
- MaxCh 2 PropDelay

A communication alarm is raised if the message error rate exceeds the ***IM Msg Alarm Lvl*** setting and persists for the period defined by the ***Comm Fail Timer*** setting. Using the default settings will raise an alarm for a persistent Bit Error Rate (BER) of 1.5 x 10 –3.

The alarm will be apparent at the receiving device, which will reflect the alarm back to the transmitting device.

Note:
*The **Comm Fail Mode** setting applies only to devices configured for dual redundant or three-terminal configuration. It defines what combination of failures on the two communications channels is used to indicate an alarm.*

Note:
*The **MaxCh1 PropDelay** and **MaxCh2 PropDelay** settings for Channel 1 (and Channel 2 if fitted) are only visible if the **Prop Delay Stats** setting is `Enabled`.*

22.3.3 IM64 SELECT 8 OR 32 BITS PER CHANNEL

To enable IM64 32 bits per channel, the devices's data rate must be increased from 64/56Kbps to 128Kbps. To maintain backward compatibility with previous software versions, the data rate will be selectable via the *PROT COMMS/IM64* column ***Comms Mode*** setting, which includes `128Kbits/s` in addition to `Standard` and `IEEE C37.94` options.

If the ***Comms Mode*** setting is set to `128Kbits/s` or `IEEE C37.94` then the option to set IM64 to 8 or 32 bits per channel (via the ***Extended IM64*** setting in the *PROT COMMS/IM64* column) will be available.

If IM64 is configured to 32 bits (***Extended IM64*** set to `Enabled`) and the ***Comms Mode*** set to `IEEE C37.94`, then the minimum number of comms channels used will be 2.

Extended IM64 input and output signal names (from ***IM64 Ch1Input 9****/***IM64 Ch2Input 9**** and ***IM64 Ch1Output 9****/***IM64 Ch2Output 9**** onward) are denoted by a trailing asterisk.

If the ***Comms Mode*** is set to `Standard` or `IEEE C37.94` and IM64 is configured to 8 bits (***Extended IM64*** set to `Disabled`), the previous software version behaviour will be unchanged.

If only one slot is configured and the ***Comms Mode*** is set to `IEEE C37.94`, then IM64 cannot be set to 32 bits (***Extended IM64*** cannot be set to `Enabled`).

When the ***Comms Mode*** is set to `IEEE C37.94`, ***Ch 1 N*64kbits/s*** or ***Ch 2 N*64kbits/s*** set to `AUTO` and IM64 is set to 32 bits (***Extended IM64*** set to `Enabled`), then a request from the multiplexer for the use of a slot will trigger a ***Ch1 Mismatch RxN*** or ***Ch2 Mismatch RxN*** flag and the request will be ignored.

Note:
*The comms message format is not backwards compatible if the **Comms Mode** is `128Kbps` or `IEEE C37.94` and IM64 is configured to 32 bits (**Extended IM64** set to `Enabled`).*

Note:
*All devices in a scheme must be capable of **Extended IM64** operation.*

The ***Invalid Mesg Fmt*** alarm and the ***IM64 SchemeFail*** alarm will activate if the received comms message is not of the correct format and data rate.

Once the new comms configuration has been set, an alarm ***Comms Changed*** will be active to prompt the user to reboot the relay. Once rebooted, the changed comms configuration will be active.

22.4 IM64 LOGIC

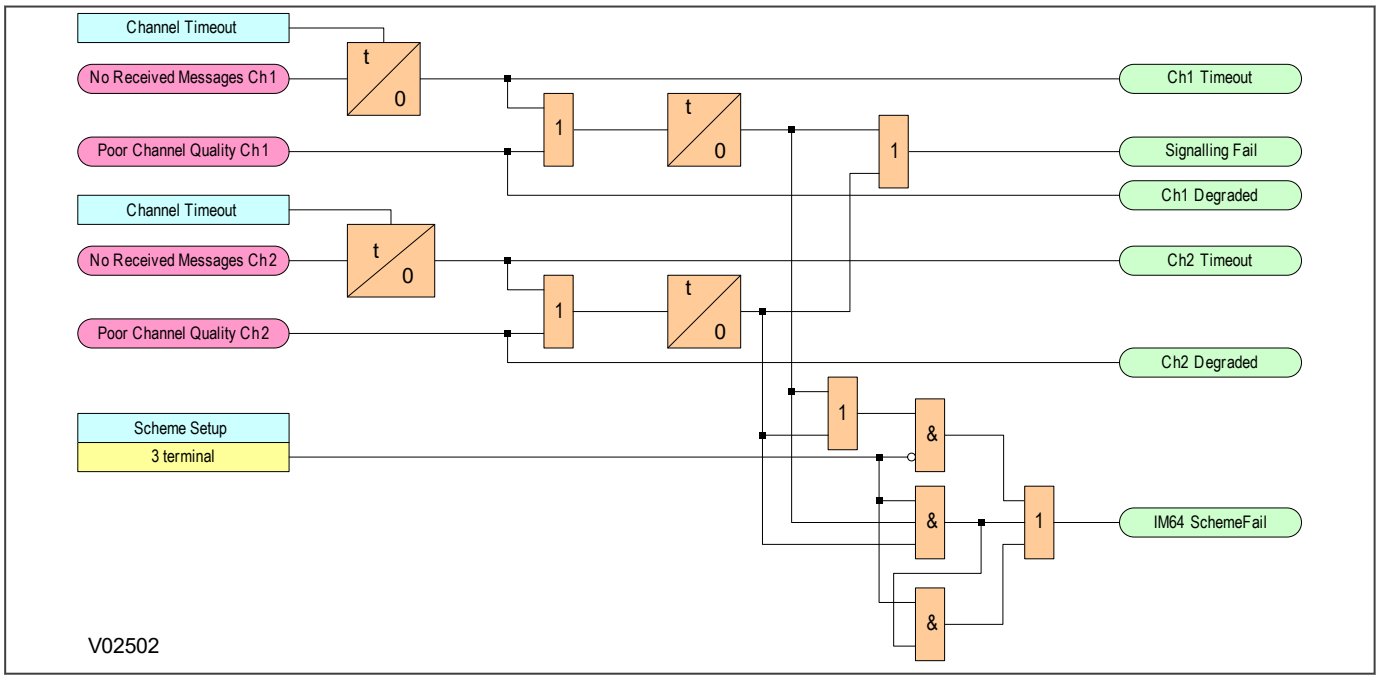


Figure 402: IM64 channel fail and scheme fail logic

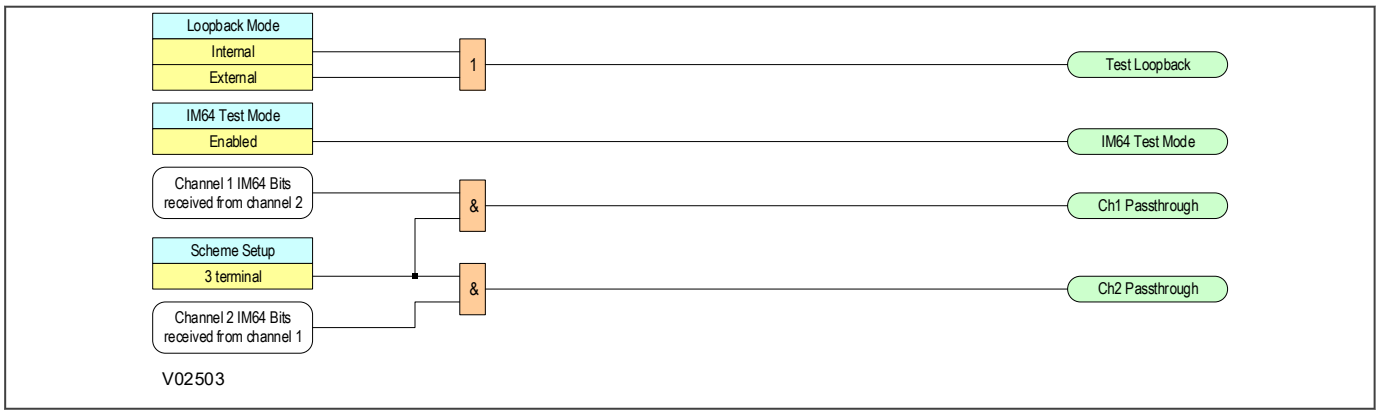


Figure 403: IM64 general alarm signals logic

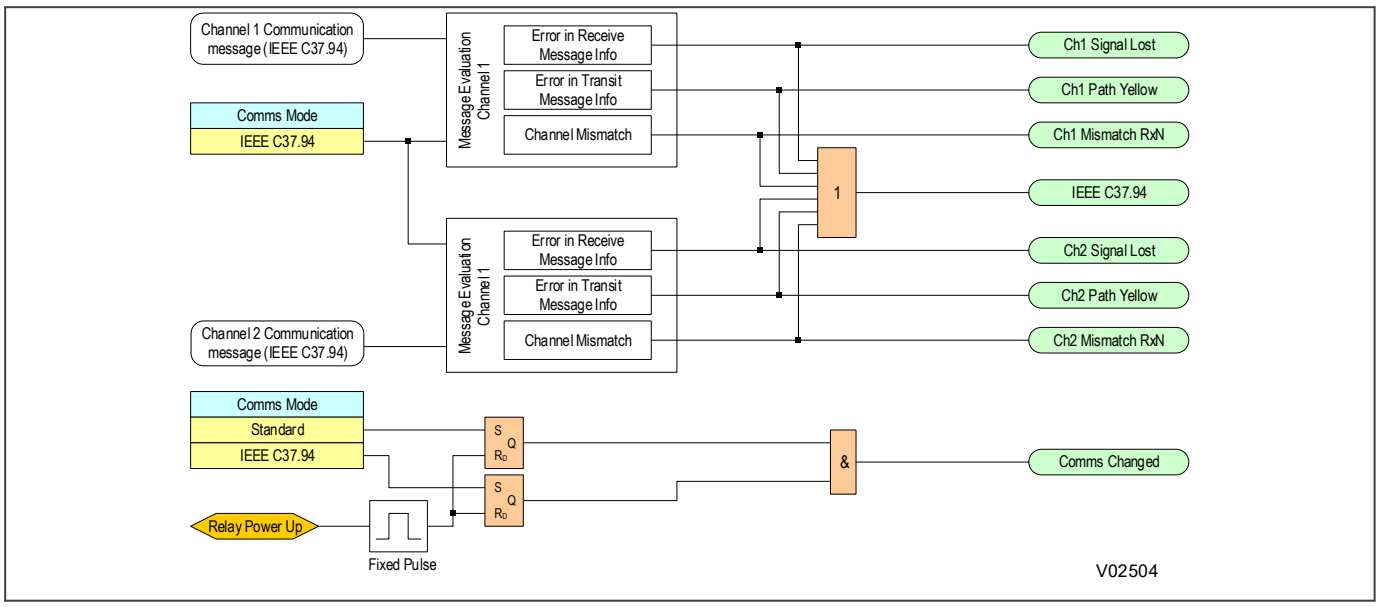


Figure 404: IM64 communications mode and IEEE C37.94 alarm signals

22.5 APPLICATION NOTES

Effective communications are essential for the performance of teleprotection schemes. Disturbances on the communications links need to be detected and reported so that appropriate actions can be taken to ensure that the power system does not go unprotected.

22.5.1 ALARM MANAGEMENT

Due to the criticality of IM64 communications for correct scheme performance, there is an extensive regime to monitor signal quality and integrity, generate and report alarms. For most applications, the alarm management provided as standard will satisfy the needs of the scheme.

For some applications, it may be necessary customise the alarm management. You can do this with the programmable scheme logic. This section provides a detailed explanation the communications alarm signals integrated in this product.

22.5.2 ALARM LOGIC

The figures in the logic diagram section show the main alarm DDB signals associated with IM64. Some of the signals are setting or hardware dependent. For example, Channel 2 alarms are not available on a simple two-terminal single communications link application. This section explains the logic, allowing you to understand how you might customise the alarm logic for your application.

The messages received on each channel are individually assessed for quality to ensure the IM64 signalling scheme is available for use. If no messages are received for a period equal to the ***Channel Timeout*** setting or the signal quality falls below a defined value, DDB signals are activated as shown in the IM64 channel fail and scheme fail logic diagram.

Poor quality is indicated if the percentage of incomplete messages exceeds the ***IM Msg Alarm Lvl*** setting in a 100 ms period (rolling window), or if the communications propagation time of the IM64 message exceeds the ***Max Ch PropDelay*** (assuming the ***Prop Delay Stats*** setting is `Enabled`), or if (in IEEE C37.94 configuration only, and not shown on the diagram) the ***Ch Mux Clk*** flag has been raised to indicate an incorrect baud rate.

If either the ***Ch Timeout*** or the ***Ch Degraded*** signal persists in the alarmed state for more than the duration of the ***Comm Fail Timer*** setting, according to the conditions set in the Comm Fail Mode setting, the ***Signalling Fail*** signal is raised.

For two-ended schemes (including dual redundant schemes), the ***IM64 SchemeFail*** signal is generated at the same time as the ***Signalling Fail*** signal. However, for three-terminal applications, the ***IM64 SchemeFail*** signal indicates that the full set of signalling bits cannot be processed by the scheme. Due to the self-healing nature of the three-terminal application, this occurs when both channels at any one terminal are not receiving valid signals. This condition generates a flag in the IM64 message structure which is passed to both remote ends, as well as generating the local ***IM64 SchemeFail*** signal. Using this method, in three-terminal applications the scheme fail indication is raised at all three ends.

The scheme fail signalling is generated by the inability of a device to receive messages through communication failure. The transmitting device only knows that communication to a remote device has failed if it receives notification from the remote device. If a device in the scheme is put into test mode, the communication failure information is not passed on to the remote ends. If the communications failure is bidirectional, there will be no indication at the remote device. If this causes operational issues, it may be necessary to include other signals to enable more precise indication of scheme failure.

In addition to the main IM64 channel fail and scheme fail conceptual logic, there are number of additional alarm DDB signals associated with test modes, reconfiguration for 3-terminal schemes, and the communication mode (‘Standard’ or ‘IEEE C37.94’) shown in the logic diagrams.

The majority of signals are associated with the ‘IEEE C37.94’ communications mode and are not activated if the `Standard` communication mode is selected. The ***Comms Changed*** DDB logic is to show that switching between the different communication modes requires a power cycle to be performed before the change is activated.

22.5.3 TWO-ENDED SCHEME EXTENDED SUPERVISION

For two-terminal applications, the ***Signalling Fail*** and ***IM64 SchemeFail*** signals operate together. As such, the basic indications available on each device should be considered as local-terminal indications only. If remote indication is needed to assure scheme functionality, it is necessary to use additional signals to communicate the status to the remote end. One method of performing this is shown below:

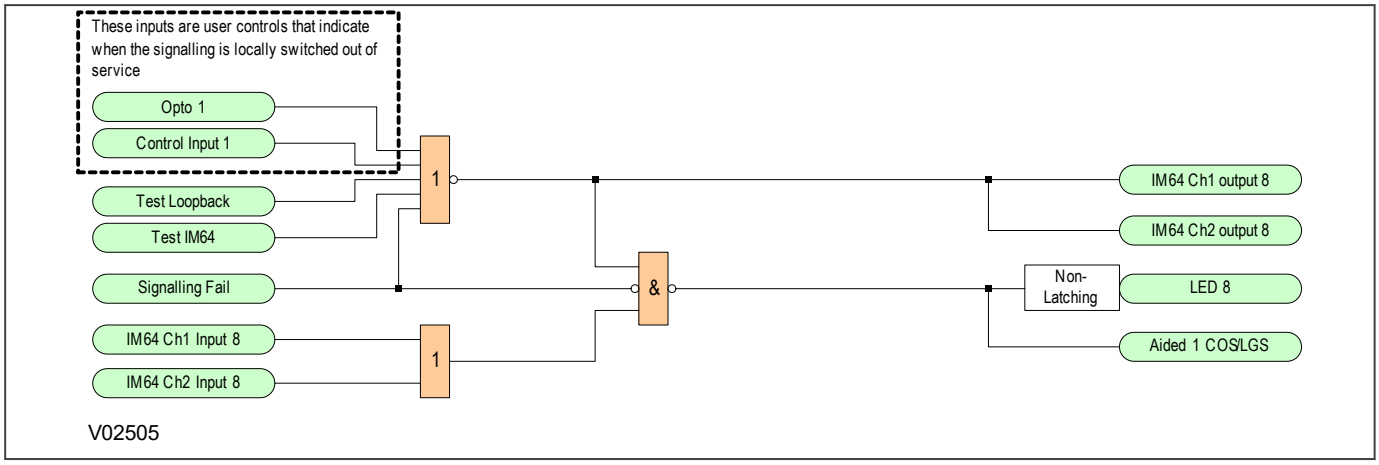


Figure 405: IM64 two-terminal scheme extended supervision

In this example scheme, several signals are used to permanently pass an IM64 signal to the remote terminal. These signals take account of the local ability to receive IM64 messages, local test/loopback modes and any other external methods of switching the signalling scheme out of service. If any of these driving signals are energised, the IM64 message is reset (a “0” sent on IM64 bit 8--or bit 32 if ***Extended IM64*** mode is `Enabled`). This causes both ends to raise an alarm (LED 8 in the example) or switch the aided scheme out of service due to loss of channel.

This is intended only as an example. You may need to customise it for your application requirements.

22.5.4 THREE-ENDED SCHEME EXTENDED SUPERVISION

The example for an IM64 two-terminal scheme above can be used for three-terminal applications. However for three-terminal applications, the ***IM64 SchemeFail*** signal that is automatically communicated to all ends of the scheme is used rather than the ***Signalling Fail*** signal.

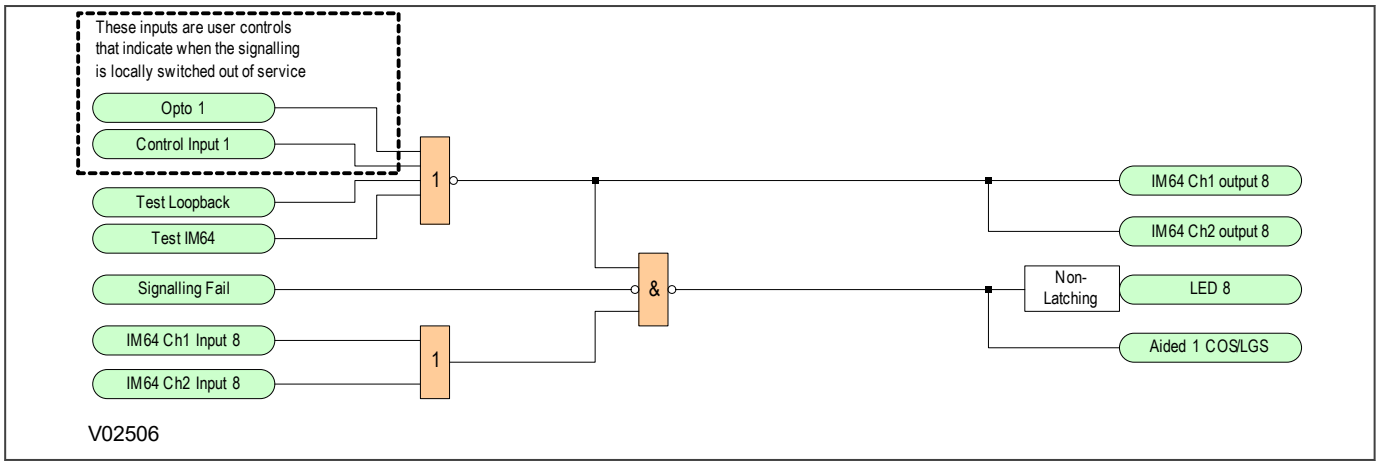


Figure 406: IM64 three-terminal scheme extended supervision

In this example if both channels at any one terminal fail to receive information, this is communicated to the other terminals. An alarm is raised and the aided scheme is switched out of service. The example given above, also takes

into account the test modes and local switching, so the scheme is signalled out of service at all terminals if one terminal is locally disabled.

The logic presented above is intended only as an example. You may need to customise it for your application requirements.

CHAPTER 23

ELECTRICAL TELEPROTECTION

23.1 CHAPTER OVERVIEW

This chapter contains the following sections:

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Introduction 654
Teleprotection Scheme Principles 655
Implementation 656
Configuration 657
Connecting to Electrical InterMiCOM 659
Application Notes 660

23.2 INTRODUCTION

Electrical Teleprotection is an optional feature that uses communications links to create protection schemes. It can be used to replace hard wiring between dedicated relay output contacts and digital input circuits. Two products equipped with electrical teleprotection can connect and exchange commands using a communication link. It is typically used to implement teleprotection schemes.

Using full duplex communications, eight binary command signals can be sent in each direction between connected products. The communication connection complies with the EIA(RS)232 standard. Ports may be connected directly, or using modems. Alternatively EIA(RS)232 converters can be used for connecting to other media such as optical fibres.

Communications statistics and diagnostics enable you to monitor the integrity of the communications link, and a loopback feature is available to help with testing.

23.3 TELEPROTECTION SCHEME PRINCIPLES

Teleprotection schemes use signalling to convey a trip command to remote circuit breakers to isolate circuits. Three types of teleprotection commands are commonly encountered:

- Direct Tripping
- Permissive Tripping
- Blocking Scheme

23.3.1 DIRECT TRIPPING

In direct tripping applications (often described by the generic term: “intertripping”), teleprotection signals are sent directly to a master trip device. Receipt of a command causes circuit breaker operation without any further qualification. Communication must be reliable and secure because any signal detected at the receiving end causes a trip of the circuit at that end. The communications system must be designed so that interference on the communication circuit does not cause spurious trips. If a spurious trip occurs, the primary system might be unnecessarily isolated.

23.3.2 PERMISSIVE TRIPPING

Permissive trip commands are monitored by a protection device. The circuit breaker is tripped when receipt of the command coincides with a ‘start’ condition being detected by the protection at the receiving. Requirements for the communications channel are less onerous than for direct tripping schemes, since receipt of an incorrect signal must coincide with a ‘start’ of the receiving end protection for a trip operation to take place. Permissive tripping is used to speed up tripping for faults occurring within a protected zone.

23.4 IMPLEMENTATION

Electrical InterMiCOM is configured using a combination of settings in the *INTERMICOM COMMS* column, settings in the *INTERMICOM CONF* column, and the programmable scheme logic (PSL).

The eight command signals are mapped to DDB signals within the product using the PSL.

Signals being sent to a remote terminal are referenced in the PSL as ***IM Output 1*** - ***IM Output 8***. Signals received from the remote terminal are referenced as ***IM Input 1*** - ***IM Input 8***.

Note:
As well as the optional Modem InterMiCOM, some products are available with a feature called InterMiCOM64 (IM64). The functionality and assignment of commands in InterMiCOM and InterMiCOM64 are similar, but they act independently and are configured independently.

23.5 CONFIGURATION

Electrical Teleprotection is compliant with IEC 60834-1:1999. For your application, you can customise individual command signals to the differing requirements of security, speed, and dependability as defined in this standard.

You customise the command signals using the ***IM# Cmd Type*** cell in the *INTERMICOM CONF* column.

Any command signal can be configured for:

- Direct intertripping by selecting 'Direct'. (this is the most secure signalling but incurs a time delay to deliver the security).
- Blocking applications by selecting 'Blocking'. (this is the fastest signalling)
- Permissive intertripping applications by selecting 'Permissive. (this is dependable signalling that balances speed and security)

You can also select to 'Disable' the command.

> *Note:*
> *When used in the context of a setting, '#' specifies which command signal (1-8) bit is being configured.*

To ensure that command signals are processed only by their intended recipient, the command signals are packaged into a message (sometimes referred to as a telegram) which contains an address field. A sending device sets a pattern in this field. A receiving device must be set to match this pattern in the address field before the commands will be acted upon. 10 patterns have been carefully chosen for maximum security. You need to choose which ones to use, and set them using the ***Source Address*** and ***Receive Address*** cells in the *INTERMICOM COMMS* column.

The value set in the ***Source Address*** of the transmitting device should match that set in the ***Receive Address*** of the receiving device. For example set ***Source Address*** to `1` at a local terminal and set ***Receive Address*** to `1` at the remote terminal.

The Source Address and Receive Address settings in the device should be set to different values to avoid false operation under inadvertent loopback conditions.

Where more than one pair of devices is likely to share a communication link, you should set each pair to use a different pair of address values.

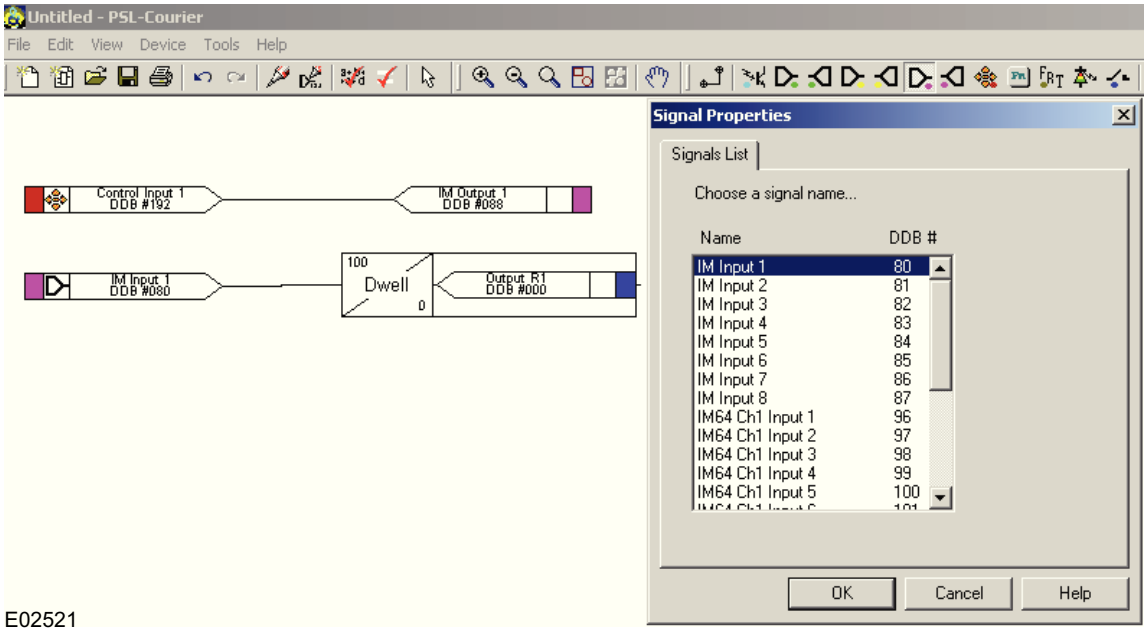
Electrical InterMiCOM has been designed to be resilient to noise on communications links, but during severe noise conditions, the communication may fail. If this is the case, an alarm is raised and you can choose how the input signals are managed using the ***IM# FallBackMode*** cell in the *INTERMICOM CONF* column:

• If you choose `Latched`, the last valid command to be received can be maintained until a new valid message is received.

• If you choose `Default`, the signal will revert to a default value after the period defined in the ***IM# FrameSyncTim*** setting has expired. You choose the default value using the ***IM# DefaultValue*** setting.

Subsequent receipt of a full valid message will reset the alarm, and the new command signals will be used.

As well as the settings described above, you will need to assign input and output signals in the Programmable Scheme Logic (PSL). Use the 'Integral Tripping' buttons to create the logic you want to apply. A typical example is shown below.



E02521

Figure 407: Example assignment of InterMiCOM signals within the PSL

Note:
When an Electrical InterMiCOM signal is sent from a local terminal, only the remote terminal will react to the command. The local terminal will only react to commands initiated at the remote terminal.

23.6 CONNECTING TO ELECTRICAL INTERMICOM

Electrical InterMiCOM uses EIA(RS)232 communication presented on a 9-pin 'D' type connector. The connector is labelled SK5 and is located at the bottom of the 2nd Rear communication board. The port is configured as standard DTE (Data Terminating Equipment).

23.6.1 SHORT DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is not a problem, direct connection between devices is possible. For this case, inter-device connections should be made as shown below the figure below.

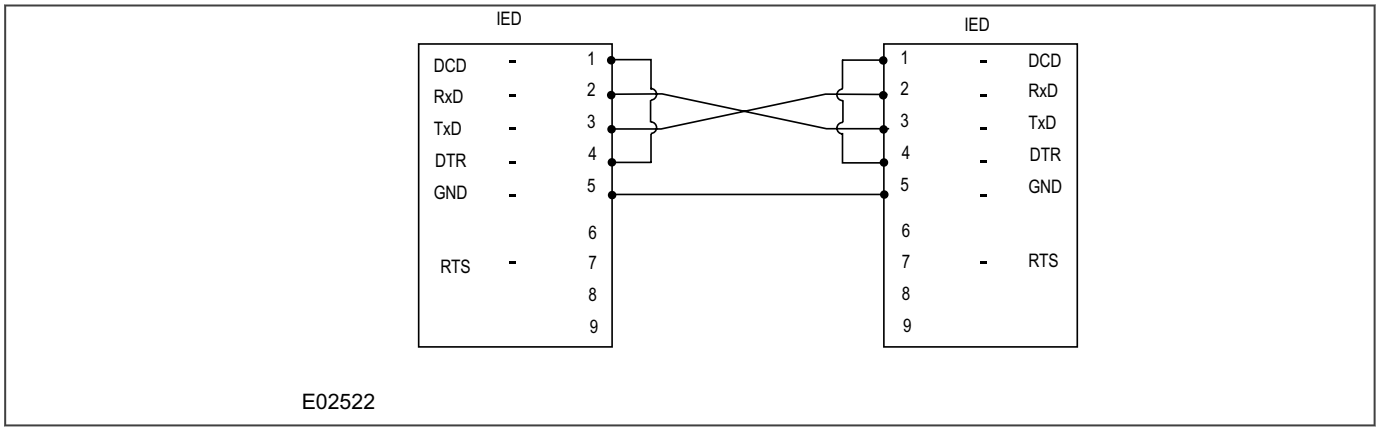


Figure 408: Direct connection

For direct connection, the maximum baud rate can generally be used.

23.6.2 LONG DISTANCE

EIA(RS)232 is suitable for short distance connections only - less than 15m. Where this limitation is a problem, direct connection between devices is not possible. For this case, inter-device connections should be made as shown below the figure below.

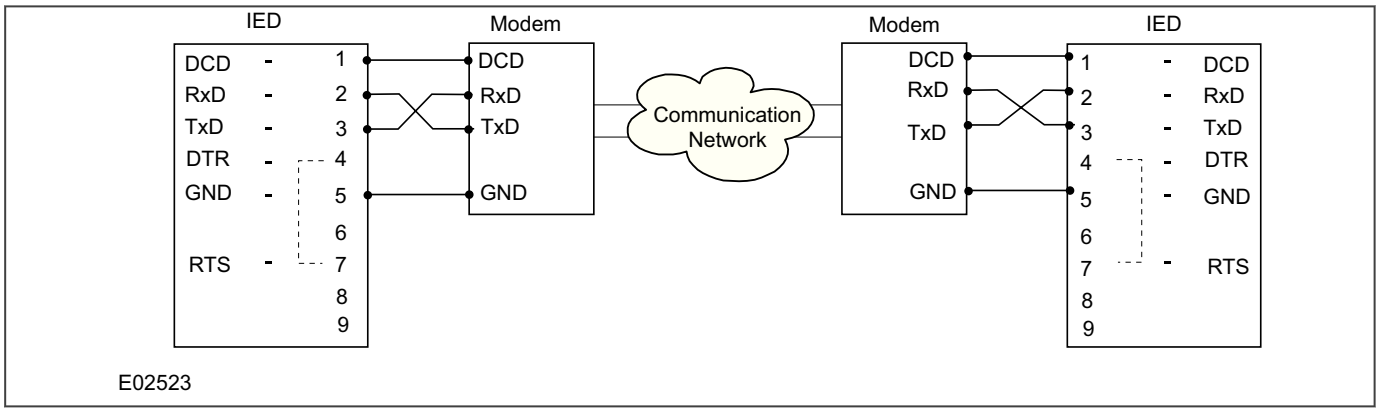


Figure 409: Indirect connection using modems

This type of connection should be used when connecting to devices that have the ability to control the DCD line. The baud rate should be chosen to be suitable for the communications network. If the Modem does not support the DCD function, the DCD terminal on the IED should be connected to the DTR terminal.

23.7 APPLICATION NOTES

Electrical InterMiCOM settings are contained within two columns; *INTERMICOM COMMS* and *INTERMICOM CONF*. The *INTERMICOM COMMS* column contains all the settings needed to configure the communications, as well as the channel statistics and diagnostic facilities. The *INTERMICOM CONF* column sets the mode of each command signal and defines how they operate in case of signalling failure.

Short metallic direct connections and connections using fire-optic converters will generally be set to have the highest signalling speed of 19200b/s. Due to this high signalling rate, the difference in operating time between the direct, permissive, and blocking type signals is small. This means you can select the most secure signalling command type ('Direct' intertrip) for all commands. You do this with the ***IM# Cmd Type*** settings. For these applications you should set the ***IM# Fallback Mode*** to `Default`. You should also set a minimal intentional delay by setting ***IM# FrameSyncTim*** to 10 msecs. This ensures that whenever two consecutive corrupt messages are received, the command will immediately revert to the default value until a new valid message is received.

For applications that use Modem and/or multiplexed connections, the trade-off between speed, security, and dependability is more critical. Choosing the fastest baud rate (data rate) to achieve maximum speed may appear attractive, but this is likely to increase the cost of the telecommunications equipment. Also, telecommunication services operating at high data rates are more prone to interference and suffer from longer re-synchronisation times following periods of disruption. Taking into account these factors we recommend a maximum baud rate setting of 9600 bps. As baud rates decrease, communications become more robust with fewer interruptions, but overall signalling times increase.

At slower baud rates, the choice of signalling mode becomes significant. You should also consider what happens during periods of noise when message structure and content can be lost.

- In 'Blocking' mode, the likelihood of receiving a command in a noisy environment is high. In this case, we recommend you set ***IM# Fallback Mode*** to `Default`, with a reasonably long ***IM# FrameSyncTim*** setting. Set ***IM# DefaultValue*** to '1'. This provides a substitute for a received blocking signal, applying a failsafe for blocking schemes.
- In 'Direct' mode, the likelihood of receiving commands in a noisy environment is small. In this case, we recommend you set ***IM# Fallback Mode*** to `Default` with a short ***IM# FrameSyncTim*** setting. Set ***IM# DefaultValue*** to '0'. This means that if a corrupt message is received, InterMiCOM will use the default value. This provides a substitute for the intertrip signal not being received, applying a failsafe for direct intertripping schemes.
- In 'Permissive' mode, the likelihood of receiving a valid command under noisy communications conditions is somwhere between that of the 'Blocking' mode and the 'Direct' intertrip mode. In this case, we recommended you set ***IM# Fallback Mode*** to `Latched`.

The table below presents recommended ***IM# FrameSyncTim*** settings for the different signalling modes and baud rates:

	Minimum Recommended "IM# FrameSyncTim" Setting			
Baud Rate	Direct Intertrip Mode	Blocking Mode	Minimum Setting (ms)	Maximum Setting (ms)
600	100	250	100	1500
1200	50	130	50	1500
2400	30	70	30	1500
4800	20	40	20	1500
9600	10	20	10	1500
19200	10	10	10	1500

Note:
As we have recommended Latched operation, the table does not contain recommendations for 'Permissive' mode. However, if you do select 'Default' mode, you should set ***IM# FrameSyncTim*** *greater than those listed above. If you set* ***IM# FrameSyncTim*** *lower than the minimum setting listed above, the device could interpret a valid change in a message as a corrupted message.*

We recommend a setting of 25% for the communications failure alarm.

CHAPTER 24

COMMUNICATIONS

24.1 CHAPTER OVERVIEW

This product supports Substation Automation System (SAS), and Supervisory Control and Data Acquisition (SCADA) communication through multiple interfaces and a choice of data protocols.

All products support rugged serial communications for SCADA and SAS applications. Optionally, any product can support Ethernet communications for IEC 61850, cyber security and remote access, either through a single port or industry-standard redundant ports.

This chapter contains the following sections:

Chapter Overview 663
Communication Interfaces 664
Serial Communication 665
Ethernet Communication 668
Ethernet Board Versions 669
Board Connections 670
Ethernet Configuration 672
Redundancy Protocols 674
Secure Shell (SSH) Communication 679
Simple Network Management Protocol (SNMP) 681
Data Protocols 687
Time Synchronisation 716

24.2 COMMUNICATION INTERFACES

The products have a number of standard and optional communication interfaces. The standard and optional hardware and protocols are summarised below:

Port	Availability	Physical Interface	Use	Data Protocols
Front	Standard	USB Type B	Local settings	Courier
Rear Port 1 (RP1 copper)	Standard	RS232/RS485/K-Bus	SCADA Remote settings	Courier, IEC 60870-5-103, DNP3.0
Rear Port 1 (RP1 fibre)	Optional	Fibre	SCADA Remote settings	Courier, IEC 60870-5-103, DNP3.0
Rear Port 2 (RP2)	Optional	RS232/RS485/K-Bus	SCADA Remote settings	SK4: Courier only SK5: InterMiCOM only
Ethernet	Optional	Ethernet	IEC 61850 Time sync Remote access	IEC 61850, Courier Tunnel, RADIUS, Syslog, SNMP, PTP, SNTP

Note:
Optional communications boards are always fitted into slot A. It is only possible to fit one optional communications board, therefore RP2 and Ethernet communications are mutually exclusive, except for ZN0098005, where both Ethernet and serial protocols are supported.
On RP1, any one of the data protocols can be selected at one time, from the COMMUNICATIONS Menu (it is no longer necessary to select one as a product order option).

24.3 SERIAL COMMUNICATION

The physical layer standards that are used for serial communications for SCADA purposes are:

- EIA(RS)485 (often abbreviated to RS485)
- K-Bus (a proprietary customisation of RS485)

USB is used for local communication with the IED (for transferring settings and downloading firmware updates).

RS485 is similar to RS232 but for longer distances and it allows daisy-chaining and multi-dropping of IEDs.

K-Bus is a proprietary protocol quite similar to RS485, but it cannot be mixed on the same link as RS485. Unlike RS485, K-Bus signals applied across two terminals are not polarised.

It is important to note that these are not data protocols. They only describe the physical characteristics required for two devices to communicate with each other.

For a description of the K-Bus standard see K-Bus and GE Vernova's K-Bus interface guide reference R6509.

A full description of the RS485 is available in the published standard.

24.3.1 USB FRONT PORT

The USB interface uses the proprietary Courier protocol for local communication with the MiCOM S1 Agile settings application software.

This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate of 19200 bps, 11-bit frame (8 data bits, 1 start bit, 1 stop bit, even parity bit), and a fixed device address of '1'.

The USB interface is a Type B connector. Normally a Type A to Type B USB cable will be required to communicate between MiCOM S1 Agile and the IED.

24.3.2 EIA(RS)485 BUS

The RS485 two-wire connection provides a half-duplex, fully isolated serial connection to the IED. The connection is polarised but there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

The RS485 bus must be terminated at each end with 120 Ω 0.5 W terminating resistors between the signal wires.

The RS485 standard requires that each device be directly connected to the actual bus. Stubs and tees are forbidden. Loop bus and Star topologies are not part of the RS485 standard and are also forbidden.

Two-core screened twisted pair cable should be used. The final cable specification is dependent on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. The total cable length must not exceed 1000 m. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The RS485 signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable, then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

It may be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master is waiting in receive mode, in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequently not responding. Symptoms of this are poor response times (due to retries), increasing message error counts, erratic communications, and in the worst case, complete failure to communicate.

24.3.2.1 EIA(RS)485 BIASING REQUIREMENTS

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean to prevent noise being injected.

Note:
Some devices may be able to provide the bus bias, in which case external components would not be required.

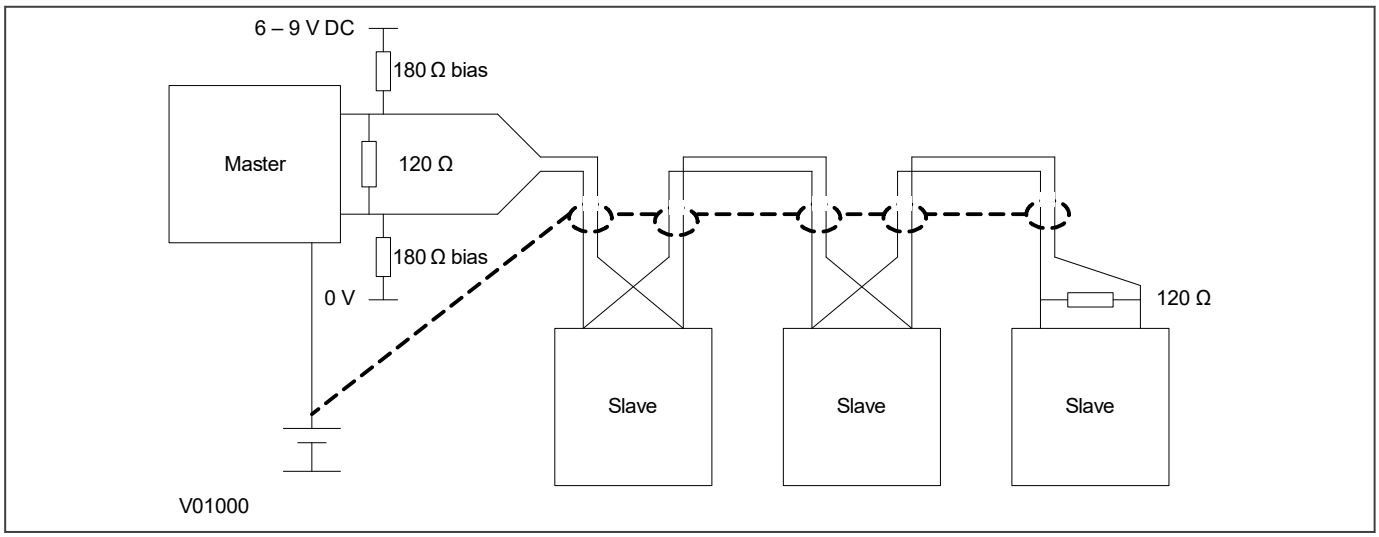


Figure 410: RS485 biasing circuit

Warning:
It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.

24.3.3 K-BUS

K-Bus is a robust signalling method based on RS485 voltage levels. K-Bus incorporates message framing, based on a 64 kbps synchronous HDLC protocol with FM0 modulation to increase speed and security.

The rear interface is used to provide a permanent connection for K-Bus, which allows multi-drop connection.

A K-Bus spur consists of up to 32 IEDs connected together in a multi-drop arrangement using twisted pair wiring. The K-Bus twisted pair connection is non-polarised.

It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. A protocol converter, namely the KITZ101 or KITZ102, must be used for this purpose. Please consult GE Vernova for information regarding the specification and supply of KITZ devices. The following figure demonstrates a typical K-Bus connection.

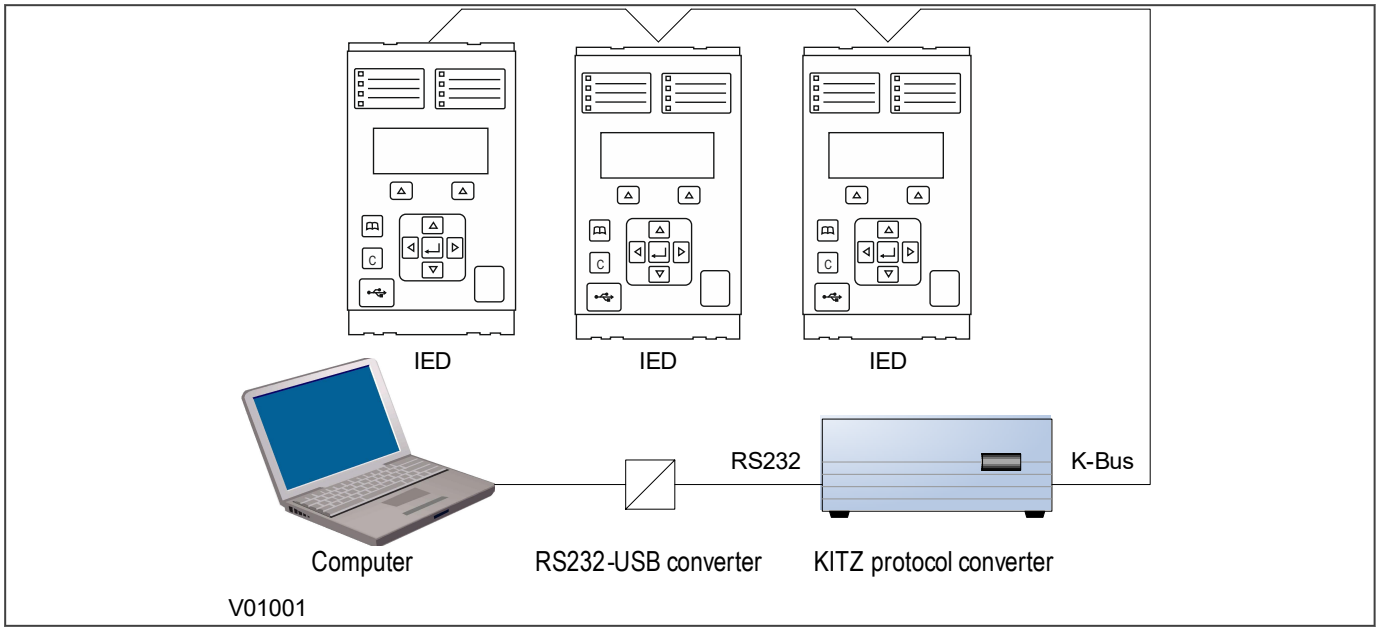


Figure 411: Remote communication using K-Bus

Note:
An RS232-USB converter is only needed if the local computer does not provide an RS232 port.

Further information about K-Bus is available in the publication R6509: K-Bus Interface Guide, which is available on request.

24.4 ETHERNET COMMUNICATION

The Ethernet interface is required for IEC 61850, and provides other Ethernet protocols including PTP, SNTP, SNMP, RADIUS authentication and syslog services, plus a universal IRIG-B time synchronisation input. It also offers communication with the settings application software for remote configuration and record extraction.

The type of Ethernet board depends on the chosen CORTEC Hardware Option. The available boards and their features are described in the Hardware Design chapter of this manual.

Fibre optic connection is recommended for use in permanent connections in a substation environment, as it offers advantages in terms of noise rejection. The fibre optic port provides 100 Mbps communication. Fibres should be suitable for 1300 nm transmission and be multimode 50/125 µm or 62.5/125 µm.

Connection can also be made to a 100Base-TX Ethernet switch using the RJ45 port.

Some P40 IEDs with later 9x software versions can support the newer Hardware Option U/W/Y Ethernet boards, in addition to the Hardware Option R/S/T Ethernet boards. Further details are provided in the Retrofit section in the Hardware Design chapter.

24.5 ETHERNET BOARD VERSIONS

Each board combines Ethernet communications, with universal IRIG-B timing functionality. There is a choice of embedded protocols for Ethernet communications, and one option that also includes support for serial protocols.

Board variants

Board	Part No.	Compatible With
One LC duplex Ethernet port with universal IRIG-B and IEEE1588 and one RJ45 Maintenance/Engineering Port	ZN0098 001	Ethernet network, no native redundancy.
Two RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/engineering port	ZN0098 002	Any PRP, HSR, RSTP or standard Ethernet network
Two LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/ engineering port	ZN0098 003	Any PRP, HSR, RSTP or standard Ethernet network
Two LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with serial fibre ST ports with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/engineering port	ZN0098 005	Any PRP, HSR, RSTP or standard Ethernet network. On the serial interface Courier, IEC 60870-5-103, DNP3

When using any of the redundant Ethernet boards on an IED, the final product will have two MAC addresses and will require two IP addresses, one for the maintenance port (NP1) for management purposes, and one for the IED station bus communications (NP2). Both of these are set using the IED Configurator tool of MiCOM S1 Agile release 3.1 or later.

All Ethernet connections are made with 1300 nm multi-mode 100BaseFx fiber optic Ethernet ports (LC connector). The boards support IEC 61850 over Ethernet.

24.6 BOARD CONNECTIONS

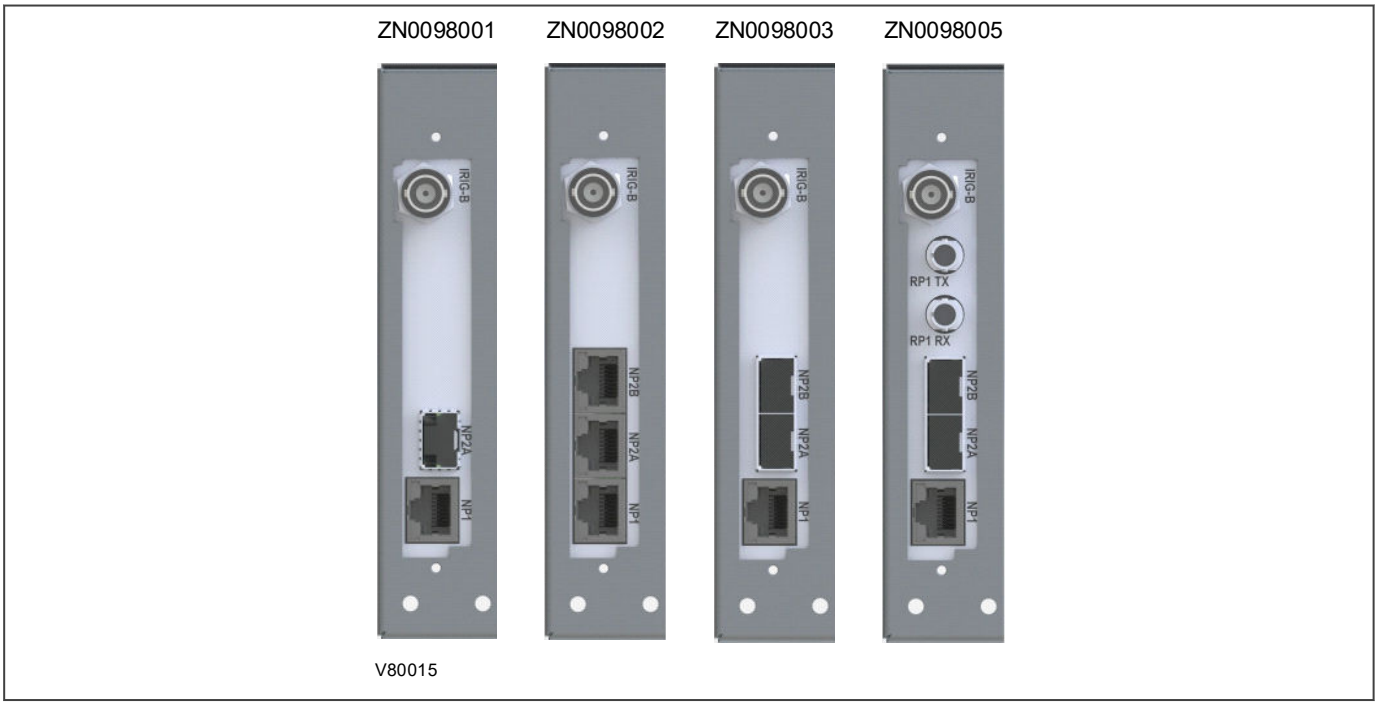


Figure 412: Board connectors

IRIG-B connector

- Centre connection: Signal
- Outer connection: Earth

RJ45 connector (NP1, NP2A and NP2B optional)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

LC optical fibre connectors (NP2A and NP2B optional)

Connector	SFP
A	TX
B	RX

Optical fibre connectors (ST only on part ZN0098005)

Connector	Serial Courier, IEC 60870-5-103, DNP3
RP1	TX
RP1	RX

24.7 ETHERNET CONFIGURATION

All configuration of Ethernet parameters and protocol services for both the monitoring/engineering port and the station bus port is done in **IED Configurator.** Any MiCOM P40 IED with an Ethernet board is required to have these parameters configured by sending an MCL file to the IED (not recommended to configure via Settings/HMI). Refer also to the MiCOM S1 Agile User Guide for additional information on configuring and sending MCL files.

The monitoring/engineering port is named "Network Port 1" and the redundant IEC 61850 station bus port is named "Network Port 2".

Network Port 1 (NP1) and Network Port 2 (NP2) have independent IP address and subnet configuration parameters, as detailed in the sub-section below. These parameters can be configured in IED Configurator, or optionally from the Front Panel UI.

The IP addresses can be in the range 0.0.0.0 to 223.255.255.255. This means it can be configured as either a Class A, B or C address.

Class	Address Range
A	0.0.0.0 to 127.255.255.255
B	128.0.0.0 to 191.255.255.255
C	192.0.0.0 to 223.255.255.255

The NP1 and NP2 IP addresses must not be configured in the same subnet.

The primary and secondary server IP addresses for RADIUS, syslog and SNMP must also be in these ranges.

24.7.1 NETWORK CONFIGURATION

To set the IP address of the monitoring/engineering port:

1. From the main window click the **Communications** section.
2. Navigate to the Network Port 1.
3. Enter the required IP address, network mask and gateway.
4. The media is not configurable for the engineering port, as they are always RJ45 copper ports.

To set the IP address of the station bus port:

1. From the main window click the **Communications** section.
2. Navigate to the Network Port 2.
3. Enter the required IP address, network mask and gateway.
4. In the Network Port 2 General configuration section, the redundancy options become available.
5. If the board supports redundancy, choose the redundant protocol desired (Failover, RSTP, PRP and HSR).
6. Each protocol has its own protocol specific settings, covered in each protocol's section.
7. The media is not configurable for the station bus port, as they are always enabled according to the ordering code. The media section is available for legacy boards only.

24.7.2 PRP CONFIGURATION

To view or configure the PRP Parameters:

1. Set the redundancy mode to **PRP**.
   - **Multicast Address:** Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
   - **Life Check Interval:** This defines how often a node sends a PRP_Supervision frame. All DANPs shall be configured with the same Life Check Interval.

24.7.3 HSR CONFIGURATION

To view or configure the HSR Parameters:

Set the redundancy mode to HSR.

- **Multicast Address:** Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
- **Life Check Interval**: This defines how often a node sends an HSR Supervision frame. All DANPs shall be configured with the same Life Check Interval.

24.7.4 RSTP CONFIGURATION

To view or configure the RSTP Parameters:

Set the redundancy mode to **RSTP**.

Parameter	Default Value (Second)	Minimum Value (Second)	Maximum Value (Second)
Bridge Max Age	20	6	40
Bridge Hello Time	2	1	10
Bridge Forward Delay	15	4	30
Bridge Priority	32768	0	61440

24.7.5 FAILOVER CONFIGURATION

To view or configure the Failover Parameters:

1. Set the redundancy mode to **Failover**.
   - Port A and Port B radio button allows to select your main port for the Failover. The name of the port in the board is also shown.
   - The Failover time defines how long it takes for the redundancy switch over to trigger. The minimum value is 2s.

24.7.6 SNTP IP ADDRESS CONFIGURATION

To configure the SNTP server IP address:

1. From the main window click the **SNTP** button.
2. The General configuration allows to set the frequency of the polling of the SNTP server. It also has a check-box **IED is a clock source** to configure the IED to be a SNTP server itself, to retransmit its date and time.
3. Under External Server 1 and 2, set the IP address of the SNTP server.

24.8 REDUNDANCY PROTOCOLS

REB variants for each of the following protocols are available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- RSTP (Rapid Spanning Tree Protocol)
- Failover

PRP and HSR are open standard, so their implementation is compatible with any standard PRP or HSR device respectively. PRP and HSR provide "bumpless" redundancy. RSTP is also an open standard, so its implementation is compatible with any standard RSTP devices. RSTP provides redundancy, however, it is not "bumpless", the standard instead utilises a loop free topology that is recalculated when a device fails and does not forward messages during recalculation.

24.8.1 PARALLEL REDUNDANCY PROTOCOL (PRP)

Power system companies have traditionally used proprietary protocols for redundant communications. This is because standardised protocols could not meet the requirements for real-time systems. Even a short loss of connectivity may result in loss of functionality.

However, Parallel Redundancy Protocol (PRP) uses the IEC 62439 standard in Dual Star Topology networks, designed for IEDs from different manufacturers to operate with each other in a substation redundant-Ethernet network. PRP provides bumpless redundancy for real-time systems and is the standard for double Star-topology networks in substations.

24.8.1.1 PRP NETWORKS

Redundant networks usually rely on the network’s ability to reconfigure if there is a failure. However, PRP uses two independent networks in parallel.

PRP implements the redundancy functions in the end nodes rather than in network elements. This is one major difference to RSTP. An end node is attached to two similar LANs of any topology which operate in parallel.

The sending node replicates each frame and transmits them over both networks. The receiving node processes the frame that arrives first and discards the duplicate. Therefore, there is no distinction between the working and backup path. The receiving node checks that all frames arrive in sequence and that frames are correctly received on both ports.

The PRP layer manages this replicate and discard function and hides the two networks from the upper layers. This scheme works without reconfiguration and switchover, so it stays available ensuring no data loss.

There should be no common point of failure between the two LANs. Therefore, they are not powered by the same source and cannot be connected directly together. They are identical in protocol at the MAC level but may differ in performance and topology. Both LANs must be on the same subnet so all IP addresses must be unique.

24.8.1.2 NETWORK ELEMENTS

A PRP compatible device has two ports that operate in parallel. Each port is connected to a separate LAN. In the IEC 62439 standard, these devices are called DANP (Doubly Attached Node running PRP). A DAN has two ports, one MAC address and one IP address.

A Single Attached Node (SAN) is a non-critical node attached to only one LAN. SANs that need to communicate with each other must be on the same LAN.

The following diagram shows an example of a PRP network. The Doubly Attached Nodes DANP 1 and DANP 2 have full node redundancy. The Singly Attached Nodes SAN 1 and SAN 4 do not have any redundancy. Singly attached nodes can be connected to both LANs using a Redundancy Box (RedBox). The RedBox converts a singly attached node into a doubly attached node. Devices such as PCs with one network board, printers, and IEDs with

one network board are singly attached nodes. A SAN behind a RedBox appears like a DAN so is called a Virtual DAN (VDAN).

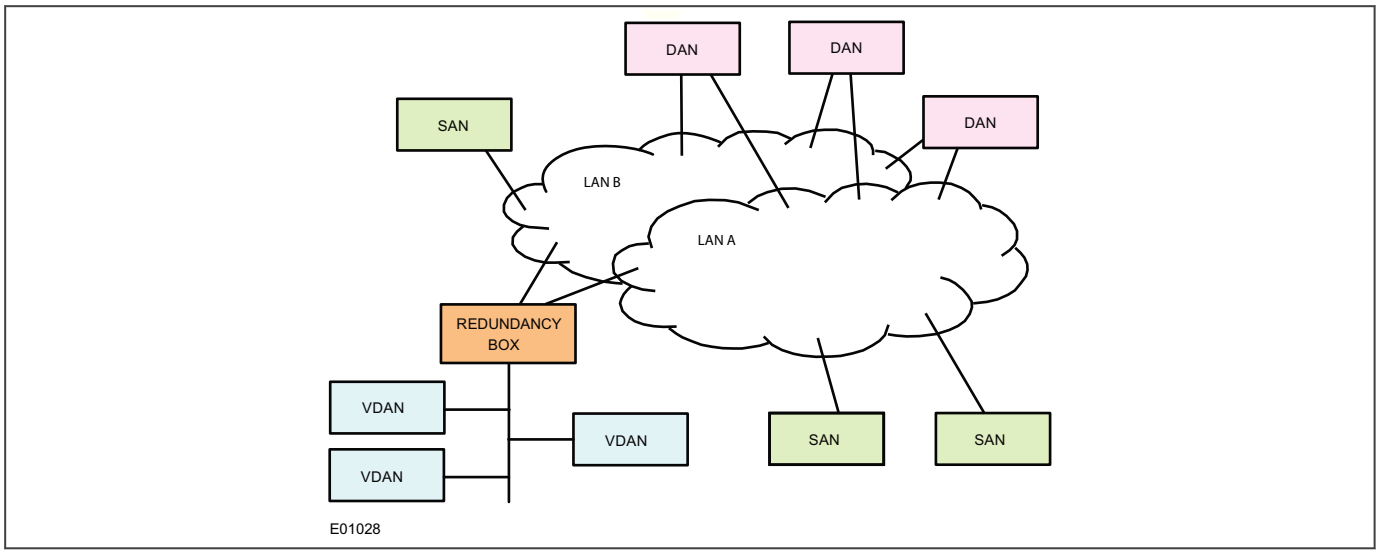


Figure 413: Example PRP redundant network

In a DAN, both ports share the same MAC address, so it does not affect the way devices talk to each other in an Ethernet network (Address Resolution Protocol at layer 2). Every data frame is seen by both ports.

When a DAN sends a frame of data, the frame is duplicated on both ports and therefore on both LAN segments. This provides a redundant path for the data frame if one of the segments fails. Under normal conditions, both LAN segments are working, and each port receives identical frames. There are two ways of handling this: Duplicate Accept and Duplicate Discard.

The GE Vernova RedBox is the H49 switch. This is compatible with any other vendor's PRP device.

24.8.2 HIGH-AVAILABILITY SEAMLESS REDUNDANCY (HSR)

HSR is standardised in IEC 62439-3 (clause 5) for use in ring topology networks. Similar to PRP, HSR provides bumpless redundancy and meets the most demanding needs of substation automation. HSR has become the reference standard for ring-topology networks in the substation environment. The HSR implementation of the redundancy Ethernet board (REB) is compatible with any standard HSR device.

HSR works on the premise that each device connected in the ring is a doubly attached node running HSR (referred to as DANH). Similar to PRP, singly attached nodes such as printers are connected via Ethernet Redundancy Boxes (RedBox).

24.8.2.1 HSR MULTICAST TOPOLOGY

When a DANH is sending a multicast frame, the frame (C frame) is duplicated (A frame and B frame), and each duplicate frame A/B is tagged with the destination MAC address and the sequence number. The frames A and B differ only in their sequence number, which is used to identify one frame from the other. Each frame is sent to the network via a separate port. The destination DANH receives two identical frames, removes the HSR tag of the first frame received and passes this (frame D) on for processing. The other duplicate frame is discarded. The nodes forward frames from one port to the other unless it was the node that injected it into the ring.

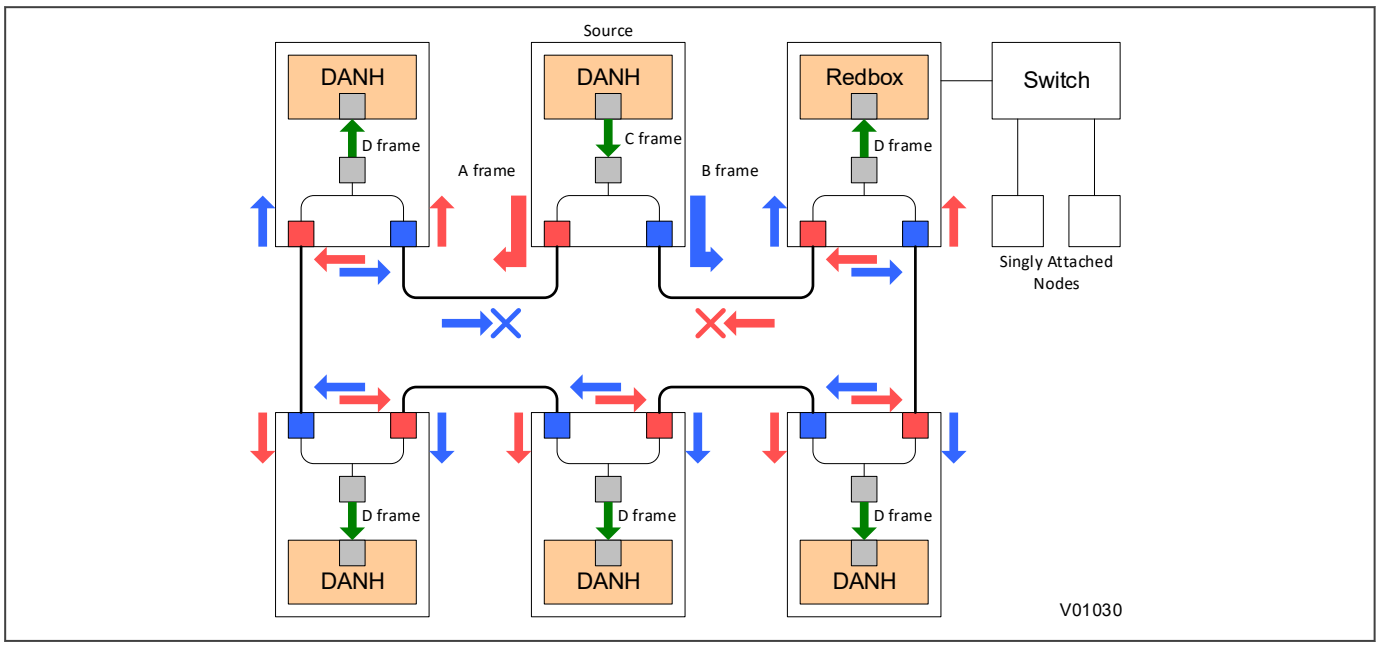


Figure 414: HSR multicast topology

Only about half of the network bandwidth is available in HSR for multicast or broadcast frames because both duplicate frames A & B circulate the full ring.

24.8.2.2 HSR UNICAST TOPOLOGY

With unicast frames, there is just one destination, and the frames are sent to that destination alone. All non-recipient devices simply pass the frames on. They do not process them in any way. In other words, D frames are produced only for the receiving DANH. This is illustrated below.

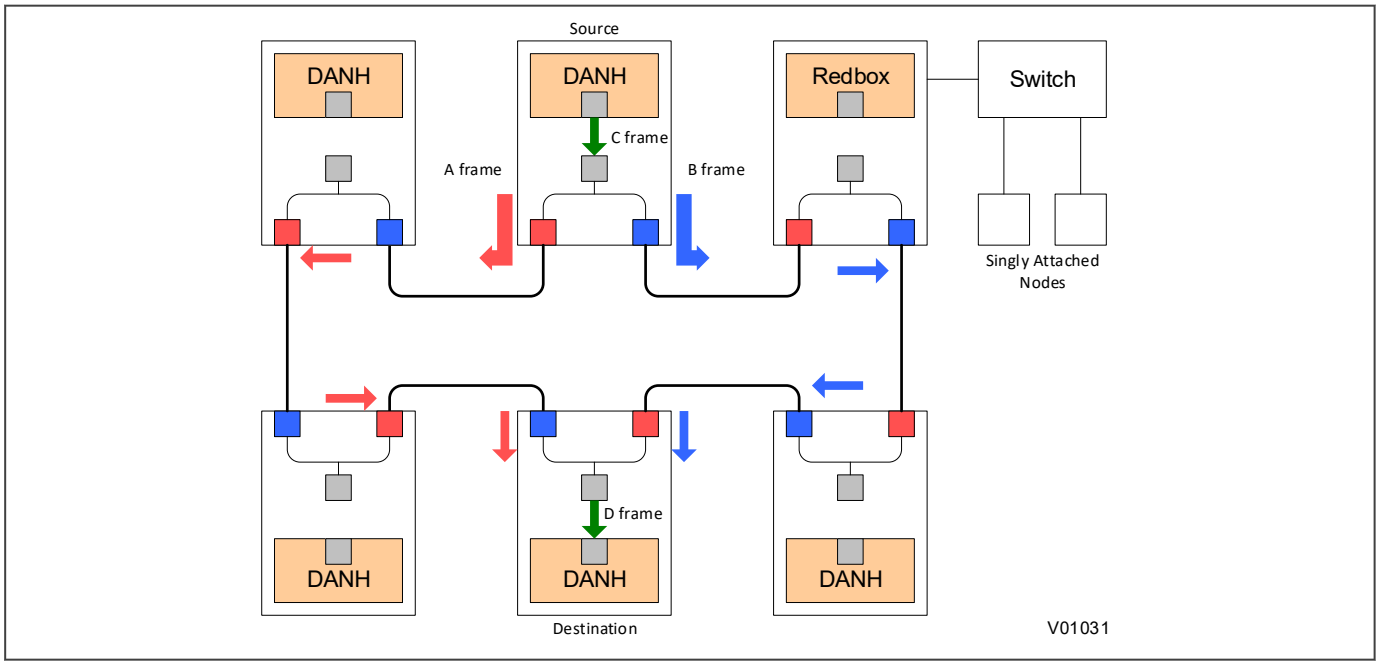


Figure 415: HSR unicast topology

For unicast frames, the whole bandwidth is available as both frames A & B stop at the destination node.

24.8.2.3 HSR APPLICATION IN THE SUBSTATION

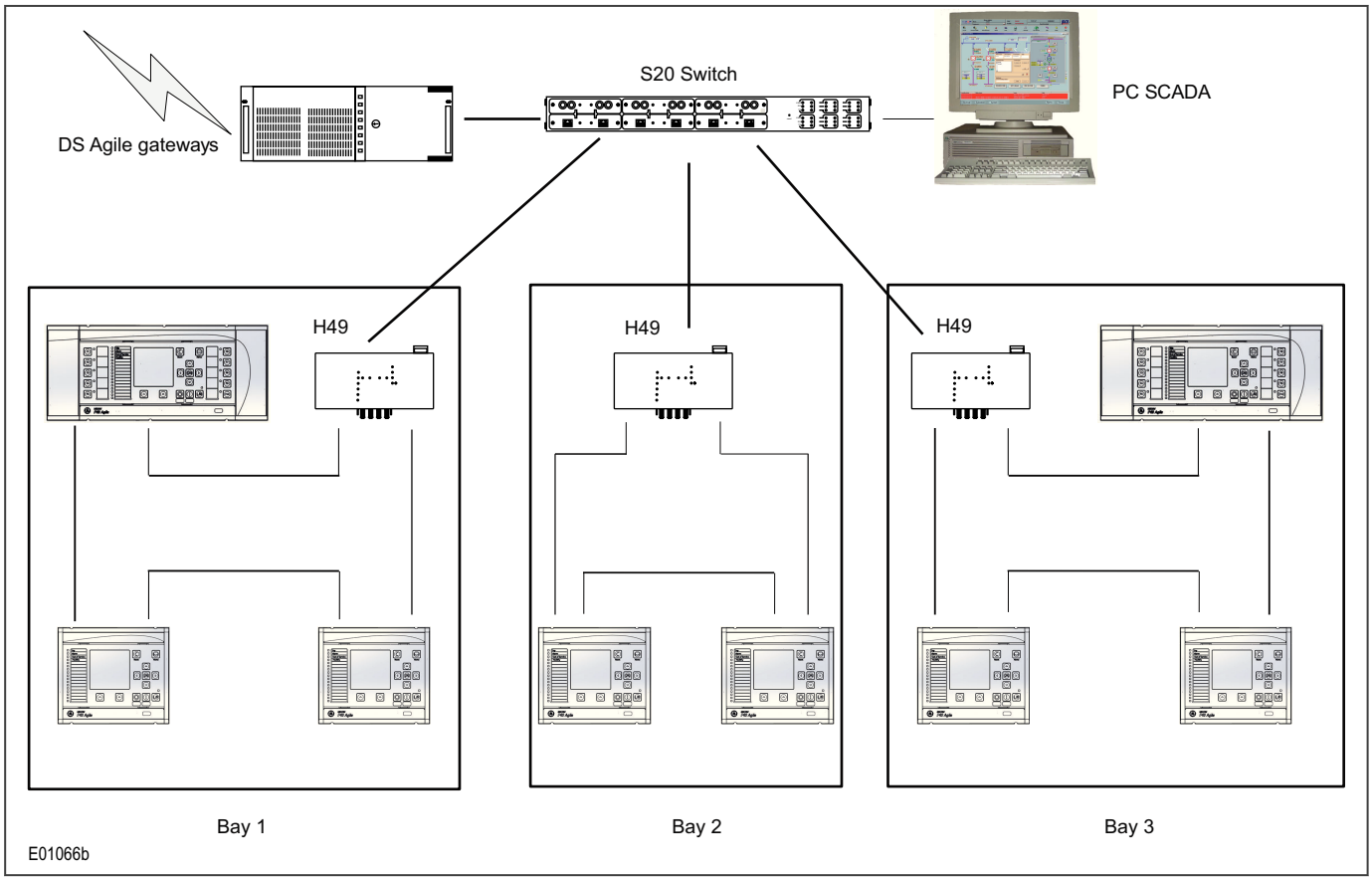


Figure 416: HSR application in the substation

24.8.2.4 RAPID SPANNING TREE PROTOCOL (RSTP)

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path, allowing loop-free network topology. Although RSTP can recover network faults quickly, the fault recovery time depends on the number of devices and the topology. The recovery time also depends on the time taken by the devices to determine the root bridge and compute the port roles (discarding, learning, forwarding). The devices do this by exchanging Bridge Protocol Data Units (BPDUs) containing information about bridge IDs and root path costs. See the IEEE 802.1D 2004 standard for further information.

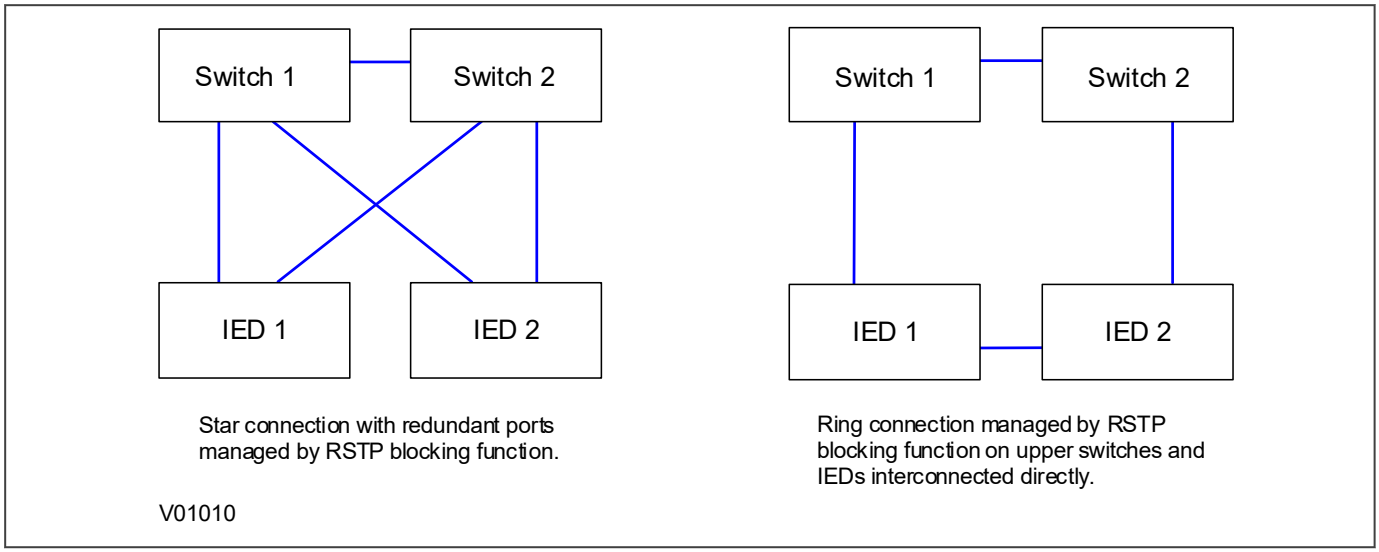


Figure 417: IED attached to redundant Ethernet star or ring circuit

The RSTP solution is based on open standards. It is therefore compatible with other Manufacturers' IEDs that use the RSTP protocol. The RSTP recovery time is typically 300 ms but it increases with network size, therefore cannot achieve the desired bumpless redundancy.

To ensure optimal performance of the protocol, make sure that one of the Ethernet switches is always the root of the RSTP topology.

24.8.2.5 FAILOVER

Failover is a simple redundancy mechanism that is not tied to any protocol. It works by selecting a main port and a switching time that can be as low as 2 seconds. When the main port link fails, the redundant port becomes physically active. At no point are both ports physically active, which means it can be used on any redundant or non-redundant network.

24.9 SECURE SHELL (SSH) COMMUNICATION

Secure Shell, commonly known as SSH, is a cryptographic network protocol designed to enable secure communication between devices over potentially unsecured networks. It is predominantly used to access and control remote systems securely and is commonly used for system administration, file transfers, and secure tunneling. Unlike older protocols such as Telnet, FTP, or Rlogin, which transmit data in plaintext and are susceptible to interception, SSH encrypts all communications, ensuring confidentiality, integrity, and authenticity.

SSH works on a client-server model where the client initiates a connection to the server, typically using the standard TCP port 22. Once the connection is established, a secure handshake occurs where cryptographic keys are exchanged, and the server presents its host key to the client. If the client recognises this key (for instance, from a previous connection saved in the known_hosts file), trust is established, and a symmetric session key is negotiated using asymmetric encryption techniques.

24.9.1 SSH COMMUNICATION BETWEEN S1 AGILE AND THE IED

S1 Agile configuration software (version 3.1.0 onwards) communicates with the IED (version AB onwards) over Ethernet through a secure tunnelled Courier protocol channel using SSHv2 on TCP port 22. The IED has an SSH server implemented and S1 Agile acts as the SSH client. To avoid connection to any rogue IED, the client (S1 Agile, in this case) supports server authentication based on a host key. Once S1 Agile receives a host key from the server, it will check if the key is already marked as "trusted", if not then S1 Agile will display a key fingerprint to the user for manually validating and confirming if the server (IED, in this case) can be "trusted". Although the server authentication can be disabled in S1 Agile, GE Vernova, strongly recommend keeping this feature "Enabled". The IED also supports client authentication using a configurable passcode. When initiating a connection, the user is presented with a Connection Parameters window, where the Client Passcode must be entered. By default, the Client Passcode is set to SSHPassphrase1#. The user needs to enter this string before the user himself is authenticated. Although client authentication can be disabled in the IED using the configurable setting, GE Vernova strongly recommend keeping this feature "Enabled". The default client passcode can be changed by users with the SECADM role within the S1 Agile software using Supervise Device Menu. The IED supports the disabling of the Courier protocol as part of hardening.

Note:
The default client passcode is SSHPassphrase1#

By default, S1 Agile version 3.1.0 or later uses SSH-based authentication when communicating with IEDs running firmware version AB or later. For IEDs belonging to other families or running earlier firmware versions, the software automatically falls back to using the legacy RPC (Remote Procedure Call) protocol for authentication and communication.

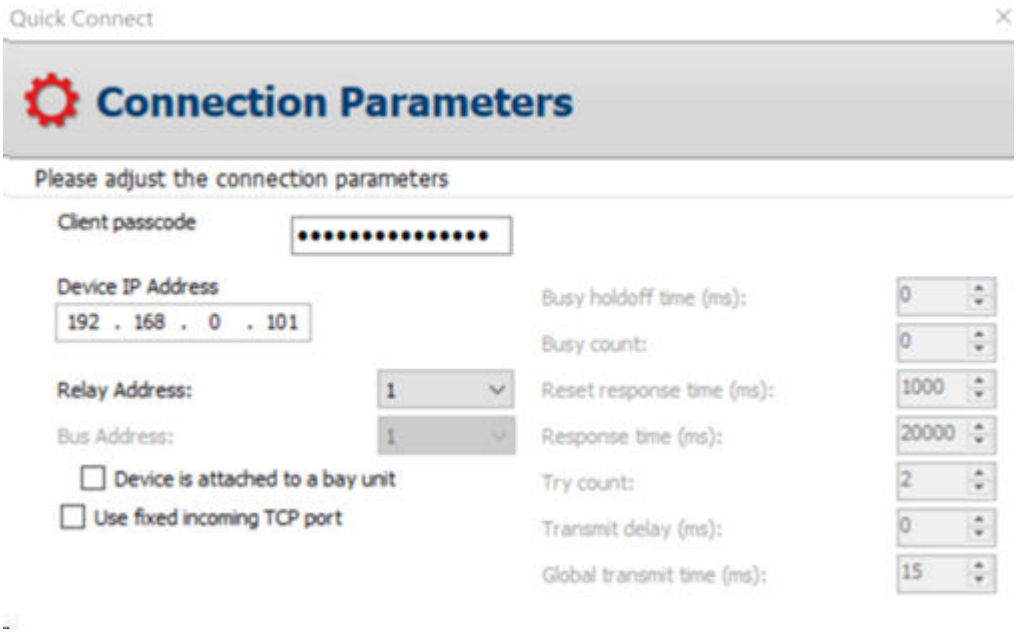


Figure 418: S1 Agile connection parameters window

24.10 SIMPLE NETWORK MANAGEMENT PROTOCOL (SNMP)

Simple Network Management Protocol (SNMP) is a network protocol designed to manage devices in an IP network. SNMP uses a Management Information Base (MIB) that contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read or set using SNMP with the appropriate software. The information in the MIB is standardised.

Each system in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

The SNMP-related branches of the MIB tree are located in the internet branch, which contains two main types of branches:

- Public branches (mgmt=2), which are defined by the Internet Engineering Task Force (IETF).
- Private branches (private=4), which are assigned by the Internet Assigned Numbers Authority (IANA). These are defined by the companies and organisations to which these branches are assigned.

The following figure shows the structure of the SNMP MIB tree. There are no limits on the width and depth of the MIB tree.

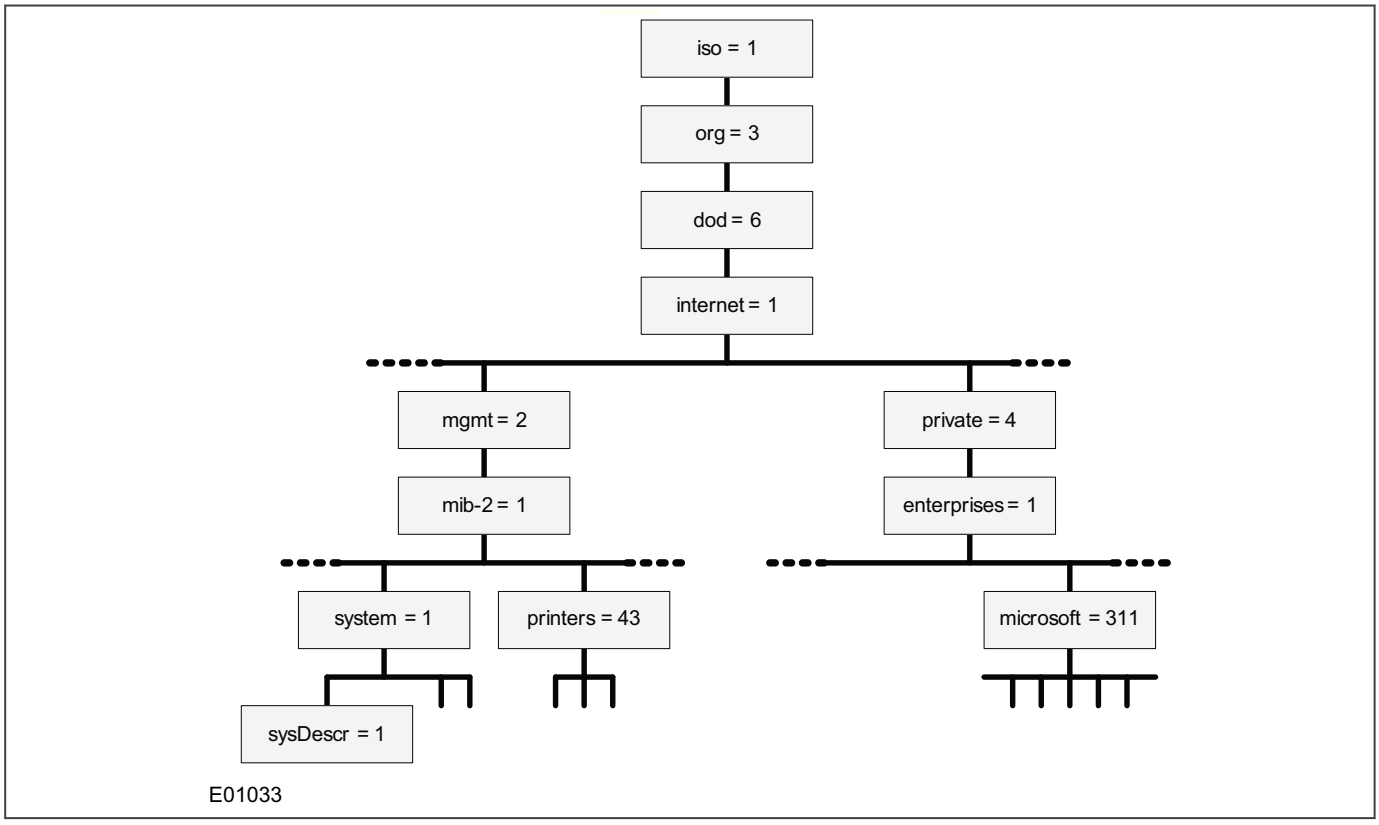


Figure 419: SNMP MIB tree

The top four levels of the hierarchy are fixed. These are:

- International Standards Organisation (iso)
- Organisation (org)
- Department of Defence (dod)
- Internet

Management (mgmt) is the main public branch. It defines network management parameters common to devices from all vendors. Underneath the Management branch is MIB-II (mib-2), and beneath this are branches for common management functions such as system management, printers, host resources, and interfaces.

The private branch of the MIB tree contains branches for large organisations, organised under the enterprises branch. This is not applicable to GE Vernova.

24.10.1 SNMP MIBS COMPATIBLE WITH THE IED

Our IED supports four different MIBs, all available for download on the GE website:

- IEC-62439-3-MIB: Standard PRP/HSR MIB.
- RMON-MIB: Standard Remote Monitoring MIB.
- GE-PX4X-MIB.mib: Private MIB that contains all the information specific to the relay. For example, model and serial number.
- GE-GRID-MIB.mib: Private MIB that only contains manufacturer information.

The information within the MIBs can be read using a simple text app like Notepad, or the MIB can be explored using an MIB Browser.

The private branch of the MIB tree contains branches for large organisations, organised under the enterprises branch. This is not applicable to GE Vernova.

24.10.2 SNMP MANAGEMENT INFORMATION BASES

SNMP uses a Management Information Base (MIB), which contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read using SNMP with the appropriate software. The information in the MIB is standardised.

Each device in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

24.10.3 MAIN PROCESSOR MIBS STRUCTURE

The Main Processor MIB uses a private OID with a specific number assigned by the IANA. Some items in this MIB also support SNMP traps (where indicated). These are items that can automatically notify a host without being read.

Address											Name	Trigger Trap?
0											ROOT NODE	
	1										ISO	
		3									Org	
			6								DOD	
				1							Internet	
					4						Private	
						1					Enterprise	

Address											Name	Trigger Trap?
							43534				(IANA No)	
								1			Px4x	
									1		System Data	
										1	Description	YES
										2	Plant Reference	YES
										3	Model Number	NO
										4	Serial Number	NO
										5	Frequency	NO
										6	Plant Status	YES
										7	Active Group	YES
										8	Software Ref.1	NO
										9	Software Ref.2	NO
										10	Access Level (UI)	YES
									2		Date and Time	
										1	Date Time	NO
										2	IRIG-B Status	YES
										3	Battery Status	YES
										4	Active Sync source	YES
										5	SNTP Server 1	NO
										6	SNTP Server 2	NO
										7	SNTP Status	YES
										8	PTP Status	YES
									3		System Alarms	
										1	Invalid Message Format	YES
										2	Main Protection Fail	YES
										3	Comms Changed	YES
										4	Max Prop. Alarm	YES
										5	9-2 Sample Alarm	YES
										6	9-2LE Cfg Alarm	YES
										7	Battery Fail	YES
										8	Rear Communication Fail	YES
										9	GOOSE IED Missing	YES
										10	Intermicom loopback	YES
										11	Intermicom message fail	YES
										12	Intermicom data CD fail	YES
										13	Intermicom Channel fail	YES
										14	Backup setting fail	YES
										15	User Curve commit to flash failure	YES
										16	SNTP time Sync fail	YES
										17	PTP failure alarm	YES
									4		Device Mode	
										1	IED Mod/Beh	YES
										2	Simulation Mode of Subscription	YES

24.10.4 NEW SNMP SYSTEM OBJECTS

The following elements have been added to the SNMP structure to more accurately describe the new functionalities added in the Ethernet boards:

24.10.4.1 NEW SNMP TRAPS

Changes in the Physical link statuses (Up or Down status) of NP1, NP2A, NP2B ethernet ports will be reported as SNMP traps.

The objects for these link statuses are added in MIB (GE-PX4X-MIB.mib). Below are the IDs for Network Port link objects:

- **np1Link**: 1.3.6.1.4.1.55461.1.6.1
- **np2ALink**: 1.3.6.1.4.1.55461.1.6.2
- **np2Blink**: 1.3.6.1.4.1.55461.1.6.3

24.10.4.2 NEW SNMP OBJECTS

The following objects have been added to MIB (GE-PX4X-MIB.mib) to add more visibility to the behaviour of the Ethernet board.

- **np2Redundancy:** .1.3.6.1.4.1.55461.1.6.4, represents active redundancy protocol set in the device.
- **rstpRootIdentifier**: .1.3.6.1.4.1.55461.1.6.5, represents RSTP Rot Bridge Identifier. It is a combination of Root bridge's priority and its MAC address.
- **rstpTimeSinceTopoChange**: .1.3.6.1.4.1.55461.1.6.6, represents the time elapsed since last RSTP topology change.
- **rstpTopoChangeCount**: .1.3.6.1.4.1.55461.1.6.7, represents RSTP topology change count.

24.10.5 SNMP ALARM ENHANCEMENT

An SNMP alarm is triggered by the relay when a security event occurs, if SNMP trap destination IP is configured in the settings.

24.10.5.1 SNMP ALARM FORMAT

The format of the SNMP trap/alarm for security events consists of three parts as described below.

"Event Description, Username, Interface".

Event Description: Short description of the alarm, same as the description present in Security event.

Username: User associated with the event, provided only when Username is available for the Security event.

Interface: Interface on which Security event has occurred, same as the interface information present in Security event.

24.10.5.2 LIST OF SNMP ALARMS

No.	Security Events	SNMP Trap Text
1	SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
2	SECUR_EVT_PW_MODIFIED	User password changed successfully
3	SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked - wrong credentials
4	SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
5	SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
6	SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - wrong credentials

No.	Security Events	SNMP Trap Text
7	SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired
8	SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
9	SECUR_EVT_IED_SEC_CODE_READ	Security Code read
10	SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
11	SECUR_EVT_PORT_DISABLED	Port Disabled
12	SECUR_EVT_PORT_ENABLED	Port Enabled
13	SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
14	SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
15	SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
16	SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
17	SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
18	SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
19	SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
20	SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
21	SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
22	SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
23	SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
24	SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
25	SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
26	SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
27	SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
28	SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
29	SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
30	SECUR_EVT_POWER_ON	Device Powered On
31	SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
32	SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
33	SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
34	SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
35	SECUR_EVT_RBAC_LOGIN	Log-in successful
36	SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
37	Bypass mode Activated	Bypass Mode Activated
38	Bypass mode Deactivated	Bypass Mode Deactivated
39	RADIUS Secret Key changed	RADIUS Secret Key changed
40	SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
41	Switch to Golden Image	Device switching to Firmware update mode
42	Fallback to Device Authentication	Fallback to Device Authentication
43	User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
44	Security events upload	Security Events uploaded from device

No.	Security Events	SNMP Trap Text
45	SSH Passcode change	SSH pass code change
46	SSH Client Authentication Fail	Failed client authentication
47	SSH Client Authentication Success	Successful client authentication
48	New User added	User account created successfully
49	User deleted	User account deleted successfully
50	User role change	Permission changed successfully
51	User name change	User renamed successfully

24.11 DATA PROTOCOLS

The products support a wide range of protocols to make them applicable to many industries and applications. The exact data protocols supported by a particular product depend on its chosen application, but the following table gives a list of the data protocols that are typically available.

Data Protocols

Data Protocol	Layer 1 Interface	Description
Courier	USB, K-Bus, RS232, RS485, Ethernet	Standard for SCADA communications developed by GE Vernova
IEC 60870-5-103	RS485	IEC standard for SCADA communications
DNP 3.0	RS485	Standard for SCADA communications
IEC 61850	Ethernet	IEC standard for substation automation. Facilitates interoperability.

The relationship of these protocols to the lower-level physical layer protocols are as follows:

Data Protocols	IEC 60870-5-103				
	DNP3.0	IEC 61850			
	Courier	Courier	Courier	Courier	Courier
Data Link Layer	EIA(RS)485	Ethernet	EIA(RS)232	K-Bus	USB
Physical Layer	Copper or Optical Fibre				USB Type B

The product supports switchable serial communication data protocol on the Rear Port 1 (RP1) interface (it is no longer necessary to select the protocol as a product order option). This setting cell is RP1 Protocol in the COMMUNICATIONS column. For example, the product can now be configured to provide IEC 61850 on the Ethernet interface and DNP3.0 on the serial port concurrently.

24.11.1 COURIER

This section should provide sufficient detail to enable understanding of the Courier protocol at a level required by most users. For situations where the level of information contained in this manual is insufficient, further publications (R6511 and R6512) containing in-depth details about the protocol and its use, are available on request.

Courier is a GE Vernova proprietary communication protocol. Courier uses a standard set of commands to access a database of settings and data in the IED. This allows a master to communicate with a number of slave devices. The application-specific elements are contained in the database rather than in the commands used to interrogate it, meaning that the master station does not need to be preconfigured. Courier also provides a sequence of event (SOE) and disturbance record extraction mechanism.

24.11.1.1 PHYSICAL CONNECTION AND LINK LAYER

Courier can be used with four physical layer protocols: USB, K-Bus, EIA(RS)232 or EIA(RS)485.

Several connection options are available for Courier:

- The front USB port (for connection to Settings application software on, for example, a laptop).
- Rear Port 1 (RP1) - for permanent SCADA connection via serial RS485 or K-Bus
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via serial optical fibre
- Optional Rear Port 2 (RP2) - for permanent SCADA connection via serial RS485, K-Bus, or RS232

Optional Ethernet board (NIC) - for remote communication with the S1 Agile settings application software across an Ethernet network.

For either of the serial rear ports, both the IED address, and baud rate can be selected using the front panel menu or by the settings application software.

Note:
*Changing the **RP2 Port Config** setting (K-Bus, EIA(RS)232) requires the IED to be rebooted, for the change to become effective.*

24.11.1.2 COURIER DATABASE

The Courier database is two-dimensional and resembles a table. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255 (0000 to FFFF Hexadecimal. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The product-specific menu databases contain the complete database definition.

24.11.1.3 SETTINGS CATEGORIES

There are two main categories of settings in protection IEDs:

- Control and support settings
- Protection settings

With the exception of the Disturbance Recorder settings, changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to the Protection settings and the Disturbance Recorder settings are stored in ‘scratchpad’ memory and are not immediately implemented. These need to be committed by writing to the ***Save Changes*** cell in the *CONFIGURATION* column.

24.11.1.4 SETTING CHANGES

Courier provides two mechanisms for making setting changes. Either method can be used for editing any of the settings in the database.

Method 1

This uses a combination of three commands to perform a settings change:

First, enter Setting mode: This checks that the cell is settable and returns the limits.

1. Preload Setting: This places a new value into the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
2. Execute Setting: This confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
3. Abort Setting: This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are extracted before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

Method 2

The Set Value command can be used to change a setting directly. The response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method; however, the limits are not extracted. This method is therefore most suitable for off-line setting editors such as MiCOM S1 Agile, or for issuing preconfigured control commands.

24.11.1.5 EVENT EXTRACTION

You can extract events either automatically (rear serial port only) or manually (either serial port). For automatic extraction, all events are extracted in sequential order using the Courier event mechanism. This includes fault and maintenance data if appropriate. The manual approach allows you to select events, faults, or maintenance data as desired.

24.11.1.5.1 AUTOMATIC EVENT RECORD EXTRACTION

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the ***Event*** bit is set in the ***Status*** byte. This indicates to the Master device that event information is available. The oldest, non-extracted event can be extracted from the IED using the ***Send Event*** command. The IED responds with the event data.

Once an event has been extracted, the ***Accept Event*** command can be used to confirm that the event has been successfully extracted. When all events have been extracted, the ***Event*** bit is reset. If there are more events still to be extracted, the next event can be accessed using the ***Send Event*** command as before.

24.11.1.5.2 MANUAL EVENT RECORD EXTRACTION

The *VIEW RECORDS* column (location 01) is used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. You can select events by event number and directly select a fault or maintenance record by number.

Event record selection ('Select Event' cell: 0101)

This cell can set the number of stored events. For simple event records (Type 0), cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault record selection ('Select Fault' cell: 0106)

This cell can be used to select a fault record directly, using a value between 0 and 99 to select one of up to a hundred stored fault records. (0 is the most recent fault and 99 is the oldest). The column then contains the details of the fault record selected.

Maintenance record selection ('Select Maint' cell: 01F0)

This cell can be used to select a maintenance record using a value between 0 and 9. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information, the number associated with a particular record changes when a new event or fault occurs.

Event types

The IED generates events under certain circumstances such as:

- Change of state of output contact
- Change of state of opto-input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

Event record format

The IED returns the following fields when the Send Event command is invoked:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Menu Database contains tables of possible events and shows how the contents of the above fields are interpreted. Fault and Maintenance records return a Courier Type 3 event, which contains the above fields plus two additional fields:

- Event extraction column
- Event number

These events contain additional information, which is extracted from the IED using column B4. Row 01 contains a ***Select Record*** setting that allows the fault or maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the IED by uploading the text and data from the column.

24.11.1.6 DISTURBANCE RECORD EXTRACTION

The stored disturbance records are accessible through the Courier interface. The records are extracted using column (B4).

The ***Select Record*** cell can be used to select the record to be extracted. Record 0 is the oldest non-extracted record. Older records which have already been extracted are assigned positive values, while younger records are assigned negative values. To help automatic extraction through the rear port, the IED sets the ***Disturbance*** bit of the ***Status*** byte, whenever there are non-extracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from the ***Trigger Time*** cell (B402). The disturbance record can be extracted using the block transfer mechanism from cell B40B and saved in the COMTRADE format. The settings application software software automatically does this.

24.11.1.7 PROGRAMMABLE SCHEME LOGIC SETTINGS

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the IED using the block transfer mechanism.

The following cells are used to perform the extraction:

- ***Domain*** cell (B204): Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- ***Sub-Domain*** cell (B208): Used to select the Protection Setting Group to be uploaded or downloaded.
- ***Version*** cell (B20C): Used on a download to check the compatibility of the file to be downloaded.
- ***Transfer Mode*** cell (B21C): Used to set up the transfer process.
- ***Data Transfer*** cell (B120): Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the IED using this mechanism. The settings application software must be used to edit the settings. It also performs checks on the validity of the settings before they are transferred to the IED.

The language of a recovered PSL file depends on the language of a settings file sent on the same interface used to recover the PSL file. All interfaces are set by default to English, which means by default, the relay will recover the PSL file in English on all interfaces.

As an example, if the PSL file needs to be recovered in French through the front port, the user is required to send the settings file to the relay in French through the front port prior to recovering the PSL file. While the PSL file will be

recovered in French through the front port, it will still be recovered in English through Ethernet and the rear RS485 port if available, unless and until the settings file is sent in French on those interfaces as well.

24.11.1.8 TIME SYNCHRONISATION

The time and date can be set using the time synchronisation feature of the Courier protocol. The device will correct for the transmission delay. The time synchronisation message may be sent as either a global command or to any individual IED address. If the time synchronisation message is sent to an individual address, then the device will respond with a confirm message. If sent as a global command, the (same) command must be sent twice. A time synchronisation Courier event will be generated/produced whether the time-synchronisation message is sent as a global command or to any individual IED address.

If the clock is being synchronised using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronised internal clock.

24.11.1.9 COURIER CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `Courier`.
4. Move down to the next cell (***RP1 Address***). This cell controls the address of the RP1 port on the device. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 1 and 254 for the Relay Address. It is set to 255 by default, which must be changed. It is important that no two IEDs share the same address.
5. Move down to the next cell (***RP1 InactivTimer***). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before revoking any password access that was enabled and discarding any changes. For the rear port this can be set between 1 and 30 minutes.
6. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
7. Move down to the next cell (***RP1 Card Status***). This cell is not settable. It displays the status of the chosen physical layer protocol for RP1.
8. Move down to the next cell (***RP1 Port Config***). This cell controls the type of serial connection. Select between K-Bus or RS485.
9. If using EIA(RS)485, the next cell (***RP1 Comms Mode***) selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity. If using K-Bus this cell will not appear.
10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; 9600, 19200 and 38400. If using K-Bus this cell will not appear as the baud rate is fixed at 64 kbps.

24.11.2 IEC 60870-5-103

The specification IEC 60870-5-103 (Telecontrol Equipment and Systems Part 5 Section 103: Transmission Protocols), defines the use of standards IEC 60870-5-1 to IEC 60870-5-5, which were designed for communication with protection equipment.

This section describes how the IEC 60870-5-103 standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 60870-5-103 standard.

This section should provide sufficient detail to enable understanding of the standard at a level required by most users.

The IEC 60870-5-103 interface is a master/slave interface with the device as the slave device. The device conforms to compatibility level 2, as defined in the IEC 60870-5-103.standard.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialisation (reset)
- Time synchronisation
- Event record extraction
- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

24.11.2.1 PHYSICAL CONNECTION AND LINK LAYER

Two connection options are available for IEC 60870-5-103:

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

If the optional fibre optic port is fitted, a menu item appears in which the active port can be selected. However, the selection is only effective following the next power up.

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

24.11.2.2 INITIALISATION

Whenever the device has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The device will respond to either of the two reset commands; Reset CU or Reset FCB (Communication Unit or Frame Count Bit). The difference between the two commands is that the Reset CU command will clear any unsent messages in the transmit buffer, whereas the Reset FCB command does not delete any messages.

The device will respond to the reset command with an identification message ASDU 5. The Cause of Transmission (COT) of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Menu Database, available from GE Vernova separately if required.

In addition to the above identification message, it will also produce a power up event.

24.11.2.3 TIME SYNCHRONISATION

The time and date can be set using the time synchronisation feature of the IEC 60870-5-103 protocol. The device will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronisation message is sent as a send/confirm message, then the device will respond with a confirm message. A time synchronisation Class 1 event will be generated/produced whether the time-synchronisation message is sent as a send confirm or a broadcast (send/no reply) message.

If the clock is being synchronised using the IRIG-B input, then it will not be possible to set the device time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronised internal clock.

24.11.2.4 CONFIGURABLE IEC 60870-5-103 SIGNAL LIST

From Software Version 91 onwards, there is a setting cell which allows the IEC 60870-5-103 private range signals to be selected and de-selected from IEC 60870-5-103 communication.

The IEC 60870-5-103 standard (compatible range) signals, that are provided according to the relay type and implementation, are always enabled. These signals cannot be disabled.

This setting cell is ***Config Mode*** in the *PROTOCOL CFG* column.

There are two settings associated with this cell. These are:

Setting	Description
Fixed	In this mode, the IED behaviour for IEC 60870-5-103 protocol is identical to pre-Software Version 91 IEDs. All the implemented signals (IEC 60870-5-103 compatible range and private range signals) are enabled for IEC 60870-5-103 communication. The COT behaviour will be according to the device IEC 60870-5-103 profile. This mode is provided for backward compatibility. This is the default setting.
Std+UserConfig	In this mode, the user can select which IEC 60870-5-103 private range signals are enabled for IEC 60870-5-103 communication. The selection is done using DDB mask setting cells in the *PROTOCOL CFG* column. The DDB mask value controls only the signal selection (enabled or disabled) for IEC 60870-5-103 communication. It does not modify the COT behaviour of the signals. The COT behaviour of the private range signals will be according to the device IEC 60870-5-103 profile. By default, only IEC 60870-5-103 standard signals are enabled. All private range signals are disabled.

When the ***Config Mode*** cell is set to `Std+UserConfig`, the DDB masks become visible in the *PROTOCOL CFG* column. These masks function in a similar way to the DDB masks in the *RECORD CONTROL* column. Editing these masks controls the DDB signals that are enabled for communication of the equivalent IEC 60870-5-103 private range signal, as listed in the IEC 60870-5-103 profile in the Menu Database.

Within these masks, only individual DDBs that are equivalent to IEC 60870-5-103 private range signals are editable. By default, all of the individual DDBs that are equivalent to IEC 60870-5-103 private range signals are set to 0 (zero), that is disabled for communication. Setting any individual DDB to 1 (one), enables the equivalent IEC 60870-5-103 private range signal for communication.

Within these masks, individual DDBs that are either equivalent to IEC 60870-5-103 standard range signals, or do not have any equivalent IEC 60870-5-103 private range signal, are not editable.

24.11.2.5 SPONTANEOUS EVENTS

Events are categorised using the following information:

- Function type
- Information Number

The IEC 60870-5-103 profile in the Menu Database contains a complete listing of all events produced by the device.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for spontaneous communication, by setting the ***Config Mode*** cell to `Std+UserConfig` and configuring the DDB masks as required.

24.11.2.6 GENERAL INTERROGATION (GI)

The GI request can be used to read the status of the device, the function numbers, and information numbers that will be returned during the GI cycle. These are shown in the IEC 60870-5-103 profile in the Menu Database.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for GI reporting, by setting the ***Config Mode*** cell to `Std+UserConfig` and configuring the DDB masks as required.

24.11.2.7 CYCLIC MEASUREMENTS

The device will produce measured values using ASDU 9 on a cyclical basis, this can be read from the device using a Class 2 poll (note ADSU 3 is not used). The rate at which the device produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu or using MiCOM S1 Agile. It is active immediately following a change.

The device transmits its measurands with maximum value of 2.4 times the rated value of the measurement.

24.11.2.8 COMMANDS

A list of the supported commands is contained in the Menu Database. The device will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating 'negative acknowledgement'.

24.11.2.9 TEST MODE

It is possible to disable the device output contacts to allow secondary injection testing to be performed using either the front panel menu or the front serial port. The IEC 60870-5-103 standard interprets this as 'test mode'. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the device is in test mode will have a COT of 'test mode'.

24.11.2.10 DISTURBANCE RECORDS

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

> *Note:*
> *IEC 60870-5-103 only supports up to 8 records.*

24.11.2.11 COMMAND/MONITOR BLOCKING

The device supports a facility to block messages in the monitor direction (data from the device) and also in the command direction (data to the device). Messages can be blocked in the monitor and command directions using one of the two following methods

- The menu command ***RP1 CS103Blcking*** in the *COMMUNICATIONS* column
- The DDB signals Monitor Blocked and Command Blocked

24.11.2.12 IEC 60870-5-103 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol - in this case `IEC 60870-5-103`.
4. Move down to the next cell (***RP1 Address***). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.
5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Two baud rates are supported by the IED, `9600 bits/s` and `19200 bits/s`. Make sure that the baud rate selected on the IED is the same as that set on the master station.

6. Move down to the next cell (***RP1 Meas Period***). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell and can be set between 1 and 60 seconds.
7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
8. The next cell down (***RP1 CS103Blcking***) can be used for monitor or command blocking.
9. There are three settings associated with this cell; these are:

Setting	Description
Disabled	No blocking selected.
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energising an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a "Termination of general interrogation" message to the master station.
Command Blocking	When the command blocking DDB signal is active high, either by energising an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a "negative acknowledgement of command" message to the master station.

24.11.3 DNP 3.0

This section describes how the DNP 3.0 standard is applied in the product. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the DNP 3.0 standard.

The descriptions given here are intended to accompany the device profile document that is included in the Menu Database document. The DNP 3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP 3.0 implementation. This is the standard format DNP 3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the device using DNP 3.0. The IED operates as a DNP 3.0 slave and supports subset level 2, as described in the DNP 3.0 standard, plus some of the features from level 3.

The DNP 3.0 protocol is defined and administered by the DNP Users Group. For further information on DNP 3.0 and the protocol specifications, please see the DNP website (www.dnp.org).

24.11.3.1 PHYSICAL CONNECTION AND LINK LAYER

DNP 3.0 can be used with EIA(RS)485.

Several connection options are available for DNP 3.0

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

The baud rate can be selected using the front panel menu or by the settings application software.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 stop bit and optional configurable parity bit.

24.11.3.2 OBJECT 1 BINARY INPUTS

Object 1, binary inputs, contains information describing the state of signals in the IED, which mostly form part of the digital data bus (DDB). In general, these include the state of the output contacts and opto-inputs, alarm signals, and protection start and trip signals. The ‘DDB number’ column in the device profile document provides the DDB numbers for the DNP 3.0 point data. These can be used to cross-reference to the DDB definition list. See the

relevant Menu Database document. The binary input points can also be read as change events using Object 2 and Object 60 for class 1-3 event data.

Note:
For the DNP Events to be transmitted it is mandatory to have the corresponding DDBs of the Configured Point Index to be included in the Courier Event Record. The RECORD CONTROL Menu lists all the DDBs, and the mask settings control their inclusion/exclusion as a Courier Event.

24.11.3.3 OBJECT 10 BINARY OUTPUTS

Object 10, binary outputs, contains commands that can be operated using DNP 3.0. Therefore, the points accept commands of type pulse on (null, trip, close) and latch on/off as detailed in the device profile in the relevant Menu Database document, and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the Control Inputs. Described as Alias Control Inputs, they reflect the state of the Control Input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

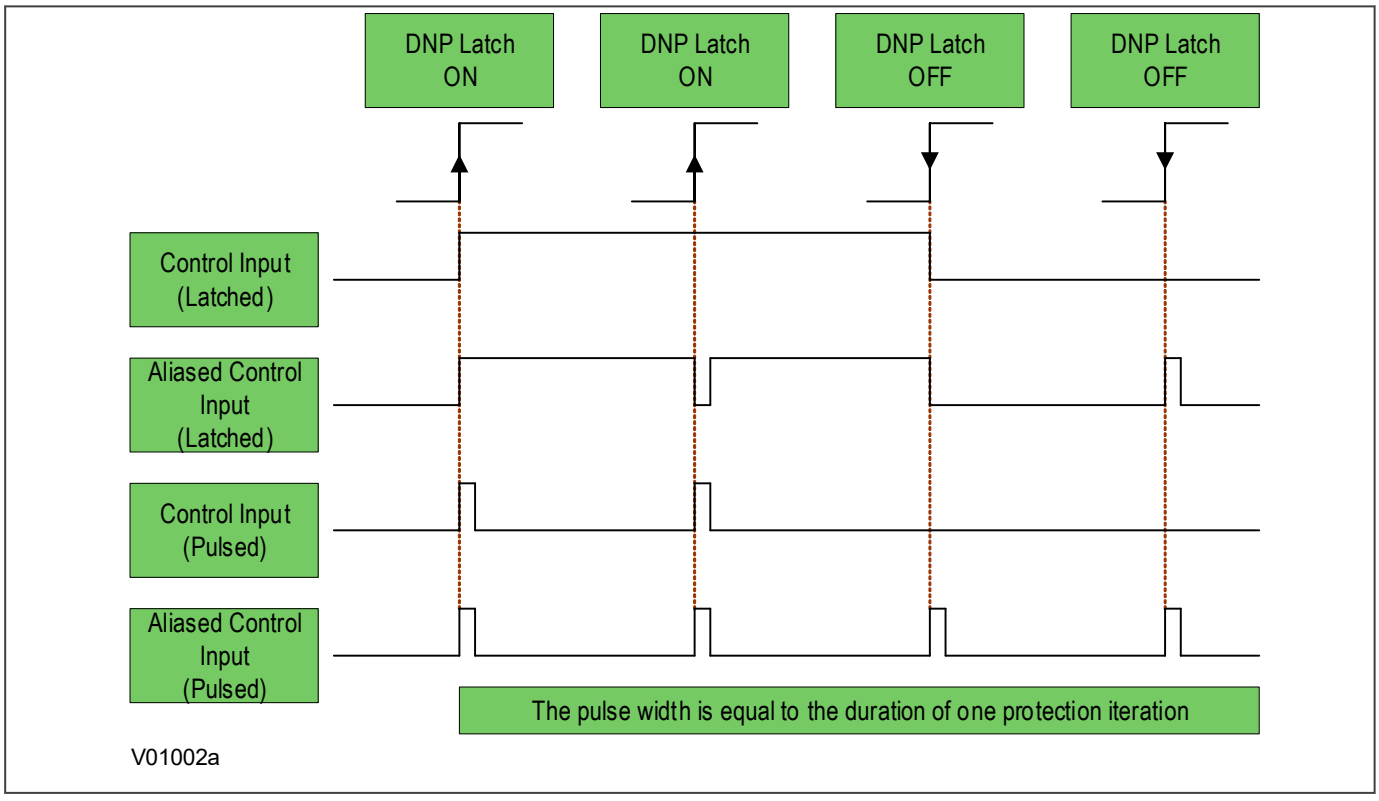


Figure 420: Control input behaviour

Many of the IEDs functions are configurable so some of the Object 10 commands described in the following sections may not be available. A read from Object 10 reports the point as off-line and an operate command to Object 12 generates an error response.

Examples of Object 10 points that may be reported as off-line are:

- Activate setting groups: Ensure setting groups are enabled
- CB trip/close: Ensure remote CB control is enabled
- Reset NPS thermal: Ensure NPS thermal protection is enabled
- Reset thermal O/L: Ensure thermal overload protection is enabled
- Reset RTD flags: Ensure RTD Inputs is enabled
- Control inputs: Ensure control inputs are enabled

24.11.3.4 OBJECT 20 BINARY COUNTERS

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from Object 20, or as a 'frozen' value from Object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding Object 21 frozen counter. The freeze and clear function resets the Object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from Object 22 and Object 23 respectively. Counter change events (Object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (Object 23) are generated whenever a freeze operation is performed, and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

24.11.3.5 OBJECT 30 ANALOGUE INPUT

Object 30, analogue inputs, contains information from the IED's measurements columns in the menu. All Object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalised values (which takes into account the IED's CT and VT ratios), and this is settable in the *COMMUNICATIONS* column in the IED. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalised value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analogue measurement that is unavailable when it is read is reported as offline. For example, the frequency would be offline if the current and voltage frequency is outside the tracking range of the IED. All Object 30 points are reported as secondary values in DNP 3.0 (with respect to CT and VT ratios).

24.11.3.6 OBJECT 40 ANALOGUE OUTPUT

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the IED such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

24.11.3.7 OBJECT 50 TIME SYNCHRONISATION

Function codes 1 (read) and 2 (write) are supported for Object 50 (time and date) variation 1. The DNP Need Time function (the duration of time waited before requesting another time sync from the master) is supported and is configurable in the range 1 - 30 minutes.

If the clock is being synchronised using the IRIG-B input, then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronised internal clock.

24.11.3.8 DNP3 DEVICE PROFILE

This section describes the specific implementation of DNP version 3.0 within GE Vernova MiCOM P40 Agile IEDs for both compact and modular ranges.

The devices use the DNP 3.0 Slave Source Code Library version 3 from Triangle MicroWorks Inc.

This document, in conjunction with the DNP 3.0 Basic 4 Document Set, and the DNP Subset Definitions Document, provides complete information on how to communicate with the devices using the DNP 3.0 protocol.

This implementation of DNP 3.0 is fully compliant with DNP 3.0 Subset Definition Level 2. It also contains many Subset Level 3 and above features.

24.11.3.8.1 DNP3 DEVICE PROFILE TABLE

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a “Document”, it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

DNP 3.0 Device Profile Document	
Vendor Name:	GE Vernova
Device Name:	MiCOM P40Agile Protection Relays - compact and modular range
Models Covered:	All models
Highest DNP Level Supported*: * This is the highest DNP level FULLY supported. Parts of level 3 are also supported	For Requests: Level 2 For Responses: Level 2
Device Function:	Slave
Notable objects, functions, and/or qualifiers supported in addition to the highest DNP levels supported (the complete list is described in the DNP 3.0 Implementation Table): For static (non-change event) object requests, request qualifier codes 00 and 01 (start-stop), 07 and 08 (limited quantity), and 17 and 28 (index) are supported in addition to the request qualifier code 06 (no range (all points)) Static object requests sent with qualifiers 00, 01, 06, 07, or 08 will be responded with qualifiers 00 or 01 Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28 For change-event object requests, qualifiers 17 or 28 are always responded 16-bit and 32-bit analogue change events with time may be requested The read function code for Object 50 (time and date) variation 1 is supported Analogue Input Deadbands, Object 34, variations 1 through 3, are supported Floating Point Analogue Output Status and Output Block Objects 40 and 41 are supported Sequential file transfer, Object 70, variations 2 through 7, are supported Device Attribute Object 0 is supported	
Maximum Data Link Frame Size (octets):	Transmitted: 292 Received: 292
Maximum Application Fragment Size (octets)	Transmitted: Configurable (100 to 2048). Default 2048 Received: 249
Maximum Data Link Retries:	Fixed at 2
Maximum Application Layer Retries:	None
Requires Data Link Layer Confirmation:	Configurable to Never or Always
Requires Application Layer Confirmation:	When reporting event data (Slave devices only) When sending multi-fragment responses (Slave devices only)

DNP 3.0 Device Profile Document	
Timeouts while waiting for:	
Data Link Confirm:	Configurable
Complete Application Fragment:	None
Application Confirm:	Configurable
Complete Application Response:	None
Others:	
Data Link Confirm Timeout:	Configurable from 0 (Disabled) to 120s, default 10s.
Application Confirm Timeout:	Configurable from 1 to 120s, default 2s.
Select/Operate Arm Timeout:	Configurable from 1 to 10s, default 10s.
Need Time Interval (Set IIN1-4):	Configurable from 1 to 30, default 10min.
Application File Timeout	60 s
Analog Change Event Scan Period:	Fixed at 0.5s
Counter Change Event Scan Period	Fixed at 0.5s
Frozen Counter Change Event Scan Period	Fixed at 1s
Maximum Delay Measurement Error:	2.5 ms
Time Base Drift Over a 10-minute Interval:	7 ms
Sends/Executes Control Operations:	
Write Binary Outputs:	Never
Select/Operate:	Always
Direct Operate:	Always
Direct Operate - No Ack:	Always
Count > 1	Never
Pulse On	Always
Pulse Off	Sometimes
Latch On	Always
Latch Off	Always
Queue	Never
Clear Queue	Never
Note: Paired Control points will accept Pulse On/Trip and Pulse On/Close, but only single point will accept the Pulse Off control command.	
Reports Binary Input Change Events when no specific variation requested:	Configurable to send one or the other
Reports time-tagged Binary Input Change Events when no specific variation requested:	Binary input change with time
Sends Unsolicited Responses:	Never
Sends Static Data in Unsolicited Responses:	Never No other options are permitted
Default Counter Object/Variation:	Configurable, Point-by-point list attached Default object: 20 Default variation: 1

DNP 3.0 Device Profile Document	
Counters Roll Over at:	32 bits
Sends multi-fragment responses:	Yes
Sequential File Transfer Support:	
Append File Mode	No
Custom Status Code Strings	No
Permissions Field	Yes
File Events Assigned to Class	No
File Events Send Immediately	Yes
Multiple Blocks in a Fragment	No
Max Number of Files Open	1

24.11.3.8.2 DNP3 IMPLEMENTATION TABLE

The implementation table provides a list of objects, variations and control codes supported by the device:

Object			Request (Library Will Parse)				Response (Library Will Respond With)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
1	0	Binary Input (Variation 0 is used to request default variation)	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
1	1 (default - see note 1)	Binary Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
1	2	Binary Input with Flag	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
2	0	Binary Input Change - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
2	1	Binary Input Change without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
2	2	Binary Input Change with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
10	0	Binary Output Status - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
10	2 (default - see note 1)	Binary Output Status	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
12	1	Control Relay Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28	(index)	129	response		echo of request
20	0	Binary Counter - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
			7 8 9 10	(freeze) (freeze noack) (freeze clear) (frz. cl. Noack)	00, 01 06 07, 08	(start-stop) (no range, or all) (limited qty)				

Object			Request (Library Will Parse)				Response (Library Will Respond With)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
20	1	32-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	2	16-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	5 (default - see note 1)	32-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	6	16-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	0	Frozen Counter - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
21	1	32-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	2	16-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	5	32-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 1)
21	6	16-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) 17, 28 (index - see note 1)
21	9 (default - see note 1)	32-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	10	16-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
`22	0	Counter Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
22	1 (default - see note 1)	32-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	2	16-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	5	32-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	6	16-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1	(read)	06 07, 08	(no range, or all) (limited qty)				
23	1 (default - see note 1)	32-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	2	16-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	5	32-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	6	16-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)

Object			Request (Library Will Parse)				Response (Library Will Respond With)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
30	0	Analog Input - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
30	1	32-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	2	16-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	3 (default - see note 1)	32-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	4	16-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	5	Short floating point	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
32	0	Analog Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
32	1 (default - see note 1)	32-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	2	16-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	3	32-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	4	16-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	5	Short floating point Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	7	Short floating point Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
34	0	Analog Input Deadband (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
34	1	16 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	2 (default - see note 1)	32 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	3	Short Floating Point Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				

Object			Request (Library Will Parse)				Response (Library Will Respond With)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
40	0	Analog Output Status (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
40	1 (default - see note 1)	32-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	2	16-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	3	Short Floating Point Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
41	1	32-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request
41	2	16-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request
41	3	Short Floating Point Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 27, 28	(index)	129	response		echo of request
50	1 (default - see note 1)	Time and Date	1	(read)	07	(limited qty = 1)	129	response	07	(limited qty = 1)
			2	(write)	07	(limited qty = 1)				
60	0	Not defined								
60	1	Class 0 Data	1	(read)	06	(no range, or all)				
60	2	Class 1 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	3	Class 2 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	4	Class 3 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	0	File Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	2	File Authentication	29	(authenticate)	5b	(free-format)	129	response		5B (free-format)
70	3	File Command	25 27	(open) (delete)	5b	(free-format)				
70	4	File Command Status	26 30	(close) (abort)	5b	(free-format)	129	response		5B (free-format)
70	5	File Transfer	1	(read)	5b	(free-format)	129	response		5B (free-format)
70	6	File Transfer Status					129	response		5B (free-format)
70	7	File Descriptor	28	(get file info)	5b	(free-format)	129	response		5B (free-format)
80	1	Internal Indications	1	(read)	00, 01	(start-stop)	129	response	00, 01	(start-stop)
		No Object (function code only)	13	(cold restart)						
		No Object (function code only)	14	(warm restart)						
		No Object (function code only)	23	(delay meas.)						

Note:
A Default variation refers to the variation responded to when variation 0 is requested and/or in class 0, 1, 2, or 3 scans.

Note:
For static (non-change-event) objects, qualifiers 17 or 28 are only responded to when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded to with qualifiers 00 or 01. For change-event objects, qualifiers 17 or 28 are always responded to.

24.11.3.8.3 DNP3 INTERNAL INDICATIONS

The following table lists the DNP3.0 Internal Indications (IIN) and identifies those that are supported by the device.

The IIN form an information element used to convey the internal states and diagnostic results of a device. This information can be used by a receiving station to perform error recovery or other suitable functions. The IIN is a two-octet field that follows the function code in all responses from the device. When a request cannot be processed due to formatting errors or the requested data is not available, the IIN is always returned with the appropriate bits set.

Bit	Indication	Description	Supported
Octet 1			
0	All stations message received	Set when a request is received with the destination address of the all stations address (6553510). It is cleared after the next response (even if a response to a global request is required). This IIN is used to let the master station know that a "broadcast" message was received by the relay.	Yes
1	Class 1 data available	Set when data that has been configured as Class 1 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
2	Class 2 data available	Set when data that has been configured as Class 2 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
3	Class 3 data available	Set when data that has been configured as Class 3 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
4	Time-synchronisation required	The relay requires time synchronisation from the master station (using the Time and Date object). This IIN is cleared once the time has been synchronised. It can also be cleared by explicitly writing a 0 into this bit of the Internal Indication object.	Yes
5	Local	Set when some or all of the relays digital output points (Object 10/12) are in the Local state. That is, the relays control outputs are NOT accessible through the DNP protocol. This IIN is clear when the relay is in the Remote state. That is, the relays control outputs are fully accessible through the DNP protocol.	No
6	Device in trouble	Set when an abnormal condition exists in the relay. This IIN is only used when the state cannot be described by a combination of one or more of the other IIN bits.	No
7	Device restart	Set when the device software application restarts. This IIN is cleared when the master station explicitly writes a 0 into this bit of the Internal Indications object.	Yes
Octet 2			
0	Function code not implemented	The received function code is not implemented within the relay.	Yes
1	Requested object(s) unknown	The relay does not have the specified objects or there are no objects assigned to the requested class. This IIN should be used for debugging purposes and usually indicates a mismatch in device profiles or configuration problems.	Yes
2	Out of range	Parameters in the qualifier, range or data fields are not valid or out of range. This is a 'catch-all' for application request formatting errors. It should only be used for debugging purposes. This IIN usually indicates configuration problems.	Yes
3	Buffer overflow	Event buffer(s), or other application buffers, have overflowed. The master station should attempt to recover as much data as possible and indicate to the user that there may be lost data. The appropriate error recovery procedures should be initiated by the user.	Yes
4	Already executing	The received request was understood but the requested operation is already executing.	
5	Bad configuration	Set to indicate that the current configuration in the relay is corrupt. The master station may download another configuration to the relay.	Yes
6	Reserved	Always returned as zero.	
7	Reserved	Always returned as zero.	

24.11.3.8.4 DNP3 RESPONSE STATUS CODES

When the device processes Control Relay Output Block (Object 12) requests, it returns a set of status codes; one for each point contained within the original request. The complete list of codes appears in the following table:

Code Number	Identifier Name	Description
0	Success	The received request has been accepted, initiated, or queued.
1	Timeout	The request has not been accepted because the 'operate' message was received after the arm timer (Select Before Operate) timed out. The arm timer was started when the select operation for the same point was received.
2	No select	The request has not been accepted because no previous matching 'select' request exists. (An 'operate' message was sent to activate an output that was not previously armed with a matching 'select' message).
3	Format error	The request has not been accepted because there were formatting errors in the control request ('select', 'operate', or 'direct operate').
4	Not supported	The request has not been accepted because a control operation is not supported for this point.
5	Already active	The request has not been accepted because the control queue is full or the point is already active.
6	Hardware error	The request has not been accepted because of control hardware problems.
7	Local	The request has not been accepted because local access is in progress.
8	Too many operations	The request has not been accepted because too many operations have been requested.
9	Not authorised	The request has not been accepted because of insufficient authorisation.
127	Undefined	The request not been accepted because of some other undefined reason.

Note:
Code numbers 10 through to 126 are reserved for future use.

24.11.3.8.5 DNP3 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `DNP3.0`.
4. Move down to the next cell (***RP1 Address***). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the Relay Address. It is important that no two IEDs have the same address.
5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps and 38400 bps. Make sure that the baud rate selected on the IED is the same as that set on the master station.
6. Move down to the next cell (***RP1 Parity***). This cell controls the parity format used in the data frames. The parity can be set to be one of `None`, `Odd` or `Even`. Make sure that the parity format selected on the IED is the same as that set on the master station.
7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
8. Move down to the next cell (***RP1 Time Sync***). This cell affects the time synchronisation request from the master by the IED. It can be set to `enabled` or `disabled`. If enabled, it allows the DNP3.0 master to synchronise the time on the IED.

24.11.3.8.5.1 DNP3 CONFIGURATOR

A PC support package for DNP3.0 is available as part of the supplied settings application software (MiCOM S1 Agile) to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new

DNP3.0 configuration takes effect after the download is complete. To restore the default configuration at any time, from the *CONFIGURATION* column, select the ***Restore Defaults*** cell then select `All Settings`.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

If the device supports DNP Over Ethernet, the configuration related settings are done in the folder **DNP Over Ethernet**.

24.11.4 IEC 61850

This section describes how the IEC 61850 standard is applied to GE Vernova products. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 61850 standard.

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security that is so essential in substations today.

This product supports IEC 61850 Edition 2 and Edition 2.1 only.

24.11.4.1 BENEFITS OF IEC 61850

The standard provides:

- Standardised models for IEDs and other equipment within the substation
- Standardised communication services (the methods used to access and exchange data)
- Standardised formats for configuration files
- Peer-to-peer communication

The standard adheres to the requirements laid out by the ISO OSI model and therefore provides complete vendor interoperability and flexibility on the transmission types and protocols used. This includes mapping of data onto Ethernet, which is becoming more and more widely used in substations, in favour of RS485. Using Ethernet in the substation offers many advantages, most significantly including:

- Ethernet allows high-speed data rates (currently 100 Mbps, rather than tens of kbps or less used by most serial protocols)
- Ethernet provides the possibility to have multiple clients
- Ethernet is an open standard in everyday use
- There is a wide range of Ethernet-compatible products that may be used to supplement the LAN installation (hubs, bridges, switches)

24.11.4.2 IEC 61850 INTEROPERABILITY

A major benefit of IEC 61850 is interoperability. IEC 61850 standardises the data model of substation IEDs, which allows interoperability between products from multiple vendors.

An IEC 61850-compliant device may be interoperable, but this does not mean it is interchangeable. You cannot simply replace a product from one vendor with that of another without reconfiguration. However, the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able to integrate a new device very quickly without having to map all the new data. IEC 61850 brings improved substation communications and interoperability to the end user, at a lower cost.

24.11.4.3 THE IEC 61850 DATA MODEL

The data model of any IEC 61850 IED can be viewed as a hierarchy of information, whose nomenclature and categorisation is defined and standardised in the IEC 61850 specification.

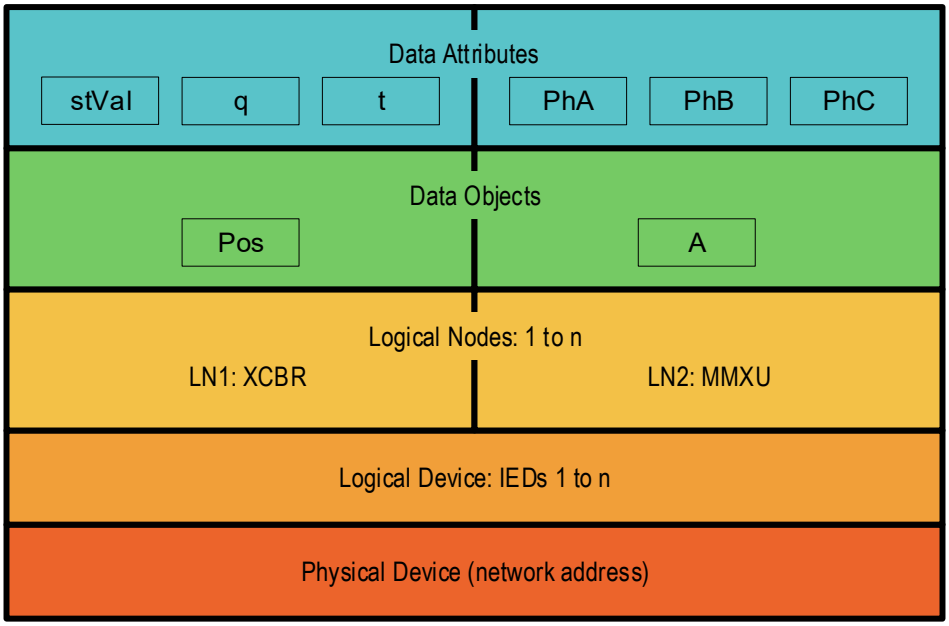


Figure 421: Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

Data frame format

Layer	Description
Physical Device	Identifies the actual IED within a system. Typically, the device's name or IP address can be used (for example Feeder_1 or 10.0.0.2.
Logical Device	Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM IEDs, multiple Logical Devices exist, for System (root LD) and various Control, Measurements, Protection, and Records LDs.
Wrapper/Logical Node Instance	Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
Data Object	This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR.
Data Attribute	This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR.

24.11.4.4 IEC 61850 IN MICOM P40 IEDS

IEC 61850 is implemented by use of a separate Ethernet board. This Ethernet board manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection functions.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a bay computer (MiCOM C264)
- An HMI
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge of the IED

The IEC 61850 compatible interface standard provides capability for the following:

- Read access to measurements
- Refresh of all measurements at a standard rate.
- Generation of non-buffered and buffered multi-client reports on change of status or measurement
- SNTP time synchronisation over an Ethernet link. (This is used to synchronise the IED's internal real time clock.
- GOOSE peer-to-peer communication
- Disturbance record extraction by IEC 61850 MMS file transfer. The record is extracted as an ASCII format COMTRADE file
- Controls (Direct and Select Before Operate)

Note:
Setting changes are not supported in the current IEC 61850 implementation. Currently these setting changes are carried out using the settings application software.

24.11.4.5 IEC 61850 DATA MODEL IMPLEMENTATION

The data model naming adopted in the IEDs has been standardised for consistency. The Logical Nodes are allocated under Logical Devices, as appropriate.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available as a separate document.

24.11.4.6 IEC 61850 COMMUNICATION SERVICES IMPLEMENTATION

The IEC 61850 communication services which are implemented in the IEDs are described in the Protocol Implementation Conformance Statement (PICS) document, which is available as a separate document.

24.11.4.7 IEC 61850 PEER-TO-PEER (GOOSE) COMMUNICATIONS

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) enables faster communication between IEDs offering the possibility for a fast and reliable system-wide distribution of input and output data values. The GOOSE model uses multicast services to deliver event information. Multicast messaging means that messages are sent to selected devices on the network. The receiving devices can specifically accept frames from certain devices and discard frames from the other devices. It is also known as a publisher-subscriber system. When a device detects a change in one of its monitored status points it publishes a new message. Any device that is interested in the information subscribes to the data it contains.

24.11.4.8 GOOSE MESSAGE VALIDATION

Whenever a new GOOSE message is received its validity is checked before the dataset is decoded and used to update the Programmable Scheme Logic. As part of the validation process a check is made for state and sequence number anomalies. If an anomaly is detected, the 'out-of-order' GOOSE message is discarded. When a message is discarded the last valid message remains active until a new valid GOOSE message is received or its validity period (TAL) expires.

Out-of-order GOOSE message indicators and reporting are provided to the subscriber via the IEC 61850 LGOS logical node.

24.11.4.9 MAPPING GOOSE MESSAGES TO VIRTUAL INPUTS

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

An IED can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

24.11.4.10 IEC 61850 GOOSE CONFIGURATION

All GOOSE configuration is performed using the IEC 61850 Configurator tool available in the MiCOM S1 Agile software application.

All GOOSE publishing configuration can be found under the **GOOSE Publishing** tab in the configuration editor window. All GOOSE subscription configuration parameters are under the **External Binding** tab in the configuration editor window.

Settings to enable GOOSE signalling and to apply Test Mode are available using the HMI.

24.11.4.11 ETHERNET FUNCTIONALITY

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association and terminate any which are no longer active.

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

24.11.4.12 IEC 61850 CONFIGURATION

To configure the MiCOM P40 IED for IEC 61850, it is necessary to use the IEC 61850 IED Configurator software tool, which is part of the MiCOM S1 Agile settings application software.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IEDs system configuration capabilities are determined from an IED Capability Description file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and test (using simulation tools), a substation's entire protection scheme before the products are installed into the substation.

To help with this process, the S1 Agile provides an IEC 61850 IED Configurator tool, which allows the pre-configured IEC 61850 configuration file (SCL format) to be imported. The Ethernet and IEC 61850 configuration is transferred to the IED as a MCL file. As well as this, you can manually create MCL configuration files for all products, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

Note:
Some configuration data is available in the IEC61850 CONFIG. column, allowing read-only access to basic configuration data.

24.11.4.12.1 IEC 61850 CONFIGURATION BANKS

There are two configuration banks:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the IED as an MCL file is automatically stored in the Inactive Configuration Bank, therefore not immediately affecting the current configuration.

Following this, the IEC 61850 IED Configurator tool can be used to transmit a command, which authorises activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the *IEC61850 CONFIG.* column of the HMI.

The SCL Name and Revision attributes of both configuration banks are available in the *IEC61850 CONFIG.* column of the HMI.

24.11.4.12.2 IEC 61850 NETWORK CONNECTIVITY

Configuration of the IP parameters and SNTP (Simple Network Time Protocol) time synchronisation parameters is performed by the IEC 61850 Configurator tool. If these parameters are not available using an SCL (Substation Configuration Language) file, they must be configured manually.

Every IP address on the Local Area Network must be unique. Duplicate IP addresses result in conflict and must be avoided. Most IEDs check for a conflict on every IP configuration change and at power up and they raise an alarm if an IP conflict is detected.

The IED can be configured to accept data from other networks using the ***Gateway*** setting. If multiple networks are used, the IP addresses must be unique across networks.

24.11.4.13 IEC 61850 EDITION 2

Many parts of the IEC 61850 standard have now been released as the second edition. This offers some significant enhancements including:

- Improved interoperability
- Many new logical nodes
- Better defined testing: it is now possible to perform off-line testing and simulation of functions

Edition 2 implementation requires use of version 3.8 of the IEC 61850 configurator, which is installed with version 2.0.1 of MiCOM S1 Agile.

24.11.4.13.1 BACKWARD COMPATIBILITY

IEC 61850 system - backward compatibility

An Edition 1 IED can operate with an Edition 2 IEC 61850 system, provided that the Edition 1 IEDs do not subscribe to GOOSE messages with data objects or data attributes which are only available in Edition 2.

The following figure explains this concept:

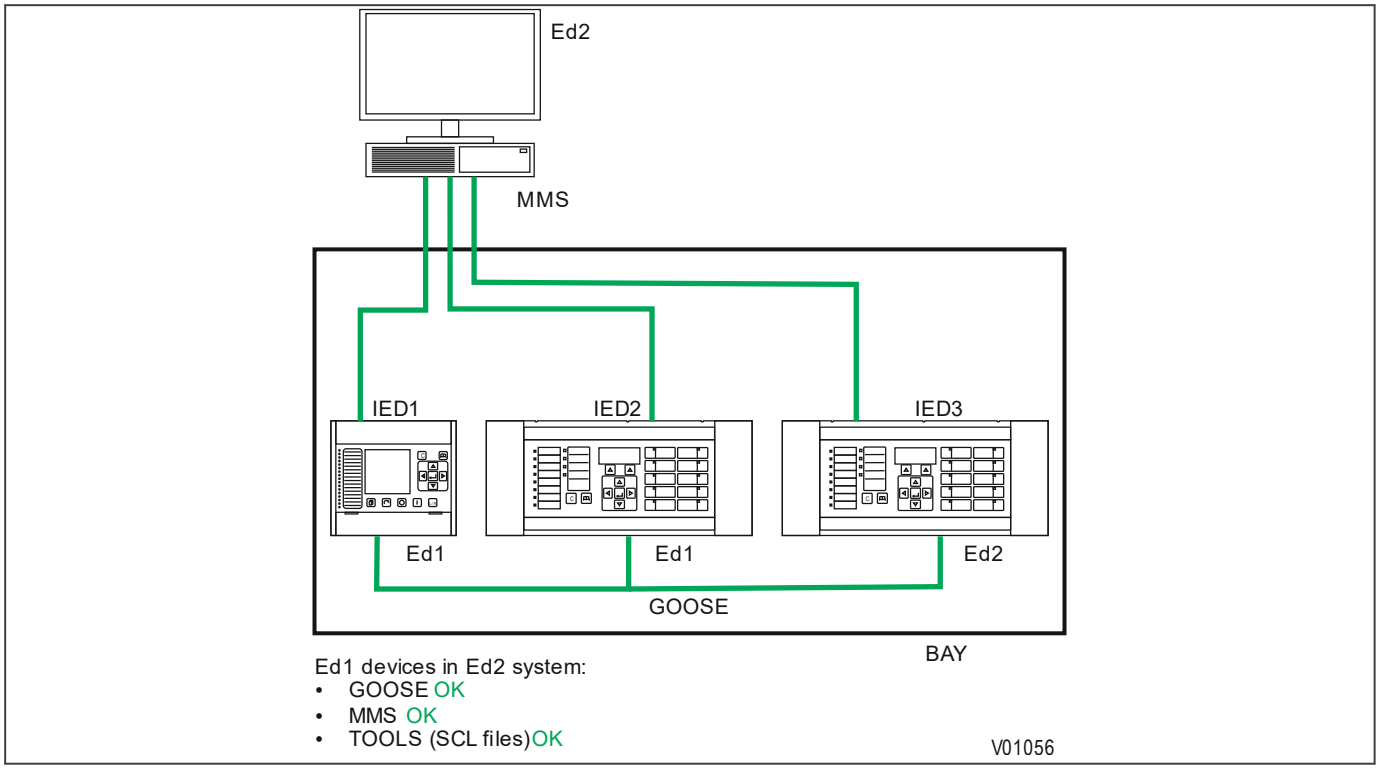


Figure 422: Edition 2 system - backward compatibility

An Edition 2 IED cannot normally operate within an Edition 1 IEC 61850 system. An Edition 2 IED can work for GOOSE messaging in a mixed system, providing the client is compatible with Edition 2.

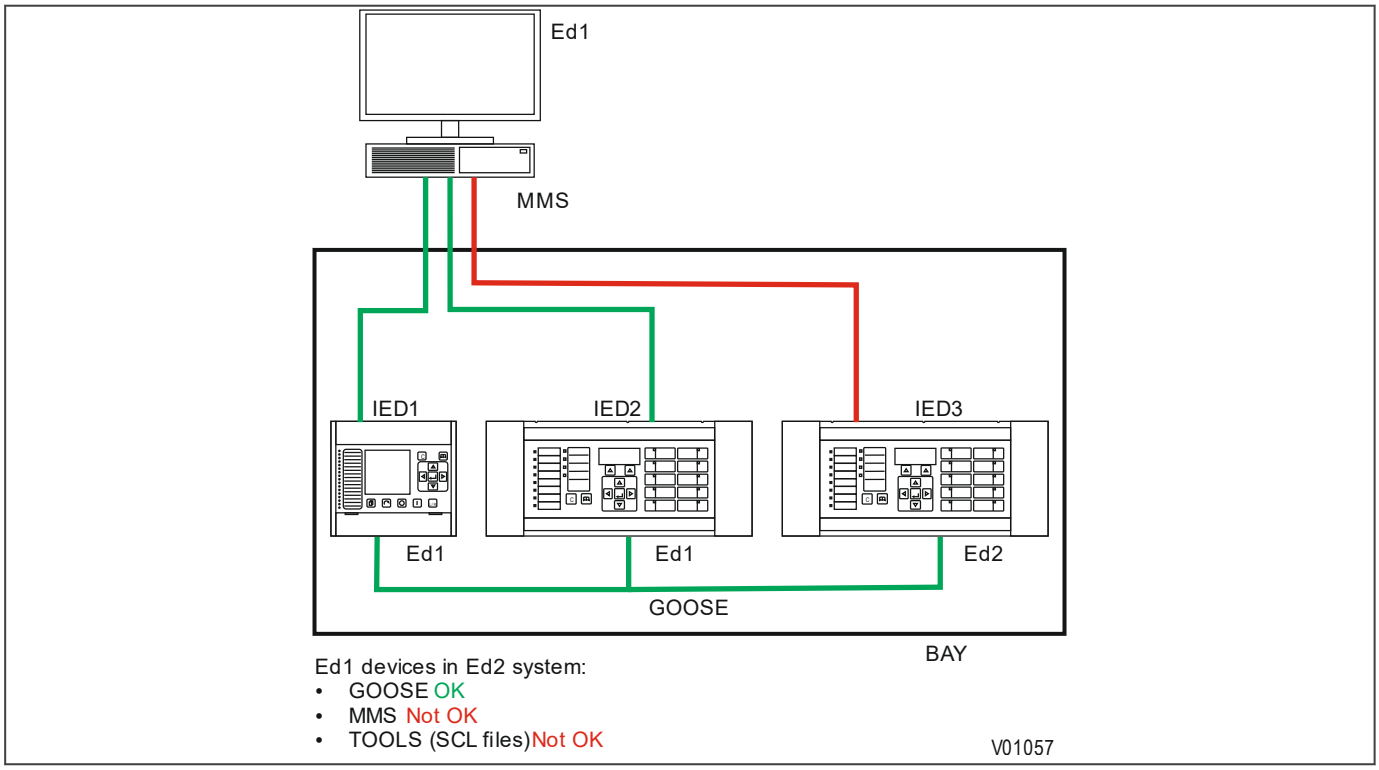


Figure 423: Edition 1 system - forward compatibility issues

24.11.4.13.2 EDITION-2 COMMON DATA CLASSES

The following common data classes (CDCs) are new to Edition 2 and therefore should not be used in GOOSE control blocks in mixed Edition 1 and Edition 2 systems

- Histogram (HST)
- Visible string status (VSS)
- Object reference setting (ORG)
- Controllable enumerated status (ENC)
- Controllable analogue process value (APC)
- Binary controlled analogue process value (BAC)
- Enumerated status setting (ENG)
- Time setting group (TSG)
- Currency setting group (CUG)
- Visible string setting (VSG)
- Curve shape setting (CSG)

Of these, only ENS and ENC types are available from a MiCOM P40 IED when publishing GOOSE messages, so Data Objects using these Common Data Classes should not be published in mixed Edition 1 and Edition 2 systems.

For compatibility between Edition 1 and Edition 2 IEDs, SCL files using SCL schema version "2.1" must be used. For a purely Edition 2 system, use the schema version "2007B4".

24.11.5 READ ONLY MODE

With IEC 61850 and Ethernet/Internet communication capabilities, security has become an important issue. For this reason, all relevant GE Vernova IEDs have been adapted to comply with the latest cyber-security standards.

In addition to this, a facility is provided which allows you to enable or disable the communication interfaces. This feature is available for products using Courier, IEC 60870-5-103, or IEC 61850.

24.11.5.1 IEC 60870-5-103 PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with IEC 60870-5-103, the following commands are blocked at the interface:

- Write parameters (=change setting) (private ASDUs)
- General Commands (ASDU20), namely:
    - INF16 auto-recloser on/off
    - INF19 LED reset
    - Private INFs (for example: CB open/close, Control Inputs)

The following commands are still allowed:

- Poll Class 1 (Read spontaneous events)
- Poll Class 2 (Read measurands)
- GI sequence (ASDU7 'Start GI', Poll Class 1)

- Transmission of Disturbance Records sequence (ASDU24, ASDU25, Poll Class 1)
- Time Synchronisation (ASDU6)
- General Commands (ASDU20), namely:
    - INF23 activate characteristic 1
    - INF24 activate characteristic 2
    - INF25 activate characteristic 3
    - INF26 activate characteristic 4

Note:
For IEC 60870-5-103, Read Only Mode function is different from the existing Command block feature.

24.11.5.2 COURIER PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with Courier, the following commands are blocked at the interface:

- Write settings
- All controls, including:
    - Reset Indication (Trip LED)
    - Operate Control Inputs
    - CB operations
    - Auto-reclose operations
    - Reset demands
    - Clear event/fault/maintenance/disturbance records
    - Test LEDs & contacts

The following commands are still allowed:

- Read settings, statuses, measurands
- Read records (event, fault, disturbance)
- Time synchronisation
- Change active setting group

24.11.5.3 IEC 61850 PROTOCOL BLOCKING

If Read-Only Mode is enabled for the Ethernet interfacing with IEC 61850, the following commands are blocked at the interface:

- All controls, including:
    - Enable/disable protection
    - Operate Control Inputs
    - CB operations (Close/Trip, Lock)
    - Reset LEDs

The following commands are still allowed:

- Read statuses, measurands
- Generate reports
- Extract disturbance records
- Time synchronisation
- Change active setting group

24.11.5.4 READ-ONLY SETTINGS

The following settings are available for enabling or disabling Read Only Mode.

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

24.11.5.5 READ-ONLY DDB SIGNALS

The remote read only mode is also available in the PSL using three dedicated DDB signals:

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

Using the PSL, these signals can be activated by opto-inputs, Control Inputs and function keys if required.

24.12 TIME SYNCHRONISATION

Effective management of today's energy systems requires precise time recording of events experienced by different devices across the network. This is achieved by synchronising real-time clocks across the devices and can be achieved in different ways. This device supports synchronisation in various ways depending on the chosen options and communication protocols.

- Using the IRIG-B input (if fitted)
- Using the SNTP time protocol (for Ethernet IEC 61850 versions)
- Using IEEE 1588 Precision Time Protocol (PTP)
- By using the time synchronisation functionality inherent in the data protocols
- Using a dedicated opto-input mapped via the PSL

The time synchronisation sources can be configured in a priority order using the Primary Source and Secondary Source cells in the DATE AND TIME column. If the Primary source becomes unavailable, the Secondary source will be used, if available.

All the protection functionality implemented in this device operates entirely independently of the real time clock. It does not matter to the protection if the clock is not set or is incorrectly synchronised. Even though the time stamping of any associated records may be compromised, the protection functionality will not.

24.12.1 IRIG-B

IRIG stands for Inter Range Instrumentation Group, which is a standards body responsible for standardising different time code formats. There are several different formats starting with IRIG-A, followed by IRIG-B and so on. The letter after the "IRIG" specifies the resolution of the time signal in pulses per second (PPS). IRIG-B, the one which we use has a resolution of 100 PPS. IRIG-B is used when accurate time-stamping is required.

The following diagram shows a typical GPS time-synchronised substation application. The satellite RF signal is picked up by a satellite dish and passed on to receiver. The receiver receives the signal and converts it into time signal suitable for the substation network. IEDs in the substation use this signal to govern their internal clocks and event recorders.

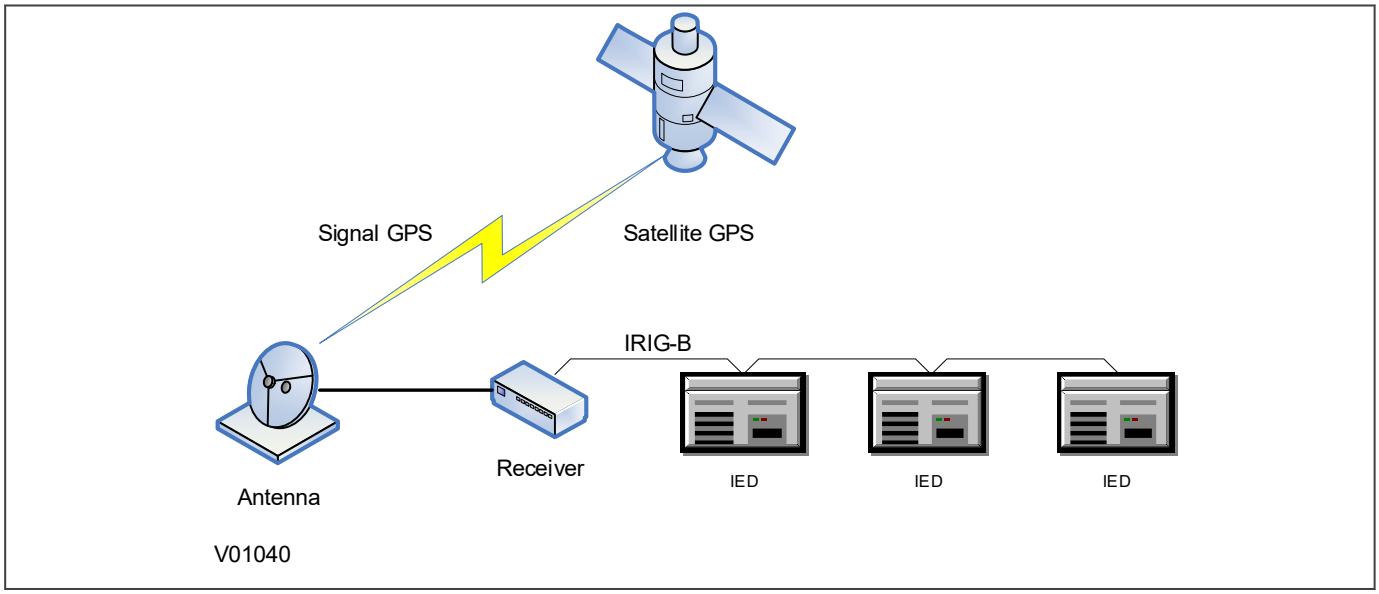


Figure 424: GPS satellite timing signal

The IRIG-B time code signal is a sequence of one second time frames. Each frame is split up into ten 100 mS slots as follows:

- Time-slot 1: Seconds
- Time-slot 2: Minutes
- Time-slot 3: Hours
- Time-slot 4: Days
- Time-slot 5 and 6: Control functions
- Time-slots 7 to 10: Straight binary time of day

The first four time-slots define the time in BCD (Binary Coded Decimal). Time-slots 5 and 6 are used for control functions, which control deletion commands and allow different data groupings within the synchronisation strings. Time-slots 7-10 define the time in SBS (Straight Binary Second of day).

24.12.1.1 IRIG-B IMPLEMENTATION

Depending on the chosen hardware options, the product can be equipped with an IRIG-B input for time synchronisation purposes. The IRIG-B interface is implemented either on a dedicated board, or together with other communication functionality such as Ethernet. The IRIG-B interface connector is a BNC connector. IRIG-B signals are usually presented as an RF-modulated signal. The boards support universal IRIG-B, which means they accept demodulated or modulated IRIG-B.

To set the device to use IRIG-B, use the setting ***IRIG-B Sync*** cell in the *DATE AND TIME* column.

The IRIG-B status can be viewed in the ***IRIG-B Status*** cell in the *DATE AND TIME* column.

24.12.2 SNTP

SNTP is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. SNTP can be used as the time synchronisation method for models using IEC 61850 over Ethernet. A time synchronisation accuracy of within 5 ms is possible.

The device is synchronised by the main SNTP server. This is achieved by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software described in the settings application software manual. A second server is also configured with a different IP address for backup purposes.

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. This could be because there is no response or no valid clock signal.

The HMI menu does not contain any configurable settings relating to SNTP, as the only way to configure it is using the IEC 61850 Configurator. However, it is possible to view some parameters in the *COMMUNICATIONS* column under the sub-heading SNTP parameters. Here you can view the SNTP server addresses and the SNTP poll rate in the cells ***SNTP Server 1***, ***SNTP Server 2*** and ***SNTP Poll rate*** respectively.

The SNTP time synchronisation status is displayed in the ***SNTP Status*** cell in the *DATE AND TIME* column.

24.12.2.1 LOSS OF SNTP SERVER SIGNAL ALARM

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. It is issued when the SNTP sever has not detected a valid time synchronisation response within its 5 second window. This is because there is no response or no valid clock. The alarm is mapped to IEC 61850.

24.12.3 IEEE 1588 PRECISION TIME PROTOCOL

The MiCOM P40 modular products support IEEE 1588 Precision Time Protocol (PTP) as a slave-only clock. MiCOM relays are profile unaware, which means that they will accept synchronisation from any PTP profile. Power Utility Profile (IEC 61850-9-3) is specifically designed to perform well for substation related applications, with PMU applications needing the most stringent requirements.

PTP can be used to replace or supplement IRIG-B and SNTP time synchronisation so that the IED can be synchronised using Ethernet messages from the substation LAN without any additional physical connections being required.

A dedicated DDB signal (***PTP Failure***) is provided to indicate failure of PTP.

24.12.3.1 ACCURACY AND DELAY CALCULATION

A time synchronisation accuracy of within 3 ms is possible. Both peer-to-peer or end-to-end mode delay measurement can be used.In peer-to-peer mode, delays are measured between each link in the network and are compensated for. This provides greater accuracy but requires that every device between the Grand Master and Slaves supports the peer-to-peer delay measurement.

In end-to-end mode, delays are only measured between each Grand Master and Slave. The advantage of this mode is that the requirements for the switches on the network are lower; they do not need to independently calculate delays. The main disadvantage is that more inaccuracy is introduced, because the method assumes that forward and reverse delays are always the same, which may not always be correct.

When using end-to-end mode, the IED can be connected in a ring or line topology using RSTP or Self-Healing Protocol without any additional Transparent Clocks. But because the IED is a slave-only device, additional inaccuracy is introduced. The additional error will be less than 1ms for a network of eight devices.

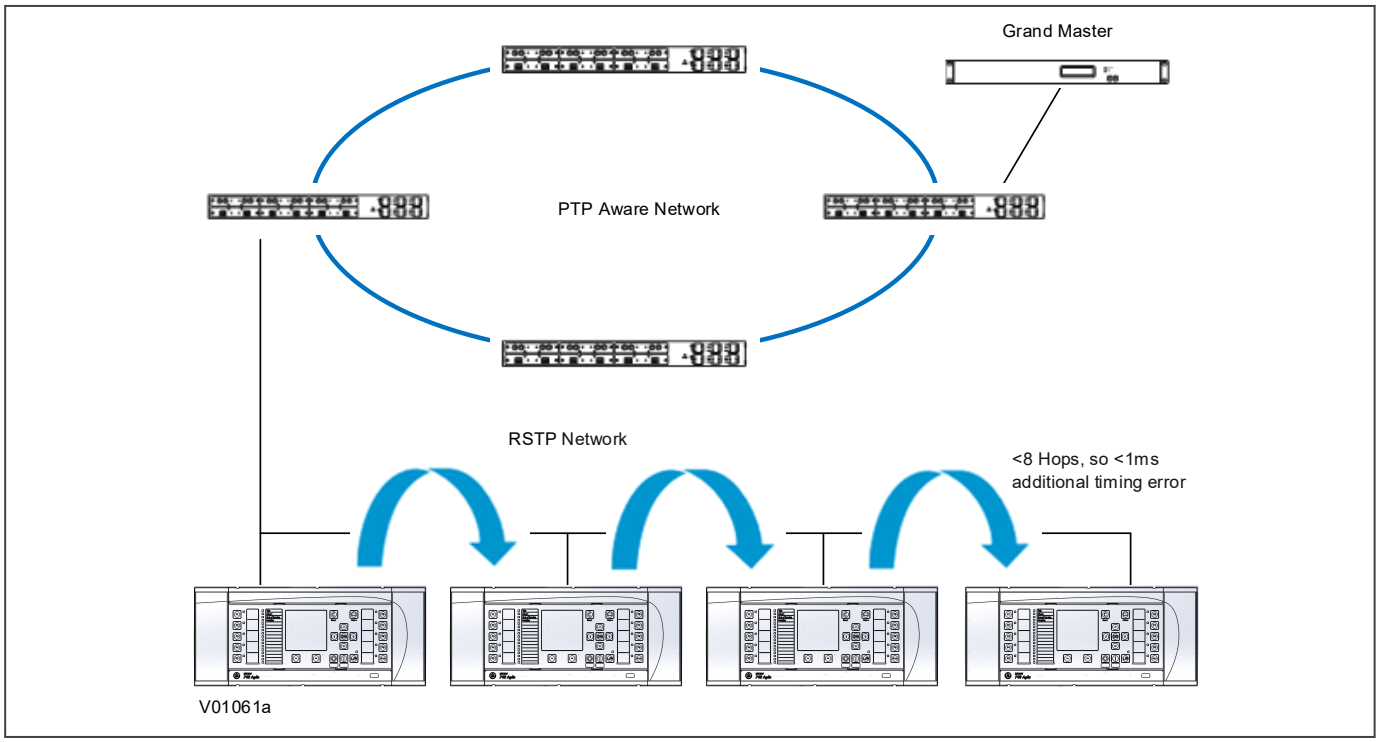


Figure 425: Timing error using ring or line topology

24.12.3.2 PTP DOMAINS

PTP traffic can be segregated into different domains using Boundary Clocks. These allow different PTP clocks to share the same network while maintaining independent synchronisation within each grouped set.

The PTP domain number can be configured in MiCOM P40 modular products using the ***Domain Number*** cell in the *DATE AND TIME* column. The domain number needs to be configured to match the domain of the local network.

24.12.4 TIME SYNCHRONISATION USING THE COMMUNICATION PROTOCOLS

All communication protocols have in-built time synchronisation mechanisms. If an external time synchronisation mechanism such as IRIG-B, SNTP, or IEEE 1588 PTP is not used to synchronise the devices, the time synchronisation mechanism within the relevant serial protocol is used. The real time is usually defined in the master station and communicated to the relevant IEDs via one of the rear serial ports using the chosen protocol. It is also possible to define the time locally using settings in the *DATE AND TIME* column.

The time synchronisation for each protocol is described in the relevant protocol description section.

24.12.5 REAL TIME CLOCK SYNCHRONISATION VIA OPTO-INPUTS

In modern protective schemes it is often desirable to synchronise the IED's real time clock so that events from different IEDs can be placed in chronological order. This can be done using the IRIG-B input, if fitted, or via the communication interface connected to the substation control system. In addition to these methods P40 IEDs offer the facility to synchronise via an opto-input by routing it in PSL to DDB 400 (***Time Sync.***). Pulsing this input results in the real time clock snapping to the nearest minute. The recommended pulse duration is 20 ms to be repeated no more than once per minute. An example of the time sync. function is shown.

IRIG-B Interface (Demodulated)	
Time of "Sync. Pulse"	**Corrected Time**
19:47:00 to 19:47:29	19:47:00
19:47:30 to 19:47:59	19:48:00

Note:
The above assumes a time format of hh:mm:ss.

To avoid the event buffer from being filled with unnecessary time sync. events, it is possible to ignore any event that is generated by the time sync. opto input. This can be done by applying the following settings:

Menu Text	Value
RECORD CONTROL	
Opto Input Event	Enabled
Protection Event	Enabled
DDB 63 - 32 (Opto Inputs)	Set "Time Sync." associated opto to 0

To improve the recognition time of the time sync. opto input by approximately 10 ms, the opto input filtering could be disabled. This is achieved by setting the appropriate bit to 0 in the ***Opto Filter Cntl.*** cell (*OPTO CONFIG.* column). Disabling the filtering may make the opto input more susceptible to induced noise. Fortunately the effects of induced noise can be minimised by using the methods described in the Software Design chapter.

CHAPTER 25

CYBERSECURITY

25.1 DISCLAIMER

GE Vernova Grid Automation products are digital devices designed to be installed and operated in utility substations & industrial plant environments and connected to secure private networks. GE Vernova IEDs should not be connected to the public internet.

GE Vernova strongly recommends that users protect their digital devices using a defense-in-depth strategy which will protect their products, their network, their systems and interfaces against cyber security threats. This includes, but is not limited to, placing digital devices inside the control system network security perimeter, deploying and maintaining access controls, monitoring and intrusion detection, security awareness training, security policies, network segmentation and firewalls installation, strong and active password management, data encryption, antivirus and other mitigating applicable technologies.

GE Vernova IEDs are available with standard features, and in some products additional optional software options, which provide cyber security mechanisms to help users protect against cyber security intrusion. GE Vernova strongly recommends using all available cyber security options.

For additional details and recommendations on how to protect the GE Vernova IEDs, please see Cyber Security sections of the manuals. GE Vernova Grid Automation may also provide additional instructions and recommendations to users from time to time relating to IED and cyber security threats or vulnerabilities.

It is the users' sole responsibility to make sure that all GE Vernova Grid Automation IEDs are installed and operated considering its cyber security capabilities, security context, and the instructions and recommendations provided to the user relating to GE Vernova. Users assume all risks and liability associated with damages or losses incurred in connection with any and all cyber security incidences.

IT IS THE SOLE RESPONSIBILITY OF THE USER TO SECURE THEIR NETWORK AND ASSOCIATED DEVICES AGAINST CYBER SECURITY INTRUSIONS OR ATTACKS. GE VERNOVA GRID AUTOMATION AND ITS AFFILIATES ARE NOT LIABLE FOR ANY DAMAGES AND/OR LOSSES ARISING FROM OR RELATED TO SUCH SECURITY INTRUSION OR ATTACKS.

25.2 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were often proprietary.

For these reasons, the substation environment was very secure against cyber-attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it cannot be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them).

However, note that these are not recognised defences against attackers.

The increasing sophistication of protection schemes, coupled with the advancement of technology and the desire for vendor interoperability, has resulted in standardisation of networks and data interchange within substations. Today, devices within substations use standardised protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardised protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for our range of Intelligent Electronic Devices (IEDs).

Note:
Cyber-security compatible devices do not enforce NERC compliance, they merely facilitate it. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary.

This chapter contains the following sections:

Disclaimer 721
Overview 722
The Need for Cybersecurity 723
Standards 724
Cyber-Security Implementation 728
Roles and Permissions 729
User Authentication 732
SNMP Configuration 749
Returning The IED To Factory 750
Security Event Management 751

25.3 THE NEED FOR CYBERSECURITY

Cybersecurity provides protection against unauthorised disclosure, transfer, modification, or destruction of information or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorised access to information)
- Integrity (preventing unauthorised modification)
- Availability/Authentication (preventing the denial of service and assuring authorised access to information)
- Non-repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyse incidents)

The threats to Cybersecurity may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber-attacks by hackers).

Good Cybersecurity can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (users keep passwords on their computer)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Bypassing of controls (users turn off security measures)
- Inadequate technology (substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate preventing access to equipment

To help tackle these issues, standards organisations have produced various standards. Compliance with these standards significantly reduces the threats associated with lack of Cybersecurity.

25.4 STANDARDS

There are several standards, which apply to substation cyber-security. The standards currently applicable to Grid Automation Systems and IEDs are NERC and IEEE1686.

Standard	Country	Description
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber-security capabilities
IEC 62351	International	Power systems management and associated information exchange - Data and communications security
IEC 62443	International	Security for industrial automation and control systems
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber-security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

25.4.1 NERC COMPLIANCE

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of 'Critical Cyber Assets', which control or have an influence on the reliability of North America’s electricity generation and distribution systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

NERC CIP standards

CIP Standard	Description
CIP-002 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005 Electronic Security	Define and document logical security perimeters where Critical Cyber Assets reside. Define and document measures to control access points and monitor electronic access
CIP-006 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside
CIP-007 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets
CIP-008 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber-security Incidents relating to Critical Cyber Assets are identified

CIP Standard	Description
CIP-009 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

25.4.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up

Power Utility Responsibilities	GE Vernova's Contribution
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

25.4.1.2 CIP 003

CIP 003 requires the implementation of a Cybersecurity policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

Power Utility Responsibilities	GE Vernova's Contribution
To create a Cybersecurity policy	We can help the power utilities to have access control to its critical assets by providing centralised Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

25.4.1.3 CIP 004

CIP 004 requires that personnel with authorised cyber access or authorised physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power Utility Responsibilities	GE Vernova's Contribution
To provide appropriate training of its personnel	We can provide Cybersecurity training

25.4.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power Utility Responsibilities	GE Vernova's Contribution
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED

25.4.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power Utility Responsibilities	GE Vernova's Contribution
Provide physical security controls and perimeter monitoring Ensure that people who have access to critical cyber assets don't have criminal records	GE Vernova cannot provide additional help with this aspect

25.4.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring

Power Utility Responsibilities	GE Vernova's Contribution
To provide an incident response team and have appropriate processes in place	Test procedures, we can provide advice and help on testing. Ports and services, our devices can disable unused ports and services Security patch management, we can provide assistance Antivirus, we can provide advise and assistance Account management, we can provide advice and assistance Monitoring, our equipment monitors and logs access

25.4.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power Utility Responsibilities	GE Vernova's Contribution
To provide an incident response team and have appropriate processes in place.	GE Vernova Vernova cannot provide additional help with this aspect.

25.4.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power Utility Responsibilities	GE Vernova's Contribution
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

25.4.2 IEEE 1686-2013

IEEE 1686-2013 is an IEEE Standard for substation IEDs' Cybersecurity capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.

- The audit trail is recorded, listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

25.5 CYBER-SECURITY IMPLEMENTATION

GE Vernova IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

MiCOM 5th Generation P40 products provide enhanced security through the following features:

- An Authentication, Authorisation, Accounting (AAA) Remote Authentication Dial-In User Service (RADIUS) client that is managed centrally, enables user attribution, provides accounting of all user activities, and uses secure standards based on strong cryptography for authentication and credential protection. In other words, this option uses a RADIUS.
- Server for user authentication. There is provision for both remote (RADIUS) and local (device) authentication.
- A Role-Based Access Control (RBAC) system in line with IEC 62351-8:2020 that provides a permission model that allows access to the device operations and configurations based on specific roles and individual user accounts configured on the AAA server.
- Security event reporting through both proprietary security event log (separate from the main events file) and the Syslog and SNMP protocols for supporting Security Information Event Management (SIEM) systems for centralised cybersecurity monitoring.
- Encryption of passwords - stored within the IED, in network messages between the MiCOM S1 Agile software and the IED, and in network messages between the RADIUS server and the IED (subject to the RADIUS server configuration).
- Secure firmware upgrade process.

25.5.1 INITIAL SETUP: DEFAULT USERNAMES AND DEFAULT PASSWORDS

The requirements for initial setup of the IED for cyber-security and RBAC will depend on:

1. which interfaces, if any, the cyber-security is required,
2. the intended authentication method, as defined in the setting ***Auth. Method*** in *SECURITY CONFIG* column (see the Authentication Methods section).

When the authentication method is configured as `Device Only`, there are four pre-defined profiles.

User Name	Default Password	IEC 62351-8 Roles
ADMIN1	ChangeMe1#	SECADM
RBACMNT1	ChangeMe2#	RBACMNT
ENGG1	ChangeMe3#	ENGINEER
VIEWER1	ChangeMe4#	VIEWER

During the first logon, it is Mandatory to change the Default Passwords, and the IED or MiCOM S1 Agile software will prompt the user to change it. The new password must comply with the strength defined by the Password Policy setting, detailed in the ***Password Policy*** section of this chapter.

When the authentication method is configured as ‘Server + Device’, and authentication using RADIUS is required, users must be set up on the RADIUS server (see the RADIUS users section). These users are separate from the pre-defined Device users. RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication (see the RADIUS server settings section). It is recommended that the RADIUS shared secret be changed from the default (see the RADIUS client-server validation section).

25.6 ROLES AND PERMISSIONS

25.6.1 ROLES

The P40 Agile products supports all the mandatory pre-defined roles as per IEC 62351-8:2020.

IEC 62351-8 Roles	Value
VIEWER	0
OPERATOR	1
ENGINEER	2
INSTALLER	3
SECADM	4
SECAUD	5
RBACMNT	6

Individual user accounts can be configured to have one or more of these roles.

- VIEWER: Can view all values and settings
- OPERATOR: Can view values and perform control operations
- ENGINEER: Can view values, and change settings of the device
- INSTALLER: Specific role required to perform firmware updates
- SECADM: Security Administrator - Can edit/modify Users and roles and configure security settings
- SECAUD: Security Auditor - Can view Security Log files
- RBACMNT: RBAC Management can change role to permission assignment

Only one role of one type is allowed to be logged in at a time from any interface. For example, one Operator can be logged in but not a second Operator at the same time from any other interface. This prevents subsets of settings from being changed at the same time.

25.6.2 PERMISSIONS

Authentication and authorisation are two different processes. An authenticated user cannot perform any action on the IED unless a privilege has been explicitly granted to them. This is the concept of “least privileges” access.

Privileges must be granted to users through roles. A role is a collection of privileges, and roles are granted to users. It is possible to have multiple roles for a user. The privilege/role matrix is stored on the IED. This is known as Role-Based-Access Control (RBAC).

On successful user authentication, the IED will load the user’s role list. If the user’s role changes, the user must logout and log back in to exercise his/her privileges.

The table below shows the predefined permissions assignment for the predefined Roles according to IEC 62351-8:2020

Value	Role Name (revision = 1)	Permission										
		LISTOBJECTS	READVALUES	DATASET	REPORTING	FILEREAD	FILEWRITE	FILEMNGT	CONTROL	CONFIG	SETTINGGROUP	SECURITY
<0>	VIEWER	C	C		X	C_1						
<1>	OPERATOR	X	X		X	C_1			X		X	
<2>	ENGINEER	X	X	X	X	X_1	X_1	X_1		X	X	
<3>	INSTALLER	X	X		X	X_2	X_2			X	X	
<4>	SECADM	X	X	X		X_4	X_4	X_4		X		X
<5>	SECAUD	X	X		X	X_3						
<6>	RBACMNT	X	X		X			X_4		X		
<7 ...32767>	Reserved	For future use of IEC defined roles.										
<-32768 .. -1>	Private	Defined by external agreement. Not guaranteed to be inoperable.										

C = Conditional read access, clarification of specific data objects may be necessary (e.g., VIEWER may not access security settings, but process values)
C_1 = Conditional read access to files of filetype data
X_1 = Access to files of type data and config
X_2 = Access to files of type config and firmware (updates)
X_3 = Access to files of type audit log
X_4 = Access to files of type security (config)

Note:
OPERATOR role is required for Alarm Acknowledgement and Function Key control.

The table below shows the predefined permissions description according to IEC 62351-8:2020

Permission	Description
LISTOBJECTS	Allows the subject/role to discover what objects are present within an IED by presenting the type and ID of those objects. If this permission is granted to a subject/role, the object for which the READVALUES permission has not been granted are not readable. This permission basically relates to all objects defined in IEC 61850 and allows a query on the existence of the data objects.
READVALUES	Allows the subject/role to obtain the values for all or some objects that are present within an IED in addition to the type and ID. This permission basically relates to all objects defined in IEC 61850 that provide a value and allows a read action on the actual values of the data objects.
DATASET	Allows the subject/role to have full service access (e.g., createDataSet, deleteDataSet) for both persistent and non-persistent DataSets.
REPORTING	Allows the subject/role to use buffered reporting as well as unbuffered reporting. Reporting relates to buffered and unbuffered report control blocks of a logical node.
FILEREAD	Allows the subject/role to perform read actions on file objects.
FILEWRITE	Allows the subject/role to perform write actions on file objects. This permission includes the FILEREAD permission.
CONTROL (group)	Allows the subject/role to perform control operations on all or some controllable objects that are present within an IED. Control services are for instance select or operate and relate to data objects defined in IEC 61850.
CONFIG	Allows the subject/role to locally or remotely configure all or some objects that are present within an IED. This relates to data attributes of the IEC 61850 functional constraints CF, DC and SP.

Permission	Description
SETTINGGROUP	Allows the subject/role to remotely configure SettingGroup control block. For example, this relates to the switching between different configured SettingGroups. SettingGroups also contains the IEC 61850 functional constraints SE.
FILEMNGT	Allows the subject/role to delete existing files on the IEDS.
SECURITY	Allows the subject/role to perform actions on all security related data objects, reportings, logs or files.

Specific product related permissions are listed in the tables below. Roles are mapped to Access Level definitions: A cross indicates that specific actions can be done by a user with the role allocated.

Extract Files	Role Name							
File Type	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Setting				X	X	X	X	X
PSL				X	X			
MCL (IEC 61850)				X	X			
DNP3				X	X			
SLD				X	X			
Events (operational)		X	X	X				
Security Events							X	
Disturbance Records		X	X	X				

Sending Files	Role Name							
File Type	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Setting				X	X	X		
PSL				X	X			
MCL (IEC 61850)				X	X			
DNP3				X	X			
SLD				X	X			
Menu Text				X	X			

25.7 USER AUTHENTICATION

25.7.1 AUTHENTICATION METHODS

The IED supports Bypass (no authentication), Device authentication and Server authentication.

Authentication Method	Description	User Interface
Bypass Auth.	IED does not provide security, any user (Local) can access the IED without logging in. IED does not validate user and password. In this case, there is no need to enter username and password to login. Bypass cannot be enabled on Rear Port 1, Rear Port 2 and Ethernet Ports.	Front Panel UI Front Port (USB port) (Local interfaces only)
Device Only	IED allows role access using local authentication.	Front Panel UI Front Port (USB port) Rear Port 1 Rear Port 2 Network Port 1 Network Port 2
Server + Device	IED uses RADIUS server authentication to validate the user first. And it allows fallback to device authentication if the RADIUS server(s) are unavailable.	Front Panel UI Front Port (USB port) Rear Port 1 Rear Port 2 Network Port 1 Network Port 2

If ***Bypass Auth.*** is enabled, the IED ignores the ***Auth. Method*** setting.

The ***Auth. Method*** setting offers the following options for user authentication:

- *Server + Device* (This is the default setting for IEDs with NIC (Ethernet Board) fitted)
- *Device Only* (This is the default setting for IEDs without NIC (Ethernet Board) fitted)

Only users with a SECADM role may change the ***Auth. Method*** setting. If the SECADM user changes it, the role remains logged in. Only when the user logs-out is their access-level revoked.

25.7.2 BYPASS

In ***Bypass Auth.*** mode, the IED does not provide user authentication - any user can login. IED does not validate user and password. The bypass security feature provides an easier access, with no authentication and encryption for situations when this is considered safe. Only users with SECADM role can enable Bypass mode. For this reason, it is recommended to always maintain at least one user with the SECADM role in the IED.

There are three modes for authentication bypass:

1. *Disabled* - no interfaces in ***Bypass Auth.*** mode (normal authentication is active)
2. *Local* - Bypass authentication when using Front Port and Front Panel
3. *Front Panel* - will bypass authentication Front Panel User Interface

Bypass Authentication for Bypass Mode:	Front Port	Front Panel UI
Disabled		
Local	X	X
Front Panel		X

The DDB signal ***Security Bypass*** is available to indicate that the IED is in ***Bypass Auth.*** mode.

The Front Panel UI will display "BYPASSED" at the top of the screen to indicate that the IED is in ***Bypass Auth***. mode.



25.7.3 LOGIN

A user can only login through the following methods:

- Front Panel User Interface
- Using MiCOM S1 Agile, connected to either the Front Port, Rear Port 1 or 2, or Ethernet Network Port 1 or 2.

A maximum of 20 characters username and 16 characters password are allowed for both device and RADIUS authentication from MiCOM S1 Agile.

25.7.3.1 FRONT PANEL LOGIN

Front panel User Interface supports both Device authentication and Server authentication. The P40 gives the user the option to enter the user credentials via UI panel. To access the Login window, select the Login text in the top banner using the arrow keys.



R80008

For both Device authentication or Server authentication, the user can enter any valid username and password combination. For ease of typing, it is preferable to do login using MiCOM S1 Agile.

After successful log in, a confirmation message is displayed, showing the logged in username at the top of the screen. For example:



R80010

25.7.3.2 LOGIN FAILED

When Authentication fails, a failure message is displayed:



25.7.3.3 OTHER LOGIN PROMPTS

For cases where the bypass is disabled and the user attempts an action which requires a user login, the Login Window appears after the error message. This is applicable while changing any setting values or pressing buttons which require user management - the Function Key, for example.

25.7.3.4 MICOM S1 LOGIN

When the user attempts to login, MiCOM S1 Agile will prompt the user with a login dialog box that contains a username and password entry fields. For both Device authentication or Server authentication, the user can enter any valid combination of username and password.

25.7.3.4.1 WARNING BANNER

After successful authentication and authorisation to access the IED, MiCOM S1 Agile will display a security warning banner to the user.

If **I Agree** is selected, the integrated authentication and authorisation is completed. Selecting **I Disagree** causes the program to close and the login user to logout.

For S1 Agile authentication, this is a pop-up dialog that the user must click to acknowledge.

25.7.4 USER SESSIONS

Only one role of one type is allowed to be logged in at a time from any interface. If the role has been logged in from one interface, an attempt to login the same role will result in a message being displayed, as below.



R60015

Open sessions will be automatically closed by the IED after a configurable session timeout.

The inactivity timer configuration setting defines the period of time that the IED waits in idleness before a logged in user is automatically logged out.

If there is any data change that does not commit to IED, the data change is discarded when user logged out. If there is any access that does not finish, the access will fail when user logged out. Front panel will display the default page when user reaches the defined inactivity time.

If the keypad is inactive for configured UI inactivity timer, the user logout message is displayed and the front panel user interface reverts to the Viewer access level.

The following settings are available in the ***SECURITY CONFIG*** column to support configurable inactivity timers.

- ***FP InactivTimer***
- ***UI InactivTimer***
- ***NIC Tunl Timeout***

Setting Name	Description	Min	Max	Default	Units	User Role Required
Attempts Limit	Number of failed authentications before the device blocks subsequent authentication attempts for the lockout period. A value of 0 means Lockout is disabled.	0 (lockout disabled)	99	3	-	SECADM
Lockout Period	The period of time in seconds a user is prevented from logging in, after being locked out.	1	5940	30	sec	SECADM
FP InactivTimer	FP Inactivity Timer is the time of idleness on Front Port before a logged in user is automatically logged out and revert the access level to the viewer role	0 (no Inactivity Timeout)	30	10	min	SECADM
UI InactivTimer	UI Inactivity Timer is the time of idleness on Front Panel before a logged in user is automatically logged out and revert the access level to the viewer role	0 (no Inactivity Timeout)	30	10	min	SECADM

Setting Name	Description	Min	Max	Default	Units	User Role Required
NIC Tunl Timeout	NIC Tunl Timeout is the time of idleness on Ethernet Port (NIC) before a logged in user is automatically logged out and revert the access level to the viewer role	1	5	5	min	SECADM

The recommended settings for ***Attempts Limit*** is *3* and ***Lockout Period*** is *30 sec* to discourage brute force attacks. If the Lockout period is too large, anybody can lockout Device users.

The following settings are available in the *COMMUNICATIONS* column to configure the inactivity timers for rear serial ports:

- ***KBUS InactTmr*** for RP1, if Courier Protocol is selected
- ***RP2 InactivTimer*** for RP2

25.7.5 USER LOCKING POLICY

A local user locking policy is implemented for Device access:

- This user locking policy applies to both Device users.
- The account is unlocked at the first successful login after the ***Lockout Period***
- If the user consecutively fails to login at the configured number of ***Attempts Limit***, the user account will be locked for the configured ***Lockout Period***

Each user account records how long it has been locked if the account is locked.

Each user account records how many times it has consecutively failed to login. User account failed times include all interfaces login attempts. For example, if the ***Attempts Limit*** setting is *3* and the operator failed to login from front panel 2 times, and they changed to login from the Courier interface, but failed again, then the Operator would be locked out.

When the IED is powered on, these ***Attempts Limit*** counter resets to zero.

When the user account exceeds the ***Attempts Limit*** it is locked for ***Lockout period***, at that time ***Attempt limit*** resets to zero.

The locked user account will be unlocked automatically, after the configured “Lockout Period” is expired.

If the locked account attempts to login the IED from the Front Panel, the unsuccessful login attempt screen is displayed.

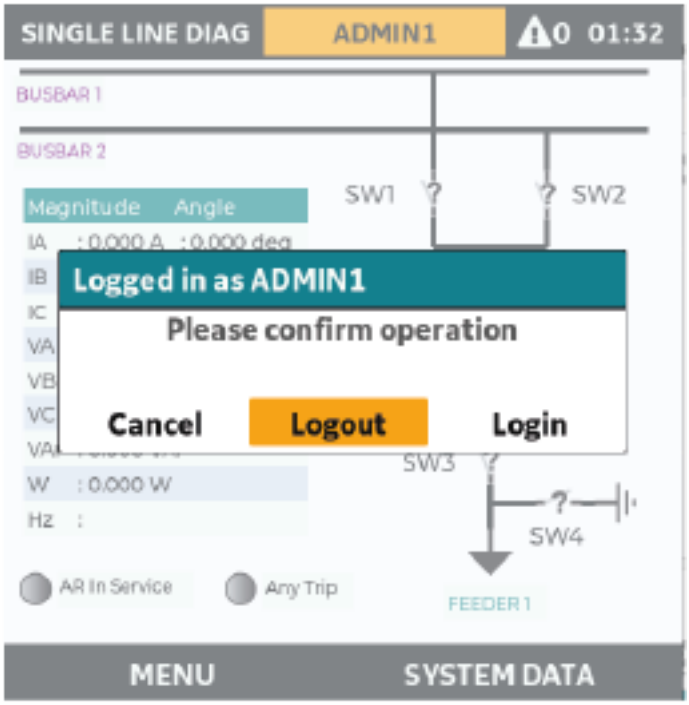
25.7.6 LOGOUT

Each user should ***Log out*** after reading or configuring the IED.

The user can only log out from the front panel, if they logged in from the front panel. If the user logged in from S1 Agile, they have to logout from S1 Agile.

25.7.6.1 FRONT PANEL LOGOUT

Go to the top of the banner and select the current logged in User. You may be prompted to log out with the following display:



R80013

If you confirm, the following screen is displayed for 2 seconds and then the action will be recorded in the security events file:



R80014

If you decide not to log out (i.e. you cancel), the logout screen would be cancelled.

25.7.6.2 MICOM S1 LOGOUT

Right-click on the device name in the System Explorer panel in MiCOM S1 Agile and select Log Off.

In the Log Off confirmation dialog, click Yes. The action will be recorded in the security events file.

25.7.7 PASSWORD POLICY

Cyber-security requires strong passwords and validation for NERC compliance. The IED will enforce one of two levels of password strength according to the ***Password Policy*** setting.

The NERC password complexity policy requires an alpha-numeric password (for all accesses, front panel, and network/local port) that meets the following **mandatory** requirements:

1. Passwords cannot contain the user's account name or parts of the user's full name that exceed two consecutive characters.
2. Passwords must be at least eight characters in length, but not exceed 16 characters in length.

Strict passwords rules must contain characters from all four categories as shown below:

a. English uppercase characters (A through Z).
b. English lowercase characters (a through z).
c. Numeric (digits 0 through 9).
d. Special non-alphanumeric characters (such as @,!,#,{, but not limited to only those)

Normal password rules: Any 3 out of 4 conditions as in strict password rules.

For Device authentication, the IED will enforce that configured passwords meet these requirements. The user can select which policies are required by selecting either Strict or Normal in the Password Policy setting under DEVICE RBAC.

Setting Name	Description	Min	Max	Default	Units	User Role Required
Password Policy	Selection of whether strict or normal rules apply for device authentication password policy	Normal	Strict	Strict	-	SECADM

For Server authentication, the password complexity and user locking policy is defined in the external RADIUS server.

25.7.8 PASSWORD EXPIRY

For Device authentication users, it is possible to select a configurable time (in days) for the password to be changed by the user.

Under *DEVICE RBAC* Settings, select ***Password Expiry*** to be Enabled. The setting of ***Disabled*** disables the password expiry check by the IED. If enabled, Max Password Age can be selected, this is in the range of days.

Setting Name	Description	Min	Max	Default	Units	User Role Required
Password Expiry	Selection of whether Password Expiry is enforced by the IED for device authentication	Disabled	Enabled	Enabled	-	SECADM
Max Password Age	Period in days if Password Expiry is enabled, the device passwords need to be changed	30	730	180	days	SECADM

When the Max Password Age has been reached and if the user attempts to login using the front panel UI, the following window will be shown.



R80011

The user will be presented with a screen to save the new password.



R80012

25.7.9 CHANGE PASSWORD

All the Device users will need to change the default password at the first logon.

The initial password change can be done either from the front panel User Interface, or from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

Any further password change can only be done from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

Users with SECADM and RBACMNT roles can change the password of any user. Users with other roles can change only their own password.

Caution:
It is recommended that user passwords are changed periodically.

25.7.10 RADIUS AUTHENTICATION

When the ***Auth. Method*** setting is configured as *Server + Device*, a user must log in with a username and password that has been predefined on the RADIUS server. RADIUS communication will work with either NP1 or NP2, provided that the device can reach the RADIUS server. This requires that the server resides in the same subnet as NP1/NP2.

This log in can be performed from any interface, as described in the Login section. The IED will authenticate the user to the active RADIUS server, over the Ethernet connection.

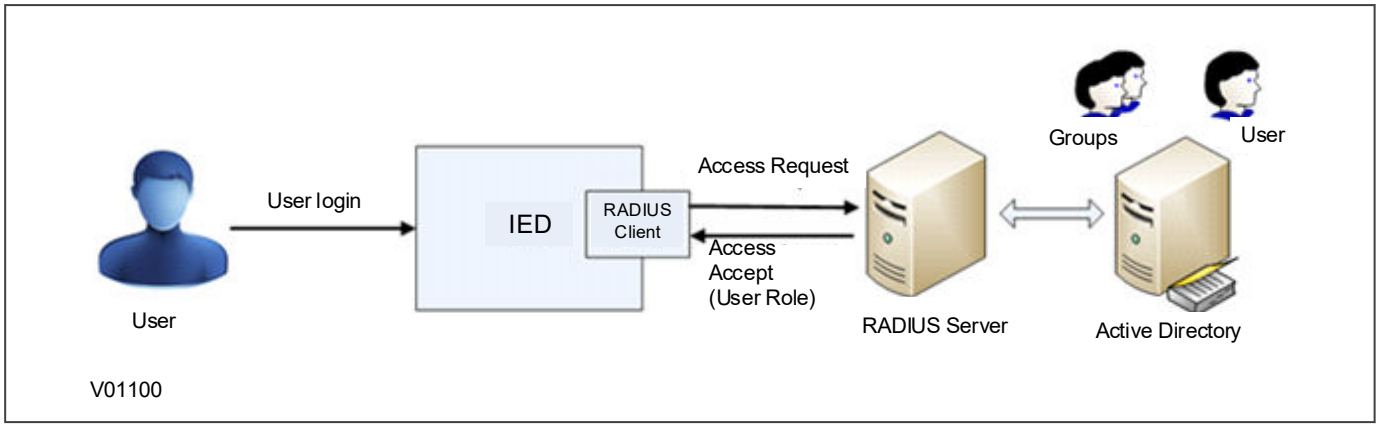


Figure 426: RADIUS server/client communication

25.7.10.1 RADIUS USERS

For Server authentication, RADIUS users and passwords are created in the RADIUS server (in the Active Directory), not in the IED.

The username must be from the ASCII Subset of 32 to 122 which includes upper and lower case letters, digits and several special characters.

Each RADIUS user must have a password that meets the password policy of the Active Directory (not the password policy of the P40) and have one of the supported roles assigned in the Active Directory.

The number of RADIUS users is not limited by the IED.

RADIUS password changes are done in the Active Directory (after password expiration).

25.7.10.2 RADIUS CLIENT

Two RADIUS servers are supported by the IED in the configuration for redundancy. The IED will try each in sequence until one responds.

The IED will first try server 1 up to the configured number of retries, leaving a request timeout between each request. If, after this point there is still no valid answer from server 1, the IED will switch to server 2 and repeat for up to the configured number of retries.

If the number of retries for the second server is exceeded the IED will fallback to Device authentication. A **RADIUS Server unavailable** security event is also logged under this condition.

The RADIUS implementation supports the following authentication protocols:

- EAP-TTLS-MSCHAP2
- PAP
- EAP-PEAP-MSCHAP2
- PAP EAP-TTLS-PAP (Default)

The RADIUS implementation queries the Role ID vendor attribute and establish the logged in user security context with that role.

RADIUS Config.	Value
Vendor ID	2910
Vendor Attribute	1
Standard Values	
VIEWER	0
OPERATOR	1
ENGINEER	2
INSTALLER	3
SECADM	4
SECAUD	5
RBACMNT	6

25.7.10.3 RADIUS SERVER SETTINGS

The following RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication.

Setting Name	Description	Min	Max	Default	Units	User Role Required
RADIUS Pri IP	IP address of Server 1. Default value indicates no Primary RADIUS server is configured, and so RADIUS is disabled.	0.0.0.0	255.255.255.255	0.0.0.0	-	SECADM
RADIUS Sec IP	IP address of Server 2. Default value indicates no Secondary RADIUS server is configured	0.0.0.0	255.255.255.255	0.0.0.0	-	SECADM
RADIUS Auth Port	RADIUS authentication port	1	65535	1812	-	SECADM
RADIUS Security	Authentication protocol to be used by RADIUS server	EAP-TTLS-MSCHAP2 PAP EAP-PEAP-MSCHAP2 PAP EAP-TTLS-PAP		PAP EAP-TTLS-PAP	-	SECADM
RADIUS Timeout	Timeout in seconds between re-transmission requests	1	900	2	sec	SECADM
RADIUS Retries	Number of retries before giving up	1	99	10	-	SECADM
RADIUS Secret	Shared Secret used in authentication. It is only displayed as asterisks.	1 character	64 characters	ChangeMe1#	-	SECADM
RADIUS NAS ID	NAS-Identifier for RADIUS	1 character	20 characters	MiCOM P40	-	SECADM

The data cell ***RADIUS Status*** indicates the status of the currently selected RADIUS server. This will display either *Disabled*, *Server OK*, or *Failed*.

25.7.10.4 RADIUS ACCOUNTING

RADIUS accounting is not supported by the IED. The user can achieve accounting through syslog (see the SYSLOG section).

25.7.10.5 RADIUS CLIENT-SERVER VALIDATION

Client-server validation is achieved using a shared secret. The IED must be configured with the ***RADIUS Secret*** setting to match the shared secret configured in the RADIUS server. It is recommended (but not enforced) that this setting meets the P40 password requirements. The device supports RADIUS secret of 1-64 characters.

MiCOM S1 Agile provides an option to save ***RADIUS Secret*** to the device. This can be achieved by logging to the device with a SECADM profile and accessing Supervise Device -> ***RADIUS Secret***.

Note:
It is recommended that the shared secret be changed from the default before using RADIUS authentication.

The IED does not support exchange of CA certificates. The RADIUS server may send a certificate, but the IED will not verify it.

25.7.11 RECOVERY

25.7.11.1 RESTORE TO LOCAL FACTORY DEFAULT

The ***Restore Defaults*** setting is available to facilitate NERC CIP compliance requirements for decommissioning critical cyber devices. Only the **Administrator** role can change this setting.

The ***Restore Defaults*** setting under the *CONFIGURATION* column is used to restore a setting group to factory default settings.

0 = *No Operation*

1 = *All Settings*

2 = *Setting Group 1*

3 = *Setting Group 2*

4 = *Setting Group 3*

5 = *Setting Group 4*

To restore the default values to the settings in any setting group, set the ***Restore Defaults*** setting to the relevant Group number. Alternatively, it is possible to set the ***Restore Defaults*** setting to *All Settings* to restore the default values to all the IEDs settings, not only one setting group.

Note:
Restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.

Data (events, DR, fault records, protection counters etc.) is left untouched. When decommissioning critical cyber IEDs, users may want to clear all data and events as well.

25.7.11.2 PASSWORD RESET PROCEDURE

If you mislay a devices password (if Administrator forgets their password), the passwords can be reset to default using a recovery password. To obtain the recovery password you must contact the Contact Centre and supply the Serial Number (TEST ID) and the security code. The Contact Centre will use these details to generate a Recovery Password.

The Serial Number required is a six-digit code followed by one letter, found in the SYSTEM DATA column of the IED. It is the same as the TEST ID shown on the label on top of the IED.

The security code is a 16-character string of uppercase characters. It is a read-only parameter. The device generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

This reset procedure can be only accomplished through front panel exclusively and cannot be done over any other interface. As soon as the security code is displayed on the front panel User Interface, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the Contact Centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the Contact Centre over weekends and bank holidays.

The procedure is:

The security code is displayed on confirmation. The validity timer is then started. The security code can only be read from the front panel.

This reset procedure can be only accomplished through front panel exclusively and cannot be done over the Ethernet/serial port, but only when physically present in front of the IED. In the event of losing all passwords (if the Administrator forgets their password) the user could reset the IED to default passwords, following the procedure below:

1. User navigates to ***Security Code*** cell in *SECURITY CONFIG* column
2. To prevent accidental reading of the IED ***Security Code***, the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

3. Press Enter to read the ***Security Code***.
4. User sends an email to the Contact Centre providing the full IED serial number and displayed ***Security Code***, using a recognisable corporate email account
5. Contact Centre emails the user with the Recovery Password. The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once - for password recovery.
6. User logs in with the username **ADMINISTRATOR** and the recovery password into the ***Password*** setting in *SYSTEM DATA* column.
7. Then IED will prompt

```
RESET PASSWORD?
ENTER or CLEAR
```

8. Press Enter to continue the reset procedure
9. If the recovery password successfully validates, the default passwords are restored for each access level for Device authentication.
10. Change ***Auth. Method*** setting to `Server + Device` if applicable.

Note:
Restoring passwords to defaults does not affect any other settings and does not provoke reboot of the IED. The protection and control functions of the IED are always maintained.

25.7.11.3 ACCESS LEVEL DDBS

The current level of access for each interface is available for use in the Programmable Scheme Logic (PSL) as these DDB signals:

- ***HMI Access Lvl 1***
- ***HMI Access Lvl 2***
- ***FPort AccessLvl1***
- ***FPort AccessLvl2***
- ***RPrt1 AccessLvl1***
- ***RPrt1 AccessLvl2***
- ***RPrt2 AccessLvl1***
- ***RPrt2 AccessLvl2***

Each pair of DDB signals indicates the access level as follows:

- Level 1 off, Level 2 off = 0
- Level 1 on, Level 2 off = 1
- Level 1 off, Level 2 on = 2
- Level 1 on, Level 2 on = 3

KEY:

HMI = Human Machine Interface

(Front Panel User Interface)

FPort = Front Port

RPrt = Rear Port

Lvl = Level

25.7.12 PORT HARDENING: PHYSICAL PORTS

It is possible to disable unused physical ports. Enabling/Disabling of physical ports can be done either via the Front Panel or by sending the modified settings to the IED. These settings are under the PORT HARDENING: PHYSICAL PORTS Section of SECURITY CONFIG column. A user with SECADM role is needed to perform this action. This action cannot be done via the Supervise Device dialog box using MiCOM S1 Agile.

The following ports can be disabled, depending on the model.

- Front Port (***Front Port*** setting)
- Rear Port 1 (***Rear Port 1*** setting)
- Rear Port 2 (***Rear Port 2*** setting)
- Ethernet Network Port 1 (***Network Port 1*** Setting)
- Ethernet Network Port 2 (***Network Port 2*** Setting)

25.7.13 PORT HARDENING: LOGICAL PORTS (PROTOCOLS)

It is possible to disable unused logical ports. Enabling/Disabling of logical ports can be done either via the Front Panel or via sending the modified settings to the IED. These settings are under the PORT HARDENING: LOGICAL PORTS Section of the SECURITY CONFIG column. A user with SECADM role is needed to perform this action, This action cannot be done via the Supervise Device dialog box using MiCOM S1 Agile.

The following NIC protocols can be disabled:

- Courier Tunnel (for S1 Agile remote connection over Ethernet)
- IEC 61850
- SNTP
- PTP
- SNMP
- SYSLOG

25.7.14 SERVICE (PROTOCOL) MAPPING: ETHERNET NETWORK PORTS 1 AND 2

This section details which of the Ethernet protocols are available on each of Network Port 1 and Network Port 2, and whether these are configurable or fixed mappings. Settings for the configurable service mappings are under the PORT HARDENING: SERVICE MAP section of the *SECURITY CONFIG* column.

Service	Port	Network Port 1	Network Port 2	Fixed/Configurable	Setting
IEC 61850	102/TCP	No	Yes	Fixed to NP2.	
SNTP	123/UDP	No	Yes	Fixed to NP2.	
PTP	-	No	Yes	Fixed to NP2.	
SSH (for S1 Agile)	22/TCP	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	Courier Tunnel
SNMP	161/UDP, 162/UDP	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	SNMP
Syslog	514/UDP	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	SYSLOG

25.7.15 SUPERVISE DEVICE DIALOG BOX

Supervise Device	Role Name							
	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Active Group			X	X	X			
Reset Cell			X					
Breakers			X					
Device Address				X	X	X		
Date and Time			X	X	X			
Bypass Options						X		
Active MCL Bank				X	X			
Device User Management						X		X
Own Password Change		X	X	X	X	X	X	X
RADIUS Secret						X		

Supervise Device	Role Name							
	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
SNMP Security						X		
Clear Records				X				
Restore Defaults				X	X			
Restore Security Settings						X		
SSH Client Passcode						X		

25.7.16 SECURE FIRMWARE UPGRADE

IEC 62351-8:2020 has defined a specific INSTALLER Role which can do firmware upgrades on the IEDs. The default users in the Device Authentication does not have any users with the INSTALLER Role. If a requirement exists to upgrade the Firmware of the IED, then the following mandatory steps must be taken before starting the firmware update:

- Using MiCOM S1 Agile, create a new user having the INSTALLER Role
- Using MiCOM S1 Agile, log into the device using the user having the INSTALLER Role. Change the default password
- Use the Firmware Download Tool and log into the IED, using the newly created user and changed password
- Once these steps are done, the firmware update process can continue.

The device supports Secure Firmware Update. The firmware files are checked for validity prior to updating of the IED. The main steps in the secure firmware update process are as follows:

- The ‘PX40 Download and Calibration’ firmware tool opens the secure firmware ZIP file and extracts its contents [Compressed Images and Signatures].
- The ‘PX40 Download and Calibration’ firmware tool transfers the firmware files [Compressed Images and Signatures] to IED Main CPU Board.
- IED validates the Compressed Images and extracts them.
- After successful validation, only then will the settings be cleared.
- In case of validation failure, IED will display the ERROR CODE and after that, the user can reboot the relay to its previous state.
- IED updates it Main CPU Board, Co-processor Board and Ethernet Board storage and verifies it.
- Finally, the Main CPU Board initiates an IED reboot.

Key steps in this process will be logged in the security events - see the Security Event Management section of this chapter for further details.

Any firmware upgrade should be organised through the GE Vernova Grid Automation After Sales Service departments, or a regional Local Service Centre. The firmware upgrade should normally be performed by GE Vernova personnel, or by suitably prepared and competent persons after instruction from GE Vernova personnel. A separate MiCOM P40 firmware download procedure guide is available.

Note:
It is not possible to update the firmware on the IED which is under Bypass mode.

Note:
During the firmware update, only the security events file is retained - all other configuration and record files are erased during a firmware upgrade.

25.8 SNMP CONFIGURATION

You configure the SNMP interface using the HMI panel or using the SNMP Security option in the Supervise Device dialog box by a user with SECADM role. Two different versions are available: SNMPv2c and SNMPv3:

To enable the SNMP interface:

1. Select the SECURITY CONFIG column and scroll to the SNMP PARAMETERS heading
2. You can select either v2C, V3 or both. Selecting None will disable the main processor SNMP interface.

SNMP trap configuration

SNMP traps allow for unsolicited reporting between the IED and up to two SNMP managers with unique IP addresses. The device MIB details what information can be reported using Traps. To configure the SNMP Traps:

1. Move down to the cell ***Trap Dest. IP 1*** and enter the IP address of the first destination SNMP manager. Setting this cell to `0.0.0.0` disables the first Trap interface.
2. Move down to the cell ***Trap Dest. IP 2*** and enter the IP address of the second destination SNMP manager. Setting this cell to `0.0.0.0` disables the Second Trap interface.

SNMP V3 security configuration

SNMPv3 provides a higher level of security via authentication and privacy protocols. The IED adopts a secure SNMPv3 implementation with a user-based security model (USM).

Authentication is used to check the identity of users; privacy allows for encryption of SNMP messages. Both are optional;however you must enable authentication in order to enable privacy. To configure these security options:

1. If SNMPv3 has been enabled, set the ***Security Level*** setting. There are three levels: without authentication and without privacy (`noAuthNoPriv`), with authentication but without privacy (`authNoPriv`), and with authentication and with privacy (`authPriv`).
2. If Authentication is enabled, use the ***Auth Protocol*** setting to select the authentication type. There are two options: `HMAC-MD5-96` or `HMAC-SHA-96`.
3. Using the ***Auth Password*** setting, enter the password (up to 20 characters) to be used by the IED for authentication.
4. Using the ***Auth Protocol*** setting, select one of the two available mechanisms for encryption of messages to be used by the IED (CBC-DES or CFB-AES128).
5. If privacy is enabled, use the ***Encrypt Password*** setting to set the encryption password (up to 20 characters) that will be used by the IED for encryption.

Note:
When setting the SNMP browser for RBAC compatible relays, the Context Name should be 'px4x'.

SNMP V2C security configuration

SNMPv2c implements authentication between the master and agent using a parameter called the ***Community Name***. This is effectively the password, but it is not encrypted during transmission (this makes it inappropriate for some scenarios in which case version 3 should be used instead). To configure the SNMP 2c security:

1. If SNMPv2c has been enabled, use the ***Community Name*** setting to set the password that will be used by the IED and SNMP manager for authentication. This may be between one and 8 characters.

25.9 RETURNING THE IED TO FACTORY

MiCOM P40 5th Generation products provide enhanced security, and there is no mechanism to bypass the implemented user management. If the IED is returned to the factory for repair or technical analysis, to facilitate the Engineers gaining access to the configuration and stored records in the IED, it is proposed that the IED is returned to the factory with one of the following options:

- Bypass enabled on the front port
- A new user with all Roles is created and left with a default password. If the details of this user are passed to the factory, the IED can be logged in after changing the default password. If the newly created user's password has been modified, it will be required that the modified password is provided

25.10 SECURITY EVENT MANAGEMENT

To implement NERC-compliant cyber-security, a range of security events are logged by the IED in three separate methods:

- In the Security Events file (security audit log) - a Courier events file that can be extracted and viewed by MiCOM S1 Agile
- As syslog events
- As SNMP events (traps)

25.10.1 SECURITY EVENTS: COURIER

The P40 supports the IEC 62351-14 format of security event messages. These are logged into a separate security audio log file named "Security events" that can be extracted and viewed by MiCOM S1 Agile, in addition to the operational events file. The maximum number of security events is 2048.

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_PW_SET_ NON_COMPLIANT	62443-AUDIT_ LOG	Info	USER_PW_ CHANGE_ FAIL_POLICY	IEC 62351-14:1.31	User Password change failed - policy check failed	
SECUR_EVT_PW_ MODIFIED	62443-CONFIG_ CHANGE	Notice	USER_PW_ CHANGE_OK	IEC 62351-14:1.25	User password changed successfully	Interface
SECUR_EVT_PW_ ENTRY_NOW_ BLOCKED	62443-ACCESS_ CONTROL	Notice	LOCK_USER_ WRONG_CR	IEC 62351-14:1.7	User locked - Wrong credentials	Interface
SECUR_EVT_PW_ ENTRY_UNBLOCKED	62443-ACCESS_ CONTROL	Notice	-	2910-MiCP40-001	User unlocked	Interface
SECUR_EVT_PW_ ENTERED_WHILE_ BLOCKED	62443-ACCESS_ CONTROL	Notice	-	2910-MiCP40-002	Log-in attempt when user is locked	Interface
SECUR_EVT_INVALID_PW _ENTERED	62443-ACCESS_ CONTROL	Notice	LOGIN_FAIL_ WRONG_ CR	IEC 62351-14:1.3	Log-in failed - Wrong credentials	Interface
SECUR_EVT_PW_ TIMED_OUT	62443-ACCESS_ CONTROL	error	LOGIN_FAIL_ CRED_ EXPIRE	IEC 62351-14:1.4	Log-in failed - credentials expired.	Interface
SECUR_EVT_ RECOVERY_PW_ ENTERED	62443-ACCESS_ CONTROL	Notice	-	2910-MiCP40-004	Recovery password entered	Interface
SECUR_EVT_IED_SEC_ CODE_READ	62443-AUDIT_ LOG	Info	-	2910-MiCP40-005	Security Code read	Interface
SECUR_EVT_IED_SEC_ CODE_TMR_ EXPIRED	62443-AUDIT_ LOG	Info	-	2910-MiCP40-006	Security Code Timer expired	Interface
SECUR_EVT_PORT_ DISABLED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-007	Port Disabled	Interface
SECUR_EVT_PORT_ ENABLED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-008	Port Enabled	Interface, Port number
SECUR_EVT_PSL_ SETTINGS_ DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-009	PSL Settings downloaded to device	Interface, Port number
SECUR_EVT_DNP_ SETTINGS_ DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-010	DNP Settings downloaded to device	Interface, Group number

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_TRACE_ DATA_DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-011	TRACE Data downloaded to device	Interface
SECUR_EVT_61850_ CONFIG_ DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-012	IEC61850 Config downloaded to device	Interface
SECUR_EVT_USER_ CURVES_ DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-013	User Curves downloaded to device	Interface
SECUR_EVT_SETTING_G RP_ DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-014	Setting Group downloaded to device	Interface, Curve number
SECUR_EVT_DR_ SETTINGS_ DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-015	DR Settings downloaded to device	Interface, Group number
SECUR_EVT_PSL_ SETTINGS_ UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-016	PSL Settings uploaded from device	Interface
SECUR_EVT_DNP_ SETTINGS_ UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-017	DNP Settings uploaded from device	Interface, Group number
SECUR_EVT_TRACE_ DATA_UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-018	TRACE Data uploaded from device	Interface
SECUR_EVT_61850_ CONFIG_UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-019	IEC61850 Config uploaded from device	Interface
SECUR_EVT_USER_ CURVES_UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-020	User Curves uploaded from device	Interface
SECUR_EVT_PSL_ CONFIG_UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-021	PSL Config uploaded from device	Interface, Curve number
SECUR_EVT_ SETTINGS_ UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-022	Settings uploaded from device	Interface, Group number
SECUR_EVT_CS_ SETTINGS_CHANGED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-023	Control & Support settings changed	Interface
SECUR_EVT_DR_ SETTINGS_CHANGED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-024	Disturbance Record Settings changed	Interface
SECUR_EVT_ SETTING_GROUP_ CHANGED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-025	Setting Group changed	Interface
SECUR_EVT_ DEFAULT_SETTINGS_ RESTORED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-026	Default Settings restored	Interface, Group number
SECUR_EVT_ DEFAULT_USRCURVE_ RESTORED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-027	Default User Curve restored	Interface
SECUR_EVT_POWER_ON	62443- CONTROL_ SYSTEM	Notice	-	2910-MiCP40-028	Device Powered On	Interface, Curve number
SECUR_EVT_RADIUS_ UNAVAIL	62443-AUDIT_ LOG	warning	RBAC_NO_ RADIUS	IEC 62351-8:1.3	RADIUS server not available	Interface
SECUR_EVT_ SESSION_LIMIT	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-030	Active user sessions limit reached	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_SLD_ FILE_DOWNLOADED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-031	SLD File downloaded to device	Interface
SECUR_EVT_SLD_ FILE_UPLOADED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-032	SLD File uploaded from device	Interface
SECUR_EVT_RBAC_ LOGIN	62443-ACCESS_ CONTROL	Notice	LOGIN_OK	IEC-62351-14:1.1	Log-in successful	Interface
SECUR_EVT_RBAC_ LOGOUT	62443-ACCESS_ CONTROL	Notice	LOGOUT_ USER	IEC 62351-14:1.8	Log-out (user logged out)	Interface
Bypass mode Activated	62443-ACCESS_ CONTROL	Notice	-	2910-MiCP40-033	Bypass Mode Activated	Interface
Bypass mode Deactivated	62443-ACCESS_ CONTROL	Notice	-	2910-MiCP40-034	Bypass Mode Deactivated	Interface
SECUR_EVT_RADIUS_ KEY_CHANGED	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-044	RADIUS Secret Key changed	Interface
SECUR_SEC_ SETTINGS_ RESTORED	62443-BACKUP_ RESTORE	Notice	-	2910-MiCP40-041	Security settings restored	Interface
Switch to Golden Image	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-045	Device switching to Firmware update mode	Interface
FIRMWARE_ VALIDATION_ SUCCESS	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-035	Firmware Digital Signature check successful	Interface
FIRMWARE_ VALIDATION_FAIL	62443-AUDIT_ LOG	warning	-	2910-MiCP40-036	Firmware Digital Signature check failed	Interface
Firmware update process started	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-046	Firmware update initiated	Interface
Fail to receive firmware files	62443-AUDIT_ LOG	Warning	-	2910-MiCP40-047	Firmware files transfer failed	Interface
Fail to update firmware	62443-AUDIT_ LOG	Warning	-	2910-MiCP40-048	Firmware update failed	Interface
Firmware update process success	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-049	Firmware update successful	Interface, Previous FW version, Latest FW version
Serial&Model number update success	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-050	Serial/Model number update successful	
Serial&Model number update fail	62443-AUDIT_ LOG	Warning	-	2910-MiCP40-051	Serial/Model number update failed	Interface
NP1 MAC update success	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-052	NP1 MAC address update successful	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
NP1 MAC update fail	62443-AUDIT_ LOG	Warning	-	2910-MiCP40-053	NP1 MAC address update failed	Interface
NP2 MAC update success	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-054	NP2 MAC address update successful	Interface
NP2 MAC update fail	62443-AUDIT_ LOG	Warning	-	2910-MiCP40-055	NP2 MAC address update failed	Interface
Fallback to Device Authentication	62443-ACCESS_ CONTROL	Warning	-	2910-MiCP40-056	Fallback to Device Authentication	Interface
User logged out due to inactivity timeout	62443-ACCESS_ CONTROL	Notice	LOGOUT_ TIMEOUT	IEC 62351-14:1.9	Log-out by user inactivity (timeout).	Interface
Security events upload	62443-AUDIT_ LOG	Notice	-	2910-MiCP40-042	Security Events uploaded from device	Interface
SSH Passcode change	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-057	SSH pass code change	Interface
SSH Client Authentication Fail	62443-ACCESS_ CONTROL	Warning	-	2910-MiCP40-059	Failed client authentication	Interface
SSH Client Authentication Success	62443-ACCESS_ CONTROL	Notice	-	2910-MiCP40-058	Successful client authentication	Interface
New User added	62443-CONFIG_ CHANGE	Notice	USER_ ACCNT_ CREATE_OK	IEC 62351-14:2.15	User account created successfully.	Interface
User deleted	62443-CONFIG_ CHANGE	Notice	USER_ ACCNT_DEL_OK	IEC 62351-14:2.21	User account deleted successfully.	Interface
User role change	62443-CONFIG_ CHANGE	Notice	USER_ PERMISSION_ CHANGE_OK	IEC 62351-14:2.11	Permission changed successfully.	Interface
User name change	62443-CONFIG_ CHANGE	Notice	-	2910-MiCP40-060	User renamed successfully	Interface

Where the Interface values in "Extra Info" parameter are: "UI", "FP", "RP1", "RP2", "NET", "HMI".

25.10.2 SECURITY EVENTS: SYSLOG

Security events are also logged to a remote server and are based on Syslog [RFC 5424].

All login and logout attempts from local and central authentication, whether successful or failed, are logged. The contents of each successful or failed, login and logout security event include a specific username.

The security log cannot be cleared by any of the available roles.

The contents of each login and/or logout security event include the relevant interface. The following interfaces are supported:

Interface	Abbr.
Front Port	FP
Rear Port 1	RP1
Rear Port 2	RP2
Network Port 1 or 2	NET
Front Panel	UI

The following events are available to be logged to the syslog server:

Security Event	SNMP Trap Text
SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
SECUR_EVT_PW_MODIFIED	User password changed successfully
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked – Wrong credentials
SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - Wrong credentials
SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired.
SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
SECUR_EVT_IED_SEC_CODE_READ	Security Code read
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
SECUR_EVT_PORT_DISABLED	Port Disabled
SECUR_EVT_PORT_ENABLED	Port Enabled
SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device

Security Event	SNMP Trap Text
SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
SECUR_EVT_RBAC_LOGIN	Log-in successful
SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
Bypass mode Activated	Bypass Mode Activated
Bypass mode Deactivated	Bypass Mode Deactivated
RADIUS Secret Key changed	RADIUS Secret Key changed
SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
Switch to Golden Image	Device switching to Firmware update mode
Fallback to Device Authentication	Fallback to Device Authentication
User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
Security events upload	Security Events uploaded from device
SSH Passcode change	SSH pass code change
SSH Client Authentication Fail	Failed client authentication
SSH Client Authentication Success	Successful client authentication
New User added	User account created successfully
User deleted	User account deleted successfully
User role change	Permission changed successfully

25.10.3 SYSLOG CLIENT

The IED supports security event reporting through the Syslog protocol for supporting Security Information Event Management (SIEM) systems for centralised cyber security Monitoring over UDP protocol.

The IED is a Syslog client that supports two Syslog servers. The following settings are available in the *SECURITY CONFIG.* column.

Setting Name	Description	Min	Max	Default	Units	User Role Required
SysLog Pri IP	The IP address of the target Syslog server (Primary)	0.0.0.0	223.255.255.254	0.0.0.0	-	SECADM
SysLog Sec IP	The IP address of the target Syslog server (Secondary)	0.0.0.0	223.255.255.254	0.0.0.0	-	SECADM
SysLog Port	The UDP port number of the target Syslog server	1	65535	514	-	SECADM

25.10.4 SYSLOG FUNCTIONALITY

P40 supports IEC 62351-14 based cyber security event monitoring and is based on Syslog [RFC 5424].

Sample Syslog messages are shown below:

Event	Access Method	Syslog Message (as from Syslog Server)
IED Powered On	UI	5492, 2024-06-12T19:18:28.982Z, 423991K, GE_RE_P543_____AB0_o, MiCP40_POWER_ON, 2910-MiCP40-028, notice, IECCTRLSYS, Device Powered On, UI
ADMIN1 Log-in successful	FP	5523, 2024-06-12T20:04:26.851Z, 423991K, GE_RE_P543_____AB0_o, LOGIN_OK, IEC 62351-14:1.1, notice, IECACCCTRL, ADMIN1, SECAM, Log-in successful, FP
SSH Successful client authentication (S1 Agile)	NET	5460, 2024-06-12T18:04:45.359Z, 423991J, GE_RE_P546_____AB0_o, MiCP40_SSH_CLIENT_AUTH_SUCCESS, 2910-MiCP40-058, notice, IECACCCTRL, Successful client authentication, NET
Firmware update successful	FP	5476, 2024-06-12T19:18:19.004Z, 423991K, GE_RE_P543_____AB0_o, MiCP40_FW_UPDATE_SUCCESS, 2910-MiCP40-049, notice, IECCONFCHG, Firmware update successful, FP, P546_____AB0_o to P543_____AB0_o

25.10.5 SECURITY EVENTS: SNMP

Security events can also be sent as SNMP traps to a remote SNMP server. These traps are supported in both V2c and V3 versions of SNMP. For further information related to the full SNMP interface in P40, refer to the SNMP section in the COMMUNICATIONS chapter.

The format of the SNMP traps for security events consists of three parts as described below:

"Event Description, Username, Interface"

- Event Description: Short description of the alarm, same as the description present in Security event.
- Username: User associated with the event, provided only when Username is available for the Security event.
- Interface: Interface on which Security event has occurred, same as the interface information present in Security event.

The following events are available to be logged to the SNMP server:

Security Event	SNMP Trap Text
SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
SECUR_EVT_PW_MODIFIED	User password changed successfully
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked - Wrong credentials
SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - Wrong credentials
SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired.
SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
SECUR_EVT_IED_SEC_CODE_READ	Security Code read
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
SECUR_EVT_PORT_DISABLED	Port Disabled
SECUR_EVT_PORT_ENABLED	Port Enabled
SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed

Security Event	SNMP Trap Text
SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
SECUR_EVT_POWER_ON	Device Powered On
SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
SECUR_EVT_RBAC_LOGIN	Log-in successful
SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
Bypass mode Activated	Bypass Mode Activated
Bypass mode Deactivated	Bypass Mode Deactivated
RADIUS Secret Key changed	RADIUS Secret Key changed
SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
Switch to Golden Image	Device switching to Firmware update mode
Fallback to Device Authentication	Fallback to Device Authentication
User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
Security events upload	Security Events uploaded from device
SSH Passcode change	SSH pass code change
SSH Client Authentication Fail	Failed client authentication
SSH Client Authentication Success	Successful client authentication
New User added	User account created successfully
User deleted	User account deleted successfully
User role change	Permission changed successfully

CHAPTER 26

INSTALLATION

26.1 CHAPTER OVERVIEW

This chapter provides information about installing the product.

This chapter contains the following sections:

Chapter Overview 761
Handling the Goods 762
Mounting the Device 763
Cables and Connectors 766
Case Dimensions 770

26.2 HANDLING THE GOODS

Our products are of robust construction but require careful treatment before installation on site. This section discusses the requirements for receiving and unpacking the goods, as well as associated considerations regarding product care and personal safety.



Caution:
Before lifting or moving the equipment you should be familiar with the Safety Information chapter of this manual.

26.2.1 RECEIPT OF THE GOODS

On receipt, ensure the correct product has been delivered. Unpack the product immediately to ensure there has been no external damage in transit. If the product has been damaged, make a claim to the transport contractor and notify us promptly.

For products not intended for immediate installation, repack them in their original delivery packaging.

26.2.2 UNPACKING THE GOODS

When unpacking and installing the product, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any CDROMs or technical documentation (where included). These should accompany the unit to its destination substation and put in a dedicated place.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies where installation is being carried out at the same time as construction work.

26.2.3 STORING THE GOODS

If the unit is not installed immediately, store it in a place free from dust and moisture in its original packaging. Keep any dehumidifier bags included in the packing. The dehumidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals before replacing it in the carton. Ideally regeneration should be carried out in a ventilating, circulating oven at about 115°C. Bags should be placed on flat racks and spaced to allow circulation around them. The time taken for regeneration will depend on the size of the bag. If a ventilating, circulating oven is not available, when using an ordinary oven, open the door on a regular basis to let out the steam given off by the regenerating silica gel.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. Avoid storing in locations of high humidity. In locations of high humidity the packaging may become impregnated with moisture and the dehumidifier crystals will lose their efficiency.

The device can be stored between –25º to +70ºC for unlimited periods or between -40°C to + 85°C for up to 96 hours (see technical specifications).

To avoid deterioration of electrolytic capacitors, power up units that are stored in a de-energised state once a year, for one hour continuously.

26.2.4 DISMANTLING THE GOODS

If you need to dismantle the device, always observe standard ESD (Electrostatic Discharge) precautions. The minimum precautions to be followed are as follows:

- Use an antistatic wrist band earthed to a suitable earthing point.
- Avoid touching the electronic components and PCBs.

26.3 MOUNTING THE DEVICE

The products are dispatched either individually or as part of a panel or rack assembly.

Individual products are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres.

The products are designed so the fixing holes in the mounting flanges are only accessible when the access covers are open.

If you use a P991 or MMLG test block with the product, when viewed from the front, position the test block on the right-hand side of the associated product. This minimises the wiring between the product and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

26.3.1 FLUSH PANEL MOUNTING

Panel-mounted devices are flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).



Caution:
Do not use conventional self-tapping screws, because they have larger heads and could damage the faceplate.

Alternatively, you can use tapped holes if the panel has a minimum thickness of 2.5 mm.

For applications where the product needs to be semi-projection or projection mounted, a range of collars are available.

If several products are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.



Caution:
Do not fasten products with pop rivets because this makes them difficult to remove if repair becomes necessary.

26.3.2 RACK MOUNTING

Panel-mounted variants can also be rack mounted using single-tier rack frames (our part number FX0021 001), as shown in the figure below. These frames are designed with dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm (19 inch) rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the products by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).



Caution:
Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS products because they have slightly larger heads.

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.



Figure 427: Rack mounting of products

Products can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from different product ranges to be pre-wired together before mounting.

Use blanking plates to fill any empty spaces. The spaces may be used for installing future products or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The part numbers are as follows:

Case Size Summation	Blanking Plate Part Number
5TE	GJ2028 001
10TE	GJ2028 002
20TE	GJ2028 004
40TE	GJ2028 008
60TE	GJ2028 012

26.3.3 REFURBISHMENT SOLUTIONS

A feature of 5th Generation MiCOM products is their fit, form, and functionality compatibility with previous generations of similar devices. Pin-for-pin compatibility with our older products eases upgrade refurbishment of existing installations to accommodate the advantages of new developments with minimal disruption. If upgrading from previous MiCOM products, or even to replace some of our legacy products (such as MiDOS MBCH or K-series KBCH), the process is simple:

- Take the order code (CORTEC) of the older device being removed
- Translate to today's latest GE Vernova MiCOM model (adding Ethernet options if required)
- Order the new 5th Generation equivalent P40 device
- Use the S1 Agile toolsuite to extract settings and logic and convert the settings
- Detach the medium duty terminal blocks from your old device, making sure you leave the wiring attached.

- Although it may be possible to reuse the (heavy duty) CT/VT terminal blocks, we recommend that those supplied on the new IED are used during refurbishment. In this case, acting with due caution, disconnect the wiring to these terminals.
- Carefully examine the terminal blocks to ensure there is no physical damage
- Attach any detached terminal blocks and disconnected wiring from your old device to the new IED
- We recommend applying rated current and voltage to the relay CT/VT inputs through secondary injection testing to check the continuity of the CT/VT terminal block connections before re-energisation.
- Download your converted files
- Test (*), then return circuit to service.

* See the Commissioning Instructions chapter for more information on testing

Please contact GA.support@gevernova.com for further advice or assistance.

26.4 CABLES AND CONNECTORS

This section describes the type of wiring and connections that should be used when installing the device. For pin-out details please refer to the Hardware Design chapter or the wiring diagrams.

Caution:
Before carrying out any work on the equipment you should be familiar with the Safety Section and the ratings on the equipment's rating label.

26.4.1 TERMINAL BLOCKS

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

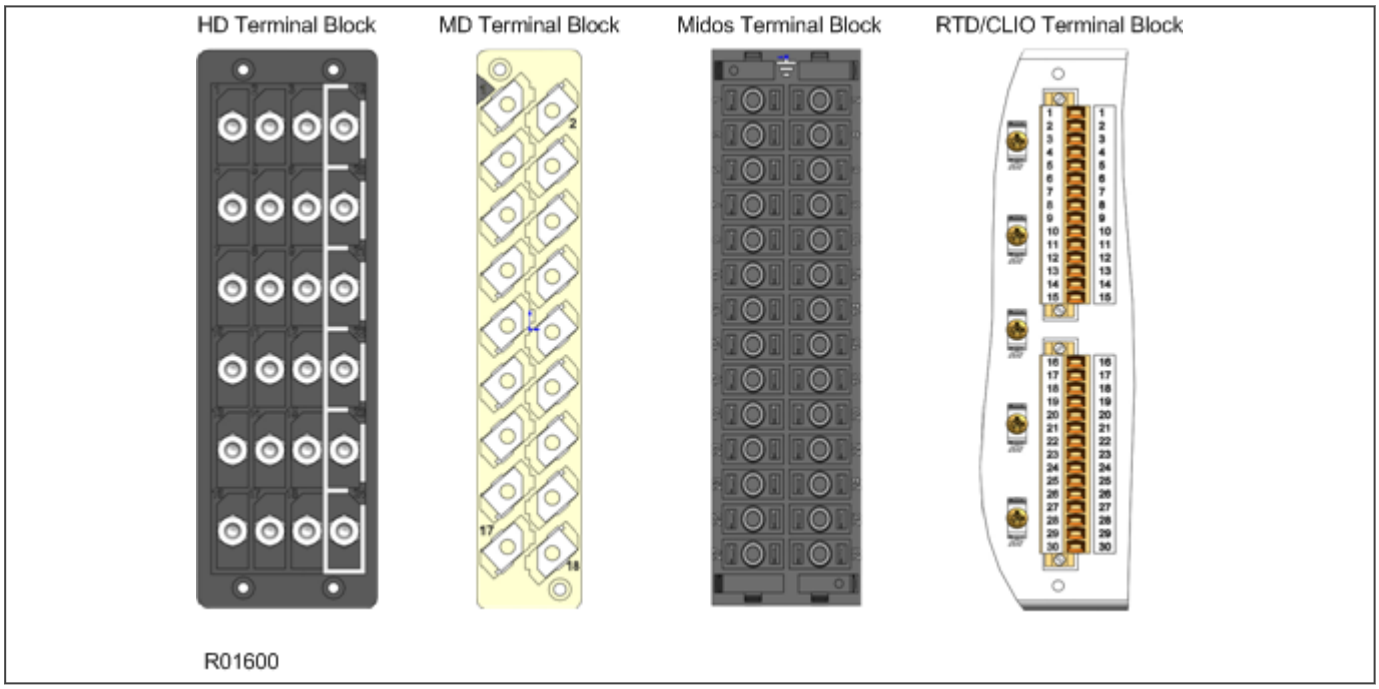


Figure 428: Terminal block types

MiCOM products are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per terminal.

If required, M4 90° crimp ring terminals can be supplied in three different sizes depending on wire size. Each type is available in bags of 100.

Part Number	Wire Size	Insulation Colour
ZB9124 901	0.25 - 1.65 mm^2 (22 - 16 AWG)	Red
ZB9124 900	1.04 - 2.63 mm^2 (16 - 14 AWG)	Blue

Note:
IP2x shields and side cover panels may be fitted to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers can be attached during installation or retrofitted to upgrade existing installations. The shields are supplied with four language fitting instructions, publication number: IP2x-TM-4L-n (where n is the current issue number). For more information, contact your local sales office or our worldwide Contact Centre.

26.4.2 POWER SUPPLY CONNECTIONS

These should be wired with 1.5 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.



Caution:
Protect the auxiliary power supply wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

26.4.3 EARTH CONNNECTION

Every device must be connected to the cubicle earthing bar using the M4 earth terminal.

Use a wire size of at least 2.5 mm^2 terminated with a ring terminal.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Note:
To prevent any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the product, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the product case, or using tinned ring terminals.

26.4.4 CURRENT TRANSFORMERS

Current transformers would generally be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.



Caution:
Current transformer circuits must never be fused.

Note:
If there are CTs present, spring-loaded shorting contacts ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken.

Note:
For 5A CT secondaries, we recommend using 2 x 2.5 mm^2 PVC insulated multi-stranded copper wire.

26.4.5 VOLTAGE TRANSFORMER CONNECTIONS

Voltage transformers should be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

26.4.6 WATCHDOG CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

26.4.7 EIA(RS)485 AND K-BUS CONNECTIONS

For connecting the EIA(RS485) / K-Bus ports, use 2-core screened cable with a maximum total length of 1000 m or 200 nF total cable capacitance.

To guarantee the performance specifications, you must ensure continuity of the screen, when daisy chaining the connections.

Two-core screened twisted pair cable should be used. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The K-Bus signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

A typical cable specification would be:

- Each core: 16/0.2 mm^2 copper conductors, PVC insulated
- Nominal conductor area: 0.5 mm^2 per core
- Screen: Overall braid, PVC sheathed

26.4.8 IRIG-B CONNECTION

The IRIG-B input and BNC connector have a characteristic impedance of 50 ohms. We recommend that connections between the IRIG-B equipment and the product are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

26.4.9 OPTO-INPUT CONNECTIONS

These should be wired with 1 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Each opto-input has a selectable preset ½ cycle filter. This makes the input immune to noise induced on the wiring. This can, however slow down the response. If you need to switch off the ½ cycle filter, either use double pole switching on the input, or screened twisted cable on the input circuit.



Caution:
Protect the opto-inputs and their wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

26.4.10 OUTPUT RELAY CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

26.4.11 ETHERNET METALLIC CONNECTIONS

If the device has a metallic Ethernet connection, it can be connected to a 100Base-TX Ethernet hub. Due to noise sensitivity, we recommend this type of connection only for short distance connections, ideally where the products and hubs are in the same cubicle. For increased noise immunity, CAT 6 (category 6) STP (shielded twisted pair) cable and connectors can be used.

The connector for the Ethernet port is a shielded RJ-45. The pin-out is as follows:

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

26.4.12 ETHERNET FIBRE CONNECTIONS

We recommend the use of fibre-optic connections for permanent connections in a substation environment. The 100 Mbps fibre optic port uses type LC connectors (one for Tx and one for Rx), compatible with 50/125 µm or 62.5/125 µm multimode fibres at 1300 nm wavelength.

26.4.13 USB CONNECTION

The IED has a type B USB socket inside the bottom compartment. A standard USB printer cable (type A one end, type B the other end) can be used to connect a local PC to the IED. This cable is the same as that used for connecting a printer to a PC.

26.4.14 GPS FIBRE CONNECTION

Some products use a GPS 1 PPS timing signal. If applicable, this is connected to a fibre-optic port on the coprocessor board in slot B. The fibre-optic port uses an ST type connector, compatible with fibre multimode 50/125 µm or 62.5/125 µm – 850 nm.

26.4.15 FIBRE COMMUNICATION CONNECTIONS

The fibre optic port consists of one or two channels using ST type connectors (one for Tx and one for Rx). The type of fibre used depends on the option selected.

850 nm and 1300 nm multimode systems use 50/125 µm or 62.5/125 µm multimode fibres. 1300 nm and 1550 nm single mode systems use 9/125 µm single mode fibres.

26.5 CASE DIMENSIONS

Not all products are available in all case sizes.

26.5.1 CASE DIMENSIONS 40TE

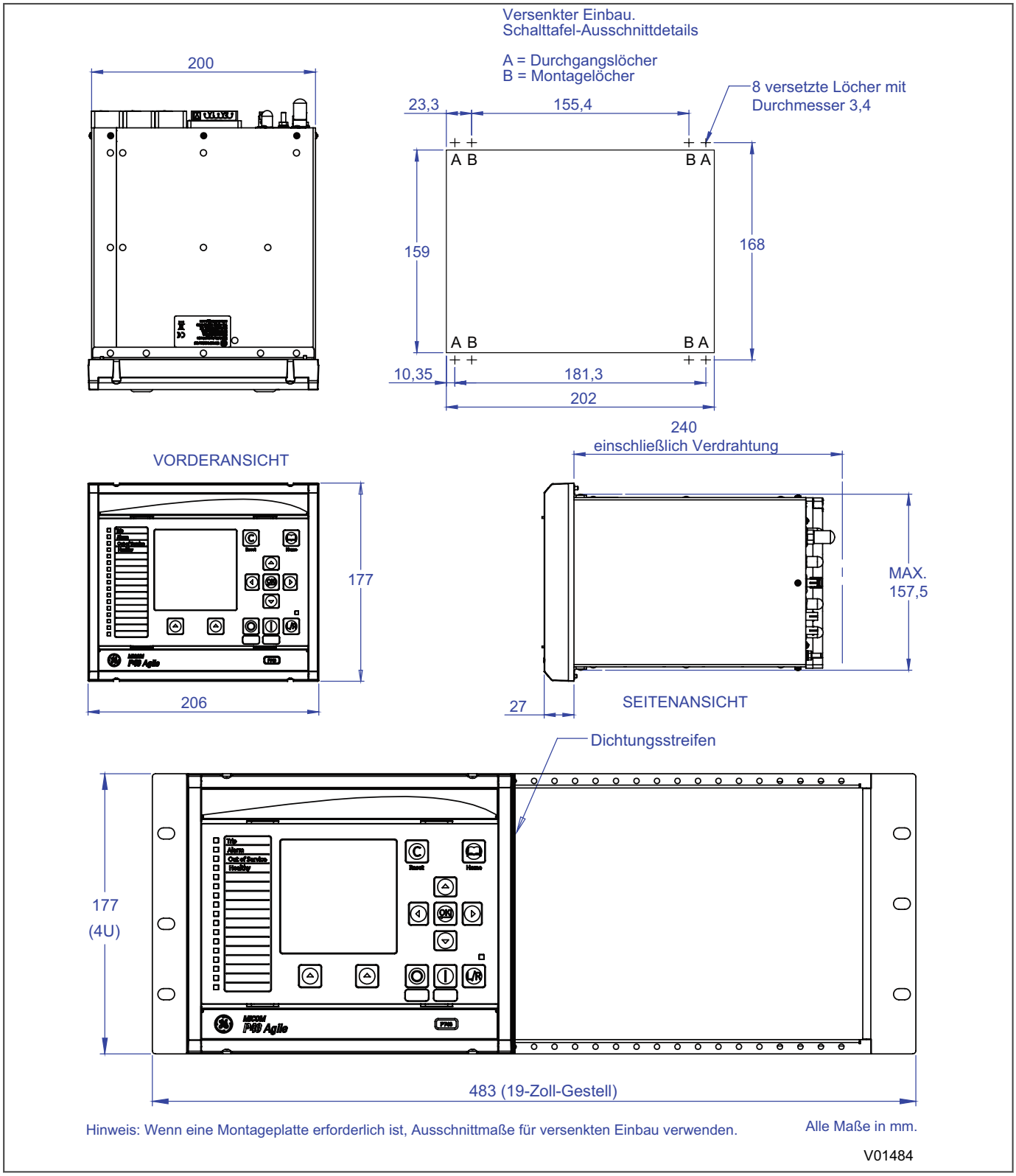


Figure 429: 40TE case dimensions

26.5.2 CASE DIMENSIONS 60TE

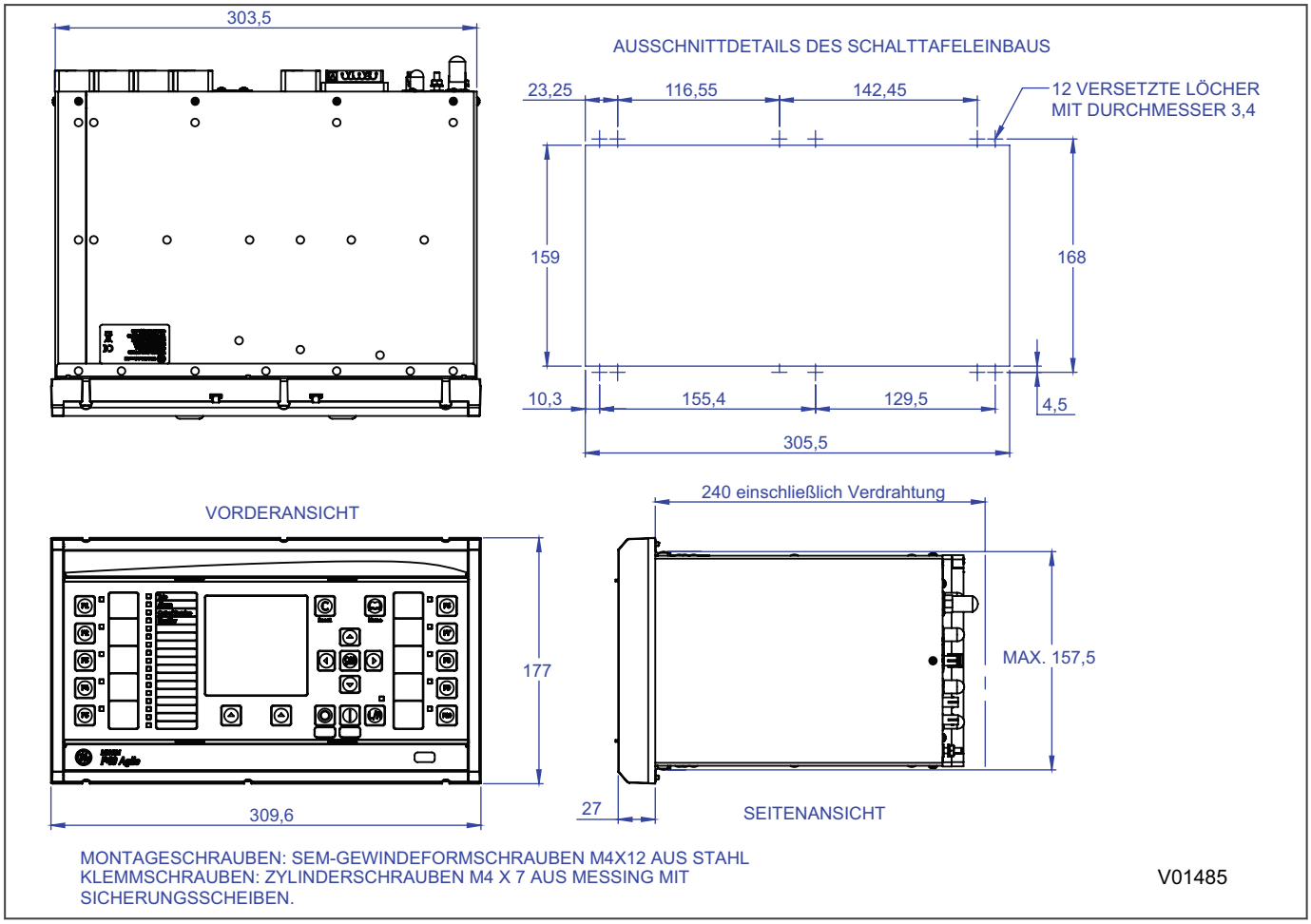


Figure 430: 60TE case dimensions

26.5.3 CASE DIMENSIONS 80TE

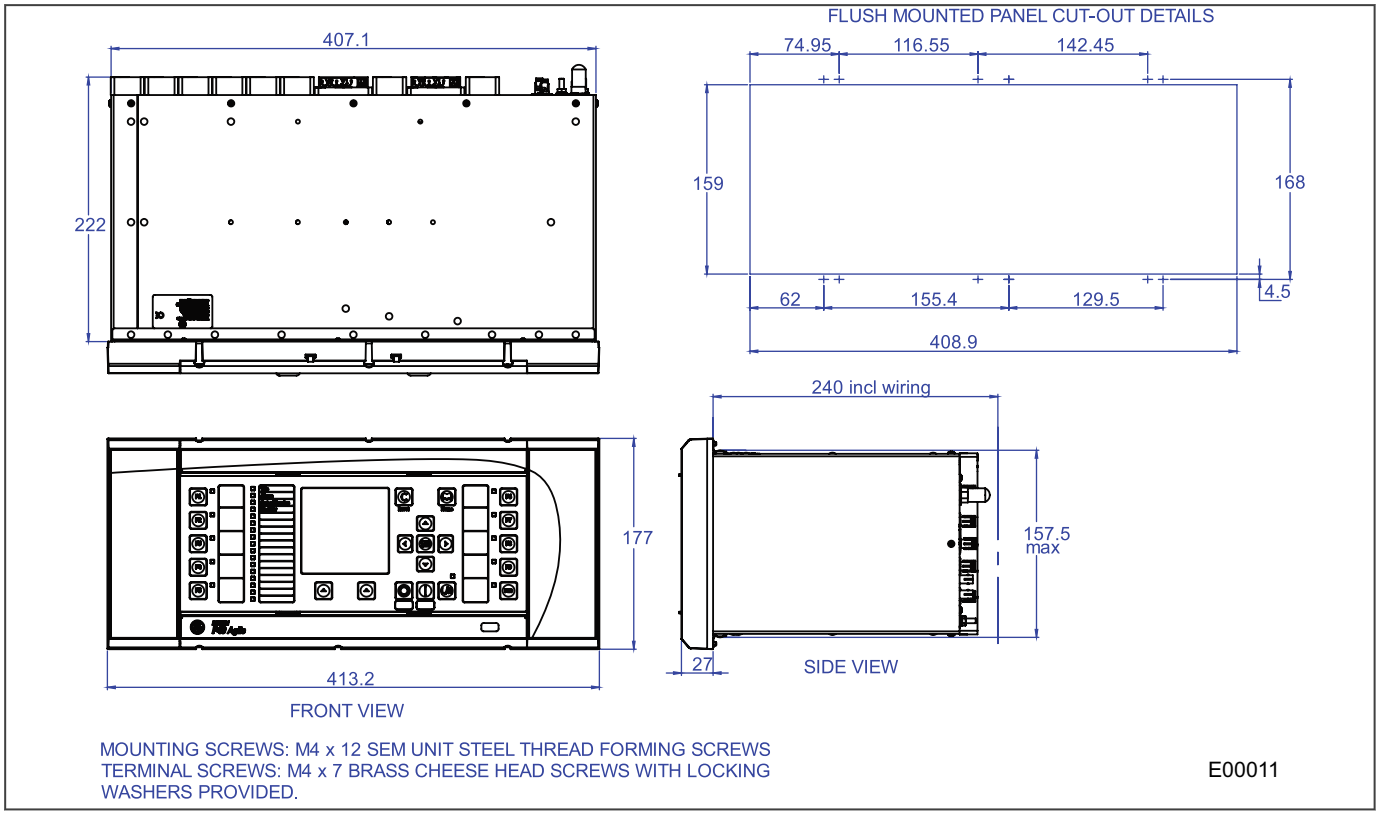


Figure 431: 80TE case dimensions

CHAPTER 27

COMMISSIONING INSTRUCTIONS

27.1 CHAPTER OVERVIEW

This chapter contains the following sections:

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General Guidelines 776
Commissioning Test Menu 777
Commissioning Equipment 781
Product Checks 783
Electrical Intermicom Communication Loopback 792
Intermicom 64 Communication 794
GPS Synchronisation 796
Setting Checks 797
IEC 61850 Edition 2 Testing 799
Current Differential Protection 804
Distance Protection 807
Delta Directional Comparison 814
DEF Aided Schemes 817
Out of Step Protection 820
Protection Timing Checks 822
System Check and Check Synchronism 824
Check Trip and Autoreclose Cycle 825
End-to-End Communication Tests 826
End-to-End Scheme Tests 829
Onload Checks 831
Final Checks 833
Commmissioning the P59x 834

27.2 GENERAL GUIDELINES

GE Vernova IEDs are self-checking devices and will raise an alarm in the unlikely event of a failure. This is why the commissioning tests are less extensive than those for non-numeric electronic devices or electro-mechanical relays.

To commission the devices, you (the commissioning engineer) do not need to test every function. You need only verify that the hardware is functioning correctly and that the application-specific software settings have been applied. You can check the settings by extracting them using the settings application software, or by means of the front panel interface (HMI panel).

The menu language is user-selectable, so you can change it for commissioning purposes if required.

Note:
Remember to restore the language setting to the customer's preferred language on completion.



Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM as well as the ratings on the equipment's rating label.



Warning:
With the exception of the CT shorting contacts check, do not disassemble the device during commissioning.

27.3 COMMISSIONING TEST MENU

The IED provides several test facilities under the *COMMISSION TESTS* menu heading. There are menu cells that allow you to monitor the status of the opto-inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs. This section describes these commissioning test facilities.

27.3.1 OPTO I/P STATUS CELL (OPTO-INPUT STATUS)

This cell can be used to monitor the status of the opto-inputs while they are sequentially energised with a suitable DC voltage. The cell is a binary string that displays the status of the opto-inputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each logic input.

27.3.2 RELAY O/P STATUS CELL (RELAY OUTPUT STATUS)

This cell can be used to monitor the status of the relay outputs. The cell is a binary string that displays the status of the relay outputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each relay output.

The cell indicates the status of the output relays when the IED is in service. You can check for device damage by comparing the status of the output contacts with their associated bits.

Note:
*When the **Test Mode** cell is set to `Contacts Blocked`, the relay output status indicates which contacts would operate if the IED was in-service. It does not show the actual status of the output relays, as they are blocked.*

27.3.3 TEST PORT STATUS CELL

This cell displays the status of the DDB signals that have been allocated in the ***Monitor Bit*** cells. If you move the cursor along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the IED. This allows you to test the Programmable Scheme Logic (PSL).

27.3.4 MONITOR BIT 1 TO 8 CELLS

The eight Monitor Bit cells allows you to select eight DDB signals that can be observed in the Test Port Status cell or downloaded via the front port.

Each Monitor Bit cell can be assigned to a particular DDB signal. You set it by entering the required DDB signal number from the list of available DDB signals.

The pins of the monitor/download port used for monitor bits are as follows:

Monitor Bit	1	2	3	4	5	6	7	8
Monitor/Download Port Pin	11	12	15	13	20	21	23	24

The signal ground is available on pins 18, 19, 22 and 25.



Caution:
The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.

27.3.5 TEST MODE CELL

This cell allows you to perform secondary injection testing. It also lets you test the output contacts directly by applying menu-controlled test signals.

To go into test mode, select the `Test Mode` option in the ***Test Mode*** cell. This takes the IED out of service causing an alarm condition to be recorded and the ***Out of Service*** LED to illuminate. This also freezes any information stored in the *CB CONDITION* column. In IEC 60870-5-103 protocol versions, it changes the Cause of Transmission (COT) to Test Mode. In IEC 61850 protocol, it changes the quality test flag to q.test = true. See section 10.1 for further detail of IEC 61850 test mode.

In Test Mode, the output contacts are still active. To disable the output contacts you must select the `Contacts Blocked` option.

Once testing is complete, return the device back into service by setting the ***Test Mode*** Cell back to `Disabled`.



Caution:
When the cell is in Test Mode, the Scheme Logic still drives the output relays, which could result in tripping of circuit breakers. To avoid this, set the *Test Mode* cell to `Contacts Blocked`.

Note:
`Test mode` and `Contacts Blocked` mode can also be selected by energising an opto-input mapped to the Test Mode signal, and the Contact Block signal respectively.

27.3.6 TEST PATTERN CELL

The ***Test Pattern*** cell is used to select the output relay contacts to be tested when the ***Contact Test*** cell is set to `Apply Test`. The cell has a binary string with one bit for each user-configurable output contact, which can be set to '1' to operate the output and '0' to not operate it.

27.3.7 CONTACT TEST CELL

When the `Apply Test` command in this cell is issued, the contacts set for operation change state. Once the test has been applied, the command text on the LCD will change to ***No Operation*** and the contacts will remain in the Test state until reset by issuing the `Remove Test` command. The command text on the LCD will show ***No Operation*** after the `Remove Test` command has been issued.

Note:
*When the **Test Mode** cell is set to `Contacts Blocked` the **Relay O/P Status** cell does not show the current status of the output relays and therefore cannot be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.*

27.3.8 TEST LEDS CELL

When the `Apply Test` command in this cell is issued, the user-programmable LEDs illuminate for approximately 2 seconds before switching off, and the command text on the LCD reverts to ***No Operation***.

27.3.9 TEST AUTORECLOSE CELL

Where the IED provides an auto-reclose function, this cell will be available for testing the sequence of circuit breaker trip and auto-reclose cycles.

The *Trip 3 Pole* option in the ***Test Autoreclose*** cell causes the device to perform the first three phase trip/ reclose cycle so that associated output contacts can be checked for operation at the correct times during the cycle. Once the trip output has operated the command text will revert to *No Operation* whilst the rest of the auto-reclose cycle is performed. To test subsequent three-phase autoreclose cycles, you repeat the *Trip 3 Pole* command. You can also test the single phases with *Trip Pole A*, *Trip Pole B* and *Trip Pole C*.

Note:
The default settings for the programmable scheme logic has the AR Trip Test signals mapped to the Trip Input signals. If the programmable scheme logic has been changed, it is essential that these signals retain this mapping for the Test Autoreclose facility to work.

27.3.10 STATIC TEST MODE

Static Test Mode can be set to *Enabled* or *Disabled*. When the Static Test mode is enabled it allows injection test that don't support dynamic switching to be used to commission and test the device.

Dynamic secondary injection test sets are able to accurately mimic real power system faults. The test sets mimic an instantaneous fault “shot”, with the real rate of rise of current, and the decaying DC exponential component. Dynamic injection test sets are available, which cater for all three phases, providing a six signal set of analogue inputs: Va, Vb, Vc, Ia, Ib, Ic. Such injection test sets can be used with the device, with no special testing limitations.

Static test sets, also known as Static Simulators, may not properly provide or simulate:

- A healthy pre-fault voltage
- A real fault shot (instead a gradually varying current or voltage would be used)
- The rate of rise of current and DC components
- A complete set of three-phase analogue inputs
- Real dynamic step changes in current and voltage.

Some of the protection in this product is based on delta techniques which recognise step changes in actual power system quantities. Because these may not be produced by static test sets,, certain functions are can be disabled or bypassed to allow injection testing with static test sets. Enabling the ***Static Test Mode*** option does this..

For the tests, the delta directional line is replaced by a conventional distance directional line. Extra filtering of distance comparators is used so the filtering slows to use a fixed one cycle window. Memory polarising is replaced by cross-polarising from unfaulted phases.

Note:
Trip times may be up to ½ cycle longer when tested in the static mode, due to the nature of the test voltage and current, and the slower filtering. This is normal, and perfectly acceptable.

27.3.11 LOOPBACK MODE

Loopback Mode can be used to test InterMiCOM^{64} signalling.

Note:
If the cell is set to Internal, only the IED software is checked. If the cell is set to External, both the software and hardware are checked.

When the device is switched into Loopback Mode, it automatically uses generic addresses 0-0. It responds as if it is connected to a remote device. The sent and received IM^{64} signals continue to be routed to and from the signals defined in the programmable logic.

Note:
Loopback mode can also be selected by energising an opto-input mapped to the Loopback signal.

27.3.12 IM64 TEST PATTERN

This cell is used with the ***IM64 Test Mode*** cell to set a 16-bit pattern (8 bits per channel), which is transmitted whenever the ***IM64 Test Mode*** cell is set to `Enabled`. The ***IM64 TestPattern*** cell has a binary string with one bit for each user-defined Inter-MiCOM command. These can be set to '1' to operate the IM64 output under test conditions and '0' for no operation.

27.3.13 IM64 TEST PATTERN CH1 & CH2

IM64 TestPattern CH1 and ***IM64 TestPattern CH2*** are used with the ***IM64 Test Mode*** cell to set a 64-bit pattern (32 bits per channel), which is transmitted whenever the ***IM64 Test Mode*** cell is `Enabled` and the ***Extended IM64*** mode is also `Enabled`. The ***IM64 TestPattern CH1*** and ***IM64 TestPattern CH2*** cells have a binary string with one bit for each user-defined Inter-MiCOM command. These can be set to '1' to operate the IM64 output under test conditions and '0' for no operation.

27.3.14 IM64 TEST MODE

When the `Enable` command in this cell is issued, the InterMiCOM^{64} commands change to reflect the state of the values set in the ***IM64 TestPattern*** cell. If the cell is set to Disabled, the InterMiCOM^{64} commands reflect the state of the signals generated by the protection and control functions.

When the ***Extended IM64*** mode is `Enabled`, two test pattern cells are used, ***IM64 TestPattern CH1*** and ***IM64 TestPattern CH2***.

27.3.15 RED AND GREEN LED STATUS CELLS

These cells contain binary strings that indicate which of the user-programmable red and green LEDs are illuminated when accessing from a remote location. A '1' indicates that a particular LED is illuminated.

Note:
*When the status in both **Red LED Status** and **Green LED Status** cells is '1', this indicates the LEDs illumination is yellow.*

27.4 COMMISSIONING EQUIPMENT

Specialist test equipment is required to commission this product. We recognise three classes of equipment for commissioning :

- Recommended
- Essential
- Advisory

Recommended equipment constitutes equipment that is both necessary, and sufficient, to verify correct performance of the principal protection functions.

Essential equipment represents the minimum necessary to check that the product includes the basic expected protection functions and that they operate within limits.

Advisory equipment represents equipment that is needed to verify satisfactory operation of features that may be unused, or supplementary, or which may, for example, be integral to a distributed control/automation scheme. Operation of such features may, perhaps, be more appropriately verified as part of a customer defined commissioning requirement, or as part of a system-level commissioning regime.

27.4.1 RECOMMENDED COMMISSIONING EQUIPMENT

The minimum recommended equipment is a multifunctional three-phase AC current and voltage injection test set featuring :

- Controlled three-phase AC current and voltage sources,
- Transient (dynamic) switching between pre-fault and post-fault conditions (to generate delta conditions),
- Dynamic impedance state sequencer (capable of sequencing through 4 impedance states),
- Integrated or separate variable DC supply (0 - 250 V)
- Integrated or separate AC and DC measurement capabilities (0-440V AC, 0-250V DC)
- Integrated and/or separate timer,
- Integrated and/or separate test switches.

In addition, you will need :

- A portable computer, installed with appropriate software to liaise with the equipment under test (EUT). Typically this software will be proprietary to the product's manufacturer (for example MiCOM S1 Agile).
- Suitable electrical test leads.
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- Continuity tester
- Verified application-specific settings files

For products that use fibre-optic communications to implement unit protection schemes :

- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm, OR single mode (according to the model variant) terminated with connectors as required by the product.
- Fibre-optic power meter
- P59x commissioning instructions

27.4.2 ESSENTIAL COMMISSIONING EQUIPMENT

As an absolute minimum, the following equipment is required:

- AC current source coupled with AC voltage source
- Variable DC supply (0 - 250V)

- Multimeter capable of measuring AC and DC current and voltage (0-440V AC, 0-250V DC)
- Timer
- Test switches
- Suitable electrical test leads
- Continuity tester

For products that use fibre-optic communications to implement unit protection schemes :

- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm, OR single mode (according to the model variant) terminated with connectors as required by the product.
- Fibre-optic power meter

Note:
If the AC test source that you are using is not capable of dynamic fault simulation (cannot dynamically switch from load to fault conditions) you must use the product's static test mode feature

Note:
To do this, in COMMISSION TESTS, set ***Static Test Mode*** *to* `Enabled`.

27.4.3 ADVISORY TEST EQUIPMENT

Advisory test equipment may be required for extended commissioning procedures:

- Current clamp meter
- Multi-finger test plug:
  - P992 for test block type P991
  - MMLB for test block type MMLG blocks
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- KITZ K-Bus - EIA(RS)232 protocol converter for testing EIA(RS)485 K-Bus port
- EIA(RS)485 to EIA(RS)232 converter for testing EIA(RS)485 Courier/IEC60870-5-103/DNP3 port
- A portable printer (for printing a setting record from the portable PC) and or writeable, detachable memory device
- Phase angle meter
- Phase rotation meter
- Fibre-optic power meter.
- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm terminated with BFOC (ST) 2.5 connectors for testing the fibre-optic RP1 port.

27.5 PRODUCT CHECKS

These product checks are designed to ensure that the device has not been physically damaged prior to commissioning, is functioning correctly and that all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the IED prior to commissioning, you should make a copy of the settings. This will allow you to restore them at a later date if necessary. This can be done by:

- Obtaining a setting file from the customer.
- Extracting the settings from the IED itself, using a portable PC with appropriate setting software.

If the customer has changed the password that prevents unauthorised changes to some of the settings, either the revised password should be provided, or the original password restored before testing.

Note:
If the password has been lost, a recovery password can be obtained from GE Vernova.

27.5.1 PRODUCT CHECKS WITH THE IED DE-ENERGISED



Warning:
The following group of tests should be carried out without the auxiliary supply being applied to the IED and, if applicable, with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the IED for these checks. If a P991 test block is provided, the required isolation can be achieved by inserting test plug type P992. This open circuits all wiring routed through the test block.

Before inserting the test plug, you should check the scheme diagram to ensure that this will not cause damage or a safety hazard (the test block may, for example, be associated with protection current transformer circuits). The sockets in the test plug, which correspond to the current transformer secondary windings, must be linked before the test plug is inserted into the test block.



Warning:
Never open-circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.

If a test block is not provided, the voltage transformer supply to the IED should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the IED terminals. Where means of isolating the auxiliary supply and trip circuit (for example isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

27.5.1.1 VISUAL INSPECTION



Warning:
Check the rating information under the top access cover on the front of the IED.



Warning:
Check that the IED being tested is correct for the line or circuit.



Warning:
Record the circuit reference and system details.



Warning:
Check the CT secondary current rating and record the CT tap which is in use.

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

27.5.1.2 CURRENT TRANSFORMER SHORTING CONTACTS

Check the current transformer shorting contacts to ensure that they close when the heavy-duty terminal block is disconnected from the current input board.

The heavy-duty terminal blocks are fastened to the rear panel using four crosshead screws. These are located two at the top and two at the bottom.

Note:
Use a magnetic bladed screwdriver to minimise the risk of the screws being left in the terminal block or lost.

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed.

27.5.1.3 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

27.5.1.4 EXTERNAL WIRING



Caution:
Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.

27.5.1.5 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

Terminals	Contact State with Product De-energised
11 - 12 on power supply board	Closed
13 - 14 on power supply board	Open

27.5.1.6 POWER SUPPLY

Depending on its nominal supply rating, the IED can be operated from either a DC only or an AC/DC auxiliary supply. The incoming voltage must be within the operating range specified below.

Without energising the IED measure the auxiliary supply to ensure it is within the operating range.

Nominal Supply Rating DC	Nominal Supply Rating AC RMS	DC Operating Range	AC Operating Range
24 - 54 V	N/A	19 to 65 V	N/A
48 - 125 V	30 - 100 V	37 to 150 V	24 - 110 V
110 - 250 V	100 - 240 V	87 to 300 V	80 to 265 V

Note:
The IED can withstand an AC ripple of up to 15% of the upper rated voltage on the DC auxiliary supply.



Warning:
Do not energise the IED or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.



Caution:
Energise the IED only if the auxiliary supply is within the specified operating ranges. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the IED.

27.5.2 PXXX_CI_PRODUCTCHECKSENERGISED



Warning:
The current and voltage transformer connections must remain isolated from the IED for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.

The following group of tests verifies that the IED hardware and software is functioning correctly and should be carried out with the supply applied to the IED.

27.5.2.1 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states when energised and healthy.

Terminals	Contact State with Product Energised
11 - 12 on power supply board	Open
13 - 14 on power supply board	Closed

27.5.2.2 TEST GRAPHICAL HMI

The Graphical HMI is designed to operate in a wide range of substation ambient temperatures. For this purpose, the IEDs have an ***LCD Brightness*** setting. The brightness is factory pre-set, but it may be necessary to adjust the contrast to give the best in-service display.

To change the contrast, you can increment or decrement the ***LCD Brightness*** cell in the *CONFIGURATION* column.



Caution:
Before applying a brightness setting, make sure that it will not make the display so light or dark that the menu text becomes unreadable. It is possible to restore the visibility of a display by downloading a setting file, and setting the LCD Brightness within the typical range of 7 - 11.

27.5.2.3 DATE AND TIME

The date and time is stored in memory, which is backed up by a supercapacitor.

The method for setting the date and time depends on whether an IRIG-B signal is being used or not. The IRIG-B signal will override the time, day and month settings, but not the initial year setting. For this reason, you must ensure you set the correct year, even if the device is using IRIG-B to maintain the internal clock.

You set the Date and Time by one of the following methods:

- Using the front panel to set the ***Date and Time*** cells respectively
- By sending a courier command to the ***Date/Time*** cell (Courier reference 0801)

Note:
If the auxiliary supply fails, the time and date will be maintained by the supercapacitor. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energised for approximately 30 seconds. On re energisation, the time should be correct.

When using IRIG-B to maintain the clock, the IED must first be connected to the satellite clock equipment (usually an RT430), which should be energised and functioning.

1. Set the IRIG-B Sync cell in the *DATE AND TIME* column to `Enabled`.
2. Ensure the IED is receiving the IRIG-B signal by checking that cell IRIG-B Status reads `Active`.
3. Once the IRIG-B signal is active, adjust the time offset of the universal co coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.
4. Check that the time, date and month are correct in the Date/Time cell. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.
5. Reconnect the IRIG-B signal.

If the time and date is not being maintained by an IRIG-B signal, ensure that the IRIG-B Sync cell in the *DATE AND TIME* column is set to `Disabled`.

1. Set the date and time to the correct local time and date using Date/Time cell or using the serial protocol.

27.5.2.4 TEST LEDS

On power-up, all LEDs should first flash yellow. Following this, the green "Healthy" LED should illuminate indicating that the device is healthy.

The IED's non-volatile memory stores the states of the alarm, the trip, and the user-programmable LED indicators (if configured to latch). These indicators may also illuminate when the auxiliary supply is applied.

If any of these LEDs are ON then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes off), no testing is needed for that LED because it is obviously operational.

27.5.2.5 TEST ALARM AND OUT-OF-SERVICE LEDS

The alarm and out of service LEDs can be tested using the *COMMISSION TESTS* menu column.

1. Set the ***Test Mode*** cell to `Contacts Blocked`.
2. Check that the out of service LED illuminates continuously and the alarm LED flashes.

It is not necessary to return the ***Test Mode*** cell to `Disabled` at this stage because the test mode will be required for later tests.

27.5.2.6 TEST TRIP LED

The trip LED can be tested by initiating a manual circuit breaker trip. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

27.5.2.7 TEST USER-PROGRAMMABLE LEDS

To test these LEDs, set the Test LEDs cell to `Apply Test`. Check that all user-programmable LEDs illuminate.

27.5.2.8 TEST OPTO-INPUTS

This test checks that all the opto-inputs on the IED are functioning correctly.

The opto-inputs should be energised one at a time. For terminal numbers, please see the external connection diagrams in the "Wiring Diagrams" chapter. Ensuring correct polarity, connect the supply voltage to the appropriate terminals for the input being tested.

The status of each opto-input can be viewed using either the ***Opto I/P Status*** cell in the *SYSTEM DATA* column, or the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column.

A '1' indicates an energised input and a '0' indicates a de-energised input. When each opto-input is energised, one of the characters on the bottom line of the display changes to indicate the new state of the input.

27.5.2.9 TEST OUTPUT RELAYS

This test checks that all the output relays are functioning correctly.

1. Ensure that the IED is still in test mode by viewing the ***Test Mode*** cell in the *COMMISSION TESTS* column. Ensure that it is set to `Contacts Blocked`.
2. The output relays should be energised one at a time. To select output relay 1 for testing, set the Test Pattern cell as appropriate.
3. Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagram.
4. To operate the output relay set the Contact Test cell to `Apply Test`.
5. Check the operation with the continuity tester.
6. Measure the resistance of the contacts in the closed state.
7. Reset the output relay by setting the Contact Test cell to `Remove Test`.
8. Repeat the test for the remaining output relays.
9. Return the IED to service by setting the Test Mode cell in the *COMMISSION TESTS* menu to `Disabled`.

27.5.2.10 TEST SERIAL COMMUNICATION PORT RP1

You need only perform this test if the IED is to be accessed from a remote location with a permanent serial connection to the communications port. The scope of this test does not extend to verifying operation with connected equipment beyond any supplied protocol converter. It verifies operation of the rear communication port (and if applicable the protocol converter) and varies according to the protocol fitted.

27.5.2.10.1 CHECK PHYSICAL CONNECTIVITY

The rear communication port RP1 is presented on terminals 16, 17 and 18 of the power supply terminal block. Screened twisted pair cable is used to make a connection to the port. The cable screen should be connected to pin 16 and pins 17 and 18 are for the communication signal:

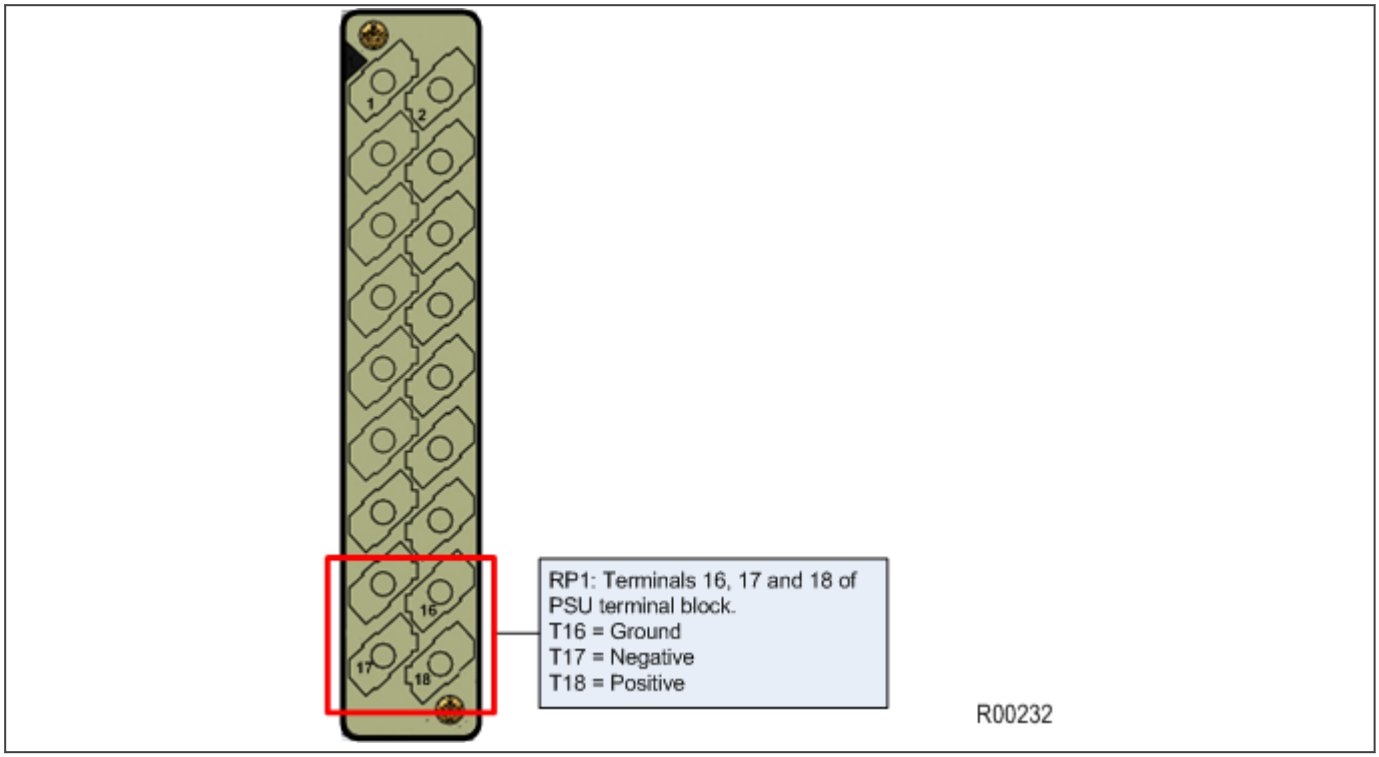


Figure 432: RP1 physical connection

For K-Bus applications, pins 17 and 18 are not polarity sensitive and it does not matter which way round the wires are connected. EIA(RS)485 is polarity sensitive, so you must ensure the wires are connected the correct way round (pin 18 is positive, pin 17 is negative).

If K-Bus is being used, a Kitz protocol converter (KITZ101, KITZ102 OR KITZ201) will have been installed to convert the K-Bus signals into RS232. Likewise, if RS485 is being used, an RS485-RS232 converter will have been installed. In the case where a protocol converter is being used, a laptop PC running appropriate software (such as MiCOM S1 Agile) can be connected to the incoming side of the protocol converter. An example for K-bus to RS232 conversion is shown below. RS485 to RS232 would follow the same principle, only using a RS485-RS232 converter. Most modern laptops have USB ports, so it is likely you will also require a RS232 to USB converter too.

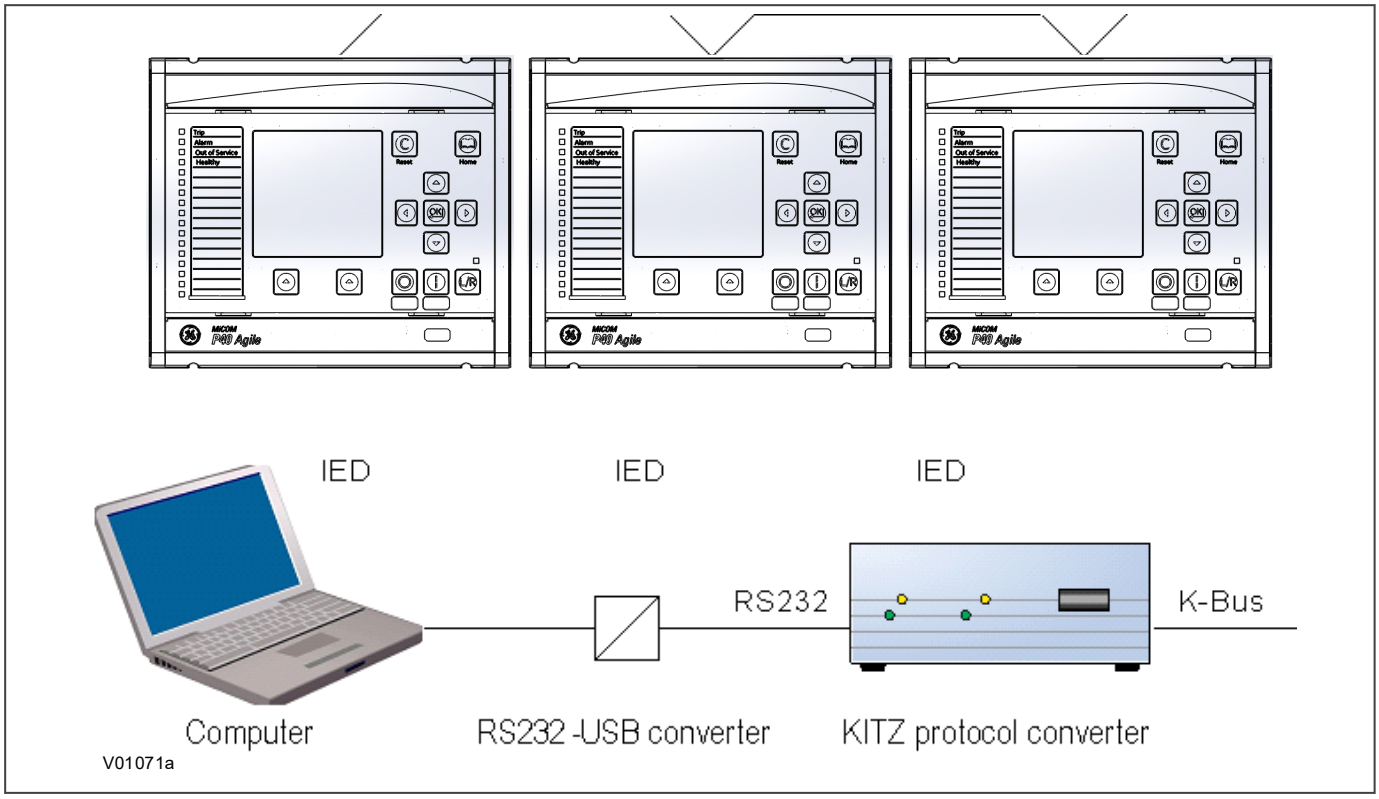


Figure 433: Remote communication using K-bus

Fibre connection

Some models have an optional fibre optic communications port fitted (on a separate communications board). The communications port to be used is selected by setting the Physical Link cell in the *COMMUNICATIONS* column, the values being `Copper` or `K-Bus` for the RS485/K-bus port and `Fibre Optic` for the fibre optic port.

27.5.2.10.2 CHECK LOGICAL CONNECTIVITY

The logical connectivity depends on the chosen data protocol, but the principles of testing remain the same for all protocol variants:

1. Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter.
2. For Courier models, ensure that you have set the correct RP1 address
3. Check that communications can be established with this IED using the portable PC/Master Station.

27.5.2.11 TEST SERIAL COMMUNICATION PORT RP2

RP2 is an optional second serial port board providing additional serial connectivity. It provides two 9-pin D-type serial port connectors SK4 and SK5. Both ports are configured as DTE (Date Terminal Equipment) ports. That means they can be connected to communications equipment such as a modem with a straight-through cable.

SK4 can be configured as an EIA(RS232), EIA(RS485), or K-Bus connection for Courier protocol only, whilst SK5 is fixed to EIA(RS)232 for InterMiCOM signalling only.

It is not the intention of this test to verify the operation of the complete communication link between the IED and the remote location, just the IED's rear communication port and, if applicable, the protocol converter.

The only checks that need to be made are as follows:

1. Set the ***RP2 Port Config*** cell in the *COMMUNICATIONS* column to the required physical protocol; (K-Bus, EIA(RS)485, or EIA(RS)232.
2. Set the IED's Courier address to the correct value (it must be between 1 and 254).

27.5.2.12 TEST ETHERNET COMMUNICATION

For products that employ Ethernet communications, we recommend that testing be limited to a visual check that the correct ports are fitted and that there is no sign of physical damage.

If there is no board fitted or the board is faulty, a NIC link alarm will be raised (providing this option has been set in the ***NIC Link Report*** cell in the *COMMUNICATIONS* column).

27.5.3 SECONDARY INJECTION TESTS

Secondary injection testing is carried out to verify the integrity of the VT and CT readings. All devices leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, you must set this in the Frequency cell in the *SYSTEM DATA* column.

The PMU must be installed and connected to a 1pps fibre optic synchronising signal and a demodulated IRIG-B signal, provided by a device such as a REASON RT430.

Connect the current and voltage outputs of the test set to the appropriate terminals of the first voltage and current channel and apply nominal voltage and current with the current lagging the voltage by 90 degrees.

27.5.3.1 TEST CURRENT INPUTS

This test verifies that the current measurement inputs are configured correctly.

1. Using secondary injection test equipment such as an Omicron, apply and measure nominal rated current to each CT in turn.
2. Check its magnitude using a multi-meter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the displayed value. The measured current values will either be in primary or secondary Amperes. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied current.

> *Note:*
> *If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

27.5.3.2 TEST VOLTAGE INPUTS

This test verifies that the voltage measurement inputs are configured correctly.

1. Using secondary injection test equipment, apply and measure the rated voltage to each voltage transformer input in turn.
2. Check its magnitude using a multimeter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the value displayed. The measured voltage values will either be in primary or secondary Volts. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be

equal to the applied voltage multiplied by the corresponding voltage transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied voltage.

Note:
If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

27.6 ELECTRICAL INTERMICOM COMMUNICATION LOOPBACK

If the IED is used in a scheme with standard InterMiCOM communication (Electrical Teleprotection), you need to configure a loopback for testing purposes.

27.6.1 SETTING UP THE LOOPBACK

The communication path may include various connectors and signal converters before leaving the substation. We therefore advise making the loopback as close as possible to where the communication link leaves the substation. This way, as much of the wiring as possible and all associated communication signal converters are included in the test.

1. Set *CONFIGURATION* > ***InterMiCOM*** to `Enabled`.
2. Set *INTERMICOM COMMS* > ***Ch Statistics*** and ***Ch Diagnostics*** to `Visible`.
3. Check that *INTERMICOM COMMS* > ***IM H/W Status*** displays OK. This means the InterMiCOM hardware is fitted and initialised.

27.6.2 LOOPBACK TEST

INTERMICOM COMMS > ***Loopback Mode*** allows you to test the InterMiCOM channel. In normal service it must be disabled. *INTERMICOM COMMS* > ***Loopback Status*** shows the status of the InterMiCOM loopback mode.

Note:
If INTERMICOM COMMS > ***Loopback Mode*** *is set to* `Internal`*, only the internal software of the device is checked. This is useful for testing functionality if no communications connections are made. Use the 'External' setting during commissioning because it checks both the software and hardware. When the IED is switched into either Internal or External Loopback Mode it automatically inhibits InterMiCOM messages to the PSL by setting all eight InterMiCOM message command states to zero.*

Set *INTERMICOM COMMS* > ***Loopback Mode*** to `External` and form a communications loopback by connecting the transmit signal (pin 2) to the receive signal (pin 3).

Note:
The DCD signal must be held high (by connecting pin 1 to pin 4) if the connected equipment does not support DCD.

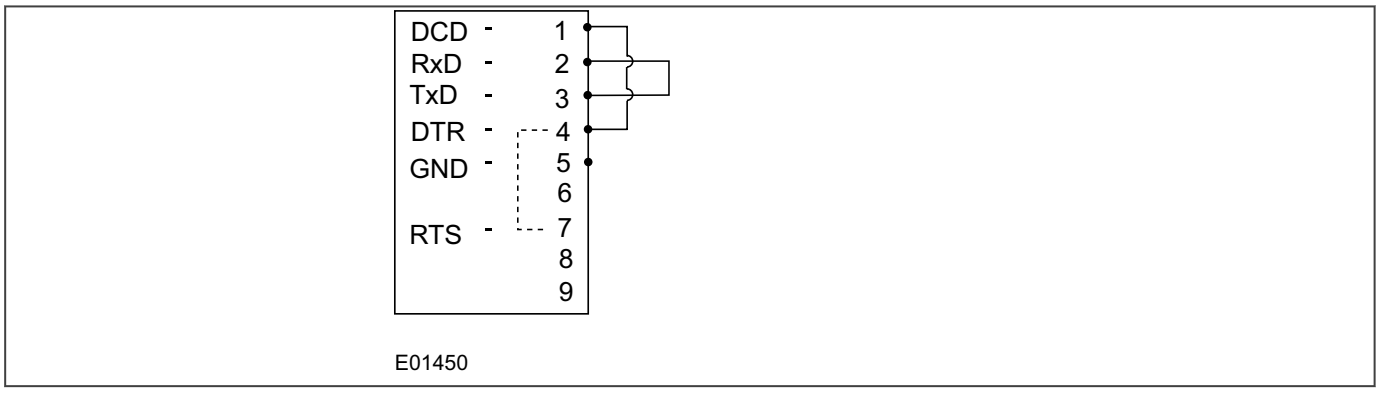


Figure 434: InterMicom loopback testing

The loopback mode is shown on the front panel by an Alarm LED and the message IM Loopback on the LCD.

Check that all connections are correct and the software is working correctly.

Check that *INTERMICOM COMMS* > ***Loopback Status*** shows OK.

27.6.2.1 INTERMICOM COMMAND BITS

To test the InterMiCOM command bits, go to the *INTERMICOM COMMS* column and do the following:

1. Enter any test pattern in the ***Test Pattern*** cell in the by scrolling through and changing selected bits between 1 and 0. The entered pattern is transmitted through the loopback.
2. Check that the ***IM Output Status*** cell matches the applied Test Pattern.
3. Check that all 8 bits in the ***IM Input Status*** cell are zero.

27.6.2.2 INTERMICOM CHANNEL DIAGNOSTICS

Check that the following cells in the *INTERMICOM COMMS* column all read **OK**.

- ***Data CD Status***
- ***FrameSync Status***
- ***Message Status***
- ***Channel Status***

27.6.2.3 SIMULATING A CHANNEL FAILURE

1. Simulate a failure of the communications link by breaking a connection and checking that some of these cells show **Fail**.
2. Restore the communications loopback and ensure that the four diagnostic cells display **OK.**

Note:
*Some or all of these cells show **Fail** depending on the communications configuration and the way the link has failed.*

27.7 INTERMICOM 64 COMMUNICATION

If the IED is used in a scheme with InterMiCOM^{64} communication, you need to configure a loopback for testing purposes.

IM64 is fibre-based. Several different fibre-optic interfaces are available. In general, 1550 nm single-mode fibres, or 1300 nm single-mode or multimode fibres are used for direct connection. 850 nm multimode fibres are generally used with multiplexing telecommunications equipment.

Note:
It is important that fibres used for testing are correct for the specified interface(s).

Optical fibres should be terminated with BFOC2.5 (ST2.5) connectors. For multimode applications use 50/125 µm core fibre. Make sure fibre test leads used for measurements are long enough for mode stripping (a method of reducing loss within the core). We recommend a minimum length of 10 m (30ft) for this.

If IEDs communicate using multiplexed electrical communication channels, a bidirectional optical-to-electrical signal converter, such as a P59x, is used. The P59x range consists of three devices: P591 for G703, P592 for V.35 and P593 for X.21.

The P59x is situated near the multiplexer, between the fibre from the IED and the electrical interface of the multiplexer. Apply the loopback either at the P59x or the multiplexer to ensure as much of the circuit as possible is tested. If the IED is connected to a multiplexer, the loopback testing is exactly the same whether connected directly or via a multiplexer. The P59x interface units require additional tests (see P59x documentation).

If Current Differential protection is used, set *CONFIGURATION* > ***Current Diff*** to `Enable`.

If Current Differential protection is not used, set *CONFIGURATION* > ***InterMiCOM64*** to `Enable`.



Warning:
NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.

27.7.1 CHECKING THE INTERFACE

Before carrying out the loopback test, you need to check that the interface is transmitting a suitable signal. To check this ...

1. Set *COMMISSION TESTS*> ***Loopback Mode*** to `External`.
2. Using an appropriate fibre-optic cable, connect the Channel 1 transmitter (TX1) to an optical power meter. Check that the average power transmitted is within the range given in the following table.
3. Record the transmit power level.
4. Repeat for Channel 2 if applicable.
5. Measure the received power strength at remote ends.

Power	850 nm Multi-Mode	1300 nm Multi-Mode	1300/1550 nm Single-Mode
Minimum transmitter power (average value)	-19 dBm	-6 dBm	-6 dBm
Receiver sensitivity (average power)	-32 dBm	-49 dBm	-49 dBm

Note:
*If CONFIGURATION > **InterMiCOM64** is set to `Enable`, the signals normally sent and received by and from the communications interface are routed to and from the signals defined in the Programmable Scheme Logic. If, however, COMMISSION TESTS > **IM64 Test Mode** is set to `Enabled`, an IM64 test pattern is transmitted instead.*

27.7.2 SETTING UP THE LOOPBACK

Set up a communications loopback for each of the two channels.

Where direct fibre connections are used (or where multiplexer channels conforming to the IEEE C37.94 standard are used), connect an appropriate fibre-optic cable from the channel transmitter to the channel receiver port on the rear of the device.

If the communications use P59x interface devices, connect the appropriate optical fibre(s) between the channel transmitter(s) on the IED used to make connection to the P59x optical receiver(s). Then commission the relevant P59x devices.

27.7.3 LOOPBACK TEST

1. Set *COMMISSION TESTS* > ***IM64 Test Mode*** to `Enabled`, and use *COMMISSION TESTS* > ***Test Pattern*** to set a bit pattern sent using the InterMiCOM^{64} loopback.
2. Check that *MEASUREMENTS 4* > ***IM64 Rx Status*** matches the test pattern set. The communication statistics show the number of valid and erroneous messages received.

Note:
*The propagation delay measurement is not valid in this mode of operation. The IED responds as if it is connected to a remote IED. It indicates a loopback alarm which can only be cleared by setting COMMISSION TESTS > **Loopback Mode** to `Disabled`.*

Note:
In loopback mode the signals sent and received through the protection communications interface continue to be routed to and from the signals defined in the programmable logic.

Note:
*A test pattern can also be sent to the remote end to test the whole InterMiCOM communication path. To do this, set COMMISSION TESTS >**IM64 Test Mode** to `Enable` and connect two ends. Take special care because the test pattern is executed using PSL at the remote end.*

27.8 GPS SYNCHRONISATION

The IED uses GPS timing information to align the local and remote current vectors in the current differential algorithm. A RT430 GPS synchronising unit is used to decode GPS signals and provide the synchronising signal.

If the IED uses GPS synchronisation, the associated RT430 unit needs to be commissioned according to the instructions in the RT430 Technical Manual.

27.8.1 GPS OPTICAL SIGNAL STRENGTH

Using the optical fibre connected to the RT430 optical transmitter:

1. With an optical cable connected to the RT430 optical transmitter, disconnect the other end of the cable from the IED.
2. Measure the received signal strength at the IED end. The value should be in the range -16.8 dBm to -25.4 dBm.
3. Record the value.
4. Restore the optical fibre connection to the IED



Warning:
NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.

27.8.2 CHECK SYNCHRONISATION SIGNAL AT THE IED

1. Connect the fibre from the RT430 to the IED's GPS port.
2. Set *PROT COMMS/IM64* > ***GPS Sync*** to `GPS -> Standard`. This enables GPS synchronisation.
3. In *MEASUREMENTS 4* > Channel Status, if the GPS synchronisation signal is being received, the display reads **11******** (where * is a ‘don’t care’ state for this test). This means both the Local GPS and Remote GPS are being received.
4. Check GPS failure condition by disconnecting the fibre from the RT430 and check that the display reverts to **00********.
5. Restore the GPS by reconnecting the fibre and check again that the display reads **11********.

27.9 SETTING CHECKS

The setting checks ensure that all of the application-specific settings (both the IED's function and Programmable Scheme Logic settings) have been correctly applied.

Note:
If applicable, the trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.

27.9.1 APPLY APPLICATION-SPECIFIC SETTINGS

There are two different methods of applying the settings to the IED

- Transferring settings to the IED from a pre-prepared setting file using MiCOM S1 Agile
- Enter the settings manually using the IED's front panel HMI

27.9.1.1 TRANSFERRING SETTINGS FROM A SETTINGS FILE

This is the preferred method for transferring function settings. It is much faster and there is a lower margin for error.

1. Connect a PC running the Settings Application Software to the IED's front port, or a rear Ethernet port. Alternatively connect to the rear Courier communications port, using a KITZ protocol converter if necessary.
2. Power on the IED
3. Enter the IP address of the device if it is Ethernet enabled
4. Right-click the appropriate device name in the System Explorer pane and select **Send**
5. In the **Send to** dialog select the setting files and click **Send**

Note:
*The device name may not already exist in the system shown in **System Explorer**. In this case, perform a **Quick Connect** to the IED, then manually add the settings file to the device name in the system. Refer to the Settings Application Software help for details of how to do this.*

27.9.1.2 CHANGING THE SETTINGS

1. Starting at the default display, highlight the required settings column/menu
2. Use the OK key to enter the highlighted settings menu.
3. To change the value of a setting, highlight the relevant cell in the menu, then press the **Enter** key to change the cell value. A settings screen will appear next to the cell. If the currently logged in user does not have the level of access required for changing the setting, a pop-up dialog box will inform the user and prevent the settings from being changed. Acknowledge the pop-up message, then navigate to the 'user accounts' section to the top of the screen (top banner) to enter the password for the required access level to change settings.
4. To change the value on the settings screen, use the cursor keys to change the desired settings. When more settings are available than can fit on the screen, a scroll bar on the right-hand side appears. In some cases, a virtual keyboard is provided to enter complex characters. The IED maintains dependencies between various settings, and only the applicable settings are displayed for changing.
5. Press the **Enter** key to confirm the new setting value or the **Clear** key or the on-screen 'x' to discard it.

6. To confirm the new settings, press the **Enter** key. Navigate away from the currently active group settings or press the **Home** key. A Settings update confirmation dialogue box will appear that requires choosing of one of the following options:
   a. Save - accept all settings including the recently changed settings
   b. Abort - discard recent changes and keep existing settings
   c. Stay on page - return to the active settings page without saving recent changes
7. To return to the top of the menu, hold down the **Up** cursor key for a second or so, or press the **Clear** key once. It is possible to move across columns from anywhere in the menu by using the Menu context keys at the bottom of the display.
8. To return to the default display, press the **Home** key at any time.
9. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.
10. The Date and time can be adjusted by navigating to the top banner and selecting the displayed time. Press the **Enter** key to adjust the date and time using the calendar/clock widget that pops up.

Note:
For the protection group and disturbance recorder settings, the changes are not saved unless confirmed using the Settings update confirmation prompt.

Note:
All other Control and support settings (such as Communications and Control inputs), however, are updated immediately after they are entered on the front HMI without the need to confirm using the Settings update confirmation prompt.

27.10 IEC 61850 EDITION 2 TESTING

27.10.1 USING IEC 61850 EDITION 2 TEST MODES

In a conventional substation, functionality typically resides in a single device. It is usually easy to physically isolate these functions, as the hardwired connects can simply be removed. Within a digital substation architecture however, functions may be distributed across many devices. This makes isolation of these functions difficult, because there are no physical wires that can be disconnected on an Ethernet network. Logical isolation of the various functions is therefore necessary.

With IEDs that support IEC 61850 Edition 2, it is possible to use a test mode to conduct online testing. The advantages of this are as follows:

- The IED can be placed into test mode, to allow testing the IED using test input signals, and with all protection functions and output contacts active.
- The IED can be placed into test/blocked mode, to allow testing the IED using test input signals, and with all protection functions active but output contacts disabled.
- GOOSE message outputs are tagged so that receiving devices can recognise they are test signals.
- An IED receiving simulated GOOSE or Sampled Value messages from test devices can differentiate these from normal process messages, and respond appropriately.

27.10.1.1 IED TEST MODE BEHAVIOUR

IEC 61850 Edition 2 defines how the IED responds to test messages in the IED test modes, and whether the relay output contacts are activated or not.

You can select the mode of operation of the P40 IED by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column.
- Using an IEC 61850 MMS control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the P40 IED behaviour under the different modes:

IED Test Mode Setting	IEC 61850 Mod	Result
Disabled	on	• Normal IED behaviour • IED only responds to incoming GOOSE and SV messages with quality q.test = false
Test	test	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are still active • IEC 61850 message outputs have 'quality' q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true
Contacts Blocked	test/blocked	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are disabled • IEC 61850 message outputs have quality q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

27.10.2 SIMULATED INPUT BEHAVIOUR

Simulated GOOSE messages and sampled value streams can be used during testing.

The ***Subscriber Sim*** setting in the *COMMISSION TESTS* column controls whether a device listens to simulated signals or to real ones. An IEC 61850 control service to System/LPHD.Sim can also be used to change this value.

The device may be presented with both real signals and test signals. An internal state machine is used to control how the device switches between signals:

- The IED will continue subscribing to the 'real' GOOSE1 (in green) until it receives the first simulated GOOSE 1 (in red). This will initiate subscription changeover.
- After changeover to this new state, the IED will continue to subscribe to the simulated GOOSE 1 message (in red). Even if this simulated GOOSE 1 message disappears, the real GOOSE 1 message (in green) will still not be processed. This means all Virtual Inputs derived from the GOOSE 1 message will go to their default state.
- The only way to bring the IED out of this state is to set the ***Subscriber Sim*** setting back to False. The IED will then immediately stop processing the simulated messages and start processing real messages again.
- During above steps, IED1 will continuously process the real GOOSE 2 and GOOSE 3 messages as normal because it has not received any simulated messages for these that would initiate a changeover.

The process is represented in the following figure:

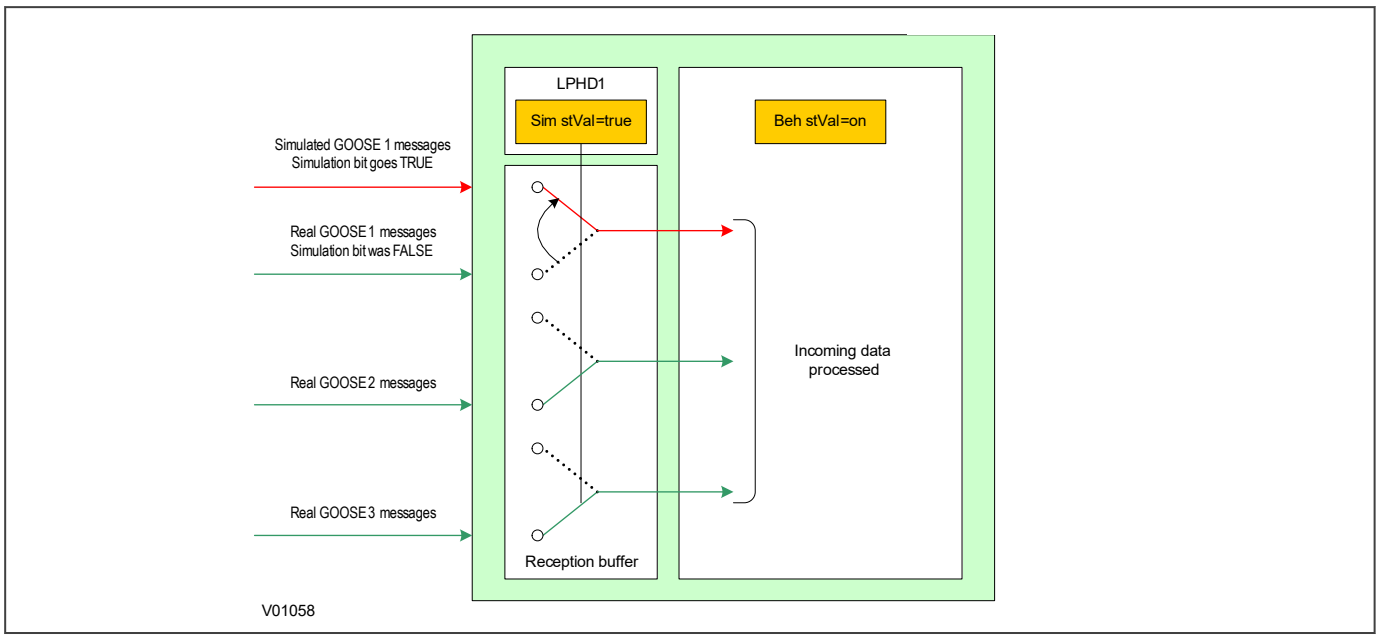


Figure 435: Simulated input behaviour

27.10.3 TESTING EXAMPLES

These examples show how you test the IED with and without simulated values. Depending on the IED Test Mode, it may respond by operating plant (for example by tripping the circuit breaker) or it may not operate plant.

27.10.3.1 TEST PROCEDURE FOR REAL VALUES

This procedure is for testing with real values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/eh***, and check that it shows `Test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Disabled`
4. Inject real signals using a test device connected to the merging units. The device will continue to listen to 'real' GOOSE messages and ignore simulated messages received.
5. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

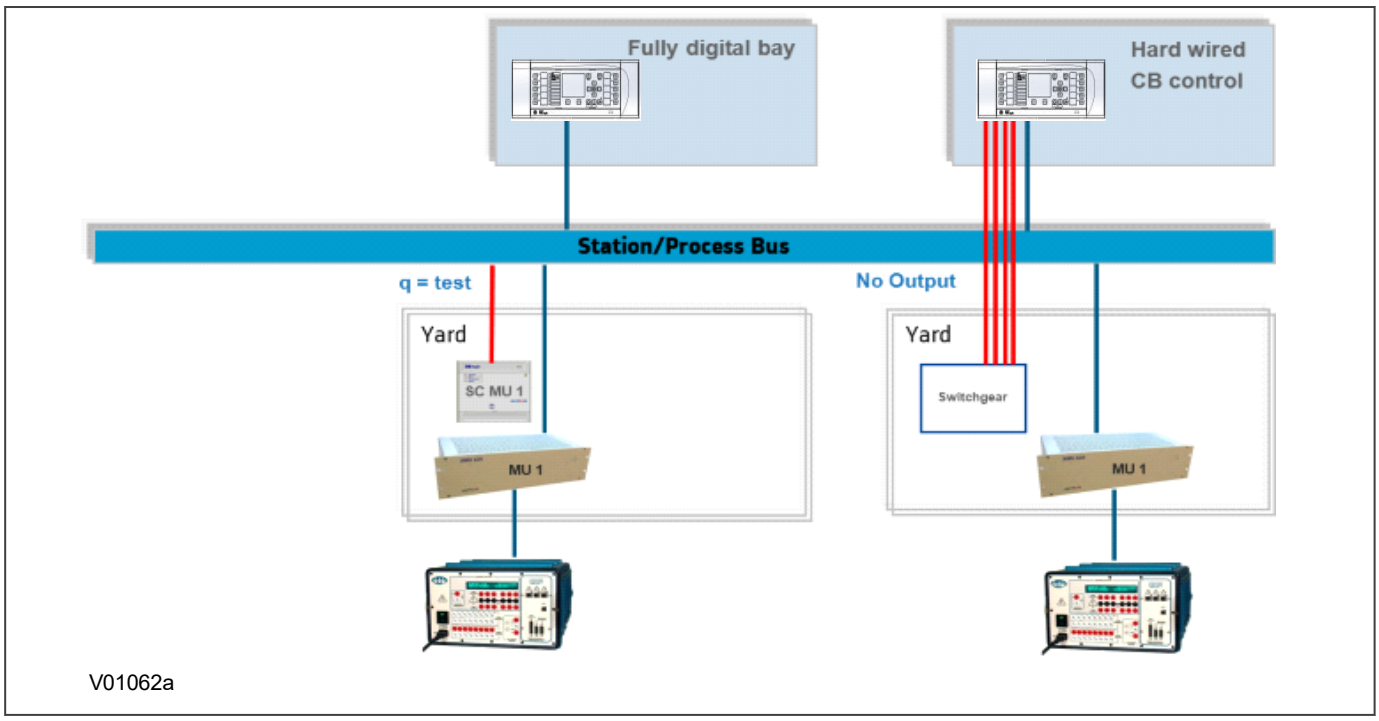


Figure 436: Test example 1

27.10.3.2 TEST PROCEDURE FOR SIMULATED VALUES - NO PLANT

This procedure is for testing with simulated values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`
4. Inject simulated signals using a test device connected to the Ethernet network. The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are

received, the corresponding ‘real’ messages are ignored until the device is taken out of test mode. Each message is treated separately, but sampled values are considered as a single message.

5. Verify function based on test signal outputs

   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

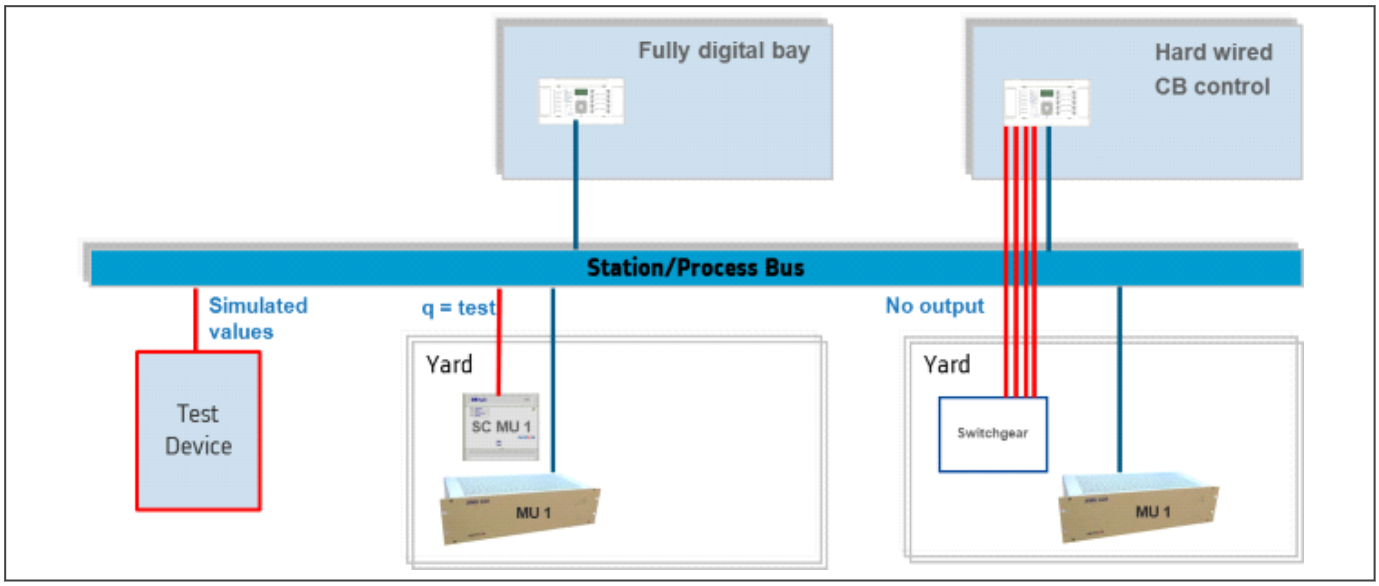


Figure 437: Test example 2

27.10.3.3 TEST PROCEDURE FOR SIMULATED VALUES - WITH PLANT

This procedure is for testing with simulated values with operating plant.

1. Set device into 'Contacts Blocked' Mode

   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Test`

2. Confirm new behaviour has been enabled

   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test`

3. Set device into Simulation Listening Mode

   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`

4. Inject simulated signals using a test device connected to the Ethernet network.

   The device will continue to listen to ‘real’ GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding ‘real’ messages are ignored until the device is taken out of IED test mode. Each message is treated separately, but sampled values are considered as a single message.

5. Verify function based on test signal outputs.

   Binary outputs (e.g. CB trips) will operate as normal. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram:

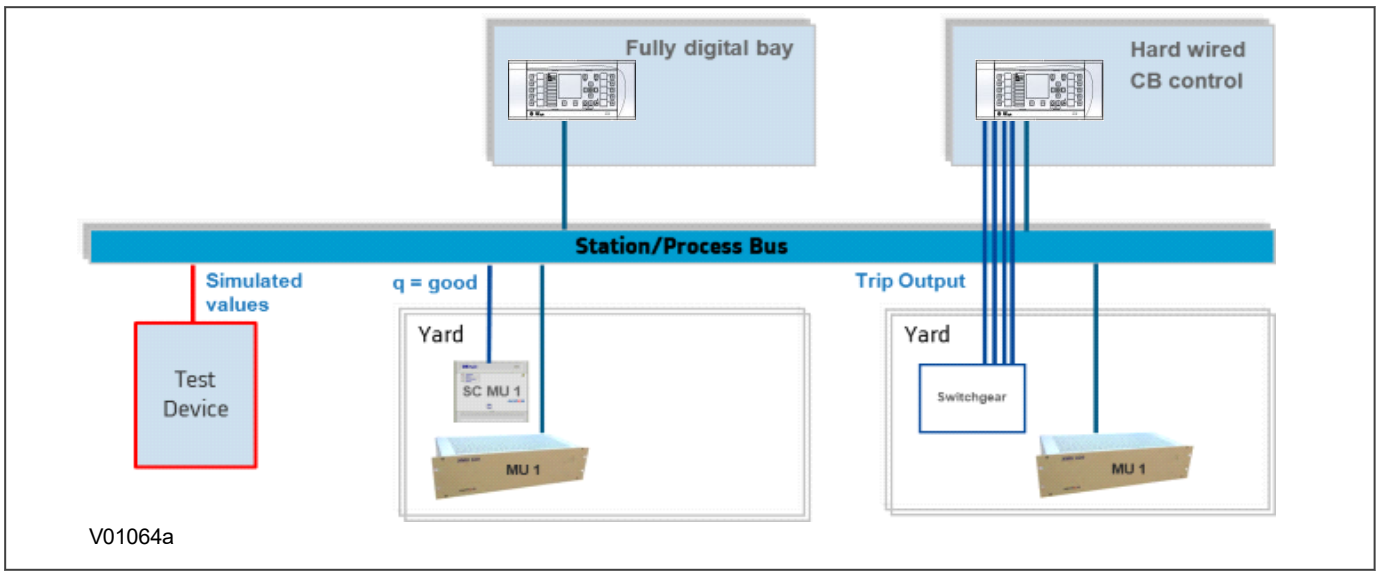


Figure 438: Test example 3

27.10.3.4 CONTACT TEST

The ***Apply Test*** command in this cell is used to change the state of the contacts set for operation.

If the device has been put into 'Contact Blocked' mode using an input signal (via the ***Block Contacts*** DDB signal) then the ***Apply Test*** command will not execute. This is to prevent a device that has been blocked by an external process having its contacts operated by a local operator using the HMI.

If the ***Block Contacts*** DDB is not set and the ***Apply Test*** command in this cell is issued, contacts change state and the command text on the LCD changes to `No Operation`. The contacts remain in the Test state until reset by issuing the ***Remove Test*** command. The command text on the LCD shows `No Operation` after the ***Remove Test*** command has been issued.

Note:
*When the **IED Test Mode** cell is set to Contacts Blocked, the **Relay O/P Status** cell does not show the current status of the output relays so cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.*

27.11 CURRENT DIFFERENTIAL PROTECTION

27.11.1 CURRENT DIFFERENTIAL BIAS CHARACTERISTIC

1. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
2. Make a note of which elements need to be re-enabled after testing.
3. Set the device to loopback mode, isolating it from the remote end.
4. Connect the test circuit shown below. Alternatively, use an injection test set to supply Ia and Ib

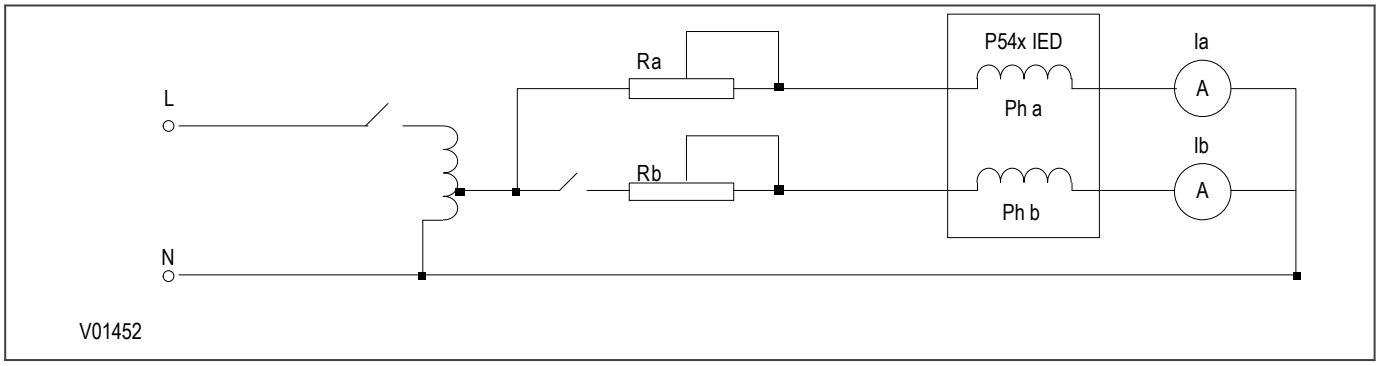


Figure 439: Current differential bias characteristics

27.11.1.1 LOWER SLOPE

If three LEDs have been assigned to provide phase segregated trip information (Trip A, Trip B and Trip C), these may be used to indicate correct operation per-phase. If LEDs are not used, use monitor options, as follows.

1. Go to *COMMISSION TESTS* > ***Monitor Bit***. Change cells 1, 2 and 3 to the values 523, 524 and 525 respectively. The ***Test Port Status*** cell then displays the status of Trip Output A (DDB 523), Trip Output B (DDB 524) and Trip Output C (DDB 525), with the rightmost bit representing Phase A Trip. From now on monitor the ***Test Port Status*** cell.
2. Make sure that the IED is in loopback mode by setting the Loopback Mode cell to External and applying a loop-back, either by direct fibre or using a P59x. Alternatively you can set the ***Test Loopback*** cell to `Internal`.
3. Adjust the variac and the resistor to give a bias current of 1pu in the A-phase (1A into terminals 3-2 for 1A applications, or 5A into terminals 1-2 for 5A applications).

   The device trips, contacts associated with the A-phase operate, and bit 1 (rightmost) of the ***Test Port Status*** cell is set to 1. Some LEDs, including the yellow alarm LED, switch OFF, but ignore these for the moment.
4. When the current in the A Phase is established, close the switch and slowly increase the current in the B phase from zero until Phase B trips (bit 2 of the ***Test Port Status*** cell is set to 1).

For the initial conditions where the magnitude of the bias current in phase A = 1 pu, record the phase B current magnitude and check that it corresponds to the following.

Connection Type	Magnitude of Current in Phase B
2-terminal & dual redundant	0.25 pu +/-10%
3-terminal	0.216 pu +/-10%

Assumption: Is1 = 0.2 pu, k1 = 30%, Is2 = 2.0 pu

For other differential settings or current injected into A phase (Ia), the following formula can be used (enter slope in pu form, which is. percentage/100):

Connection Type	Magnitude of Differential Current in Phase B
2-terminal & dual redundant	0.5 x (Is1 + (Ia x k1)) pu +/- 10%
3-terminal	0.333 x (Is1 + (1.5 x Ia x k1)) pu +/- 10

Assumption: Ia < Is2

Switch OFF the AC supply, read and clear all alarms.

27.11.1.2 UPPER SLOPE

1. Repeat the lower slope test but with the bias current set in the A-phase to 3 pu.
2. When the current in the A Phase is established, close the switch and slowly increase the current in the B phase from zero until phase B trips (bit 2 of the ***Test Port Status*** cell is set to 1).

For the initial conditions where the magnitude of the bias current in phase A = 3 pu, record the phase B current magnitude and check that it corresponds to the information below.

Connection Type	k2	Magnitude of Differential Current in Phase B
2-terminal & dual redundant	150%	1.15 pu +/- 10%
2-terminal & dual redundant	100%	0.9 pu +/- 10%
3-terminal	150%	1.51 pu +/- 10%
3-terminal	100%	1.1 pu +/- 10%

Assumption: Is1 = 0.2 pu, k1 = 30%, Is2 = 2.0 pu, k2 as above

For other differential settings or current injected into A phase (Ia), the formula below can be used (enter slopes in pu form, which is percentage/100):

Connection Type	Magnitude of Differential Current in Phase B
2-terminal & dual redundant	0.5 x [(Ia x k2) – {(k2 – k1) x Is2\- } + Is1] pu +/- 20%
3-terminal	0.333 x [(1.5 x Ia x k2) – {(k2 – k1) x Is2\- } + Is1] pu +/- 20%

Assumption: Ia > IS2

Switch OFF the ac supply and reset the alarms.

Note:
For 5 A applications, keep the duration of current injections short to avoid overheating of the variac or injection test set

27.11.2 CURRENT DIFFERENTIAL OPERATION AND CONTACT ASSIGNMENT

Phase A

1. Retaining the same test circuit as before, prepare for an instantaneous injection of 3 pu current in the A phase, with no current in the B phase (B phase switch open).
2. Set a timer to start when the fault injection is applied, and to stop when the trip occurs.
3. To verify the correct output contact mapping, use the trip contacts that would be expected to trip the circuit breaker(s), as shown below. For two breaker applications, stop the timer once both CB1 and CB2 trip contacts have closed. This can be achieved by connecting the contacts in series to stop the timer.

	Single Breaker	Two Circuit Breakers
Three Pole Tripping	Any Trip	Any Trip (CB1) and Any Trip (CB2)
Single Pole Tripping	Trip A	Trip A (CB1) and Trip A (CB2)

Phase B

1. Reconfigure the test equipment to inject fault current into the B phase.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to B phase operation close correctly.
3. Record the B phase trip time.
4. Switch OFF the ac supply and reset the alarms

Phase C

1. Repeat the above procedure for the C phase.
2. Switch OFF the ac supply and reset the alarms.

The average of the recorded operating times for the three phases should be less than 40 ms for 50 Hz, and less than 35 ms for 60 Hz when set for instantaneous operation.

Note:
For applications using magnetising inrush current restraint, use a test current higher than the Inrush High setting to obtain fast operating times. A setting of at least twice the Inrush High setting is recommended.

The expected operating time is typically within +/- 5% (for IDMT) or +/-2% (for DT) of that for the curve equation plus the “instantaneous” delay quoted above.

When the tests are completed, restore the original settings of any elements which were disabled for testing purposes. Use the *CONFIGURATION* column.

27.12 DISTANCE PROTECTION

27.12.1 DEPENDENCY CONDITIONS

Some protection elements can be set to have dependencies on the availability of the protection communication channel(s) and on the status of the voltage transformer supervision function (VTS).

If you are testing a distance model, the distance protection can be permanently enabled, or it can be set so that it is only enabled in the event of a failure of the protection communications channel(s).

The overcurrent and earth faults elements can be permanently enabled, or can be set so that they are only enabled:

- in the event of a failure of the protection communications channel(s)
- in the event of a VTS alarm
- according to a logical combination of both conditions.

If these elements are enabled with a dependency upon the above conditions, it is necessary to simulate the condition to test the correct operation of the protection function.

A communications failure can be simulated by setting the Test Loopback cell to Disabled and checking that the IED raises a Comms Fail alarm.

At the end of the test, clear the communications alarms and reset the statistics.

A VTS alarm can be raised by applying a 3-phase voltage to the VT inputs and then removing one phase voltage for a duration exceeding the VTS Time Delay setting.

At the end of the tests, clear the VTS alarm.

27.12.2 DISTANCE PROTECTION SINGLE-ENDED TESTING

If the distance protection function is being used, test the reaches and time delays.

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Disable the current differential function, directly or indirectly:
   a. If the distance element is enabled without dependency, disable the current differential element ***Current Diff***.
   b. If the distance protection is enabled with dependency on communication channel failure, the current differential element ***Current Diff*** should remain enabled and the communication should be disrupted to cause a suitable failure of the current differential protection
4. Make a note of which elements need to be re-enabled after testing

27.12.2.1 PRELIMINARIES

You should now connect the IED to equipment able to supply phase-phase and phase-neutral volts with current in the correct phase relation for a particular type of fault on the selected characteristic angle. The facility for altering the loop impedance (phase-to-ground fault or phase-phase) presented to the IED is essential.

Use a three-phase digital/electronic injection test set to make the commissioning procedure easier.

1. If testing the distance elements using using test sets that do not provide a dynamic model to generate true fault delta conditions, set *COMMISSION TESTS* > ***Static Test Mode*** to `Enabled`. When set, this disables phase selector control and forces the device to use a conventional (non-delta) directional line.
2. For lower specification test equipment that cannot apply a full three phase set of healthy simulated pre-fault voltages, the VT supervision may need to be disabled to avoid spurious pickup. Set *CONFIGURATION* > ***Supervision*** to `Disabled`.
3. Connect the test equipment to the device using the test block(s), taking care not to open-circuit any CT secondary windings. If using MMLG type test blocks, the live side of the test plug must be provided with shorting links before it is inserted into the test block.
4. When the test is complete, make sure *COMMISSION TESTS* > ***Static Test Mode*** is set back to `Disabled`.

27.12.2.2 ZONE 1 REACH CHECK

The zone 1 element is set to be directional forward.

1. Apply a dynamic A-phase-to-neutral fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ1 timer setting, but less than tZ2. These settings are in the *DISTANCE* column. No trip should occur, and the red Trip LED should remain OFF.
2. Reduce the impedance and reapply the simulated fault.
3. Repeat this procedure until a trip occurs. When this happens, the display shows **Alarms/Faults present** and the Alarm and Trip LEDs switch ON.
4. To view the alarm message, keep pressing the read key until the yellow alarm LED changes from flashing to being steadily on.
5. At the prompt Press clear to reset alarms, press the C key. This clears the fault record from the display.
6. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
7. Read and reset the alarms

Modern injection test sets usually calculate the expected fault loop impedance from the device settings. For those that do not, check the reach for phase-phase and confirm the operation of the contacts. The appropriate loop impedance is given by the vector sum:

Z1 + Z1 residual = Z1 + (Z1.kZN Res Comp ∠kZN Angle) Ω

27.12.2.3 ZONE 2 REACH CHECK

The zone 2 element is set to be directional forward.

1. Apply a dynamic B-C fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ2 timer setting, but less than tZ3. These settings are in the *DISTANCE* column. No trip should occur, and the red Trip LED should remain OFF.
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
4. Read and reset the alarms.

Modern injection test sets usually calculate the expected fault loop impedance from the device settings. For those that do not, check the reach for phase-phase and confirm the operation of the appropriate contacts. The appropriate loop impedance is now given by:

2 x Z2 Ω

27.12.2.4 ZONE 3 REACH CHECK

1. The zone 3 element is set to forward, reverse or offset. The current injected must be in the appropriate direction to match the setting in the *DISTANCE SETUP* column.
2. Apply a dynamic C-A fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ3 timer setting (typically tZ3 + 100 ms).
3. Repeat the test described above to find the zone reach.
4. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
5. Read and reset the alarms.
6. Check that the correct reverse offset (Z3') has been applied. The setting is in the ***Z3' Ph Rev Reach*** and ***Z3' Gnd Rev Reach*** cells.

27.12.2.5 ZONE 4 REACH CHECK

The zone 4 element is set to be directional reverse.

1. Apply a dynamic B-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZ4 timer setting (typically tZ4 + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the device trips. The measured impedance should be within +/- 10% of the expected reach.
4. Read and reset the alarms.

27.12.2.6 ZONE P REACH CHECK

The zone P element can be set to forward or reverse directional or offset. The current injected must be in the correct direction to match the setting in the *DISTANCE SETUP* column.

1. Apply a dynamic C-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZP timer setting (typically tZP + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the relay trips. The measured impedance should be within +/-10% of the expected reach.
4. Read and reset the alarms.

27.12.2.7 ZONE Q REACH CHECK

The zone Q element can be set to forward or reverse directional or offset. The current injected must be in the correct direction to match the setting in the *DISTANCE SETUP* column.

1. Apply a dynamic C-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZQ timer setting (typically tZQ + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the relay trips. The measured impedance should be within +/-10% of the expected reach.
4. Read and reset the alarms.

27.12.2.8 ZONE P REACH CHECK

The zone R element can be set to forward or reverse directional or offset. The current injected must be in the correct direction to match the setting in the *DISTANCE SETUP* column.

1. Apply a dynamic C-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZR timer setting (typically tZR + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the relay trips. The measured impedance should be within +/-10% of the expected reach.
4. Read and reset the alarms.

27.12.2.9 ZONE Q REACH CHECK

The zone S element can be set to forward or reverse directional or offset. The current injected must be in the correct direction to match the setting in the *DISTANCE SETUP* column.

1. Apply a dynamic C-N fault, slightly in excess of the expected reach. The duration of the injection should be in excess of the tZS timer setting (typically tZS + 100 ms).
2. Repeat the test described above to find the zone reach.
3. Record the impedance at which the relay trips. The measured impedance should be within +/-10% of the expected reach.
4. Read and reset the alarms.

27.12.2.10 RESISTIVE REACH

This is for quadrilateral characteristics only.

Check that the correct settings for phase and ground element resistive reaches have been applied. The relevant settings are:

- R1Ph, R2Ph, R3Ph, R3Ph reverse, R4Ph and RP Ph for phase fault zones.
- R1Gnd, R2Gnd, R3Gnd, R3Gnd reverse, R4Gnd and RP Gnd for ground fault zones.

> *Note:*
> *Zone 3 has an independent setting for the forward resistance reach (right-hand resistive reach line), and the reverse resistance reach (left-hand resistive reach line).*

27.12.2.11 LOAD BLINDER

1. Check that the correct settings for the load blinder have been applied. The settings are at the end of the *DISTANCE SETUP* column.
2. Verify that the ***Load B/Angle*** cell is set at least 10 degrees less than the ***Line Angle*** setting in the *LINE PARAMETERS* column.

27.12.3 OPERATION AND CONTACT ASSIGNMENT

You should inject a fault at half Z1 reach with the intention of causing a distance protection trip.

27.12.3.1 PHASE A

1. Prepare a dynamic A-phase-to-neutral fault, as detailed above.
2. Set a timer to start when the fault injection is applied and to stop when the trip occurs.
3. To verify correct output contact mapping use the trip contacts that would be expected to trip the circuit breaker(s) (Any Trip for 3-pole tripping, Trip A for single pole tripping).

4. For two breaker applications, stop the timer when CB1 and CB2 trip contacts have both closed. Monitor by connecting the contacts in series to stop the timer if necessary.
5. Record the phase A trip time.
6. Switch OFF the AC supply and reset the alarms.

27.12.3.2 PHASE B

1. Reconfigure to test a B phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to B phase operation close correctly.
3. Record the phase B trip time.
4. Switch OFF the AC supply and reset the alarms.

27.12.3.3 PHASE C

1. Reconfigure to test a C phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to C phase operation close correctly.
3. Record the phase C trip time.
4. Switch OFF the AC supply and reset the alarms.

The average of the recorded operating times for the three phases should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.

Note:
Where a non-zero time delay is set in the DISTANCE menu column, the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" delay.

27.12.3.4 TIME DELAY SETTINGS

Check that the correct time delay settings have been applied. The relevant settings are in the *SCHEME LOGIC* column and are as follows:

- tZ1 Ph Time Delay and tZ1 Gnd Time Delay
- tZ2 Ph Time Delay and tZ2 Gnd Time Delay
- tZ3 Ph Time Delay and tZ3 Gnd Time Delay
- tZP Ph Time Delay and tZP Gnd Time Delay
- tZ4 Ph Time Delay and tZ4 Gnd Time Delay
- tZQ Ph Time Delay and tZQ Gnd Time Delay
- tZR Ph Time Delay and tZR Gnd Time Delay
- tZS Ph Time Delay and tZS Gnd Time Delay

Note:
The device allows separate time delay settings for phase ("Ph") and ground ("Gnd") fault elements. BOTH must be checked to ensure that they have been set correctly.

27.12.4 SCHEME TESTING

The device is tested for its response to internal and external fault simulations but the response depends on the aided channel (pilot) scheme selected. The response to the 'Reset Z1 Extension' opto-input is shown in the case of a Zone 1 Extension scheme.

We assume a conventional signalling scheme implementation.

If an InterMiCOM^{64} scheme is used to provide the signalling, the scheme logic may not use opto-inputs for the aided scheme implementation. In this case, internal DDB signals need to be set or reset to test the operation of the protection scheme.

Use the IM64 Test Mode with the IM64 Test Pattern to assert or monitor the relevant signals.

Ensure that the injection test set timer is still connected to measure the time taken for the device to trip. A series of fault injections are applied, with a Zone 1, end-of-line, or Zone 4 fault simulated. At this stage, note the method in which each fault is applied, but do not inject yet:

- **Zone 1 fault**: A dynamic forward A-B fault at half the Zone 1 reach is simulated.
- **End of line fault**: A dynamic forward A-B fault at the remote end of the line is simulated. The fault impedance simulated should match the *LINE PARAMETERS* > ***Line Impedance*** setting.
- **Zone 4 fault**: A dynamic reverse A-B fault at half the Zone 4 reach is simulated.

The following table indicates the expected response for various test situations for a conventional signalling scheme.

Fault Type Simulated	IED Response					
	Forward Fault in Zone 1		Forward Fault at End of Line (Within Z1X/Z2)		Reverse Fault in Zone 4	
Signal receive opto	ON	OFF	ON	OFF	ON	OFF
Zone 1 extension	Trip	Trip	No Trip	Trip	No Trip	No Trip
Blocking scheme	Trip, No Signal Send	Trip, No Signal Send	No Trip, No Signal Send	Trip, No Signal Send	No Trip, Signal Send	No Trip, Signal Send
Permissive scheme (PUR/PUTT)	Trip, Signal Send	Trip, Signal Send	Trip, No Signal Send	No Trip, No Signal Send	No Trip, No Signal Send	No Trip, No Signal Send
Permissive scheme (POR/POTT)	Trip, Signal Send	Trip, Signal Send	Trip, Signal Send	No Trip, Signal Send	No Trip, No Signal Send	No Trip, No Signal Send

27.12.4.1 SCHEME TRIP TEST FOR ZONE 1 EXTENSION

1. Energise the ***Reset Z1X*** (Reset Zone 1 Extension) opto-input. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, or station battery.
2. Inject an end of line fault. The duration of injection should be set to 100 ms. No trip should occur.
3. De-energise the ***Reset Z1X*** opto-input
4. Repeat the test injection and record the operating time. This should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.
5. Switch OFF the AC supply and reset the alarms.

Note:
Here a non-zero tZ1 Ph or tZ1 Gnd time delay is set in the DISTANCE column, the expected operating time is typically within +/- 5% of the tZ1 setting plus the "instantaneous" delay quoted above.

27.12.4.2 SCHEME TRIP TESTS FOR PERMISSIVE SCHEMES

This test applies to both Permissive Underreach, and Permissive Overreach aided scheme applications.

1. Energise the ***Signal Receive*** opto-input. This is done by applying a continuous DC voltage onto the required opto-input from the test set, or station battery.
2. Inject an end of line fault, and record the operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.
3. Switch OFF the AC supply and reset the alarms.
4. De-energise the ***Signal Receive*** opto-input (remove the temporary energisation link, to turn it OFF).

Note:
Where a non-zero Aided Distance Dly time delay is set in the DISTANCE menu column, the expected operating time is typically within +/- 5% of the tZ1 setting plus the "instantaneous" delay quoted above.

27.12.4.3 SCHEME TRIP TESTS FOR BLOCKING SCHEME

1. Energise the ***Signal Receive*** opto-input. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, or station battery.
2. Inject an end of line fault. The duration of injection should be set to 100 ms. No trip should occur.
3. De-energise the ***channel received*** opto-input.
4. Repeat the test injection, and record the operating time.
5. Switch OFF the AC supply and reset the alarms.

Note:
For blocking schemes, a non-zero Aided Distance Dly time delay is set, so the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" operating delay. The trip time should thus be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz, plus 1.05 x Delay setting.

27.12.4.4 SIGNAL SEND TEST FOR PERMISSIVE SCHEMES

This test applies to both Permissive Underreach, and Permissive Overreach scheme applications.

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the ***Signal Send*** contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Inject a Zone 1 fault, and record the ***Signal Send*** contact operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
3. Switch OFF the AC supply and reset the alarms.

27.12.4.5 SIGNAL SEND TEST FOR BLOCKING SCHEME

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the Signal Send contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Inject a Zone 4 fault, and record the signal send contact operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
3. Switch OFF the ACsupply and reset the alarms.

27.12.4.6 SCHEME TIMER SETTINGS

1. Check that the correct time delay settings have been applied. The relevant settings in the *AIDED SCHEMES* column are:
   a. ***tRev. Guard*** (if applicable/visible)
   b. ***Unblocking Delay*** (if applicable/visible)
   c. ***WI Trip Delay*** (if applicable/visible)
2. When the tests are completed, restore all settings that were disabled for testing purposes.
3. Set the ***Static Test Mode*** to `Disabled`.
4. Remove any wires or leads temporarily fitted to energise the channel receive opto-input

27.13 DELTA DIRECTIONAL COMPARISON

27.13.1 SINGLE-ENDED TESTING

If the delta directional comparison aided scheme is being used, test the operation

1. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
2. Make a note of which elements need to be re-enabled after testing

27.13.1.1 PRELIMINARIES

Use a three-phase digital/electronic injection test set to make the commissioning procedure easier.

Connect the test equipment to the device using the test block(s) taking care not to open-circuit any CT secondary. If MMLG type test blocks are used, the live side of the test plug must be provided with shorting links before it is inserted into the test block.

27.13.1.2 SINGLE-ENDED INJECTION TEST

This set of injection tests aims to determine correct operation of a single IED at one end of the scheme. The device is tested in isolation, with the communications channel to the remote line terminal disconnected.

First verify that the device cannot send or receive channel scheme signals to or from the remote line end.

The device is tested for its response to forward and reverse fault injections, but the response depends on the aided channel (pilot) scheme that is selected. The table below shows the expected response for various test situations for a conventional signalling scheme.

We assume a conventional signalling scheme implementation.

If an InterMiCOM^{64} scheme is used to provide the signalling, the scheme logic may not use opto-inputs for the aided scheme implementation. In this case, internal DDB signals need to be set or reset to test the operation of the protection scheme.

Use the IM64 Test Mode with the IM64 Test Pattern to assert or monitor the relevant signals.

Direction of Fault Test Injection	IED Response			
	Forward Fault		Reverse Fault	
Signal receive opto	ON	OFF	ON	OFF
Blocking scheme	No Trip, No Signal Send	Trip, No Signal Send	No Trip, Signal Send	No Trip, Signal Send
Permissive scheme (POR/POTT)	Trip, Signal Send	No Trip, Signal Send	No Trip, No Signal Send	No Trip, No Signal Send

27.13.1.3 FORWARD FAULT PREPARATION

Configure the test set to inject a dynamic sequence of injection, as follows:

1. Simulate a healthy three-phase set of balanced voltages, each of magnitude Vn. No load current should be simulated. The duration of injection should be set to 1 second. Step 1 therefore mimics a healthy unloaded line before the onset of a fault.
2. Simulate a forward fault on the A-phase. The A-phase voltage must be simulated to drop by 3 times the ***Dir. V Fwd*** setting,

Va = Vn – 3 (***Dir. V Fwd***)

The fault current on the A-phase should be set to 3 times the Dir. I Fwd setting, lagging Va by a phase angle equal to the line angle,

Ia = 3 (Dir. I Fwd)∠-θ Line

Phases B and C should retain their healthy pre-fault voltage, and no current. The duration of injection should be set to 100 ms longer than the ***Aid. 1 Delta Dly***, ***Aid. 2 Delta Dly*** time setting.

27.13.2 OPERATION AND CONTACT ASSIGNMENT

You should inject a forward fault with the intention of causing a scheme trip. For a Permissive scheme, the Signal Receive opto-input needs to be energised. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, or station battery.

For a Blocking scheme, the opto-input should remain de-energised.

27.13.2.1 PHASE A

1. Prepare a dynamic A-phase-to-neutral fault, as detailed above.
2. Set a timer to start when the fault injection is applied and to stop when the trip occurs.
3. To verify correct output contact mapping use the trip contacts that would be expected to trip the circuit breaker(s) (Any Trip for 3-pole tripping, Trip A for single pole tripping).
4. For two breaker applications, stop the timer when CB1 and CB2 trip contacts have both closed. Monitor by connecting the contacts in series to stop the timer if necessary.
5. Record the phase A trip time.
6. Switch OFF the AC supply and reset the alarms.

27.13.2.2 PHASE B

1. Reconfigure to test a B phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to B phase operation close correctly.
3. Record the phase B trip time.
4. Switch OFF the AC supply and reset the alarms.

27.13.2.3 PHASE C

1. Reconfigure to test a C phase fault.
2. Repeat the test, this time ensuring that the breaker trip contacts relative to C phase operation close correctly.
3. Record the phase C trip time.
4. Switch OFF the AC supply and reset the alarms.

The average of the recorded operating times for the three phases should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz when set for instantaneous operation.

Note:
Where a non-zero time delay is set in the DISTANCE menu column, the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" delay.

27.13.3 DELTA PROTECTION SCHEME TESTING

27.13.3.1 SIGNAL SEND TEST FOR PERMISSIVE SCHEMES

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the ***Signal Send*** contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Repeat the forward fault injection, and record the ***Signal Send*** contact operating time. The measured operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
3. Switch OFF the AC supply and reset the alarms.

27.13.3.2 SIGNAL SEND TEST FOR BLOCKING SCHEMES

Configure the test set to inject a dynamic sequence of injection, as follows:

1. Simulate a healthy three-phase set of balanced voltages, each of magnitude Vn. No load current should be simulated. The duration of injection should be set to 1 second. Step 1 therefore mimics a healthy unloaded line, prior to the onset of a fault.
2. Simulate a reverse fault on the A-phase. The A-phase voltage must be simulated to drop by 3 times the Dir. V Rev setting; Va = Vn – 3(Dir. V Rev)
3. The fault current on the A-phase should be set to 3 times the DI Rev setting, and in antiphase to the forward injections; Ia = 3 (Dir. I Rev) ∠180°-θ Line
4. Prepare the dynamic A phase reverse fault, as detailed above. Ensure that the test set is simulating Steps 1 and 2 as one continuous transition.
5. Set a timer to start when the fault injection is applied, and to stop when the Delta scheme Signal Send contact closes.
6. Apply the test, and record the signal send contact response time. The recorded operating time should typically be less than 20 ms for 50 Hz, and less than 16.7 ms for 60 Hz applications.
7. Switch OFF the AC supply and reset the alarms.



Caution:
When the tests are completed, restore all settings that were disabled for testing purposes.



Caution:
Remove any wires or leads temporarily fitted to energise the channel receive opto-input.

27.14 DEF AIDED SCHEMES

27.14.1 DEPENDENCY CONDITIONS

Some protection elements can be set to have dependencies on the availability of the protection communication channel(s) and on the status of the voltage transformer supervision function (VTS).

If you are testing a distance model, the distance protection can be permanently enabled, or it can be set so that it is only enabled in the event of a failure of the protection communications channel(s).

The overcurrent and earth faults elements can be permanently enabled, or can be set so that they are only enabled:

- in the event of a failure of the protection communications channel(s)
- in the event of a VTS alarm
- according to a logical combination of both conditions.

If these elements are enabled with a dependency upon the above conditions, it is necessary to simulate the condition to test the correct operation of the protection function.

A communications failure can be simulated by setting the Test Loopback cell to Disabled and checking that the IED raises a Comms Fail alarm.

At the end of the test, clear the communications alarms and reset the statistics.

A VTS alarm can be raised by applying a 3-phase voltage to the VT inputs and then removing one phase voltage for a duration exceeding the VTS Time Delay setting.

At the end of the tests, clear the VTS alarm.

27.14.2 EARTH CURRENT PILOT SCHEME

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Disable the current differential function, directly or indirectly:
   a. If the distance element is enabled without dependency, disable the current differential element ***Current Diff***.
   b. If the distance protection is enabled with dependency on communication channel failure, the current differential element ***Current Diff*** should remain enabled and the communication should be disrupted to cause a suitable failure of the current differential protection
4. Make a note of which elements need to be re-enabled after testing

We assume a conventional signalling scheme implementation.

If an InterMiCOM^{64} scheme is used to provide the signalling, the scheme logic may not use opto-inputs for the aided scheme implementation. In this case, internal logic signals (DDBs) need to be set or reset to test the operation of the protection scheme.

The IM64 Test Mode in conjunction with the IM64 Test Pattern should be used to assert or monitor the relevant signals.

This set of injection tests aims to determine that a single device, at one end of the scheme is performing correctly.

> *Note:*
> *The device must be tested in isolation, with the communications channel to the remote line terminal disconnected.*

27.14.2.1 PRELIMINARIES

1. Determine which output relays have been selected to operate when a DEF trip occurs, by viewing the programmable scheme logic. If the trip outputs are phase segregated (a different output relay allocated for each phase), the output relay assigned for tripping on 'A' phase faults should be used.
2. Connect the output relay so that its operation will trip the test set and stop the timer.
3. Connect the current output of the test set to the 'A' phase current transformer input
4. Connect, all three phase voltages Va, Vb, and Vc.
5. Depending on the test equipment used, make sure the timer is set to start when the current is applied.

27.14.2.2 PERFORM THE TEST

1. Ensure that the timer is reset and prepare the following test shot.
2. Simulate a forward fault on the A-phase. The A-phase voltage must be simulated to drop by 4 times the ***DEF VNpol Set*** setting; Va = Vn - 4 (DEF Vpol)
3. Set the fault current on the A-phase should to 2 times the DEF Threshold setting, and in the forward direction. For a forward fault, the current Ia should lag the voltage Va by the DEF Char Angle setting; Ia = 2 (IN DEF Threshold $\angle \theta$ DEF)
4. Phases B and C should retain their healthy pref-ault voltage, and no current. The duration of the injection should be in excess of the DEF Delay setting (typically ***Aid. 1 DEF Dly.*** and ***Aid. 2 DEF Dly.*** + 100 ms).

Direction of Fault Test Injection	IED Response			
	Forward Fault		Reverse Fault	
Signal receive opto	ON	OFF	ON	OFF
Blocking scheme	No Trip, No Signal Send	Trip, No Signal Send	No Trip, Signal Send	No Trip, Signal Send
Permissive scheme (POR/POTT)	Trip, Signal Send	No Trip, Signal Send	No Trip, No Signal Send	No Trip, No Signal Send

27.14.2.3 FORWARD FAULT TRIP TEST

A forward fault is now injected as described, with the intention to cause a scheme trip.

For a permissive scheme, the ***Signal Receive*** opto-input should be energised. This is done by applying a continuous DC voltage onto the required opto-input, either from the test set, station battery, or IED field voltage. The commissioning engineer decides on the best method.

For a blocking scheme, the opto-input should remain de-energised ("OFF").

1. Apply the fault and record the (phase A) trip time.
2. Switch OFF the AC supply and reset the alarms.

The aided earth fault (DEF) scheme trip time for POR schemes (permissive overreach) POR schemes should be less than 40 ms.

For blocking schemes, where a non-zero ***DEF Dly*** time delay is set, the expected operating time is typically within +/- 5% of the delay setting plus the "instantaneous" (40 ms) delay quoted above.

There is no need to repeat the test for phases B and C, as these trip assignments have already been proven by the distance/delta trip tests.

27.14.3 SCHEME TESTING

27.14.3.1 SIGNAL SEND TEST FOR PERMISSIVE SCHEMES

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the ***Signal Send*** contact (the contact that would normally be connected to the pilot/signalling channel).
2. Repeat the forward fault injection, and record the ***Signal Send*** contact operating time. The measured operating time should typically be less than 40 ms.
3. Switch OFF the AC supply and reset the alarms.

27.14.3.2 SIGNAL SEND TEST FOR BLOCKING SCHEMES

1. Reconnect the test set so that the timer is no longer stopped by the Trip contact, but is now stopped by the Signal Send contact. This is the contact that would normally be connected to the pilot/signalling channel.
2. Reverse the current flow direction on the A phase to simulate a reverse fault.
3. Perform the reverse fault injection and record the signal send contact operating time. The measured operating time should typically be less than 40 ms.
4. Switch OFF the AC supply and reset the alarms.



Caution:
When the tests are completed, restore all settings that were disabled for testing purposes.



Caution:
Remove any wires or leads temporarily fitted to energise the channel receive opto-input.

27.15 OUT OF STEP PROTECTION

For this test, an injection set with a state sequencer function is required, as dynamic impedance conditions are going to be tested. The four states impedances that applied during the Out of Step commissioning process are shown below:

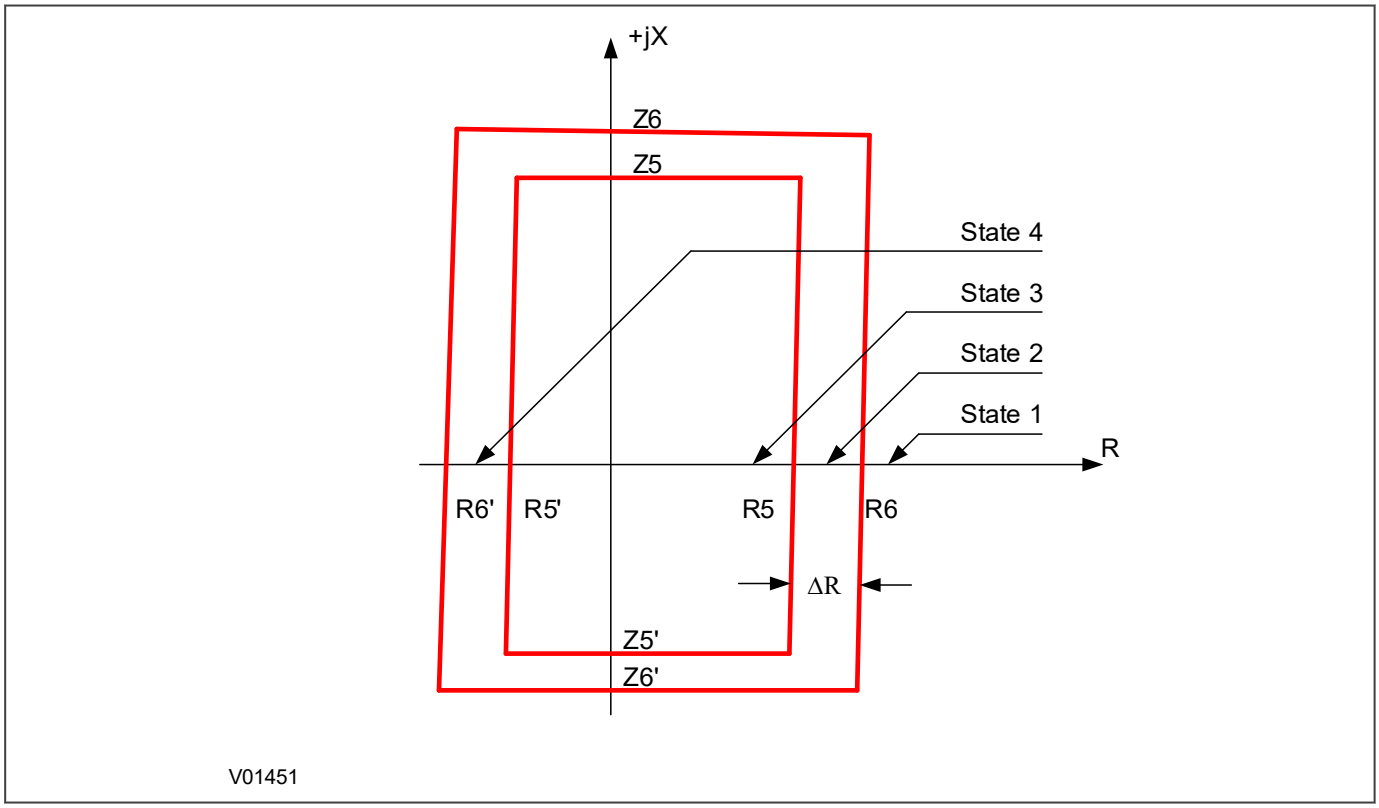


Figure 440: State impedances

Depending on the Out of Step (OST) settings, use one of the following setting options.

- OST setting
- Predictive OST setting
- Predictive and OST setting

27.15.1 OST SETTING

1. Clear all alarms.
2. Set the OST timer to zero.
3. To test OST, a 4-state test sequence is required. Based on healthy voltages (VA = VB = VC = 57.8 V) calculate the currents to generate the impedances as below.

	State 1	State 2	State 3	State 4
Applied current (all 3 phases)	57.8/(1.1R6)	57.8/(R5+0.5(R6-R5))	57.8/(0.95R5)	57.8/(1.1R5')
Angle	0°	0°	0°	180°
Duration	500 ms	Longer than 'Delta t' set time	100 ms	500 ms

Now apply the 4-state sequence, check that all 3-phases have tripped and that an OST alarm is displayed on the local LCD.

Note:
The angle in the table above is the angle between voltages and their respective currents. In state 4 the currents are displaced 180° from their respective voltages.

27.15.2 PREDICTIVE OST SETTING

1. Clear all alarms.
2. Set the OST timer to zero.
3. To test OST, a 3-state test sequence is required. Based on healthy voltages (VA = VB = VC = 57.8 V) calculate the currents to generate the impedances as below.

	State 1	State 2	State 3
Applied current (all 3 phases)	57.8/(1.1R6)	57.8/(R5+0.5(R6-R5))	57.8/(0.95R5)
Angle	0°	0°	0°
Duration	500 ms	Longer than 25 ms but shorter than 'Delta t' set time	500 ms

Now apply the 3-state sequence, check that all 3-phases have tripped and that an OST alarm is displayed on the local LCD.

27.15.3 PREDICTIVE AND OST SETTING

As per Predictive OST

27.15.4 OST TIMER TEST

1. Repeat the test as for 'predictive OST' and observe that the 3-phase tripping comes up after the 'Tost' set delay.
2. Record the operating time in the commissioning record sheet.

27.16 PROTECTION TIMING CHECKS

There is no need to check every protection function. Only one protection function needs to be checked as the purpose is to verify the timing on the processor is functioning correctly.

27.16.1 DEPENDENCY CONDITIONS

Some protection elements can be set to have dependencies on the availability of the protection communication channel(s) and on the status of the voltage transformer supervision function (VTS).

If you are testing a distance model, the distance protection can be permanently enabled, or it can be set so that it is only enabled in the event of a failure of the protection communications channel(s).

The overcurrent and earth faults elements can be permanently enabled, or can be set so that they are only enabled:

- in the event of a failure of the protection communications channel(s)
- in the event of a VTS alarm
- according to a logical combination of both conditions.

If these elements are enabled with a dependency upon the above conditions, it is necessary to simulate the condition to test the correct operation of the protection function.

A communications failure can be simulated by setting the Test Loopback cell to Disabled and checking that the IED raises a Comms Fail alarm.

At the end of the test, clear the communications alarms and reset the statistics.

A VTS alarm can be raised by applying a 3-phase voltage to the VT inputs and then removing one phase voltage for a duration exceeding the VTS Time Delay setting.

At the end of the tests, clear the VTS alarm.

27.16.2 OVERCURRENT CHECK

If the overcurrent protection function is being used, test the overcurrent protection for stage 1.

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Make a note of which elements need to be re-enabled after testing.
4. Connect the test circuit.
5. Perform the test.
6. Check the operating time.

27.16.3 CONNECTING THE TEST CIRCUIT

1. Use the PSL to determine which output relay will operate when an overcurrent trip occurs.
2. Use the output relay assigned to ***Trip Output A***.
3. Use the PSL to map the protection stage under test directly to an output relay.

> *Note:*
> *If using the default PSL, use output relay 3 as this is already mapped to the DDB signal* ***Trip Command Out****.*

4. Connect the output relay so that its operation will trip the test set and stop the timer.
5. Connect the current output of the test set to the A-phase current transformer input.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column is set to `Directional Fwd`, the current should flow out of terminal 2. If set to `Directional Rev`, it should flow into terminal 2.

If the ***I>1 Directional*** cell in the *OVERCURRENT* column has been set to `Directional Fwd` or `Directional Rev`, the rated voltage should be applied to terminals 20 and 21.

6. Ensure that the timer starts when the current is applied.

Note:
If the timer does not stop when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the direction of operation set. Try again with the current connections reversed.

27.16.4 PERFORMING THE TEST

1. Ensure that the timer is reset.
2. Apply a current of twice the setting shown in the ***I>1 Current Set*** cell in the *OVERCURRENT* column.
3. Note the time displayed when the timer stops.
4. Check that the red trip LED has illuminated.

27.16.5 CHECK THE OPERATING TIME

Check that the operating time recorded by the timer is within the range shown below.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating Time at Twice Current Setting and Time Multiplier/Time Dial Setting of 1.0	
	Nominal (Seconds)	Range (Seconds)
DT	I>1 Time Delay setting	Setting ±2%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	24.67 - 28.67
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 4.0
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.50	9.02 - 9.97
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Note:
With the exception of the definite time characteristic, the operating times given are for a Time Multiplier Setting (TMS) or Time Dial Setting (TDS) of 1. For other values of TMS or TDS, the values need to be modified accordingly.
For definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively. You may need to add this the IED's acceptable range of operating times.



Caution:
On completion of the tests, you must restore all settings to customer specifications.

27.17 SYSTEM CHECK AND CHECK SYNCHRONISM

This function performs a comparison between the line voltage and the bus voltage.

There are two voltage inputs to compare:

- one from the voltage transformer input from the line side of the circuit breaker (Main VT)
- one from the VT on the bus side of the circuit breaker (CS VT).

In most cases the line VT input is three phase, whereas the bus VTs are single phase.

The bus VT inputs are normally single phase so the system voltage checks are made on single phases and the VT may be connected to either a phase-to-phase or phase to neutral voltage.

For these reasons, the IED has to be programmed with the appropriate connection. The ***CS Input*** setting in the *CT AND VT RATIOS* column can be set to A-N, B-N, C-N, A-B, B-C or C-A according to the application.

The single-phase bus VT inputs each have associated phase shift and voltage magnitude compensation settings to compensate for healthy voltage angle and magnitude differences between the check sync VT input and the selected main VT reference phase. These are:

- ***CS VT Ph Shift*** and ***CS VT Mag***

Any voltage measurements or comparisons using bus VT inputs are made using the compensated values.

Each circuit breaker controlled can have two stages of check synchronism enabled according to the settings:

- ***System Checks***, ***CS1 Status*** and ***CS2 Status***

When the system voltage check conditions are satisfied, the relevant DDB signals are asserted high as follows:

- DDB (883): Check Sync 1 OK
- DDB (884): Check Sync 2 OK

These DDB signals should be mapped to the monitor/download port and used to indicate that the system check synchronism condition has been satisfied.

27.17.1 CHECK SYNCHRONISM PASS

1. Taking note of the check synchronism settings, identify the appropriate VT input terminals and inject voltage signals that should satisfy the system voltage check synchronism criteria.
2. Check that the DDB signals are asserted high.

27.17.2 CHECK SYNCHRONISM FAIL

1. Change the voltage signals so that the criteria are not satisfied
2. Check that the appropriate DDB signals are driven low

27.18 CHECK TRIP AND AUTORECLOSE CYCLE

If the auto-reclose function is being used, the circuit breaker trip and auto reclose cycle can be tested automatically by using the application-specific settings.

To test the trip and close operation without operating the breaker, the following conditions must be satisfied:

- The ***CB Healthy*** DDB signal should either not be mapped, or if it is mapped it must be asserted high.
- The CB status inputs (52A, etc.) should either not be mapped, or if they are mapped they should be activated to mimic the circuit breaker operation.
- Some models can be configured for single-pole tripping. If configured for single pole tripping, either set *CT/VT RATIO* > ***VT Connected*** to `No`, or apply appropriate voltage signals to prevent the pole dead logic from converting to 3-pole tripping.

1. To test the first three-phase auto-reclose cycle, set *COMMISSION TESTS* > ***Test Autoreclose*** to `Trip 3 Pole`. The IED performs a trip/reclose cycle.
2. Repeat this operation to test the subsequent three-phase auto-reclose cycles.
3. Check all output relays (used for such as circuit breaker tripping and closing, or blocking other devices) operate at the correct times during the trip/close cycle.

Check the auto-reclose cycles for single phase trip conditions one at a time by sequentially setting *COMMISSION TESTS* > ***Test Autoreclose*** to `Trip Pole A`, `Trip Pole B` and `Trip Pole C`.

27.19 END-TO-END COMMUNICATION TESTS

If the IED is being used in a scheme with InterMiCOM^{64} communications you must perform end-to-end testing of the protection communications channels.

In this section all loopbacks are removed and satisfactory communications between line ends of the IEDs in the scheme are confirmed.

Note:
End-to-end communication requires a working telecommunication channel between line ends (which may be a multiplexed link or may be a direct connection). If the telecommunication channel is not available, it is not possible to establish end-to end communication. Unless otherwise directed by local operational practise, follow the instructions in this section so the scheme is ready for full operation when the telecommunications channels become available.

Note:
The trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.

27.19.1 REMOVE LOCAL LOOPBACKS

As well as removing the loopback, this section checks that all wiring and optical fibre are reconnected. If P591, P592 or P593 interface units are installed the application-specific settings are also applied.

1. Check the alarm records to ensure that no communications failure alarms have occurred while the loopback test was in progress. If it was necessary to 'fail' the communications while testing the non-current differential elements, observe the communications behaviour for a few minutes before removing the loopbacks.
2. After you are satisfied with the communications behaviour in loopback, set *COMMISSION TESTS* > ***Test Mode*** and ***Test Loopback*** to `Disabled`.

Note:
Most of the required optical signal power levels have already been measured and recorded. If all signalling uses P59x interface units, no further measurements are required. If, however, 56/64 kb/s or C37.94 direct fibre communications are used, further measurements are needed.

27.19.1.1 RESTORING DIRECT FIBRE CONNECTIONS

When restoring direct fibre connections, check the optical power level received from the remote IED(s).

1. Remove the loopback test fibres and at both ends of each channel used, reconnect the fibre optic cables for communications between IEDs.
2. For each channel fitted, remove the fibre connecting to the optical receiver (RX).
3. Using an optical power meter measure the strength of the signal received from the remote IED. The measurements should be within -25.4 dBm and -16.8 dBm for 850 nm fibre connections and between -37 dBm and -7 dBm for 1300 nm fibre connections
4. Record the received power level(s).
5. Reconnect the fibre(s) to the IED receiver(s).



Warning:
NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.

27.19.1.2 RESTORING C37.94 FIBRE CONNECTIONS

When restoring C37.94 fibre connections, check the optical power level received from both the IED and the C37.94 multiplexer.

1. Remove the loopback test fibres and at both ends of each channel used.
2. Reconnect the fibre optic cables for communications between IEDs and the C37.94 compatible multiplexer.
3. Check that the value received from the IED at the C37.94 multiplexer, as well as that received by the IED from the C37.94 multiplexer are between -25.4 dBm (min) and -16.8 dBm (max).
4. Record the received power level(s).
5. Reconnect the fibre(s) to the IED receiver(s).



Warning:
NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.

27.19.1.3 COMMUNICATIONS USING P59X INTERFACE UNITS

If external wiring has been removed to facilitate testing, ensure that it is replaced in accordance with the relevant connection diagram or scheme diagram.

For the P591:

1. Check that all the cabling is correct.
2. Verify that the Healthy LED is on.
3. If you are using the C37.94 protocol, please confirm one P591 is set to Master and the other P591 is set to Slave.

For the P592:

1. Set the V.35 LOOPBACK switch to the 0 position.
2. Set the CLOCK SWITCH, DSR, CTS and DATA RATE switches on each unit to the positions required for the specific application.
3. Ensure the OPTO LOOPBACK switch is in the 0 position.
4. If applicable, replace the secondary front cover.

For the P593:

1. Set the X.21 LOOPBACK switch to the OFF position.
2. Ensure the OPTO LOOPBACK switch is also in the OFF position.
3. If applicable, replace the secondary front cover.

27.19.2 REMOVE REMOTE LOOPBACKS

Remove loopbacks at remote terminal connected to channel 1 and channel 2 by repeating the instructions for local loopback removal.

27.19.3 VERIFY COMMUNICATION BETWEEN IEDS

Communications statistics and status - non GPS synchronised.

1. Reset any alarm indications and check that no further communications failure alarms are raised.
2. Check channel status and propagation delays in *MEASUREMENTS 4* column for channel 1 (and channel 2 where fitted).

3. Check that the first two bits in ‘Channel Status’ (Rx and Tx) are displaying ‘1’ (11********** where * indicates a ‘don’t care’ state).
4. Clear the statistics and record the number of valid messages and the number of errored messages after a minimum period of 1 hour.
5. Check that the ratio of errored/good messages is better than 10-4.
6. Record the measured message propagation delays for channel 1, and channel 2 (if fitted).

Communications statistics and status - GPS synchronised with RT430

1. Reset any alarm indications and check that no further communications failure alarms are raised.
2. Check channel status and propagation delays in the *MEASUREMENTS 4* column for channel 1 (and channel 2 where fitted).
3. Check that the first four bits in ‘Channel Status’ (Rx, Tx, Local GPS, and remote GPS) are displaying ‘1’ (1111********** where * indicates a ‘don’t care’ state).
4. Clear the statistics and record the number of valid messages and the number of errored messages after a minimum period of 1 hour.
5. Check that the ratio of errored/good messages is better than 10-4. Record the measured message propagation delays for channel 1, and channel 2 (if fitted).

27.20 END-TO-END SCHEME TESTS

This section aims to check that the signalling channel is able to transmit the ON/OFF signals used in aided schemes between the remote line ends.

Before testing, check that the channel is healthy. For example, if a power line carrier link is being used, it may not be possible to perform the tests until the protected circuit is in service.

27.20.1 AIDED SCHEME 1

Aided Scheme 1 can be tested by operating output contacts to mimic the transmission of an aided channel signal.

For these tests, an engineer needs to be present at both ends of the line - at the local end to send aided signals, and at the remote end to observe that the signals are received. A telephone link between the two commissioning engineers is also necessary, to allow conversation.

1. Put the IED in test mode by setting *COMMISSION TESTS* > ***Test Mode*** to `Blocked`.
2. Record which contact is assigned as the ***Signal Send 1*** output
3. Select this output contact as the one to test and advise the engineer at the remote end that the contact is about to be tested.

27.20.1.1 PREPARATION AT REMOTE END

At the remote end, the engineer must confirm the assignment of the ***Monitor Bits*** in the *COMMISSION TESTS* column in the menu, to be able to see the aided channel on arrival.

Scroll down and ensure that the ***Monitor Bit 1*** cell is set to `DDB493` and that the ***Monitor Bit 5*** cell is set to `DDB507`. The Test Port Status cell appropriately sets or resets the bits that now represent Aided 1 Scheme Receive (DDB493), and Aided 2 Scheme Receive (DDB507), with the rightmost bit representing Aided Channel 1. From now on the engineer at the remote end should monitor the indication of the ***Test Port Status*** cell.

27.20.1.2 PERFORMING THE TEST

1. At the local end, set the *COMMISSION TESTS* > ***Contact Test*** to `Apply Test`.
2. Reset the output relay by setting *COMMISSION TESTS* > ***Contact Test*** to `Remove Test`.
3. Check with the engineer at the remote end that the Aided Channel 1 signal did change state as expected. The ***Test Port Status*** cell should have responded as in the table below.

DDB No.				507				493
Monitor Bit	8	7	6	5	4	3	2	1
Contact Test OFF	X	X	X	X	X	X	X	0
Contact Test Applied (ON)	X	X	X	X	X	X	X	1
Test OFF	X	X	X	X	X	X	X	0

X = Don't Care

Now return the IED to service by setting *COMMISSION TESTS* > ***Test Mode*** to `Disabled`.

27.20.1.3 CHANNEL CHECK IN THE OPPOSITE DIRECTION

Repeat the aided scheme 1 test procedure, but this time to check that the channel responds correctly when keyed from the remote end. The remote end commissioning engineer should perform the contact test, with the Monitor Option observed at the local end.

27.20.2 AIDED SCHEME 2

1. If applicable, repeat the test for Aided Channel 2.
2. Return the device to service by setting *COMMISSION TESTS* > ***Test Mode*** to `Disabled`.

27.21 ONLOAD CHECKS



Warning:
Onload checks are potentially very dangerous and may only be carried out by qualified and authorised personnel.

Onload checks can only be carried out if there are no restrictions preventing the energisation of the plant, and the other devices in the group have already been commissioned.

Remove all test leads and temporary shorting links, then replace any external wiring that has been removed to allow testing.



Warning:
If any external wiring has been disconnected for the commissioning process, replace it in accordance with the relevant external connection or scheme diagram.

27.21.1 CONFIRM VOLTAGE CONNECTIONS

1. Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated.
2. Check that the system phase rotation is correct using a phase rotation meter.
3. Compare the values of the secondary phase voltages with the measured voltage magnitude values, which can be found in the *MEASUREMENTS 1* menu column.

Cell in MEASUREMENTS 1 Column	Corresponding VT Ratio in CT/VT RATIOS Column
VAB MAGNITUDE *VBC MAGNITUDE* *VCA MAGNITUDE* *VAN MAGNITUDE* *VBN MAGNITUDE* *VCN MAGNITUDE*	Main VT Primary/Main VT Sec'y
C/S Voltage Mag	CS VT Primary/CS VT Secondary

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

27.21.2 CONFIRM CURRENT CONNECTIONS

1. Measure the current transformer secondary values for each input either by:
   a. reading from the device's HMI panel (providing it has first been verified by a secondary injection test)
   b. using a current clamp meter
2. Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control centre.
3. Ensure the current flowing in the neutral circuit of the current transformers is negligible.

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

27.21.3 MEASURE CAPACITIVE CHARGING CURRENT

1. With the feeder energised from one end only, compare the local and remote measured currents in the *MEASUREMENTS 3* column to confirm that the feeder capacitive charging current is similar to that expected on all three phases.
2. Check that GROUP 1 *CURRENT DIFF* > ***Phase Is1*** is set higher than 2.5 times the capacitive charging current. If this is not the case, notify those concerned of the setting required to ensure stability under normal operating conditions.

27.21.4 CHECK DIFFERENTIAL CURRENT

With the feeder supplying load current, check that the measurements in the *MEASUREMENTS 3* column are as expected and that the differential current is similar to the value of capacitive charging current previously measured for all.

27.21.5 CHECK CURRENT TRANSFORMER POLARITY

The load current should be high enough to be certain that the main current transformers are connected with the same polarity to each device in the group. On cable circuits with high line capacitance, it is possible that the load current could be masked by the capacitive charging current.

1. If necessary reverse the connections to the main current transformers and check that the 'A' current differential in *MEASUREMENTS 3* > ***IA Differential*** cell is significantly higher than for the normal connection. If the differential current falls with the connection reversed, the main current transformers may not be correct and should be thoroughly checked.
2. Repeat the test for phases B and C using the IB Differential and IC Differential cells respectively.

27.21.6 ON-LOAD DIRECTIONAL TEST

This test ensures that directional overcurrent and fault locator functions have the correct forward/reverse response to fault and load conditions. For this test you must first know the actual direction of power flow on the system. If you do not already know this you must determine it using adjacent instrumentation or protection already in-service.

- For load current flowing in the Forward direction (power export to the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show positive power signing.
- For load current flowing in the Reverse direction (power import from the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show negative power signing.

> *Note:*
> *This check applies only for Measurement Modes 0 (default), and 2. This should be checked in the MEASURE'T SETUP column (**Measurement Mode** = 0 or 2). If measurement modes 1 or 3 are used, the expected power flow signing would be opposite to that shown above.*

In the event of any uncertainty, check the phase angle of the phase currents with respect to their phase voltage.

27.22 FINAL CHECKS

1. Remove all test leads and temporary shorting leads.
2. If you have had to disconnect any of the external wiring in order to perform the wiring verification tests, replace all wiring, fuses and links in accordance with the relevant external connection or scheme diagram.
3. The settings applied should be carefully checked against the required application-specific settings to ensure that they are correct, and have not been mistakenly altered during testing.
4. Ensure that all protection elements required have been set to `Enabled` in the *CONFIGURATION* column.
5. Ensure that the IED has been restored to service by checking that the ***Test Mode*** cell in the *COMMISSION TESTS* column is set to `Disabled`.
6. If the IED is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using the ***Reset All Values*** cell. If the required access level is not active, the device will prompt for a password to be entered so that the setting change can be made.
7. If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.
8. If a P991/MMLG test block is installed, remove the P992/MMLB test plug and replace the cover so that the protection is put into service.
9. Ensure that all event records, fault records, disturbance records, alarms and LEDs and communications statistics have been reset.

Note:
Remember to restore the language setting to the customer's preferred language on completion.

27.23 COMMMISSIONING THE P59X

If you are setting up a scheme, which involves a P59x device, you will need to commission the P59x too. The following instructions describe the commissioning procedure for a P59x.

27.23.1 VISUAL INSPECTION



Warning:
Check the rating information under the top access cover on the front of the IED.



Warning:
Check that the IED being tested is correct for the line or circuit.



Warning:
Record the circuit reference and system details.



Warning:
Check the CT secondary current rating and record the CT tap which is in use.

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

27.23.2 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

Note:
The V.35 circuits and the X.21 circuits of the P592 and P593 respectively are isolated from all other circuits but are electrically connected to the outer case. The circuits must therefore not be insulation or impulse tested to the case.

27.23.3 EXTERNAL WIRING



Caution:
Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.

27.23.4 P59X AUXILIARY SUPPLY

P591 devices operate from a DC auxiliary supply within the range of 19 V to 65 V for a 24 - 48 V version and 87.5 V to 300 V for a 110 - 250 V version.

P592 and P593 units operate from a DC auxiliary supply within the range of 19 V to 300 V.

Without energising the device, measure the auxiliary supply to ensure it is within the operating range.

The devices are designed to withstand an AC ripple component of up to 15% of the normal DC auxiliary supply. However, in all cases the peak value of the DC supply must not exceed the maximum specified operating limit.



Warning:
Do not energise the device or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.

27.23.5 P59X LEDS

On power up the green ‘SUPPLY HEALTHY’ LED should be permanently illuminated, indicating that the device is healthy.

P592 only

The four red LEDs can be tested by appropriate setting of the DIL switches on the front plate. Set the data rate switch according to the communication channel bandwidth available. Set all other switches to 0. To illuminate the ‘DSR OFF’ and ‘CTS OFF’ LED’s, disconnect the V.35 connector from the rear of the P592 and set the ‘DSR’ and ‘CTS’ switches to ‘0’. The ‘OPTO LOOPBACK’ and ‘V.35 LOOPBACK’ LEDs can be illuminated by setting their corresponding switches to ‘1’.

Once operation of the LEDs has been established set all DIL switches, except for the ‘OPTO LOOPBACK’ switch, to ‘0’ and reconnect the V.35 connector.

P593 only

Set the ‘X.21 LOOPBACK’ switch to ‘ON’. The green ‘CLOCK’ and red ‘X.21 LOOPBACK’ LED’s should illuminate. Reset the ‘X.21 LOOPBACK’ switch to the ‘OFF’ position.

Set the ‘OPTO LOOPBACK’ switch to ‘ON’. The red ‘OPTO LOOPBACK’ LED should illuminate. Do not reset the “OPTO LOOPBACK’ switch as it is required in this position for the next test.

27.23.6 RECEIVED OPTICAL SIGNAL LEVEL

1. With an optical cable connected to the P54x optical transmitter, disconnect the other end of the cable from the P59x receiver (Rx) and use an optical power meter to measure the received signal strength. The value should be in the range -16.8 dBm to -25.4 dBm.
2. Record the measured value and replace the connector to the P59x receiver.



Warning:
NEVER look directly into the transmit port or the end of an optical fibre, as this could severely damage your eyes.

27.23.7 OPTICAL TRANSMITTER LEVEL

1. Using an appropriate fibre-optic cable, connect the optical transmitter (Tx) to an optical power meter.
2. Check that the average power transmitted is within the range -16.8 dBm to -22.8 dBm.
3. Record the transmit power level.
4. Connect the appropriate optical fibre to connect the P591 transmitter to the IED's optical receiver
5. Return to the IED

27.23.8 LOOPBACK TEST

P591

It is necessary to loop the transmitted electrical G.703 signal presented on terminals 3 and 4 of the P591 to the received signal presented on terminals 7 and 8.

If test links have been designed into the scheme to facilitate this they should be used. Alternatively, remove any external wiring from terminals 3, 4, 7 and 8 at the rear of each P591 unit. Loopback the G.703 signals on each device by connecting a wire link between terminals 3 and 7, and a second wire between terminals 4 and 8.

P592

With the ‘OPTO LOOPBACK’ switch in the ‘1’ position, the receive and transmit optical ports are connected together. This allows the optical fibre communications between the IED and the P592 to be tested, but not the internal circuitry of the P592 itself.

P593

Set the ‘OPTO LOOPBACK’ switch to ‘OFF’ and ‘X.21 LOOPBACK’ switch to ‘ON’ respectively. With the ‘X.21 LOOPBACK’ switch in this position the ‘Receive Data’ and ‘Transmit Data’ lines of the X.21 communication interface are connected together. This allows the optical fibre communications between the IED and the P593, and the internal circuitry of the P593 itself to be tested.

CHAPTER 28

MAINTENANCE AND TROUBLESHOOTING

28.1 CHAPTER OVERVIEW

The Maintenance and Troubleshooting chapter provides details of how to maintain and troubleshoot products based on the Px4x and P40Agile platforms. Always follow the warning signs in this chapter. Failure to do so may result injury or defective equipment.



Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

The troubleshooting part of the chapter allows an error condition on the IED to be identified so that appropriate corrective action can be taken.

If the device develops a fault, it is usually possible to identify which module needs replacing. It is not possible to perform an on-site repair to a faulty module.

If you return a faulty unit or module to the manufacturer or one of their approved service centres, you should include a completed copy of the Repair or Modification Return Authorisation (RMA) form.

This chapter contains the following sections:

Chapter Overview 838

Maintenance 839

Troubleshooting 847

28.2 MAINTENANCE

28.2.1 MAINTENANCE CHECKS

In view of the critical nature of the application, GE Vernova products should be checked at regular intervals to confirm they are operating correctly. GE Vernova products are designed for a life in excess of 20 years.

The devices are self-supervising and so require less maintenance than earlier designs of protection devices. Most problems will result in an alarm, indicating that remedial action should be taken. However, some periodic tests should be carried out to ensure that they are functioning correctly and that the external wiring is intact. It is the responsibility of the customer to define the interval between maintenance periods. If your organisation has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

Although some functionality checks can be performed from a remote location, these are predominantly restricted to checking that the unit is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. For this reason, maintenance checks should also be performed locally at the substation.



Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

28.2.1.1 ALARMS

First check the alarm status LED to see if any alarm conditions exist. If so, press the Read key repeatedly to step through the alarms.

After dealing with any problems, clear the alarms. This will clear the relevant LEDs.

28.2.1.2 OPTO-ISOLATORS

Check the opto-inputs by repeating the commissioning test detailed in the Commissioning chapter.

28.2.1.3 OUTPUT RELAYS

Check the output relays by repeating the commissioning test detailed in the Commissioning chapter.

28.2.1.4 MEASUREMENT ACCURACY

If the power system is energised, the measured values can be compared with known system values to check that they are in the expected range. If they are within a set range, this indicates that the A/D conversion and the calculations are being performed correctly. Suitable test methods can be found in Commissioning chapter.

Alternatively, the measured values can be checked against known values injected into the device using the test block, (if fitted) or injected directly into the device's terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

28.2.2 REPLACING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, you can replace either the complete device or just the faulty PCB, identified by the in-built diagnostic software.

If possible you should replace the complete device, as this reduces the chance of damage due to electrostatic discharge and also eliminates the risk of fitting an incompatible replacement PCB. However, we understand it may be difficult to remove an installed product and you may be forced to replace the faulty PCB on-site. The case and rear terminal blocks are designed to allow removal of the complete device, without disconnecting the scheme wiring.



Caution:
Replacing PCBs requires the correct on-site environment (clean and dry) as well as suitably trained personnel.



Caution:
If the repair is not performed by an approved service centre, the warranty will be invalidated.



Caution:
Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.



Warning:
Before working at the rear of the device, isolate all voltage and current supplying it.

Note:
The current transformer inputs are equipped with integral shorting switches which will close for safety reasons, when the terminal block is removed.

To replace the complete device:

1. Carefully disconnect the cables not connected to the terminal blocks (e.g. IRIG-B, fibre optic cables, earth), as appropriate, from the rear of the device.
2. Remove the terminal block screws using a magnetic screwdriver to minimise the risk of losing the screws or leaving them in the terminal block.
3. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
4. Remove the terminal block screws that fasten the device to the panel and rack. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.
5. Withdraw the device from the panel and rack. Take care, as the device will be heavy due to the internal transformers.
6. To reinstall the device, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the chassis ground, IRIG-B and fibre optic connections are replaced. The terminal blocks are labelled alphabetically with 'A' on the left hand side when viewed from the rear.

Once the device has been reinstalled, it should be re-commissioned as set out in the Commissioning chapter.

Caution:
If the top and bottom access covers have been removed, some more screws with smaller diameter heads are made accessible. Do NOT remove these screws, as they secure the front panel to the device.

Note:
There are four possible types of terminal block: RTD/CLIO input, heavy duty, medium duty, and MiDOS. The terminal blocks are fastened to the rear panel with slotted or cross-head screws depending on the type of terminal block. Not all terminal block types are present on all products.

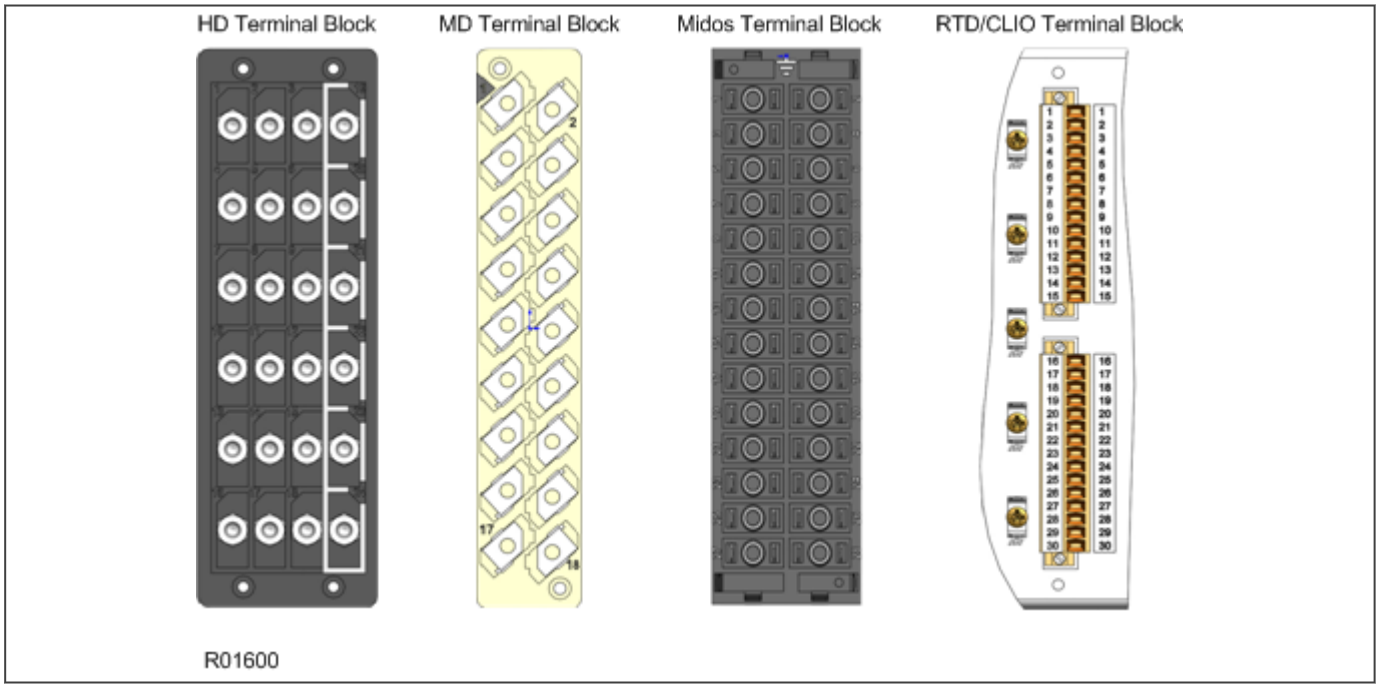


Figure 441: Possible terminal block types

28.2.3 REPAIRING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, either the complete unit or just the faulty PCB, identified by the in-built diagnostic software, should be replaced.

Replacement of printed circuit boards and other internal components must be undertaken by approved Service Centres. Failure to obtain the authorisation of after-sales engineers prior to commencing work may invalidate the product warranty.

We recommend that you entrust any repairs to Automation Support teams, which are available world-wide.

28.2.4 REMOVING THE FRONT PANEL

Warning:
Before removing the front panel to replace a PCB, you must first remove the auxiliary power supply and wait 5 seconds for the internal capacitors to discharge. You should also isolate voltage and current transformer connections and trip circuit.



Caution:
Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

To remove the front panel:

1. Open the top and bottom access covers. You must open the hinged access covers by more than 90° before they can be removed.
2. If fitted, remove the transparent secondary front cover.
3. Apply outward pressure to the middle of the access covers to bow them and disengage the hinge lug, so the access cover can be removed. The screws that fasten the front panel to the case are now accessible.
4. Undo and remove the screws. The 40TE case has four cross-head screws fastening the front panel to the case, one in each corner, in recessed holes. The 60TE/80TE cases have an additional two screws, one midway along each of the top and bottom edges of the front plate.
5. When the screws have been removed, pull the complete front panel forward to separate it from the metal case. The front panel is connected to the rest of the circuitry by a 64-way ribbon cable.
6. The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable and a plug with locking latches on the front panel. Gently push the two locking latches outwards which eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.



Caution:
Do not remove the screws with the larger diameter heads which are accessible when the access covers are fitted and open. These screws hold the device in its mounting (panel or cubicle).



Caution:
The internal circuitry is now exposed and is not protected against electrostatic discharge and dust ingress. Therefore ESD precautions and clean working conditions must be maintained at all times.

28.2.5 REPLACING PCBS

1. To replace any of the PCBs, first remove the front panel.
2. Once the front panel has been removed, the PCBs are accessible. The numbers above the case outline identify the guide slot reference for each printed circuit board. Each printed circuit board has a label stating the corresponding guide slot number to ensure correct relocation after removal. To serve as a reminder of the slot numbering there is a label on the rear of the front panel metallic screen.
3. Remove the 64-way ribbon cable from the PCB that needs replacing
4. Remove the PCB in accordance with the board-specific instructions detailed later in this section.

Note:
To ensure compatibility, always replace a faulty PCB with one of an identical part number.

28.2.5.1 REPLACING THE MAIN PROCESSOR BOARD

The main processor board is situated in the front panel. This board contains application-specific settings in its non-volatile memory. You may wish to take a backup copy of these settings. This could save time in the re-commissioning process.

To replace the main processor board:

1. Remove front panel.
2. Place the front panel with the user interface face down and remove the six screws from the metallic screen, as shown in the figure below. Remove the metal plate.
3. Remove the screws that hold the main processor board in position.
4. Carefully disconnect the ribbon cable. Take care as this could easily be damaged by excessive twisting.
5. Replace the main processor board
6. Reassemble the front panel using the reverse procedure. Make sure the ribbon cable is reconnected to the main processor board and that all eight screws are refitted.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, carry out the standard commissioning procedure as defined in the Commissioning chapter.

Note:
After replacing the main processor board, all the settings required for the application need to be re-entered. This may be done either manually or by downloading a settings file.

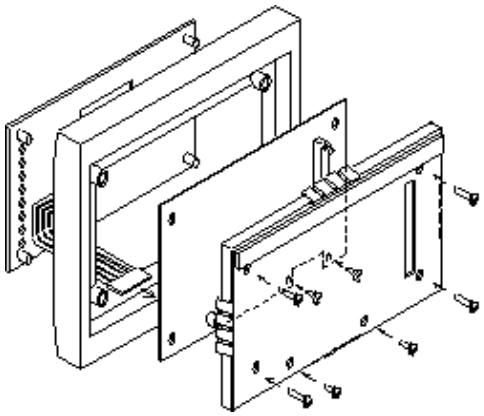


Figure 442: Front panel assembly

28.2.5.2 REPLACEMENT OF COMMUNICATIONS BOARDS

Most products will have at least one communications board of some sort fitted. There are several different boards available offering various functionality, depending on the application. Some products may even be fitted with two boards of different types.

To replace a faulty communications board:

1. Remove front panel.
2. Disconnect all connections at the rear.
3. The board is secured in the device case by two screws, one at the top and another at the bottom. Remove these screws carefully as they are not captive in the rear panel.
4. Gently pull the communications board forward and out of the case.

5. Before fitting the replacement PCB check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
6. Fit the replacement PCB carefully into the correct slot. Make sure it is pushed fully back and that the securing screws are refitted.
7. Reconnect all connections at the rear.
8. Refit the front panel.
9. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
10. Once the unit has been reassembled, commission it according to the Commissioning chapter.

28.2.5.3 REPLACEMENT OF THE INPUT MODULE

Depending on the product, the input module consists of two or three boards fastened together and is contained within a metal housing. One board contains the transformers and one contains the analogue to digital conversion and processing electronics. Some devices have an additional auxiliary transformer contained on a third board.

To replace an input module:

1. Remove front panel.
2. The module is secured in the case by two screws on its right-hand side, accessible from the front, as shown below. Move these screws carefully as they are not captive in the front plate of the module.
3. On the right-hand side of the module there is a small metal tab which brings out a handle (on some modules there is also a tab on the left). Grasp the handle(s) and pull the module firmly forward, away from the rear terminal blocks. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
4. Remove the module from the case. The module may be heavy, because it contains the input voltage and current transformers.
5. Slot in the replacement module and push it fully back onto the rear terminal blocks. To check that the module is fully inserted, make sure the v-shaped cut-out in the bottom plate of the case is fully visible.
6. Refit the securing screws.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.



Caution:
With non-mounted IEDs, the case needs to be held firmly while the module is withdrawn. Withdraw the input module with care as it suddenly comes loose once the friction of the terminal blocks is overcome.

Note:
If individual boards within the input module are replaced, recalibration will be necessary. We therefore recommend replacement of the complete module to avoid on-site recalibration.

28.2.5.4 REPLACEMENT OF THE POWER SUPPLY BOARD



Caution:
Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

The power supply board is fastened to an output relay board with push fit nylon pillars. This doubled-up board is secured on the extreme left hand side, looking from the front of the unit.

1. Remove front panel.
2. Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
3. Separate the boards by pulling them apart carefully. The power supply board is the one with two large electrolytic capacitors.
4. Before reassembling the module, check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label
5. Reassemble the module with a replacement PCB. Push the inter-board connectors firmly together. Fit the four push fit nylon pillars securely in their respective holes in each PCB.
6. Slot the power supply module back into the housing. Push it fully back onto the rear terminal blocks.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

28.2.5.5 REPLACEMENT OF THE I/O BOARDS

There are several different types of I/O boards, which can be used, depending on the product and application. Some boards have opto-inputs, some have relay outputs and others have a mixture of both.

1. Remove front panel.
2. Gently pull the board forward and out of the case
3. If replacing the I/O board, make sure the setting of the link above IDC connector on the replacement board is the same as the one being replaced.
4. Before fitting the replacement board check the number on the round label next to the front edge of the board matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
5. Carefully slide the replacement board into the appropriate slot, ensuring that it is pushed fully back onto the rear terminal blocks.
6. Refit the front panel.
7. Refit and close the access covers then press at the hinge assistance T-pieces so they click back into the front panel moulding.
8. Once the unit has been reassembled, commission it according to the Commissioning chapter.

28.2.6 RECALIBRATION

Recalibration is not needed when a PCB is replaced, unless it is one of the boards in the input module. If any of the boards in the input module is replaced, the unit must be recalibrated.

Although recalibration is needed when a board inside the input module is replaced, it is not needed if the input module is replaced in its entirety.

Although it is possible to carry out recalibration on site, this requires special test equipment and software. We therefore recommend that the work be carried out by the manufacturer, or entrusted to an approved service centre.

28.2.7 SUPERCAPACITOR DISCHARGED

The supercapacitor maintains charge for two weeks with the IED de-energised. When first energising the IED after this time there may be a ***SuperCap Alarm*** due to the supercapacitor voltage dropping below a pre-defined

threshold. The ***SuperCap Alarm*** will clear after approximately 30 minutes of IED being energised, and once cleared there will be enough charge in the supercapacitor to maintain the RTC.

Note:
The Real Time Clock will be reset if the supercapacitor is fully discharged.

28.2.8 CLEANING



Warning:
Before cleaning the device, ensure that all AC and DC supplies and transformer connections are isolated, to prevent any chance of an electric shock while cleaning.

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the product's surfaces and leave a conductive residue.

28.3 TROUBLESHOOTING

28.3.1 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

28.3.2 POWER-UP ERRORS

If the IED does not appear to power up, use the following to determine whether the fault is in the external wiring, auxiliary fuse, IED power supply module or IED front panel.

Test	Check	Action
1	Measure the auxiliary voltage on terminals 1 and 2. Verify the voltage level and polarity against the rating label on the front. Terminal 1 is –dc, 2 is +dc	If the auxiliary voltage is correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply.
2	Check the LEDs and LCD backlight switch on at power-up. Also check the N/O (normally open) watchdog contact for closing.	If the LEDs and LCD backlight switch on, or the contact closes and no error code is displayed, the error is probably on the main processor board in the front panel. If the LEDs and LCD backlight do not switch on and the contact does not close, go to test 3.
3	Check the output (nominally 48 V DC).	If there is no field voltage, the fault is probably in the IED power supply module.

28.3.3 ERROR MESSAGE OR CODE ON POWER-UP

The IED performs a self-test during power-up. If it detects an error, a message appears on the LCD and the power-up sequence stops. If the error occurs when the IED application software is running, a maintenance record is created and the device reboots.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If the IED locks up and displays an error code permanently, go to test 2. If the IED prompts for user input, go to test 4. If the IED reboots automatically, go to test 5.
2	Record displayed error, and then remove and re-apply IED auxiliary supply.	Record whether the same error code is displayed when the IED is rebooted. If no error code is displayed, contact the local service centre stating the error code and IED information. If the same code is displayed, go to test 3.

Test	Check	Action
3	Error Code Identification The following text messages (in English) are displayed if a fundamental problem is detected, preventing the system from booting: Bus Fail - address lines SRAM Fail - data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail The following hex error codes relate to errors detected in specific IED modules:	These messages indicate that a problem has been detected on the IED's main processor board in the front panel.
3.1	0c140005/0c0d0000	Input Module (including opto-isolated inputs)
3.2	0c140006/0c0e0000	Output IED boards
3.3	The last four digits provide details on the actual error.	Other error codes relate to hardware or software problems on the main processor board. Contact GE Vernova with details of the problem for a full analysis.
4	The IED displays a message for corrupt settings and prompts for the default values to be restored for the affected settings.	The power-up tests have detected corrupted IED settings. Restore the default settings to allow the power-up to complete, and then reapply the application-specific settings.
5	The IED resets when the power-up is complete. A record error code is displayed	Error 0x0E080000, programmable scheme logic error due to excessive execution time. If the IED powers up successfully, check the programmable logic for feedback paths. Other error codes relate to software errors on the main processor board.

28.3.4 OUT OF SERVICE LED ON AT POWER-UP

Test	Check	Action	
1	Using the IED menu, confirm the Commission Test or Test Mode setting is Enabled. If it is not Enabled, go to test 2.	If the setting is Enabled, disable the test mode and make sure the Out of Service LED is OFF.	
2	Select the *VIEW RECORDS* column then view the last maintenance record from the menu.	Check for the H/W Verify Fail maintenance record. This indicates a discrepancy between the IED model number and the hardware. Examine the ***Maint Data***; cell. This indicates the causes of the failure using bit fields: Bit Meaning	
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110 V VTs fitted)
		7	The VT type field in the model number is incorrect (440 V VTs fitted)
		8	The VT type field in the model number is incorrect (no VTs fitted)

28.3.5 ERROR CODE DURING OPERATION

The IED performs continuous self-checking. If the IED detects an error it displays an error message, logs a maintenance record and after a short delay resets itself. A permanent problem (for example due to a hardware fault) is usually detected in the power-up sequence. In this case the IED displays an error code and halts. If the problem was transient, the IED reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

28.3.6 MAL-OPERATION DURING TESTING

28.3.6.1 FAILURE OF OUTPUT CONTACTS

An apparent failure of the relay output contacts can be caused by the configuration. Perform the following tests to identify the real cause of the failure. The self-tests verify that the coils of the output relay contacts have been energised. An error is displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED ON?	If this LED is ON, the device may be in test mode or the protection has been disabled due to a hardware verify error.
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, go to test 4; if not, go to test 3.
3	Examine the fault record or use the test port to check the protection element is operating correctly.	If the protection element does not operate, check the test is correctly applied. If the protection element operates, check the programmable logic to make sure the protection element is correctly mapped to the contacts.
4	Using the Commissioning or Test mode function, apply a test pattern to the relevant relay output contacts. Consult the correct external connection diagram and use a continuity tester at the rear of the device to check the relay output contacts operate.	If the output relay operates, the problem must be in the external wiring to the device. If the output relay does not operate the output relay contacts may have failed (the self-tests verify that the relay coil is being energised). Ensure the closed resistance is not too high for the continuity tester to detect.

28.3.6.2 FAILURE OF OPTO-INPUTS

The opto-isolated inputs are mapped onto the IED's internal DDB signals using the programmable scheme logic. If an input is not recognised by the scheme logic, use the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column to check whether the problem is in the opto-input itself, or the mapping of its signal to the scheme logic functions.

If the device does not correctly read the opto-input state, test the applied signal. Verify the connections to the opto-input using the wiring diagram and the nominal voltage settings in the *OPTO CONFIG* column. To do this:

1. Select the nominal voltage for all opto-inputs by selecting one of the five standard ratings in the ***Global Nominal V*** cell.
2. Select `Custom` to set each opto-input individually to a nominal voltage.
3. Using a voltmeter, check that the voltage on its input terminals is greater than the minimum pick-up level (See the Technical Specifications chapter for opto pick-up levels).

If the signal is correctly applied, this indicates failure of an opto-input, which may be situated on standalone opto-input board, or on an opto-input board that is part of the input module. Separate opto-input boards can simply be replaced. If, however, the faulty opto-input board is part of the input module, the complete input module should be replaced. This is because the analogue input module cannot be individually replaced without dismantling the module and recalibration of the IED.

28.3.6.3 INCORRECT ANALOGUE SIGNALS

If the measured analogue quantities do not seem correct, use the measurement function to determine the type of problem. The measurements can be configured in primary or secondary terms.

1. Compare the displayed measured values with the actual magnitudes at the terminals.
2. Check the correct terminals are used.
3. Check the CT and VT ratios set are correct.
4. Check the phase displacement to confirm the inputs are correctly connected.

28.3.7 COPROCESSOR BOARD FAILURES

If a coprocessor board is used, this may cause the IED to report one or more of the following alarms:

- Signalling failure alarm (on its own)
- C diff failure (on its own)
- Signalling failure and C diff failure together
- Incompatible IED
- Comms changed
- IEEE C37.94 fail

28.3.7.1 SIGNALLING FAILURE ALARM (ON ITS OWN)

This indicates that there is a problem with one of the fibre-optic signalling channels. This alarm can occur in dual redundant or three terminal schemes. The fibre may have been disconnected, the device may have been incorrectly configured at one of the ends, or there is a problem with the communications equipment. Further information about the status of the signalling channels can be found in *MEASUREMENTS 4* column.

28.3.7.2 C DIFF FAILURE ALARM (ON ITS OWN)

This indicates there is a problem with the Coprocessor board. As a result the current differential/distance protection is not available and backup protection will operate, if configured to do so. Further information can be found in the maintenance records.

28.3.7.3 SIGNALLING FAILURE AND C DIFF FAILURE ALARMS TOGETHER

This indicates that there is a problem with one or both fibre-optic signalling channels. The fibre may have been disconnected, the device may have been incorrectly configured at one of the ends, or there is a problem with the communications equipment. As a result the current differential protection is not available and backup protection will operate, if configured to do so. Further information about the status of the signalling channels can be found in *MEASUREMENTS 4* column.

28.3.7.4 INCOMPATIBLE IED

This occurs if the IEDs trying to communicate with each other are of incompatible types.

28.3.7.5 COMMS CHANGED

This indicates that the ***Comms Mode*** setting has been changed without a subsequent power off and on.

28.3.7.6 IEEE C37.94 FAIL

This indicates a Signal Lost, a Path Yellow (indicating a fault on the communications channel) or a mismatch in the number of N*64 channels used on either channel 1 or channel 2. Further information can be found in the *MEASUREMENTS 4* column.

28.3.8 PSL EDITOR TROUBLESHOOTING

A failure to open a connection could be due to one or more of the following:

- The IED address is not valid (this address is always 1 for the front port)
- Password in not valid
- Communication set-up (COM port, Baud rate, or Framing) is not correct
- Transaction values are not suitable for the IED or the type of connection
- The connection cable is not wired correctly or broken
- The option switches on any protocol converter used may be incorrectly set

28.3.8.1 DIAGRAM RECONSTRUCTION

Although a scheme can be extracted from an IED, a facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals are drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B. Any annotation added to the original diagram such as titles and notes are lost.

Sometimes a gate type does not appear as expected. For example, a single-input AND gate in the original scheme appears as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 also appear as OR gates

28.3.8.2 PSL VERSION CHECK

The PSL is saved with a version reference, time stamp and CRC check (Cyclic Redundancy Check). This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

28.3.9 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Return Authorisation (RMA) form
   An electronic version of the RMA form is available from the following:
   GA.support@gevernova.com
2. Fill in the RMA form
   Fill in only the white part of the form.
   Please ensure that all fields marked **(M)** are completed such as:
   - Equipment model
   - Model No. and Serial No.
   - Description of failure or modification required (please be specific)
   - Value for customs (in case the product requires export)
   - Delivery and invoice addresses
   - Contact details
3. Send the RMA form to your local contact
   For a list of local service contacts worldwide, email us at:
   GA.support@gevernova.com
4. The local service contact provides the shipping information
   Your local service contact provides you with all the information needed to ship the product:
   - Pricing details
   - RMA number
   - Repair centre address

If required, an acceptance of the quote must be delivered before going to the next stage.

5. Send the product to the repair centre
    - Address the shipment to the repair centre specified by your local contact
    - Make sure all items are packaged in an anti-static bag and foam protection
    - Make sure a copy of the import invoice is attached with the returned unit
    - Make sure a copy of the RMA form is attached with the returned unit
    - E-mail or fax a copy of the import invoice and airway bill document to your local contact.

CHAPTER 29

TECHNICAL SPECIFICATIONS

29.1 CHAPTER OVERVIEW

This chapter describes the technical specifications of the product.

This chapter contains the following sections:

Chapter Overview 854
Interfaces 855
Protection Functions 860
Performance of Voltage Protection Functions 868
Performance of Frequency Protection Functions 871
Power Protection Functions 873
Monitoring, Control and Supervision 874
Measurements and Recording 876
Ratings 877
Input/Output Connections 880
Mechanical Specifications 882
Type Tests 883
Environmental Conditions 884
Electromagnetic Compatibility 885

29.2 INTERFACES

29.2.1 GRAPHICAL HMI

Graphical HMI	
Screen size	4.0" diagonal
Display format	480 x 480 Dots
Number of colour	16.7M
Dimensions	77 mm (H) x 80 mm (V) x 2.3 mm (D)
Active area	71.86 mm (H) x 70.18 mm (V)
Display mode	Transmissive/normally black
Viewing direction	All round
Backlight type	LED, white
Operating temperature	-30°C ~ +85°C
Storage temperature	-40°C ~ +90°C

29.2.2 FRONT USB PORT

Front USB Port	
Use	For local connection to laptop for configuration purposes and firmware downloads
Connector	USB type B
Isolation	Isolation to ELV level
Constraints	Maximum cable length 5 m

29.2.3 REAR SERIAL PORT 1

Rear Serial Port 1 (RP1)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus
Connector	General purpose block, M4 screws (2 wire)
Cable	Screened twisted pair (STP)
Supported protocols *	Courier, IEC-60870-5-103, DNP3.0
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m

29.2.4 FIBRE REAR SERIAL PORT 1

Optional Fibre Rear Serial Port (RP1)	
Main Use	Serial SCADA communications over fibre
Connector	IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx)
Fibre type	Multimode 50/125 µm or 62.5/125 µm
Supported protocols	Courier, IEC870-5-103, DNP 3.0
Wavelength	850 nm

29.2.5 REAR SERIAL PORT 2

Optional Rear Serial Port (RP2)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus, EIA(RS)232
Designation	SK4
Connector	9 pin D-type female connector
Cable	Screened twisted pair (STP)
Supported protocols	Courier
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m for RS485 and K-bus, 15 m for RS232

29.2.6 OPTIONAL REAR SERIAL PORT (SK5)

Optional Rear Serial Port for Teleprotection	
Use	For teleprotection in distance products
Standard	EIA(RS)232
Designation	SK5
Connector	9 pin D-type female connector
Cable	Screened twisted pair (STP)
Supported protocols	InterMiCOM (IM)
Isolation	Isolation to SELV level
Constraints	Maximum cable length 15 m

29.2.7 IRIG-B (DEMODULATED)

IRIG-B Interface (Demodulated)	
Use	External clock synchronisation signal
Standard	IRIG 200-98 format B00X
Connector	BNC
Cable type	50 ohm coaxial
Isolation	Isolation to SELV level
Input signal	TTL level
Input impedance	10 k ohm at dc
Accuracy	+/-1 ms

29.2.8 IRIG-B (MODULATED)

IRIG-B Interface (Modulated)	
Use	External clock synchronisation signal
Standard	IRIG 200-98 format B12X
Connector	BNC
Cable type	50 ohm coaxial
Isolation	Isolation to SELV level

IRIG-B Interface (Modulated)	
Input signal	Peak to peak, 200 mV to 20 mV
Input impedance	6 k ohm at 1000 Hz
Accuracy	+/-1 ms

29.2.9 REAR ETHERNET PORT COPPER

Rear Ethernet Port using CAT 5/6/7 Wiring	
Main use	Substation Ethernet communications
Standard	IEEE 802.3 100BaseTX
Connector	RJ45
Cable type	Screened twisted pair (STP)
Isolation	1.5 kV
Supported protocols	Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog
Redundancy protocols supported	PRP (Parallel Redundancy Protocol) HSR (High-availability Seamless Redundancy) RSTP (Rapid Spanning Tree Protocol) Failover
Constraints	Maximum cable length 100 m

29.2.10 REAR ETHERNET PORT FIBRE

Rear Ethernet Port using Fibre-optic Cabling	
Main use	Substation Ethernet communications
Connector	IEC 874-10 BFOC 2.5 - (LC®) (1 each for Tx and Rx)
Standard	IEEE 802.3 100 BaseFX
Fibre type	Multimode 50/125 µm (OM2 or OM3) or 62.5/125 µm (OM1)
Supported protocols	Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog
Redundancy protocols supported	PRP (Parallel Redundancy Protocol) HSR (High-availability Seamless Redundancy) RSTP (Rapid Spanning Tree Protocol) Failover
Wavelength	1310 nm

29.2.10.1 100 BASE FX RECEIVER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Input optical power minimum at window edge	PIN Min. (W)	-31.0		-12.0	dBm avg.
Input optical power minimum at eye centre	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input optical power maximum	PIN Max.	-14	-11.8		dBm avg.

Note:
Conditions: TA = 0°C to 70°C

29.2.10.2 100 BASE FX TRANSMITTER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Output optical power BOL 62.5/125 µm NA = 0.275 Fibre EOL	PO	-20	-17.0	-14.0	dBm avg.
Output optical power BOL 50/125 µm NA = 0.20 Fibre EOL	PO	-24.0	-21.0	-17.0	dBm avg.
Optical extinction ratio	ER	10			dB
Output optical power at logic "0" state	$P_{O(off)}$			-45	dBm avg.

Note:
Conditions: TA = 0°C to 70°C

29.2.11 1 PPS PORT

1 PPS Port (Fibre)	
Main use	GPS accuracy clock reference
Connector	BFOC 2.5 –(ST®)
Standard	IEC 874-10
Fibre type	Multimode 50/125 µm or 62.5/125 µm
Wavelength	850 nm
Minimum reception level	-28 dBm
Accuracy	Better than +/- 50 ns for maximum absolute error between actual GPS time and rising edge of 1 PPS signal

29.2.12 FIBRE TELEPROTECTION INTERFACE

Fibre Teleprotection Interface	
Main use	Teleprotection communications
Connectors (2)	BFOC 2.5 –(ST®)
Standard	IEC 874-10
Protocol	InterMicom 64
Fibre type	Multimode 50/125 µm or 62.5/125 µm or single-mode 9/125 µm
Wavelength	850 nm or 1300 nm (multimode), 1300 nm or 1500 nm (single mode)
Minimum reception level	-28 dBm
Accuracy	Better than +/- 50 ns for maximum absolute error between actual GPS time and rising edge of 1 PPS signal

Optical Budget

	850nm MM	1300 nm MM	1300 nm SM	1550 nm SM
Minimum transmit output level (average power)	-19 dBm	-6 dBm	-6 dBm	-6 dBm
Receiver sensitivity (average power)	-32 dBm	-49 dBm	-49 dBm	-49 dBm
Optical budget	13 dB	43 dB	43 dB	43 dB
Less safety margin (3 dB)	10 dB	40 dB	40 dB	40 dB
Typical cable loss	2.6 dB/km	0.8 dB/km	0.4 dB/km	0.3 dB/km
Maximum transmission distance	3.8 km	50 km	100 km	130 km
Typical transmitter optical power	-16 dBm	-	-	-
Maximum receiver optical power	-11 dBm	-	-	-

Note:
This optical interface has been designed and tested for compliance with IEEE C37.94.

29.3 PROTECTION FUNCTIONS

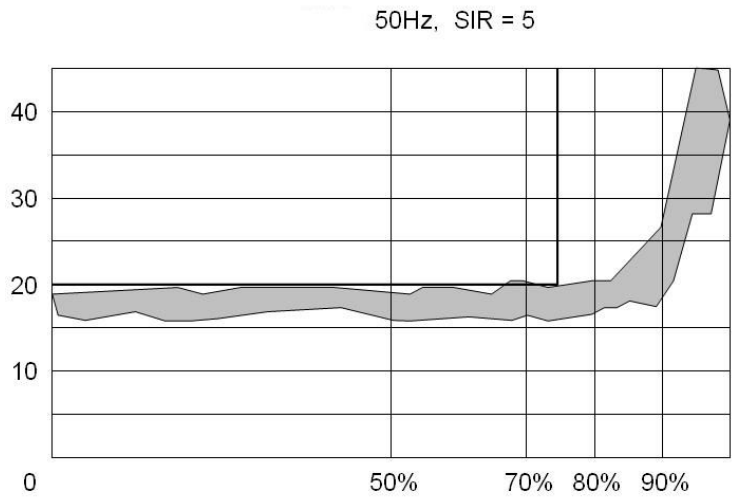
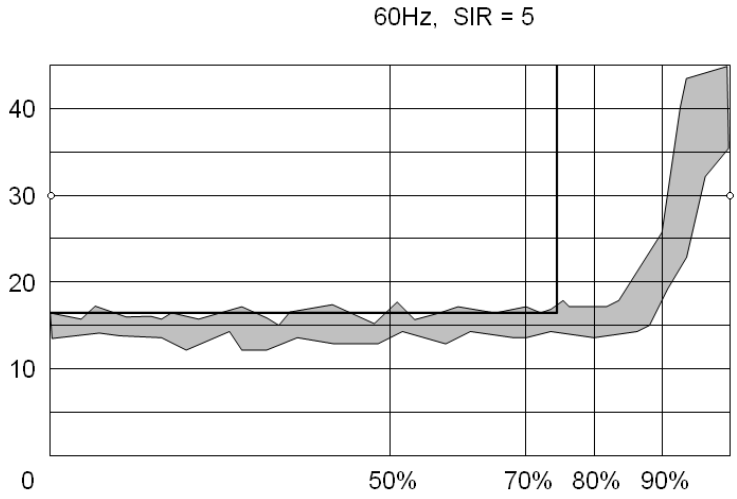
29.3.1 PHASE CURRENT DIFFERENTIAL PROTECTION

Accuracy	
Pick-up	Formula +/-10%
Drop-off	0.75 x Formula +/-10%
IDMT characteristic shape	+/-5% or 40 ms, whichever is greater
DT operation	+/-2% or 20 ms, whichever is greater
Typical instantaneous operation with default settings, back-to-back propagation delay included 50 Hz, 1 p.u. ≤ relay current < 2 p.u. 60 Hz, 1 p.u. ≤ relay current < 2 p.u. 50 Hz, relay current ≥ 2 p.u. 60 Hz, relay current ≥ 2 p.u.	 <35 ms <30 ms <30 ms <25 ms
Reset time	<60 ms
Repeatability	+/-2.5%
Characteristic	UK curves IEC 60255-151: 2009 US curves IEEE C37.112 – 1996
Vector compensation	No affect on accuracy
Current transformer ratio compensation	No affect on accuracy
High set characteristic setting	No affect on accuracy
Three ended scheme operation	No affect on accuracy

29.3.2 NEUTRAL CURRENT DIFFERENTIAL PROTECTION

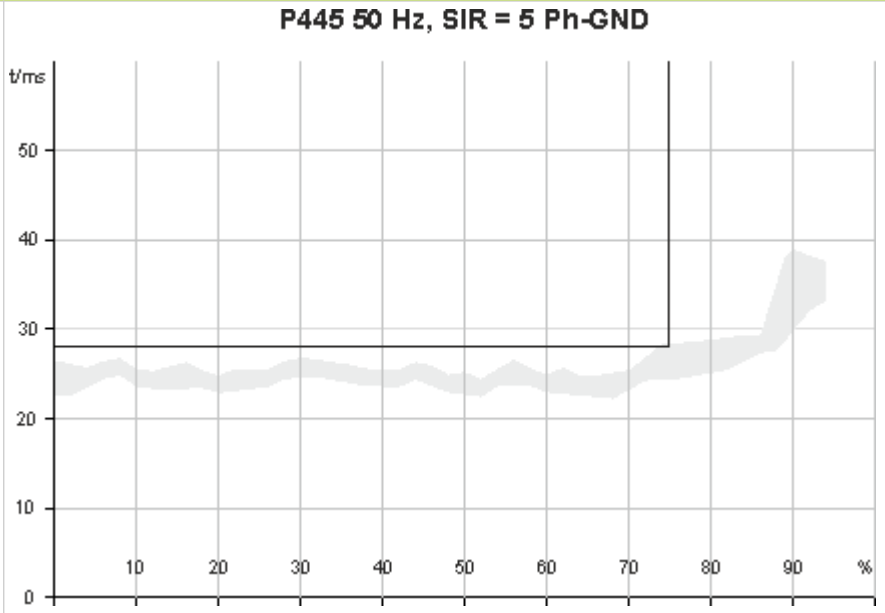
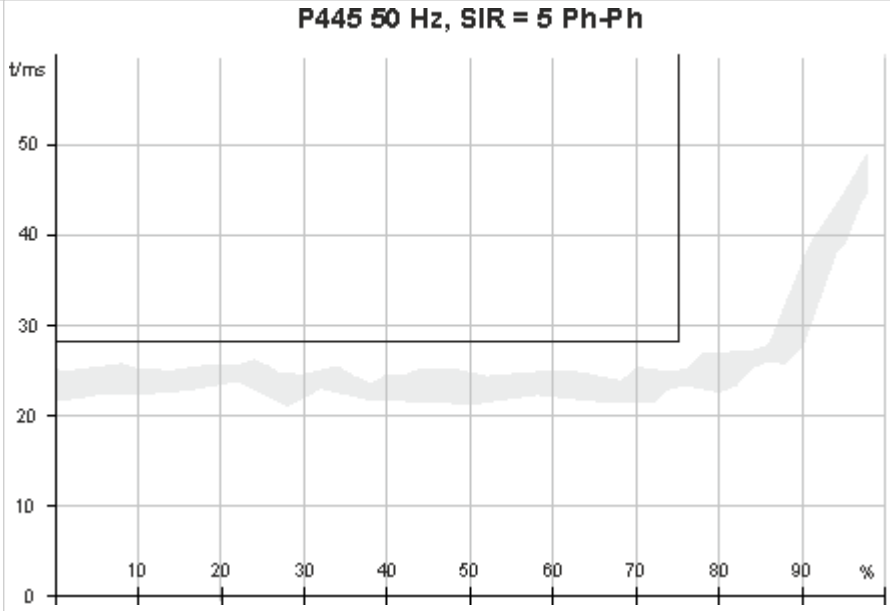
Accuracy	
Pick-up	Formula +/-10%
Drop-off	0.75 x Formula +/-10%
DT operation	+/-2% or 40 ms, whichever is greater
Typical instantaneous operation with default settings and IN Differential > 50% above threshold 50 Hz 60 Hz	 30 - 50 ms 25 - 42 ms
Repeatability	+/-2.5%
Current transformer ratio compensation	No affect on accuracy
Three ended scheme operation	No affect on accuracy

29.3.3 DISTANCE PROTECTION - CHARACTERISTIC A

Tripping Characteristics P54xxxxxxxAxxxQ Subcycle Transmission Distance	
Operating time versus reach percentage, for faults close to line angle. 50 Hz, SIR = 5 All quoted operating times include closure of the trip output contact.	
Operating time versus reach percentage, for faults close to line angle. 60 Hz, SIR = 5 All quoted operating times include closure of the trip output contact.	
Operating time for resistive faults > 20% inside the characteristic Reset time	50 Hz, up to SIR = 30 < 30 ms 60 Hz, up to SIR = 30 < 25 ms Typically < 60 ms

Accuracy	
Characteristic shape, up to SIR = 30	+/-5% for on-angle fault (on the set line angle) +/-10% for off-angle fault Example: For a 70 degree set line angle, injection testing at 40 degrees would be referred to as "off-angle".
Zone time delay deviations	+/-20 ms or 2%, whichever is greater

29.3.4 DISTANCE PROTECTION - CHARACTERISTIC B

Tripping Characteristics P54xxxxxxxBxxxQ Subtransmission/Distribution Distance Protection, 3 Pole Tripping only	
Ph-Gnd Operating time versus reach percentage, for faults close to line angle. 50 Hz, SIR = 5 Ph-GND All quoted operating times include closure of the trip output contact.	
Ph-Ph Operating time versus reach percentage, for faults close to line angle. 50 Hz, SIR = 5 Ph-Ph All quoted operating times include closure of the trip output contact.	

Accuracy	
Characteristic shape, up to SIR = 30	+/-5% for on-angle fault (on the set line angle) +/-10% for off-angle fault Example: For a 70 degree set line angle, injection testing at 40 degrees would be referred to as "off-angle".
Zone time delay deviations	+/-20 ms or 2%, whichever is greater

29.3.5 POWER SWING BLOCKING

Accuracy	
Accuracy of zones and timers	As per Distance

29.3.6 OUT OF STEP PROTECTION

Accuracy	
Accuracy of zones and timers	As per distance
Operating range	Up to 7 Hz

29.3.7 FIBRE TELEPROTECTION TRANSFER TIMES

The table below shows the minimum and maximum transfer time for InterMiCOM64 (IM64). The times are measured from opto initialisation (with no opto filtering) to relay standard output and include a small propagation delay for back-back test.

IDiff IM64 indicates InterMiCOM64 signals working in conjunction with the differential protection fibre optic communications channel. IM64 indicates InterMiCOM64 signals working as a standalone feature.

Configuration	Signals	Permissive Op Times (ms)	Direct Op Times (ms)	MaxCh1 Prop Delay Measured
IM64 at 56kbps	8	18-21	21-24	1.6ms
IM64 at 64kbps	8	18-21	21-24	1.3ms
IM64 at 128kbps	24	17-20	20-23	1.4ms
IDiff IM64 at 56kbps	8	24-26	29-31	3.3ms
IDiff IM64 at 64kbps	8	24-26	29-31	2.9ms
IDiff IM64 at 128kbps	32	20-26	24-31	1.9ms

29.3.8 AUTORECLOSE AND CHECK SYNYCHRONISM

Accuracy	
Timers	+/-20 ms or 2%, whichever is greater

29.3.9 PHASE OVERCURRENT PROTECTION

Accuracy	
IDMT pick-up	1.05 x Setting +/-5%
DT pick-up	Setting +/-5%
Drop-off (IDMT and DT)	0.95 x setting +/-5%
IDMT operate time	+/-5% or 40 ms, whichever is greater *
IEEE reset time	+/-5% or 40 ms, whichever is greater **
DT operate time	+/-2% or 25 ms, whichever is greater (non-directional) * +/-2% or 40 ms, whichever is greater (directional) *
DT reset time	+/-5% or 40 ms, whichever is greater **
Repeatability	<5%
Characteristic UK	IEC 60255-151: 2009
Characteristic US	IEEE C37.112 1996

29.3.9.1 TRANSIENT OVERREACH AND OVERSHOOT

Additional tolerance due to increasing X/R ratios	+/-5% over the X/R ratio of 1 to 90
Overshoot of IDMT overcurrent elements	<30 ms
Overshoot of DT overcurrent elements	<25 ms

29.3.9.2 PHASE OVERCURRENT DIRECTIONAL PARAMETERS

Accuracy	
Directional boundary pickup (RCA +/-90%)	+/-2° ◆
Directional boundary hysteresis	<2°
Directional boundary repeatability	<2%

29.3.10 EARTH FAULT PROTECTION

Accuracy	
IDMT pick-up	1.05 x setting +/-5%
DT pick-up	Setting +/-5%, or 20 mA, whichever is greater
Drop-off (IDMT and DT)	0.95 x setting +/-5%
IDMT operate time	+/-5% or 40 ms, whichever is greater *
IEEE reset time	+/-10% or 40 ms, whichever is greater **
Repeatability	<5%
DT operate time	+/-2% or 25 ms, whichever is greater (non-directional) * +/-2% or 40 ms, whichever is greater (directional) *
DT reset time	+/-5% or 40 ms, whichever is greater **

29.3.10.1 EARTH FAULT DIRECTIONAL PARAMETERS

Zero Sequence Polarising Accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2° ◆
Hysteresis	<3°
VN> pick-up	Setting +/-10%
VN> drop-off	0.9 x setting +/-10%

Negative Sequence Polarising Accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2° ◆
Hysteresis	<3°
V2> pick-up	Setting +/-10%
V2> drop-off	0.9 x setting +/-10%
I2> pick-up	Setting +/-10%
I2> drop-off	0.9 x setting +/-10%

29.3.11 SENSITIVE EARTH FAULT PROTECTION

IDMT Pick-up	1.05 x Setting +/-5%
DT Pick-up	Setting +/-5%
Drop-off (IDMT + DT)	0.95 x setting +/-5%
IDMT operate time	+/-5% or 40 ms, whichever is greater *
IEEE reset time	+/-5% or 40 ms, whichever is greater **
DT operate time	+/-2% or 25 ms, whichever is greater (non-directional) * +/-2% or 40 ms, whichever is greater (directional) *
DT reset time	+/-5% or 40 ms, whichever is greater **
Repeatability	<5%

Note:
SEF claims apply to SEF input currents of no more than 2 x In. For input ranges above 2 x In, the claim is not supported.

29.3.11.1 SENSITIVE EARTH FAULT PROTECTION DIRECTIONAL ELEMENT

Directional Accuracy	
Directional boundary pick-up (RCA+/-90°)	+/-5° ◆
Hysteresis	<3°
VN> pick-up	Setting +/-10%
VN> drop-off	0.9 x setting +/-10%

Wattmetric SEF Accuracy	
Pick-up P = 0 W	ISEF> +/-5% or 5 mA
Pick-up P > 0 W	P > +/-5%
Drop-off P = 0 W	0.95 x ISEF> +/-5% or 5 mA
Drop-off P > 0 W	0.9 x P> +/-5% or 5 mA
Boundary accuracy	+/-5° with hysteresis < 1°
Repeatability	<1%

SEF CosΦ Accuracy	
Pick-up	Setting +/-5% for angles RCA+/-60°
Drop-off	0.95 x setting +/-5%
Repeatability	+/-2%

SEF SinΦ Accuracy	
Pick-up	Setting +/-5% for angles RCA+/-60° to RCA+/-90°
Drop-off	0.9 x setting +/-5%
Repeatability	+/-2%

29.3.12 RESTRICTED EARTH FAULT PROTECTION

Low Impedance REF	
Pick-up	Setting formula +/- 5%
Drop-off	0.8 x Setting formula +/-5%
Operating time	<60 ms
Repeatability	<5%

High Impedance REF	
High set pick-up	Setting +/-10%
High set operating time	<30 ms
Repeatability	<5%

29.3.13 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

IDMT pick-up	1.05 x Setting +/-5%
DT pick-up	Setting +/-5%
Drop-off (IDMT and DT)	0.95 x Setting +/-5%
IDMT operate time	+/-5% or 40 ms, whichever is greater *
DT operate time	+/-2% or 60 ms, whichever is greater **
DT Reset time	Setting +/-5%

29.3.13.1 NEGATIVE SEQUENCE OVERCURRENT PROTECTION DIRECTIONAL PARAMETERS

Directional boundary pick-up (RCA+/-90%)	+/-2° ◆
Directional boundary hysteresis	<1°
Directional boundary repeatability	<1%

29.3.14 CIRCUIT BREAKER FAIL AND UNDERCURRENT PROTECTION

I< Pick-up	Setting +/-10% or 0.025 In, whichever is greater
I< Drop-off	Setting +/-5% or 20 mA, whichever is greater
Operate time	<12 ms ‡
Timers	+/-2% or 20 ms, whichever is greater
Reset time	<15 ms

Note:
‡ Operating time measured with applied current of 20% above thermal setting.

29.3.15 BROKEN CONDUCTOR PROTECTION

Pick-up	Setting +/- 2.5%
Drop-off	0.95 x Setting +/- 2.5%
DT operate time	+/- 2% or 40 ms, whichever is greater
Reset time	<30 ms

29.3.16 THERMAL OVERLOAD PROTECTION

Thermal alarm pick-up	Calculated trip time +/-10%
Thermal overload pick-up	Calculated trip time +/-10%
Cooling time accuracy	+/-15% of theoretical
Repeatability	<5%

Note:
*‡ **CS VT Ph Shift** setting = 0°.*
** Reference conditions: Injected value is 2 x pick-up value or more, effective range (0.1 - 20In).*
*** Reference conditions: Injected value instantaneously reduced to 0 (zero) from 2 x pick-up value.*
♦ Reference conditions: Tested with nominal voltage or current.

29.4 PERFORMANCE OF VOLTAGE PROTECTION FUNCTIONS

29.4.1 OVERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/-1%
Pick-up (IDMT)	1.02 x setting +/-2%
Drop-off (DT and IDMT)	0.98 x setting +/-2%
DT operate time	+/-2% or 40 ms, whichever is greater
IDMT operate time	+/-2% or 40 ms, whichever is greater
Reset	<75 ms
Repeatability	<1%

29.4.2 UNDERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/-5%
Pick-up (IDMT)	0.98 x setting +/-2%
Drop-off (DT and IDMT)	1.02 x setting +/-2%
DT operate time	+/-2% or 50 ms, whichever is greater ⌑
IDMT operate time	+/-5% or 50 ms, whichever is greater ⌑
Reset	<35 ms
Repeatability	<1%

29.4.3 RESIDUAL OVERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/-5%
Pick-up (IDMT)	1.05 x setting +/-5%
Drop-off (DT and IDMT)	0.95 x Setting +/-5%
DT operate time	+/-2% or 60 ms, whichever is greater ⌑
IDMT operate time	+/-5% or 65 ms, whichever is greater ⌑
Instantaneous operation	<50 ms
Reset	<35 ms
Repeatability	<10%

29.4.4 COMPENSATED OVERVOLTAGE PROTECTION

Pick-up (DT)	Setting +/-1%
Pick-up (IDMT)	1.02 x Setting +/-2%
Drop-off (DT and IDMT)	(1-(**Cp V Hysteresis** setting))* setting +/-2%
DT operate time	+/-2% or 40 ms, whichever is greater

IDMT operate time	+/-2% or 40 ms, whichever is greater
Reset	< 75 ms
Repeatability	< 1%

29.4.5 VOLTAGE MONITOR

Live Voltage Accuracy	
Pick-up	Setting +/-3% or +/-0.1 V, whichever is greater
Drop-off	(0.98 x setting) +/-3% or +/-0.1 V, whichever is greater
Repeatability	<1%

Dead Voltage Accuracy	
Pick-up	Setting +/-3% or +/-0.1 V, whichever is greater
Drop-off	(1.02 x setting) +/-3% or +/-0.1 V, whichever is greater
Repeatability	<1%

Diff Voltage Accuracy	
Pick-up	Setting +/-3% or +/-0.1 V, whichever is greater
Drop-off	(0.98 x setting) +/-3% or +/-0.1 V, whichever is greater
Repeatability	<1%

Overvoltage Accuracy	
Pick-up	Setting +/-3% or +/-0.1 V, whichever is greater
Drop-off	(0.98 x setting) +/-3% or +/-0.1 V, whichever is greater
Repeatability	<1%

Undervoltage Accuracy	
Pick-up	Setting +/-3% or +/-0.1 V, whichever is greater
Drop-off	(1.02 x setting) +/-3% or +/-0.1 V, whichever is greater
Repeatability	<1%

29.4.6 CHECK SYNCHRONISATION

Accuracy (CS1/CS2)	
Phase Angle	
Pick-up	(Setting-2°) ±1° ‡
Drop-off	(Setting-1°) ±1° ‡
Repeatability	<1%
Slip Frequency	
Pick-up	Setting ±0.01 Hz
Drop-off	(0.95 x Setting) ±0.01 Hz
Repeatability	<1%
Slip Timer	

Accuracy (CS1/CS2)	
Timers	+/-1% or 40 ms, whichever is greater
Reset time	<30 ms
Repeatability	<10 ms

29.4.7 SYSTEM SPLIT

SS Phase Angle Accuracy	
Pick-up	(Setting +2°) +/-1°
Drop-off	(Setting +1°) +/-1°
Repeatability	<1%

SS Undervoltage Accuracy	
Pick-up	Setting +/-3%
Drop-off	1.02 x setting
Repeatability	<1%

SS Timer	
Timers	Setting +/-1% or 40 ms, whichever is greater
Reset time	<30 ms
Repeatability	<10 ms

29.5 PERFORMANCE OF FREQUENCY PROTECTION FUNCTIONS

29.5.1 OVERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/-10 mHz
Drop-off	Setting -20 mHz +/-10 mHz
Operating timer	+/-2% or 50 ms, whichever is greater

Operating and Reset Time	
Operating time (Fs/Ff ratio less than 2)	<125 ms
Operating time (Fs/Ff ratio between 2 and 30)	<150 ms
Operating time (Fs/Ff ratio greater than 30)	<200 ms
Reset time	<200 ms

Note:
Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.
Fs = start frequency - frequency setting
Ff = frequency setting - end frequency

29.5.2 UNDERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/-10 mHz
Drop-off	Setting + 20 mHz +/-10 mHz
Operating timer	+/-2% or 50 ms, whichever is greater

Operating and Reset Time	
Operating time (Fs/Ff ratio less than 2)	<100 ms
Operating time (Fs/Ff ratio between 2 and 6)	<160 ms
Operating time (Fs/Ff ratio greater than 6)	<230 ms
Reset time	<200 ms

Note:
Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.
Fs = start frequency - frequency setting
Ff = frequency setting - end frequency

29.5.3 INDEPENDENT RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (df/dt)	Setting +/-3% or +/-10 mHz/s, whichever is greater

Accuracy	
Drop-off (df/dt, for settings between 10 mHz/s and 100 mHz/s)	(Setting -5 mHz/s) +/-3% or +/-10 mHz/s, whichever is greater
Drop-off (df/dt, for settings greater than 100 mHz/s)	(0.95 x Setting) +/-3% or +/-10 mHz/s, whichever is greater
Operating timer	+/-2% or 50 ms, whichever is greater

Operating and Reset Time	
Operating time (for ramps 2 x setting or greater)	<300 ms
Operating time (for ramps 1.3 x setting or greater)	<475 ms
Reset time	<150 ms

Note:
Reference Conditions: Tested with df/dt Average Cycles = 2, df/dt Smoothing Factor = 0.01, for df/dt settings greater than 0.1 Hz/s, and no intentional time delay.

29.6 POWER PROTECTION FUNCTIONS

29.6.1 OVERPOWER/UNDERPOWER PROTECTION

Pick-up	Setting +/-10%
Reverse/overpower drop-off	0.95 x setting +/-10%
Low forward power drop-off	1.05 x setting +/-10%
Angle variation pick-up	+/-2°
Angle variation drop-off	+/-2.5°
Operating time	+/-2% or 50 ms, whichever is greater
Repeatability	<5%
Disengagement time	<50 ms
tRESET	+/-5%
Instantaneous operating time	<50 ms

29.7 MONITORING, CONTROL AND SUPERVISION

29.7.1 VOLTAGE TRANSFORMER SUPERVISION

Fast block operation, loss of 1 and 2 phases	<1 cycle
Fast block operation, loss of 3 phases	<1.5 cycle
Time delay	+/-2% or 30 ms, whichever is greater

29.7.2 STANDARD CURRENT TRANSFORMER SUPERVISION

IN> Pick-up	Setting +/-5%
VN< Pick-up	Setting +/-5%
IN> Drop-off	0.9 x setting +/-5%
VN< Drop-off	1.05 x setting +/-5% or 1 V, whichever is greater
Time delay operation	Setting +/-2% or 30 ms, whichever is greater
CTS block operation	<1 cycle
CTS reset	<35 ms

29.7.3 DIFFERENTIAL CURRENT TRANSFORMER SUPERVISION

Accuracy	
I1> Pick-up	Setting +/- 5%
I1> Drop-off	0.9 x setting +/- 5%
I2/I1> Pick-up	Setting +/- 5%
I2/I1> Drop-off	0.9 x setting +/-5%
I2/I1>> Pick-up	Setting +/- 5%
I2/I1 >> Drop-off	0.9 x setting +/-5%
Time delay operation	Setting +/-2% or 20 ms, whichever is greater
CTS block diff operation	<1 cycle
CTS reset	<35 ms

29.7.4 CB STATE AND CONDITION MONITORING

Accuracy	
Timers	+/-40 ms or 2%, whichever is greater
Broken current accuracy	+/-5%
Reset time	<30 ms

29.7.5 PSL TIMERS

Output conditioner timer	Setting +/-2% or 50 ms, whichever is greater
Dwell conditioner timer	Setting +/-2% or 50 ms, whichever is greater
Pulse conditioner timer	Setting +/-2% or 50 ms, whichever is greater

29.8 MEASUREMENTS AND RECORDING

29.8.1 GENERAL

General Measurement Accuracy	
Current (0.05 to 3 In)	+/-0.5% between 0.2 - 2 In Else +/-1.0% or 4mA whichever is greater (1A input) Else +/-1.0% or 20mA whichever is greater (5A input)
Voltage (0.05 to 2 Vn)	+/-0.5% between 0.2 - 2 Vn Else +/-1.0% or 100mV whichever is greater
Phase	+/-2° at rated voltage and current
Frequency (45 to 65 Hz)	+/-0.025 Hz
Power (W) (0.2 to 2 Vn and 0.05 to 3 In)	+/-5.0% of reading at unity power factor
Reactive power (Vars) (0.2 to 2 Vn and 0.05 to 3 In)	+/-5.0% of reading at zero power factor
Apparent power (VA) (0.2 to 2 Vn and 0.05 to 3 In)	+/-.0% of reading
Energy (Wh) (0.2 to 2 Vn and 0.2 to 3 In)	+/-5.0% of reading at unity power factor
Energy (Varh) (0.2 to 2 Vn and 0.2 to 3In)	+/-5.0% of reading at zero power factor

29.8.2 DISTURBANCE RECORDS

Disturbance Records Measurement Accuracy	
Minimum record duration	0.1 s
Maximum record duration	10.5 s
Minimum number of records at 10.5 seconds	100
Magnitude and relative phases accuracy	+/-5% of applied quantities
Duration accuracy	+/-2%
Trigger position accuracy	+/-2% (minimum Trigger 100 ms)

29.8.3 EVENT, FAULT AND MAINTENANCE RECORDS

Event, Fault & Maintenance Records	
Record location	Flash memory
Viewing method	Front panel display or Settings Application Software
Extraction method	Extracted via USB, RP1, RP2, NIC (Ethernet) port
Number of event records	Up to 5000 time tagged event records (newest overwrites oldest)
Number of fault records	Up to 100
Number of maintenance records	Up to 10
Event time stamp resolution	1 ms

29.8.4 FAULT LOCATOR

Accuracy	
Fault Location	+/-5% of line length Reference conditions: solid fault applied on line

29.9 RATINGS

29.9.1 AC MEASURING INPUTS

AC Measuring Inputs	
Nominal frequency	50 Hz or 60 Hz (settable)
Operating range	45 to 65 Hz
Phase rotation	ABC or CBA

29.9.2 CURRENT TRANSFORMER INPUTS

AC Current Inputs	
Nominal current (In)	1A or 5A
Nominal burden per phase	<0.2 VA at In
AC current thermal withstand (5A input)	20 A (continuous operation) 150 A (for 10 s) 500 A (for 1 s)
AC current thermal withstand (1A input)	4 A (continuous operation) 30 A (for 10 s) 100 A (for 1 s)
Linearity	Standard: Linear up to 64 × In (non-offset AC current) Sensitive: Linear up to 2 × In (non-offset AC current)

29.9.3 VOLTAGE TRANSFORMER INPUTS

AC Voltage Inputs	
Nominal voltage (Vn)	100 V to 120 V (ph-ph)
Nominal burden per VT input *1	<0.003 VA @ 69.3 V (ph-n) <0.01 VA @ 138.6 V (ph-n)
Linearity for each VT input	Linear up to 200 Vac rms
Continuous rating for each VT input	240 Vac rms
10 seconds rating for each VT input	312 Vac rms

Note:
*Reference Conditions: * = Overfrequency operating range 50/60 Hz and over temperature range 20° +/-5°C.*

29.9.4 AUXILIARY SUPPLY VOLTAGE

Nominal operating range	CORTEC option (DC only) 24 to 48 V DC CORTEC option (rated for AC or DC operation) 48 to 110 V DC 40 to 100 V AC rms CORTEC option (rated for AC or DC operation) 110 to 250 V DC 100 to 240 V AC rms

Maximum operating range	CORTEC option (DC only) 19 to 65 V DC CORTEC option (rated for AC or DC operation) 37 to 150 V DC 32 to 110 V AC rms CORTEC option (rated for AC or DC operation) 87 to 300 V DC 80 to 265 V AC rms
Frequency range for AC supply	45 to 65 Hz
Ripple	<15% for a DC supply (compliant with IEC 60255-26:2013)
Power up time	<11 seconds

29.9.5 NOMINAL BURDEN

Quiescent burden	11.2 W or 22 VA
2nd rear communications port	1.25 W or 2.5 VA
Each relay output burden	0.13 W or 0.25 VA per output relay
Each opto-input burden (24 - 27 V)	0.065 W or 0.13 VA max
Each opto-input burden (30 - 34 V)	0.065 W or 0.13 VA max
Each opto-input burden (48 - 54 V)	0.125 W or 0.25 VA max
Each opto-input burden (110 - 125 V)	0.36 W or 0.72 VA max
Each opto-input burden (220 - 250 V)	0.9 W or 1.8 VA max

29.9.6 POWER SUPPLY INTERRUPTION

Standard	IEC 60255-26:2013 (DC and AC)
24 - 48V DC Supply 100% interruption without de-energising	20 ms at 24 V (half and full load) 50 ms at 36 V (half and full load) 100 ms at 48 V (half and full load)
48 - 110V DC Supply 100% interruption without de-energising	20 ms at 37 V (half and full load) 50 ms at 60 V (half and full load) 100 ms at 72 V (half load) 100 ms at 85 V (full load) 200 ms at 110 V (half and full load)
110 - 250V DC Supply 100% interruption without de-energising	20 ms at 87 V (half load) 50 ms at 110 V (half load) 50 ms at 98 V (full load) 100 ms at 160 V (half load) 100 ms at 135 V (full load) 200 ms at 210 V (half load) 200 ms at 174 V (full load)
40 - 100V AC Supply 100% voltage dip without de-energising	50 ms at 32 V (half load) 10 ms at 32 V (full load)
100 - 240V AC Supply 100% voltage dip without de-energising	50 ms at 80 V (full and half load)

Note:
Maximum loading = all inputs/outputs energised.
Quiescent or 1/2 loading = 1/2 of all inputs/outputs energised.

29.9.7 SUPERCAPACITOR

Discharge time	>14 days

29.10 INPUT/OUTPUT CONNECTIONS

29.10.1 ISOLATED DIGITAL INPUTS

Opto-isolated Digital Inputs (Opto-inputs)	
Compliance	ESI 48-4
Rated nominal voltage	24 to 250 V dc
Operating range	19 to 265 V dc
Withstand	300 V dc
Recognition time with half-cycle ac immunity filter removed	<2 ms
Recognition time with filter on	<12 ms

29.10.1.1 NOMINAL PICKUP AND RESET THRESHOLDS

Nominal Battery Voltage	Logic Levels: 60-80% DO/PU	Logic Levels: 50-70% DO/PU
24/27 V	Logic 0 <16.2 V, Logic 1 >19.2 V	Logic 0 <12 V, Logic 1 >16.8 V
30/34	Logic 0 <20.4 V, Logic 1 >24 V	Logic 0 <15 V, Logic 1 >21 V
48/54	Logic 0 <32.4 V, Logic 1 >38.4 V	Logic 0 <24 V, Logic 1 >33.6 V
110/125	Logic 0 <75 V, Logic 1 >88 V	Logic 0 <55 V, Logic 1 >77 V
220/250	Logic 0 <150 V, Logic 1 >176 V	Logic 0 <110 V, Logic 1 >154 V

Note:
Filter is required to make the opto-inputs immune to induced AC voltages.

In addition to the above thresholds, some models of this product provide the following threshold levels for FSK applications:

- For 220/250 voltage inputs: Logic 0 < 145V, Logic 1 > 165V

29.10.2 STANDARD OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	General purpose relay outputs for signalling, tripping and alarming
Rated voltage	300 V
Maximum continuous current	10 A
Short duration withstand carry	30 A for 3 s 250 A for 30 ms
Make and break, dc resistive	50 W
Make and break, dc inductive	62.5 W (L/R = 50 ms)
Make and break, ac resistive	2500 VA resistive (cos phi = unity)
Make and break, ac inductive	2500 VA inductive (cos phi = 0.7)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to a maximum load of 7500W))
Make, carry and break, dc resistive	4 A for 1.5 s, 10000 operations (subject to the above limit for make and break, dc resistive load)

Make, carry and break, dc inductive	0.5 A for 1 s, 10000 operations (subject to the above limit for make and break, dc inductive load)
Make, carry and break ac resistive	30 A for 200 ms, 2000 operations (subject to the above limits)
Make, carry and break ac inductive	10 A for 1.5 s, 10000 operations (subject to the above limits)
Loaded contact	10000 operations min.
Unloaded contact	100000 operations min.
Operate time	<5 ms
Reset time	<10 ms

29.10.3 HIGH BREAK OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	For applications requiring high rupture capacity
Rated voltage	300 V
Maximum continuous current	10 A DC
Short duration withstand carry	30 A DC for 3 s 250 A for 30 ms
Make and break, dc resistive	7500 W
Make and break, dc inductive	2500 W (L/R = 50 ms)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to the above limits)
Make, carry and break, dc resistive	30 A for 3 s, 5000 operations (subject to the above limit for make and break, dc resistive load) 30 A for 200 ms, 10000 operations (subject to the above limit for make and break, dc resistive load)
Make, carry and break, dc inductive	10 A for 40 ms, 10000 operations (subject to the above limit for make and break, dc inductive load) 10 A for 20 ms (250 V, 4 shots per second, subject to the above limit for make and break, dc inductive load)
Loaded contact	10,000 operations minimum.
Unloaded contact	100,000 operations minimum.
Operate time	<0.2 ms
Reset time	<8 ms
MOV Protection	Maximum voltage 330 V DC

29.10.4 WATCHDOG CONTACTS

Use	Non-programmable contacts for relay healthy/relay fail indication
Breaking capacity, dc resistive	30 W
Breaking capacity, dc inductive	15 W (L/R = 40 ms)
Breaking capacity, ac inductive	375 VA inductive (cos phi = 0.7)

29.11 MECHANICAL SPECIFICATIONS

29.11.1 PHYSICAL PARAMETERS

Case Types*	40TE 60TE 80TE
Weight (40TE case)	7 kg - 8 kg (depending on chosen options)
Weight (60TE case)	9 kg - 12 kg (depending on chosen options)
Weight (80TE case)	13 kg - 16 kg (depending on chosen options)
Dimensions in mm (w x h x l) (40TE case)	W: 206.0 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w x h x l) (60TE case)	W: 309.6 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w x h x l) (80TE case)	W 413.2 mm H 177.0 mm D 243.1 mm
Mounting	Panel, rack, or retrofit

Note:
** Case size is product dependent.*

29.11.2 ENCLOSURE PROTECTION

Against dust and dripping water (front face)	IP52 as per IEC 60529:1989/A2:2013
Protection against dust (whole case)	IP50 as per IEC 60529:1989/A2:2013
Protection for sides of the case (safety)	IP30 as per IEC 60529:1989/A2:2013
Protection for rear of the case (safety)	IP10 as per IEC 60529:1989/A2:2013

29.11.3 MECHANICAL ROBUSTNESS

Vibration test per EN 60255-21-1:1998	Response: class 2, Endurance: class 2
Shock and bump immunity per EN 60255-21-2:1988	Shock response: class 2, Shock withstand: class 1, Bump withstand: class 1
Seismic test per EN 60255-21-3: 1993	Class 2

29.11.4 TRANSIT PACKAGING PERFORMANCE

Primary packaging carton protection	ISTA 1C
Vibration tests	3 orientations, 7 Hz, amplitude 5.3 mm, acceleration 1.05g
Drop tests	10 drops from 610 mm height on multiple carton faces, edges and corners

29.12 TYPE TESTS

29.12.1 INSULATION

Compliance	IEC 60255-27: 2013
Insulation resistance	>100 M ohm at 500 V DC (Using only electronic/brushless insulation tester)

29.12.2 CREEPAGE DISTANCES AND CLEARANCES

Compliance	IEC 60255-27: 2013
Pollution degree	3
Overvoltage category	III
Impulse test voltage (not RJ45)	5 kV
Impulse test voltage (RJ45)	1 kV

29.12.3 HIGH VOLTAGE (DIELECTRIC) WITHSTAND

IEC compliance	IEC 60255-27: 2013
Between all independent circuits	2 kV ac rms for 1 minute
Between independent circuits and protective earth conductor terminal	2 kV ac rms for 1 minute
Between all case terminals and the case earth	2 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute
Across open contacts of changeover output relays	1 kV ac rms for 1 minute
Between all RJ45 contacts and protective earth	1 kV ac rms for 1 minute
Between all screw-type EIA(RS)485 contacts and protective earth	1 kV ac rms for 1 minute
ANSI/IEEE compliance	ANSI/IEEE C37.90-2005
Across open contacts of normally open output relays	1.5 kV ac rms for 1 minute
Across open contacts of normally open changeover output relays	1 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute

29.12.4 IMPULSE VOLTAGE WITHSTAND TEST

Compliance	IEC 60255-27: 2013
Between all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between terminals of all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between all independent circuits and protective earth conductor terminal	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J

Note:
Exceptions are communications ports and normally-open output contacts, where applicable.

29.13 ENVIRONMENTAL CONDITIONS

29.13.1 AMBIENT TEMPERATURE RANGE

Compliance	IEC 60255-27: 2013
Test method	IEC 60068-2-1:2007 and IEC 60068-2-2 2007
Operating temperature range	-25°C to +55°C (continuous)
Storage and transit temperature range	-25°C to +70°C (continuous)

29.13.2 TEMPERATURE ENDURANCE TEST

Temperature Endurance Test	
Test method	IEC 60068-2-1: 2007 and 60068-2-2: 2007
Operating temperature range	-40°C (96 hours) +70°C (96 hours)
Storage and transit temperature range	-40°C (96 hours) +70°C (96 hours)

29.13.3 AMBIENT HUMIDITY RANGE

Compliance	IEC 60068-2-78: 2012 and IEC 60068-2-30: 2005
Durability	56 days at 93% relative humidity and +40°C
Damp heat cyclic	Six (12 + 12) hour cycles, 93% RH, +25 to +55°C

29.13.4 CORROSIVE ENVIRONMENTS

Compliance, Industrial corrosive environment/poor environmental control	IEC 60068-2-42:2003, IEC 60068-2-43:2003, IEC 60068-2-52:1996
Sulphur Dioxide, IEC 60068-2-42:2003	21 days exposure to elevated concentrations (25ppm) of SO_2 at 75% relative humidity and +25°C
Hydrogen Sulphide, IEC 60068-2-43:2003	21 days exposure to elevated concentrations (10ppm) of H_2S at 75% relative humidity and +25°C
Salt Mist, IEC 60068-2-52:1996	7 days, KB severity 3

29.14 ELECTROMAGNETIC COMPATIBILITY

29.14.1 1 MHZ BURST HIGH FREQUENCY DISTURBANCE TEST

Compliance	IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Differential test voltage (level 3)	1.0 kV

29.14.2 DAMPED OSCILLATORY TEST

Compliance	EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz. Level 4: 3 MHz, 10 MHz and 30 MHz, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Common-mode test voltage (level 4)	4.0 kV
Differential mode test voltage	1.0 kV

29.14.3 IMMUNITY TO ELECTROSTATIC DISCHARGE

Compliance	IEC 60255-26:2013, IEC 61000-4-2:2009
Class 4 Condition	15 kV discharge in air to user interface, display, and exposed metalwork
Class 3 Condition	8 kV discharge in air to all communication ports

29.14.4 ELECTRICAL FAST TRANSIENT OR BURST REQUIREMENTS

Compliance	IEC 60255-26:2013, IEC 61000-4-4:2012
Applied to communication inputs	Amplitude: 2 kV, burst frequency 5 kHz and 100 KHz (level 4)
Applied to power supply and all other inputs except for communication inputs	Amplitude: 4 kV, burst frequency 5 kHz and 100 KHz (level 4)

29.14.5 SURGE WITHSTAND CAPABILITY

Compliance	IEEE/ANSI C37.90.1: 2012
Condition 1	4 kV fast transient and 2.5 kV oscillatory applied common mode and differential mode to opto inputs, output relays, CTs, VTs, power supply
Condition 2	4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B

29.14.6 SURGE IMMUNITY TEST

Compliance	IEC 60255-26:2013, IEC 61000-4-5:2014 + AMD1:2017

Pulse duration	Time to half-value: 1.2/50 µs
Between all groups and protective earth conductor terminal	Amplitude 4 kV
Between terminals of each group (excluding communications ports, where applicable)	Amplitude 2 kV

29.14.7 IMMUNITY TO RADIATED ELECTROMAGNETIC ENERGY

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency band	80 MHz to 3.0 GHz
Spot tests at	80, 160, 380, 450, 900, 1850, 2150 MHz
Test field strength	10 V/m
Test using AM	1 kHz @ 80%
Compliance	IEEE/ANSI C37.90.2: 2004
Frequency band	80 MHz to 1 GHz
Spot tests at	80, 160, 380, 450 MHz
Waveform	1 kHz @ 80% am and pulse modulated
Field strength	35 V/m

29.14.8 RADIATED IMMUNITY FROM DIGITAL COMMUNICATIONS

Compliance	IEC 61000-4-3:2006 + A2:2010
Frequency bands	800 to 960 MHz, 1.4 to 2.0 GHz
Test field strength	30 V/m
Test using AM	1 kHz/80%

29.14.9 RADIATED IMMUNITY FROM DIGITAL RADIO TELEPHONES

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency bands	900 MHz and 1.89 GHz
Test field strength	10 V/m

29.14.10 IMMUNITY TO CONDUCTED DISTURBANCES INDUCED BY RADIO FREQUENCY FIELDS

Compliance	IEC 60255-26:2013, IEC 61000-4-6:2013 Level 3
Frequency bands	150 kHz to 80 MHz
Test disturbance voltage	10 V rms
Test using AM	1 kHz @ 80%
Spot tests	27 MHz and 68 MHz

29.14.11 MAGNETIC FIELD IMMUNITY

Compliance	IEC 61000-4-8:2009 Level 5 IEC 61000-4-9:2016 Level 5 IEC 61000-4-10:2016 Level 5
IEC 61000-4-8 test	100 A/m applied continuously, 1000 A/m applied for 3 s
IEC 61000-4-9 test	1000 A/m applied in all planes
IEC 61000-4-10 test	100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 seconds

29.14.12 CONDUCTED EMISSIONS

Compliance	IEC 60255-26:2013, EN 55032: 2015 + A1:2020
Power supply test 1	0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
Power supply test 2	0.5 - 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)
RJ45 test 1 (where applicable)	0.15 - 0.5 MHz, 97 dBµV (quasi peak) 84 dBµV (average)
RJ45 test 2 (where applicable)	0.5 - 30 MHz, 87 dBµV (quasi peak) 74 dBµV (average)

29.14.13 RADIATED EMISSIONS

Compliance	IEC 60255-26:2013
Test 1	30 - 230 MHz, 40 dBµV/m at 10 m measurement distance
Test 2	230 - 1 GHz, 47 dBµV/m at 10 m measurement distance
Test 3	1 - 2 GHz, 76 dBµV/m at 10 m measurement distance

29.14.14 POWER FREQUENCY

Compliance	IEC 60255-26:2013
Opto-inputs (compliance is achieved using the opto-input filter)	300 V common-mode (Class A) 150 V differential mode (Class A)

Note:
Compliance is achieved using the opto-input filter.

APPENDIX A

ORDERING OPTIONS

Ordering Information

CORTEC Order Code Matrix		1-3	4	5	6	7	8	9	10	11	12-14	15
Current Differential with Distance and Autoreclose/Check Synchronising		P54									**	
Single Breaker Application			3									
Breaker and a Half or Dual Breaker Appplication			6									
Nominal Auxiliary Supply Voltage												
24-54 Vdc				7								
48-125 Vdc (40-100 Vac)				8								
110-250 Vdc (100-240 Vac)				9								
CT and VT Ratings	Hardware Options Compatibility											
In = 1A/5A ; Vn = 100-120Vac	All				1							
IEC 61850-9-2LE Redundant Sampled Analogue Values Ethernet - process bus model *	Options U, V, W & Y only				C							
Hardware Options												
Standard - 1 x RS485 rear serial communications port provided with all ordering options (Courier, -103, DNP3 ready)						1						
With additional IRIG-B (Modulated)						2						
With additional IRIG-B (Modulated) & Serial Fibre Optic comms						4						
Single Ethernet 1 LC Duplex port + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						U						
Redundant Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex port + IEC870-103 Serial Fibre ST ports + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						V						
Redundant Ethernet PRP/HSR/RSTP/Failover 2 RJ45 + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						W						
Redundant Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex ports + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						Y						
Input/Output Options	Case Size Compatibility											
8 inputs, 7 outputs	40TE, 60TE						A					
8 inputs, 8 outputs	40TE, 60TE						B					
8 inputs, 14 outputs	60TE						C					
12 inputs, 11 outputs **	60TE						D					
12 inputs, 12 outputs	60TE						E					
16 inputs, 7 outputs **	60TE						F					
16 inputs, 14 outputs	60TE						G					
16 inputs, 16 outputs	60TE						H					
16 inputs, 16 outputs + 4 High-Speed High-Break	P543 only 60TE, 80TE						J					
16 inputs, 21 outputs	P543 only 60TE, 80TE						K					
16 inputs, 24 outputs	P543 only 60TE, 80TE						L					
20 inputs, 20 outputs **	P543 only 60TE, 80TE						P					
24 inputs, 8 outputs **	60TE						Q					
24 inputs, 14 outputs **	P543 only 60TE, 80TE						R					
24 inputs, 16 outputs **	P543 only 60TE, 80TE						S					
24 inputs, 16 outputs + 8 High-Speed High-Break	80TE						T					
24 inputs, 24 outputs **	80TE						U					
24 inputs, 32 outputs	80TE						V					
28 inputs, 43 outputs	P543 only - 80TE						Y					
32 inputs, 14 outputs **	80TE						Z					
32 inputs, 24 outputs **	80TE						1					
32 inputs, 32 outputs	P543 only - 80TE						2					
40 inputs, 24 outputs	P543 only - 80TE						4					
40 inputs, 32 outputs **	P543 only - 80TE						5					
48 inputs, 16 outputs **	P543 only - 80TE						7					
Line Differential Channel Options												
Ch1=850nm multi-mode, Ch2=850nm multi-mode								A				
Ch1=1300nm single-mode, Ch2=not fitted (2 Terminal only)								B				
Ch1=1300nm single-mode, Ch2=1300nm single-mode								C				
Ch1=1300nm multi-mode, Ch2=not fitted (2 Terminal only)								D				
Ch1=1300nm multi-mode, Ch2=1300nm multi-mode								E				
Ch1=1550nm single-mode, Ch2=not fitted (2 Terminal only)								F				
Ch1=1550nm single-mode, Ch2=1550nm single-mode								G				
Ch1=850nm multi-mode, Ch2=1300nm single-mode								H				
Ch1=850nm multi-mode, Ch2=1300nm multi-mode								J				
Ch1=850nm multi-mode, Ch2=1550nm single-mode								K				
Case Size and Mounting	Product Compatibility											
80TE Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P543, P546								S			
80TE Case - 19" Rack Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P543, P546								T			
40TE Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port, without Function Keys	P543. P546 with IEC 61850-9-2LE								U			
60TE Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P543, P546								V			
Product Features												
Subtransmission/Distribution Distance Protection, 3 Pole Tripping Only										A		
Subcycle Transmission Distance										B		
Multi Ended Differential Plus SubCycle Distance										M		
Software Version												
Major Version - please visit On-Line Store to select											**	
Customer-Specific Additions												
Standard version												0
Customer-specific configuration/options												A
Hardware Version												
5th Generation Hardware, Graphical Colour HMI with High Performance Processing												Q

APPENDIX B

SETTINGS AND SIGNALS

Tables containing a full list of settings for each model are provided in a separate Excel file, attached as an embedded resource. If using Adobe Acrobat Reader, click on the button below to open the spreadsheet.

This manual must be opened with a PDF viewer capable of opening attachments, such as Adobe Acrobat Reader or Nitro PDF. If using Nitro PDF, attachments are shown in the attachment pane. To show or hide the attachments pane, look in the sidebar and click the attachments tab.

Note:
An Open File dialogue box may open with a warning message about potential harm from programs, macros or viruses. The file supplied does not contain any harmful content, and may be safely opened.

Settings and Signals

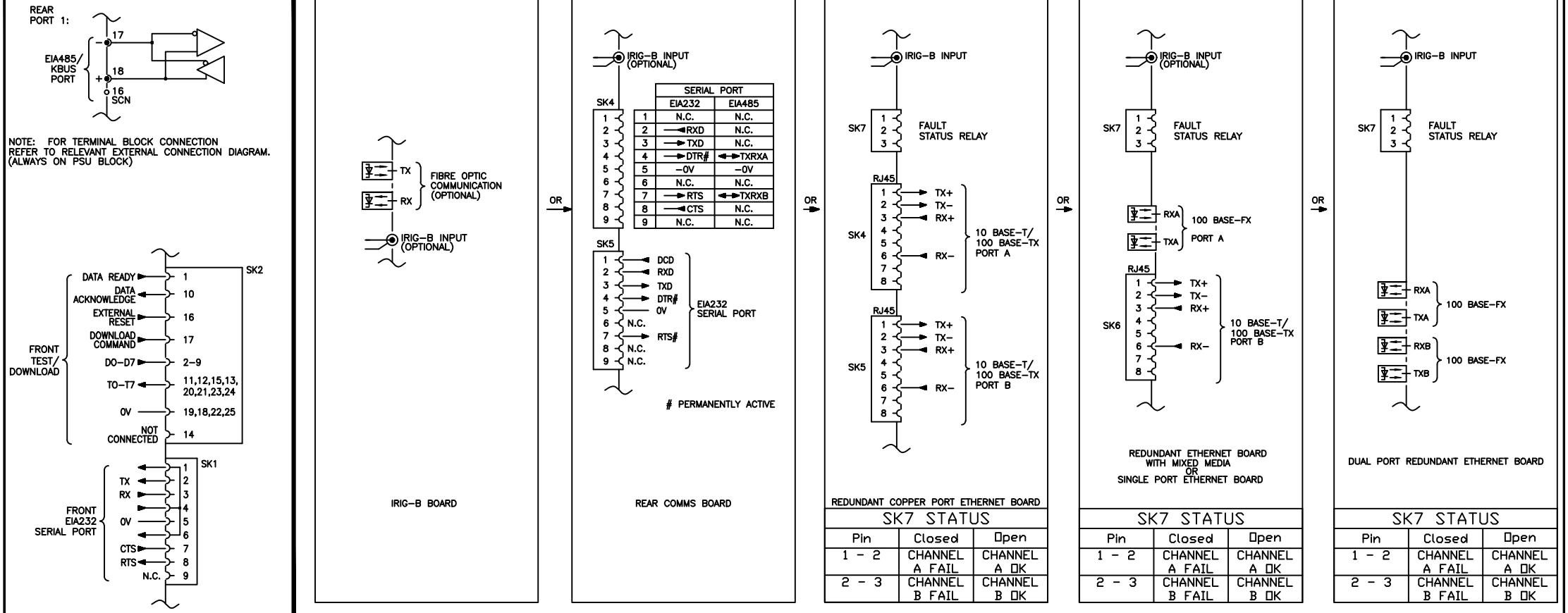
APPENDIX C

WIRING DIAGRAMS

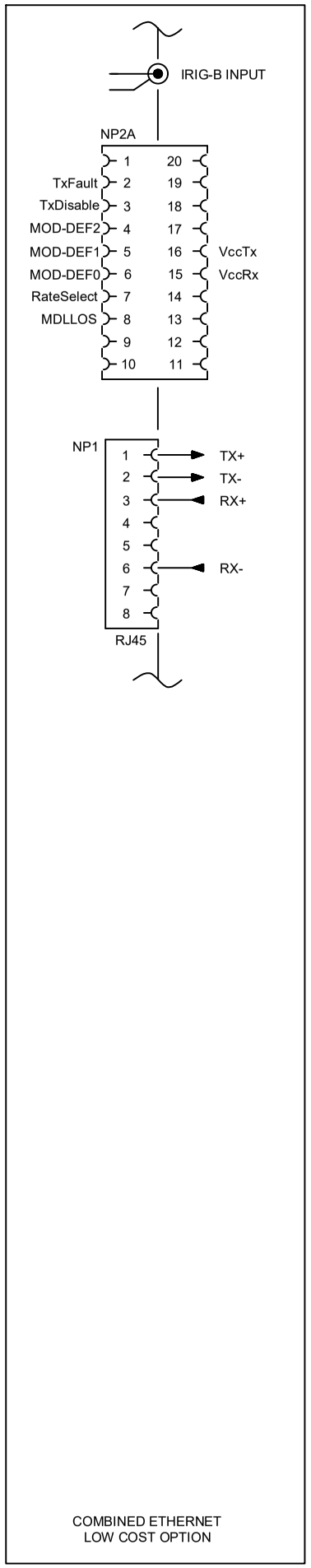
Model	CORTEC Option*	Input/Output Options and Case Size Compatibility	Drawing-Sheet	Issue
All	-	Comms Options MiCOM Px40 Platform	10Px4001-1 10Px4001-2	N B
P543	I/O Option A	8 Inputs, 7 Outputs (40TE)	10P54322-1	D
		(60TE)	10P54313-1	B
	I/O Option B	8 Inputs, 8 Outputs (40TE)	10P54323-1	D
		(60TE)	10P54314-1	B
	I/O Option C	8 Inputs, 14 Outputs (60TE)	10P54315-1	B
	I/O Option E	12 Inputs, 12 Outputs (60TE)	10P54316-1	C
	I/O Option G	16 Inputs, 14 Outputs (60TE)	10P54317-1	C
	I/O Option H	16 Inputs, 16 Outputs (60TE)	10P54318-1	B
	I/O Option J	16 Inputs, 16 Outputs + 4 High-Speed High-Break (60TE)	10P54319-1	B
		(80TE)	10P54306-1	C
	I/O Option K	16 Inputs, 21 Outputs (60TE)	10P54320-1	B
		(80TE)	10P54307-1	B
	I/O Option L	16 Inputs, 24 Outputs (60TE)	10P54321-1	B
		(80TE)	10P54308-1	B
	I/O Option P	20 Inputs, 20 Outputs (60TE)	10P54368-1	B
		(80TE)	10P54358-1	B
	I/O Option S	24 Inputs, 16 Outputs (60TE)	10P54371-1	B
		(80TE)	10P54360-1	B
	I/O Option T	24 Inputs, 16 Outputs + 8 High-Speed High-Break (80TE)	10P54309-1	B
		(80TE)	10P54336-1	B
	I/O Option U	24 Inputs, 24 Outputs (80TE)	10P54361-1	B
	I/O Option V	24 Inputs, 32 Outputs (80TE)	10P54310-1	B
	I/O Option Y	28 Inputs, 43 Outputs (80TE)	10P54341-1	B
	I/O Option 1	32 Inputs, 24 Outputs (80TE)	10P54363-1	B
	I/O Option 2	32 Inputs, 32 Outputs (80TE)	10P54311-1	B
	I/O Option 4	40 Inputs, 24 Outputs (80TE)	10P54312-1	B
	I/O Option 5	40 Inputs, 32 Outputs (80TE)	10P54364-1	B
P546	-	P546 Current Differential Power System Connections only (80TE)	10P54600-1 10P54600-2 10P54600-3 10P54600-4	G E A A
	I/O Option A	8 Inputs, 7 Outputs (60TE)	10P54616-1	C
	I/O Option B	8 Inputs, 8 Outputs (60TE)	10P54617-1	C
	I/O Option C	8 Inputs, 14 Outputs (60TE)	10P54618-1	C
	I/O Option E	12 Inputs, 12 Outputs (60TE)	10P54619-1	C
	I/O Option G	16 Inputs, 14 Outputs (60TE)	10P54620-1	C
	I/O Option H	16 Inputs, 16 Outputs (60TE)	10P54621-1	C
	I/O Option J	16 Inputs, 16 Outputs + 4 High-Speed High-Break (80TE)	10P54611-1	B
	I/O Option K	16 Inputs, 21 Outputs (80TE)	10P54612-1	C
	I/O Option L	16 Inputs, 24 Outputs (80TE)	10P54613-1	B

Model	CORTEC Option*	Input/Output Options and Case Size Compatibility	Drawing-Sheet	Issue
P546	I/O Option P	20 Inputs, 20 Outputs (80TE)	10P54658-1	B
	I/O Option S	24 Inputs, 16 Outputs (80TE)	10P54660-1	B
	I/O Option T	24 Inputs, 16 Outputs + 8 High-Speed High-Break (80TE)	10P54614-1	B
	I/O Option U	24 Inputs, 24 Outputs (80TE)	10P54661-1	B
	I/O Option V	24 Inputs, 32 Outputs (80TE)	10P54615-1	B
	I/O Option 1	32 Inputs, 24 Outputs (80TE)	10P54663-1	B

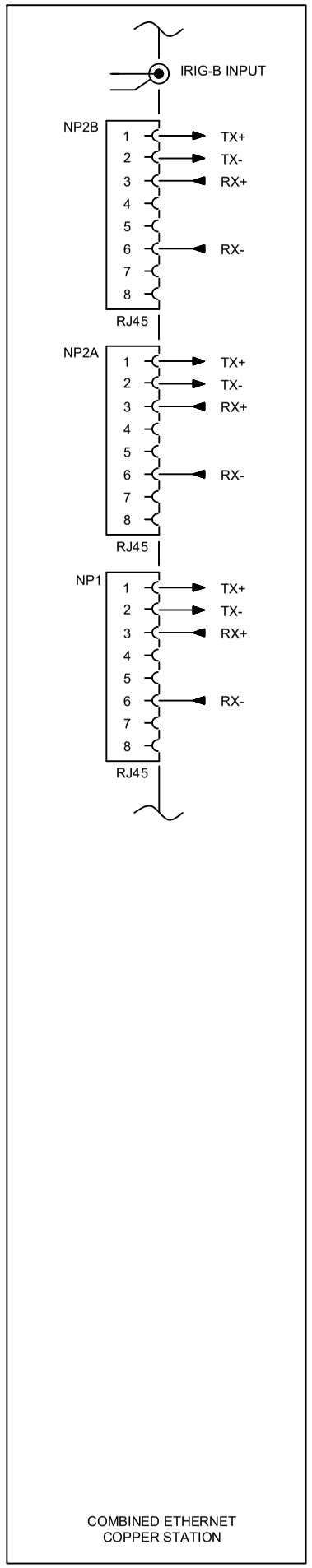
* When selecting the applicable wiring diagram(s), refer to the appropriate model CORTEC.



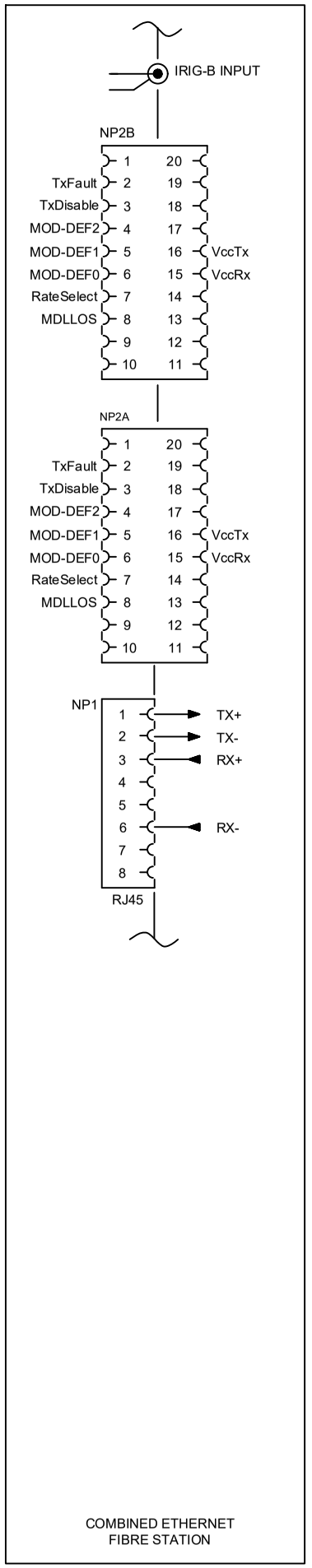
Issue: N	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM: COMMS OPTIONS MICOM Px40 PLATFORM		
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10PX4001**	PLM No: A20022917	Sht: 1 / Next Sht: 2
Date:	Chkd:				GE VERNOVA



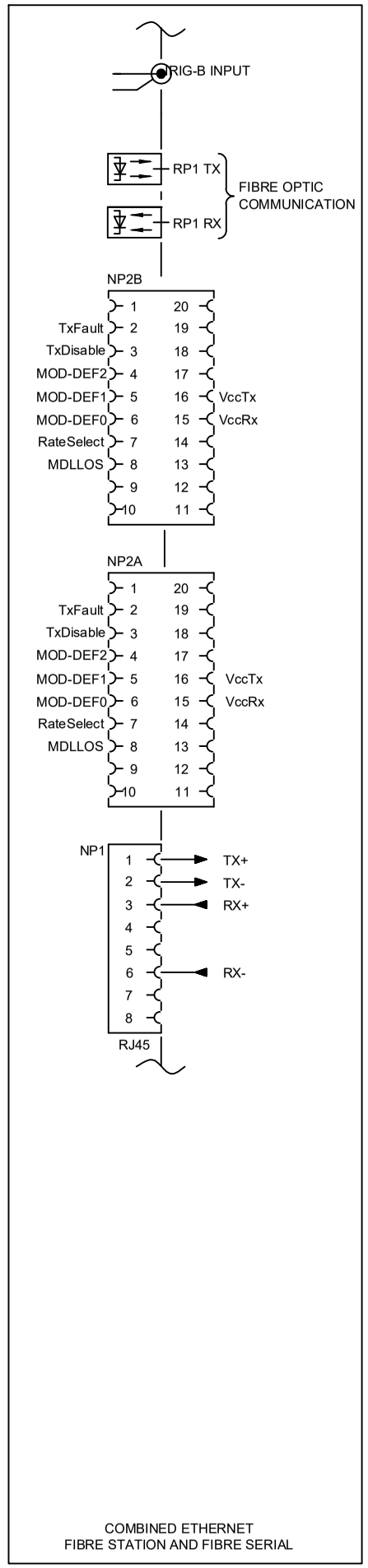
COMBINED ETHERNET
LOW COST OPTION



COMBINED ETHERNET
COPPER STATION

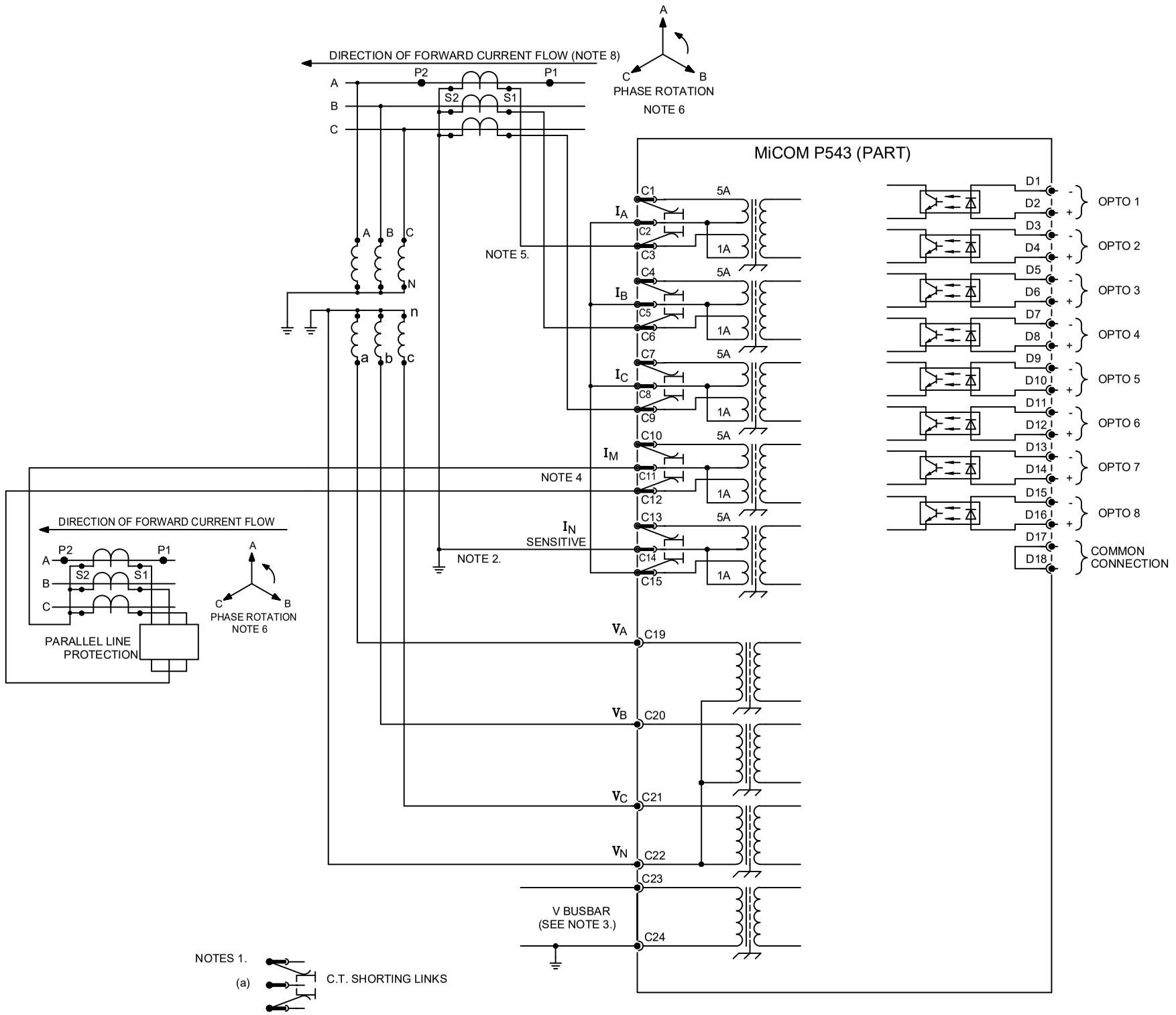


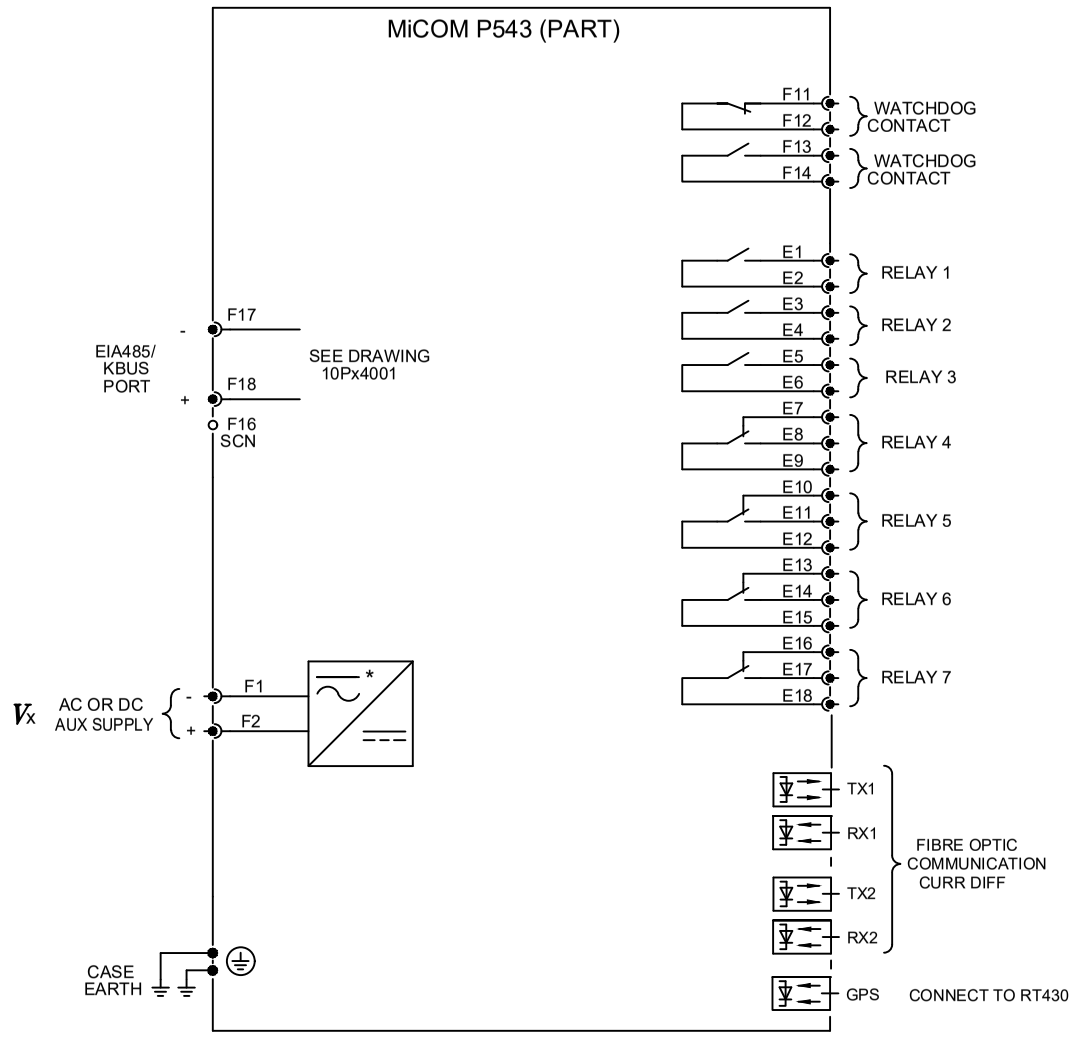
COMBINED ETHERNET
FIBRE STATION



COMBINED ETHERNET
FIBRE STATION AND FIBRE SERIAL

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM COMMS OPTIONS MICOM Px40			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10PX4001**	PLM No: A20095995	Sht: 2 Next Sht: -	GE VERNOVA
Date:	Chkd:					





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

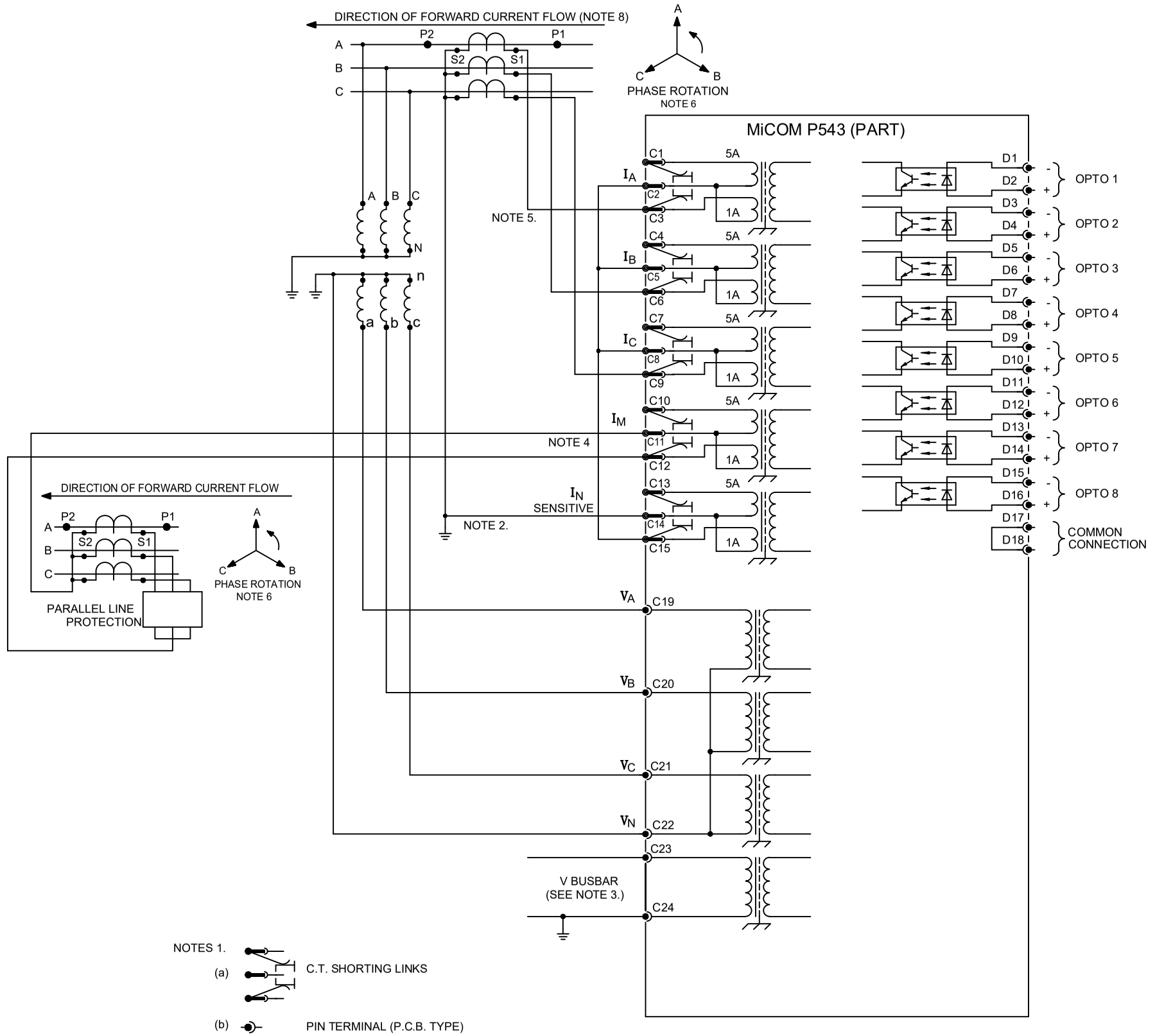
(b) PIN TERMINAL (P.C.B. TYPE)

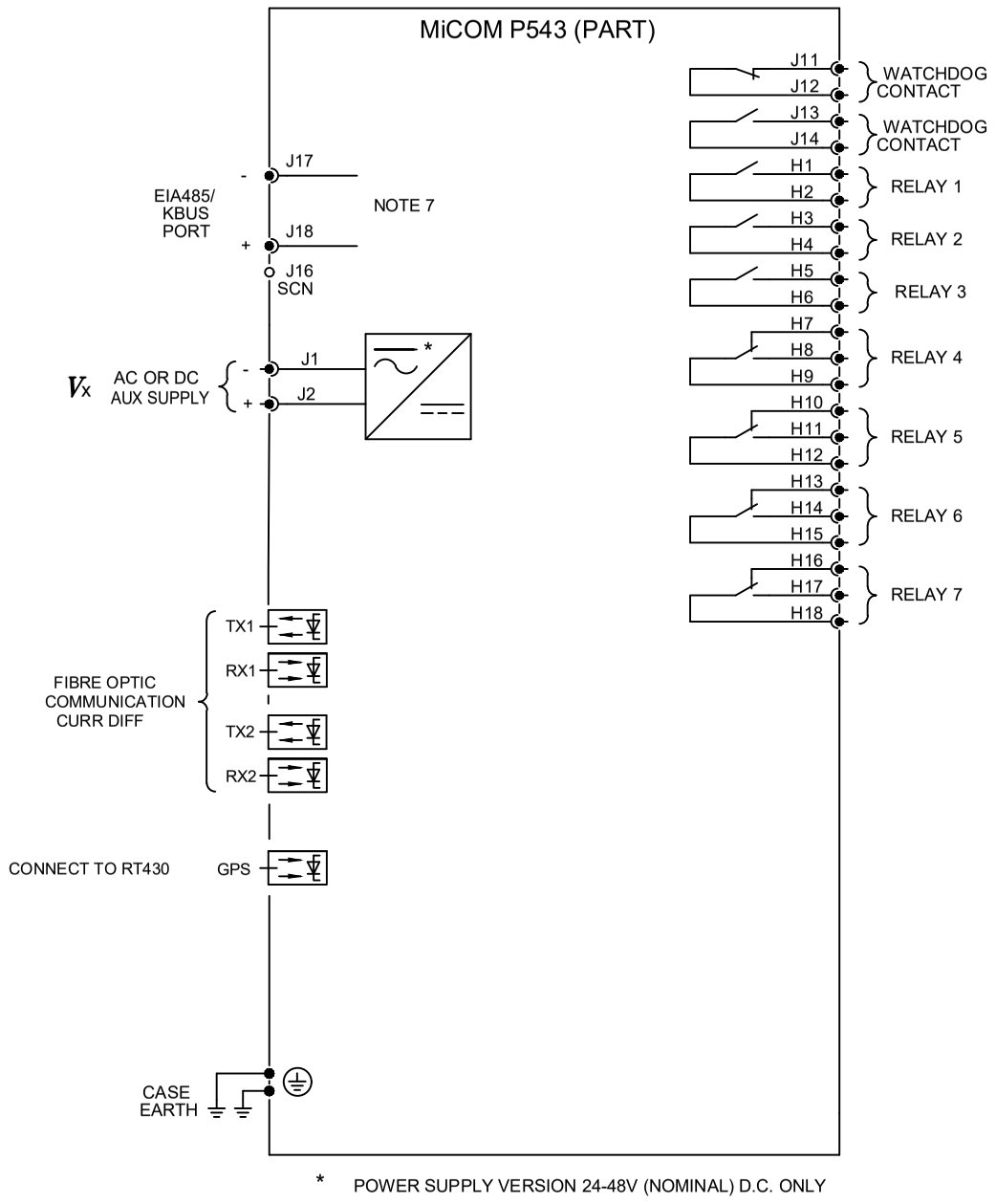
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: D	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (40TE) 8I/7O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54322**	PLM No: A20076557	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

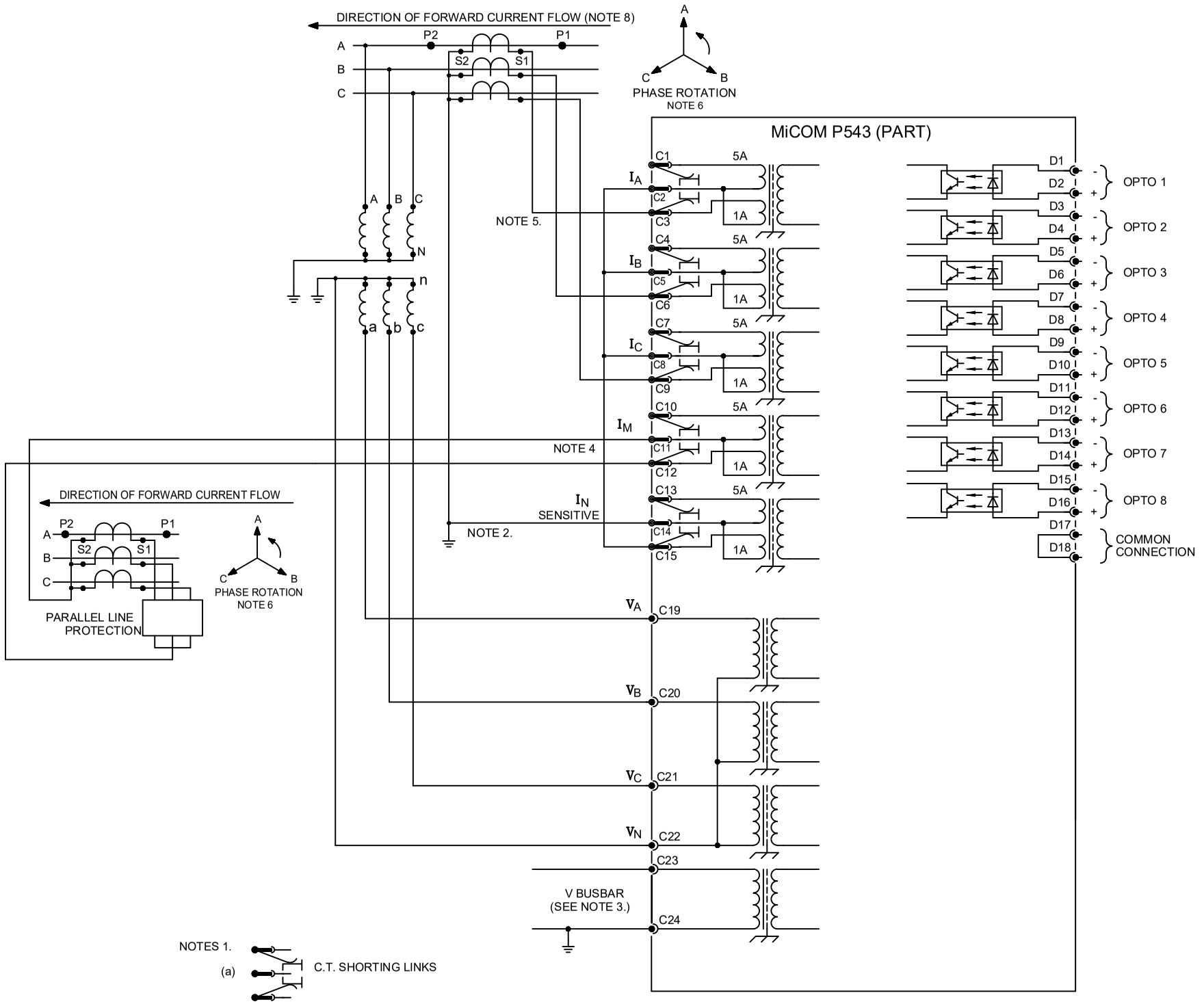
(b) PIN TERMINAL (P.C.B. TYPE)

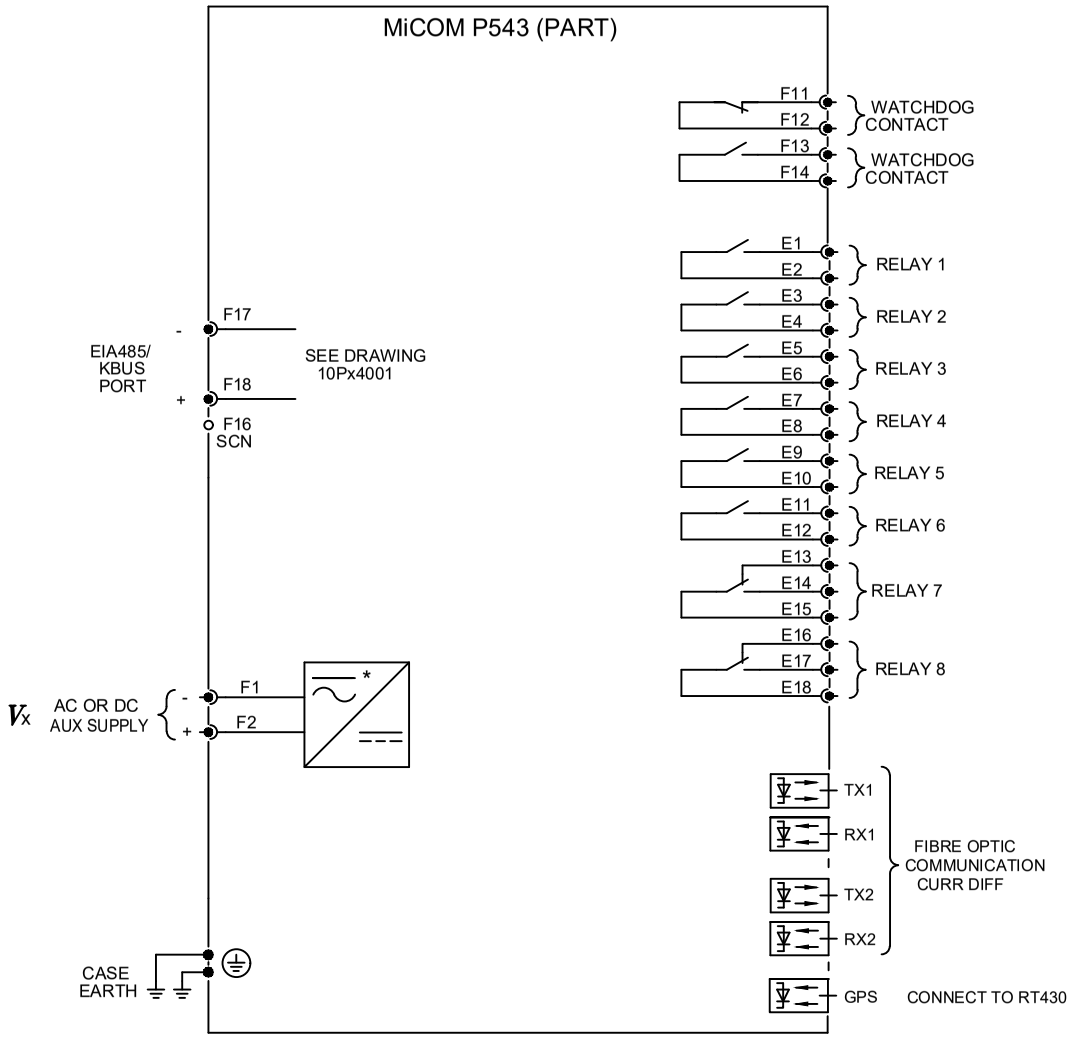
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 8I/7O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54313**	PLM No: A20076535	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

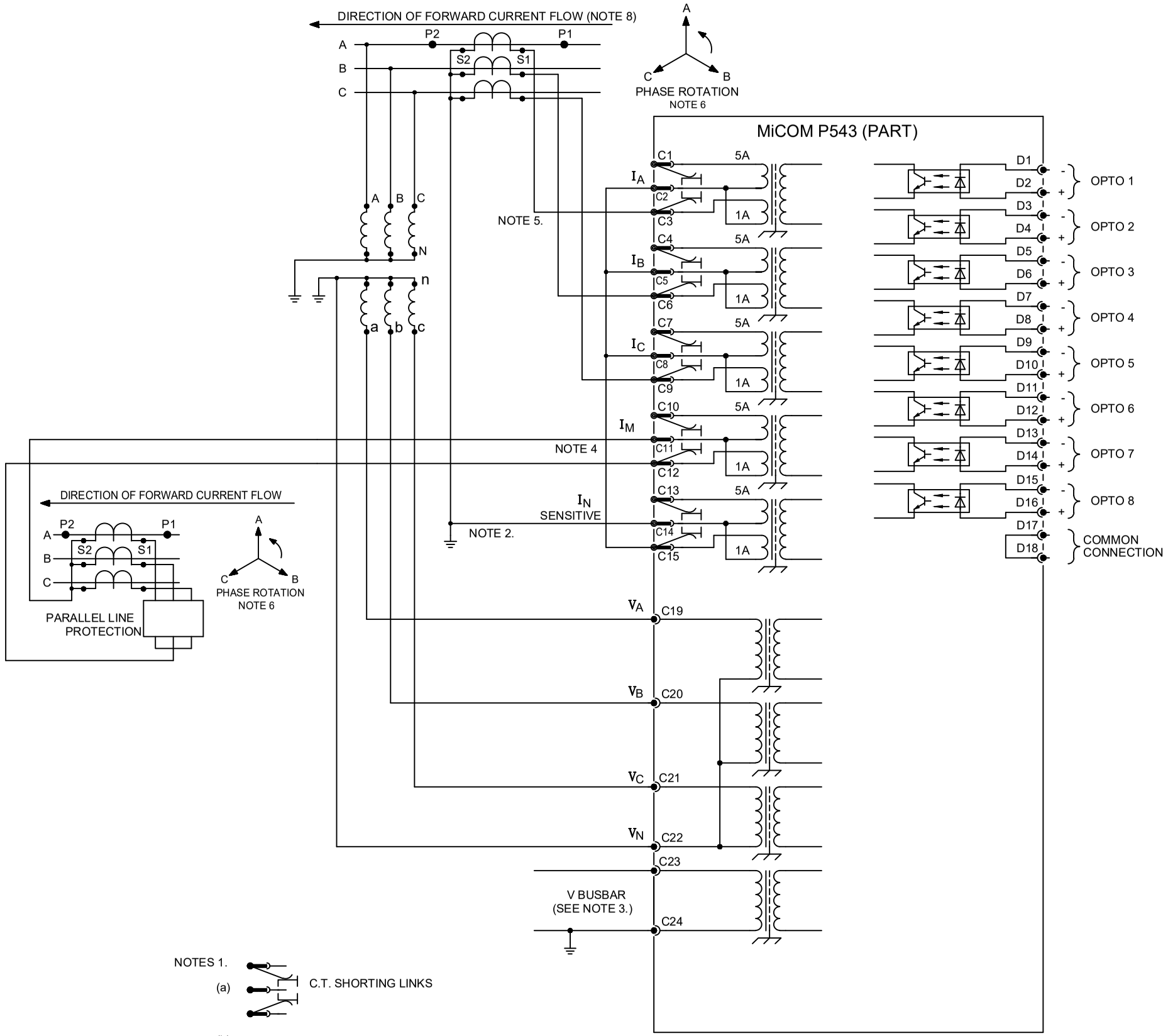
(b) PIN TERMINAL (P.C.B. TYPE)

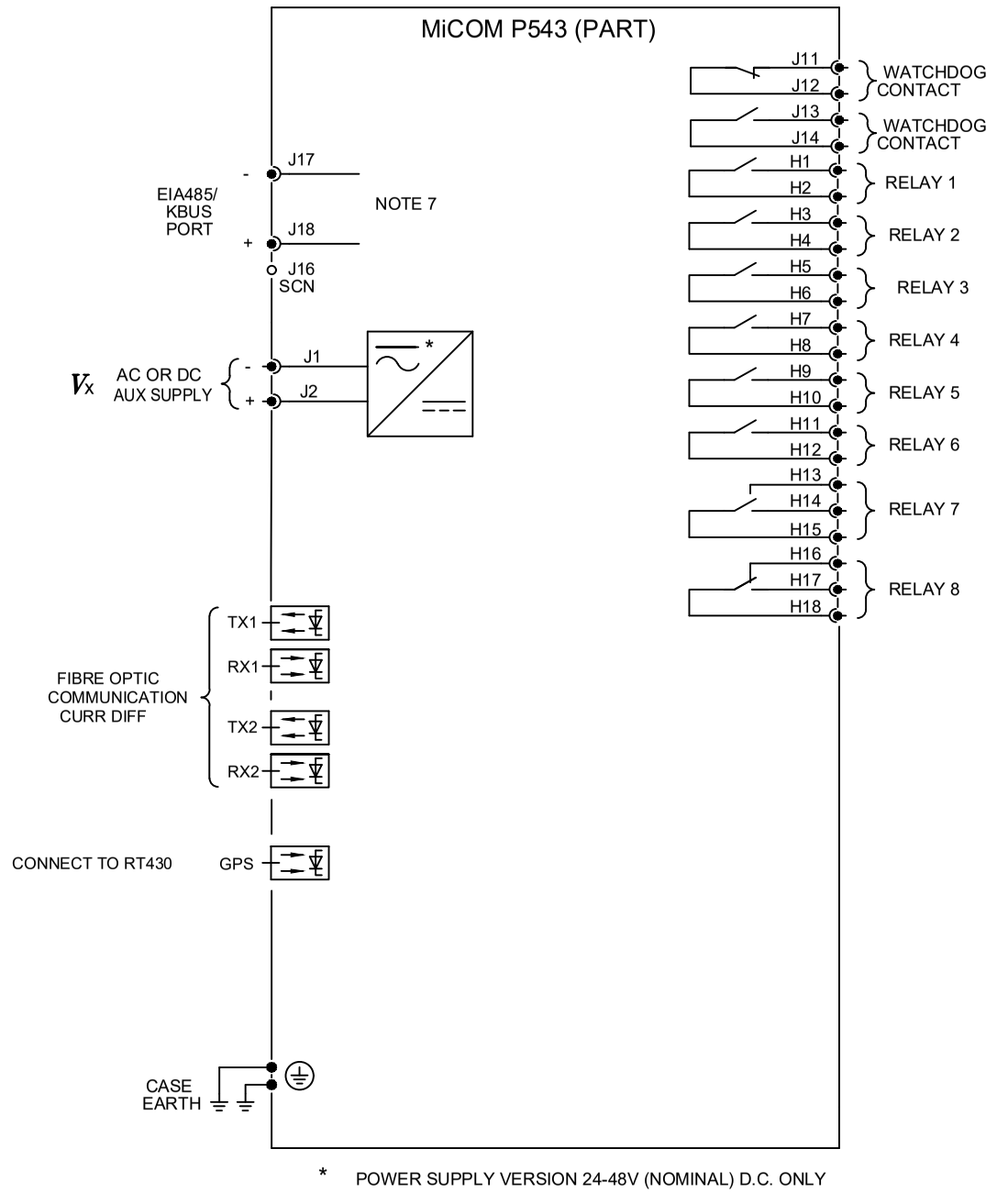
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: D	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (40TE) 8I/8O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54323**	PLM No: A20076558	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

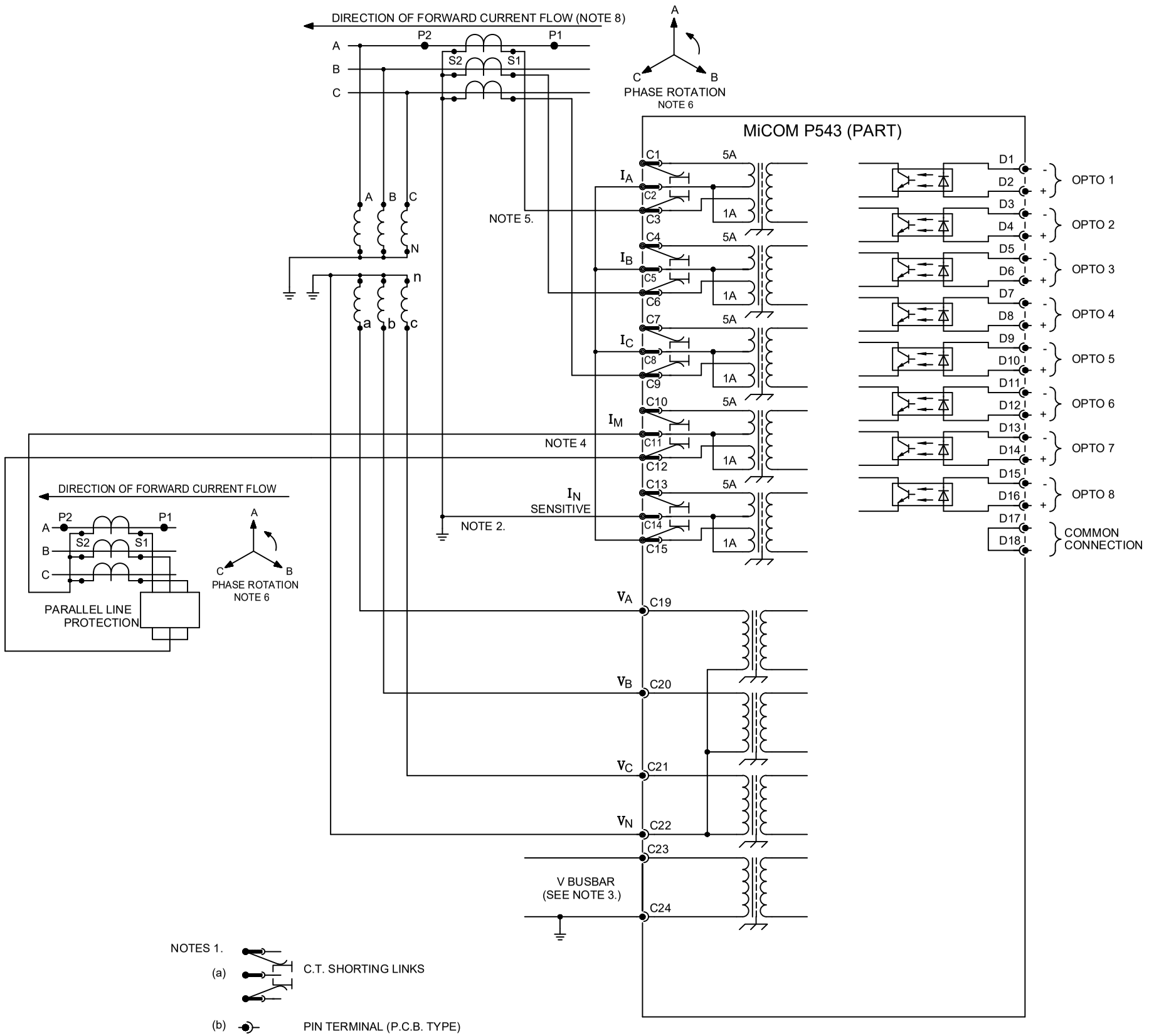
(b) PIN TERMINAL (P.C.B. TYPE)

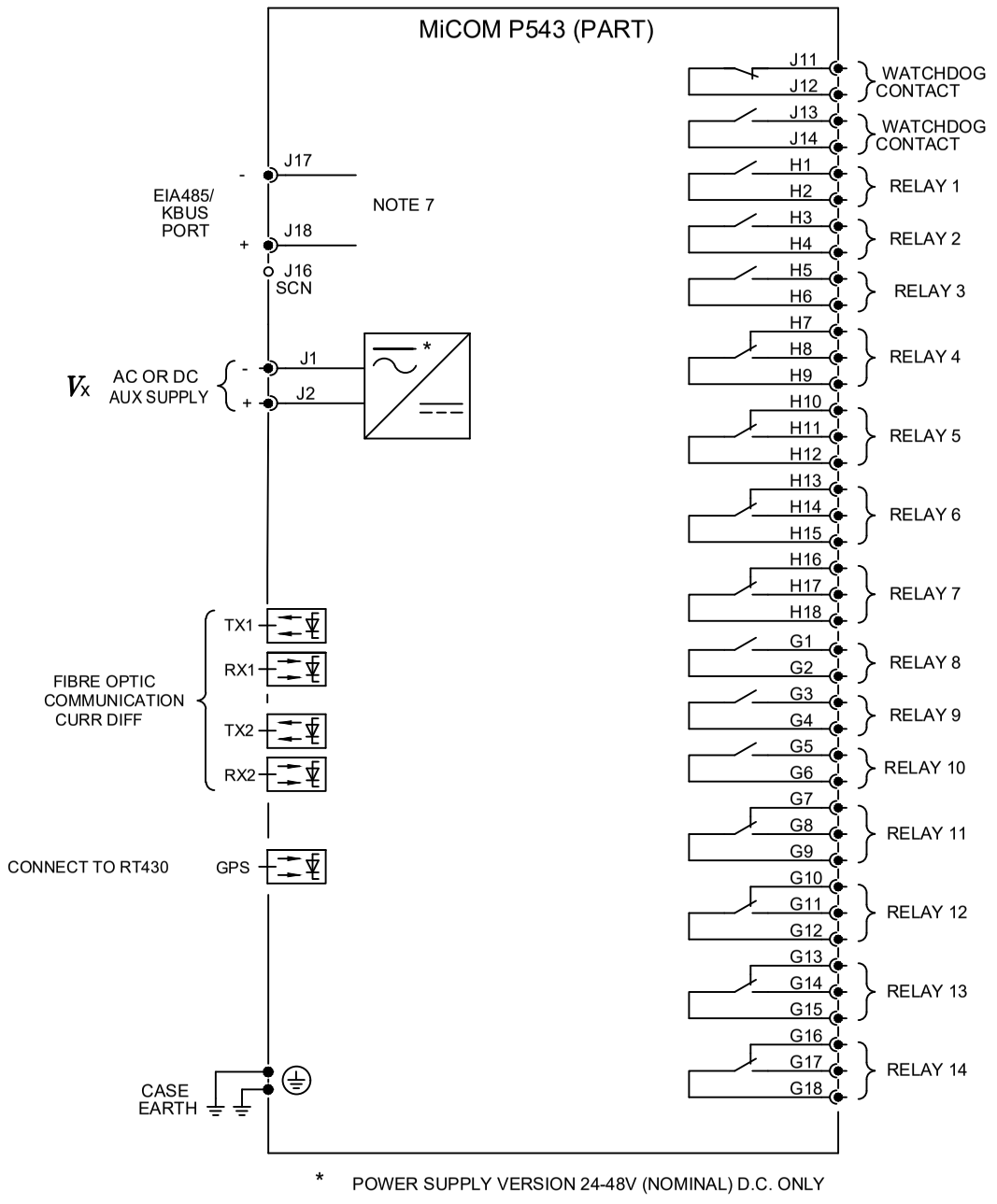
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 8I/8O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54314**	PLM No: A20076536	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

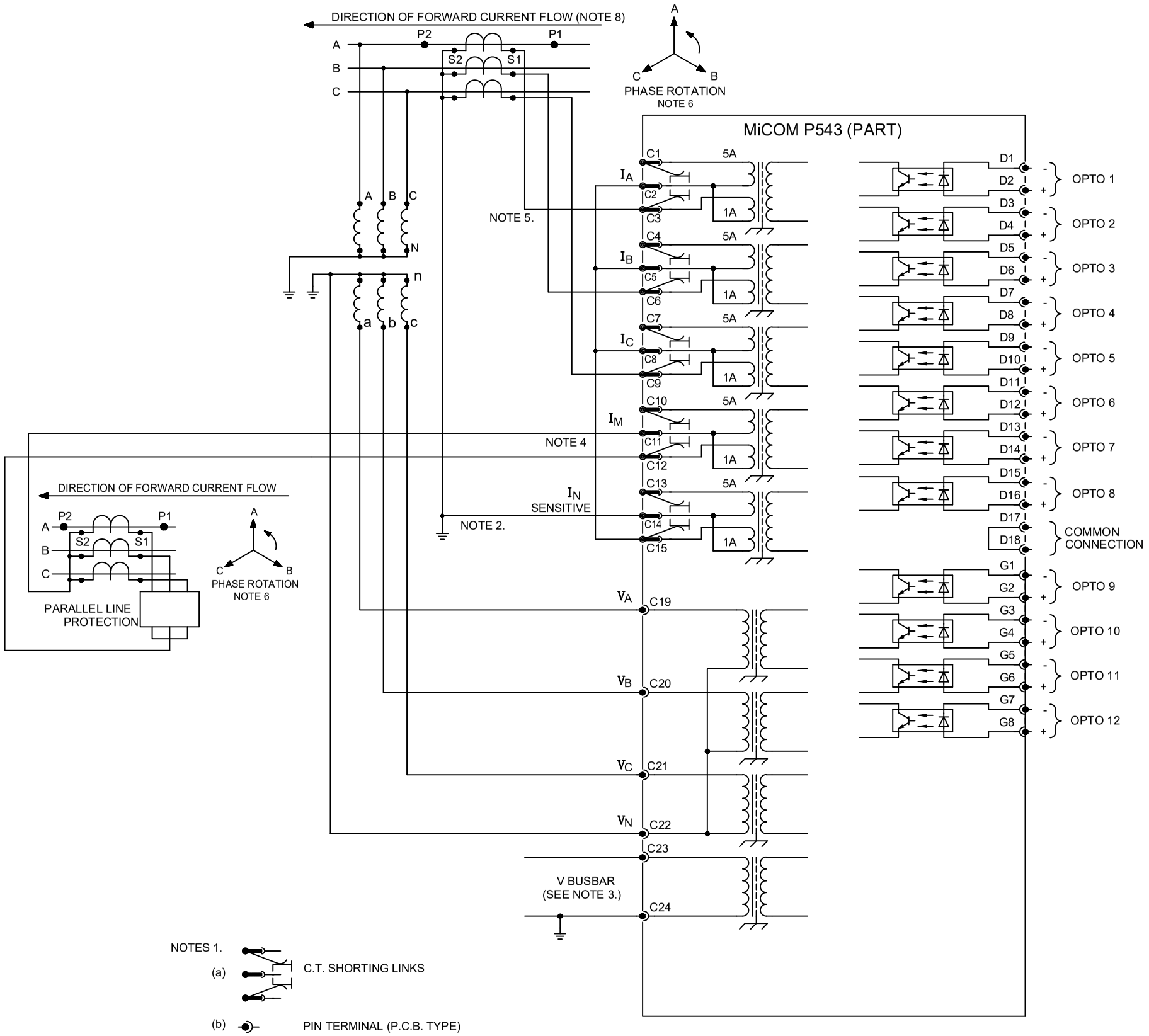
(b) PIN TERMINAL (P.C.B. TYPE)

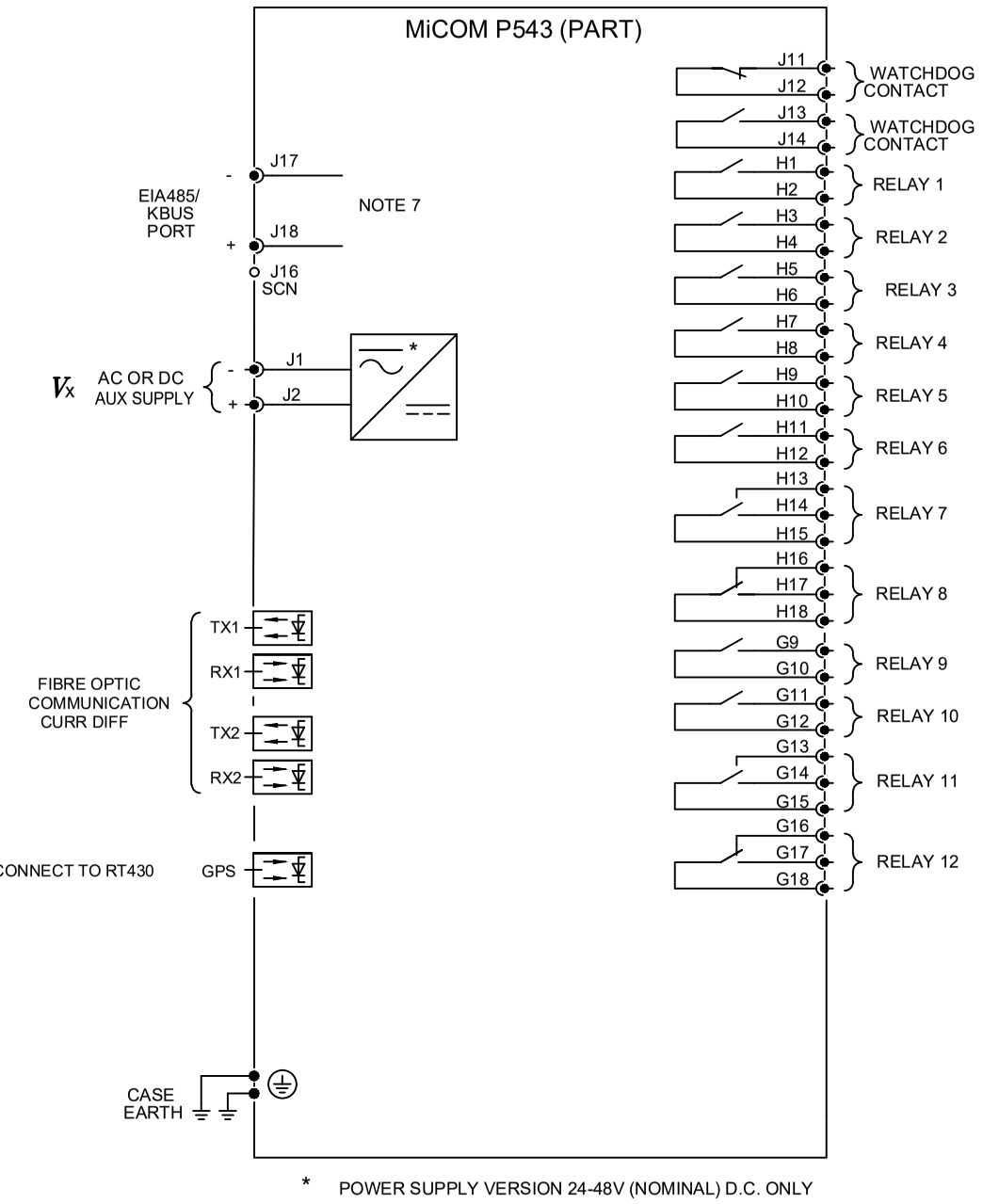
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 8I/14O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54315**	PLM No: A20076537	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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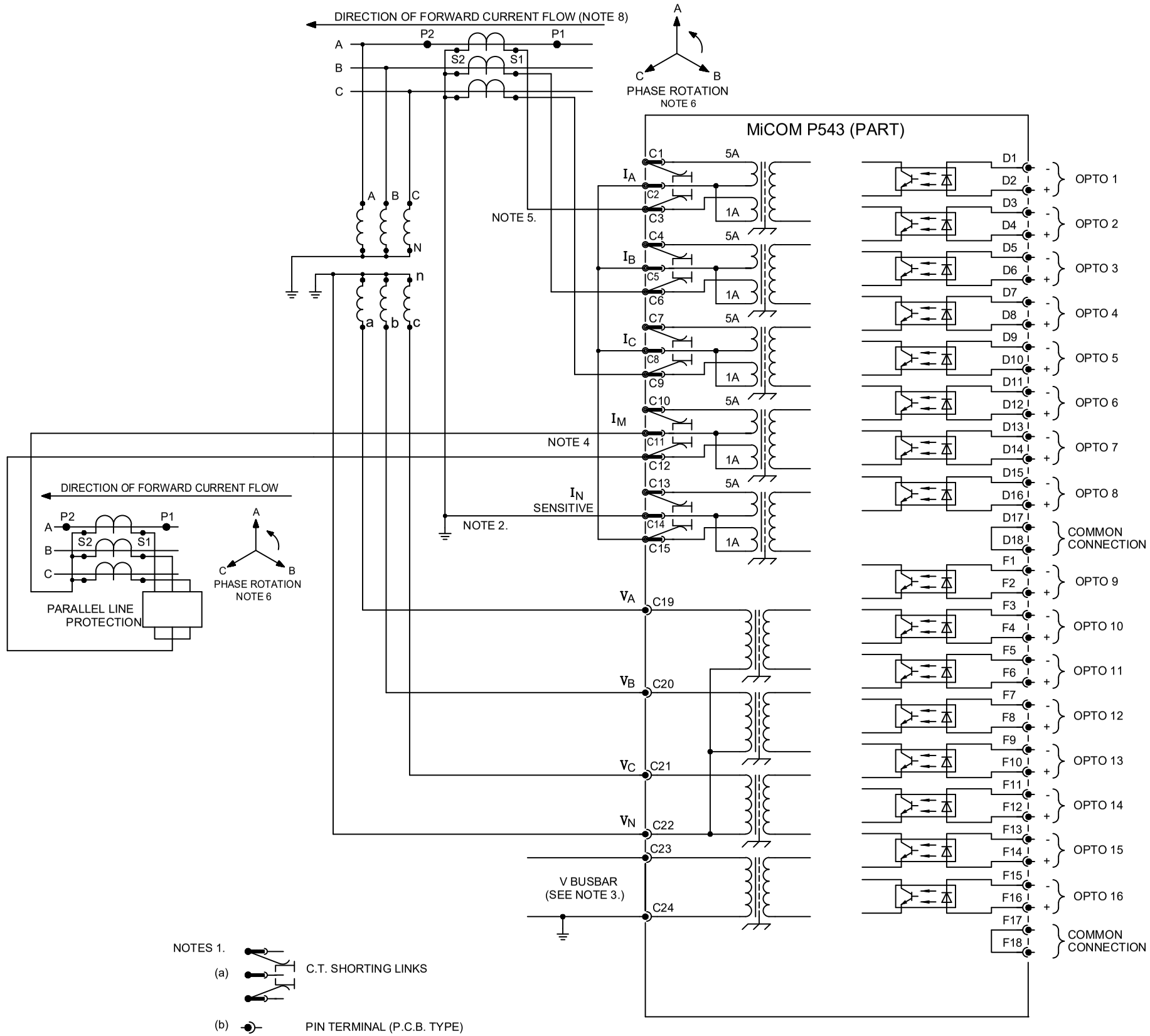
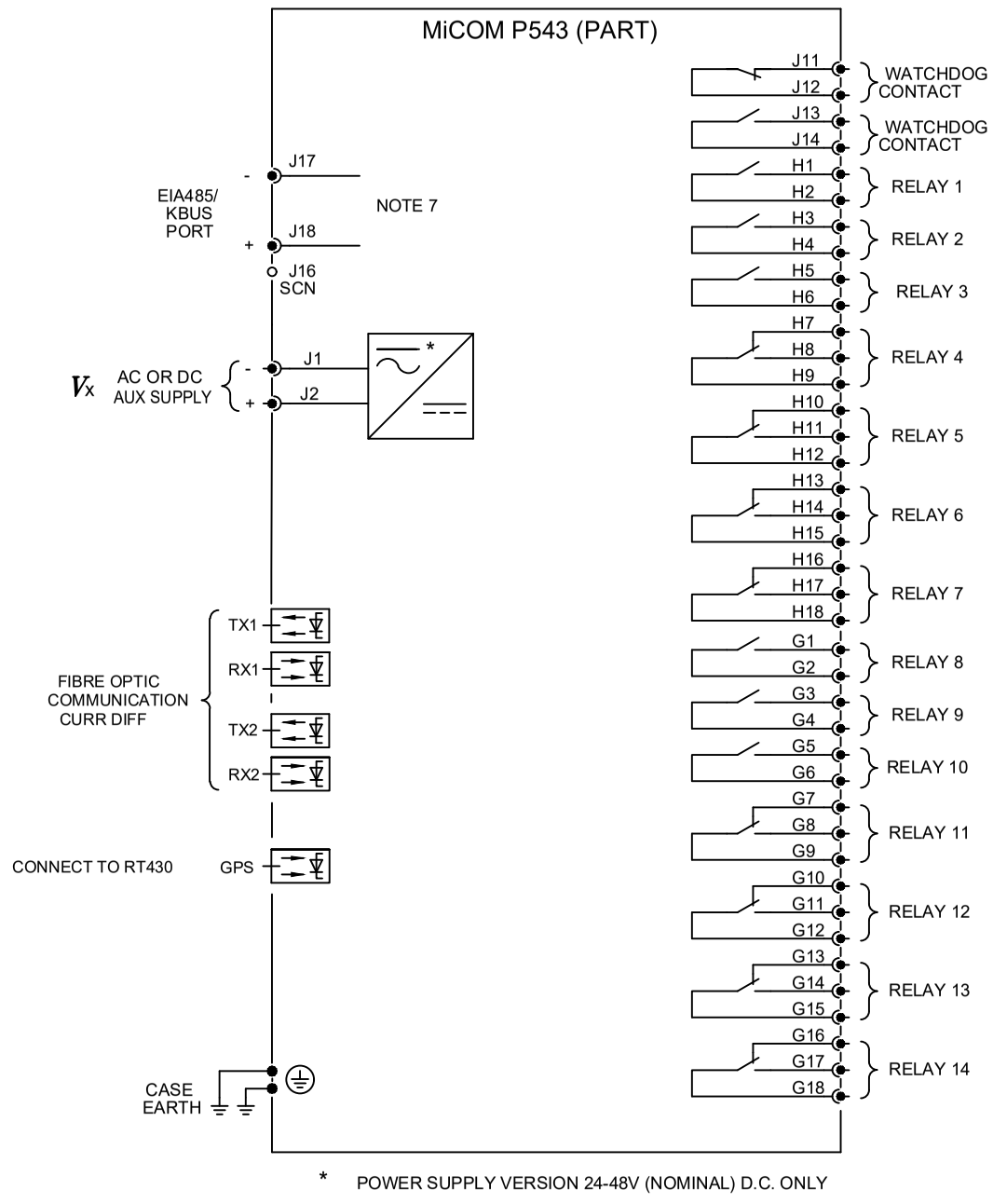
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: C	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 12I/12O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54316**	PLM No: A20076538	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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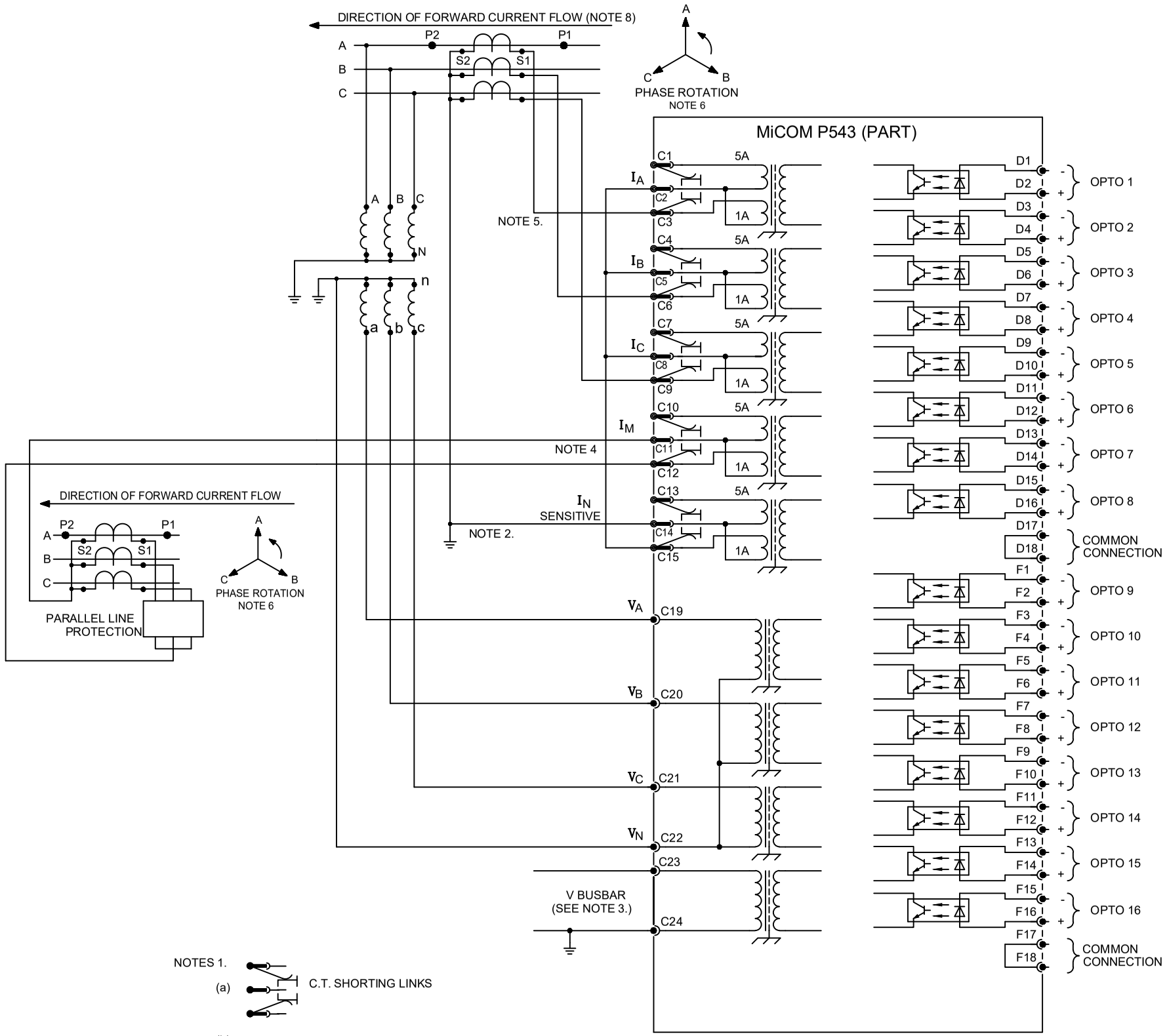
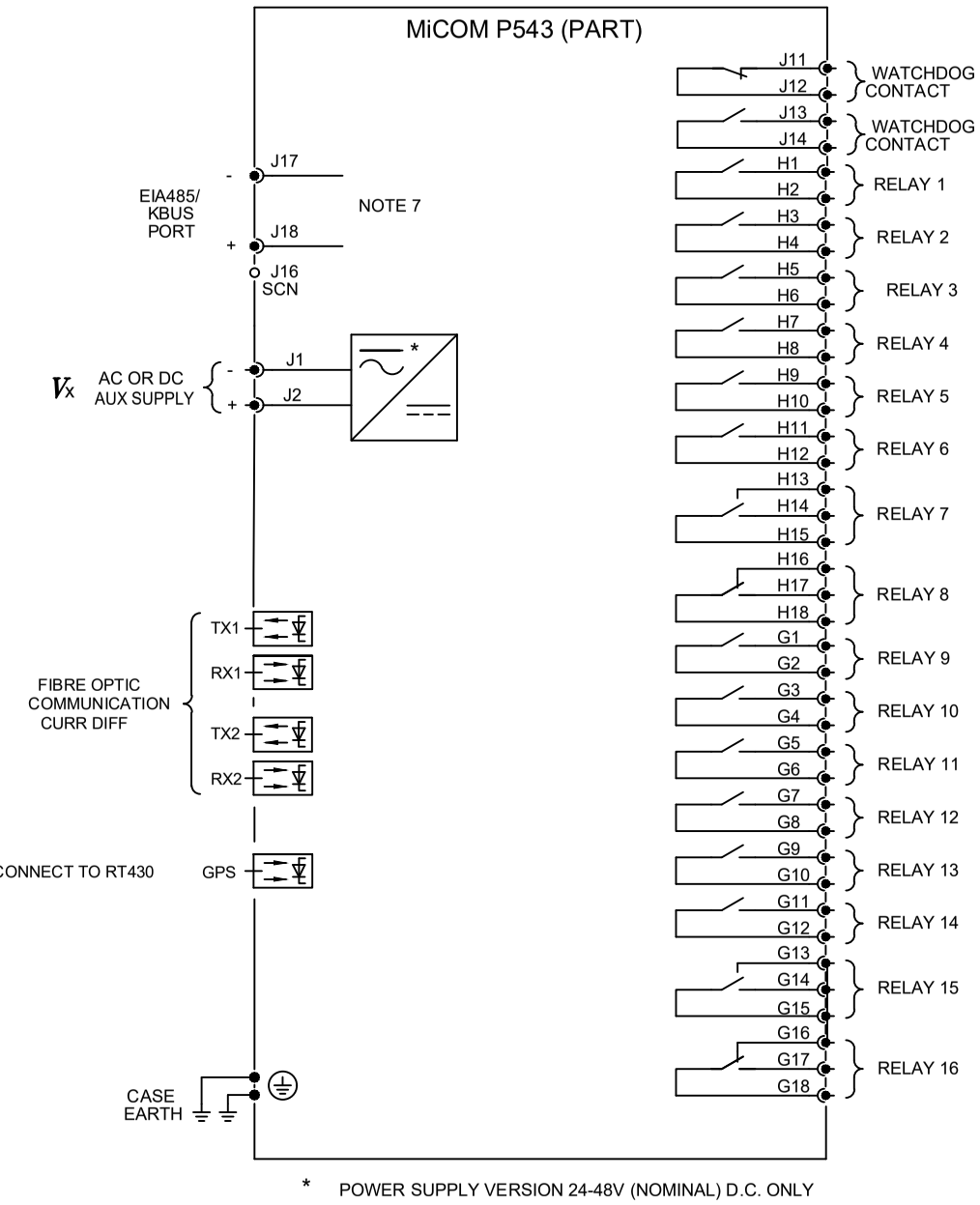
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: C	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 16I/14O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54317**	PLM No: A20076539	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.

3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.

4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.

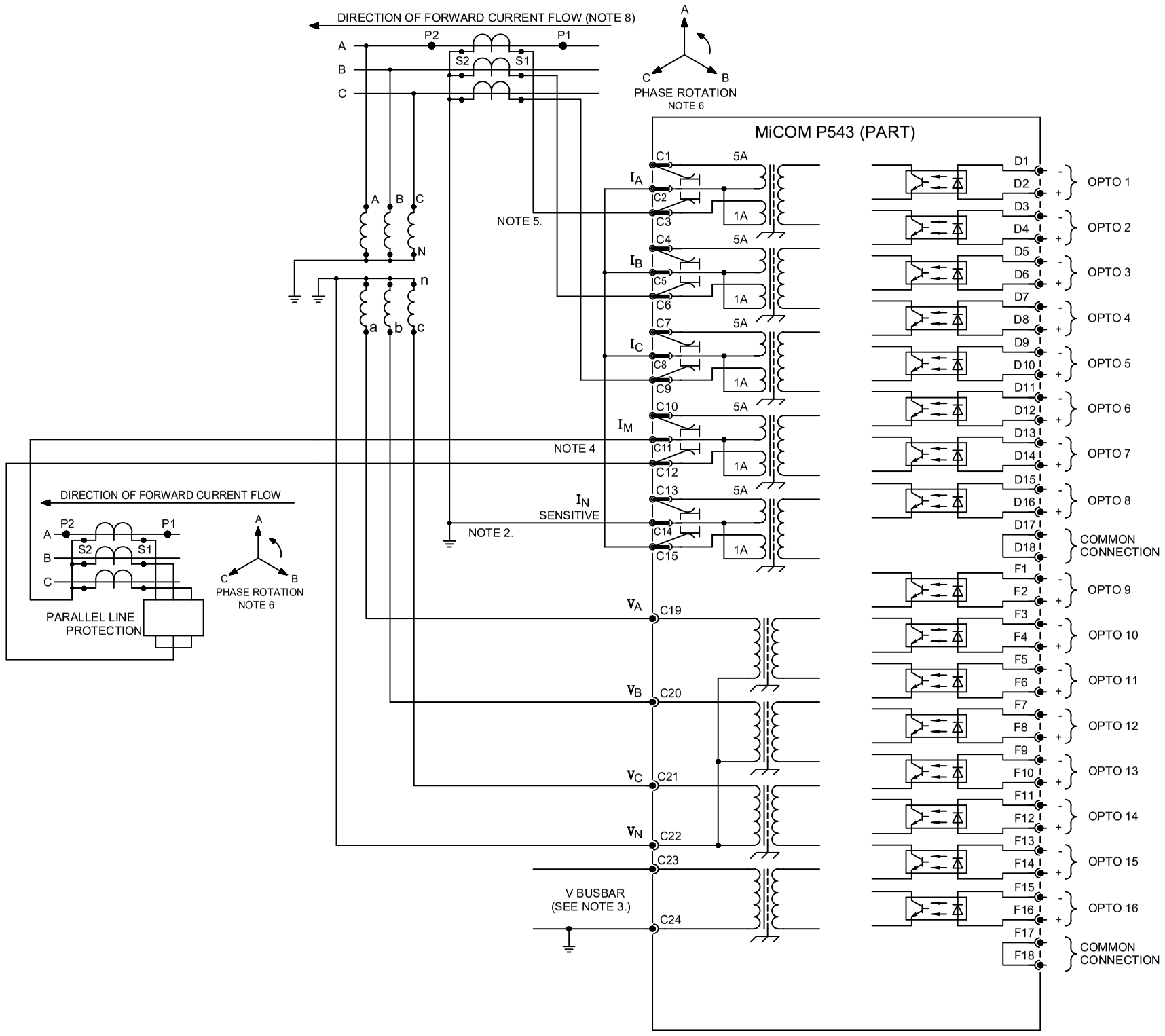
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.

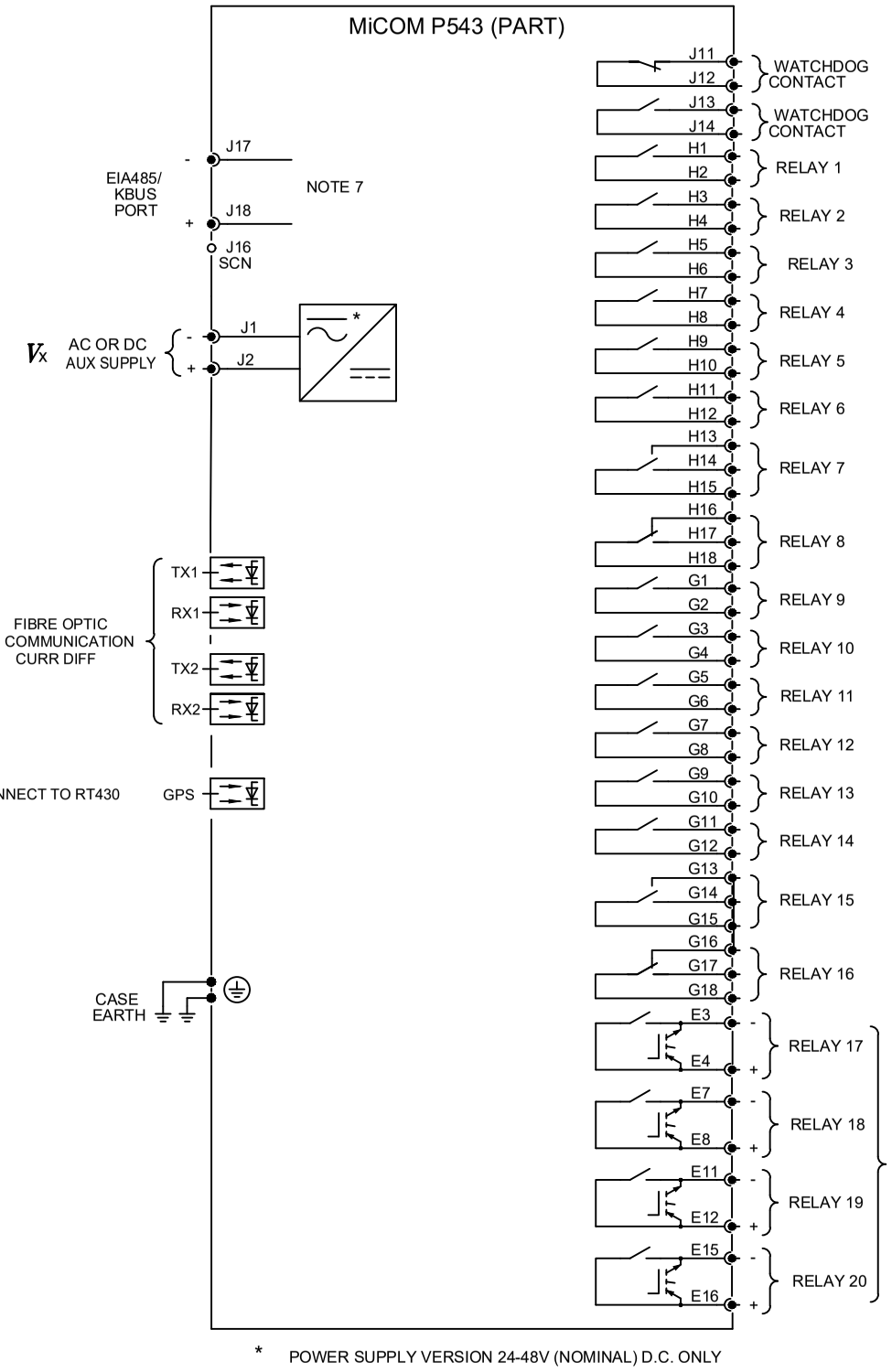
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED

7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 16I/16O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54318**	PLM No: A20076540	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.

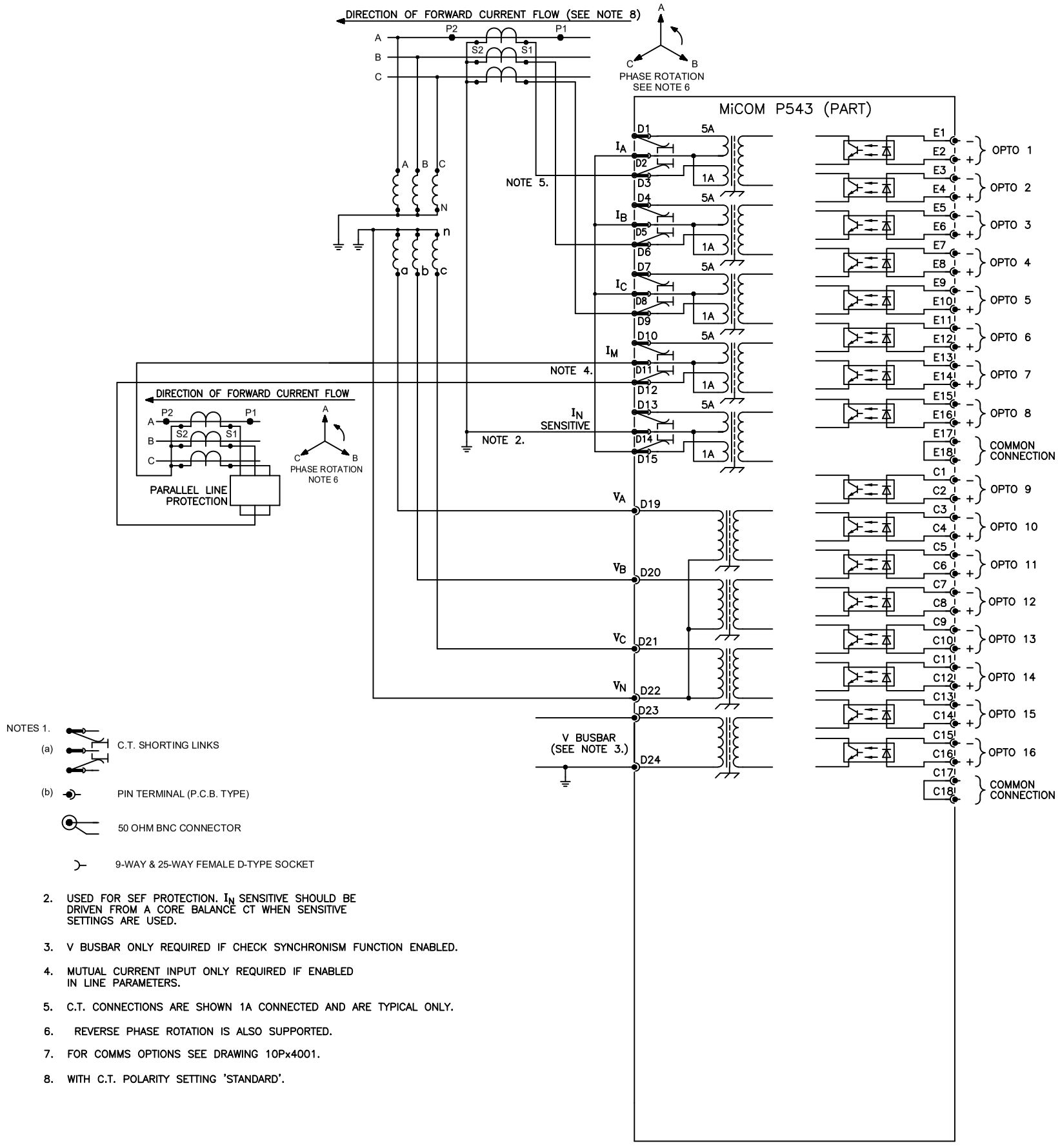
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.

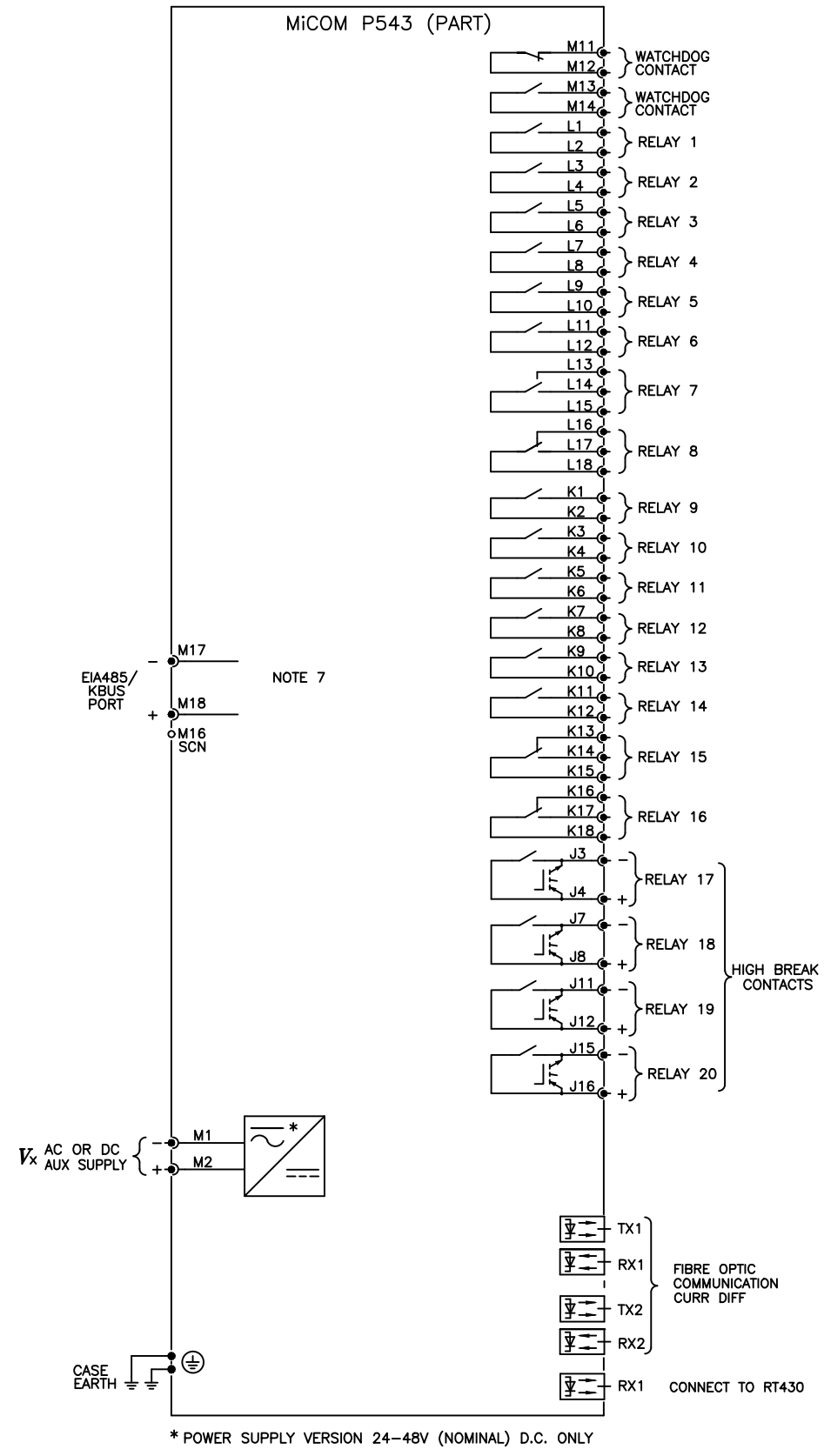
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED

7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 16I/16O + 4 HIGH SPEED HIGH BREAK RELAYS			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54319**	PLM No: A20076541	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





NOTES 1.

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(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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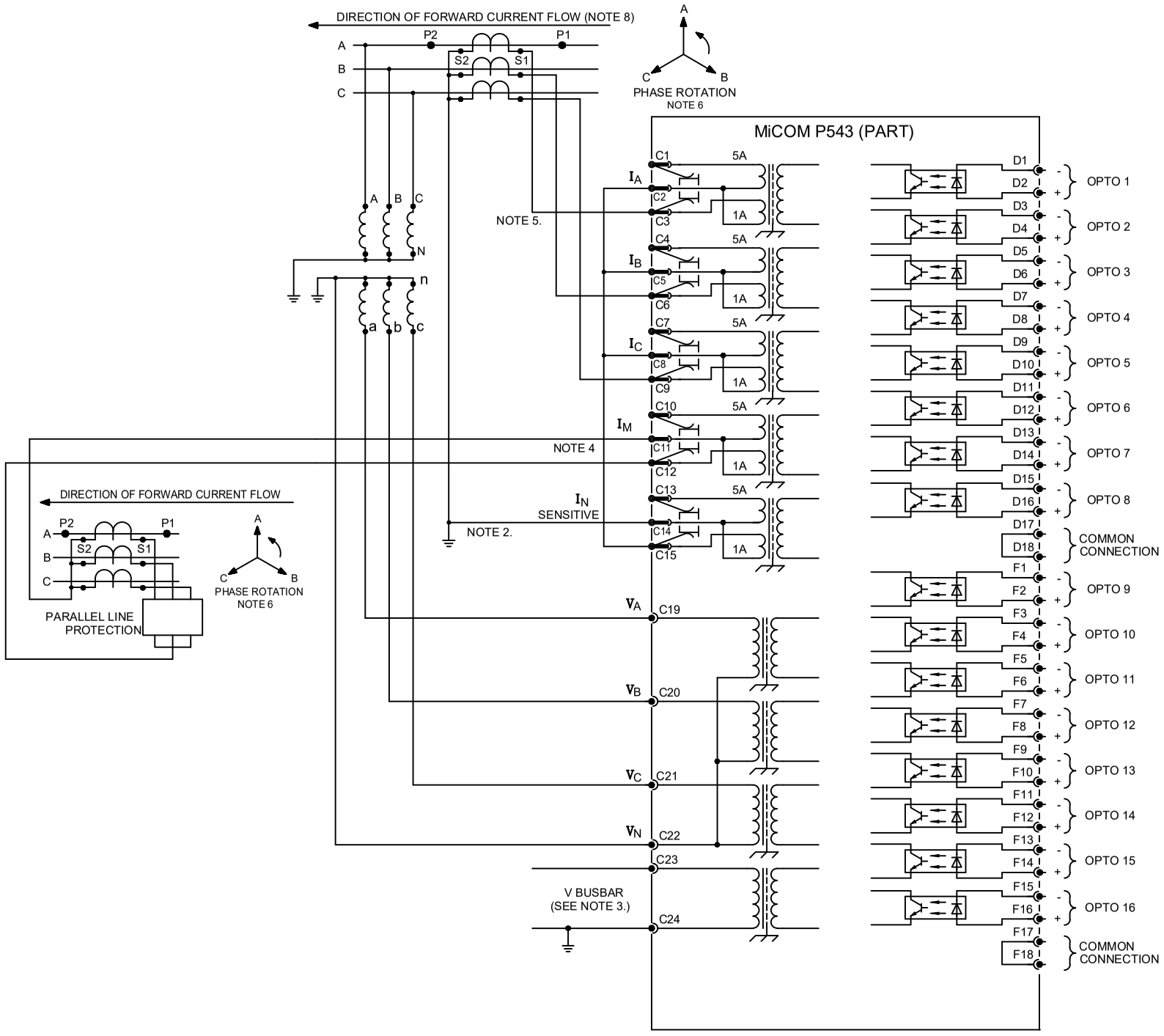
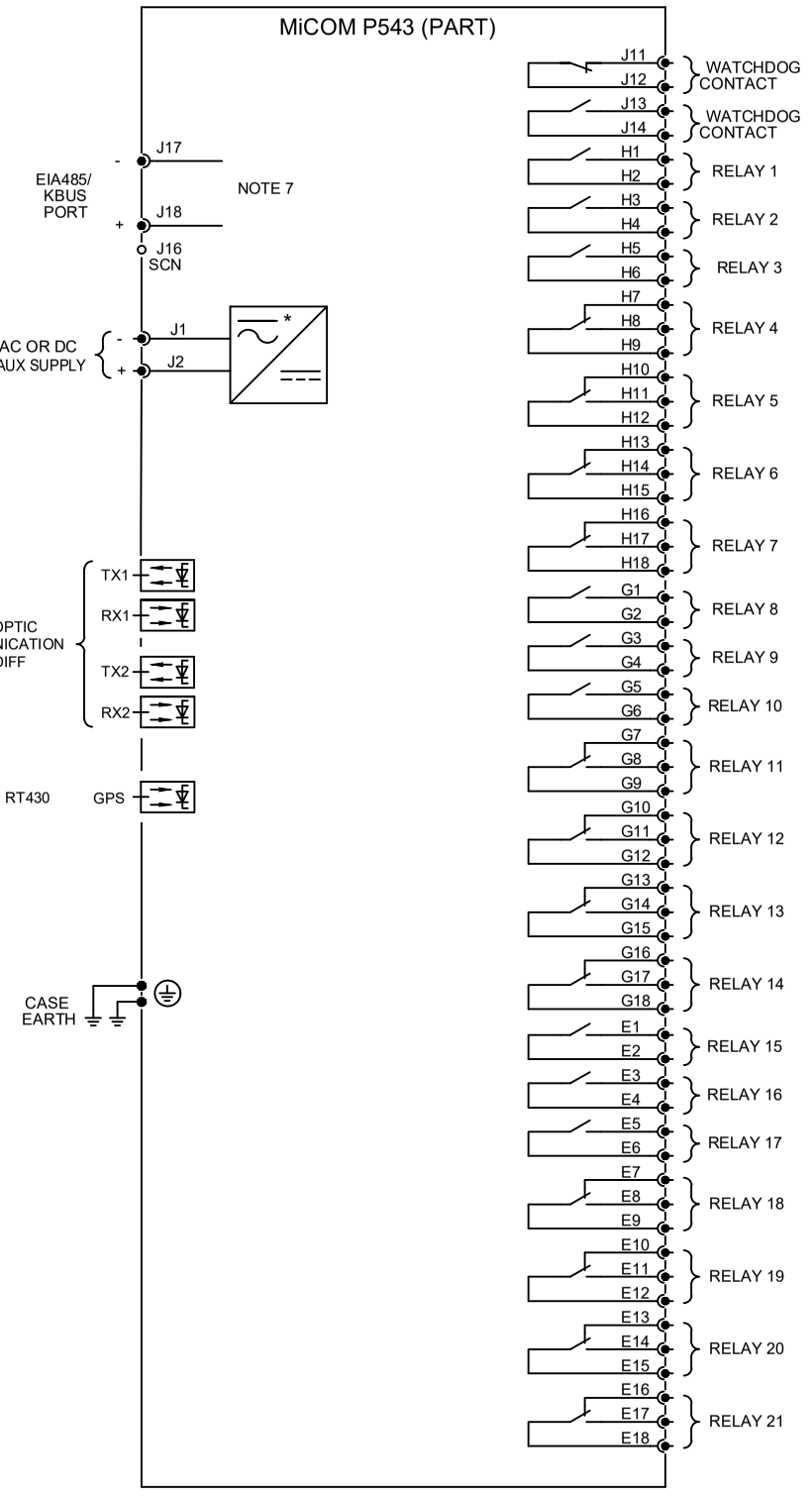
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: C	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 RELAY (80TE) 16I/16O + 4 HIGH SPEED HIGH BREAK			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54306**	PLM No: A20076495	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

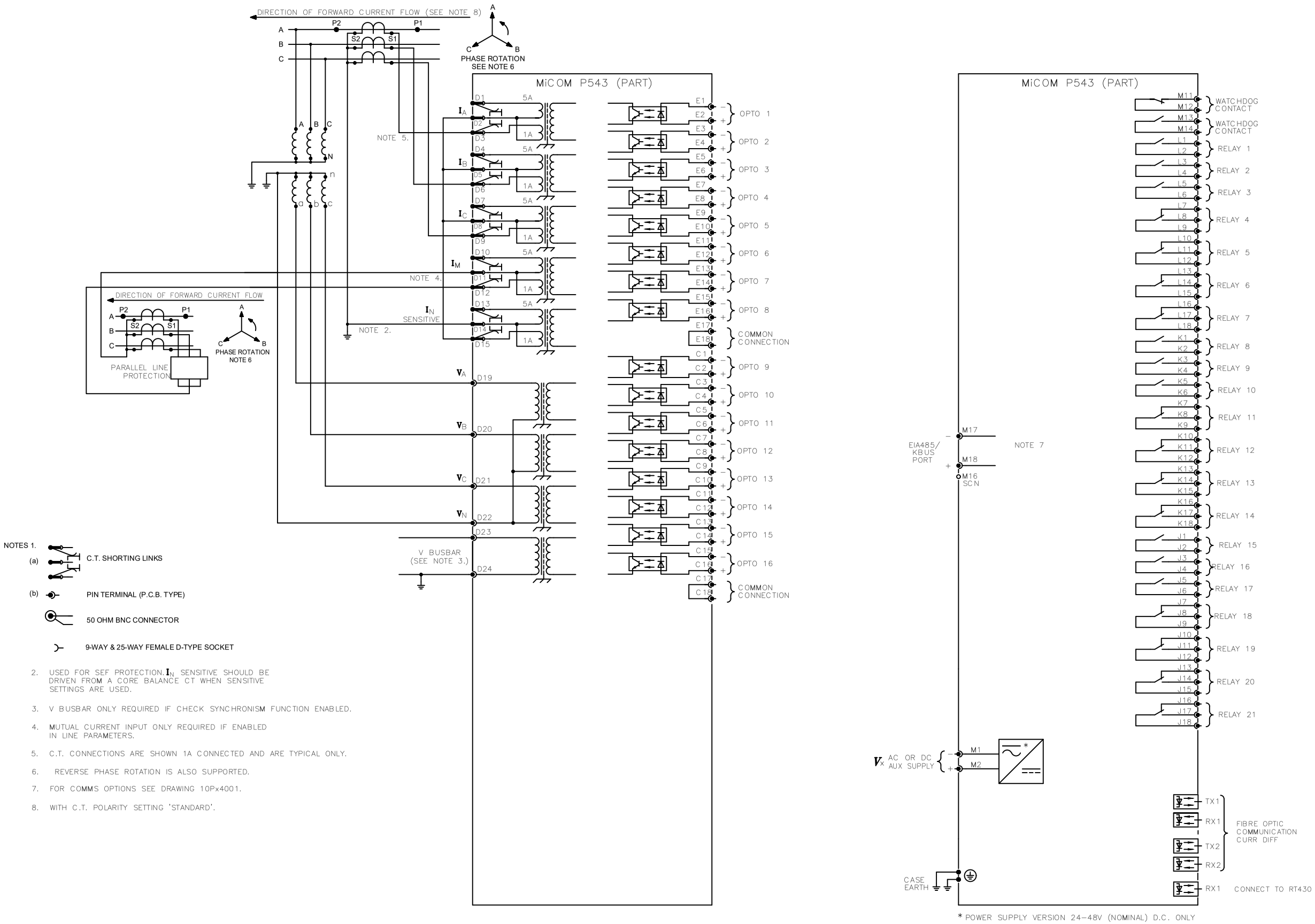
(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 16I/21O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54320**	PLM No: A20076555	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

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9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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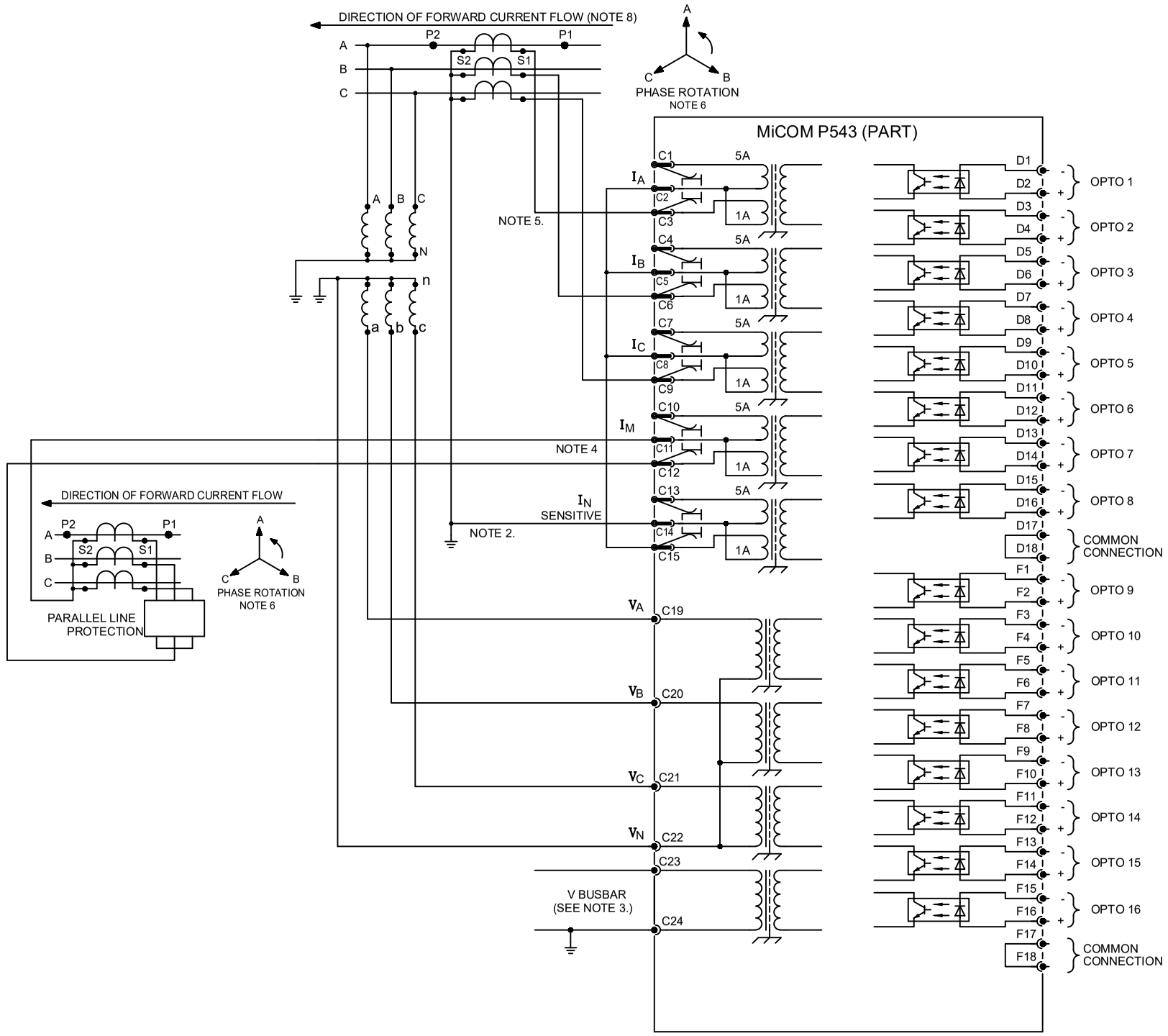
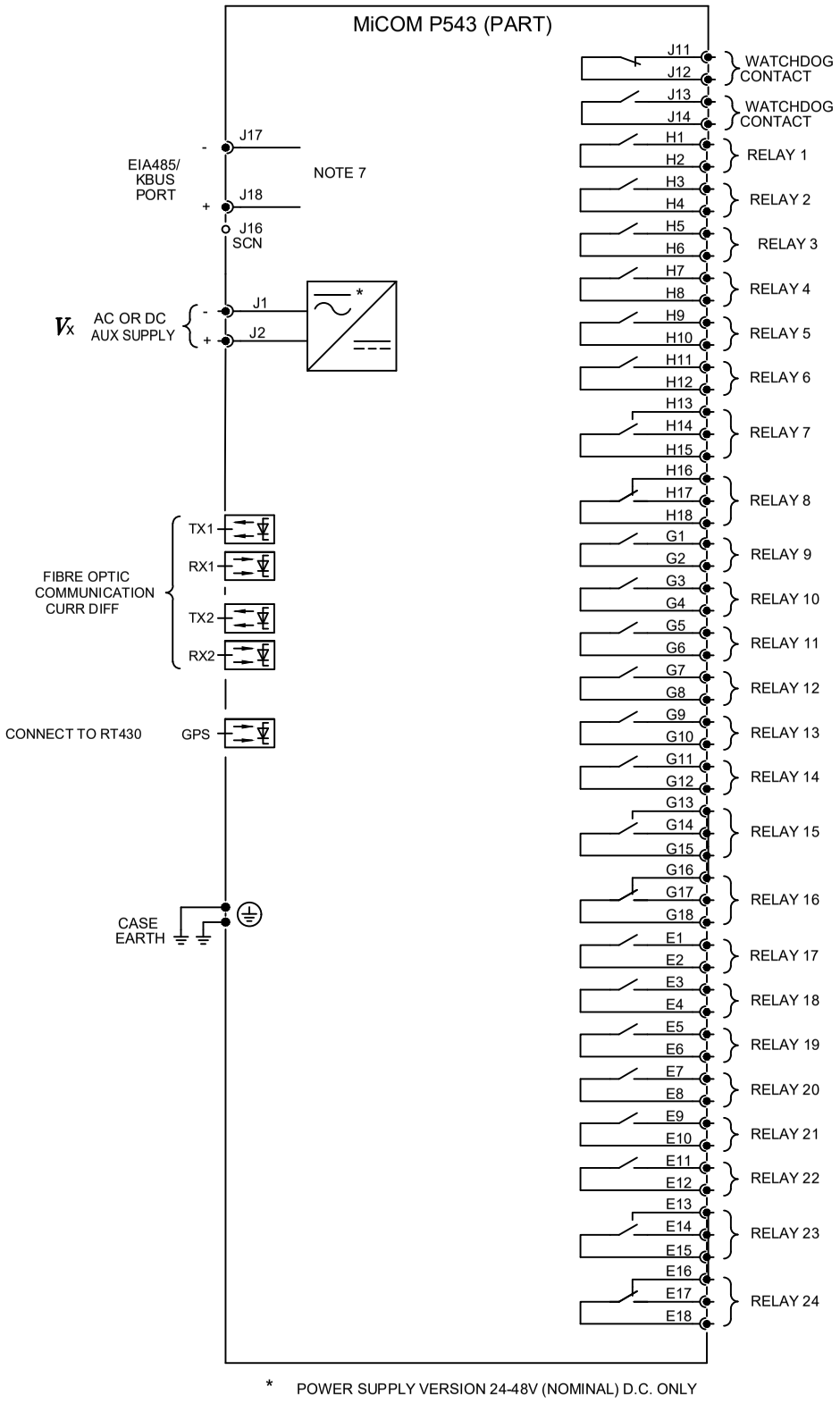
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 16I/21O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54307**	PLM No: A20076496	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

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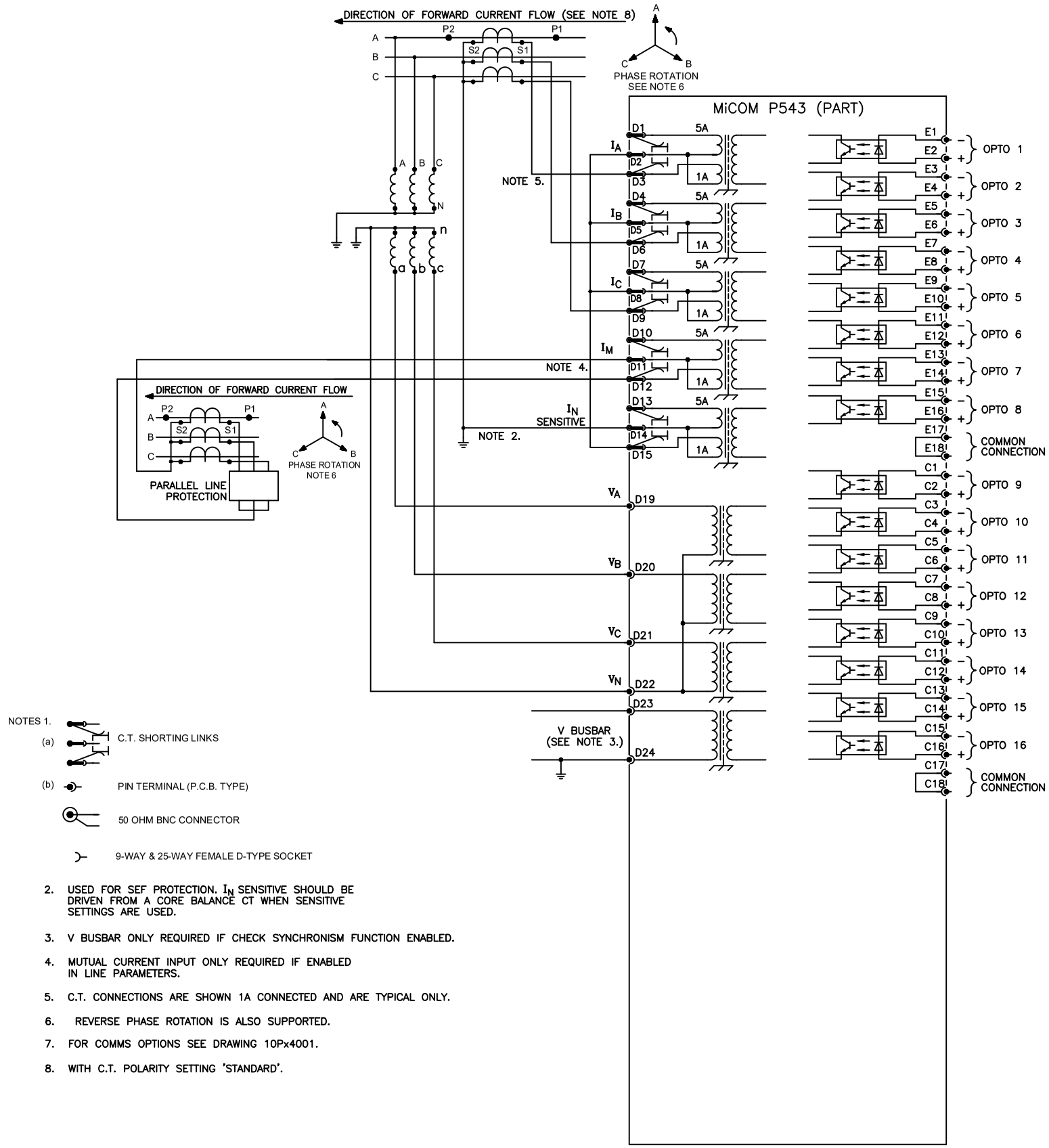
Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (60TE) 16I/24O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54321**	PLM No: A20076556	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



NOTES 1.

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(b) PIN TERMINAL (P.C.B. TYPE)

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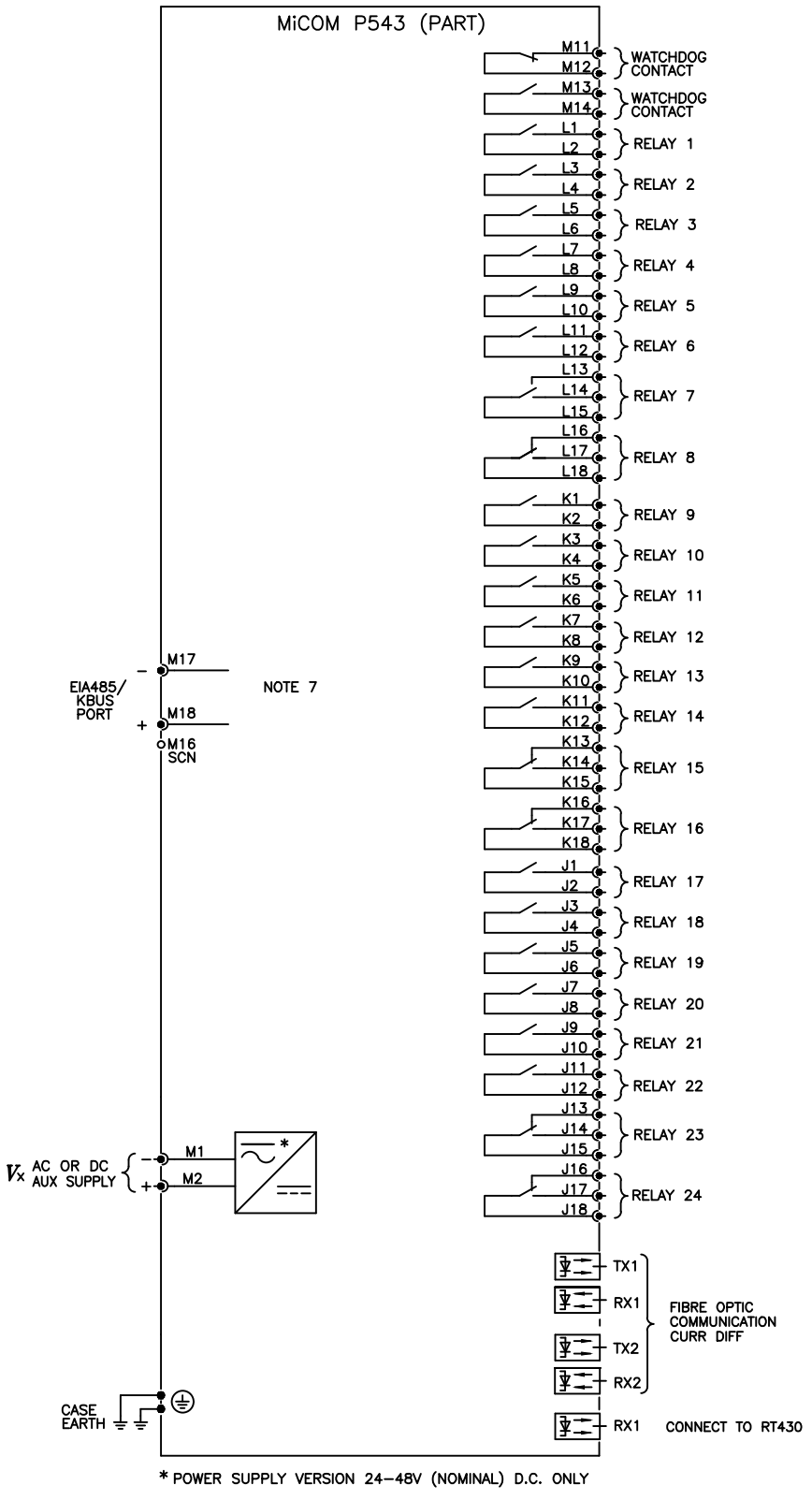

* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 16I/24O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54308**	PLM No: A20076515	Sht: 1	GE VERNOVA
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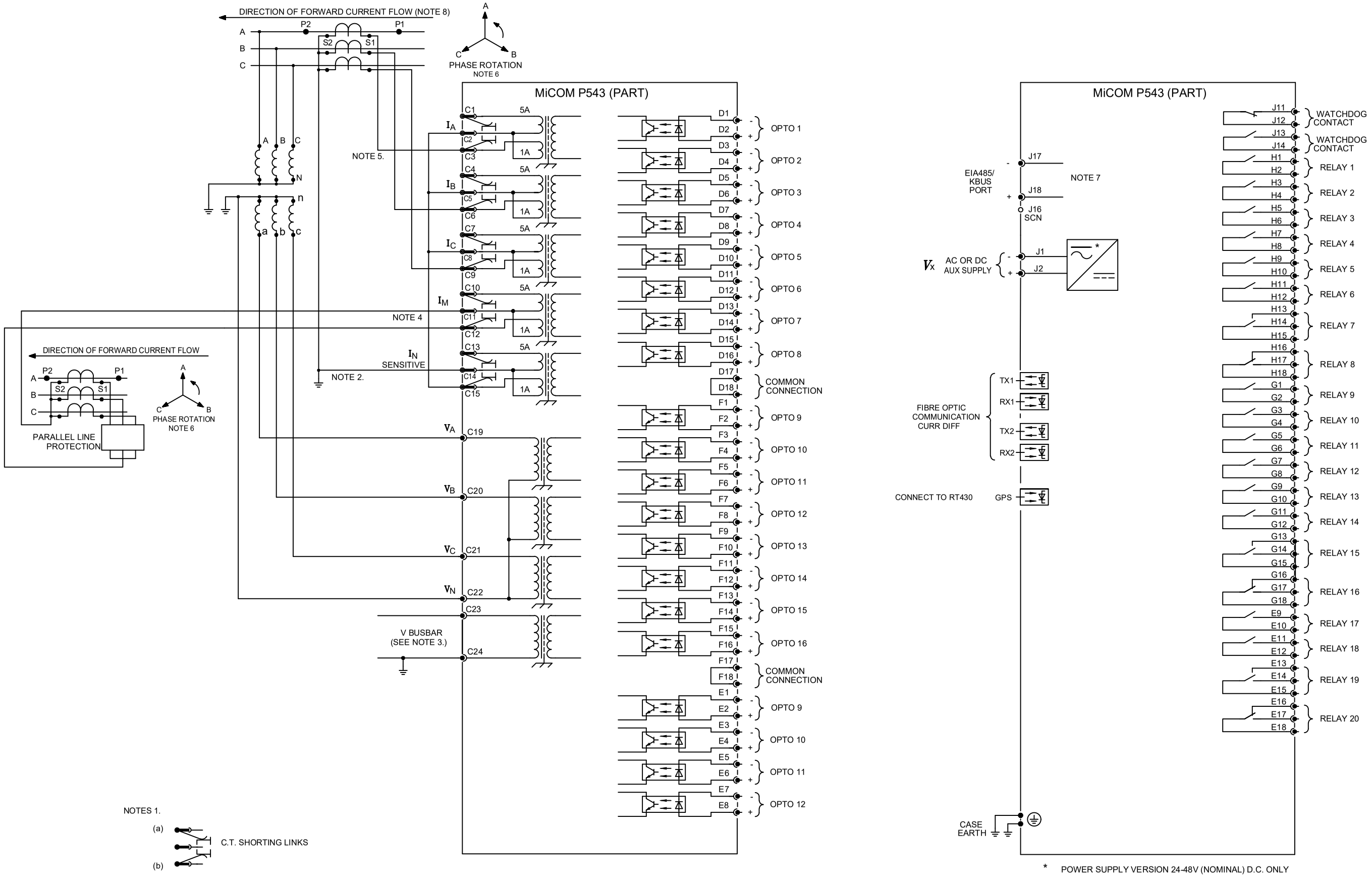

NOTES 1.

(a) C.T. SHORTING LINKS

(b)

PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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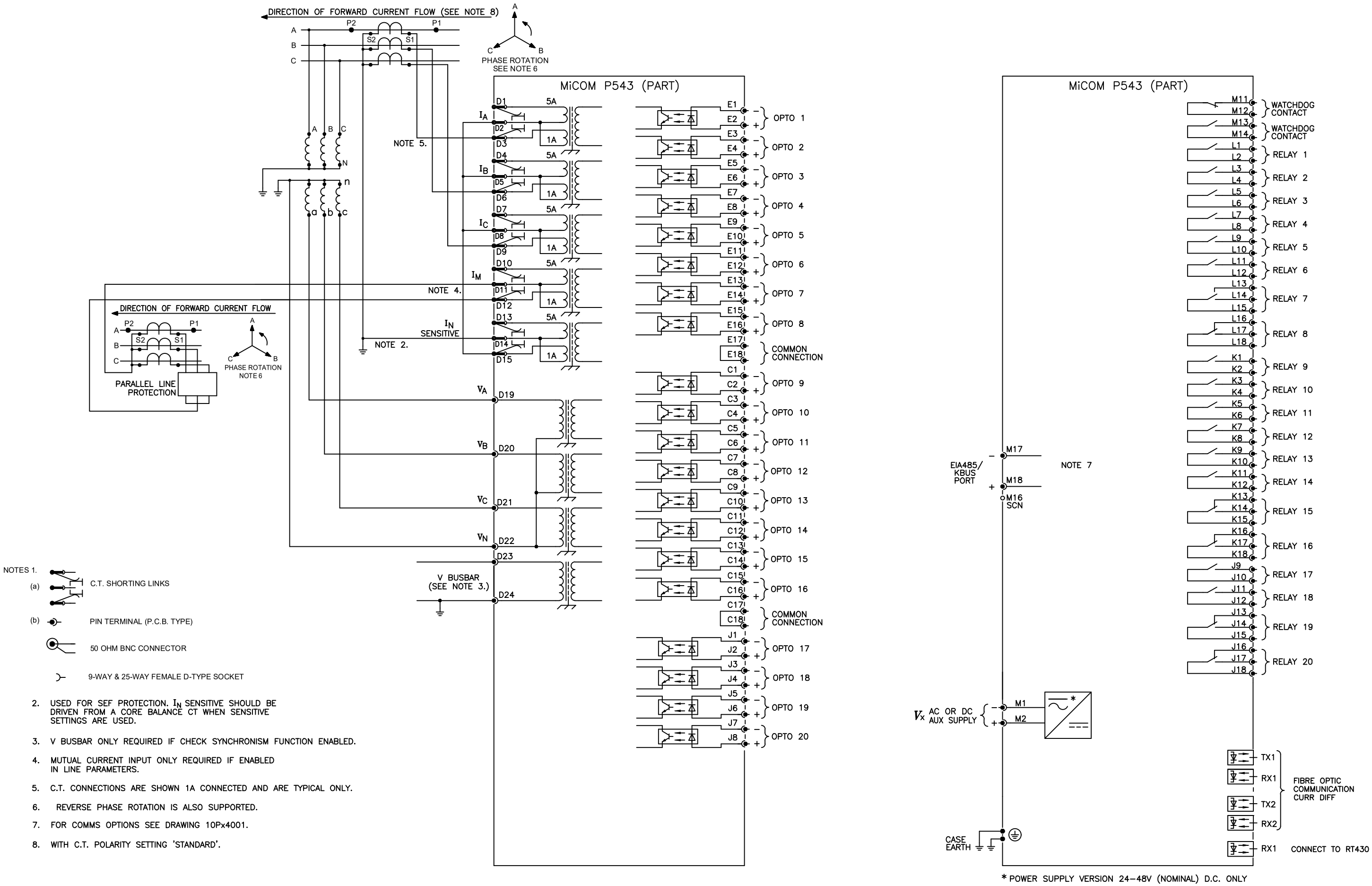
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 20I/20O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54368**	PLM No: A20097497	Sht: 1 Next Sht: -	GE VERNOVA
Date:	Chkd:					



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

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9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 20I/20O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54358**	PLM No: A20097218	Sht: 1	GE VERNOVA
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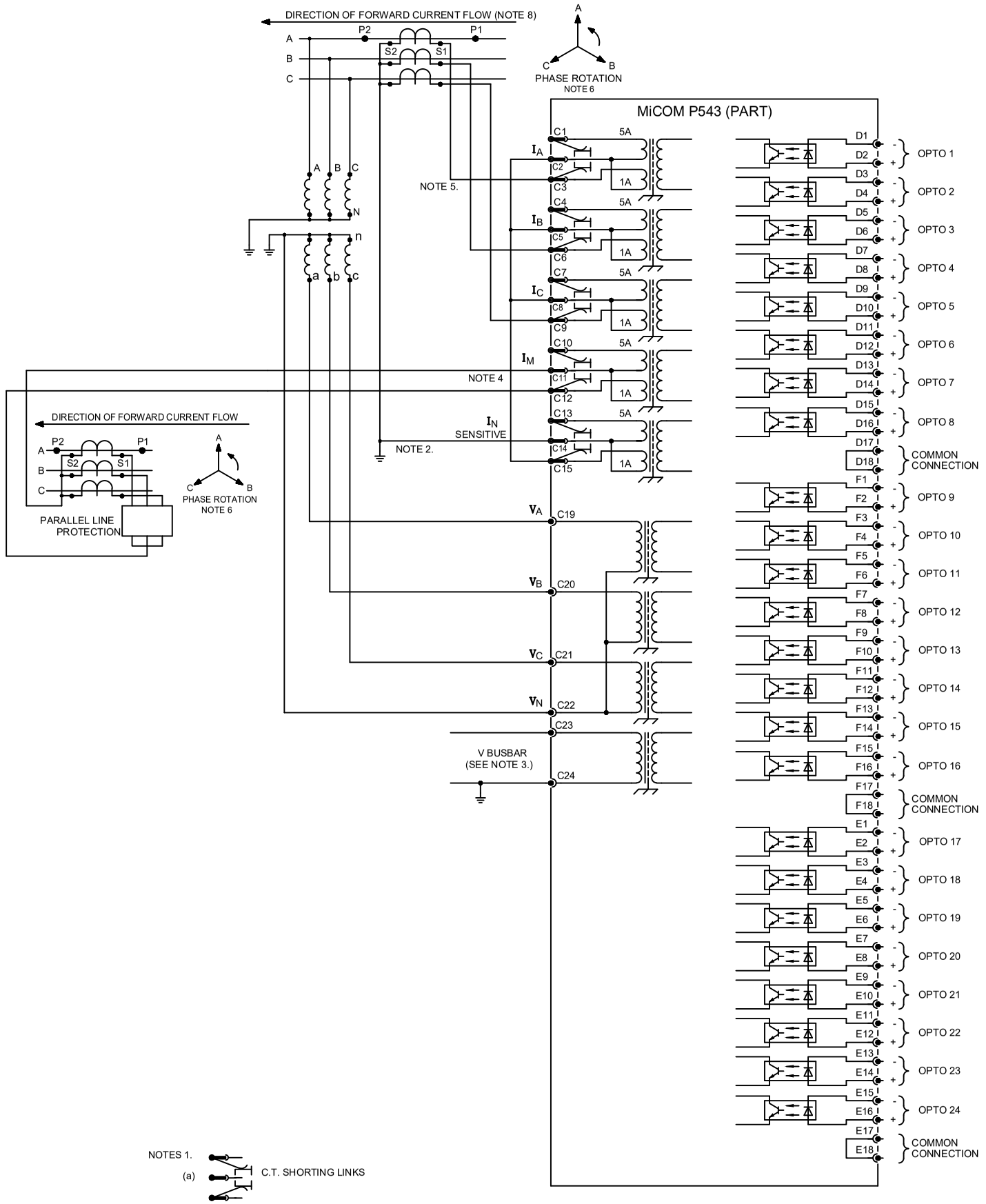

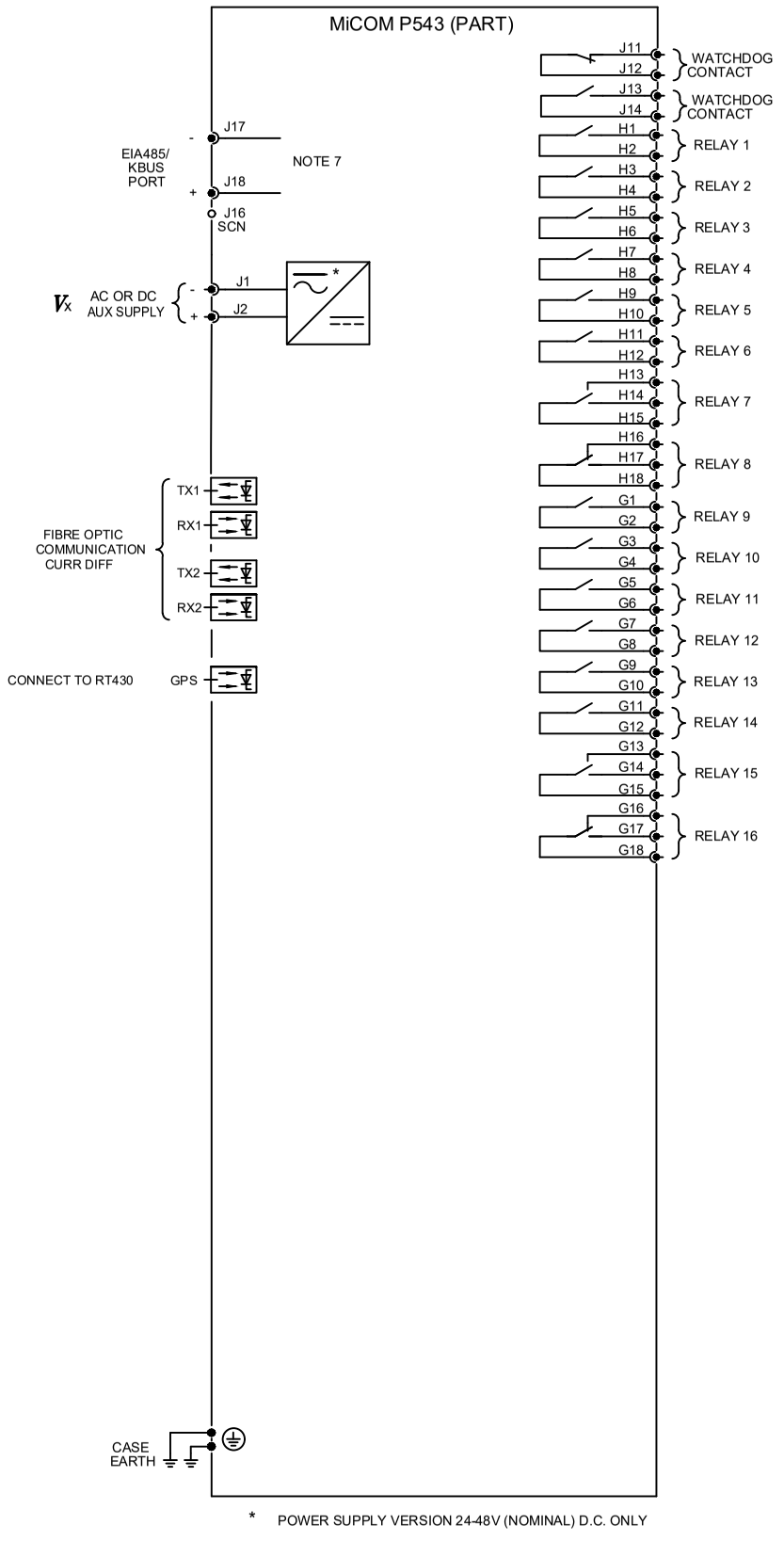

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES 1.

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7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 24I/16O		
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54371**	PLM No: A20097501	Sht: 1
Date:	Chkd:				Next Sht: -

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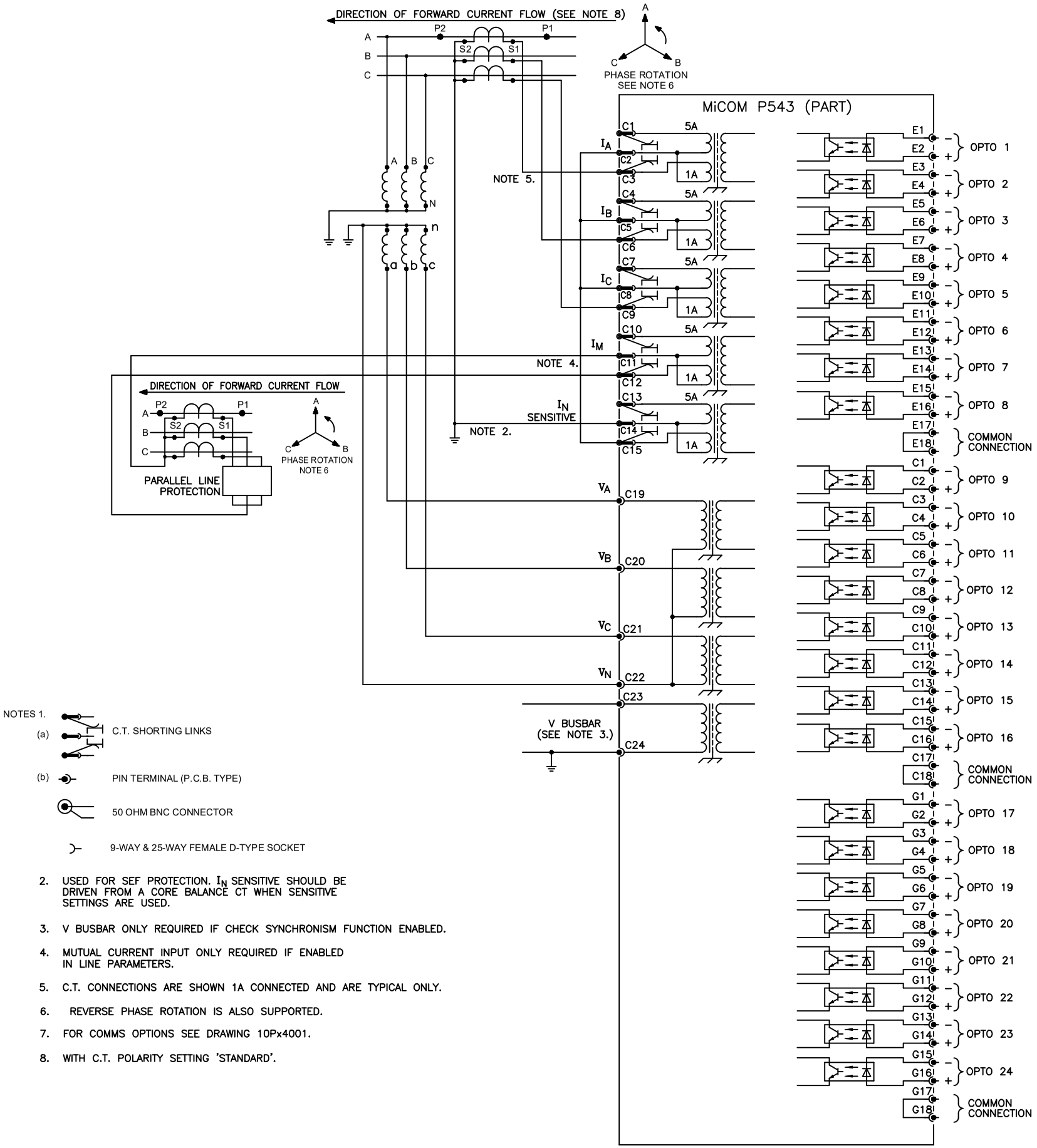

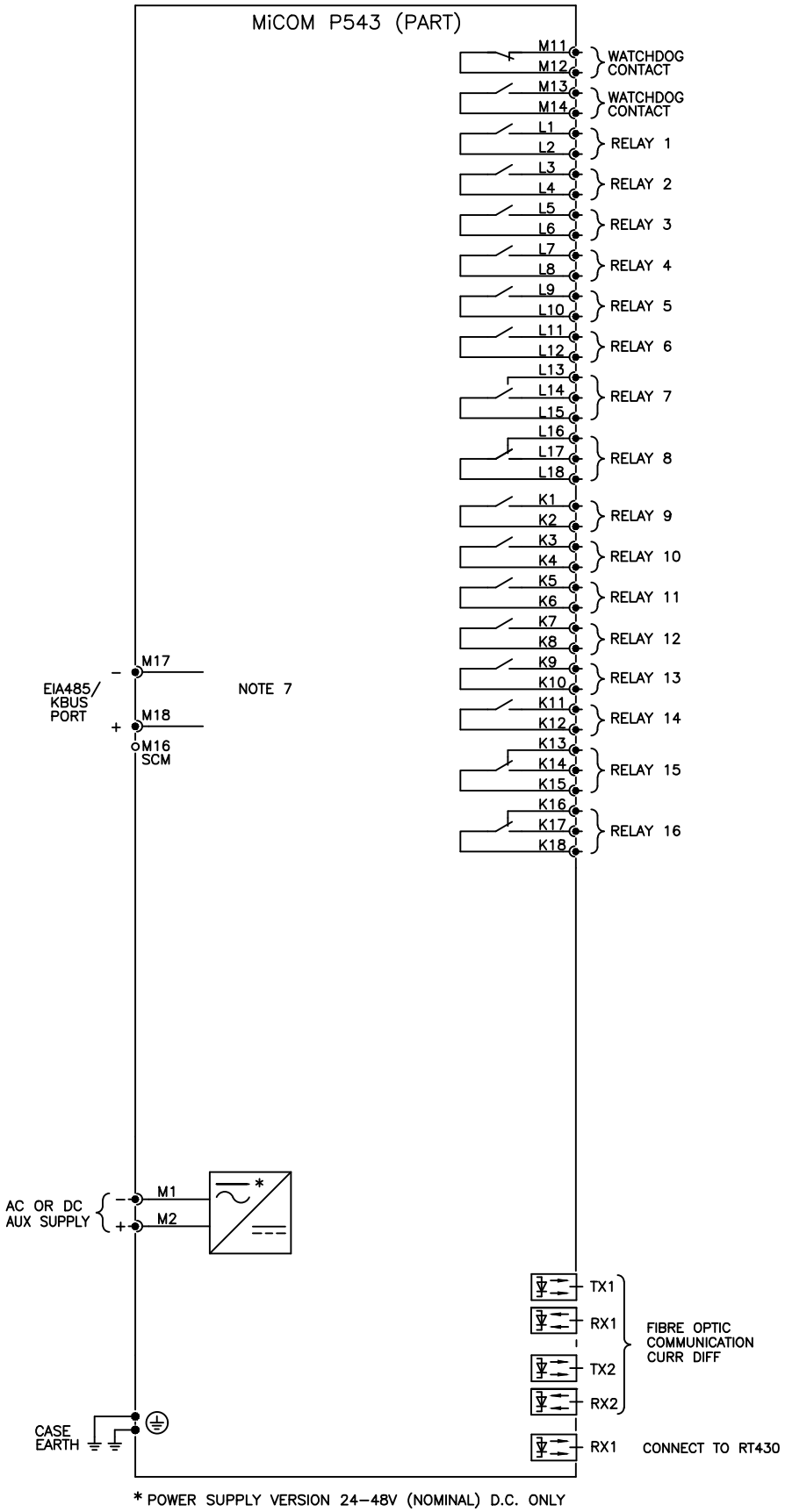

NOTES 1.

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Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I/16O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54360**	PLM No: A20097235	Sht: 1	GE VERNOVA
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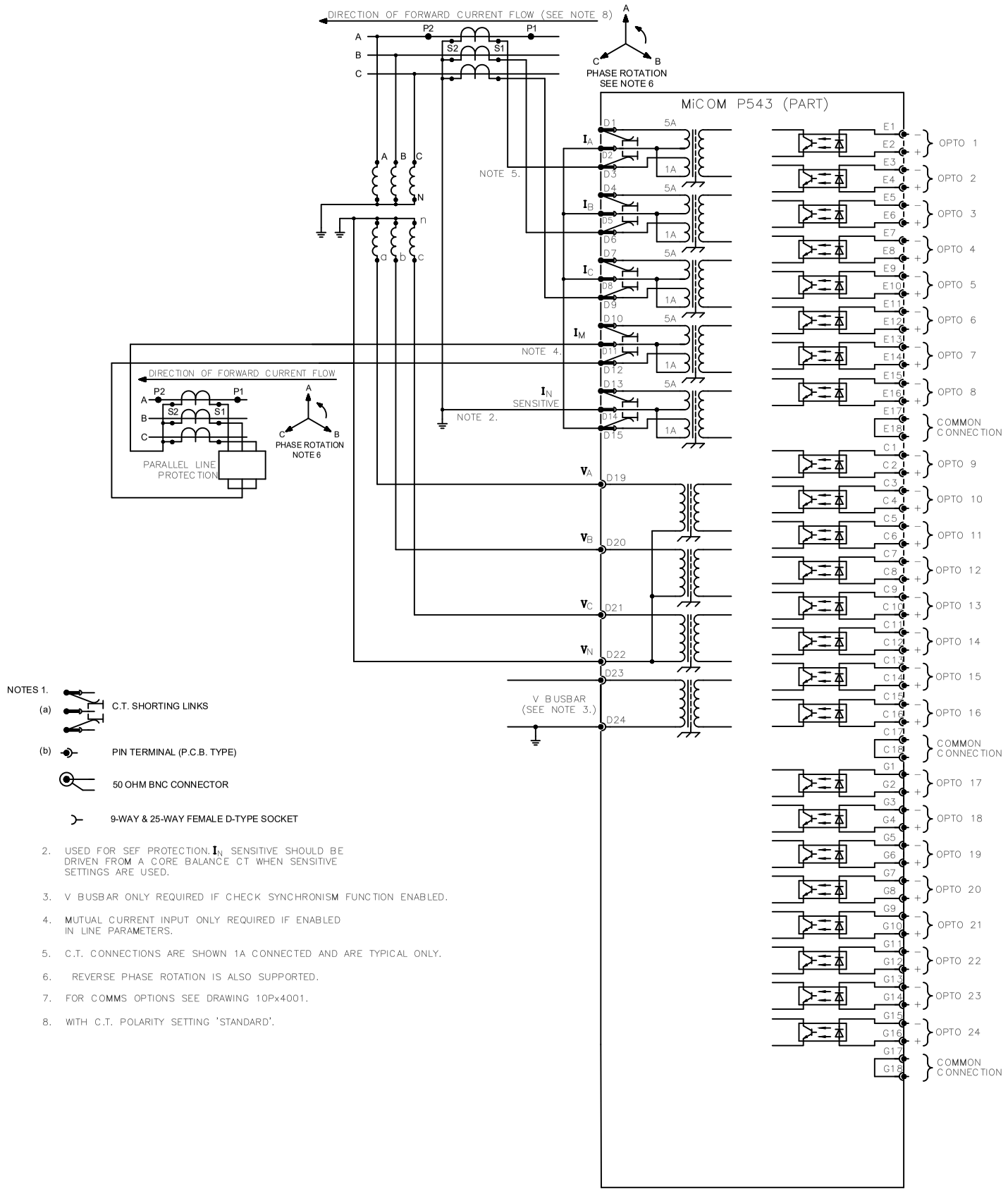

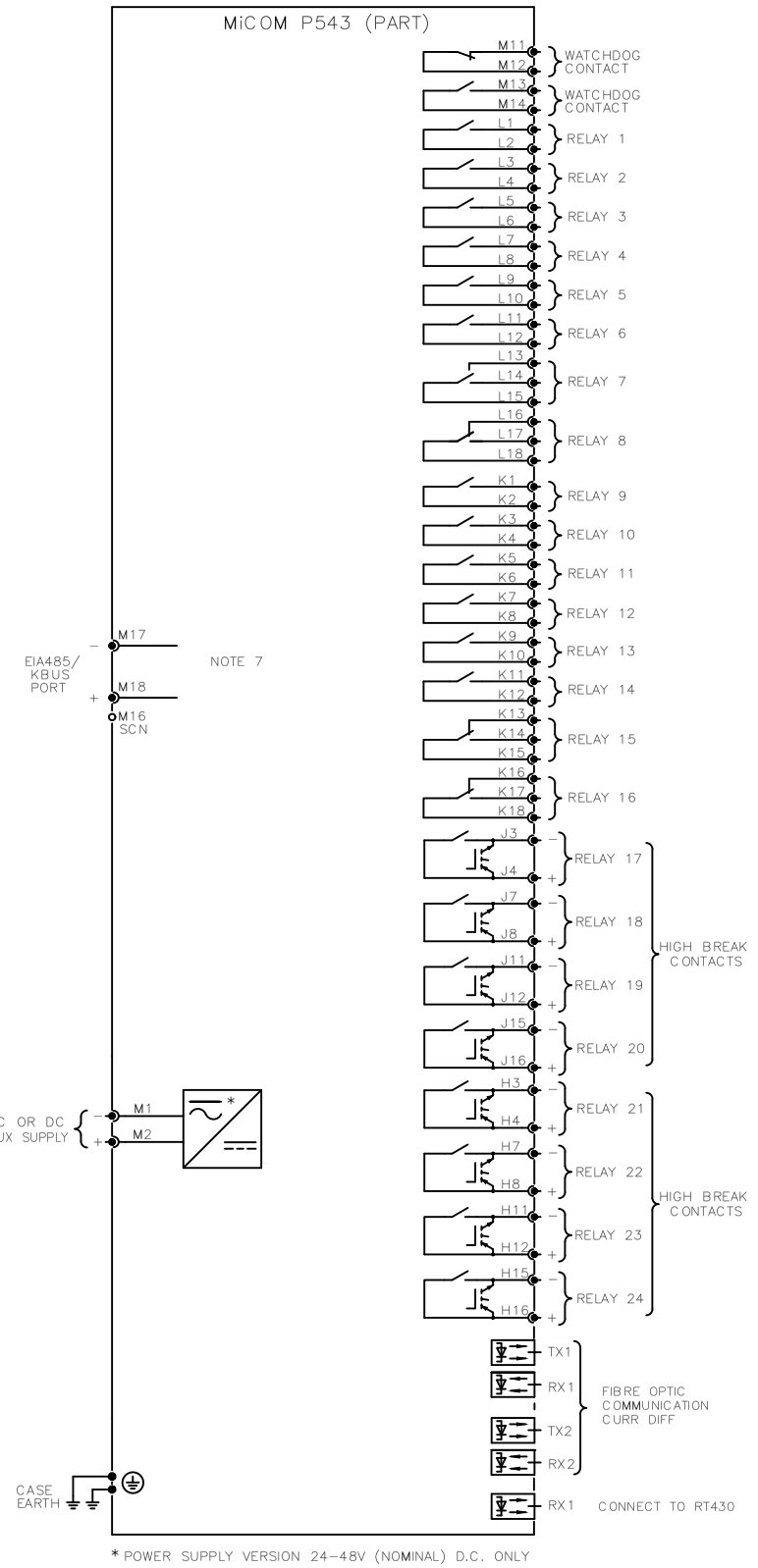

NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

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8. WITH C.T. POLARITY SETTING 'STANDARD'.

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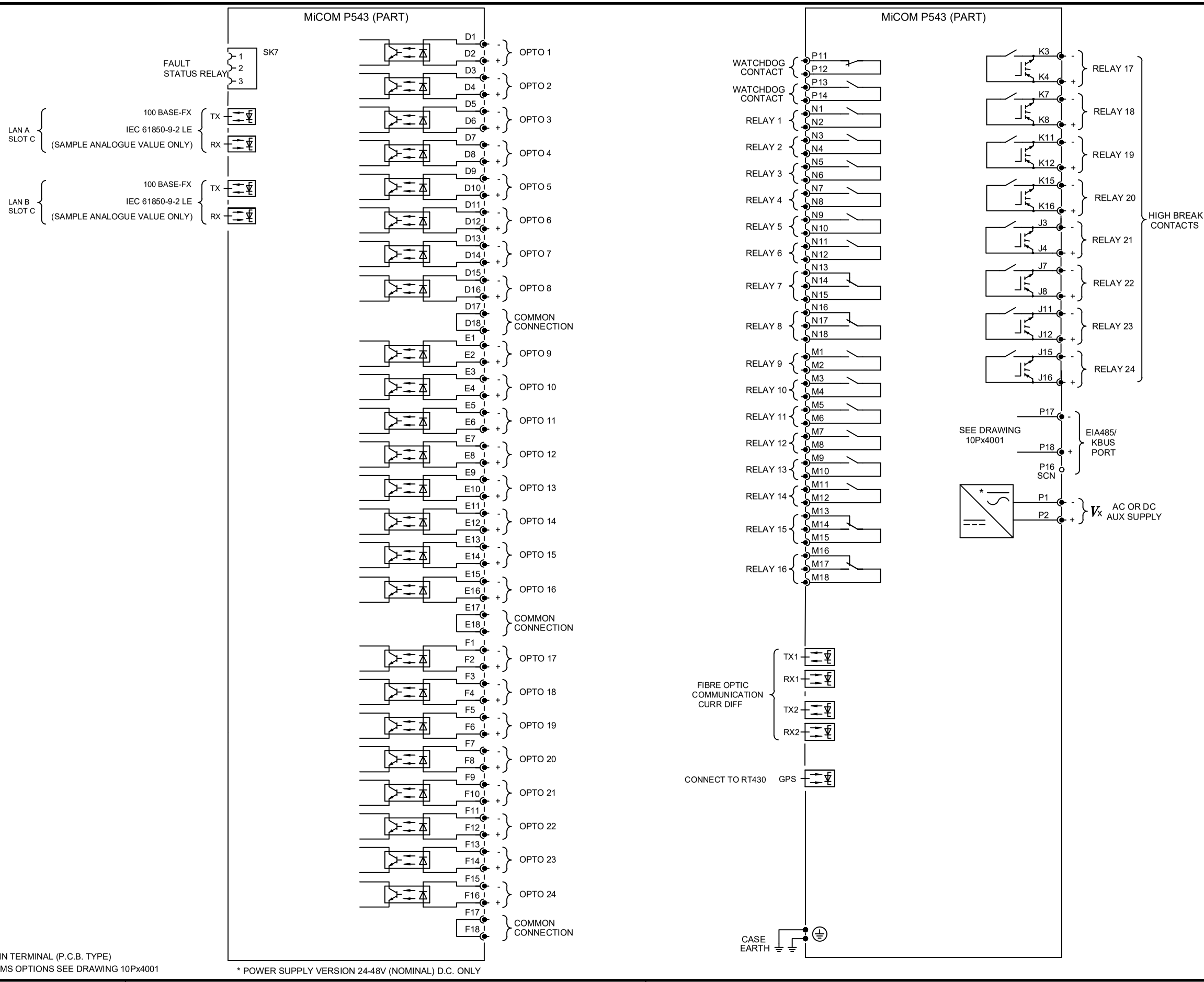
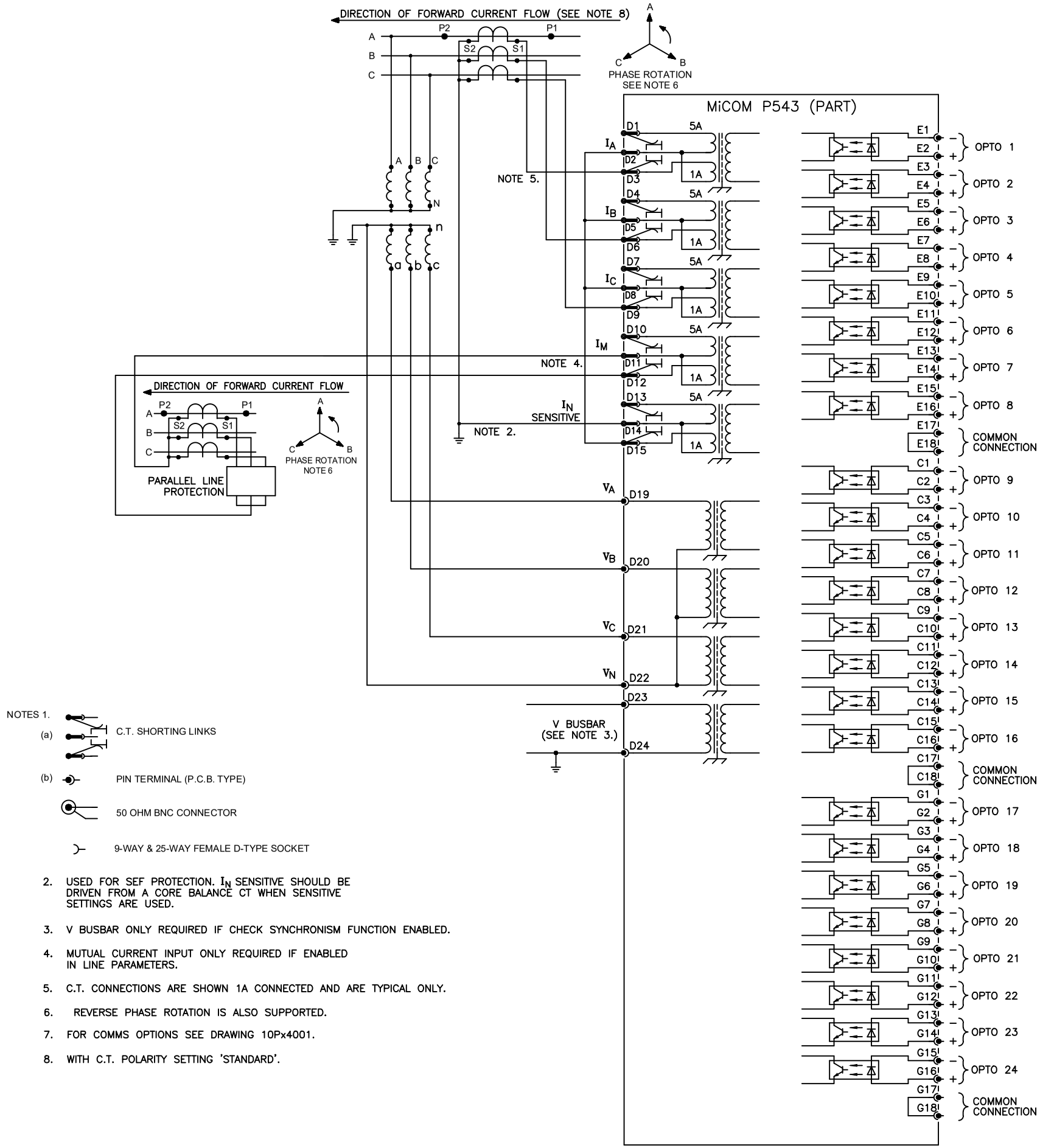
Issue: B	Status: **In Work**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 24I/16O + 8 HIGH SPEED HIGH BREAK			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54309**	PLM No: A20076516	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	

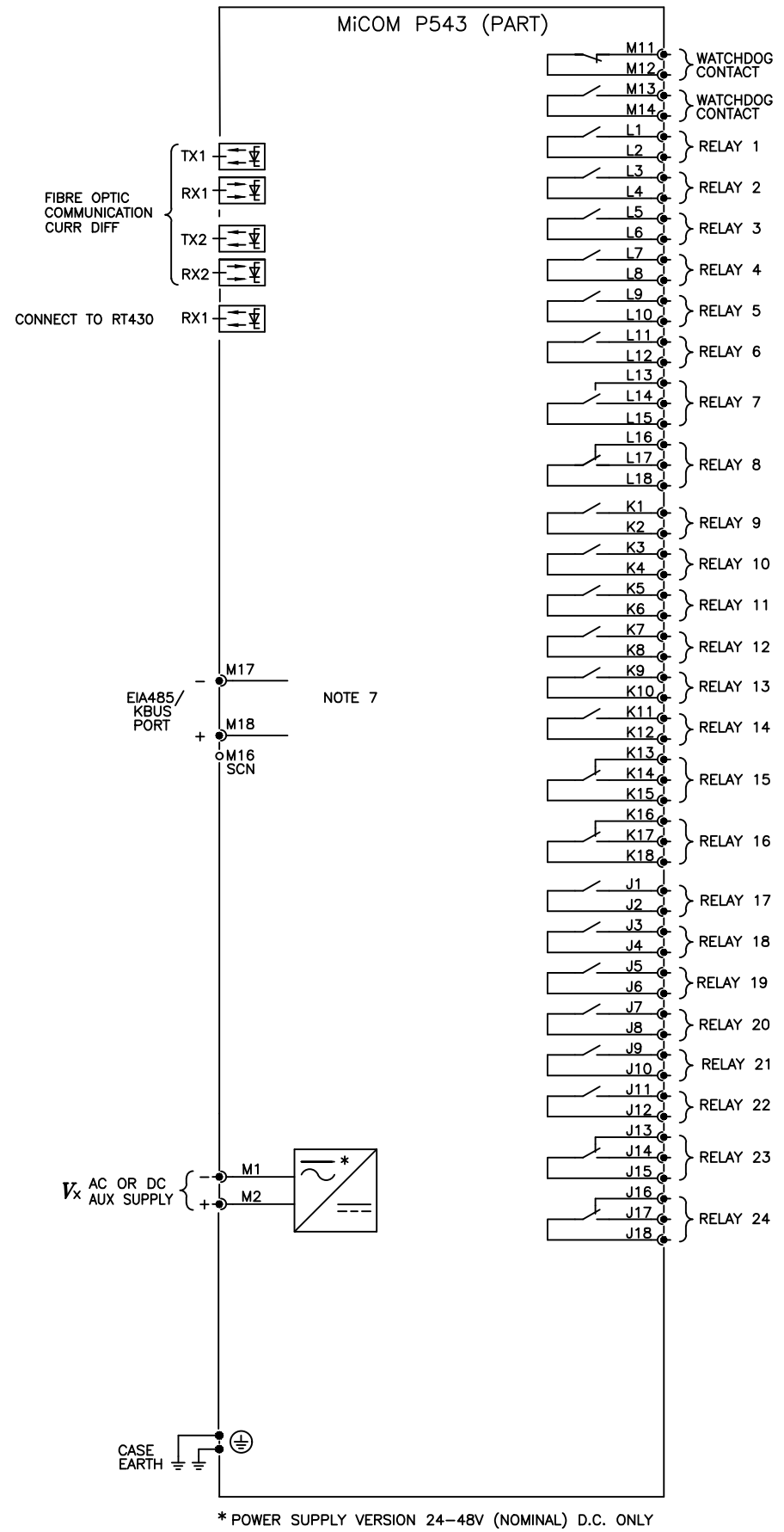


NOTES .

1. PIN TERMINAL (P.C.B. TYPE)
2. FOR COMMS OPTIONS SEE DRAWING 10Px4001

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 24I/16O + 8 HIGH SPEED HIGH BREAK RELAYS			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54336**	PLM No: A20076598	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





NOTES 1.

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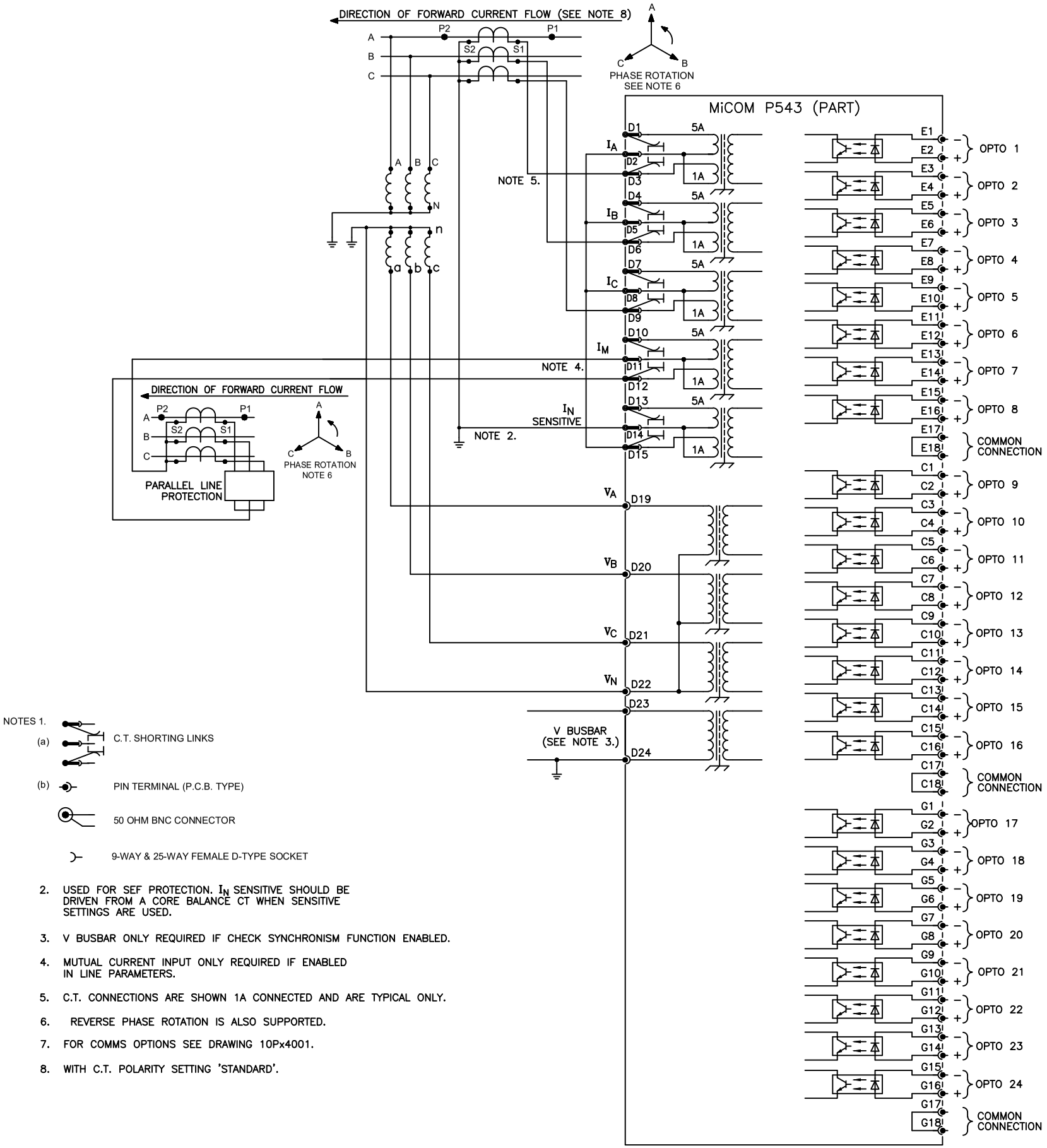
Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I/24O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54361**	PLM No: A20097236	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



NOTES 1.

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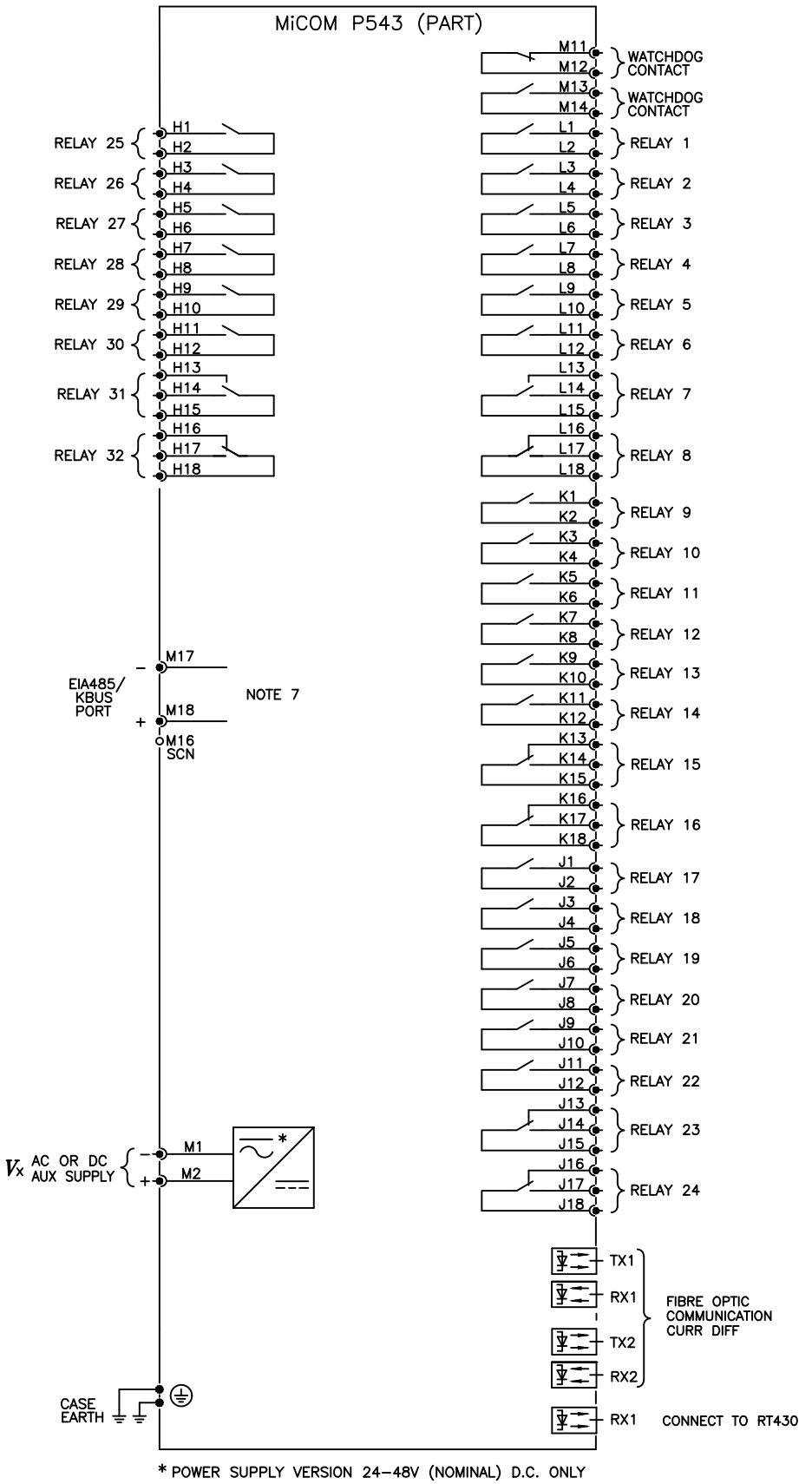
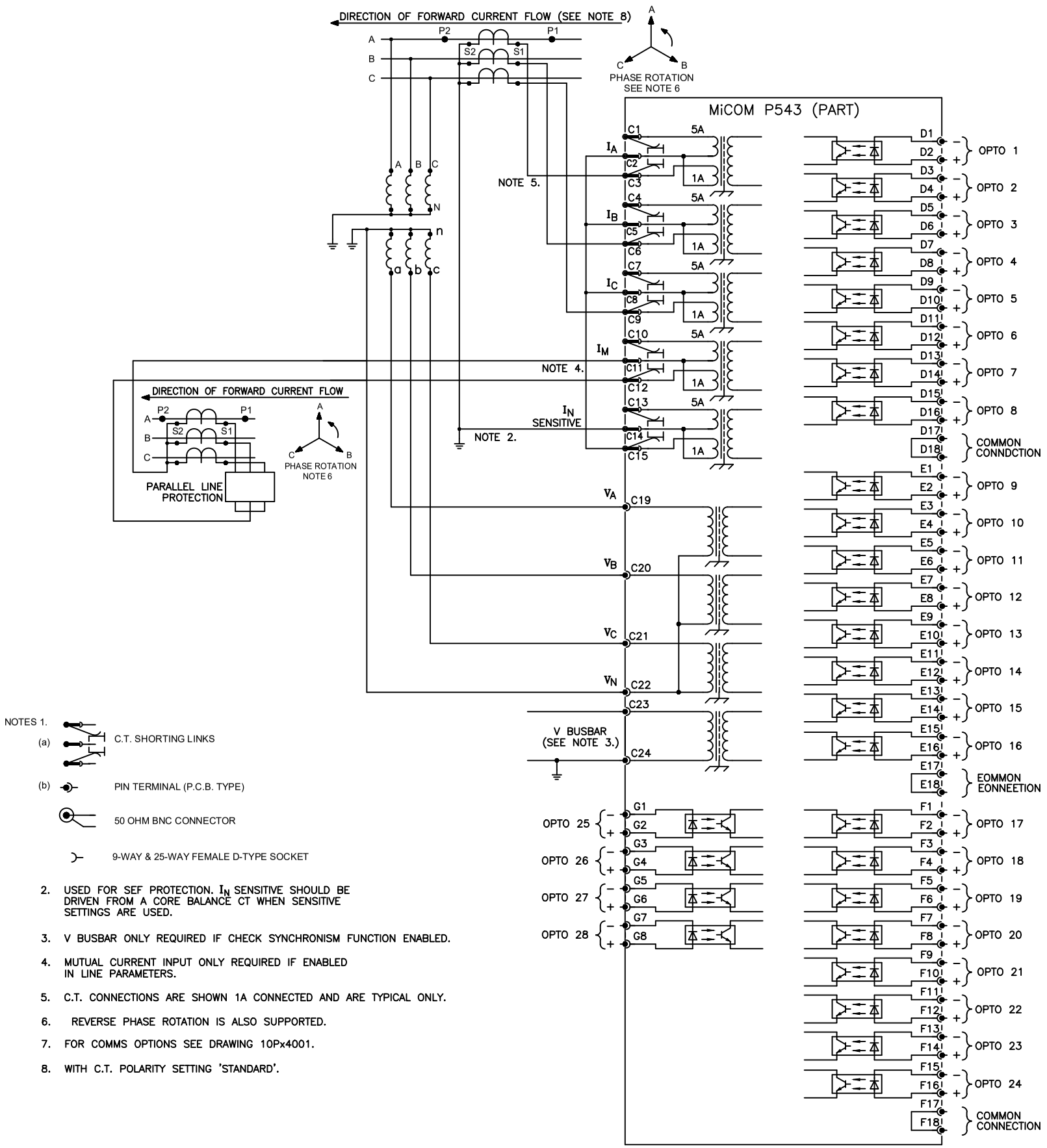
2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.



* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 24I/32O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54310**	PLM No: A20076517	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



NOTES 1.

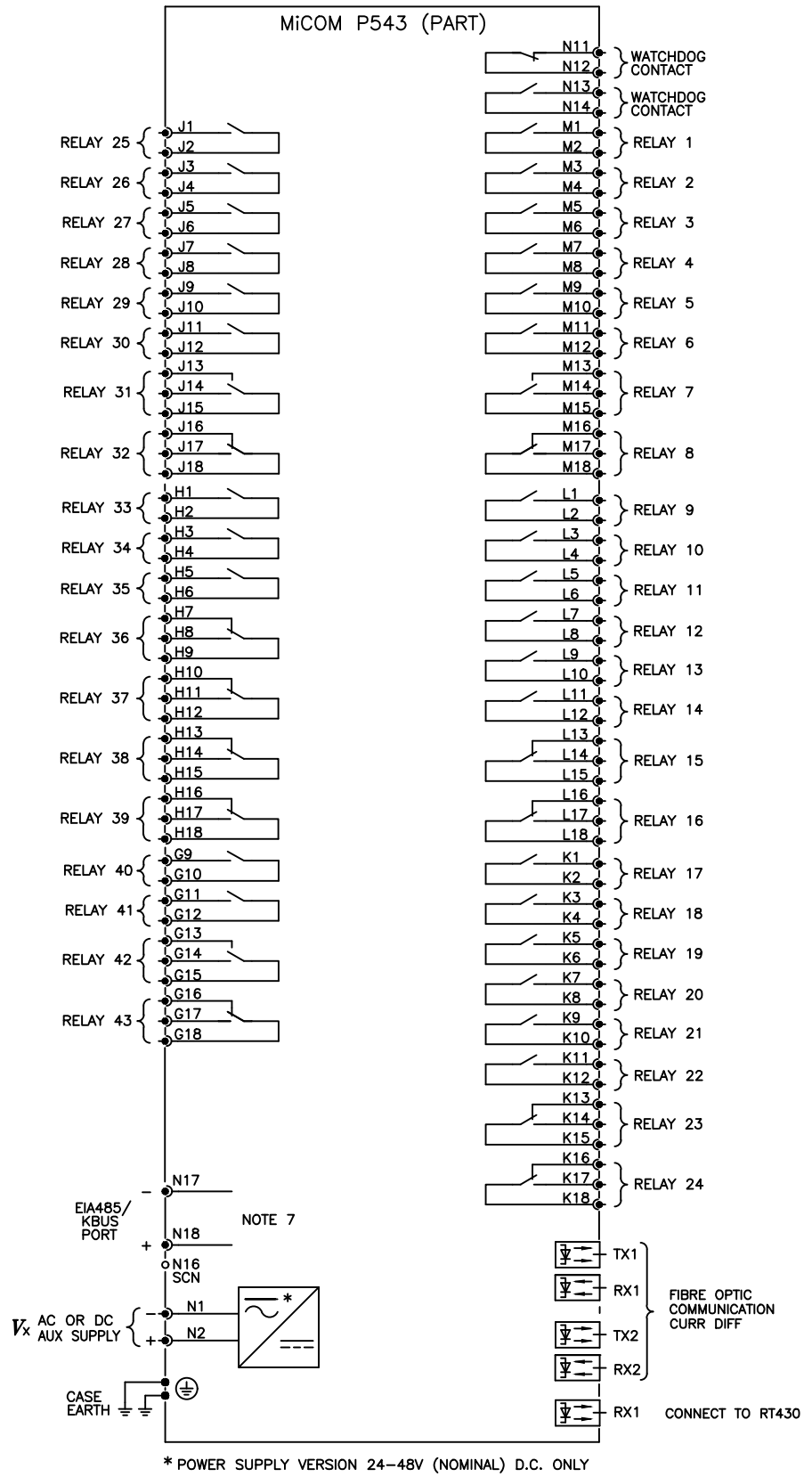
(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

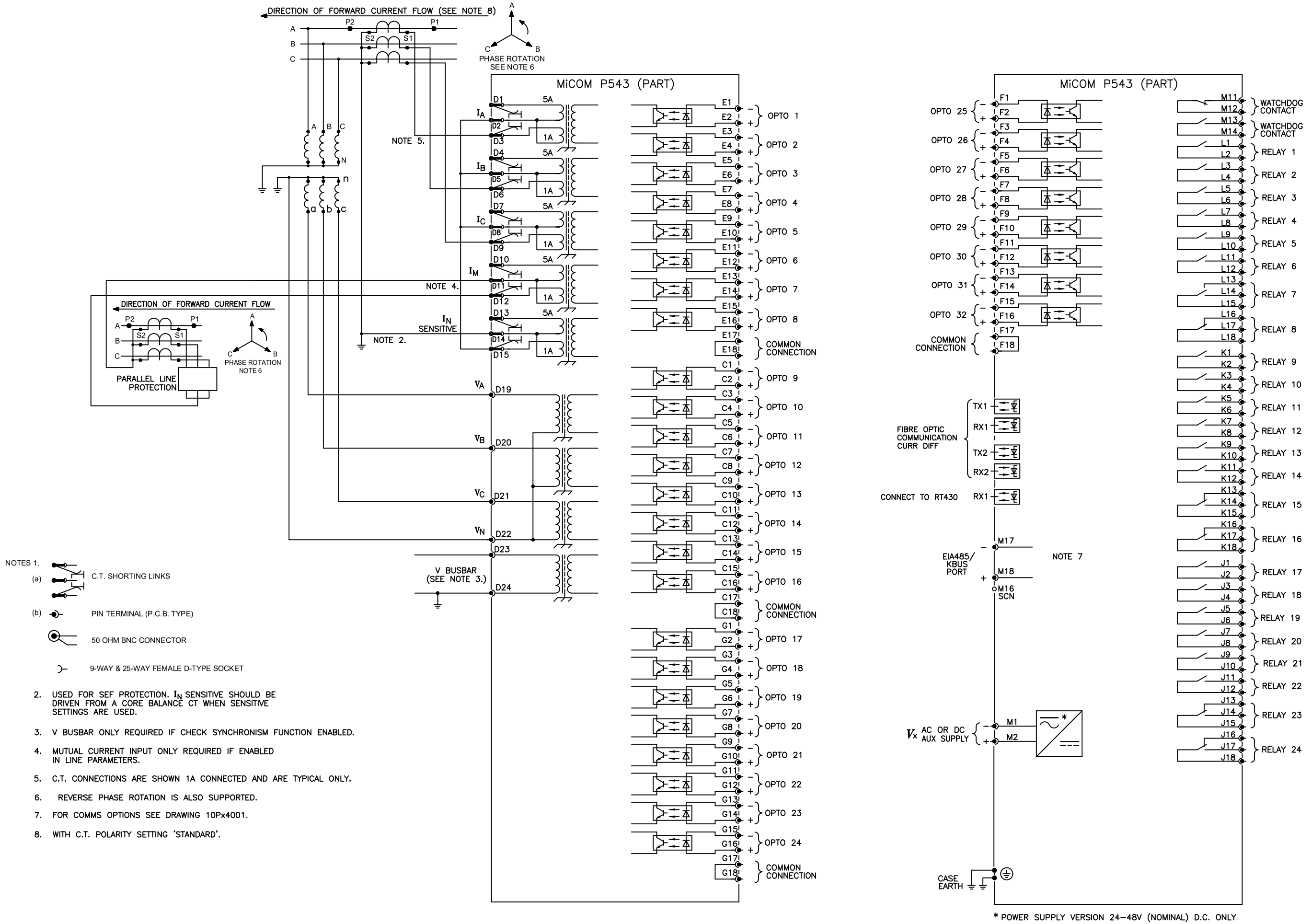
9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.



* POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 28I/43O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54341**	PLM No: A20076615	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



NOTES 1.

(a) C.T. SHORTING LINKS

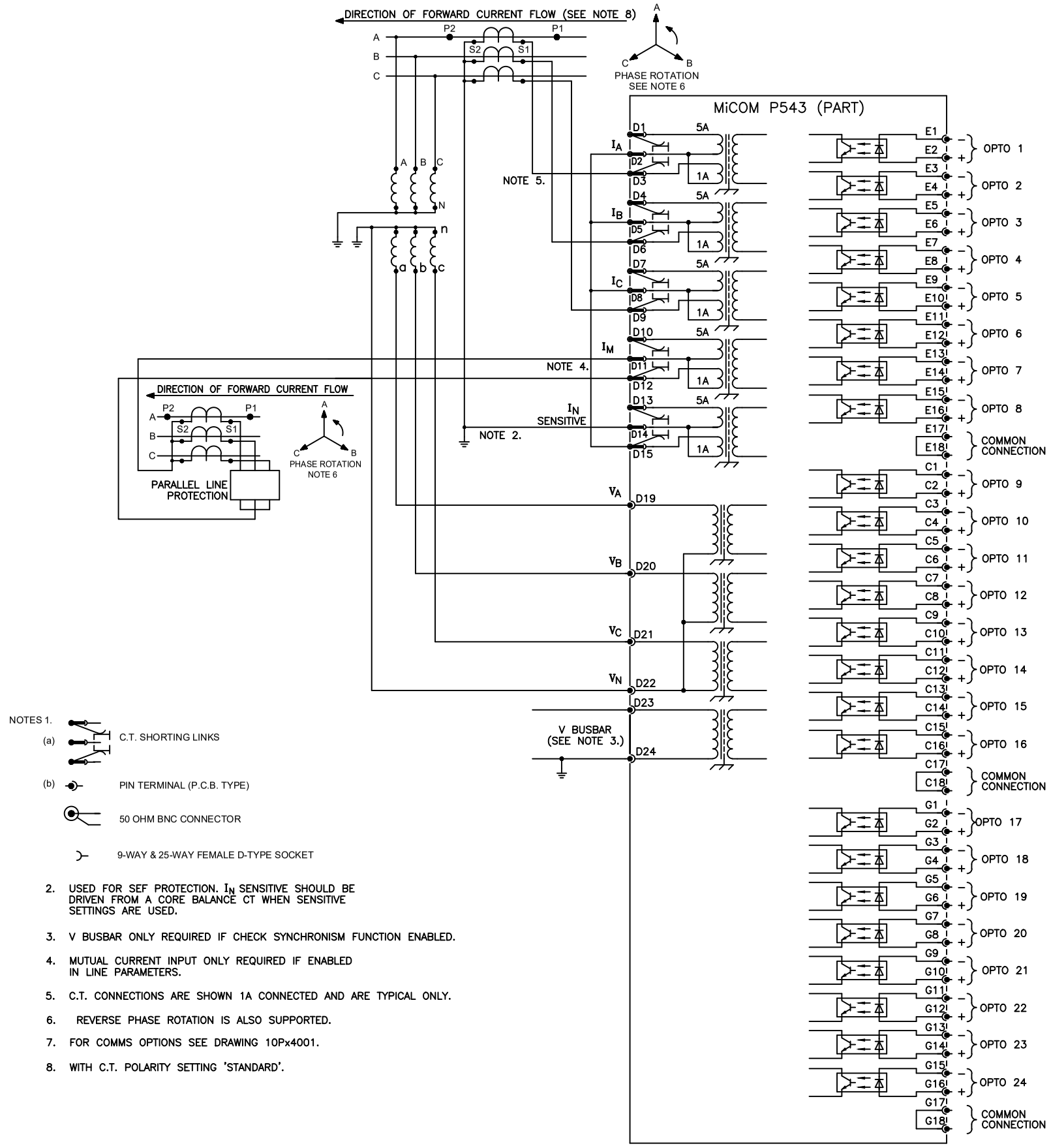
(b) PIN TERMINAL (P.C.B. TYPE)

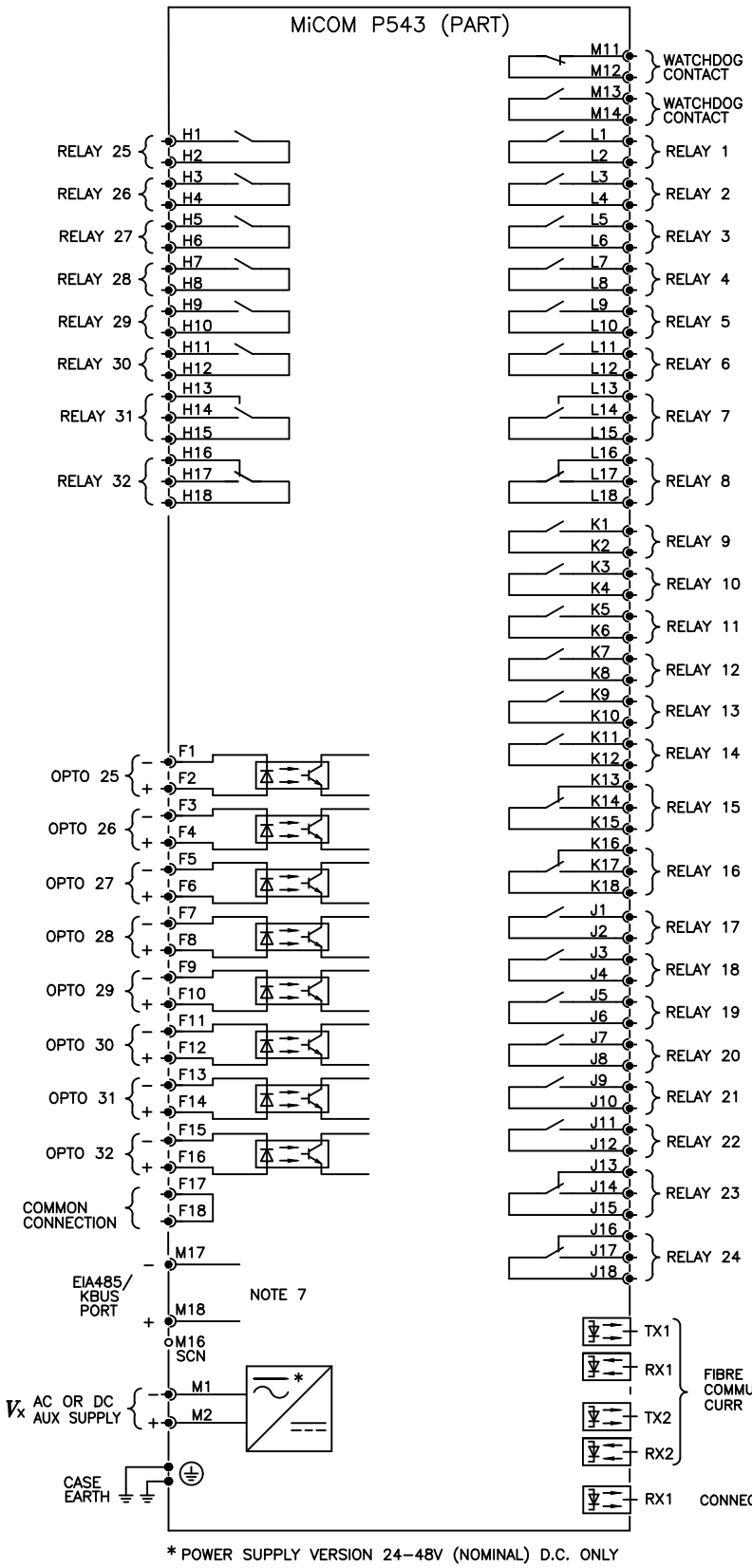
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 32I/24O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54363**	PLM No: A20097256	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

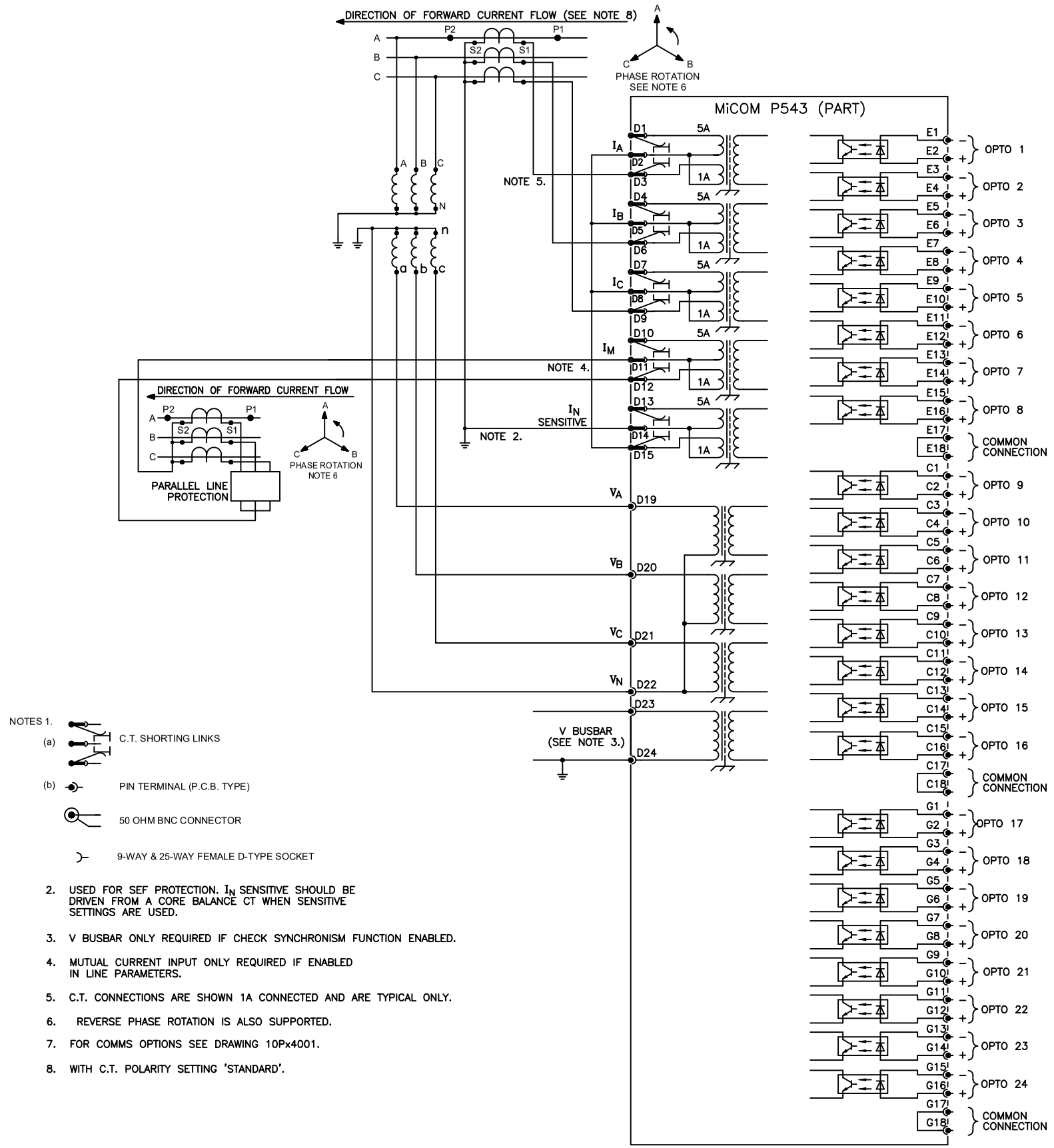
(b) PIN TERMINAL (P.C.B. TYPE)

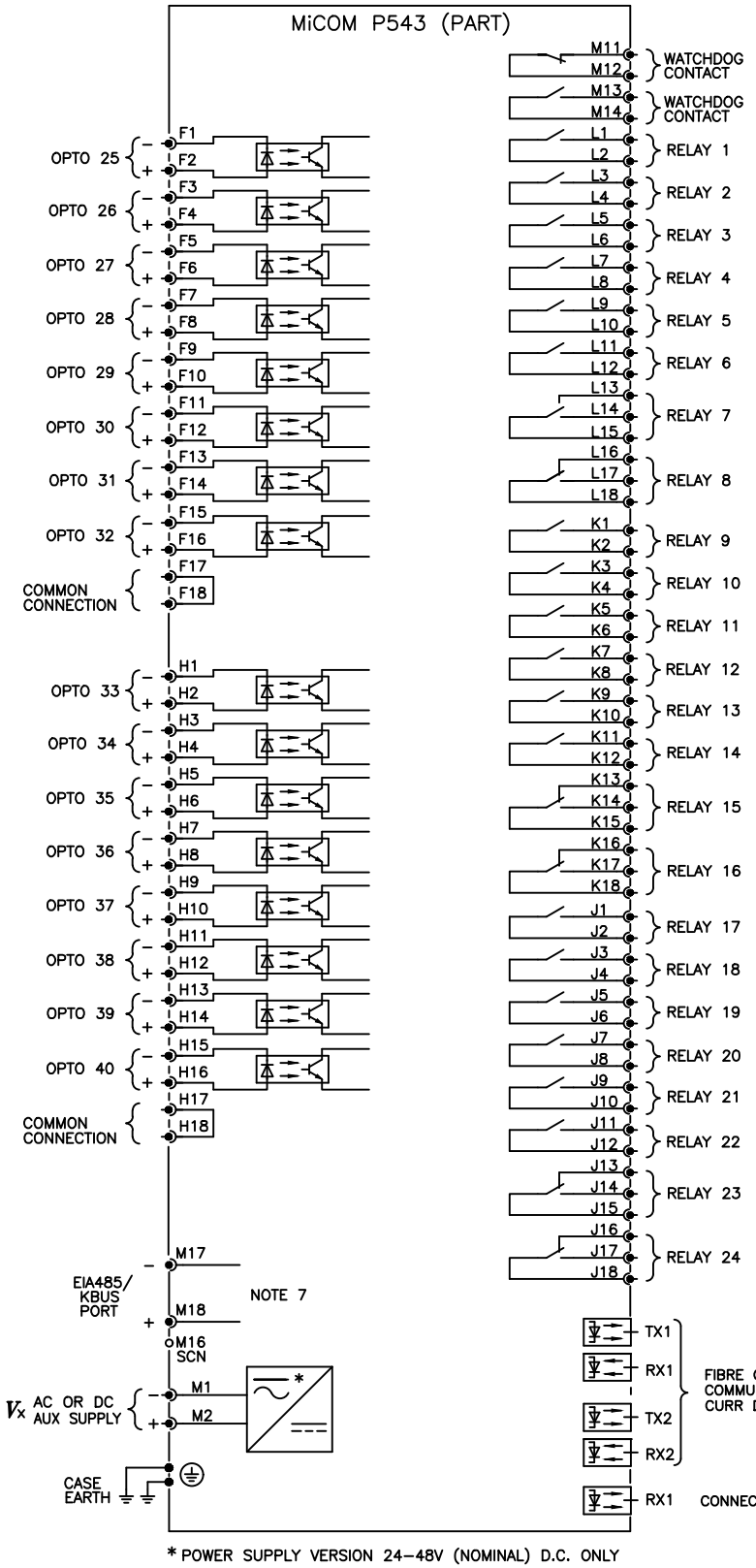
50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

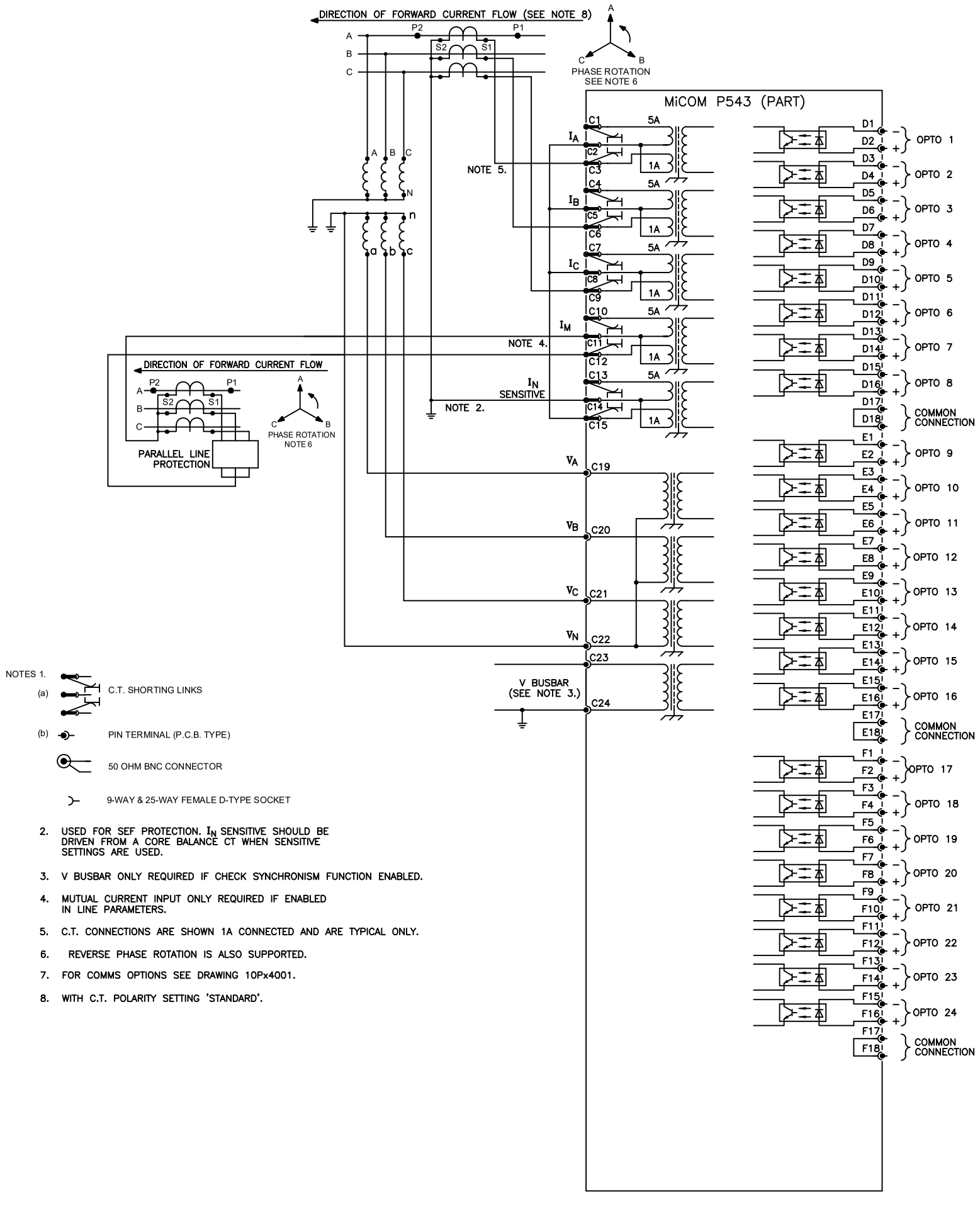
2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

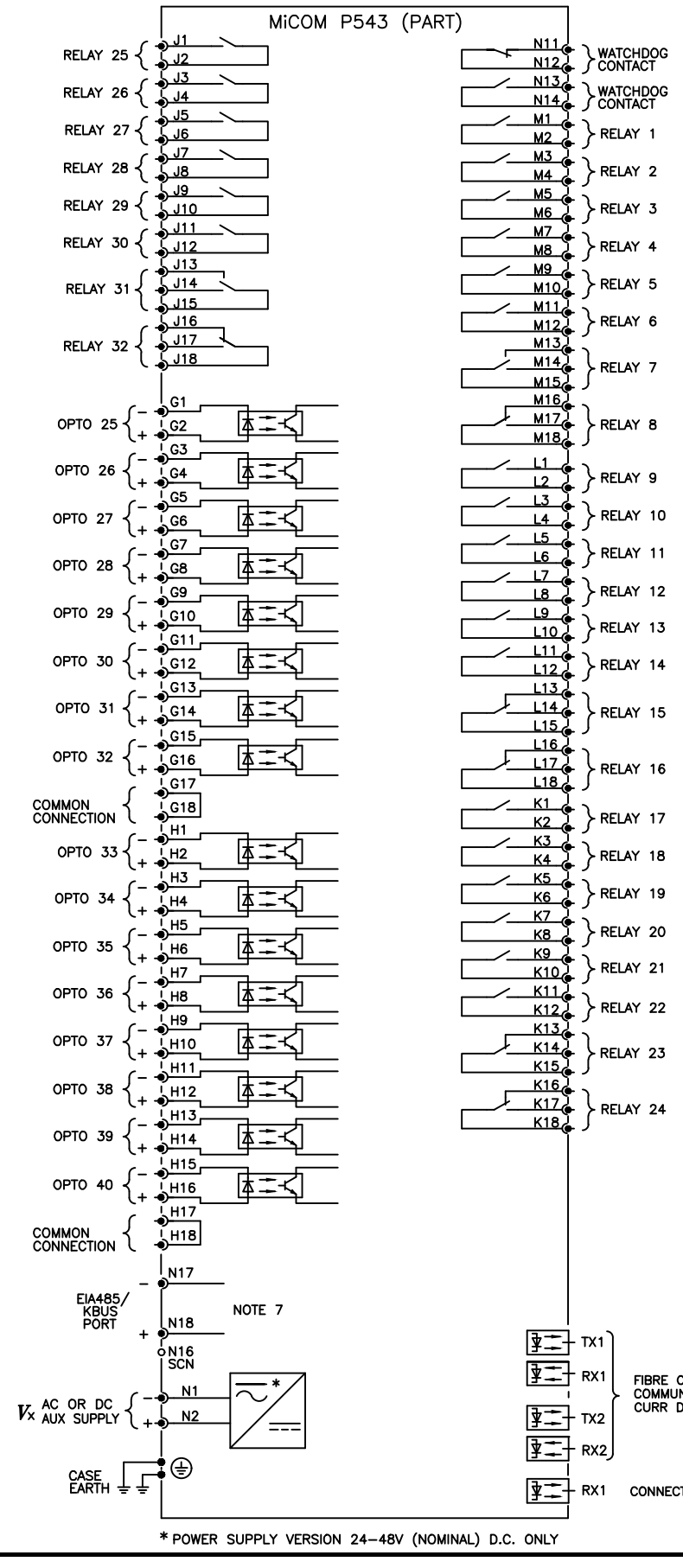
Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 32I/32O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54311**	PLM No: A20076519	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM CURRENT DIFF 3 (80TE) 40I/24O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54312**	PLM No: A20076520	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	





NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

50 OHM BNC CONNECTOR

9-WAY & 25-WAY FEMALE D-TYPE SOCKET

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. V BUSBAR ONLY REQUIRED IF CHECK SYNCHRONISM FUNCTION ENABLED.
4. MUTUAL CURRENT INPUT ONLY REQUIRED IF ENABLED IN LINE PARAMETERS.
5. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. WITH C.T. POLARITY SETTING 'STANDARD'.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 40I/32O		
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54364**	PLM No: A20097335	Sht: 1
Date:	Chkd:				Next Sht: -

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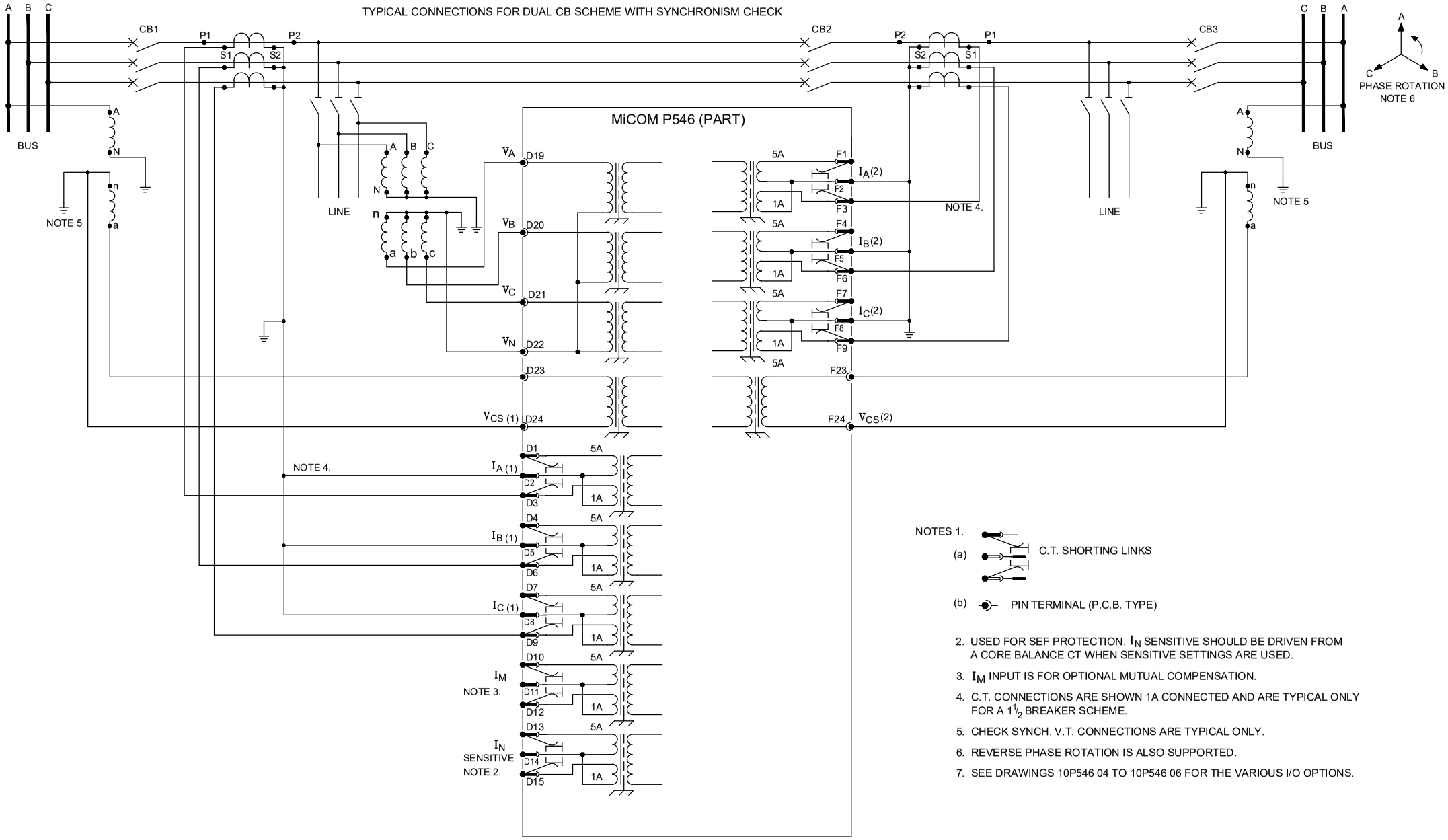
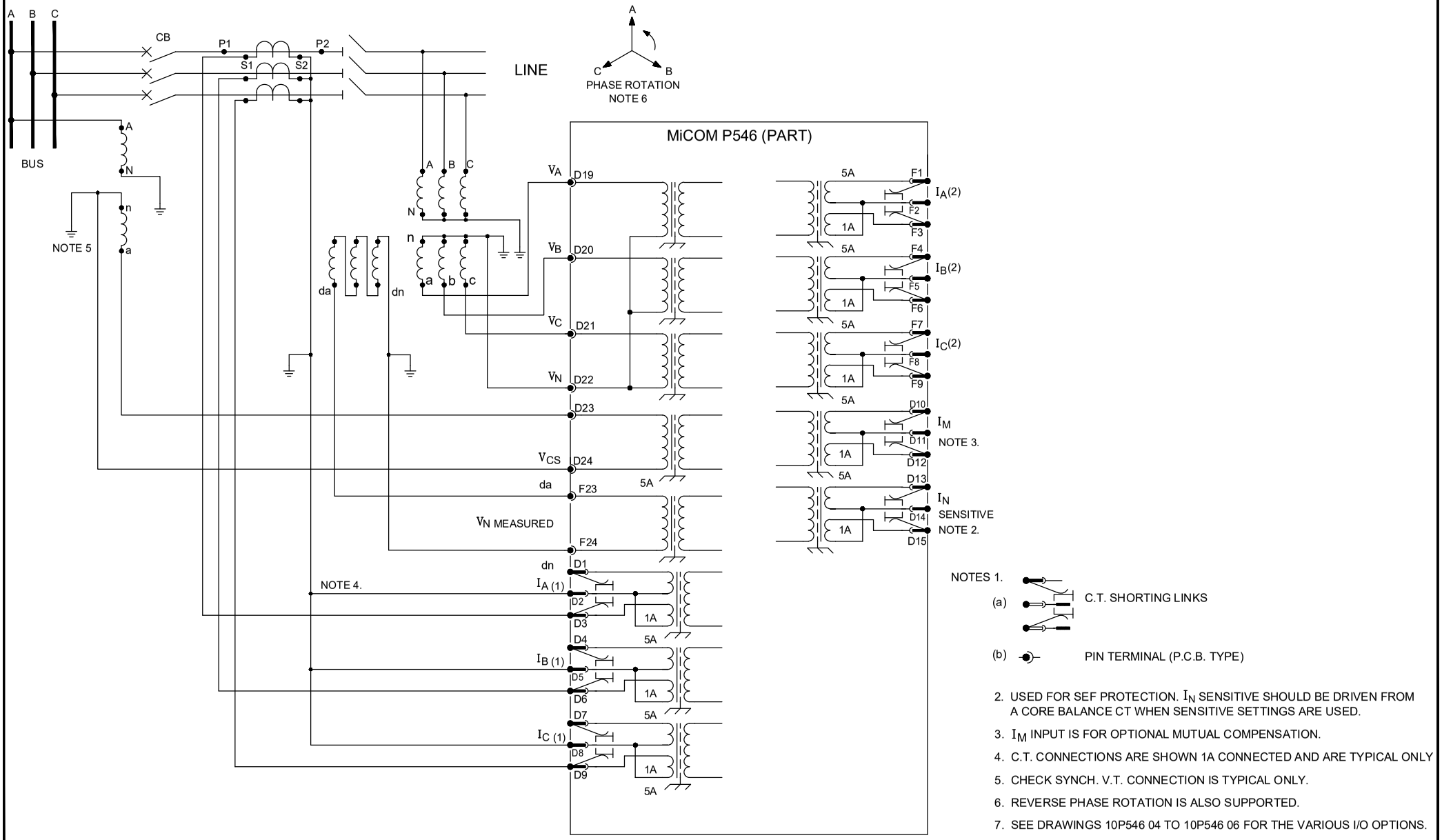


Issue: G	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAG: P546 CURRENT DIFFERENTIAL POWER SYSTEM CONNECTIONS ONLY (80TE)			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54600**	PLM No: A20064877	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: 2	

TYPICAL CONNECTIONS FOR SINGLE CB SCHEME WITH SYNCHRONISM CHECK AND MEASURED RESIDUAL VOLTAGE



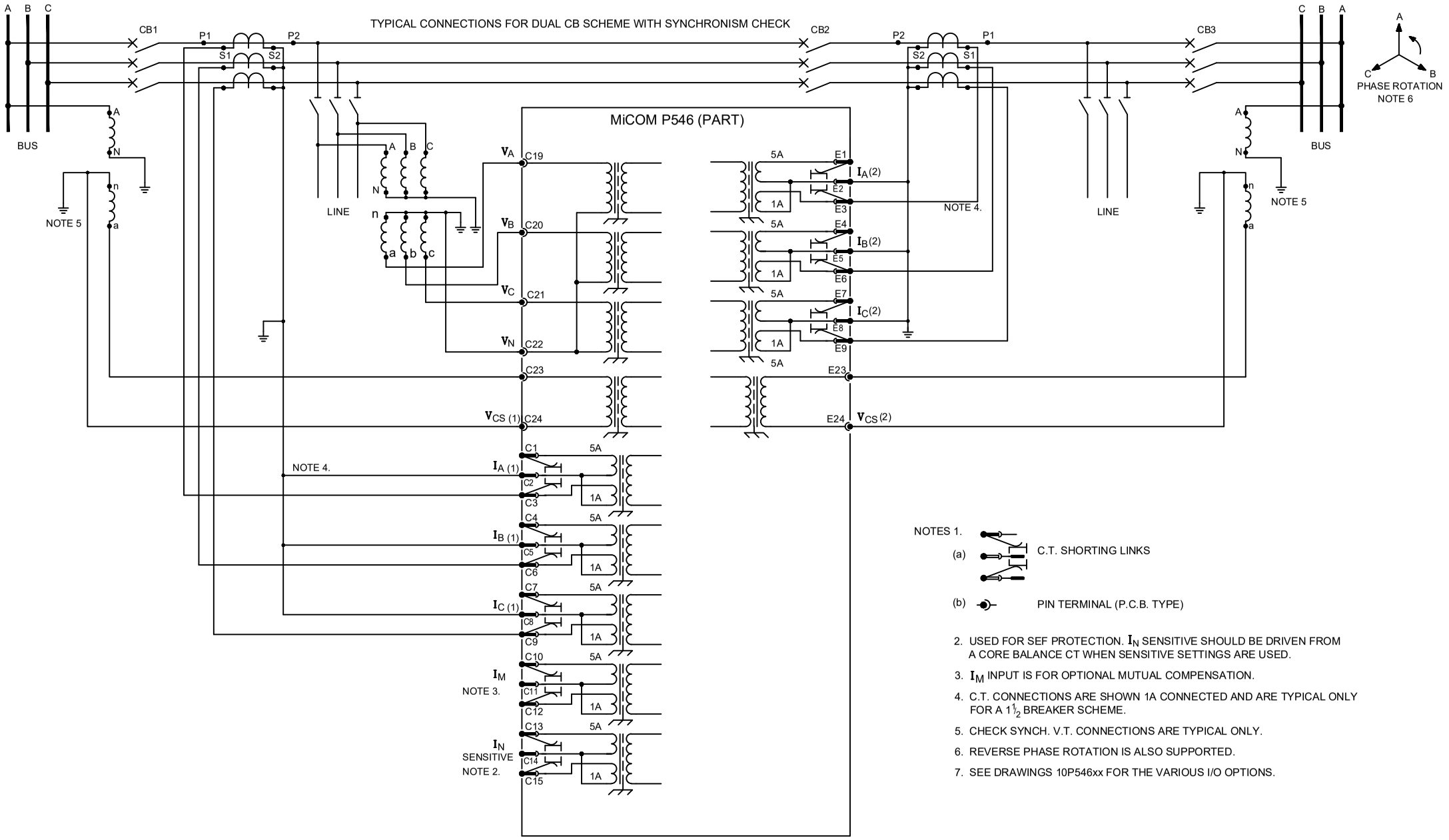
NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. I_M INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY
5. CHECK SYNCH. V.T. CONNECTION IS TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. SEE DRAWINGS 10P546 04 TO 10P546 06 FOR THE VARIOUS I/O OPTIONS.

Issue: E	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAG:P546 CURRENT DIFFERENTIAL POWER SYSTEM CONNECTIONS ONLY (80TE)			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54600**	PLM No: A20065260	Sht: 2	GE VERNOVA
Date:	Chkd:				Next Sht: 3	



NOTES 1.

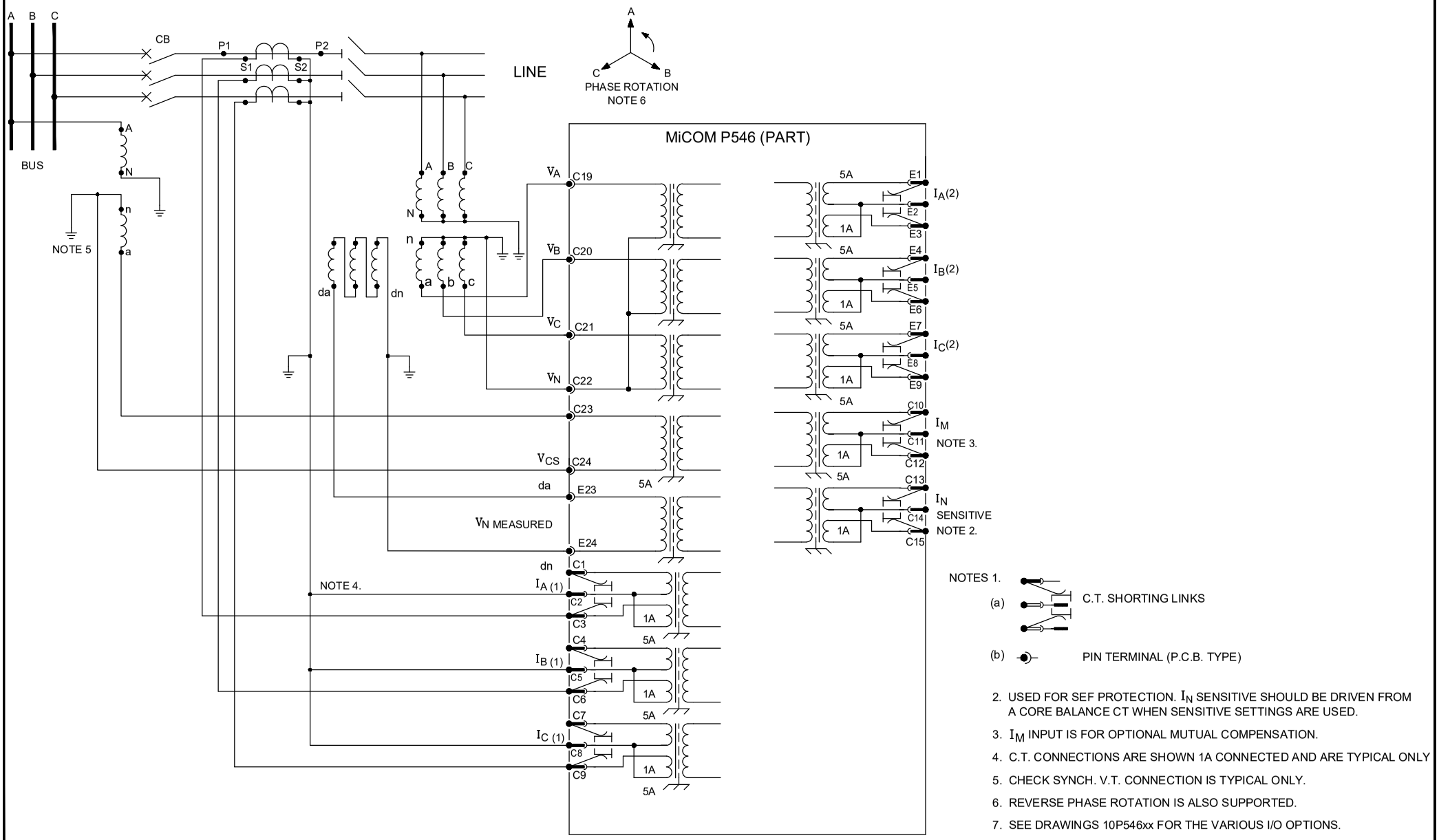
(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. I_M INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY FOR A $1\frac{1}{2}$ BREAKER SCHEME.
5. CHECK SYNCH. V.T. CONNECTIONS ARE TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. SEE DRAWINGS 10P546xx FOR THE VARIOUS I/O OPTIONS.

Issue: A	Status: **Stage Reviewed**	Revision Notes: CID009162 Initial issue	Title: EXTERNAL CONNECTION DIAG: P544 CURRENT DIFFERENTIAL POWER SYSTEM CONNECTIONS ONLY (60TE)			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54600**	PLM No: A20134786	Sht: 3	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: 4	

TYPICAL CONNECTIONS FOR SINGLE CB SCHEME WITH SYNCHRONISM CHECK AND MEASURED RESIDUAL VOLTAGE



NOTES 1.

(a) C.T. SHORTING LINKS

(b) PIN TERMINAL (P.C.B. TYPE)

2. USED FOR SEF PROTECTION. I_N SENSITIVE SHOULD BE DRIVEN FROM A CORE BALANCE CT WHEN SENSITIVE SETTINGS ARE USED.
3. I_M INPUT IS FOR OPTIONAL MUTUAL COMPENSATION.
4. C.T. CONNECTIONS ARE SHOWN 1A CONNECTED AND ARE TYPICAL ONLY
5. CHECK SYNCH. V.T. CONNECTION IS TYPICAL ONLY.
6. REVERSE PHASE ROTATION IS ALSO SUPPORTED.
7. SEE DRAWINGS 10P546xx FOR THE VARIOUS I/O OPTIONS.

Issue: A	Status: **Approved**	Revision Notes: CID009162 Initial Issue.	Title:	EXTERNAL CONNECTION DIAG:P546 CURRENT DIFFERENTIAL POWER SYSTEM CONNECTIONS ONLY (60TE)		
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No:	**10P54600**	PLM No: A20134787	Sht: 4
Date: 02/12/2025	Chkd: J Hutchins					Next Sht: -
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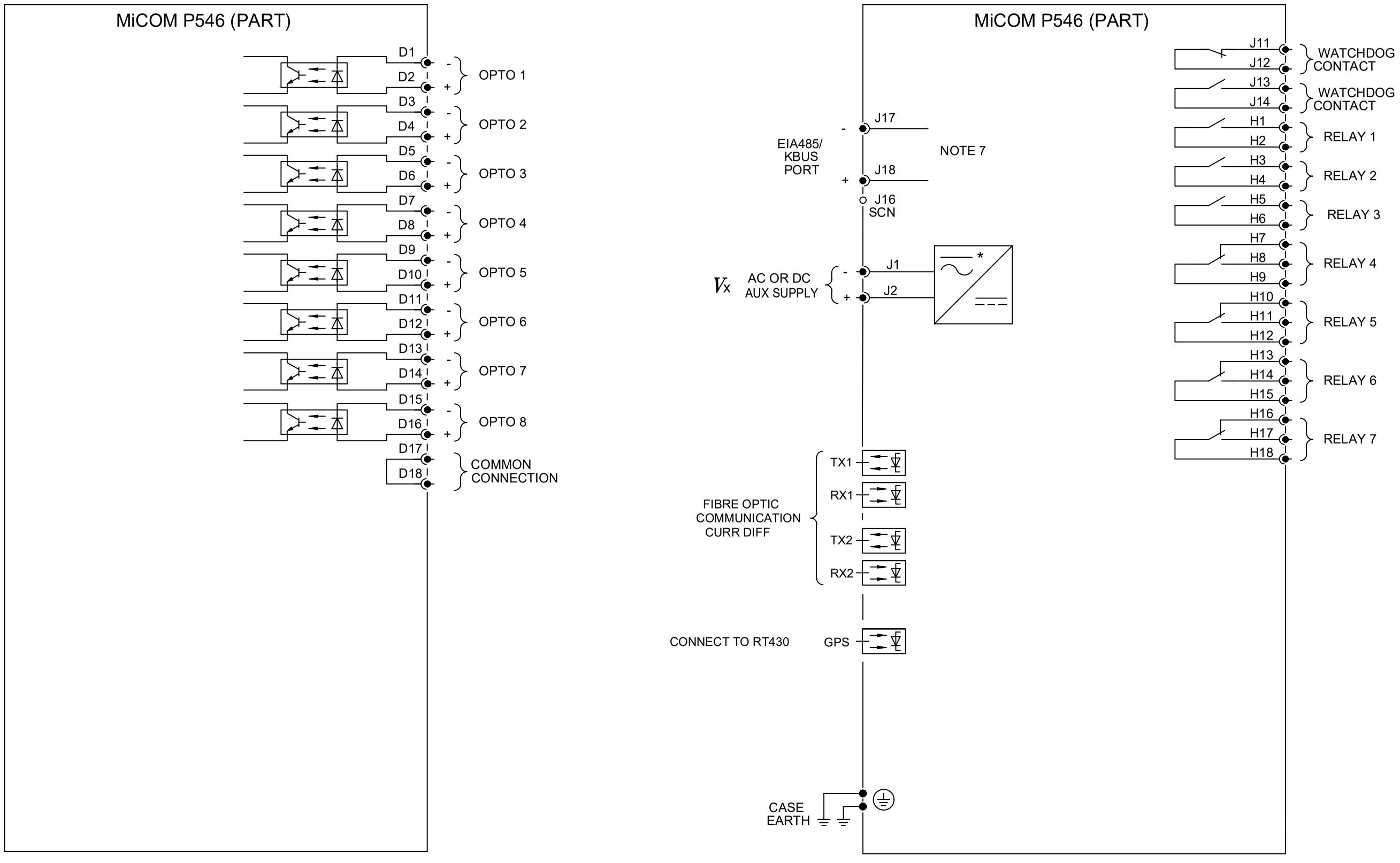
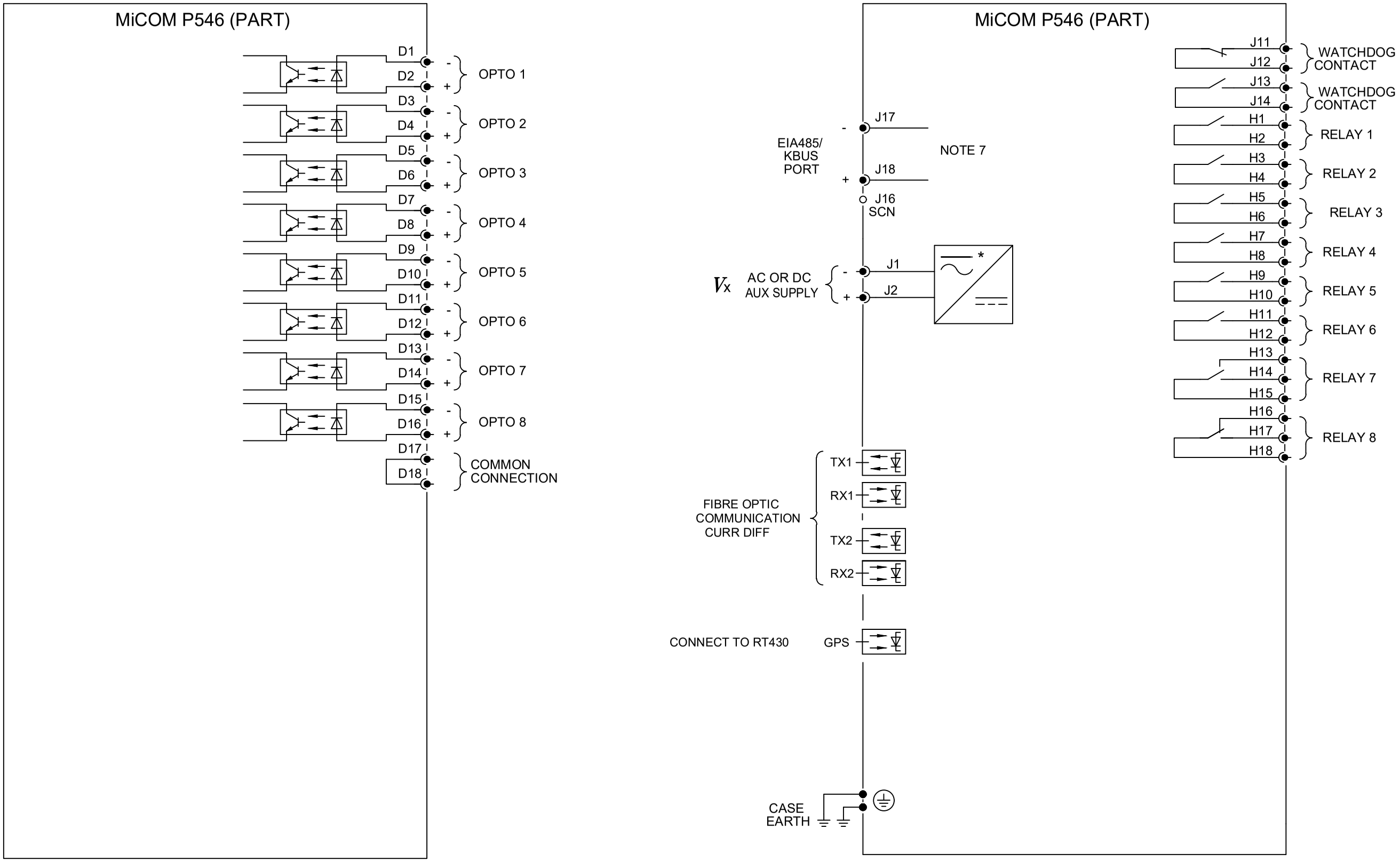


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. FOR POWER SYSTEM CONNECTIONS SEE 10P54600 SHEETS 3 & 4

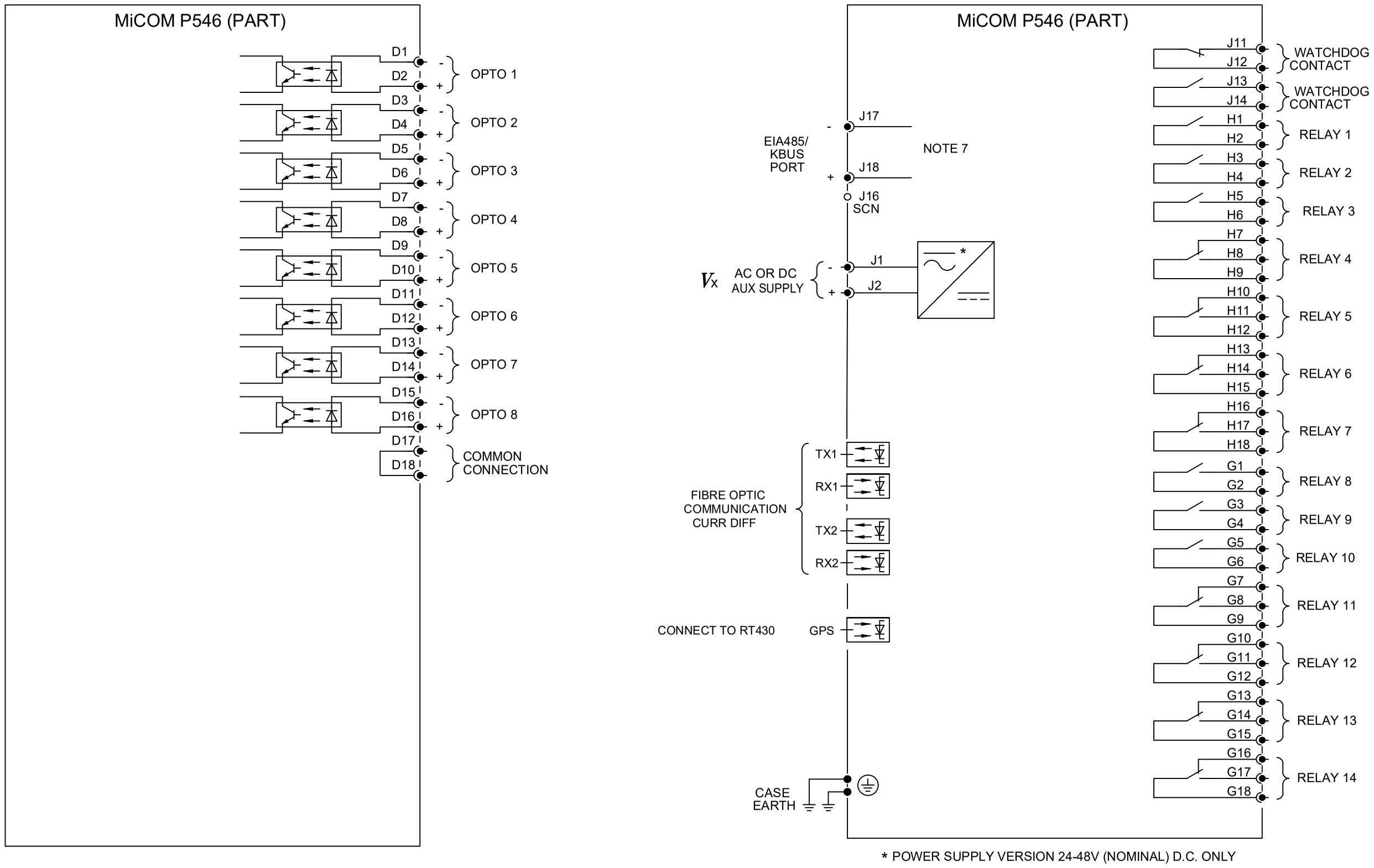
Issue: C	Status: **Approved**	Revision Notes: CID009162. Power system and CTVT connections removed.	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 8I/7O			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54616**	PLM No: A20077815	Sht: 1	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. FOR POWER SYSTEM CONNECTIONS SEE 10P54600 SHEETS 3 & 4

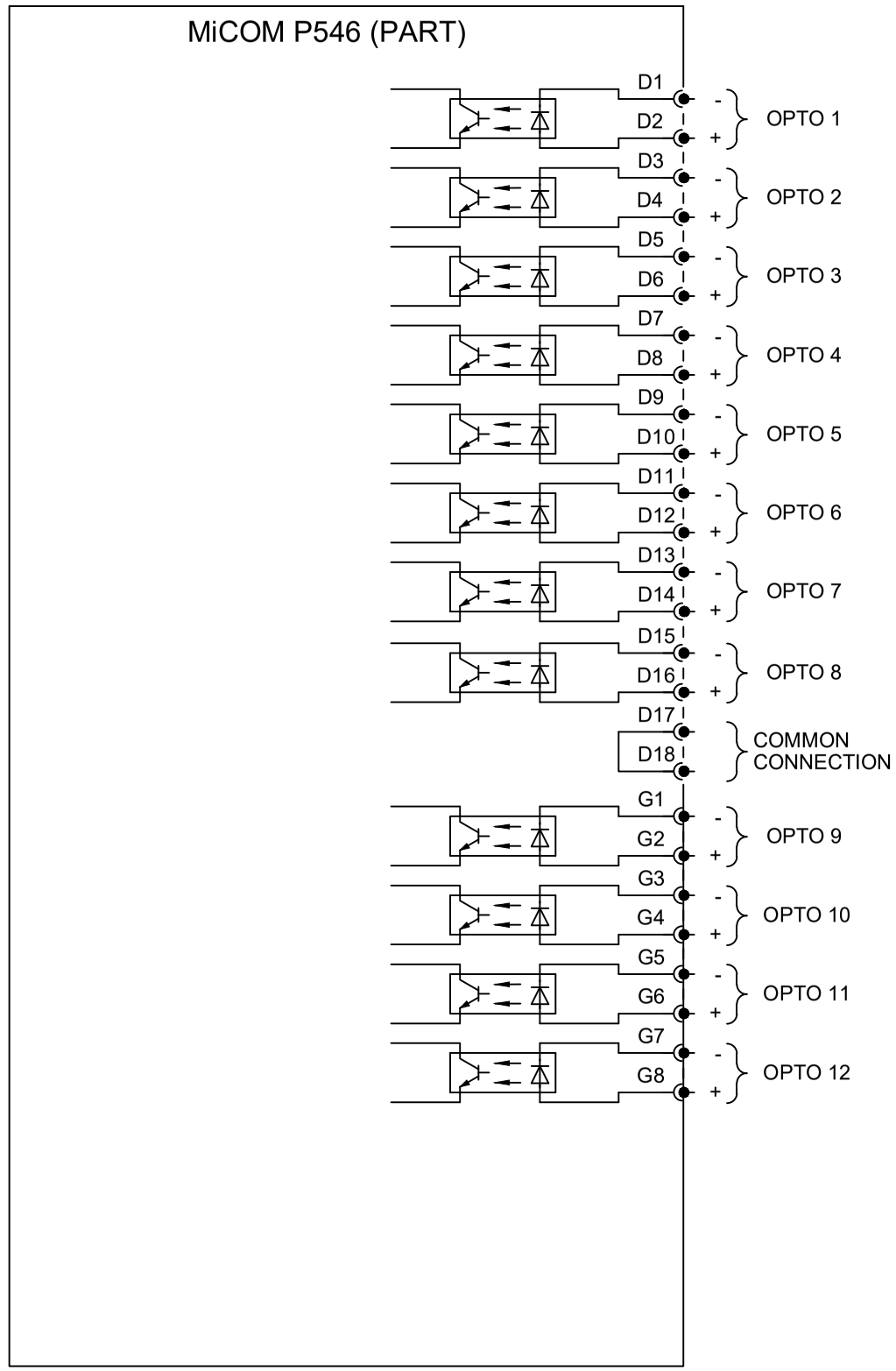
Issue: C	Status: **Approved**	Revision Notes: CID009162. Power system and CTVT connections removed.	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 8I/8O			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54617**	PLM No: A20077816	Sht: 1	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: -	

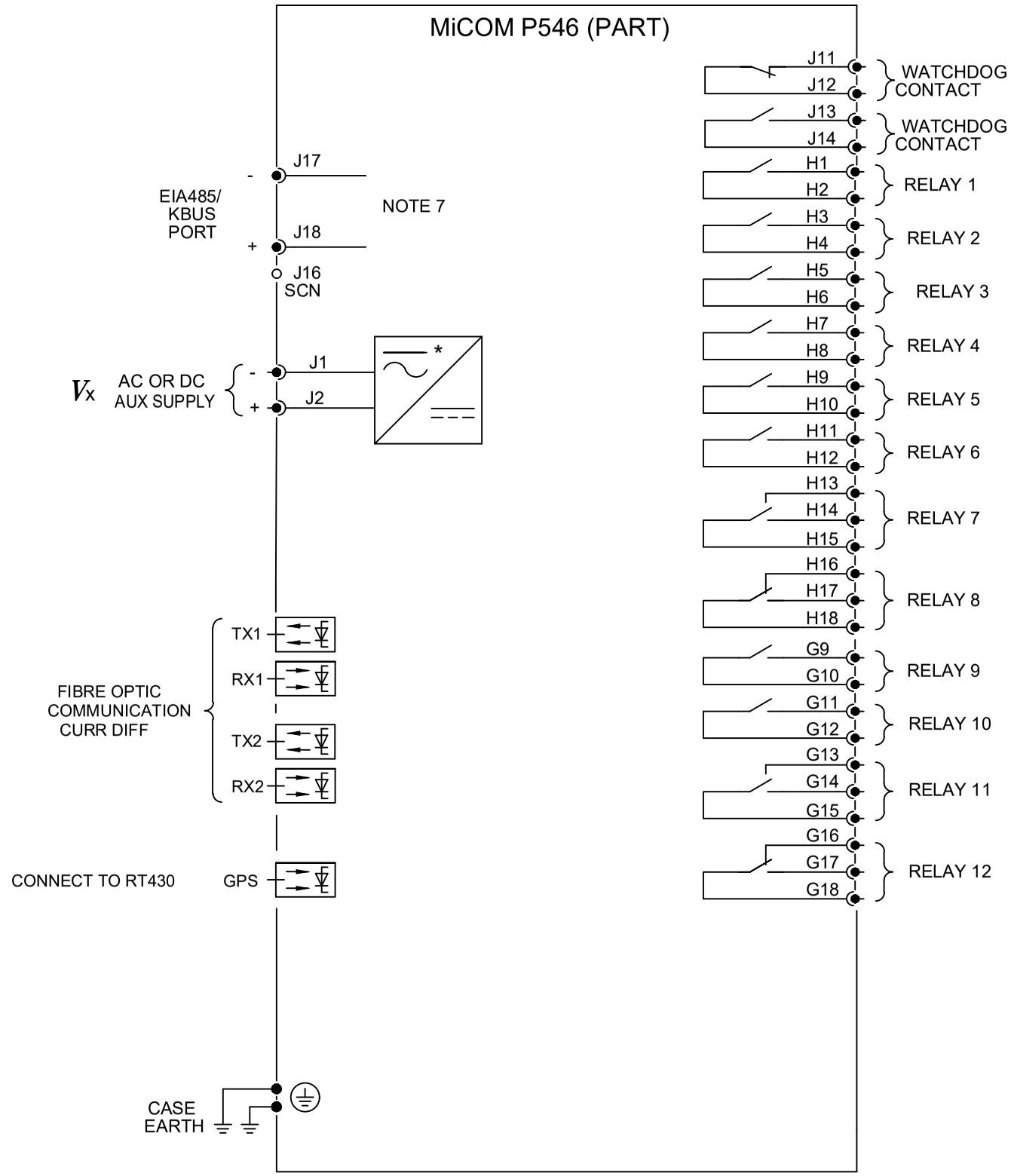


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. FOR POWER SYSTEM CONNECTIONS SEE 10P54600 SHEETS 3 & 4

Issue: C	Status: **Stage Review**	Revision Notes: CID009162. Power system and CTVT connections removed.	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 8I/14O			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54618**	PLM No: A20077817	Sht: 1	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: -	

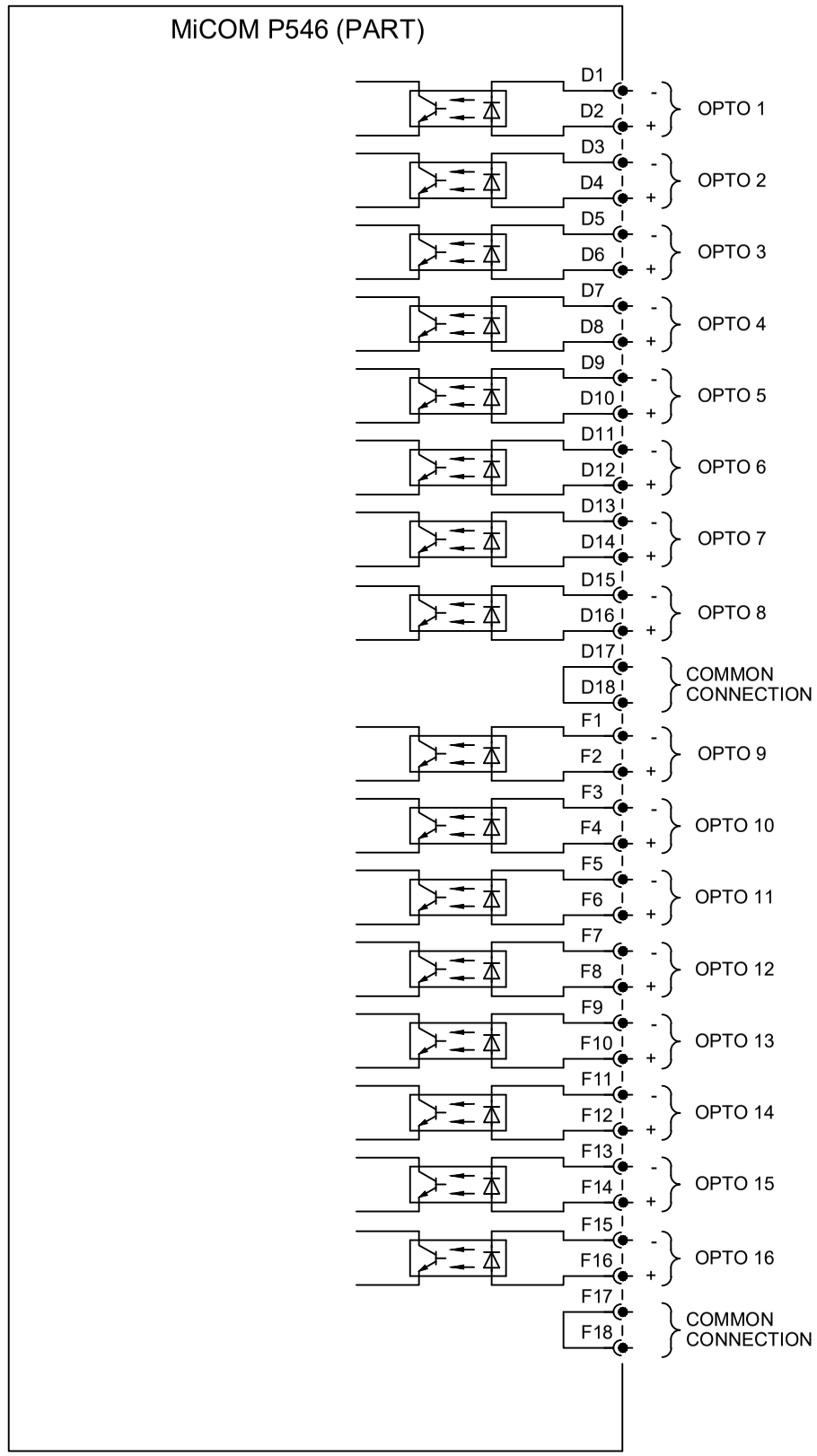


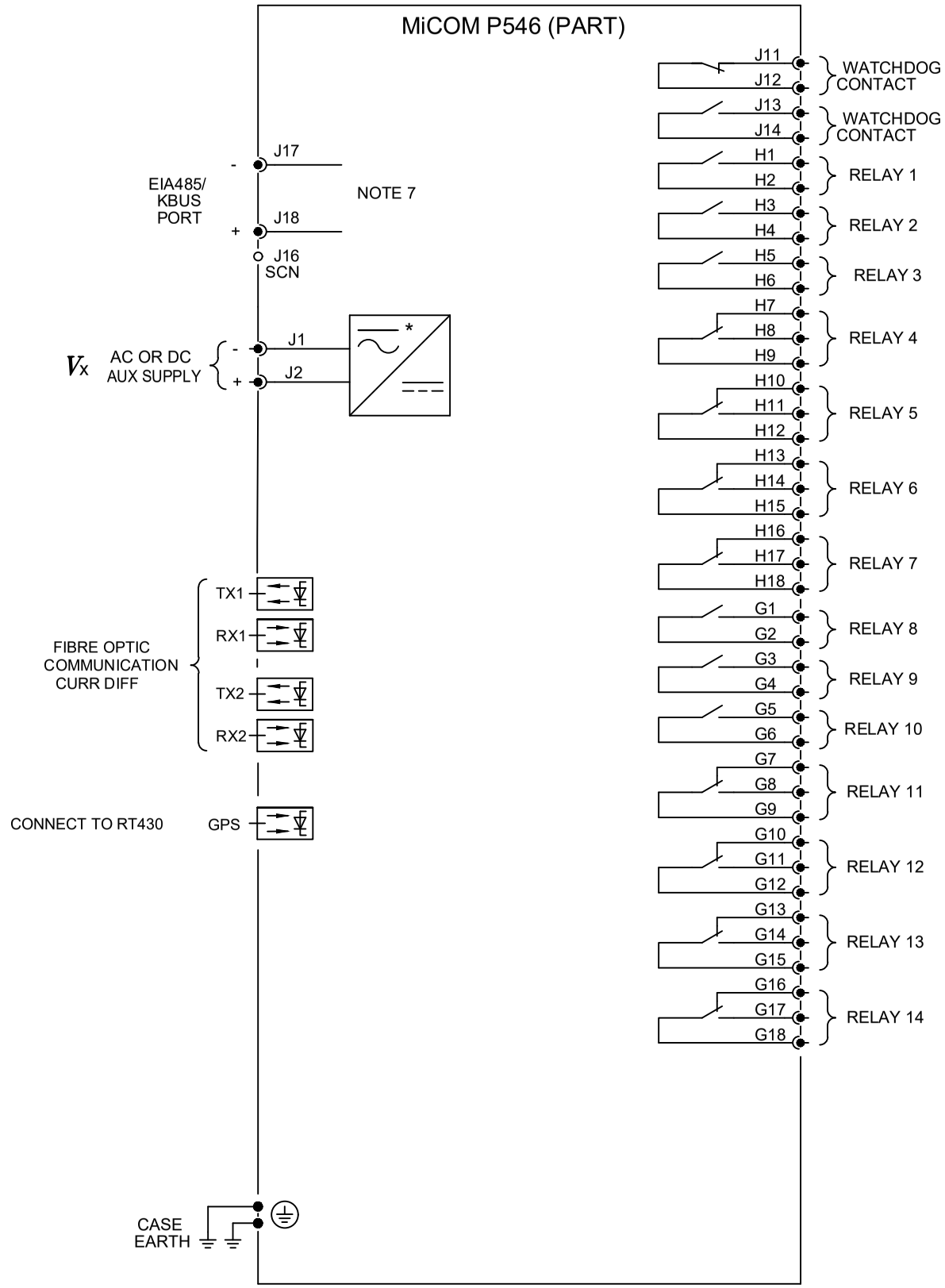


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. FOR POWER SYSTEM CONNECTIONS SEE 10P54600 SHEETS 3 & 4

Issue: C	Status: **Stage Review**	Revision Notes: CID009162. Power system and CTVT connections removed.	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 12I/12O			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54619**	PLM No: A20077818	Sht: 1	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: -	

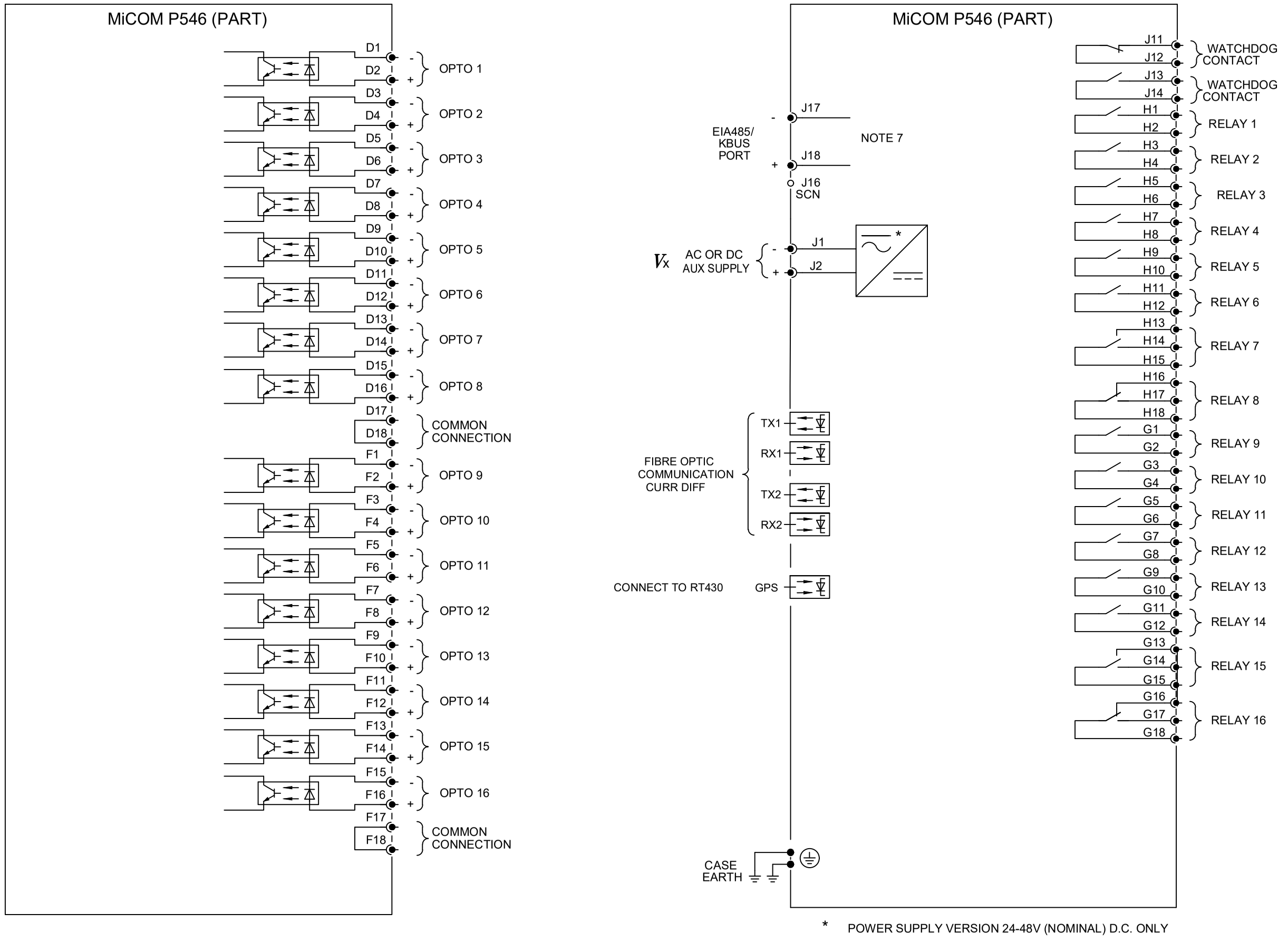




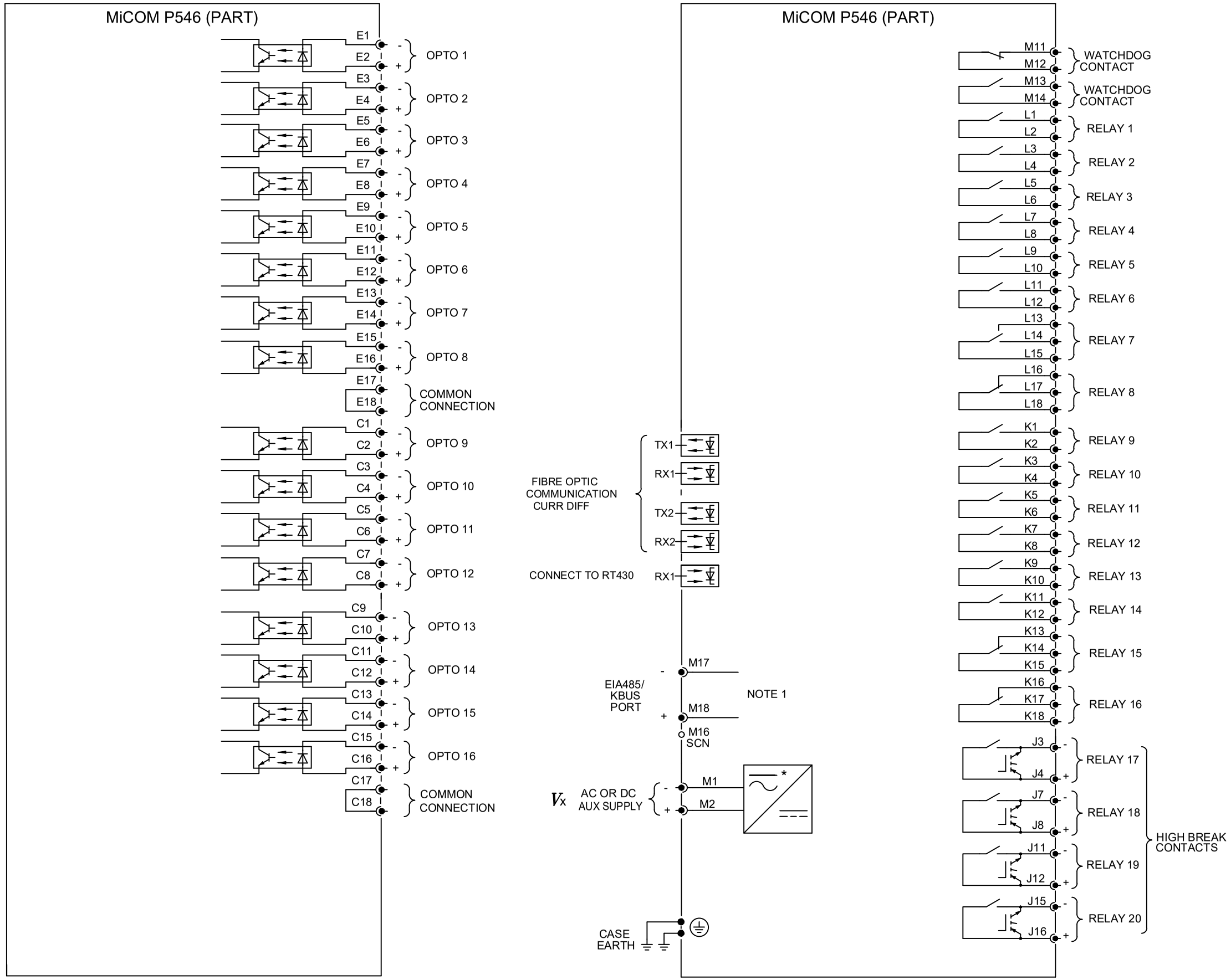
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. FOR POWER SYSTEM CONNECTIONS SEE 10P54600 SHEETS 3 & 4

Issue: C	Status: **Approved**	Revision Notes: CID009162. Power system and CTVT connections removed.	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) 16I/14O			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54620**	PLM No: A20077819	Sht: 1	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: -	



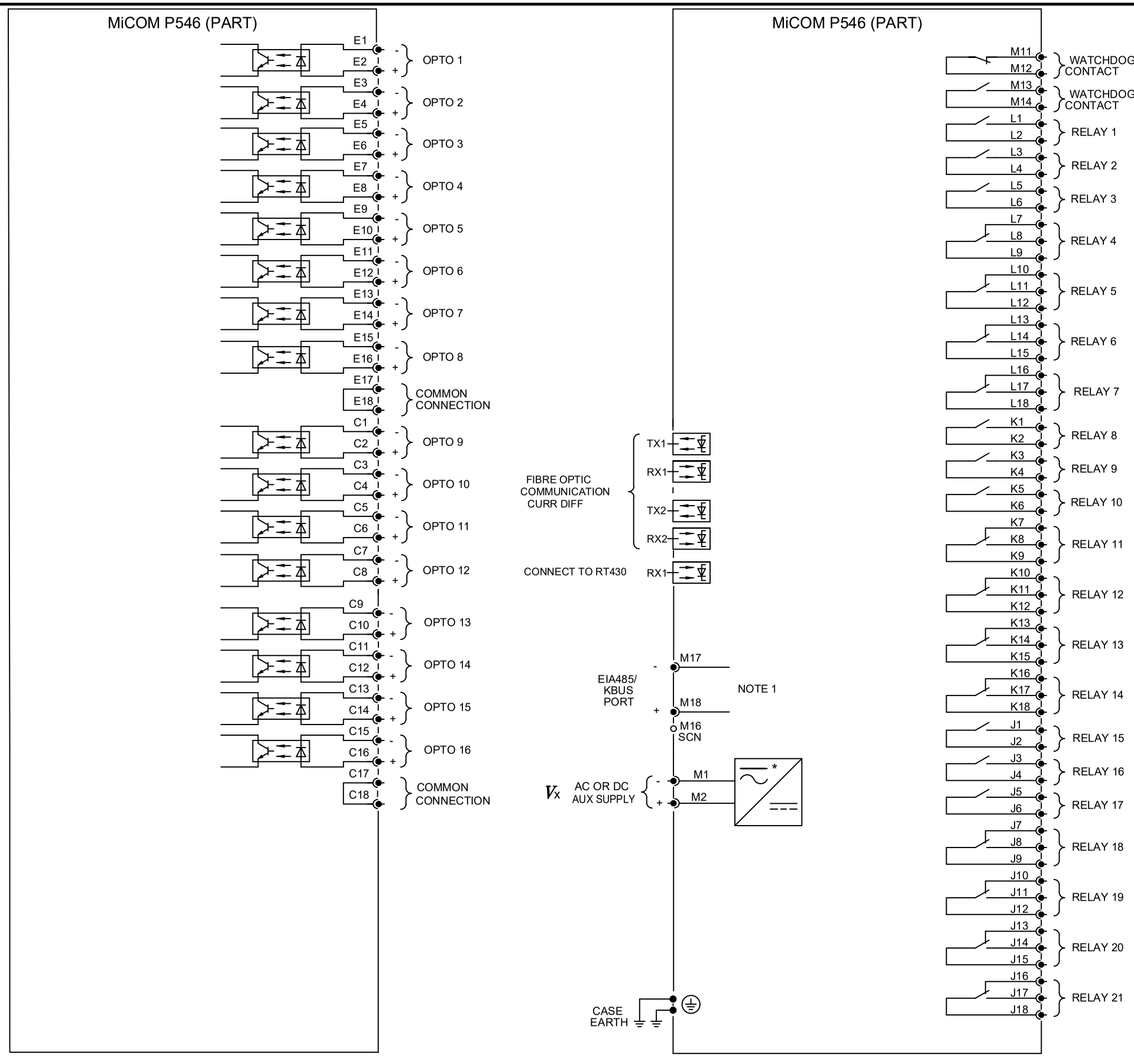
Issue: C	Status: **Approved**	Revision Notes: CID009162. Power system and CTVT connections removed.	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (60TE) DISTANCE PROTECTION			
Date: 02/12/2025	Name: S Wootton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54621**	PLM No: A20077820	Sht: 1	GE VERNOVA
Date: 02/12/2025	Chkd: J Hutchins				Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

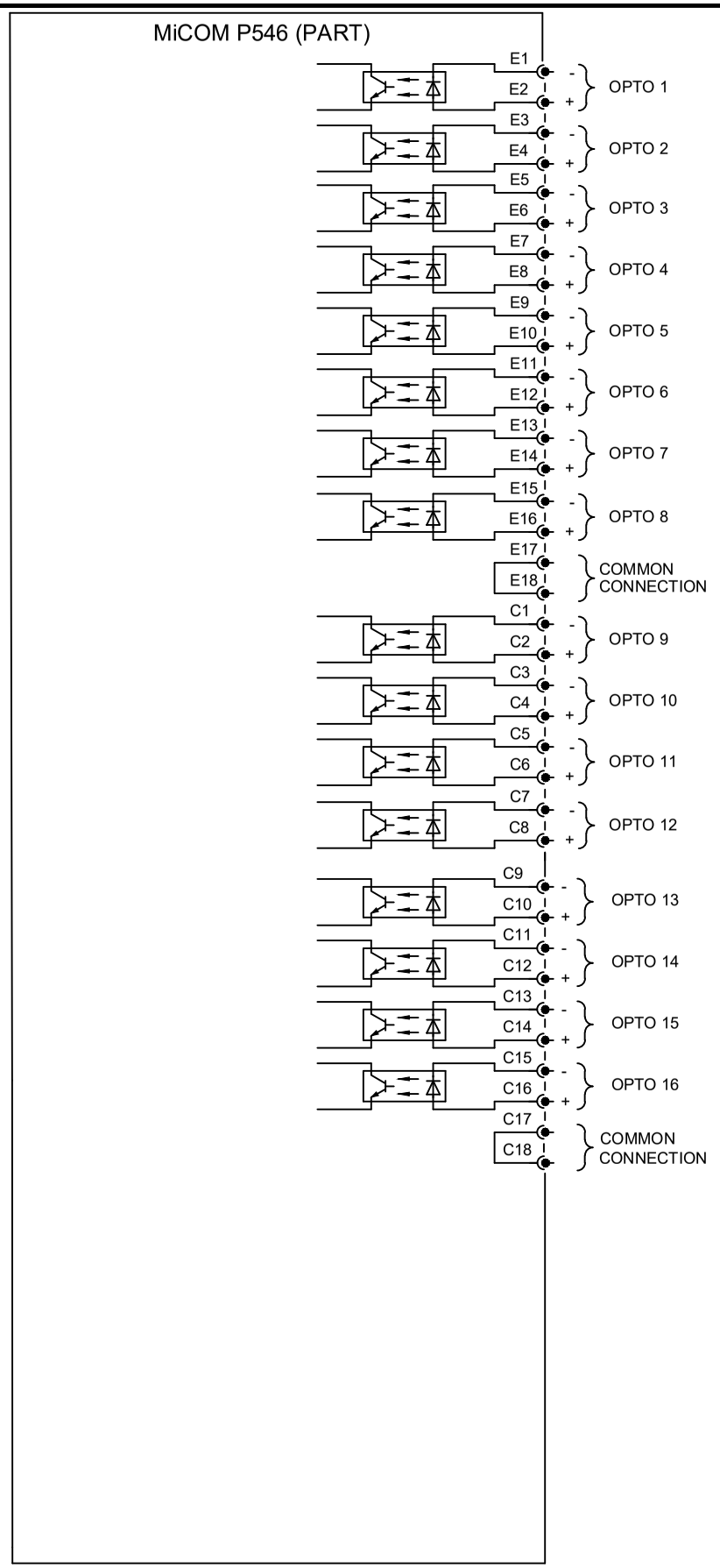
Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 16I/16O + 4 HIGH SPEED HIGH BREAK RELAYS			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54611**	PLM No: A20076909	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	

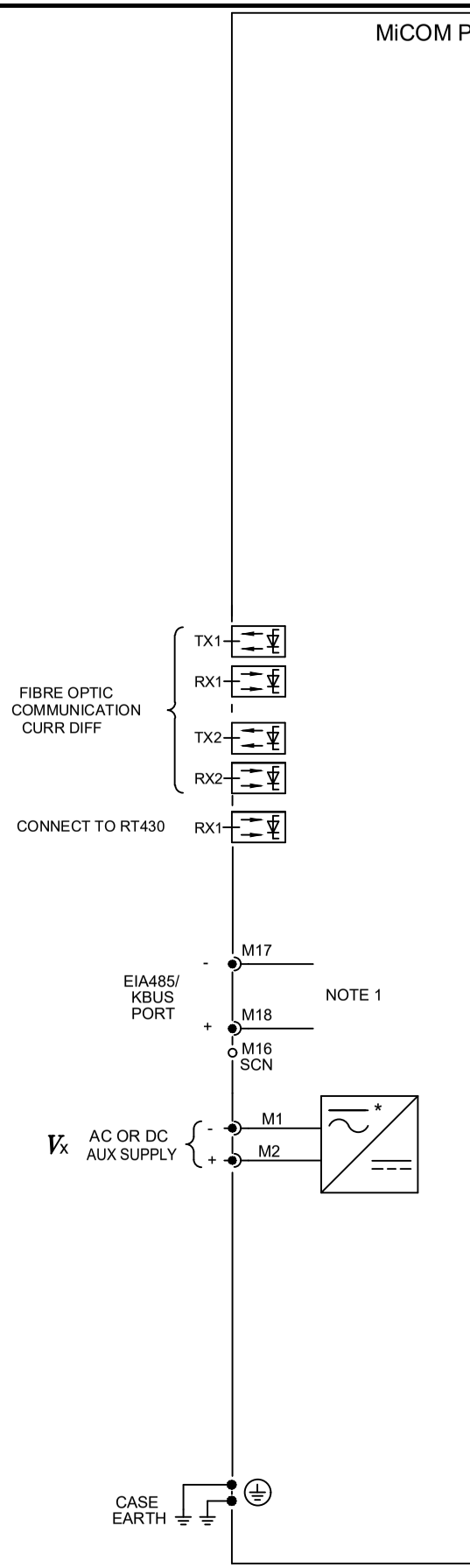


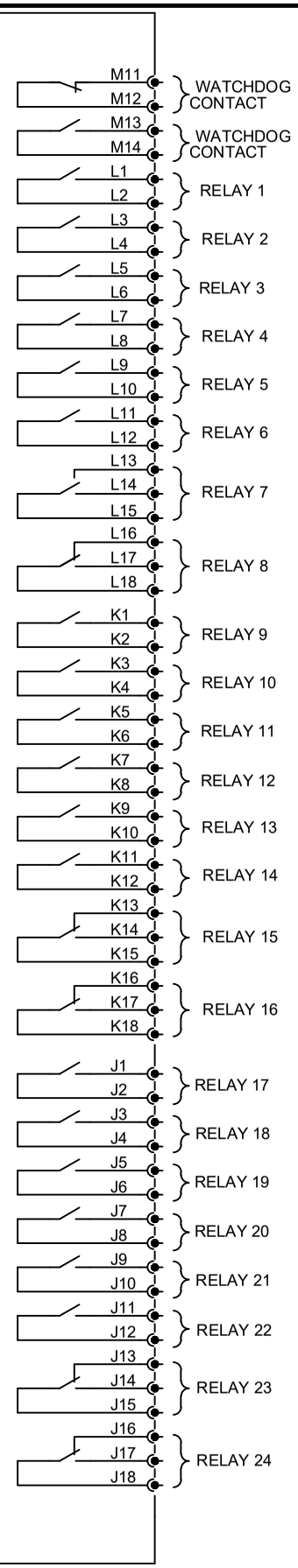
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: C	Status: **In Work**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 16I/21O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54612**	PLM No: A20076910	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



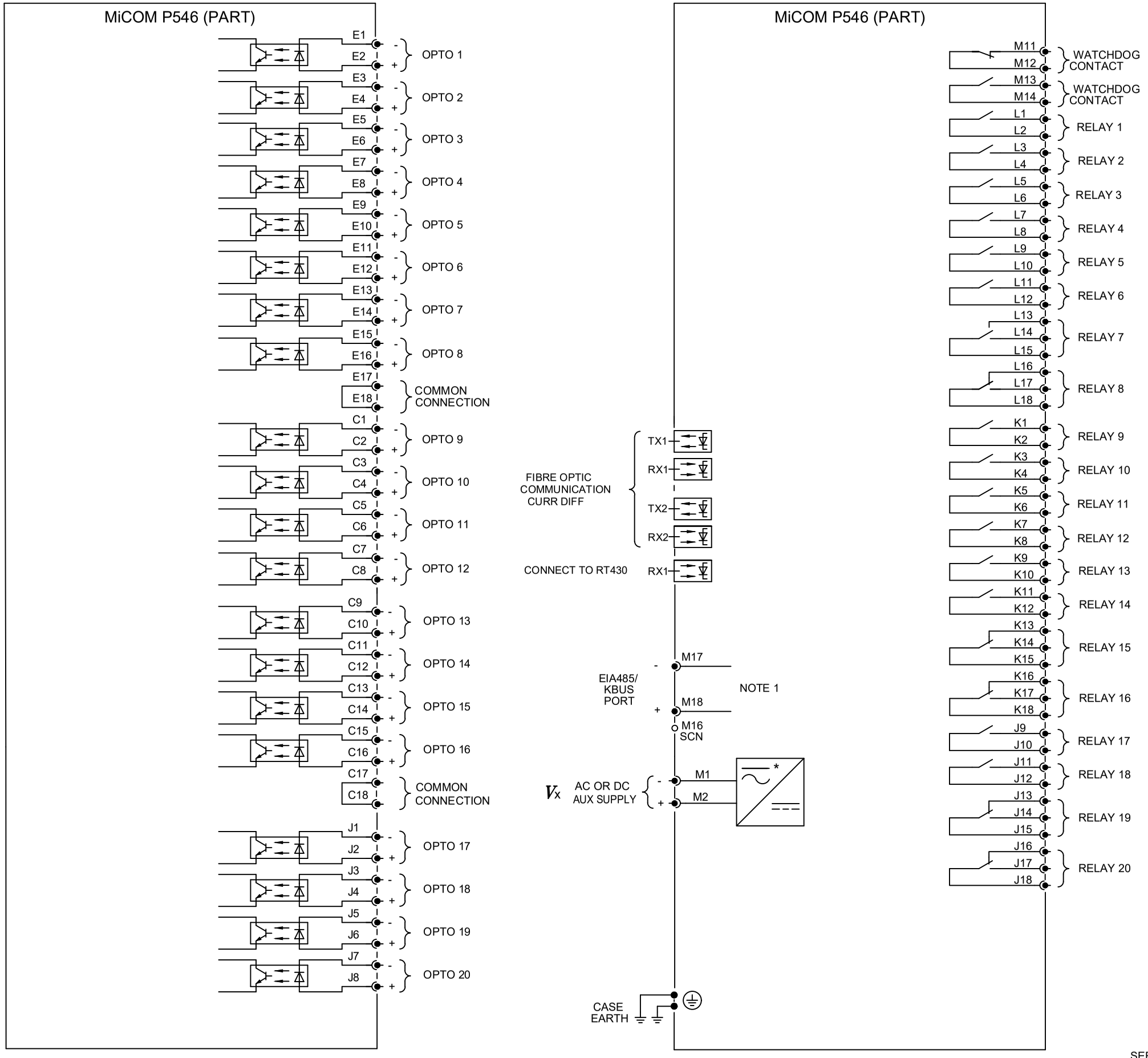




* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 16I/24O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54613**	PLM No: A20076911	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



SEE 10P54600 FOR POWER SYSTEM CONNECTIONS.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 20I 20O			
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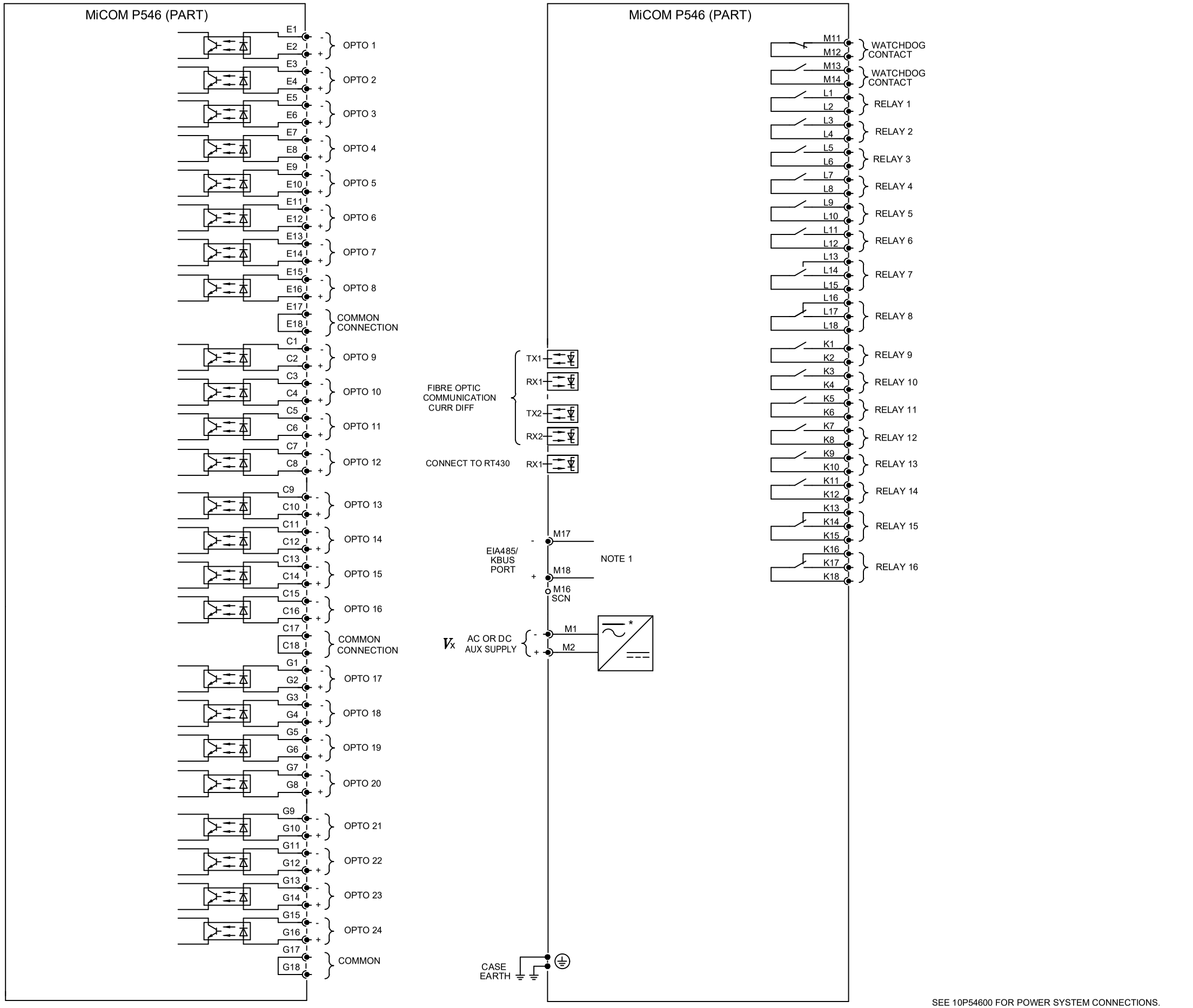
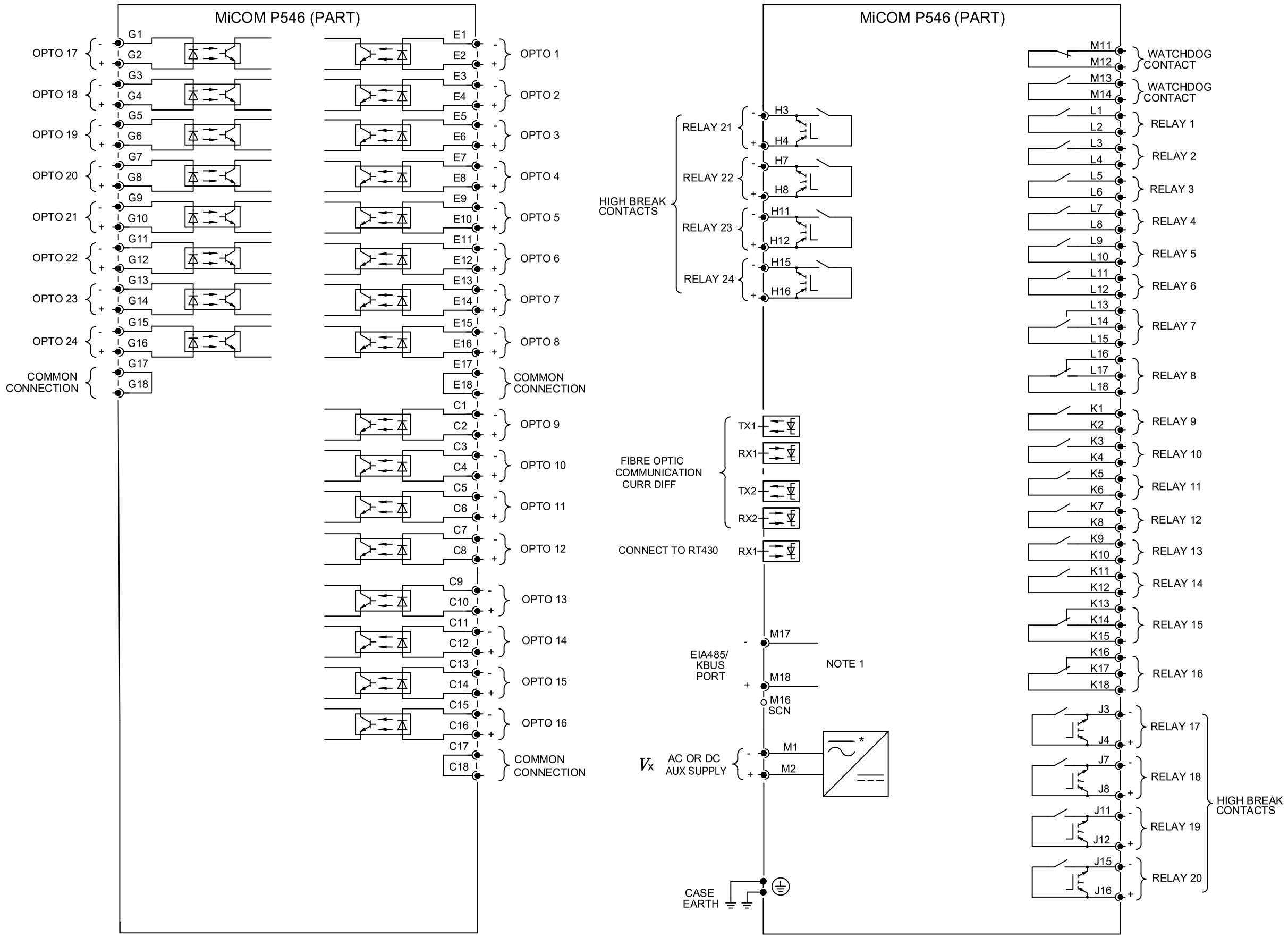
Date:	Chkd:				Next Sht: -	



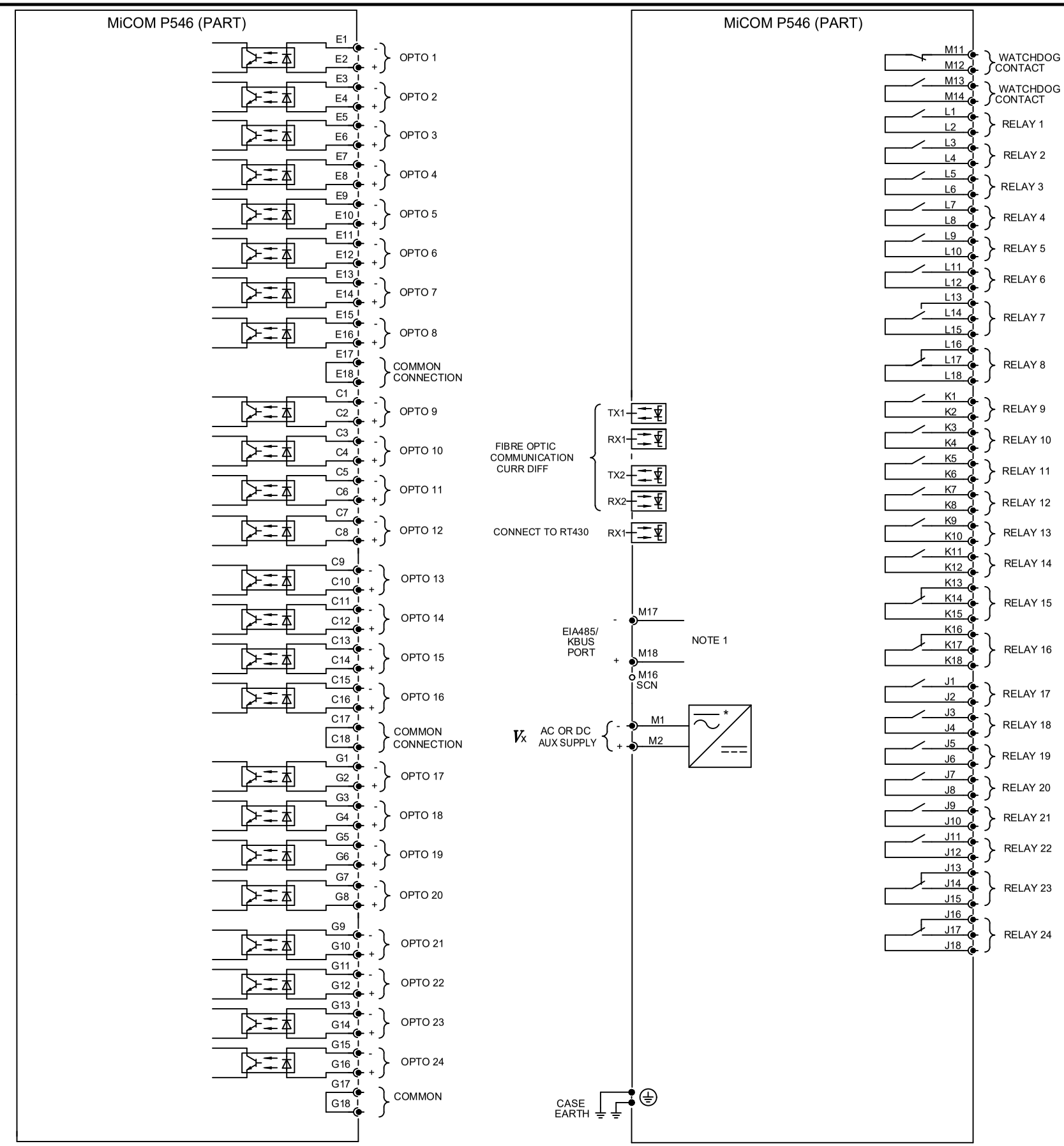
Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I/16O			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54660**	PLM No: A20096995	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: B	Status: **In Work**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I/16O + 8 HIGH SPEED HIGH BREAK RELAYS			
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54614**	PLM No: A20076912	Sht: 1	GE VERNOVA
Date:	Chkd:				Next Sht: -	



Issue: B	Status: **In Work**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I24O			
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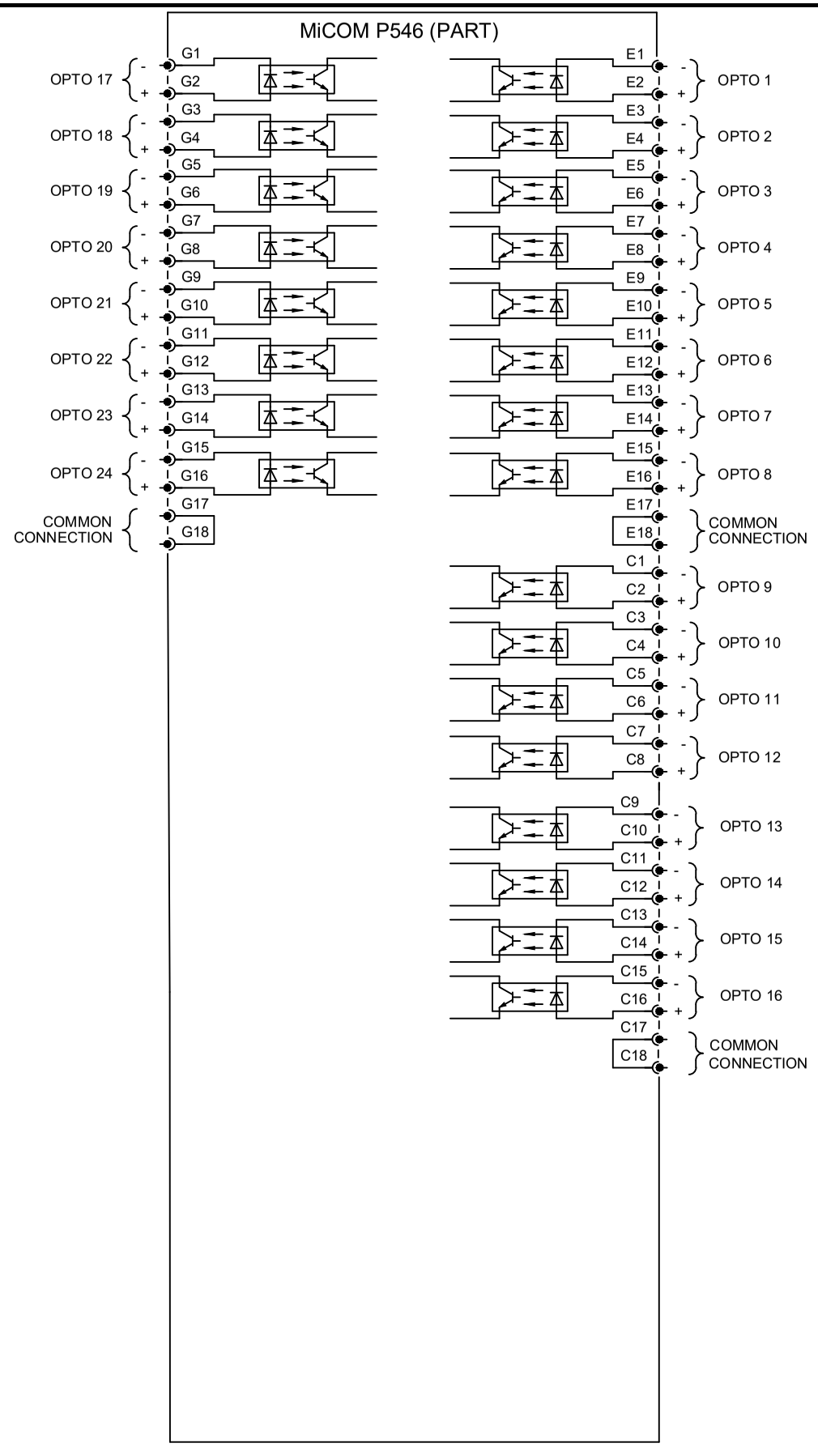

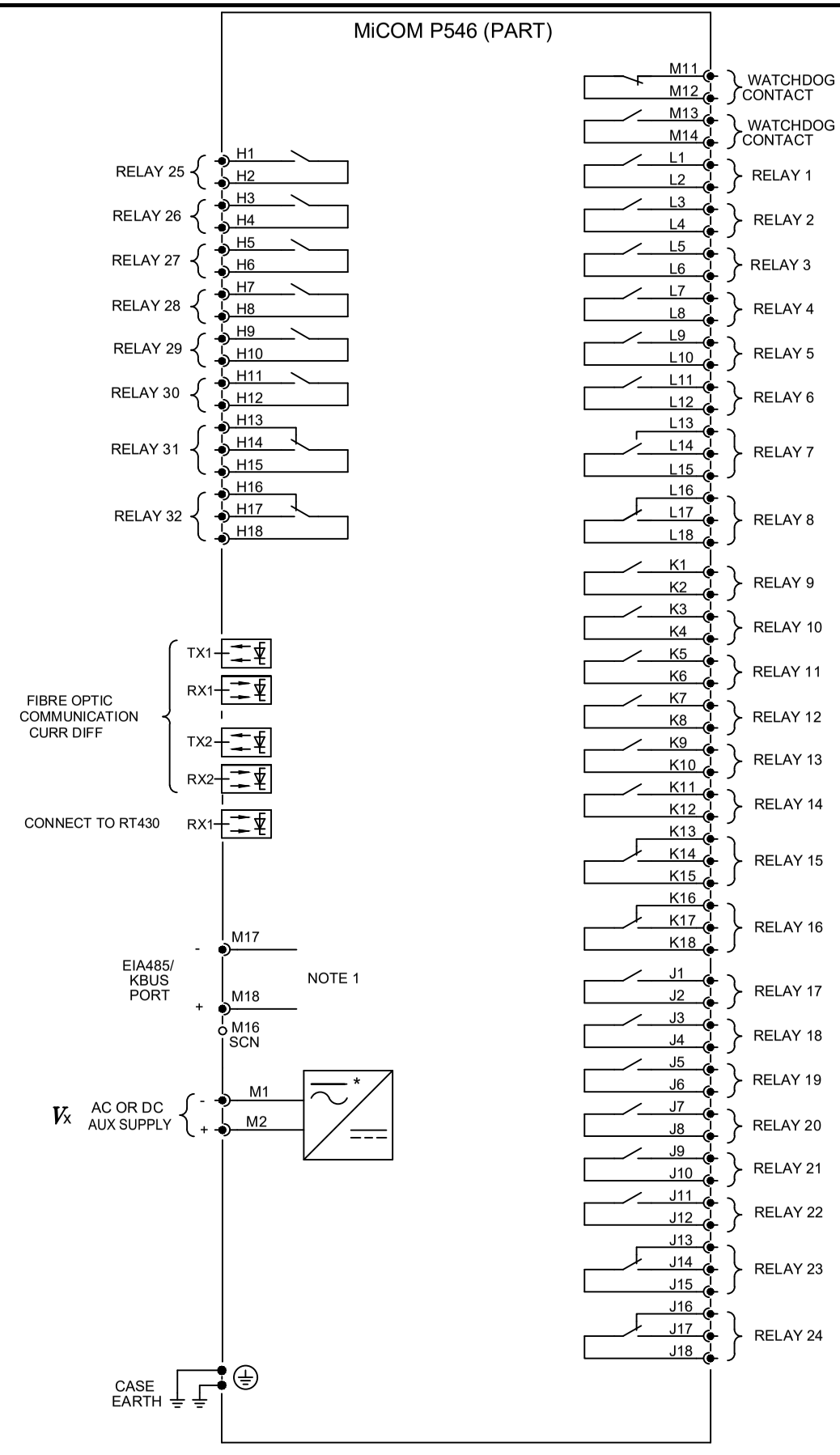

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 24I/32O			
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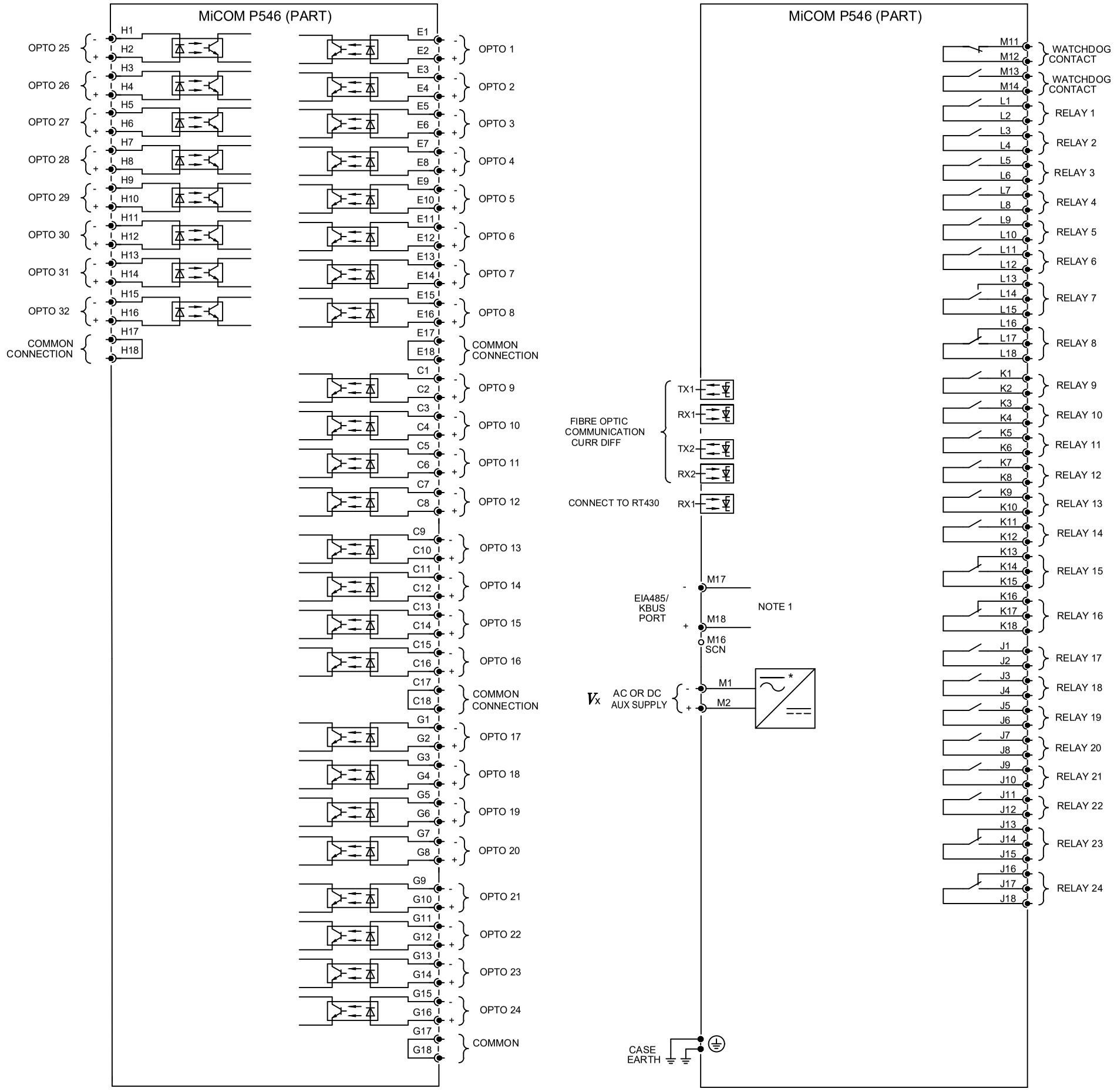
Date:	Chkd:				Next Sht: -	



* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

1. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
2. PIN TERMINAL (PCB TYPE)

SEE 10P54600 FOR POWER SYSTEM CONNECTIONS.

Issue: B	Status: **Approved**	Revision Notes: CID008567 - Outline update only	Title: EXTERNAL CONNECTION DIAGRAM DISTANCE PROTECTION (80TE) 32I/24O		
Date: 10/10/2024	Name: S Burton	PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova (GEV) and contains proprietary information of GEV. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GEV, and that the information shall be used by the recipient only as approved expressly by GEV. This document shall be returned to GEV upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE VERNOVA Company, GEV CONFIDENTIAL UNPUBLISHED WORK.	Drg No: **10P54663**	PLM No: A20097027	Sht: 1 Next Sht: -
Date:	Chkd:				GE VERNOVA

APPENDIX D

HARDWARE/COMMUNICATIONS COMPATIBILITY MATRIX TABLES

A compatibility matrix table for MiCOM P541 - P546 Line Differential Protection Relays is provided in a separate Excel file, attached as an embedded resource. The matrix can be used to check communications compatibility between related devices. If using Adobe Acrobat Reader, click on the button below to open the spreadsheet.

This manual must be opened with a PDF viewer capable of opening attachments, such as Adobe Acrobat Reader or Nitro PDF. If using Nitro PDF, attachments are shown in the attachment pane. To show or hide the attachments pane, look in the sidebar and click the attachments tab.

Note:
An Open File dialogue box may open with a warning message about potential harm from programs, macros or viruses. The file supplied does not contain any harmful content, and may be safely opened.

Compatibility Matrix



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