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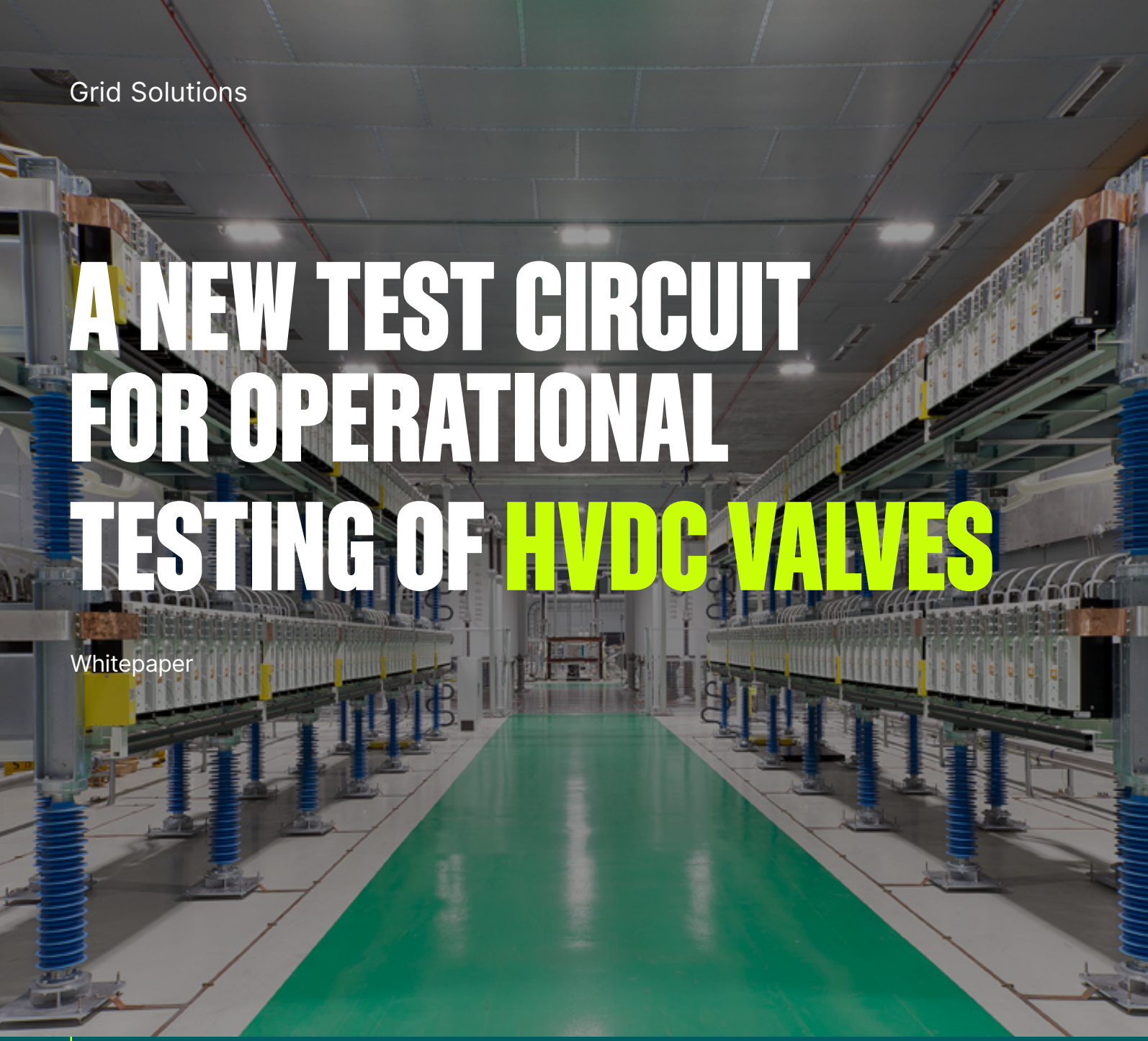

A NEW TEST CIRCUIT FOR OPERATIONAL TESTING OF HVDC VALVES

Whitepaper

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SUMMARY

Type tests for valves for HVDC converters are defined in IEC 60700-1 (for line commutated converter [LCC] valves) and IEC 62501 (for voltage sourced converter [VSC] valves). Of the tests described therein, the operational tests (which demonstrate the ability of the valve to withstand the repetitive voltage and current stresses occurring alternately during normal operation) are challenging and require a very specialized test circuit. For LCC valves, the established technique has been to use a synthetic test circuit while for VSC valves, the use of some form of back-to-back test circuit is common. Both methods have limitations; however, and a brand-new test facility, operating on different principles, has recently been commissioned. Its operation for both LCC mode and VSC mode is described in the paper.

1. HOW DO WE GET STARTED?

Type tests for HVDC valves are defined in IEC 60700-1[1] (for LCC valves) and IEC 62501[2] (for VSC valves). These standards define several categories of testing; however, the most challenging category of test is the "operational tests" that demonstrate the ability of the valve to withstand the repetitive voltage and current stresses occurring alternately during normal operation. With currents of several kiloamperes and off-state voltages of hundreds of kilovolts for the valve as a whole, such circuits are challenging to design and build without requiring very powerful test supplies.

2. REVIEW OF EXISTING TEST METHODS

2.1 Line-Commutated Converter valves

Since the early days of HVDC transmission in the 1950s and 1960s, a topic which has exercised engineers is that of how to test the HVDC valves under conditions that are representative of real-life operating conditions. The advent of thyristor valves in the 1970s, based on the series-connection of many hundreds of small thyristors, led to the possibility of conducting certain tests on scaled-down sections of the valve – something that was not possible with the mercury arc valves that had preceded them. Nevertheless, testing remained a challenge and the highly specialized nature of HVDC valves meant that only a few special test laboratories were capable of performing the tests. Particularly challenging were the operational tests, which are to prove the ability of the valve to withstand the repetitive voltage and current stresses occurring alternately during normal operation (Figure 1).

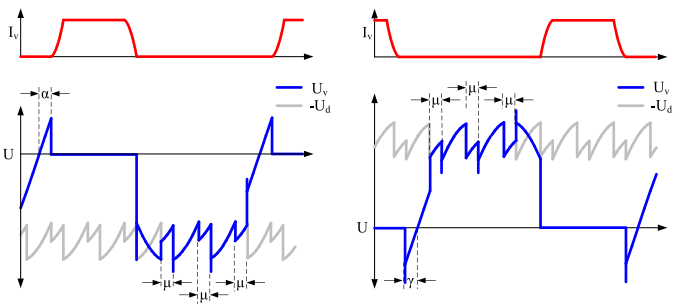

Figure 1: LCC valve voltage and current waveforms

The operational tests must reproduce a number of critical aspects in relation to these voltage and current waveforms, in particular:

- Heating effect in thyristors due to load current
- di/dt at turn-on and turn-off
- Peak firing voltage (PFV)
- Prospective recovery voltage (PRV)
- Heating effect in damping circuits due to step-changes of voltage

For LCC valves, CIGRE TB113[3] identified two principal types of test circuit suitable for such testing: those based on a back-to-back six-pulse (or three-pulse) test circuit and those based on a synthetic test circuit.

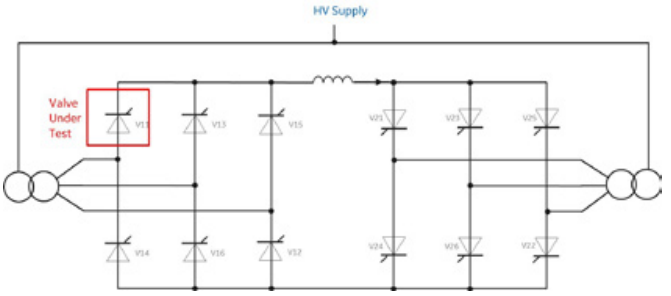

Figure 2: Six-pulse back-to-back test circuit

The back-to-back test circuit (an example of which is illustrated in Figure 2) consists of two separate bridges fed from a common AC supply by two dedicated step-down transformers. The valve under test makes up one valve of one of the converters.

The advantage of this method is that the voltage and current waveforms applied to the test valve are (nearly) equivalent to what the valve would see in service.

However, the back-to-back test circuits suffered from two inherent limitations: firstly the difficulty in obtaining high power ratings and secondly their dependence on the frequency of the AC network to which they were connected. In addition, because the current and voltage waveforms depend on the impedance of the transformer and the coupling between star and delta bridges, it is not possible to obtain perfect voltage and current waveforms without using a custom-designed transformer for each project, an approach which is clearly very costly.

As the voltage and power ratings of thyristors increased steeply in the 1980s and 1990s, reaching levels of 8 kV and 4000 A by the end of the 1990s, it became increasingly difficult to obtain adequate test levels on a realistically-sized test object. As a result, the alternative approach - the synthetic test circuit - has become the most common method. Synthetic test circuits rely on separate sources for high voltage and high current (Figure 3), such that the power requirements for each are modest.

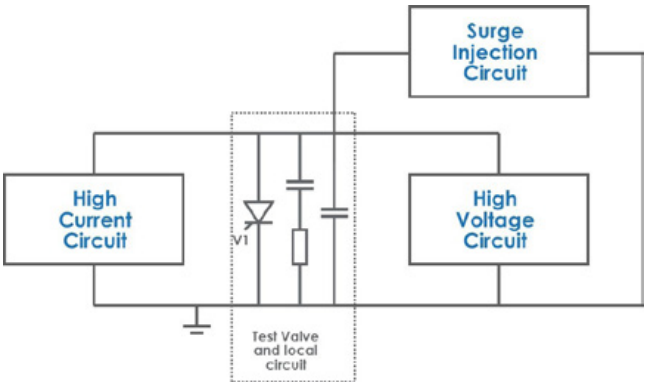

Figure 3: Synthetic test circuit

The use of a synthetic test circuit was first proposed for testing thyristor valves in 1978[4] as a refinement of the existing method used for more than 10 years for testing mercury arc valves. Synthetic test circuits provided a way of overcoming the limitations of the back-to-back test circuit and allowing much larger (and more representative) sections of valve to be tested in a single stage. Synthetic test circuits were initially viewed with scepticism

in the industry but over the intervening years they have become accepted as the standard method for performing operational tests. Over the years, GE Vernova and its predecessors in Stafford, UK, have progressively refined the synthetic test circuit[5].

The principal disadvantage of synthetic test circuits in their current form is that the voltage and current waveforms do not look visually similar to those of a real HVDC converter (Figure 4). Although a well-designed synthetic test circuit is able to reproduce all the key parameters required by the standards, it can never achieve perfect waveform fidelity.

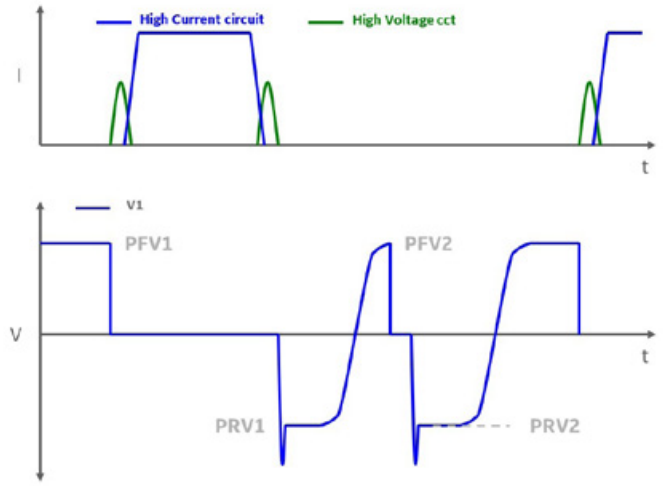

Figure 4: Voltage and current waveforms from GE Vernova's established synthetic test circuit

2.2 Voltage-Sourced Converter valves

The aim of the operational tests for VSC valves is similar to that of LCC valves, namely to demonstrate that the valve is suitable for the repetitive voltage and current stresses it will experience in service. However, with VSC valves based on the modular multi-level converter (MMC), there is a crucial difference in that the valve is not merely a switch, but rather a controllable voltage source through which a time-variant current passescontinuously (Figure 5).

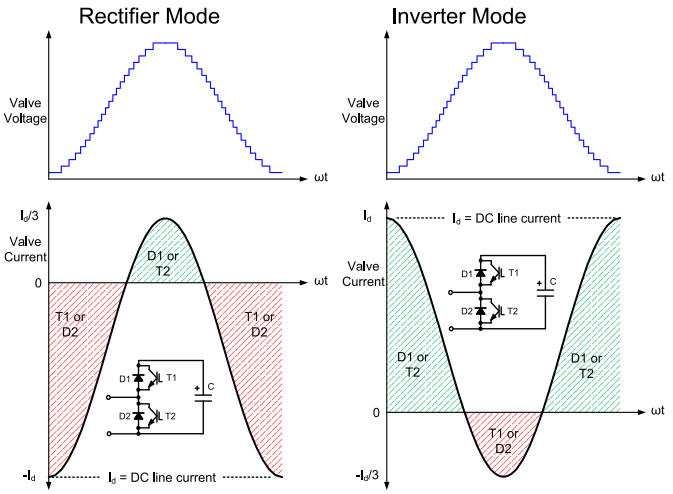

Figure 5: MMC valve voltage and current waveforms

Several test circuits have been proposed for performing operational-type tests on VSC valves. All generally involve dividing the test object into several sections, typically two or four, in a back-to-back or bridge arrangement and operating them together with a load inductor, as illustrated in Figure 66. This method is capable of allowing the valve voltage and current to be controlled independently and meets all the objectives defined in IEC 62501. However, a limitation is that because the valve sections under test are effectively being used to drive current through an inductive load, the phase relationship between valve voltage and valve current cannot be changed with this approach. This may lead to the switching losses in the submodules not being represented perfectly.

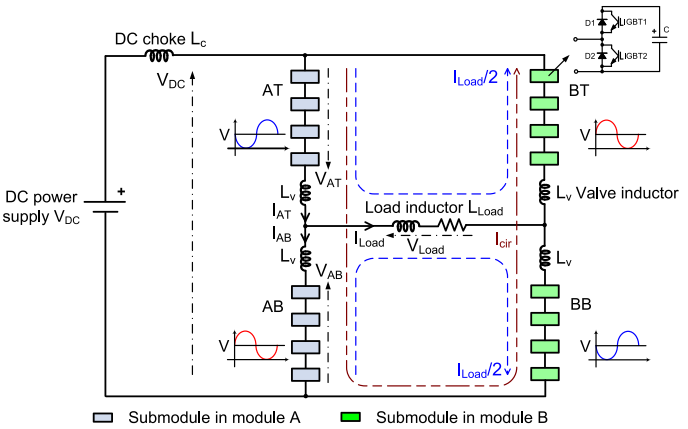

Figure 6: VSC operational test circuit described in "Electrical Type Tests for the Voltage Sourced Converter Valves based on Modular Multi-Level Converter"[6]

For the above reasons, when GE Vernova decided to invest in a new state-of-the-art HVDC valve test facility in Stafford, UK, a novel and fundamentally different approach was taken.

3. Introduction to new test facility

The MMC topology has transformed the HVDC industry, allowing the flexibility of VSC to be achieved with power ratings and efficiency that are now starting to challenge those of LCC technology. Accordingly, when the need was identified to build a new, purpose-built HVDC valve test facility (VTF), it was fitting that MMC valves should be at the heart of the new test circuit.

The new VTF makes use of the fact, already noted above, that MMC valves are effectively "controllable voltage sources". It therefore stands to reason that if a sufficiently large and powerful MMC valve is used (and provided with a source of energy to make up the losses in the circuit) then it can be used as a current or voltage "arbitrary waveform generator" and take the place of both the high-current and high-voltage parts of the older synthetic test circuit. This allows the test circuit, shown schematically in (Figure 7), to be made considerably simpler than the classic synthetic test circuit of (Figure 3).

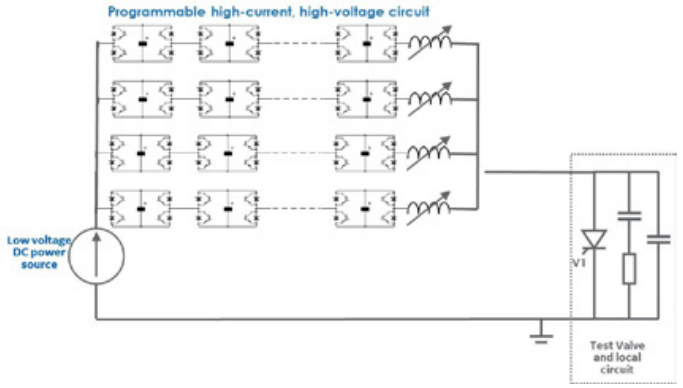

Figure 7: Schematic overview of new test circuit for operational tests

The programmable waveform generator is constructed from four series arrays of full-bridge MMC submodules, with 48 submodules in each array. By using this number of submodules, the test circuit is capable of producing a repetitive test voltage far in excess of what is required by the international standards, with a test current in LCC mode of up to 6000 A. The submodules are of identical design to those of the three STATCOMs currently being supplied by GE Vernova to National Grid in the UK[7]. Figure 8 shows the full-bridge valves in the new test facility.

Figure 8: Full-bridge valves in new test facility

In series with each of the four arrays of full-bridge submodules is a multiple-tapped reactor, which allows the effective commutating reactance for the project to be adjusted to accurately represent the conditions for the valve under test. This is particularly important for testing LCC valves.

The circuit also includes an impulse generator which can be used to apply carefully-timed impulses of various different front-times to the valve during the recovery interval. This is an essential requirement of the type tests for an LCC valve operated under inverter conditions[1]. For the slower front times, such as 100 µs, the full-bridge valves of the main operational test circuit can be used as the impulse generator.

In addition, provisions are made to perform the insulated-gate bipolar transistor (IGBT) turn-off tests and diode overcurrent tests required for the testing of VSC valves in IEC 62501. The test methods for these tests are similar to those described in "Electrical Type Tests for the Voltage Sourced Converter Valves based on Modular Multi-Level Converter"[6].

4. DESCRIPTION OF OPERATION IN LCC MODE

When testing LCC valves, the full-bridge valves of the test circuit fulfil the roles previously played by both the high-voltage and high-current test circuits. The full-bridge valves are alternately controlled as a controllable voltage-source (during the off-state interval of the valve under test) and as a controllable current source (during the on-state interval).

In the on-state, the test circuit directly reproduces the required trapezoidal shape of current with the correct peak and correct di/dt at switching. The di/dt during the first 10-20 µs after turn-on and the last 200 µs before the current falls to zero are particularly important[3] since these have a substantial effect on the inrush stress on the thyristor, the commutation overshoot at turn-off and the turn-off time of the thyristors. These aspects are also influenced by the stray capacitance of other converter equipment and the effective damping circuit impedance of other valves in the bridge. This is why in parallel with the test object are a plain capacitor (representing stray capacitance) and an RC circuit (representing the damping circuits of other valves) – a practice carried over from the previous test circuit. The RC circuit is provided partly by connecting an additional "auxiliary valve" based on GE Vernova's latest LCC valve design in parallel with the test object. The auxiliary valve is fully equipped with thyristors and other components so that can be used instead of the test object during the setting-up of the plant. The auxiliary valve is scaled to 1.5x the number of test-object levels to give a representative impedance across a wide frequency range.

In the off-state, the full-bridge valves are controlled as a controllable voltage source. This allows enormous flexibility in the amplitude and waveshape of the voltage applied. The previous test circuit (Figure 3) was able to reproduce the correct voltage at turn-on and turn-off (PFV1 and PRV1) but also, by imposing additional voltage steps PFV2 and PRV2 with an auxiliary valve in parallel with the test valve, the correct value of $\Sigma(\Delta\partial)^2$. This is important from the perspective of reproducing correctly the damping circuit losses. The new test circuit can achieve all these aims. In addition, it can correctly reproduce the amplitudes of all of the step-changes of voltage that occur during the off-state interval as other valves in the bridge turn on or off, as well as the sinusoidal sections of voltage that interconnect these step-changes. Figures 9 and 10 illustrate examples of the voltage and current waveforms for testing a single valve module of GE Vernova's latest LCC HVDC valve in, respectively, rectifier and inverter mode at a DC current of 4200 A and a frequency of 60 Hz. This demonstrates well the independence of the test circuit from the local grid frequency (50Hz).

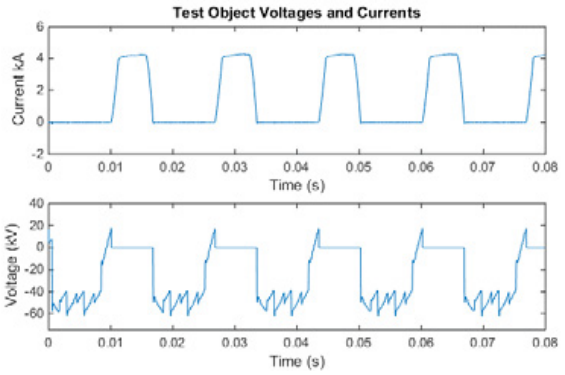

Figure 9: Example of test circuit voltage and current waveforms in rectifier mode

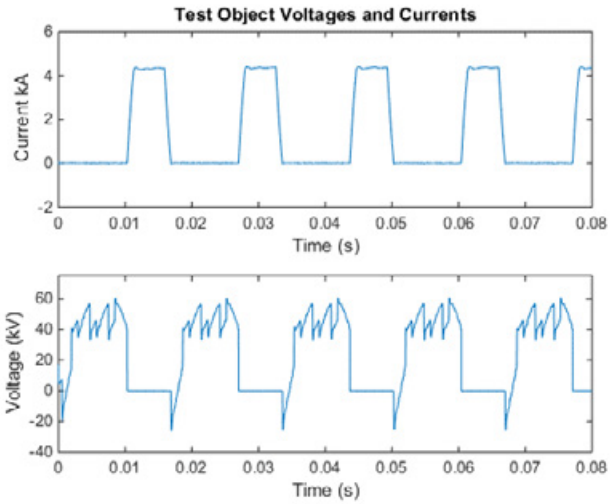

Figure 10: Example of test circuit voltage and current waveforms in inverter mode

At the core of the test facility control solution is the concept of a test definition. Duty cycles may be defined as free-form or sinusoidal voltage and current waveforms alongside precisely timed firing and triggering events.

The off-state voltage waveform is selected in the HMI system by defining a series of ramps and step-changes (Figure 11). It is possible to program over 40 reference points per fundamental-frequency cycle, which is more than sufficient for any practical purposes. Although normally the test wave-forms would be defined by directly specifying the equivalent peak valve-winding voltage (scaled to the test object), control angle and overlap angle, it is possible to define a completely arbitrary voltage waveform if required for special purposes.

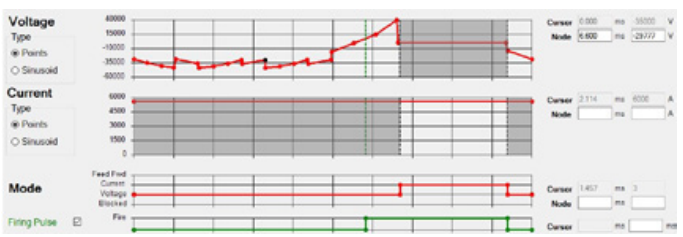

Figure 11: Example of the waveform definition HMI screen for LCC

The test controller is able to operate with pre-defined sequences of test conditions, such as a period of operation at a steady-state operating point with normal control angles, followed by a short-duration operation at a firing angle of α=90°.

In common with the previous test circuit[5], the circuit also allows operation in intermittent direct current (with up to eight turn-on/off cycles per fundamental cycle) and with impulses applied during the recovery interval of the inverter valve.

Once defined, the platform-independent test definitions may be run in a virtual simulation environment, on an RTDS arrangement or on the test facility itself. This approach allows for comparison of test results and even for the test definitions to be tested under simulation before execution on the facility.

5. DESCRIPTION OF OPERATION IN VSC MODE

As mentioned in section 3, the existing method used by GE Vernova for testing VSC valves is to use two "valve modules" (each with eight submodules) in a back-to-back configuration so as to control the current in a load reactor.

However, although this method allows the voltage of the valve sections and the root mean square current through them to be controlled to the correct in-service values, there is very little flexibility in the phase-relationship between the voltage and current.

In the real VSC application, as shown on Figure 5, there can in principle be almost any phase shift between voltage and current, depending on whether the HVDC scheme is operating as a rectifier or an inverter and how much reactive power it is generating or consuming.

The new test circuit allows the required phase shift to be set, ensuring the valve section duty is represented more accurately, exceeding the requirements of IEC 62501.

In a VSC valve based on the modular multi-level converter, contrary to what one might expect each valve is typically controlled as a current source. The vector control generates a valve current order for each valve, and this current order is passed to the modulation controller which then decides what combination of submodules need to be in the output state for the next switching cycle in order to meet or approach that current order. Nevertheless, the individual submodules know nothing of the overall current order that the valve, as a whole, is trying to meet, and therefore continue to behave as controlled voltage sources.

So, when testing a submodule or a small group of submodules, it is preferable to control those submodules as a controlled voltage source but connect them to a test plant configured to behave as a controlled current source representing the rest of the VSC valve. This was not possible with the previous test circuit outlined in M.L. Woodhouse and T Simanwe's CIGRE session paper[5] but since the VSC valves that form the new test plant contain a much larger number of submodules than the test object itself, they can easily impose the desired target current on the test object.

As a consequence, it is possible to arrange for the test object to see exactly the correct amplitude and waveshape of both voltage and current, including the phase relationship between them. Figures 12 and 13 illustrate this by showing typical voltage and current waveforms for rectifier and inverter operation respectively.

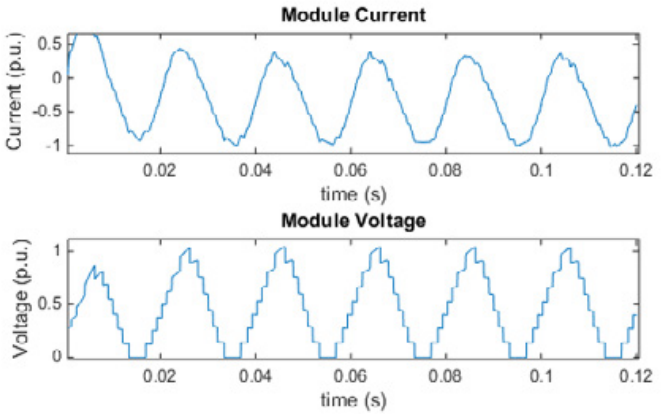

Figure 12: Typical VSC valve voltage and current waveforms when testing in rectifier mode

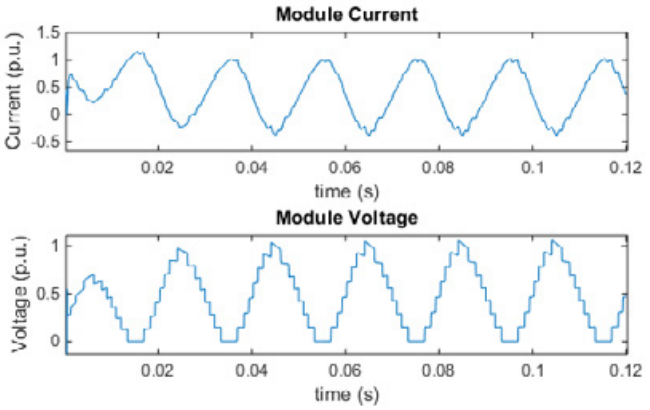

Figure 13: Typical VSC valve voltage and current waveforms when testing in inverter mode

Because the test plant has been dimensioned for the very high valve currents experienced in some LCC HVDC schemes, it has a far higher current capability than is needed for present-day VSC schemes. As a result, the test plant has a high degree of "future-proofing" against the possible expansion of VSC current ratings that may be expected in future.

As with any power electronic circuit, it is essential that the net flow of energy into and out of energy storage components is zero in order for the system to operate in steady state. In the case of the VTF circuit, the individual capacitor voltages are balanced using the same algorithm that has been applied to VSC HVDC schemes whereby the most appropriate module is selected depending on whether the control action would charge or discharge that module. In addition, the total stored energy is controlled by regulating the voltage output of the DC supply and the sharing of energy between the valves is regulated by controlling the contribution of the total current through each valve. This is sufficient for LCC testing, where the test object has no energy store of its own. However, the capacitor voltages of a VSC test object must also be regulated, and this is achieved by controlling the DC component of the test current.

In addition to the steady-state, repetitive operational tests described above, two other operational tests are also important for VSC valves: a test to demonstrate the capability of the IGBTs to turn off under worst-case fault conditions with very high rate of change of current, and a test to demonstrate that the freewheel diodes (and, where fitted, the protection thyristors) are able to withstand the high transient current resulting from a DC line fault. The new test plant can also perform both of these tests, which are performed in a similar way to the previous test lab described in "Electrical Type Tests for the Voltage Sourced Converter Valves based on Modular Multi-Level Converter"[6]. The new facility has been specifically designed to allow these tests to be performed immediately following the continuous operating duty tests. This allows the test object to be heated to its worst-case continuous junction temperature using the operational test before being exposed to the fault conditions.

6. CONCLUSIONS

Operational tests on HVDC valves have always been challenging to perform and require highly specialized test circuits. Moreover, the test circuits known until the present time have always involved some degree of compromise such that not every aspect of the test object voltage and current can simultaneously be reproduced exactly as it would be in service.

Although GE Vernova's earlier HVDC valve test laboratory was able to reproduce all the key aspects required by the relevant international standards,[1, 2] neither it nor any of the other known test circuits was able to reproduce the test object conditions with complete fidelity.

GE Vernova has now built a new, purpose-built test facility which allows the testing of HVDC valves to be taken to new levels of waveform fidelity. The test plant, which was commissioned in 2018, is located in Stafford, UK, near GE Vernova's HVDC Centre of Excellence and is capable of testing both LCC and VSC valves to voltage and current levels higher than are required today or in the foreseeable future.

References

[1] IEC 60700-1: “Thyristor valves for high voltage direct current (HVDC) power transmission - Part 1: Electrical testing”.

[2] IEC 62501: “Voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission - Electrical testing”.

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[6] T.Xu, P.S.Jones, C.C.Davidson, “Electrical Type Tests for the Voltage Sourced Converter Valves based on Modular Multi-Level Converter”, 17th European Conference on Power Electronics and Applications (2015).

[7] GE Vernova Press Release, 14th Dec 2016: “GE Vernova to Provide National Grid with Largest, Most Stable Utility STATCOM in Europe”.

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