

Application of Line Relays at Dual-Breaker Terminals

Ilia Voloh General Electric
Bogdan Kasztenny formerly with General Electric

Presented at the 33rd Annual Western Protective Relay Conference
Spokane, WA, October 17-19, 2006

APPLICATION OF LINE RELAYS AT DUAL-BREAKER TERMINALS

Iliia Voloh
General Electric

Bogdan Kaztenny
formerly with GE

Abstract—Line protection in breaker-and-a-half configurations requires main protection functions to respond to the sum of the two currents on the diameter. This concerns many protection functions particularly when sensitive settings are applied and/or significant CT saturation occurs. If the remote system is relatively weak, the current supplied through the line towards a close-in reverse fault on the breaker-and-a-half terminal may be overwritten with a spurious current produced by saturated CTs. This may affect directionality and impact not only fast and sensitive ground protection functions used by pilot-aided schemes, but also distance, and current differential protection elements. This paper addresses the problem by providing practical solutions for ground directional overcurrent, distance and differential functions. A new design for the digital line current differential relay is presented. The relay is capable of protecting three-terminal applications with each terminal fed from up to four currents.

Keywords—breaker-and-a-half, current transformer saturation, digital line current differential protection, distance protection, integrated bus and line protection, transmission lines.

1. INTRODUCTION

Standard practice today with respect to protecting line terminals arranged as breaker-and-a-half is to sum the two currents externally and feed single-input distance or line differential relays with the total current flowing into the protected line. Breaker failure functionality requires monitoring the two breakers and currents separately and is typically implemented outside of the main protection relay. Reclosing and synchrocheck functions require monitoring and controlling both breakers independently, as well as measuring two pairs of voltages for the synchrocheck purpose, are also – in majority of cases – implemented outside of the main line protection device.

With the breaker failure, reclosing and synchrocheck functions performed in a separate device (a breaker controller, such as [1]), application of the main line protection for the breaker-and-a-half is treated with no major differences compared to single breaker configurations.

Fed with externally added currents (Fig.1a) a typical line differential relay produces a restraint signal as per its design equations, preferably applying some countermeasures for the CT saturation problem, all based on the summation of the two local currents. Because the relay does not respond to the individual currents, but to the sum of thereof, a combination of restrained and unrestrained differential principles is effectively applied, and as such, it may face stability problems. For example, with weak feed from the remote terminal(-s), and a large through fault current along the breaker-and-a-half diameter, CT saturation errors would manifest themselves as a spurious differential current while relatively small restraint would be produced from the low remote-end currents (high through-diameter current not seen by the relay, low through-line current seen by the relay as depicted in

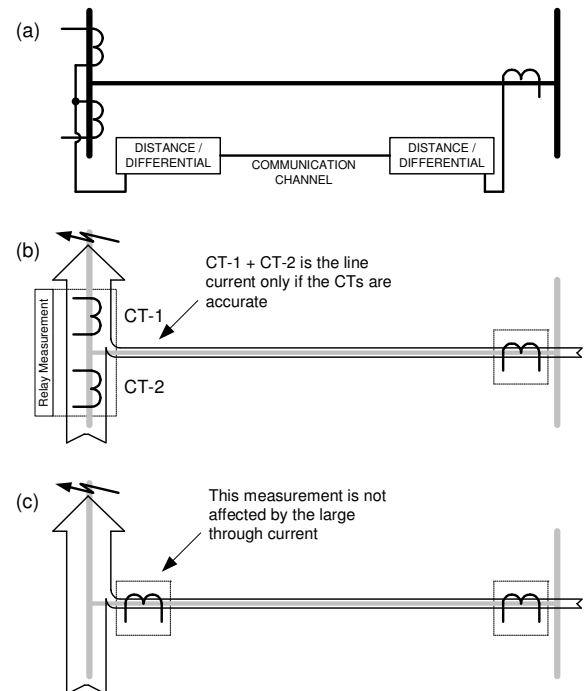


Fig.1. Breaker-and-a-half arrangement: external CT summation (a), through fault under weak remote and strong local systems (b), through fault in a single-breaker application (c).

Fig.1b).

This problem does not exist in single breaker applications (Fig.1c). With the line current measured directly in single-breaker applications there is no danger of producing a large error signal even if the line CT saturates.

The problem in the breaker-and-a-half arrangements demonstrates itself not only under severe CT saturation, but could become significant under relatively small CT errors, including linear errors related to the accuracy class. As long as the through current of the line is considerably higher compared with the error current produced by the CTs, there is no danger of the CT error signals overriding the actual through line current. When the error current is comparable with the through current, the protection system is in danger of misoperation. The through current could be low for long lines and/or when the remote system is relatively weak. The current flowing along the breaker-and-a-half diameter is controlled by the short-circuit level of the local system alone. With the local terminal strong, and the remote terminal weak, any relay could be brought to its design limits by saturating the CTs on the diameter, or even by linear errors of the two CTs.

Distance relays are also exposed to this problem. During close-in reverse faults, the voltage is depressed to very low levels, and stability of the relay is maintained by the directional supervision alone. If, under such circumstances, CT that carries the current away from the terminal saturates (CT1 in Fig.1b), the error current appears in the direction of the line. With enough error current, the through line current becomes overridden, and the true reverse direction may get reversed as seen by the relay. As a result, with the voltage depressed and the current elevated and flowing spuriously in the forward direction, distance functions may pickup inadvertently. This includes a directly tripping underreaching zone 1, as well as an overreaching zone 2 typically used by teleprotection schemes. In both cases, a false trip could occur. Current-reversal logic, application of a blocking or hybrid permissive schemes, or similar approaches, may enhance the performance and solve the problem partially. These approaches, however, often rely on a reverse-looking distance zone 4. The latter may spuriously drop out when the effective current gets inverted from the true reverse to a false forward direction due to CT errors. Extending the blocking action by using timers is a crude solution, and will jeopardize dependability and speed of operation on evolving external-to-internal faults.

Ground directional overcurrent functions, neutral and negative-sequence specifically – being both fast and sensitive – are good supplements enhancing performance of teleprotection schemes [2]. They, however, face similar security problems in the breaker-and-a-half applications. With reference to Fig.2 consider an external line-to-line fault on the diameter. Now performance of all four CTs (A1, A2, B1 and B2) affects the neutral current. With any of the CTs saturating, a spurious neutral current will be created. There is no real neutral current through the line for this type of fault. Therefore, the operating signal for the Neutral Directional Overcurrent function is entirely driven by CT errors. The remote terminal will see the fault via its distance function and key permission to trip, unless separate pilot channels are used to key from distance and ground directional functions. Combined with the spurious operation of the neutral directional function at the local terminal, the received

permission would cause a false trip. Three-phase symmetrical faults affect both negative-sequence and neutral functions in a similar manner.

This paper addresses issues related to distance, ground directional and differential functions under CT saturation in breaker-and-a-half applications, and is organized as follows. Section 2 outlines the overall application of the main protection, breaker failure, autoreclose and synchro-check functions for two breakers in a single device. Section 3 introduces simple supervision logic for ensuring stability of distance, differential and ground directional functions in the breaker-and-a-half arrangement. Section 4 presents a new design principle for a line current differential relay with multiple current inputs at each terminal of

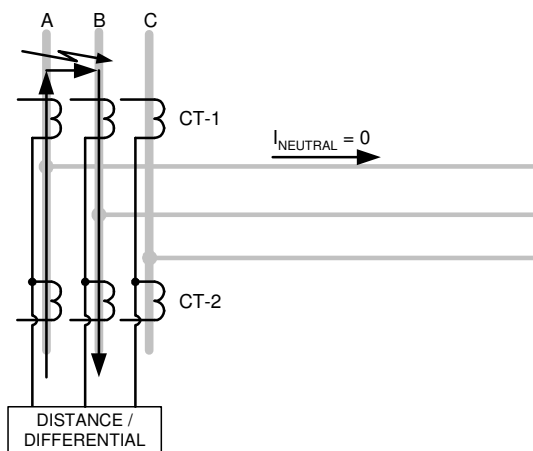


Fig.2. Possibility of spurious neutral or negative-sequence currents in the breaker-and-a-half application.

the line.

2. BREAKER-AND-A-HALF TERMINAL PROTECTED AND CONTROLLED FROM A SINGLE IED

Modern line protection relays (Intelligent Electronic Devices, IEDs) allow for protection and control of the breaker-and-a-half arrangement from a single IED. Application of separate breaker failure and/or synchrocheck relays is no longer dictated by limitations of the main protection relay, but driven by application philosophy to either combine the required functions for cost benefit, or to keep them separate for dependability.

With reference to Fig.3, a modern IED capable of the breaker-and-a-half application supports two three-phase current inputs in order to measure both the currents individually for the breaker failure protection (50BF), backup overcurrent protection (51P), and associated metering functions. The two currents are added in software to become the input for the main protection functions of the line: distance (21) or line differential (87L) in particular, as well as for the line metering.

The IED must support one three-phase voltage input required for the main protection, and at least two single-phase voltage inputs in order to accomplish the synchrocheck functionality (25) for both the breakers. A dual-breaker autorecloser (79) typically capable of reclosing the breakers simultaneously, or sequentially, with the ability to cover out-of-service conditions for any of the two breakers, completes the application. A suite of backup and auxiliary functions are typically attached to the voltages and the three currents (breaker 1, breaker 2, and the line).

Modern IED such as [3] or [4] are designed to support enough AC inputs (at least 5 voltages, and 6 currents), digital inputs (breaker status, external breaker fail initiate, etc.) and output contacts (per pole trip for both breakers, reclose per breaker, breaker fail re-trip and trip, etc.) to facilitate protection and control of a breaker-and-a-half terminal from a single IED.

These devices shall be designed and configured to cope with the problems outlined in Section 1, particularly in applications with long lines and/or weak remote systems.

3. SUPERVISORY LOGIC TO COPE WITH CT ERRORS

This section outlines a simple supervisory logic to ensure security of the main protection during through current conditions on the breaker-and-a-half diameter with weak feed through the line. The logic can be programmed from a number of standard Instantaneous Overcurrent elements (IOCs) and Phase Directional (Ph Dir) elements of the relay.

The logic has been developed to meet the following requirements:

- The supervision should not penalize speed of response to internal faults (trip time) or sensitivity of the relay to high-resistance internal faults. Therefore the permission to trip should be given all the time unless a through fault condition is detected.
- Permission to trip should be maintained during transition from load conditions, possibly a reverse load, to internal faults.
- The supervision should allow the relay to trip an evolving external-to-internal fault, in particular

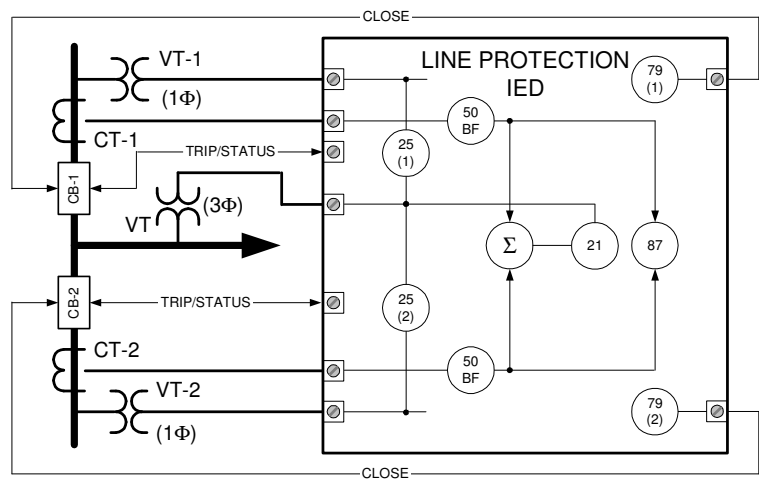


Fig.3. Breaker-and-a-half terminal protected and controlled from a single IED.

with both faults present at the same time, i.e. before the external fault is cleared by the associated protection system.

- The supervision should respond to elevated phase currents as the high phase currents cause CT errors and the latter could jeopardize security of the line protection.
- The supervision shall be easily applied to distance, differential, and overcurrent directional functions, including the negative-sequence and neutral directional overcurrent elements.

3.1. Protection Elements Used by the Supervisory Logic

With reference to Figures 3 and 4 the following elements shall be enabled:

- IOC 1 to respond to forward current of CT-1. The element shall be set at 2-3 times the nominal of CT-1, and is used to unblock the relay on external-to-internal evolving faults.
- IOC2 to respond to elevated current of CT-1. Set at 1.5-2 times the nominal of CT-1 and used to supervised the blocking action.
- PHS DIR 1 to respond to reverse current direction in CT-1.
- IOC3 – similar to IOC1, but for CT-2.
- IOC4 – similar to IOC2, but for CT-2.
- PHS DIR 2 – similar to PHS DIR 1, but for CT-2.

The directional functions in one particular application [3-4] use quadrature polarization with memory action, if required.

3.2. The Supervisory Logic

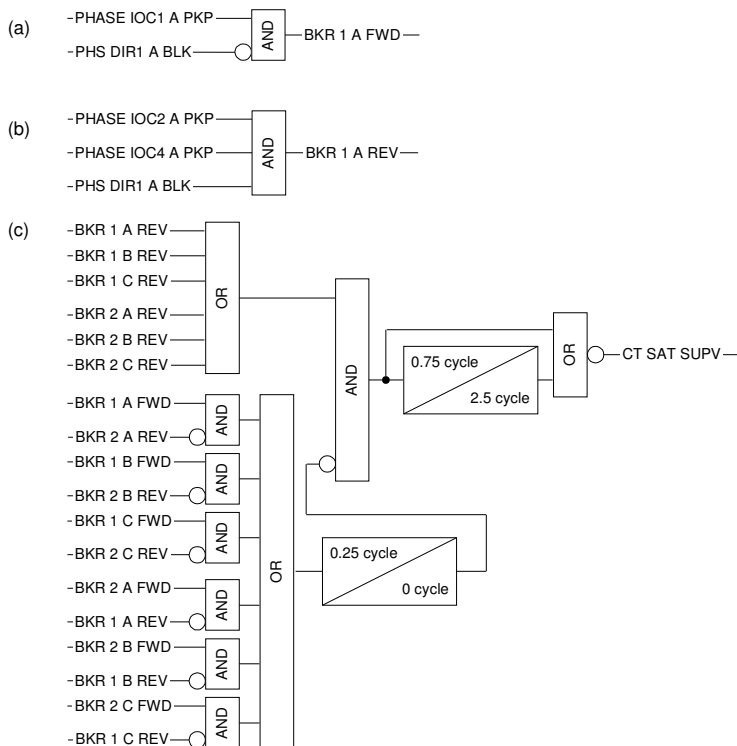


Fig.4. Supervisory Logic To Cope with CT Errors in the Breaker-and-a-Half Configuration.

With reference to Fig.4, forward and reverse direction indications are derived for both the breakers.

A reverse direction for CB-1 (Fig.4a) is declared if both currents are elevated (IOC2 and IOC4) and the directional element sees a reverse direction (PHS DIR 1 BLK). Similar logic is implemented for CB-2, and phases B and C. The reverse direction flags will be asserted only if an elevated current is flowing through the diameter, and the direction is reverse in one of the legs.

A forward direction for CB-1 (Fig.4b) is declared if the current is elevated in the CB-1 leg and appears in the forward direction. Declaration of the forward direction is not impacted by the situation in the second leg of the diameter. Similar logic is implemented for CB-2, and phases B and C.

As shown in Fig.4c, the blocking action is established if any of the three phases shows a through current flow-

ing outside, either through CB-1 or CB-2.

For security, the blocking action gets artificially extended for extra 2.5 cycles if lasts for 0.75 of a cycle (switch off transient logic to cope with clearance of the external fault).

The blocking action gets cancelled if any of the currents is elevated, appears in the forward direction, and is not accompanied by the reverse direction in the associated leg of the breaker-and-a-half arrangement. A 0.25 cycle delay is added for security.

3.3. Performance Analysis and Explanation

During load conditions (current below some 1.5 times CT nominal) none of the IOCs is picked up and the trip permission is asserted permanently.

During internal fault conditions with very weak feed from the breaker-and-a-half terminal, the current is not elevated and may appear in the reverse direction as dominated by the load – permission is maintained as none of the IOCs picks up.

During high current internal faults, none of the directional elements operates in the reverse direction, and the trip permission is maintained.

During external faults with one breaker opened, the blocking action is not established, but it is not needed either.

During external faults with both breakers closed, the blocking action is established as long as both the currents flowing through the diameter are above the pickup of IOC2 and IOC4.

During evolving external-to-internal faults in different phases, the blocking action is first established (say, phase A), and then canceled when the second fault appears in the forward direction in a different phase (say, phase B).

The output flag, CT SAT SUPV of Fig.4c, shall be used to supervise distance and ground directional functions of a distance relay, and the differential function of a line current differential relay, if required.

3.4. Transient Response Examples

Fig.5 presents an external fault example. The trip supervision is removed in 0.5 of a power cycle when using one particular IED to implement the logic of Fig.4c [2].

Fig.6 shows an evolving fault example. The trip supervision is removed in 1 cycle after the external fault, but is re-established in 0.75 of a cycle after the fault evolves into internal.

4. LINE DIFFERENTIAL ALGORITHM

This section presents a description of a line current differential algorithm based on the original idea [5-6], but extended to breaker-and-a-half-applications.

Concept [5-6] has been originally implemented for a single-breaker arrangement. In such an application, each relay [4] sends phasors of local current in all three-phases calculated using a half-cycle estimator (6 numbers) as well as dynamic terms used for adaptive restraint (3 numbers). Some extra data is appended to this core of the packet such as relay ID, direct I/Os for teleprotection, time stamps to facilitate synchronization with the use of the ping-pong algorithm [6], GPS-driven time stamps to facilitate channel asymmetry compensation [7], CRC-check, etc.

The presented solution targets communications channels of 64kbps. The baud-rate of the channel imposes certain limitation for the packet size. Application in breaker-and-a-half configurations calls for producing a proper restraining signal out of all the currents of the zone. For example, in three-terminal applications with each of the terminals being breaker-and-a-half, 6 three-phase currents surround the line differential zone. Exchanging all these currents between the terminals would increase the packet size.

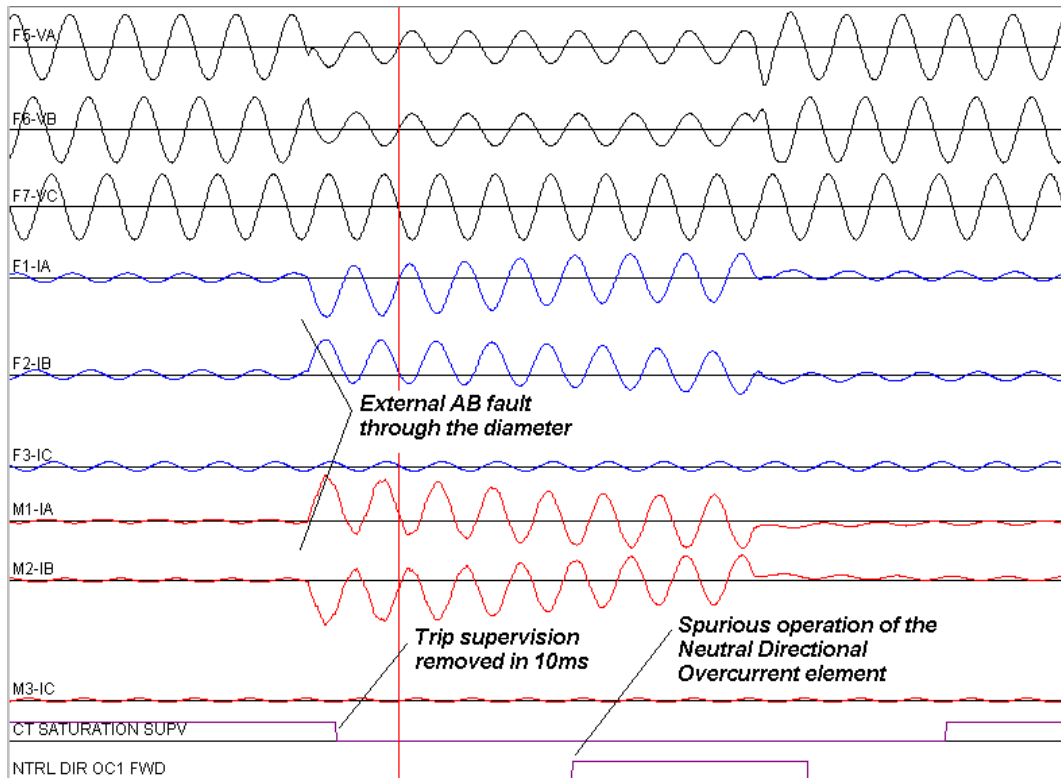


Fig.5. External Fault Example. Phase-to-phase fault through the diameter causes enough CT error to operate spuriously the Neutral Directional OC function. The CT supervisory logic blocks in 0.5 cycle.

The following design targets have been stated:

- The packet size should remain unchanged. A total of 9 numbers must represent currents at each terminal in terms of phasors and dynamic restraint factors.
- Window resizing shall be applied for fast relay operation.
- Proper restraint shall be produced to secure the differential system on external faults through the breaker-and-a-half diameter.
- Up to four currents could be used at each terminal in order to facilitate combined bus and line protection for small buses and mashed corners.
- Backwards compatibility of the operating principle shall be maintained if the relay is applied in a single breaker configuration.

The following subsections address the above constraints.

4.1. Phasor Estimation

The input currents are sampled at 64 samples per cycle and pre-filtered using an optimized MIMIC filter aimed at removing dc component(-s) and other low-frequency oscillations. The optimized filter is a Finite Response Filter (FIR) with the window length of approximately $1/3^{\text{rd}}$ of a power system cycle.

The digitally pre-filtered currents are converted into phasors by applying half-cycle Fourier algorithm. The half-cycle values are either used as calculated, or two consecutive half-cycle measurements are combined into an equivalent full-cycle measurement. The operation of switching from full- to half-cycle is referred to as window resizing and is implemented to speed up operation of the relay. The differential system transmits half-cycle values, and the resizing is done independently at each terminal of the line.

Half-cycle magnitudes are also calculated and transmitted in order to reflect properly through fault condi-

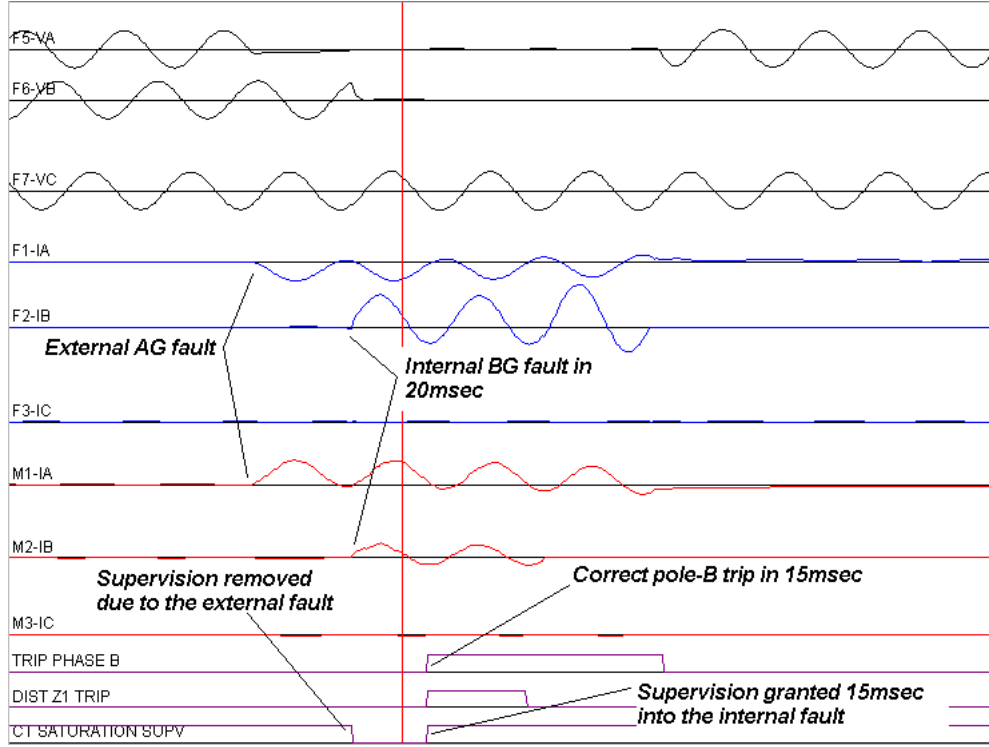


Fig.6. External-to-Internal Evolving Fault Example. The relay trips single-pole the correct phase despite the pre-existing external fault. The CT supervisory logic unblocks in 0.75 of a cycle.

tions at each terminal of the line.

In addition “a goodness of fit” factor is calculated for each current in order to measure the error between the waveform and its Fourier estimated phasor [5]. The goodness of fit factor is further used to produce an extra restraint to countermeasure the estimation error, and increase security of the relay. Conceptually, the goodness of fit factor is proportional to the following value:

$$\delta_{(k)} = \sum_{n=0}^{N-1} \left| x_{(k-n)} - X_{(k)} \cdot \cos\left(\frac{2 \cdot \pi \cdot n}{N} + \Theta_{(k)}\right) \right|^2 \quad (1)$$

In equation (1), the present magnitude and phase estimate (X, Θ) at the k -th sample is compared with the actual waveform (x) over the duration of the data window (N), and the sum of squares error measure is calculated.

4.2. Consolidating Local Currents – the Outgoing Packet

Each terminal of the current differential system consolidates the local signals into an outgoing packet. Compression of information takes place in order to reduce the packet size and distribute the calculations between the two or three relays of the line current differential system. This is possible without compromising operating equations or accuracy if the operating equations are shaped accordingly.

First, the phasors (real, imaginary) of all the local currents are summated to give a sub-sum of the total differential current of the protected line:

$$I_{LOC_RE_A} = I_{1_RE_A} + I_{2_RE_A} + \dots \quad (2)$$

Equation (2) is applies to up to four local current inputs and holds true for both real and imaginary parts, in all three phases.

Second, the measure of a through fault current is estimated locally using magnitudes of all the local currents via the following equation:

$$(I_{LOC_TRAD_A})^2 = \max((I_{1_MAG_A})^2, (I_{2_MAG_A})^2, \dots) \quad (3)$$

Equation (3) selects, on a per phase basis, the largest among the local currents to be a measure of local restraint. Fig.7 illustrates the principles behind equations (2) and (3).

Third, the protection system applies differential characteristic locally to each of the restraining currents. The presented system does not use an explicit restraining characteristic, but the total operating and restraining value [5-6]. The latter incorporates values of the pickup, slopes (S_1 , S_2) and breakpoint (B). The following equations are used to accommodate the characteristic:

- In two-terminal applications:

$$\text{If } (I_{LOC_TRAD_A})^2 < B^2$$

$$\text{Then } (I_{LOC_REST_TRAD_A})^2 = 2 \cdot (S_1)^2 \cdot (I_{LOC_TRAD_A})^2 \quad (4a)$$

$$\text{Else } (I_{LOC_REST_TRAD_A})^2 = 2 \cdot ((S_2)^2 \cdot (I_{LOC_TRAD_A})^2 - (S_2 \cdot B)^2) + 2 \cdot (S_1 \cdot B)^2 \quad (4b)$$

- In three-terminal applications:

$$\text{If } (I_{LOC_TRAD_A})^2 < B^2$$

$$\text{Then } (I_{LOC_REST_TRAD_A})^2 = \frac{4}{3} \cdot (S_1)^2 \cdot (I_{LOC_TRAD_A})^2 \quad (4c)$$

$$\text{Else } (I_{LOC_REST_TRAD_A})^2 = \frac{4}{3} \cdot ((S_2)^2 \cdot (I_{LOC_TRAD_A})^2 - (S_2 \cdot B)^2) + \frac{4}{3} \cdot (S_1 \cdot B)^2 \quad (4d)$$

The adaptive portion of the restraint is a geometrical sum of errors derived from eq. (1) and a measure of the clock synchronization error [5-6]. The traditional and adaptive restraints are combined geometrically using a concept of an extra arbitrary multiplier:

$$I_{LOC_RESTRIANT_A} = \sqrt{(I_{LOC_REST_TRAD_A})^2 + MULT_A \cdot (I_{LOC_ADA_A})^2} \quad (5)$$

The multiplier increases the impact of signal distortions on the restraint, and is used to provide better restraint during CT saturation conditions on through faults.

Values defined by equations (1-5) are based on half-cycle windows, and constitute the following outgoing packet:

$$I_{LOC_RE_A}, I_{LOC_RE_B}, I_{LOC_RE_C}, I_{LOC_IM_A}, I_{LOC_IM_B}, I_{LOC_IM_C}, I_{LOC_RESTRIANT_A}, I_{LOC_RESTRIANT_B}, I_{LOC_RESTRIANT_C} \quad (6)$$

4.3. Total Differential and Restraint Currents

The local and remote data when received are used to calculate the total differential and restraining signals for the current differential system.

Before the data is used, a decision is made to either use the full- or half-cycle measurements. The half-cycle data is used one time after detecting a fault. After such half-cycle window is used, the relay switches back to the full-cycle version when proceeding into the fault. Also, when a packet is lost, the next packet that arrives triggers window resizing. This is simply to enable protection using the latest packet even though the previous packet required to calculate the full-cycle quantities is lost.

The following equations are used to combine the half-cycle values into full-cycle measurements:

$$I_{LOC_PHASOR_RE_A} = 0.5 \cdot (I_{LOC_RE_A(present)} + I_{LOC_RE_A(previous)}) \quad (7a)$$

$$(I_{LOC_PHASOR_RESTRAINT_A})^2 = 0.5 \cdot [(I_{LOC_RESTRAINT_A(present)})^2 + (I_{LOC_RESTRAINT_A(previous)})^2] \quad (7b)$$

Equation (7b) is accurate; equation (7b) is a good approximation. Equations (7) apply to both local and remote signals, all three phases, and real and imaginary parts.

Next, the relay calculates the total differential and restraint currents:

$$I_{DIFF_RE_A} = I_{LOC_PHASOR_RE_A} + I_{REM1_PHASOR_RE_A} + I_{REM2_PHASOR_RE_A} \quad (8a)$$

$$(I_{REST_A})^2 = (I_{LOC_PHASOR_RESTRAINT_A})^2 + (I_{REM1_PHASOR_RESTRAINT_A})^2 + (I_{REM2_PHASOR_RESTRAINT_A})^2 \quad (8b)$$

And applies the severity equation in order to decide if the line should not should not be tripped [5-6]:

$$S_A = (I_{DIFF_A})^2 - (P^2 + (I_{REST_A})^2) \quad (9)$$

Positive values of the fault severity, S , cause the relay to operate. P is the pickup of the characteristic (the slopes and breakpoints were already accommodated before sending the data in equations (4)). As indicated by all the equations, the algorithm is fully phase-segregated.

4.4. CT Saturation Detection

The algorithm has a built-in immunity to saturated CTs owing to the concept of the dynamic restraint. The goodness of fit (1) becomes degraded on saturated CTs, producing a measure of error (1), which added to the restraining signal allows for extra security.

In order to boost this natural effect, the system is using an adaptive multiplier in order to increase further the impact of the dynamic portion of the restraint (5) on the overall performance of the relay.

The multiplier is calculated adaptively per phase as follows:

$$MULT_A = \max(MULT_{1A}, MULT_{2A}) \quad (10)$$

The first component is based on local currents only, and as such is instantaneous. This component is meant to detect through fault condition on the local diameter of the breaker-and-a-half arrangement.

The second component is based on local and remote currents, and as such is lagging the real time by the channel time. Input signals for this component are taken from the alignment table, which aligns instantaneous local values with delayed remote values. This component is meant to detect through fault conditions between terminals of the line.

The first multiplier is calculated as follows:

Step 1. Select the greatest current from the local currents. The selection is based on half-cycle magnitudes: I_{1_MAG} , I_{2_MAG} , I_{3_MAG} , I_{4_MAG} . Assume the largest current is in the k -th circuit ($k = 1, 2, 3$ or 4).

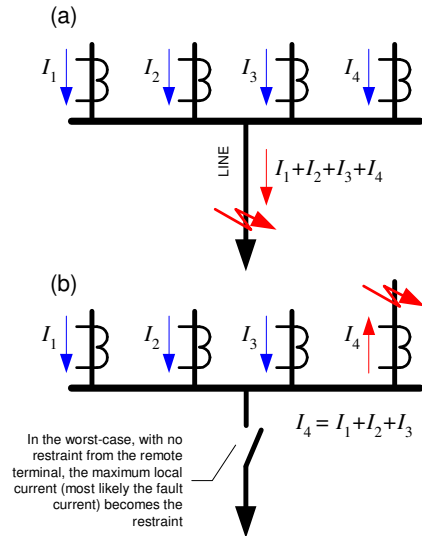


Fig.7. The differential current is created from sums of all the local currents (a). The restraining current is created based on the maximum local current (b). The latter is an external fault current in the worst-case scenario with no feed through the line.

Step 2. Calculate two auxiliary currents:

$$I_{X_RE} = I_{k_RE} \quad (11a)$$

$$I_{X_IM} = I_{k_IM} \quad (11b)$$

$$I_{Y_RE} = I_{1_RE} + I_{2_RE} + I_{3_RE} + I_{4_RE} - I_{X_RE} \quad (11c)$$

$$I_{Y_IM} = I_{1_IM} + I_{2_IM} + I_{3_IM} + I_{4_IM} - I_{X_IM} \quad (11d)$$

The X-current is the maximum current among the local currents. The Y-current is the sum of all the local currents but the maximum current. Note that during through faults with no feed from the remote terminals $I_X = -I_Y$ if no CT saturation. With CT saturation the currents differ, but remain approximately out of phase.

Step 3. Calculate the multiplier as follows:

$$\text{If } |I_X| > 3pu \quad \& \quad |I_Y| > 3pu \quad (12a)$$

$$\text{then If } \text{abs}(\text{angle}(I_X, I_Y)) > 90^\circ \quad (12b)$$

$$\text{then } MULT := \text{abs}(\text{angle}(I_X, I_Y)) \cdot \frac{5}{180^\circ} \quad (12c)$$

$$\text{else } MULT := 1 \quad (12d)$$

$$\text{else } MULT := 1 \quad (12e)$$

Equations (12) check if both currents (the maximum among the local currents, and the sum of all the other local currents) are large enough to cause significant CT saturation. If so, the relative direction of the two currents is checked. If the angle is less than 90 degrees, the multiplier stays at the regular value 1.00. If the angle is larger than 90 degrees, the multiplier is proportional to the angle difference and could reach the maximum value of 5.00 if the currents are exactly out of phase.

The second multiplier is calculated applying exactly the same procedure, but instead of using local currents, the procedure uses the sum of the local currents, and the remote currents. In other words the currents into the line at each of up to three terminals of the line, regardless of the number of local currents at each terminal of the line. The second multiplier detects through fault conditions of the entire line.

Fig.8 illustrates application of the new algorithm under through fault conditions. In this example the traditional restraint of 15pu, is additionally augmented by adding the dynamic factor. The dynamic restraint is naturally increased by saturated CT, and artificially multiplied by the multiplier. In this example, the T3 terminal sees CT saturation in the leg carrying the current out of the line toward the fault. This CT saturation will jeopardize stability of all terminals. However, all terminals will use high values of the multiplier to boost the effect of dynamic restraint, and will not misoperate.

5. CONCLUSIONS

This paper presents practical application solutions for protection of lines in breaker-and-a-half applications. A simple logic that could be implemented on modern line relays is presented to ensure security under CT saturation during through faults on the breaker-and-a-half diameter.

A novel line current differential system is described suitable not only for breaker-and-a-half applications, but also for applications with up to four local inputs at each of the up to three terminals of the line. The solution is designed to produce correct restraining signal as per principle of differential protection without sending all the raw local currents between all terminals of the line. The solution incorporates CT saturation detection, charging current compensation and zero-sequence removal for application on tapped lines with power transformers [8].

The described algorithm is implemented on a relay [4] with thousands of unit-years of field experience.

6. REFERENCES

- [1] GE Publication GEK-112987A, 2005, *C60 Breaker Management Relay*, Instruction Manual.
- [2] B.Kasztenny, D.Sharpley, B.Campbell, M.Pozzuoli, "Fast Ground Directional Overcurrent Protection – Limitations and Solutions", in *Proc. 27th Annual Western Protective Relay Conference*, Spokane, WA, October 24-26, 2000.
- [3] GE Publication GEK-112989A, 2005, *D60 Line Distance Relay*, Instruction Manual.
- [4] GE Publication GEK-112994A, 2005, *L90 Line Differential Relay*, Instruction Manual.
- [5] A.Adamiak, G.Alexander, W.Premarlani, "A New Approach to Current Differential Protection for Transmission Lines", in *Proc. Electric Council of New England – Protective Relaying Committee Meeting*, Portsmouth, NH, October 22-23, 1998.
- [6] M.Adamiak, G.Alexander, W.Premarlani, E.Saulnier, B.Yazici, "Digital Current Differential System", U.S. Patent 5 809 045, Sep.15, 1998.
- [7] G.Brunello, I.Voloh, I.Hall, J.Fitch, "Current Differential Relaying – Coping with Communications Channel Asymmetry", in *Proc. 8th Developments in Power System Protection Conference*, Amsterdam, April 5-8, 2004, pp.821-4.
- [8] B.Kasztenny, B.Campbell, "Improved Line Current Differential Protective Relaying Method and Relay for in-Zone Tapped Transformers", U.S. Patent 6 829 544, Dec.7, 2004.

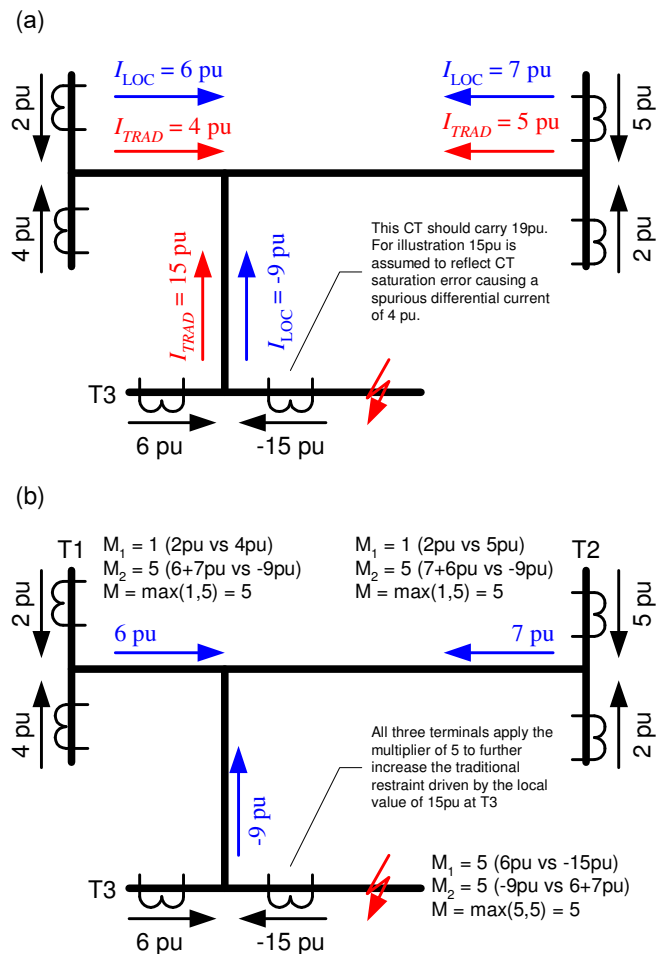


Fig.8. An example of calculating the restraints (a) and multipliers for CT saturation algorithm (b).