GE
Grid Solutions

MiCOM P40 Agile

P14D

Technical Manual
Feeder Management IED

Hardware Version: A
Software Version: 70
Publication Reference: P14DEd2-TM-EN-11.1

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CHAPTER 1

INTRODUCTION

1 CHAPTER OVERVIEW

This chapter provides some general information about the technical manual and an introduction to the device(s) described in this technical manual.

This chapter contains the following sections:

2 FOREWORD

This technical manual provides a functional and technical description of General Electric's P14D, as well as a comprehensive set of instructions for using the device. The level at which this manual is written assumes that you are already familiar with protection engineering and have experience in this discipline. The description of principles and theory is limited to that which is necessary to understand the product. For further details on general protection engineering theory, we refer you to General Electric's publication NPAG, which is available online or from our contact centre.

We have attempted to make this manual as accurate, comprehensive and user-friendly as possible. However we cannot guarantee that it is free from errors. Nor can we state that it cannot be improved. We would therefore be very pleased to hear from you if you discover any errors, or have any suggestions for improvement. Our policy is to provide the information necessary to help you safely specify, engineer, install, commission, maintain, and eventually dispose of this product. We consider that this manual provides the necessary information, but if you consider that more details are needed, please contact us.

All feedback should be sent to our contact centre via:

contact.centre@ge.com

2.1 TARGET AUDIENCE

This manual is aimed towards all professionals charged with installing, commissioning, maintaining, troubleshooting, or operating any of the products within the specified product range. This includes installation and commissioning personnel as well as engineers who will be responsible for operating the product.

The level at which this manual is written assumes that installation and commissioning engineers have knowledge of handling electronic equipment. Also, system and protection engineers have a thorough knowledge of protection systems and associated equipment.

2.2 TYPOGRAPHICAL CONVENTIONS

The following typographical conventions are used throughout this manual.

- The names for special keys appear in capital letters.
  For example: ENTER
- When describing software applications, menu items, buttons, labels etc as they appear on the screen are written in bold type.
  For example: Select **Save** from the file menu.
- Filenames and paths use the courier font
  For example: `Example\File.text`
- Special terminology is written with leading capitals
  For example: Sensitive Earth Fault
- If reference is made to the IED's internal settings and signals database, the menu group heading (column) text is written in upper case italics
  For example: The *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the setting cells and DDB signals are written in bold italics
  For example: The ***Language*** cell in the *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the value of a cell's content is written in the Courier font
  For example: The ***Language*** cell in the *SYSTEM DATA* column contains the value *`English`*

2.3 NOMENCLATURE

Due to the technical nature of this manual, many special terms, abbreviations and acronyms are used throughout the manual. Some of these terms are well-known industry-specific terms while others may be special product-specific terms used by General Electric. The first instance of any acronym or term used in a particular chapter is explained. In addition, a separate glossary is available on the General Electric website, or from the General Electric contact centre.

We would like to highlight the following changes of nomenclature however:

- The word 'relay' is no longer used to describe the device itself. Instead, the device is referred to as the 'IED' (Intelligent Electronic Device), the 'device', or the 'product'. The word 'relay' is used purely to describe the electromechanical components within the device, i.e. the output relays.
- British English is used throughout this manual.
- The British term 'Earth' is used in favour of the American term 'Ground'.

2.4 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

3 PRODUCT SCOPE

The P14D feeder management IED has been designed for the protection of a wide range of overhead lines and underground cables. The P14D provides integral directional and non-directional overcurrent, overvoltage and earth-fault protection and is suitable for application on solidly earthed, impedance earthed, Petersen coil earthed, and isolated systems.

In addition to the protection features, the devices include a comprehensive range of other features and measurements and recording facilities to aid with power system diagnosis and fault analysis.

The P14D can be used in various applications, depending on the chosen firmware. There are five different models according to which firmware is installed: P14DA, P14DB, P14DG, P14DL, P14DZ, P14DH.

- The P14DA is a compact device in a 20TE case
- The P14DB is the base device for general application
- The P14DG is for small generator applications
- The P14DL is for line protection
- The P14DZ is for high impedance earth fault applications
- The P14DH includes Wattmetric Directional Earth Fault protection

All models are available with a range of Input/Output options, which are described in the hardware design chapter and summarised in the ordering options.

A major advantage of the P40 Agile platform is its backward compatibility with the K-series products. The P40 Agile products have been designed such that the case, back panel terminal layout and pin-outs are identical to their K-series predecessors and can be retrofitted without the usual overhead associated with replacing and rewiring devices. This allows easy upgrade of the protection system with minimum impact and minimum shutdown time of the feeder.

This product is not only compatible with the K-series products in terms of hardware. It can be used as a direct replacement for the KMPC 130 not only is compatible in both terms of hardware and the measurements and communications options.

3.1 ORDERING OPTIONS

All current models and variants for this product are defined in an interactive spreadsheet called the CORTEC. This is available on the company website.

Alternatively, you can obtain it via the Contact Centre at:

contact.centre@ge.com

A copy of the CORTEC is also supplied as a static table in the Appendices of this document. However, it should only be used for guidance as it provides a snapshot of the interactive data taken at the time of publication.

4 FEATURES AND FUNCTIONS

4.1 PROTECTION FUNCTIONS

The P14D models offer the following protection functions:

ANSI	IEC 61850	Protection Function	P14DA	P14DB	P14DG	P14DH	P14DL	P14DZ
37		Undercurrent detection (low load)	Yes	Yes	Yes	Yes	Yes	Yes
46	NgcPTOC	Negative sequence overcurrent	Yes	Yes	Yes	Yes	Yes	Yes
46BC		Broken Conductor	Yes	Yes	Yes	Yes	Yes	Yes
49	ThmPTTR	Thermal Overload	Yes	Yes	Yes	Yes	Yes	Yes
50 SOTF		Switch onto Fault	Yes	Yes	Yes	Yes	Yes	Yes
50BF	RBRF	CB Failure	Yes	Yes	Yes	Yes	Yes	Yes
50	OcpPTOC	Definite time overcurrent protection	6 stages	6 stages	6 stages	6 stages	6 stages	6 stages
50N	EfdPTOC	Neutral/Ground Definite time overcurrent protection Measured and Derived (standard EF CT), Derived (SEF CT)	4 stages	4 stages	4 stages	4 stages	4 stages	4 stages
51	OcpPTOC	IDMT overcurrent protection (stages)	3 stages	3 stages	3 stages	3 stages	3 stages	3 stages
51N	EfdPTOC	Neutral/Ground IDMT overcurrent protection	2 stages	2 stages	2 stages	2 stages	2 stages	2 stages
67	OcpPTOC	Directional Phase Overcurrent	Yes	Yes	Yes	Yes	Yes	Yes
67N	EfdPTOC	Directional Neutral Overcurrent	Yes	Yes	Yes	Yes	Yes	Yes
		Wattmetric Earth Fault	Yes	Yes	Yes	Yes	Yes	Yes
		Wattmetric Directional Earth Fault (WDE protection)	No	No	No	Yes	No	No
		Cold load pick up	Yes	Yes	Yes	Yes	Yes	Yes
VTS		VT supervision	Yes	Yes	Yes	Yes	Yes	Yes
CTS		CT supervision	Yes	Yes	Yes	Yes	Yes	Yes
64N	RefPDIF	Restricted Earth Fault	Yes	Yes	Yes	Yes	Yes	Yes
		Sensitive Earth Fault (with SEF CT only)	Yes	Yes	Yes	Yes	Yes	Yes
68		2nd Harmonic Blocking	Yes	Yes	Yes	Yes	Yes	Yes
27	VtpPhsPTUV	Undervoltage	3 stages	3 stages	3 stages	3 stages	3 stages	3 stages
47		Negative sequence overvoltage	Yes	Yes	Yes	Yes	Yes	Yes
59	VtpPhsPTOV	Overvoltage	3 stages	3 stages	3 stages	3 stages	3 stages	3 stages
59N	VtpResPTOV	Residual Overvoltage	3 stages	3 stages	3 stages	3 stages	3 stages	3 stages
78		Voltage Vector Shift	No	No	Yes	No	Yes	Yes
81O	FrqPTOF	Overfrequency	No	9 stages	9 stages	9 stages	9 stages	9 stages
81U	FrqPTUF	Underfrequency	No	9 stages	9 stages	9 stages	9 stages	9 stages
81df/dt		Rate of change of frequency (df/dt)	No	9 stages	9 stages	9 stages	9 stages	9 stages
81V	DfpPFRC	Undervoltage blocking of frequency protection	No	Yes	Yes	Yes	Yes	Yes
		Programmable curves	Yes	Yes	Yes	Yes	Yes	Yes
51V		Voltage Controlled Overcurrent	Yes	Yes	Yes	Yes	Yes	Yes
		Voltage Restrained Overcurrent	No	No	Yes	Yes	Yes	Yes

ANSI	IEC 61850	Protection Function	P14DA	P14DB	P14DG	P14DH	P14DL	P14DZ
25		Check synchronising	No	No	Yes	Yes	Yes	Yes
32		Phase Directional Power	No	No	Yes	Yes	Yes	Yes
		Sensitive power	No	No	Yes	Yes	Yes	Yes
		Load Encroachment supervision (Load Blinders)	No	No	No	No	Yes	Yes
79	RREC	Autoreclose (3 phases)	No	No	No	No	4 shots	4 shots
21FL		Fault Locator	No	No	No	No	Yes	Yes
81RF	DfpPFRC	Frequency supervised rate of change of frequency	No	No	No	No	Yes	Yes
81RAV	DfpPFRC	Frequency supervised average rate of change of frequency	No	No	No	No	Yes	Yes
81R		Load Restoration	No	No	No	No	Yes	Yes
		Rate of change of voltage (dv/dt)	No	No	No	No	4 stages	4 stages
		Neutral Admittance protection	No	No	No	No	Yes	Yes
		Blocking scheme	Yes	Yes	Yes	Yes	Yes	Yes
		Programmable curves	Yes	Yes	Yes	Yes	Yes	Yes
		High Impedance Earth Fault	No	No	No	No	No	Yes
		CB Monitoring	No	No	No	No	No	Yes
86		Latching output contacts (Lockout)	Yes	Yes	Yes	Yes	Yes	Yes

4.2 CONTROL FUNCTIONS

Feature	IEC 61850	ANSI
Power-up diagnostics and continuous self-monitoring		
Fully customizable menu texts		
Function keys	FnkGGIO	
Alternative setting groups (4)		
Programmable LEDs	LedGGIO	
Programmable hotkeys		
Watchdog contacts		
Read-only mode		
NERC compliant cyber-security		
Programmable allocation of digital inputs and outputs		
Control inputs	PloGGIO1	
Graphical programmable scheme logic (PSL)		
Circuit breaker control, status & condition monitoring	XCBR	52
Trip circuit and coil supervision		
CT supervision (only for products with VT inputs)		
VT supervision (only for products with VT inputs)	TVTR	
Fault locator (only for products with VT inputs)	RFLO	

4.3 MEASUREMENT FUNCTIONS

The device offers the following measurement functions:

Measurement Function	Details
Measurements (Exact range of measurements depend on the device model)	• Measured currents and calculated sequence and RMS currents • Measured voltages and calculated sequence and RMS voltages • Power and energy quantities • Peak, fixed and rolling demand values • Frequency measurements • Others measurements
Disturbance records (waveform capture, oscillography) Channels / duration each or total / samples per cycle	9 / 10, 5 / 24
Fault Records	10
Maintenance Records	10
Event Records / Event logging	2048
Time Stamping of Opto-inputs	Yes

4.4 COMMUNICATION FUNCTIONS

The device offers the following communication functions:

Communication Function	Details
Local HMI	Yes
Multi-language HMI (English, French, German, Italian, Portuguese, Spanish, Russian)	Yes
Front port	USB
1st rear port	RS485 or IRIG-B
2nd rear port (optional)	RS485 or IRIG-B or single channel Ethernet or dual redundant Ethernet
Serial Protocols available	IEC 60870-5-103, MODBUS, Courier, DNP3
Ethernet Protocols available	IEC 61850, DNP3 over Ethernet, PRP, HSR
Virtual inputs	64
Cyber-security	Yes
Enhanced Studio (S1 Agile)	Yes

5 LOGIC DIAGRAMS

This technical manual contains many logic diagrams, which should help to explain the functionality of the device. Although this manual has been designed to be as specific as possible to the chosen product, it may contain diagrams, which have elements applicable to other products. If this is the case, a qualifying note will accompany the relevant part.

The logic diagrams follow a convention for the elements used, using defined colours and shapes. A key to this convention is provided below. We recommend viewing the logic diagrams in colour rather than in black and white. The electronic version of the technical manual is in colour, but the printed version may not be. If you need coloured diagrams, they can be provided on request by calling the contact centre and quoting the diagram number.

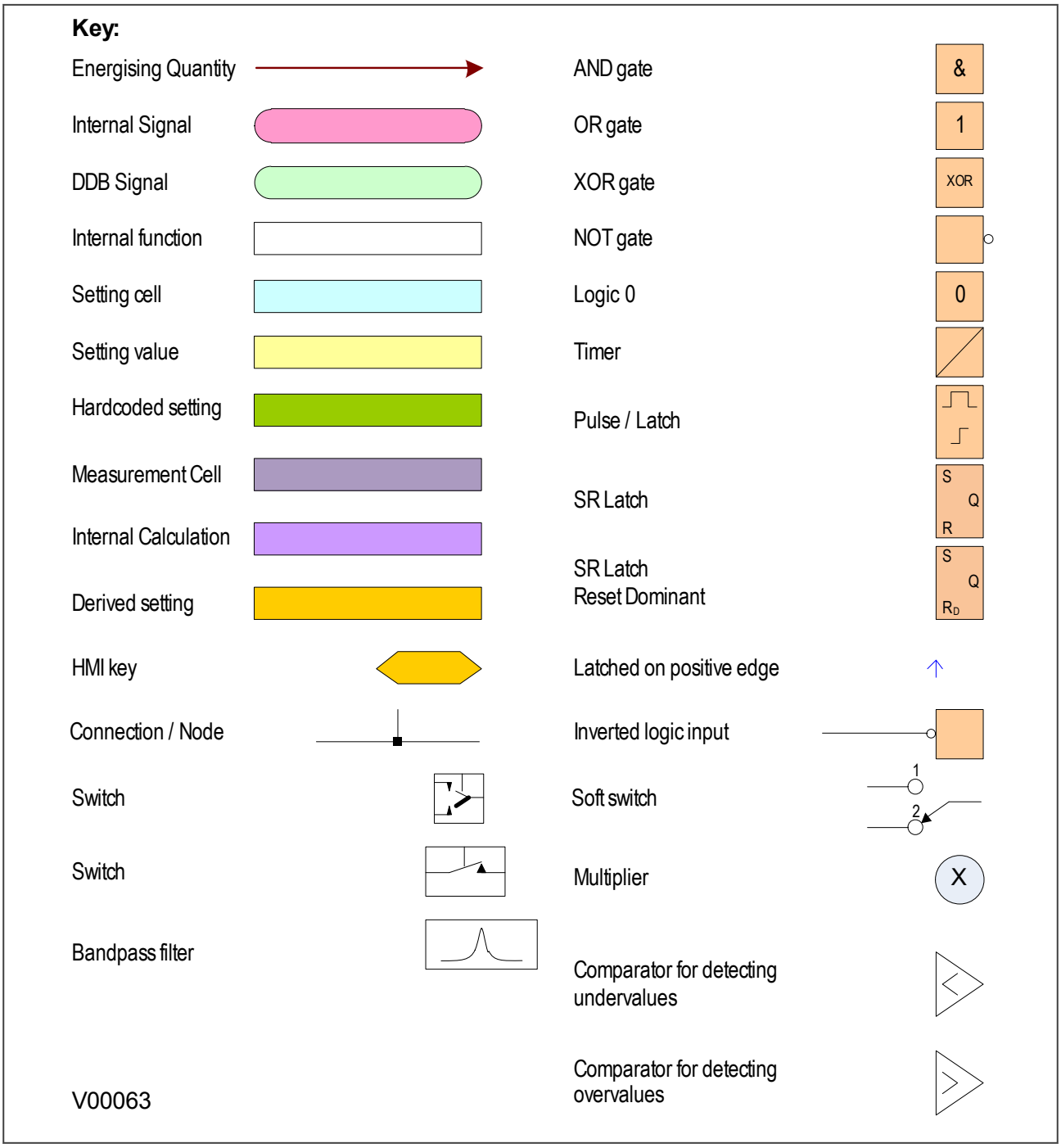


Figure 1: Key to logic diagrams

6 FUNCTIONAL OVERVIEW

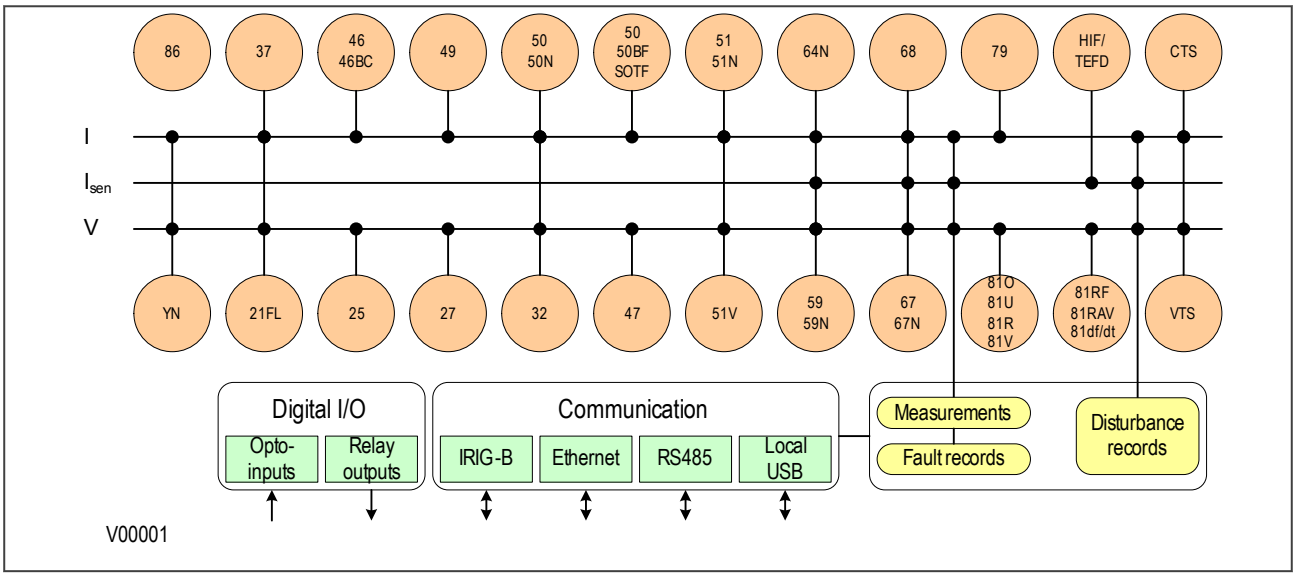


Figure 2: Functional Overview

CHAPTER 2

SAFETY INFORMATION

1 CHAPTER OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

This chapter contains the following sections:

2 HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

3 SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.

Caution:
Refer to equipment documentation. Failure to do so could result in damage to the equipment

Warning:
Risk of electric shock

Warning:
Risk of damage to eyesight

Earth terminal. *Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.*

Protective conductor (earth) terminal

Instructions on disposal requirements

Note:
The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

4 INSTALLATION, COMMISSIONING AND SERVICING

4.1 LIFTING HAZARDS

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

4.2 ELECTRICAL HAZARDS

Caution:
All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.

Caution:
Consult the equipment documentation before installing, commissioning, or servicing the equipment.

Caution:
Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.

Warning:
Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.

Warning:
Isolate the equipment before working on the terminal strips.

Warning:
Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.

Caution:
Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.

Warning:
NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.

Warning:
Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.

Caution:
Operate the equipment within the specified electrical and environmental limits.

Caution:
Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.

Note:
Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

4.3 UL/CSA/CUL REQUIREMENTS

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.

Caution:
Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).

Caution:
To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

4.4 FUSING REQUIREMENTS

Caution:
Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).

Caution:
Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).
For P50 models, use a 1A maximum T-type fuse.
For P60 models, use a 4A maximum T-type fuse.

Caution:
Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

Caution:
CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

4.5 EQUIPMENT CONNECTIONS

Warning:
Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.

Caution:
Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.
Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.

Caution:
Always use insulated crimp terminations for voltage and current connections.

Caution:
Always use the correct crimp terminal and tool according to the wire size.

Caution:
Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

4.6 PROTECTION CLASS 1 EQUIPMENT REQUIREMENTS

Caution:
Earth the equipment with the supplied PCT (Protective Conductor Terminal).

Caution:
Do not remove the PCT.

Caution:
The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.

Caution:
Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.

Caution:
The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations.
For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.

Caution:
The PCT connection must have low-inductance and be as short as possible.

Caution:
All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

4.7 PRE-ENERGISATION CHECKLIST

Caution:
Check voltage rating/polarity (rating label/equipment documentation).

Caution:
Check CT circuit rating (rating label) and integrity of connections.

Caution:
Check protective fuse or miniature circuit breaker (MCB) rating.

Caution:
Check integrity of the PCT connection.

Caution:
Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

4.8 PERIPHERAL CIRCUITRY

Warning:
Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.

Note:
For most General Electric equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.

Caution:
Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.

Warning:
Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.

Warning:
Data communication cables with accessible screens and/or screen conductors, (including optical fibre cables with metallic elements), may create an electric shock hazard in a sub-station environment if both ends of the cable screen are not connected to the same equipotential bonded earthing system.

To reduce the risk of electric shock due to transferred potential hazards:

i. The installation shall include all necessary protection measures to ensure that no fault currents can flow in the connected cable screen conductor.

ii. The connected cable shall have its screen conductor connected to the protective conductor terminal (PCT) of the connected equipment at both ends. This connection may be inherent in the connectors provided on the equipment but, if there is any doubt, this must be confirmed by a continuity test.

iii. The protective conductor terminal (PCT) of each piece of connected equipment shall be connected directly to the same equipotential bonded earthing system.

iv. If, for any reason, both ends of the cable screen are not connected to the same equipotential bonded earth system, precautions must be taken to ensure that such screen connections are made safe before work is done to, or in proximity to, any such cables.

v. No equipment shall be connected to any download or maintenance circuits or connectors of this product except temporarily and for maintenance purposes only.

vi. Equipment temporarily connected to this product for maintenance purposes shall be protectively earthed (if the temporary equipment is required to be protectively earthed), directly to the same equipotential bonded earthing system as the product.

Warning:
Small Form-factor Pluggable (SFP) modules which provide copper Ethernet connections typically do not provide any additional safety isolation. Copper Ethernet SFP modules must only be used in connector positions intended for this type of connection.

4.9 UPGRADING/SERVICING

Warning:
Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.

Caution:
Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

5 DECOMMISSIONING AND DISPOSAL

Caution:
Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.

Caution:
Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.

6 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

6.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

6.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

6.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

6.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL us

CHAPTER 3

HARDWARE DESIGN

1 CHAPTER OVERVIEW

This chapter provides information about the product's hardware design.

This chapter contains the following sections:

2 HARDWARE ARCHITECTURE

The main components comprising devices based on the P40Agile platform are as follows:

- The housing, consisting of a front panel and connections at the rear
- The Main processor module consisting of the main CPU (Central Processing Unit), memory and an interface to the front panel HMI (Human Machine Interface)
- An I/O board consisting of output relay contacts and digital opto-inputs
- Communication modules
- Power supply

All modules are connected by a parallel data and address bus, which allows the processor module to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sampled data from the input module to the CPU. These parallel and serial databuses are shown as a single interconnection module in the following figure, which shows typical modules and the flow of data between them.

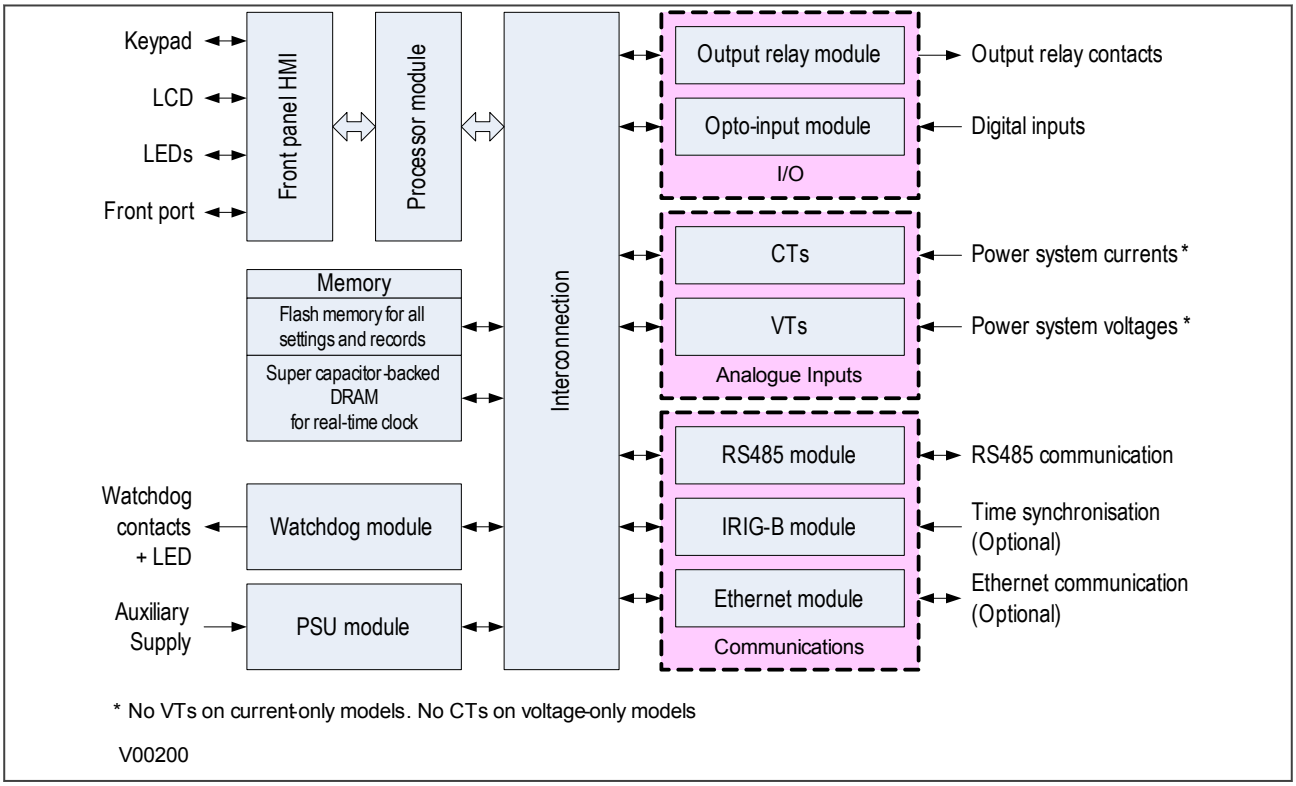


Figure 3: Hardware design overview

2.1 MEMORY AND REAL TIME CLOCK

The IED contains flash memory for storing the following operational information:

- Fault, Maintenance and Disturbance Records
- Events
- Alarms
- Measurement values
- Latched trips
- Latched contacts

Flash memory is non-volatile and therefore no backup battery is required.

A dedicated Supercapacitor keeps the on board real time clock operational for up to four days after power down.

3 MECHANICAL IMPLEMENTATION

All products based on the P40Agile platform have common hardware architecture. The hardware comprises two main parts; the cradle and the housing.

The cradle consists of the front panel which is attached to a carrier board into which all of the hardware boards and modules are connected. The products have been designed such that all the boards and modules comprising the product are fixed into the cradle and are not intended to be removed or inserted after the product has left the factory.

The housing comprises the housing metalwork and connectors at the rear into which the boards in the cradle plug into.

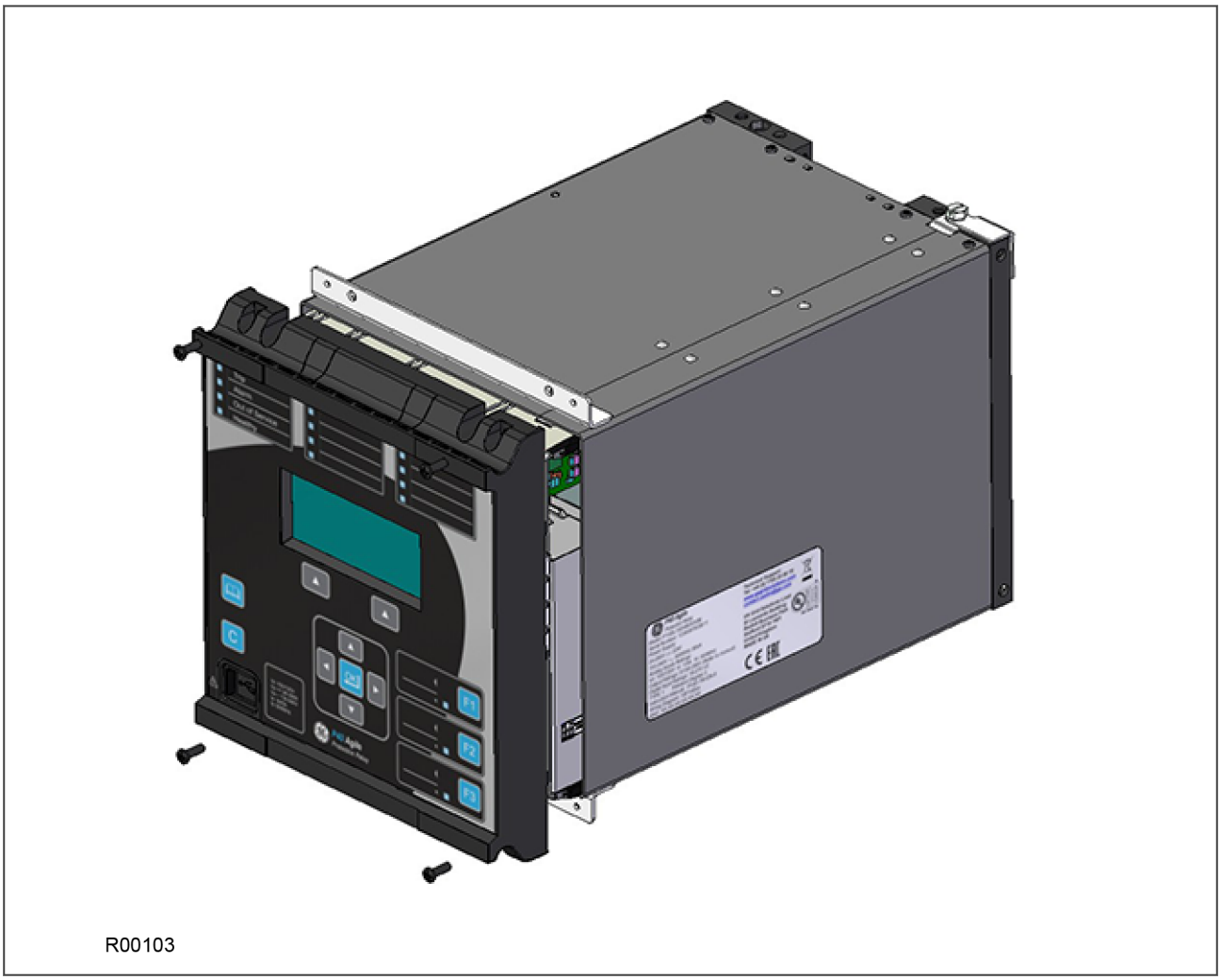


Figure 4: Exploded view of IED

3.1 HOUSING VARIANTS

The P40 Agile range of products are implemented in one of three case sizes. Case dimensions for industrial products usually follow modular measurement units based on rack sizes. These are: U for height and TE for width, where:

- 1U = 1.75 inches = 44.45 mm
- 1TE = 0.2 inches = 5.08 mm

The products are available in panel-mount or standalone versions. All products are nominally 4U high. This equates to 177.8 mm or 7 inches.

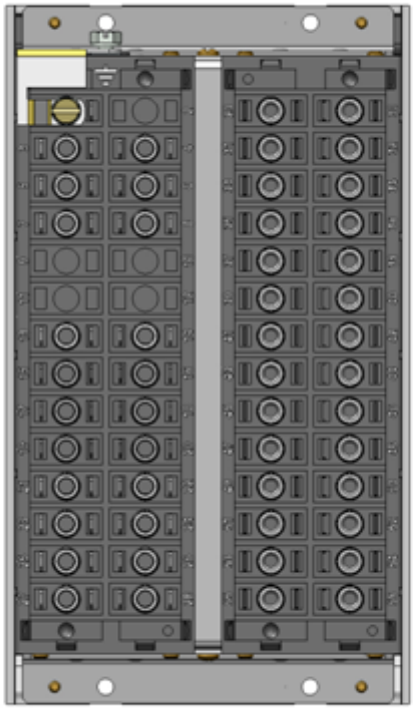
The cases are pre-finished steel with a conductive covering of aluminium and zinc. This provides good grounding at all joints, providing a low resistance path to earth that is essential for performance in the presence of external noise.

The case width depends on the product type and its hardware options. There are three different case widths for the described range of products: 20TE, 30TE and 40TE. The products in the P40Agile range can be used as a K-series refit and the cases, cradle, and pin-outs are completely inter-compatible. The case dimensions and compatibility criteria are as follows:

Case width (TE)	Case width (mm)	Equivalent K series
20TE	102.4 mm (4 inches)	KCGG140/142
30TE	154.2 mm (6 inches)	KCEG140/142
40TE	203.2 mm (8 inches)	KCEG140/142

3.2 20TE REAR PANEL

The 20TE rear panel consists of two MIDOS heavy duty terminal blocks.



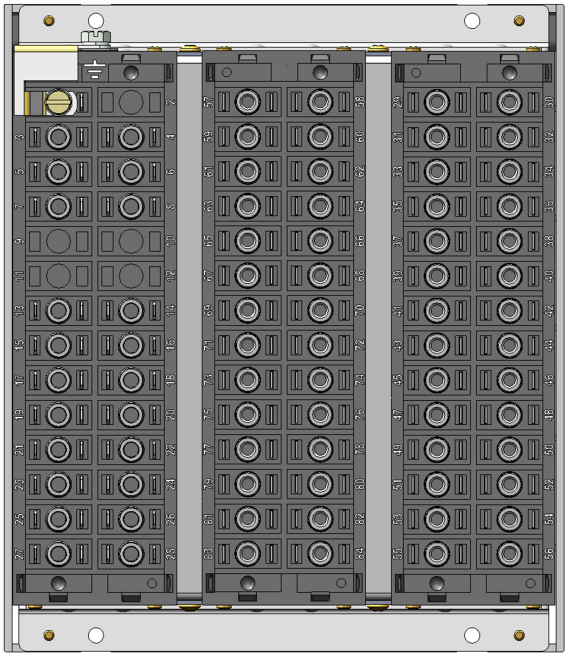
R00202

Figure 5: 20TE rear panel

3.3 30TE REAR PANEL

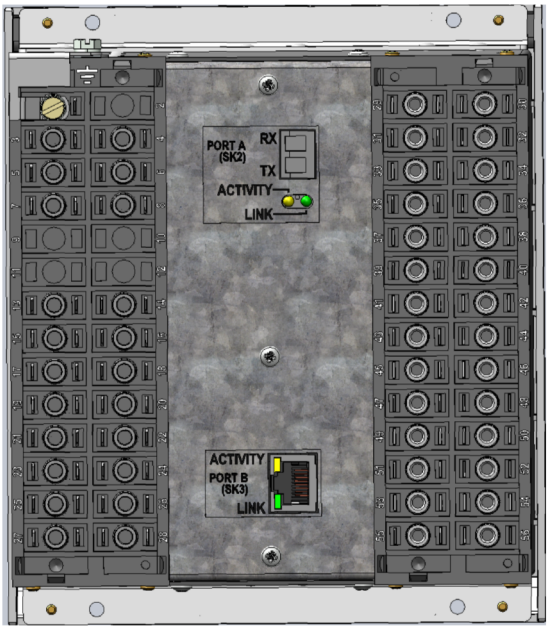
The 30TE rear panel consists of either:

- Three MIDOS heavy duty terminal blocks
- Two MIDOS heavy duty terminal blocks and a communication board
- Two MIDOS heavy duty terminal blocks and a blanking panel



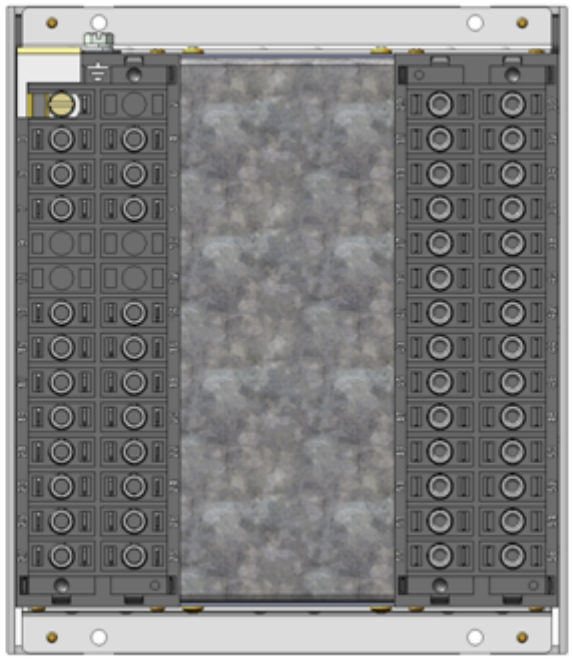
R00203

Figure 6: 30TE Three-MIDOS block rear panel



R00204

Figure 7: 30TE Two-MIDOS block + communications rear panel



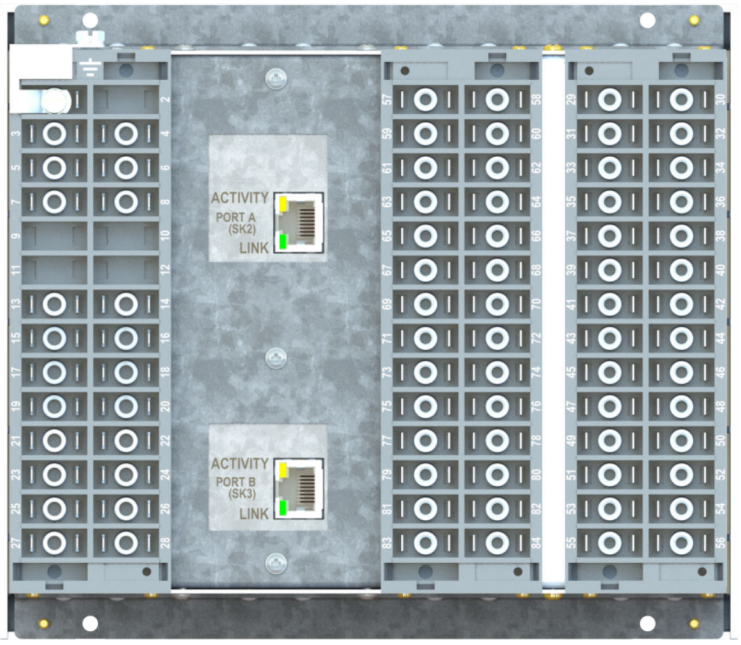
R00222

Figure 8: 30TE Two-MIDOS block + blanking plate

3.4 40TE REAR PANEL

The 40TE rear panel consists of:

- Three MIDOS heavy duty terminal blocks and a communication board



R00288

Figure 9: 40TE Three-MIDOS block + communications rear panel

4 TERMINAL CONNECTIONS

4.1 I/O OPTIONS

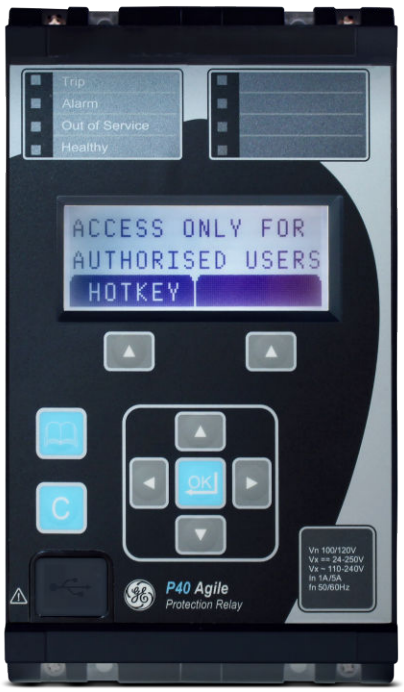
Component	I/O option A	I/O option B	I/O option C	I/O option D	I/O option E	I/O option F	I/O option G	I/O option H	I/O option J
Digital inputs	8 (1 group of 3 and 1 group of 5)	11 (2 groups of 3 and 1 group of 5)	11 (1 group of 3, 1 group of 5 and 3 individual)	13 (1 group of 3 and 2 groups of 5)	3 (1 group of 3)	6 (1 group of 3 and 3 individual)	7 1 group of 5 and 2 individual)	10 1 group of 3, 1 group of 5 and 2 individual)	12 (2 groups of 5 and 2 individual)
Output relays	8 (NO)	12 (NO)	12 (11 NO, 1 NC)	12 (NO)	4 (NO)	8 (7 NO, 1 NC)	8 (NO)	12 (NO)	12 (NO)

Note:
I/O options C, F, G, H and J are suitable for Trip Circuit Supervision (TCS) applications.

Note:
For details of terminal connections, refer to the Wiring Diagrams Appendix.

5 FRONT PANEL

5.1 20TE FRONT PANEL



R00100

Figure 10: Front panel (20TE)

The figures show the front panels for the 20TE variant.

It consists of:

- LCD display
- Keypad
- USB port
- 4 x fixed function tri-colour LEDs
- 4 x programmable tri-colour LEDs

5.2 30TE FRONT PANEL

R00101

Figure 11: Front panel (30TE)

The figures show the front panels for the 30TE variant.

It consists of:

- LCD display
- Keypad
- USB port
- 4 x fixed function tri-colour LEDs
- 8 x programmable tri-colour LEDs
- 3 x function keys
- 3 x tri-colour LEDs for the function keys

5.3 40TE FRONT PANEL

R00102

Figure 12: Front panel (40TE)

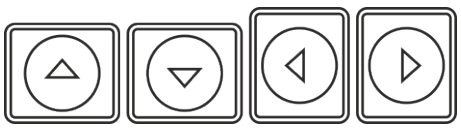
The figure shows the front panel for the 40TE variant.

It consists of:

- LCD display
- Keypad
- USB port
- 4 x fixed function tri-colour LEDs
- 8 x programmable tri-colour LEDs
- 3 x function keys
- 3 x tri-colour LEDs for the function keys

5.4 KEYPAD

The keypad consists of the following keys:

4 arrow keys to navigate the menus (organised around the Enter key)	
An enter key for executing the chosen option	

A clear key for clearing the last command	
A read key for viewing larger blocks of text (arrow keys now used for scrolling)	
2 hot keys for scrolling through the default display and for control of setting groups. These are situated directly below the LCD display.	

5.5 LIQUID CRYSTAL DISPLAY

The LCD is a high resolution monochrome display with 16 characters by 3 lines and controllable back light.

5.6 USB PORT

The USB port is situated on the front panel in the bottom left hand corner, and is used to communicate with a locally connected PC. It has two main purposes:

- To transfer settings information to/from the PC from/to the device.
- For downloading firmware updates and menu text editing.

The port is intended for temporary connection during testing, installation and commissioning. It is not intended to be used for permanent SCADA communications. This port supports the Courier communication protocol only. Courier is a proprietary communication protocol to allow communication with a range of protection equipment, and between the device and the Windows-based support software package.

You can connect the unit to a PC with a USB cable up to 5 m in length.

The inactivity timer for the front port is set to 15 minutes. This controls how long the unit maintains its level of password access on the front port. If no messages are received on the front port for 15 minutes, any password access level that has been enabled is cancelled.

Note:
The front USB port does not support automatic extraction of event and disturbance records, although this data can be accessed manually.

Caution:
When not in use, always close the cover of the USB port to prevent contamination.

5.7 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

5.8 FUNCTION KEYS

The programmable function keys are available for custom use for some models.

Factory default settings associate specific functions to these keys, but by using programmable scheme logic, you can change the default functions of these keys to fit specific needs. Adjacent to these function keys are programmable LEDs, which are usually set to be associated with their respective function keys.

5.9 PROGRAMABLE LEDS

The device has a number of programmable LEDs. All of the programmable LEDs on the unit are tri-colour and can be set to RED, YELLOW or GREEN.

In the 20TE case, four programmable LEDs are available. In 30TE and 40TE, eight are available.

CHAPTER 4

SOFTWARE DESIGN

1 CHAPTER OVERVIEW

This chapter describes the software design of the IED.

This chapter contains the following sections:

2 SOFTWARE DESIGN OVERVIEW

The range of products based on the P40 Agile platform can be conceptually categorised into several elements as follows:

- The system level software
- The platform software
- The protection and control software

These elements are not distinguishable to the user, and the distinction is made purely for the purposes of explanation.

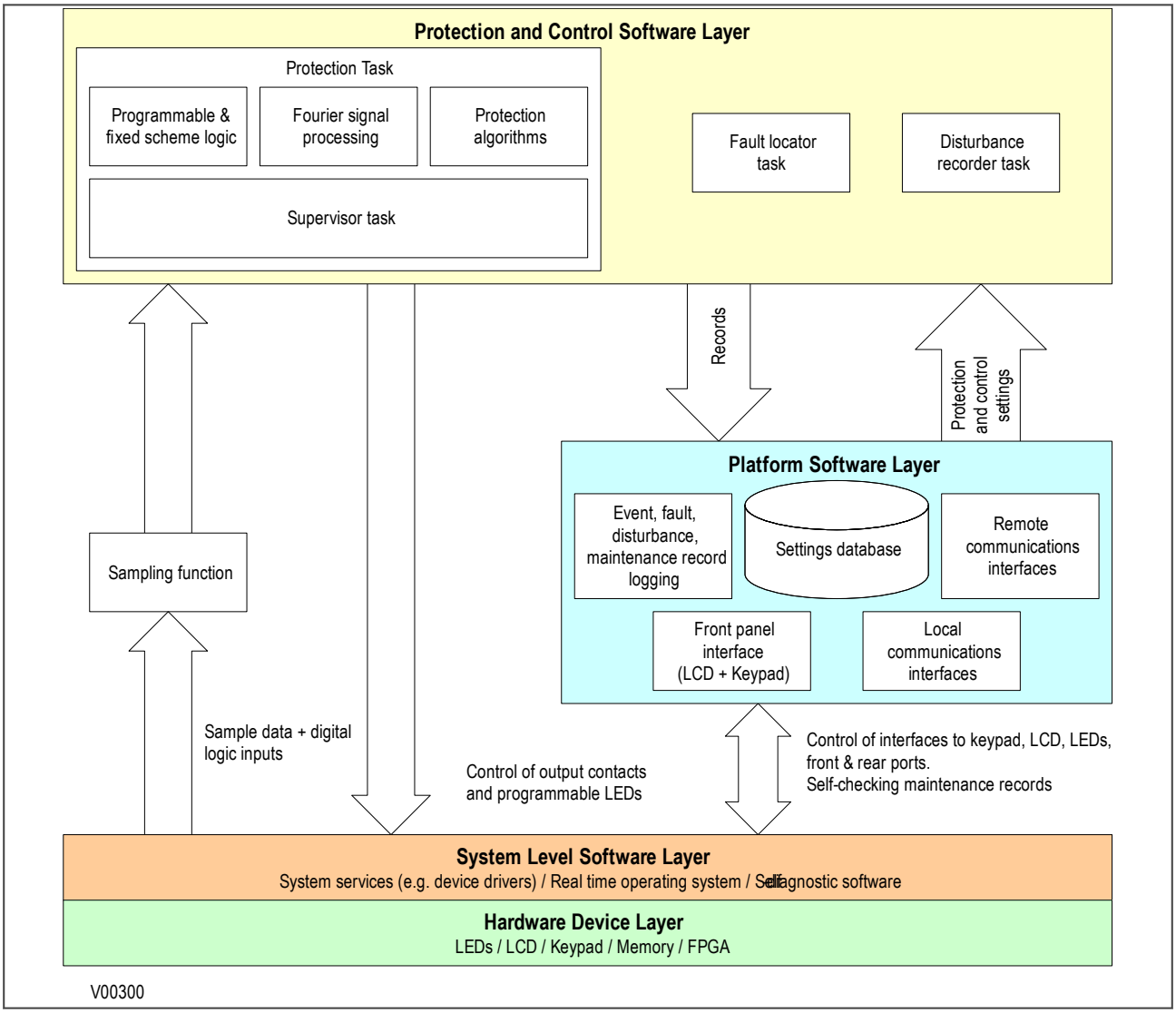


Figure 13: Software structure

The software can be divided into a number of functions as illustrated above. Each function is further broken down into a number of separate tasks. These tasks are then run according to a scheduler. They are run at either a fixed rate or they are event driven. The tasks communicate with each other as required.

3 SYSTEM LEVEL SOFTWARE

3.1 REAL TIME OPERATING SYSTEM

The real-time operating system is used to schedule the processing of the various tasks. This ensures that they are processed in the time available and in the desired order of priority. The operating system also plays a part in controlling the communication between the software tasks.

3.2 SYSTEM SERVICES SOFTWARE

The system services software provides the layer between the hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls things like the booting of the processor and the downloading of the processor code into RAM at startup.

3.3 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

3.4 STARTUP SELF-TESTING

The self-testing takes a few seconds to complete, during which time the IED's measurement, recording, control, and protection functions are unavailable. On a successful start-up and self-test, the 'Healthy' state LED on the front of the device is switched on. If a problem is detected during the start-up testing, the device remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

1. System boot
2. System software initialisation
3. Platform software initialisation and monitoring

3.4.1 SYSTEM BOOT

The integrity of the Flash memory is verified using a checksum before the program code and stored data is loaded into RAM for execution by the processor. When the loading has been completed, the data held in RAM is compared to that held in the Flash memory to ensure that no errors have occurred in the data transfer and that the two are the same. The entry point of the software code in RAM is then called. This is the IED's initialisation code.

3.4.2 SYSTEM LEVEL SOFTWARE INITIALISATION

The initialization process initializes the processor registers and interrupts, starts the watchdog timers (used by the hardware to determine whether the software is still running), starts the real-time operating system and creates and starts the supervisor task. In the initialization process the device checks the following:

- The status of the supercapacitor (which is used to back up the SRAM)
- The integrity of the non-volatile memory, which is used to store event, fault and disturbance records
- The operation of the LCD controller
- The watchdog operation

At the conclusion of the initialization software the supervisor task begins the process of starting the platform software.

3.4.3 PLATFORM SOFTWARE INITIALISATION AND MONITORING

When starting the platform software, the IED checks the following:

- The integrity of the data held in non-volatile memory (using a checksum)
- The operation of the real-time clock
- The optional IRIG-B function (if applicable)
- The presence and condition of the input board
- The analog data acquisition system (it does this by sampling the reference voltage)

At the successful conclusion of all of these tests the unit is entered into service and the application software is started up.

3.5 CONTINUOUS SELF-TESTING

When the IED is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software and the results are reported to the platform software. The functions that are checked are as follows:

- The Flash memory containing all program code and language text is verified by a checksum
- The code and constant data held in system memory is checked against the corresponding data in Flash memory to check for data corruption
- The system memory containing all data other than the code and constant data is verified with a checksum
- The integrity of the digital signal I/O data from the opto-isolated inputs and the output relay coils is checked by the data acquisition function every time it is executed.
- The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed. This is done by sampling the reference voltages
- The operation of the optional Ethernet board is checked by the software on the main processor card. If the Ethernet board fails to respond an alarm is raised and the card is reset in an attempt to resolve the problem.
- The operation of the optional IRIG-B function is checked by the software that reads the time and date from the board

In the event that one of the checks detects an error in any of the subsystems, the platform software is notified and it attempts to log a maintenance record.

If the problem is with the supercapacitor or IRIG-B board, the device continues in operation. For problems detected in any other area, the device initiates a shutdown and re-boot, resulting in a period of up to 10 seconds when the functionality is unavailable.

A restart should clear most problems that may occur. If, however, the diagnostic self-check detects the same problem that caused the IED to restart, it is clear that the restart has not cleared the problem, and the device takes itself permanently out of service. This is indicated by the ‘‘health-state’ LED on the front of the device, which switches OFF, and the watchdog contact which switches ON.

4 PLATFORM SOFTWARE

The platform software has three main functions:

- To control the logging of records generated by the protection software, including alarms, events, faults, and maintenance records
- To store and maintain a database of all of the settings in non-volatile memory
- To provide the internal interface between the settings database and the user interfaces, using the front panel interface and the front and rear communication ports

4.1 RECORD LOGGING

The logging function is used to store all alarms, events, faults and maintenance records. The records are stored in non-volatile memory to provide a log of what has happened. The IED maintains four types of log on a first in first out basis (FIFO). These are:

- Alarms
- Event records
- Fault records
- Maintenance records

The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software. The platform software is responsible for logging a maintenance record in the event of an IED failure. This includes errors that have been detected by the platform software itself or errors that are detected by either the system services or the protection software function. See the Monitoring and Control chapter for further details on record logging.

4.2 SETTINGS DATABASE

The settings database contains all the settings and data, which are stored in non-volatile memory. The platform software manages the settings database and ensures that only one user interface can modify the settings at any one time. This is a necessary restriction to avoid conflict between different parts of the software during a setting change.

Changes to protection settings and disturbance recorder settings, are first written to a temporary location SRAM memory. This is sometimes called 'Scratchpad' memory. These settings are not written into non-volatile memory immediately. This is because a batch of such changes should not be activated one by one, but as part of a complete scheme. Once the complete scheme has been stored in SRAM, the batch of settings can be committed to the non-volatile memory where they will become active.

4.3 INTERFACES

The settings and measurements database must be accessible from all of the interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each of the interfaces (LCD display, keypad and all the communications interfaces).

5 PROTECTION AND CONTROL FUNCTIONS

The protection and control software processes all of the protection elements and measurement functions. To achieve this it has to communicate with the system services software, the platform software as well as organise its own operations.

The protection task software has the highest priority of any of the software tasks in the main processor board. This ensures the fastest possible protection response.

The protection and control software provides a supervisory task, which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

5.1 ACQUISITION OF SAMPLES

After initialization, the protection and control task waits until there are enough samples to process. The acquisition of samples on the main processor board is controlled by a 'sampling function' which is called by the system services software.

This sampling function takes samples from the input module and stores them in a two-cycle FIFO buffer. The sample rate is 24 samples per cycle. This results in a nominal sample rate of 1,200 samples per second for a 50 Hz system and 1,440 samples per second for a 60 Hz system. However the sample rate is not fixed. It tracks the power system frequency as described in the next section.

5.2 FREQUENCY TRACKING

The device provides a frequency tracking algorithm so that there are always 24 samples per cycle irrespective of frequency drift within a certain frequency range (see technical specifications). If the frequency falls outside this range, the sample rate reverts to its default rate of 1200 Hz for 50 Hz or 1440 Hz for 60 Hz.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals. It works by detecting a change in the signal's measured phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module, in order to achieve a constant sample rate per cycle of the power waveform. The value of the tracked frequency is also stored for use by the protection and control task.

The frequency tracks off any voltage or current in the order VA, VB, VC, IA, IB, IC, down to 10%Vn for voltage and 5%In for current.

5.3 FOURIER SIGNAL PROCESSING

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. Although some protection algorithms use some Fourier-derived harmonics (e.g. second harmonic for magnetizing inrush), most protection functions are based on the Fourier-derived fundamental components of the measured analog signals. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms.

The Fourier components are calculated using single-cycle Fourier algorithm. This Fourier algorithm always uses the most recent 24 samples from the 2-cycle buffer.

Most protection algorithms use the fundamental component. In this case, the Fourier algorithm extracts the power frequency fundamental component from the signal to produce its magnitude and phase angle. This can be represented in either polar format or rectangular format, depending on the functions and algorithms using it.

The Fourier function acts as a filter, with zero gain at DC and unity gain at the fundamental, but with good harmonic rejection for all harmonic frequencies up to the nyquist frequency. Frequencies beyond this nyquist frequency are known as alias frequencies, which are introduced when the sampling frequency becomes less than twice the frequency component being sampled. However, the Alias frequencies are significantly attenuated by an anti-aliasing filter (low pass filter), which acts on the analog signals before they are sampled. The ideal cut-off point of an anti-aliasing low pass filter would be set at:

(samples per cycle) × (fundamental frequency)/2

At 24 samples per cycle, this would be nominally 600 Hz for a 50 Hz system, or 720 Hz for a 60 Hz system.

The following figure shows the nominal frequency response of the anti-alias filter and the Fourier filter for a 24-sample single cycle fourier algorithm acting on the fundamental component:

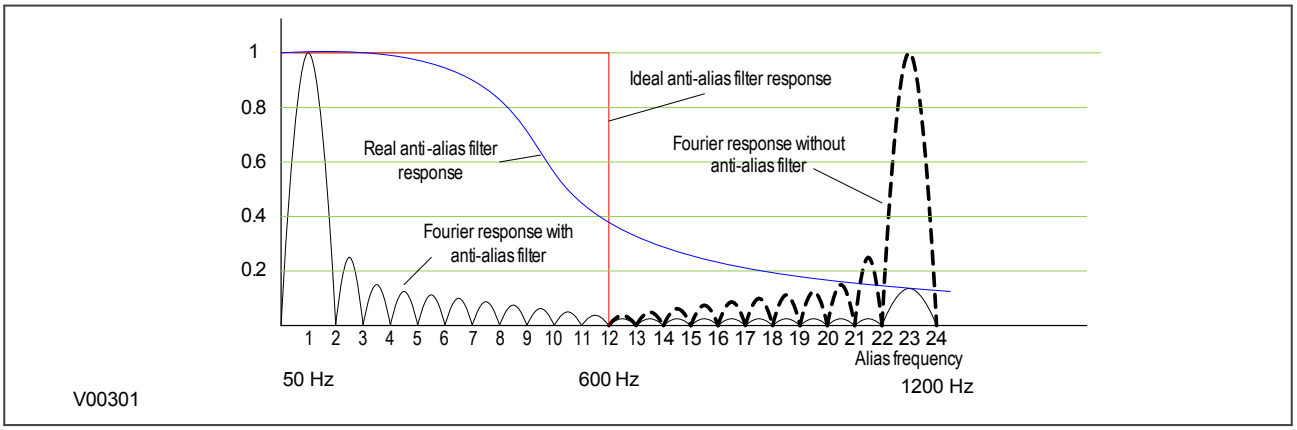


Figure 14: Frequency Response (indicative only)

5.4 PROGRAMMABLE SCHEME LOGIC

The purpose of the programmable scheme logic (PSL) is to allow you to configure your own protection schemes to suit your particular application. This is done with programmable logic gates and delay timers. To allow greater flexibility, different PSL is allowed for each of the four setting groups.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic (FSL). The fixed scheme logic provides the standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven. The logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

The PSL can be configured to create very complex schemes. Because of this PSL desing is achieved by means of a PC support package called the PSL Editor. This is available as part of the settings application software MiCOm S1 Agile, or as a standalone software module.

5.5 EVENT RECORDING

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer controlled by the supervisor task. When the supervisor task receives an event record, it instructs the platform software to create the appropriate log in non-volatile memory (flash memory). The operation of the record logging to SRAM is slower than the supervisor buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost, if the supervisor buffer is full before the platform software is able to create a new log in SRAM. If this occurs then an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner, with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem.

For more information, see the Monitoring and Control chapter.

5.6 DISTURBANCE RECORDER

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms of the calibrated analog channels, plus the values of the digital signals. The recording time is user selectable up to a maximum of 10.5 seconds. The disturbance recorder is supplied with data by the protection and control task once per cycle, and collates the received data into the required length disturbance record. The disturbance records can be extracted using application software or the SCADA system, which can also store the data in COMTRADE format, allowing the use of other packages to view the recorded data.

For more information, see the Monitoring and Control chapter.

5.7 FAULT LOCATOR

The fault locator uses 12 cycles of the analog input signals to calculate the fault location. The result is returned to the protection and control task, which includes it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record. When the fault record is complete, including the fault location, the protection and control task sends a message to the supervisor task to log the fault record.

The Fault Locator is not available on all models.

5.8 FUNCTION KEY INTERFACE

The function keys interface directly into the PSL as digital input signals. A change of state is only recognized when a key press is executed on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed. It can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up thus allowing the function key state to be reinstated after power-up, should power be inadvertently lost.

CHAPTER 5

CONFIGURATION

1 CHAPTER OVERVIEW

Each product has different configuration parameters according to the functions it has been designed to perform. There is, however, a common methodology used across the entire product series to set these parameters.

Some of the communications setup can only be carried out using the HMI, and cannot be carried out using settings applications software. This chapter includes concise instructions of how to configure the device, particularly with respect to the communications setup, as well as a description of the common methodology used to configure the device in general.

This chapter contains the following sections:

2 SETTINGS APPLICATION SOFTWARE

To configure this device you will need to use the Settings Application Software. The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for setting up and managing the IEDs.

Although you can change many settings using the front panel HMI, some of the features cannot be configured without the Settings Application Software; for example the programmable scheme logic, or IEC61850 communications.

If you do not already have a copy of the Settings Application Software, you can obtain it from General Electric contact centre.

To configure your product, you will need a data model that matches your product. When you launch the Settings Application Software, you will be presented with a panel that allows you to invoke the “Data Model Manager”. This will close the other aspects of the software in order to allow an efficient import of the chosen data model. If you don’t have, or can’t find, the data model relating to your product, please call the General Electric contact centre.

When you have loaded all the data models you need, you should restart the Settings Application Software and start to create a model of your system using the “System Explorer” panel.

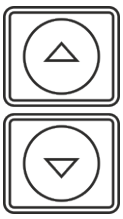
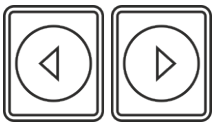
The software is designed to be intuitive, but help is available in an online help system and also the Settings Application Software user guide P40-M&CR-SAS-UG-EN-n, where 'Language' is a 2 letter code designating the language version of the user guide and 'n' is the latest version of the settings application software.

3 USING THE HMI PANEL

Using the HMI, you can:

- Display and modify settings
- View the digital I/O signal status
- Display measurements
- Display fault records
- Reset fault and alarm indications

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the LCD.

Keys	Description	Function
	Up and down cursor keys	To change the menu level or change between settings in a particular column, or changing values within a cell
	Left and right cursor keys	To change default display, change between column headings, or changing values within a cell
	ENTER key	For changing and executing settings
	Hotkeys	For executing commands and settings for which shortcuts have been defined
	Cancel key	To return to column header from any menu cell
	Read key	To read alarm messages
	Function keys (not all models)	For executing user programmable functions

Note:
As the LCD display has a resolution of 16 characters by 3 lines, some of the information is in a condensed mnemonic form.

3.1 NAVIGATING THE HMI PANEL

The cursor keys are used to navigate the menus. These keys have an auto-repeat function if held down continuously. This can be used to speed up both setting value changes and menu navigation. The longer the key is held pressed, the faster the rate of change or movement.

The navigation map below shows how to navigate the menu items.

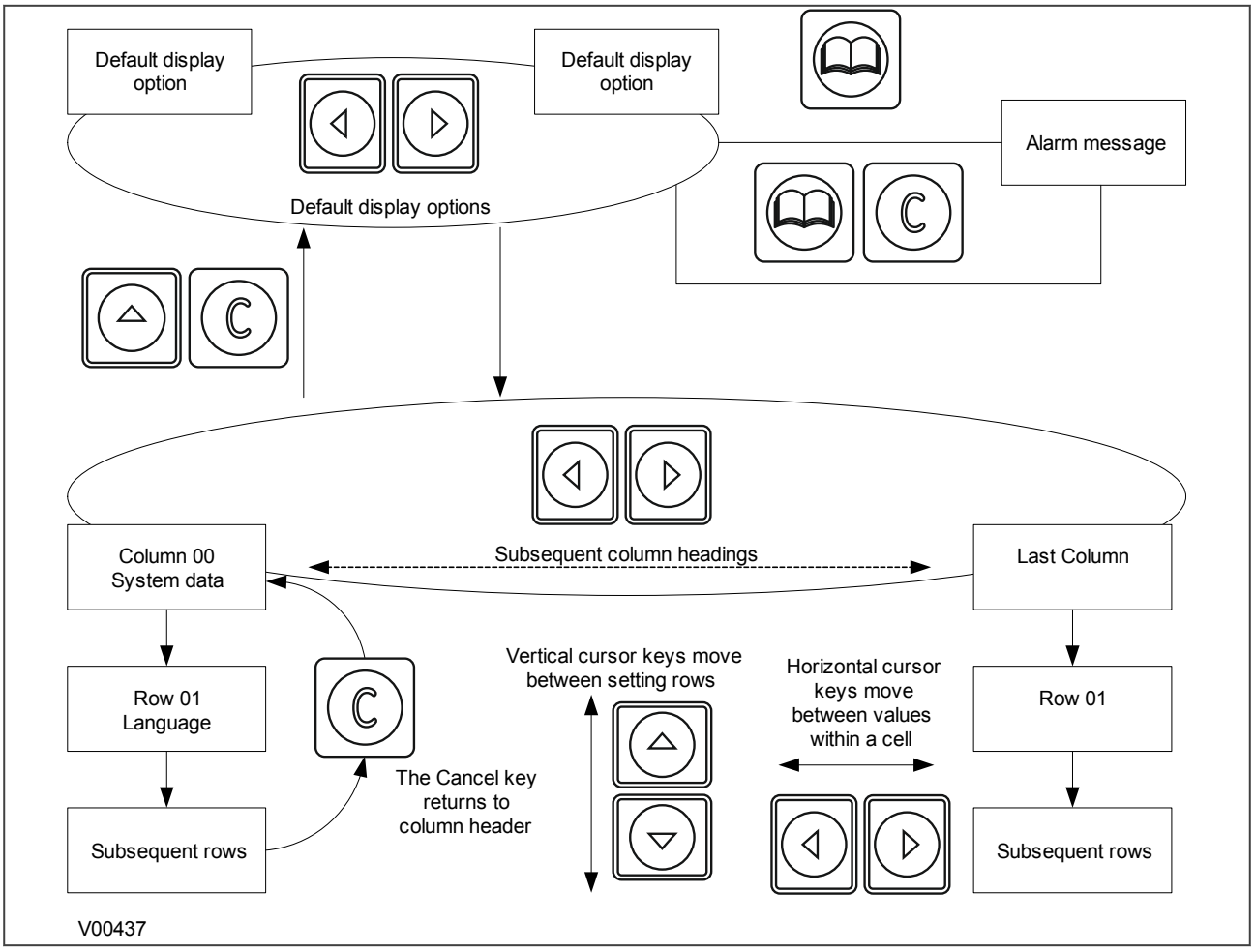


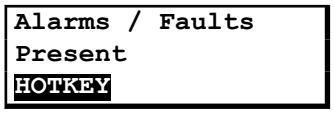
Figure 15: Navigating the HMI

3.2 GETTING STARTED

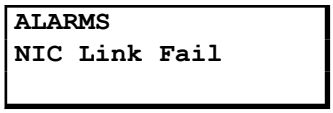
When you first start the IED, it will go through its power up procedure. After a few seconds it will settle down into one of the top level menus. There are two menus at this level:

- The Alarms menu for when there are alarms present
- The default display menu for when there are no alarms present.

If there are alarms present, the yellow Alarms LED will be flashing and the menu display will read as follows:



Even though the device itself should be in full working order when you first start it, an alarm could still be present, for example, if there is no network connection for a device fitted with a network card. If this is the case, you can read the alarm by pressing the 'Read' key.



If the device is fitted with an Ethernet card, you will first need to connect the device to an active Ethernet network to clear the alarm and get the default display.

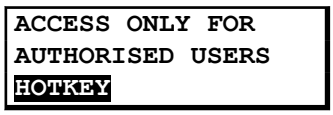
If there are other alarms present, these must also be cleared before you can get into the default display menu options.

3.3 DEFAULT DISPLAY

The HMI contains a range of possible options that you can choose to be the default display. The options available are:

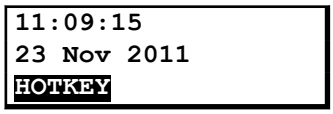
NERC Compliant banner

If the device is a cyber-security model, it will provide a NERC-compliant default display. If the device does not contain the cyber-security option, this display option is not available.



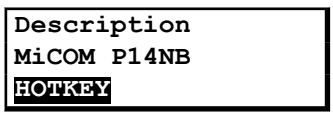
Date and time

For example:



Description (user-defined)

For example:



Plant reference (user-defined)

For example:

```
Plant Reference
MiCOM
HOTKEY
```

Access Level

For example:

```
Access Level
3
HOTKEY
```

In addition to the above, there are also displays for the system voltages, currents, power and frequency etc., depending on the device model.

3.4 DEFAULT DISPLAY NAVIGATION

The following diagram is an example of the default display navigation. In this example, we have used a cyber-secure model. This is an example only and may not apply in its entirety to all models. The actual display options available depend on the exact model.

Use the horizontal cursor keys to step through from one display to the next.

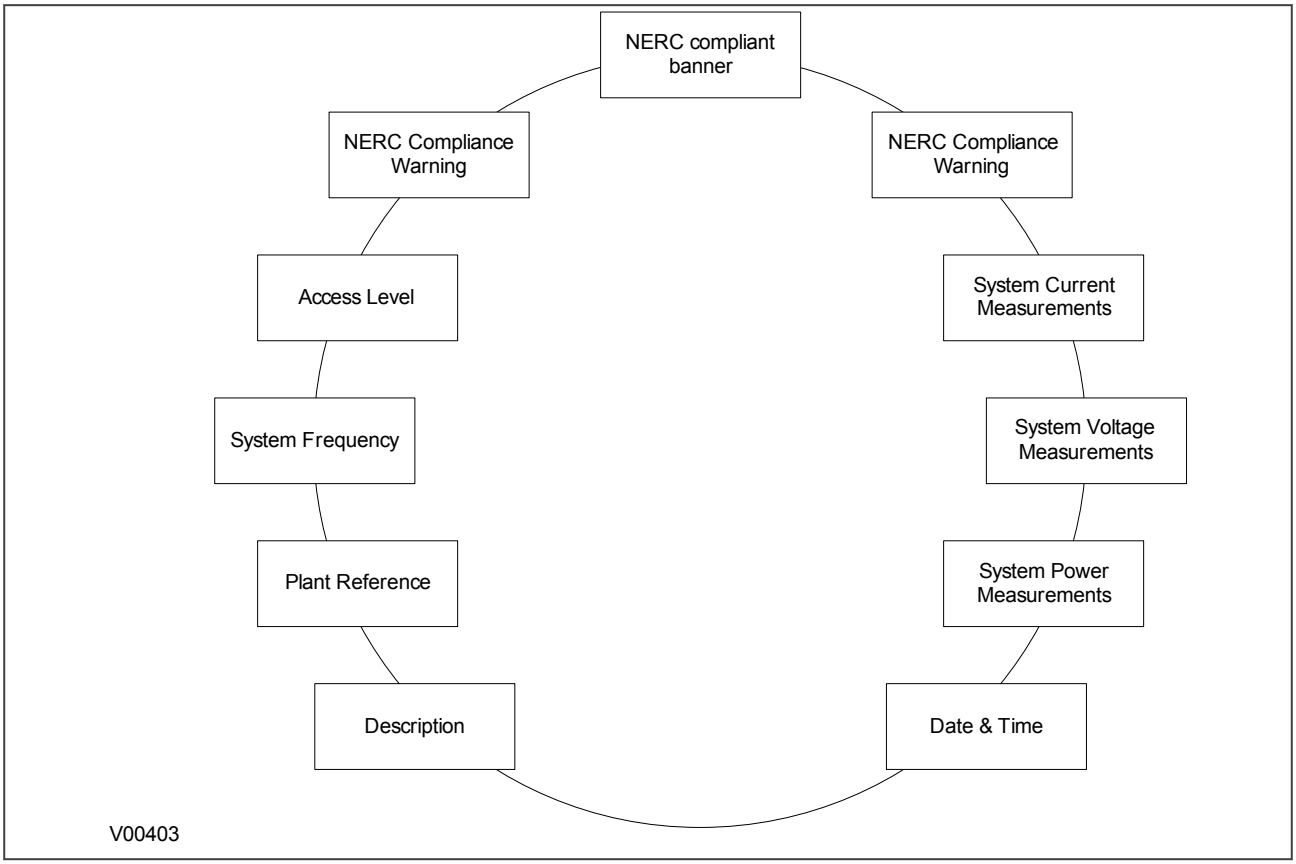
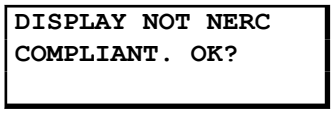


Figure 16: Default display navigation

If the device is cyber-secure but is not yet configured for NERC compliance (see Cyber-security chapter), a warning will appear when moving from the "NERC compliant" banner. The warning message is as follows:



You will have to confirm with the **Enter** button before you can go any further.

Note:
Whenever the IED has an uncleared alarm the default display is replaced by the text Alarms/ Faults present. You cannot override this default display. However, you can enter the menu structure from the default display, even if the display shows the Alarms/Faults present message.

3.5 PASSWORD ENTRY

Configuring the default display (in addition to modification of other settings) requires level 3 access. You will be prompted for a password before you can make any changes, as follows. The default level 3 password is AAAA.

1. A flashing cursor shows which character field of the password can be changed. Press the up or down cursor keys to change each character (tip: pressing the up arrow once will return an upper case "A" as required by the default level 3 password).
2. Use the left and right cursor keys to move between the character fields of the password.
3. Press the **Enter** key to confirm the password. If you enter an incorrect password, an invalid password message is displayed then the display reverts to ***Enter password***. On entering a valid password a message appears indicating that the password is correct and which level of access has been unlocked. If this level is sufficient to edit the selected setting, the display returns to the setting page to allow the edit to continue. If the correct level of password has not been entered, the password prompt page appears again.
4. To escape from this prompt press the **Clear** key. Alternatively, enter the password using the ***Password*** setting in the *SYSTEM DATA* column. If the keypad is inactive for 15 minutes, the password protection of the front panel user interface reverts to the default access level.

To manually reset the password protection to the default level, select ***Password***, then press the CLEAR key instead of entering a password.

Note:
In the SECURITY CONFIG column, you can set the maximum number of attemps, the time window in which the failed attempts are counted and the time duration for which the user is blocked.

3.6 PROCESSING ALARMS AND RECORDS

If there are any alarm messages, they will appear on the default display and the yellow alarm LED flashes. The alarm messages can either be self-resetting or latched. If they are latched, they must be cleared manually.

1. To view the alarm messages, press the **Read** key. When all alarms have been viewed but not cleared, the alarm LED changes from flashing to constantly on, and the latest fault record appears (if there is one).
2. Scroll through the pages of the latest fault record, using the cursor keys. When all pages of the fault record have been viewed, the following prompt appears.

```
Press Clear To
Reset Alarms
```

3. To clear all alarm messages, press the **Clear** key. To return to the display showing alarms or faults present, and leave the alarms uncleared, press the **Read** key.
4. Depending on the password configuration settings, you may need to enter a password before the alarm messages can be cleared.
5. When all alarms are cleared, the yellow alarm LED switches off. If the red LED was on, this will also be switched off.

Note:
*To speed up the procedure, you can enter the alarm viewer using the **Read** key and subsequently pressing the **Clear** key. This goes straight to the fault record display. Press the **Clear** key again to move straight to the alarm reset prompt, then press the **Clear** key again to clear all alarms.*

3.7 MENU STRUCTURE

Settings, commands, records and measurements are stored in a local database inside the IED. When using the Human Machine Interface (HMI) it is convenient to visualise the menu navigation system as a table. Each item in the menu is known as a cell, which is accessed by reference to a column and row address. Each column and row is assigned a 2-digit hexadecimal numbers, resulting in a unique 4-digit cell address for every cell in the database. The main menu groups are allocated columns and the items within the groups are allocated rows, meaning a particular item within a particular group is a cell.

Each column contains all related items, for example all of the disturbance recorder settings and records are in the same column.

There are three types of cell:

- Settings: this is for parameters that can be set to different values
- Commands: this is for commands to be executed
- Data: this is for measurements and records to be viewed, which are not settable

Note:
Sometimes the term "Setting" is used generically to describe all of the three types.

The table below, provides an example of the menu structure:

SYSTEM DATA (Col 00)	VIEW RECORDS (Col 01)	MEASUREMENTS 1 (Col 02)	...
Language (Row 01)	"Select Event [0...n]" (Row 01)	IA Magnitude (Row 01)	...
Password (Row 02)	Menu Cell Ref (Row 02)	IA Phase Angle (Row 02)	...
Sys Fn Links (Row 03)	Time & Date (Row 03)	IB Magnitude (Row 03)	...
...	...	...	...

It is convenient to specify all the settings in a single column, detailing the complete Courier address for each setting. The above table may therefore be represented as follows:

Setting	Column	Row	Description
SYSTEM DATA	**00**	**00**	**First Column definition**
Language (Row 01)	00	01	First setting within first column
Password (Row 02)	00	02	Second setting within first column
Sys Fn Links (Row 03)	00	03	Third setting within first column
...	...	...	
VIEW RECORDS	**01**	**00**	**Second Column definition**
Select Event [0...n]	01	01	First setting within second column
Menu Cell Ref	01	02	Second setting within second column
Time & Date	01	03	Third setting within second column
...	...	...	
MEASUREMENTS 1	**02**	**00**	**Third Column definition**
IA Magnitude	02	01	First setting within third column
IA Phase Angle	02	02	Second setting within third column
IB Magnitude	02	03	Third setting within third column
...	...	...	

The first three column headers are common throughout much of the product ranges. However the rows within each of these column headers may differ according to the product type. Many of the column headers are the same for all products within the series. However, there is no guarantee that the addresses will be the same for a particular column header. Therefore you should always refer to the product settings documentation and not make any assumptions.

3.8 CHANGING THE SETTINGS

1. Starting at the default display, press the **Down** cursor key to show the first column heading.
2. Use the horizontal cursor keys to select the required column heading.
3. Use the vertical cursor keys to view the setting data in the column.
4. To return to the column header, either press the Up cursor key for a second or so, or press the **Clear** key once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the Up cursor key or the **Clear** key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
7. To change the setting value, press the **Up** and **Down** cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the horizontal cursor keys.

8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the Down cursor key. Before returning to the default display, the following prompt appears.

```
Update settings?
ENTER or CLEAR
```

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

Note:
*For the protection group and disturbance recorder settings, if the menu time-out occurs before the changes have been confirmed, the setting values are discarded. Control and support settings, howeverr, are updated immediately after they are entered, without the **Update settings?** prompt.*

3.9 DIRECT ACCESS (THE HOTKEY MENU)

For settings and commands that need to be executed quickly or on a regular basis, the IED provides a pair of keys directly below the LCD display. These so called **Hotkeys** can be used to execute specified settings and commands directly.

The functions available for direct access using these keys are:

- Setting group selection
- Control inputs
- Circuit Breaker (CB) control functions

The availability of these functions is controlled by the ***Direct Access*** cell in the *CONFIGURATION* column. There are four options: `Disabled`, `Enabled`, `CB Ctrl only` and `Hotkey only`.

For the Setting Group selection and Control inputs, this cell must be set to either `Enabled` or `Hotkey only`. For CB Control functions, the cell must be set to `Enabled` or `CB Ctrl only`.

3.9.1 SETTING GROUP SELECTION USING HOTKEYS

In some models you can use the hotkey menu to select the settings group. By default, only Setting group 1 is enabled. Other setting groups will only be available if they are first enabled. To be able to select a different setting group, you must first enable them in the *CONFIGURATION* column.

To access the hotkey menu from the default display, you press the key directly below the HOTKEY text on the LCD. The following screen will appear.

```
←User32 STG GP→
HOTKEY MENU
              EXIT
```

Use the right cursor keys to enter the *SETTING GROUP* menu.

```
←Menu User01→
SETTING GROUP 1
Nxt Grp Select
```

Select the setting group with ***Nxt Grp*** and confirm by pressing ***Select***. If neither of the cursor keys is pressed within 20 seconds of entering a hotkey sub menu, the device reverts to the default display.

3.9.2 CONTROL INPUTS

The control inputs are user-assignable functions. You can use the *CTRL I/P CONFIG* column to configure the control inputs for the hotkey menu. In order to do this, use the first setting ***Hotkey Enabled*** cell to enable or disable any of the 32 control inputs. You can then set each control input to latched or pulsed and set its command to *On/Off*, *Set/Reset*, *In/Out*, or *Enabled/Disabled*.

By default, the hotkey is enabled for all 32 control inputs and they are set to *Set/Reset* and are *Latched*.

To access the hotkey menu from the default display, you press the key directly below the HOTKEY text on the LCD. The following screen will appear.

```
←User32 STG GP→
HOTKEY MENU
              EXIT
```

Press the right cursor key twice to get to the first control input, or the left cursor key to get to the last control input.

```
←STP GP User02→
Control Input 1
EXIT SET
```

Now you can execute the chosen function (Set/Reset in this case).

If neither of the cursor keys is pressed within 20 seconds of entering a hotkey sub menu, the device reverts to the default display.

3.9.3 CIRCUIT BREAKER CONTROL

You can open and close the controlled circuit breaker with the hotkey to the right, if enabled as described above. By default, hotkey access to the circuit breakers is disabled.

If hotkeyaccess to the circuit breakers has been enabled, the bottom right hand part of the display will read "Open or Close" depending on whether the circuit breaker is closed or open respectively:

For example:

```
Plant Reference
MiCOM
HOTKEY  CLOSE
```

To close the circuit breaker (in this case), press the key directly below CLOSE. You will be given an option to cancel or confirm.

```
Execute
CB CLOSE
Cancel Confirm
```

More detailed information on this can be found in the Monitoring and Control chapter.

3.10 FUNCTION KEYS

Most products have a number of function keys for programming control functionality using the programmable scheme logic (PSL).

Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are in the *FUNCTION KEYS* column.

The first cell down in the *FUNCTION KEYS* column is the ***Fn Key Status*** cell. This contains a binary string, which represents the function key commands. Their status can be read from this binary string.

```
FUNCTION KEYS
Fn Key Status
0000000000
```

The next cell down (***Fn Key 1***) allows you to activate or disable the first function key (1). The ***Lock*** setting allows a function key to be locked. This allows function keys that are set to *Toggled* mode and their DDB signal active 'high', to be locked in their active state, preventing any further key presses from deactivating the associated function. Locking a function key that is set to the Normal mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

```
FUNCTION KEYS
Fn Key 1
Unlocked
```

The next cell down (***Fn Key 1 Mode***) allows you to set the function key to *Normal* or *Toggled*. In the Toggle mode the function key DDB signal output stays in the set state until a reset command is given, by activating the function key on the next key press. In the Normal mode, the function key DDB signal stays energised for as long as the function key is pressed then resets automatically. If required, a minimum pulse width can be programmed by adding a minimum pulse timer to the function key DDB output signal.

```
FUNCTION KEYS
Fn Key 1 Mode
Toggled
```

The next cell down (***Fn Key 1 Label***) allows you to change the label assigned to the function. The default label is *Function key 1* in this case. To change the label you need to press the enter key and then change the text on the bottom line, character by character. This text is displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

```
FUNCTION KEYS
Fn Key 1 Label
Function Key 1
```

Subsequent cells allow you to carry out the same procedure as above for the other function keys.

The status of the function keys is stored in non-volatile memory. If the auxiliary supply is interrupted, the status of all the function keys is restored. The IED only recognises a single function key press at a time and a minimum key

press duration of approximately 200 ms is required before the key press is recognised. This feature avoids accidental double presses.

4 DATE AND TIME CONFIGURATION

The date and time setting will normally be updated automatically by the chosen UTC (Universal Time Co-ordination) time synchronisation mechanism when the device is in service. You can also set the date and time manually using the ***Date/Time*** cell in the *DATE AND TIME* column.

4.1 TIME ZONE COMPENSATION

The UTC time standard uses Greenwich Mean Time as its standard. Without compensation, the date and time would be displayed on the device irrespective of its location.

You may wish to display the local time corresponding to its geographical location. You can do this with the settings ***LocalTime Enable*** and ***LocalTime Offset***.

The ***LocalTime Enable*** has three setting options; `Disabled`, `Fixed`, and `Flexible`.

With `Disabled`, no local time zone is maintained. Time synchronisation from any interface will be used to directly set the master clock. All times displayed on all interfaces will be based on the master clock with no adjustment.

With `Fixed`, a local time zone adjustment is defined using the ***LocalTime Offset*** setting and all non-IEC 61850 interfaces, which uses the Simple Network Time Protocol (SNTP), are compensated to display the local time.

With `Flexible`, a local time zone adjustment is defined using the ***LocalTime Offset*** setting. The non-local and non-IEC 61850 interfaces can be set to either the UTC zone or the local time zone. The local interfaces are always set to the local time zone and the Ethernet interface is always set to the UTC zone.

The interfaces where you can select between UTC and Local Time are the serial interfaces RP1, RP2, DNP over Ethernet (if applicable) and Tunnelled Courier (if applicable). This is achieved by means of the following settings, each of which can be set to UTC or Local.:

- RP1 Time Zone
- RP2 Time Zone
- DNPOE Time Zone
- Tunnel Time Zone

The ***LocalTime Offset*** setting allows you to enter the local time zone compensation from -12 to + 12 hours at 15 minute intervals.

4.2 DAYLIGHT SAVING TIME COMPENSATION

It is possible to compensate for Daylight Saving time using the following settings

- DST Enable
- DST Offset
- DST Start
- DST Start Day
- DST Start Month
- DST Start Mins
- DST End
- DST End Day
- DST End Month
- DST End Mins

These settings are described in the *DATE AND TIME* settings table in the configuration chapter.

5 SETTINGS GROUP SELECTION

You can select the setting group using opto inputs, a menu selection, and for some models the hotkey menu or function keys. You choose which method using the Setting Group setting in the *CONFIGURATION* column. There are two possibilities; Select via Menu, or Select via PSL. If you choose ***Select via Menu***, you set the settings group using the ***Active Settings*** setting or with the hotkeys. If you choose ***Select via PSL*** , you set the settings group with DDB signals according to the following table:

SG Select 1X	SG Select X1	Selected Setting Group
0	0	1
0	1	2
1	0	3
1	1	4

Each setting group has its own PSL. Once a PSL configuration has been designed it can be allocated to any one of the 4 setting groups. When downloading or extracting a PSL configuration, you will be prompted to enter the required setting group to which it will allocated.

CHAPTER 6

CURRENT PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

The P14D provides a wide range of current protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

2 OVERCURRENT PROTECTION PRINCIPLES

Most electrical power system faults result in an overcurrent of one kind or another. It is the job of protection devices, formerly known as 'relays' but now known as Intelligent Electronic Devices (IEDs) to protect the power system from faults. The general principle is to isolate the faults as quickly as possible to limit the danger and prevent fault currents flowing through systems, which can cause severe damage to equipment and systems. At the same time, we wish to switch off only the parts of the power grid that are absolutely necessary, to prevent unnecessary blackouts. The protection devices that control the tripping of the power grid's circuit breakers are highly sophisticated electronic units, providing an array of functionality to cover the different fault scenarios for a multitude of applications.

The described products offer a range of overcurrent protection functions including:

- Phase Overcurrent protection
- Earth Fault Overcurrent protection
- Negative Sequence Overcurrent protection
- Sensitive Earth Fault protection

To ensure that only the necessary circuit breakers are tripped and that these are tripped with the smallest possible delay, the IEDs in the protection scheme need to co-ordinate with each other. Various methods are available to achieve correct co-ordination between IEDs in a system. These are:

- By means of time alone
- By means of current alone
- By means of a combination of both time and current.

Grading by means of current alone is only possible where there is an appreciable difference in fault level between the two locations where the devices are situated. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest.

For these reasons the most commonly applied characteristic in co-ordinating overcurrent devices is the IDMT (Inverse Definite Minimum Time) type.

2.1 IDMT CHARACTERISTICS

There are two basic requirements to consider when designing protection schemes:

- All faults should be cleared as quickly as possible to minimise damage to equipment
- Fault clearance should result in minimum disruption to the electrical power grid.

The second requirement means that the protection scheme should be designed such that only the circuit breaker(s) in the protection zone where the fault occurs, should trip.

These two criteria are actually in conflict with one another, because to satisfy (1), we increase the risk of shutting off healthy parts of the grid, and to satisfy (2) we purposely introduce time delays, which increase the amount of time a fault current will flow. With IDMT protection applied to radial feeders, this problem is exacerbated by the nature of faults in that the protection devices nearest the source, where the fault currents are largest, actually need the longest time delay.

IDMT characteristics are described by operating curves. Traditionally, these were defined by the performance of electromechanical relays. In numerical protection, equations are used to replicate these characteristics so that they can be used to grade with older equipment.

The old electromechanical relays countered this problem somewhat due to their natural operate time v. fault current characteristic, whereby the higher the fault current, the quicker the operate time. The characteristic typical of these electromechanical relays is called Inverse Definite Minimum Time or IDMT for short.

2.1.1 IEC 60255 IDMT CURVES

There are four well-known variants of this characteristic:

- Standard Inverse
- Very inverse
- Extremely inverse
- UK Long Time inverse

These equations and corresponding curves governing these characteristics are very well known in the power industry.

Standard Inverse

This characteristic is commonly known as the 3/10 characteristic, i.e. at ten times setting current and TMS of 1 the relay will operate in 3 seconds.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{0.14}{\left(\frac{I}{I_s}\right)^{0.02} - 1}$$

The standard inverse time characteristic is widely applied at all system voltages – as back up protection on EHV systems and as the main protection on HV and MV distribution systems.

In general, the standard inverse characteristics are used when:

- There are no co-ordination requirements with other types of protective equipment further out on the system, e.g. Fuses, thermal characteristics of transformers, motors etc.
- The fault levels at the near and far ends of the system do not vary significantly.
- There is minimal inrush on cold load pick up. Cold load inrush is that current which occurs when a feeder is energised after a prolonged outage. In general the relay cannot be set above this value but the current should decrease below the relay setting before the relay operates.

Very Inverse

This type of characteristic is normally used to obtain greater time selectivity when the limiting overall time factor is very low, and the fault current at any point does not vary too widely with system conditions. It is particularly suitable, if there is a substantial reduction of fault current as the distance from the power source increases. The steeper inverse curve gives longer time grading intervals. Its operating time is approximately doubled for a reduction in setting from 7 to 4 times the relay current setting. This permits the same time multiplier setting for several relays in series.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{13.5}{\left(\frac{I}{I_s}\right) - 1}$$

Extremely Inverse

With this characteristic the operating time is approximately inversely proportional to the square of the current. The long operating time of the relay at peak values of load current make the relay particularly suitable for grading with fuses and also for protection of feeders which are subject to peak currents on switching in, such as feeders supplying refrigerators, pumps, water heaters etc., which remain connected even after a prolonged interruption of supply.

For cases where the generation is practically constant and discrimination with low tripping times is difficult to obtain, because of the low impedance per line section, an extremely inverse relay can be very useful since only a small difference of current is necessary to obtain an adequate time difference.

Another application for this relay is with auto reclosers in low voltage distribution circuits. As the majority of faults are of a transient nature, the relay is set to operate before the normal operating time of the fuse, thus preventing perhaps unnecessary blowing of the fuse.

Upon reclosure, if the fault persists, the recloser locks itself in the closed position and allows the fuse to blow to clear the fault.

This characteristic is also widely used for protecting plant against overheating since overheating is usually an I2t function.

This characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{80}{\left(\frac{I}{I_s}\right)^2 - 1}$$

UK Long Time Inverse

This type of characteristic has a long time characteristic and may be used for protection of neutral earthing resistors (which normally have a 30 second rating). The relay operating time at 5 times current setting is 30 seconds at a TMS of 1.

This can be defined by:

$$t_{op} = T \frac{120}{\left(\frac{I}{I_s}\right) - 1}$$

In the above equations:

- t_{op} is the operating time
- T is the time multiplier setting
- I is the measured current
- I_s is the current threshold setting.

The ratio I/I_s is sometimes defined as 'M' or 'PSM' (Plug Setting Multiplier).

These curves are plotted as follows:

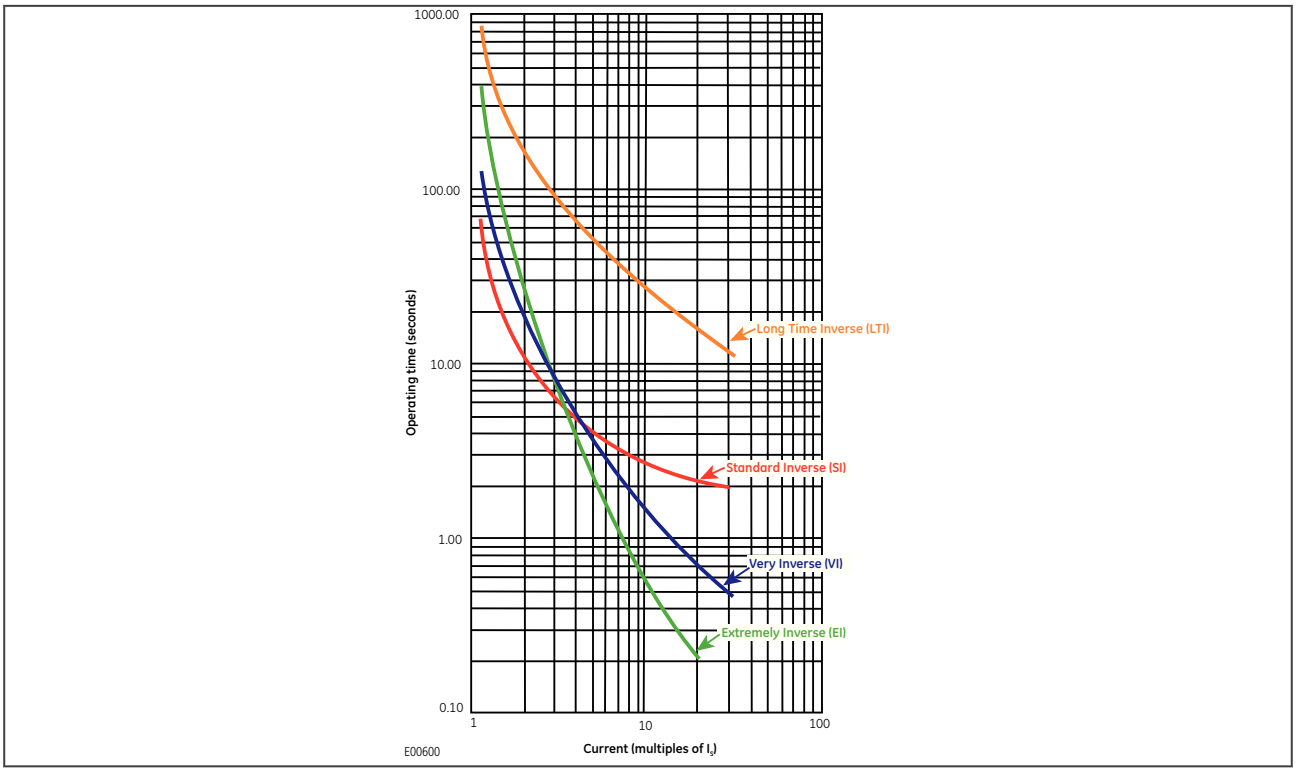


Figure 17: IEC 60255 IDMT curves

2.1.2 EUROPEAN STANDARDS

The IEC 60255 IDMT Operate equation is:

$$t_{op} = T\left(\frac{\beta}{M^{\alpha}-1}+L\right)+C$$

and the IEC 60255 IDMT Reset equation is:

$$t_r = T\left(\frac{\beta}{1-M^{\alpha}}\right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- T is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/Is)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEC IDMT curves are as follows:

Curve Description	β constant	α constant	L constant
IEC Standard Inverse Operate	0.14	0.02	0
IEC Standard Inverse Reset	8.2	6.45	0

Curve Description	β constant	α constant	L constant
IEC Very Inverse Operate	13.5	1	0
IEC Very Inverse Reset	50.92	2.4	0
IEC Extremely Inverse Operate	80	2	0
IEC Extremely Inverse Reset	44.1	3.03	0
UK Long Time Inverse Operate*	120	1	0
UK Rectifier Operate*	45900	5.6	0

Rapid Inverse (RI) characteristic

The RI operate curve is represented by the following equation:

$$t_{op} = K\left(\frac{1}{0.339 - \frac{0.236}{M}}\right)$$

where:

- t_{op} is the operating time
- K is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/I_S)

Note:
** When using UK Long Time Inverse, UK Rectifier or RI for the Operate characteristic, DT (Definite Time) is always used for the Reset characteristic.*

2.1.3 NORTH AMERICAN STANDARDS

The IEEE IDMT Operate equation is:

$$t_{op} = TD\left(\frac{\beta}{M^{\alpha} - 1} + L\right) + C$$

and the IEEE IDMT Reset equation is:

$$t_r = TD\left(\frac{\beta}{1 - M^{\alpha}}\right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- TD is the Time Dial setting
- M is the ratio of the measured current divided by the threshold current (I/I_S)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEEE curves are as follows:

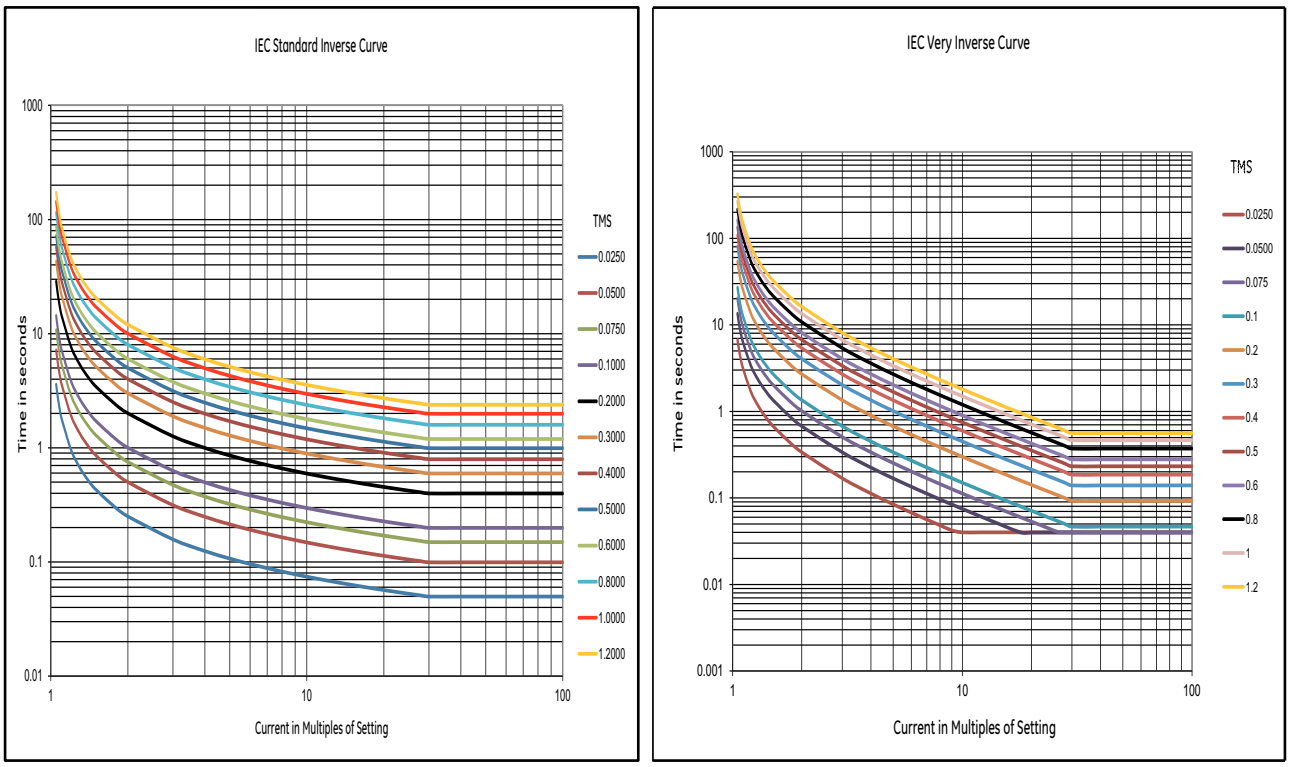
Curve Description	β constant	α constant	L constant
IEEE Moderately Inverse Operate	0.0515	0.02	0.114
IEEE Moderately Inverse Reset	4.85	2	0
IEEE Very Inverse Operate	19.61	2	0.491
IEEE Very Inverse Reset	21.6	2	0
IEEE Extremely Inverse Operate	28.2	2	0.1217
IEEE Extremely Inverse Reset	29.1	2	0
CO8 US Inverse Operate	5.95	2	0.18
CO8 US Inverse Reset	5.95	2	0
CO2 US Short Time Inverse Operate	0.16758	0.02	0.11858
CO2 US Short Time Inverse Reset	2.261	2	0

The constant values for the ANSI curves are as follows:

Curve Description	β constant	α constant	L constant
ANSI Normally Inverse Operate	8.9341	2.0938	0.17966
ANSI Normally Inverse Reset	9	2	0
ANSI Short Time Inverse Operate	0.03393	1.2969	0.2663
ANSI Short Time Inverse Reset	0.5	2	0
ANSI Long Time Inverse Operate	2.18592	1	5.6143
ANSI Long Time Inverse Reset	15.75	2	0

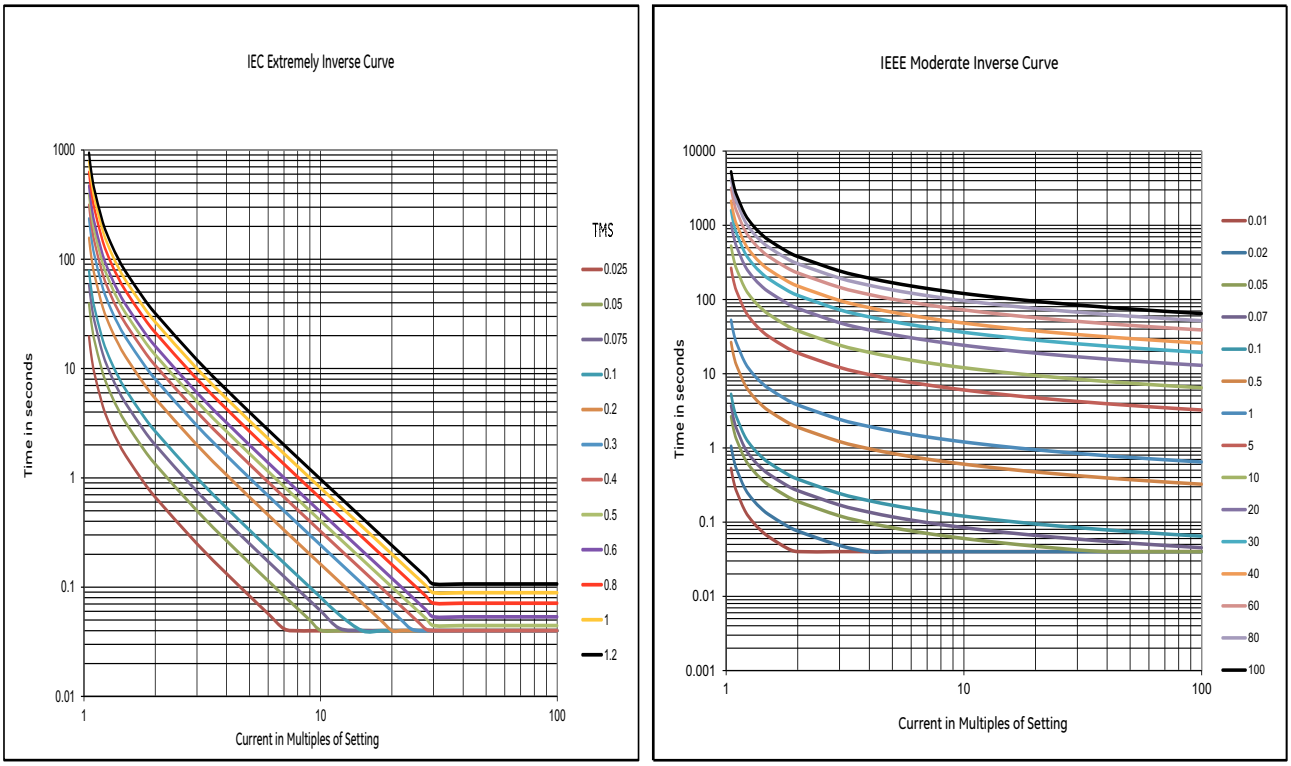
Note:
** When using UK Long Time Inverse or UK Rectifier for the Operate characteristic, DT is always used for the Reset characteristic.*

2.1.4 IEC AND IEEE INVERSE CURVES



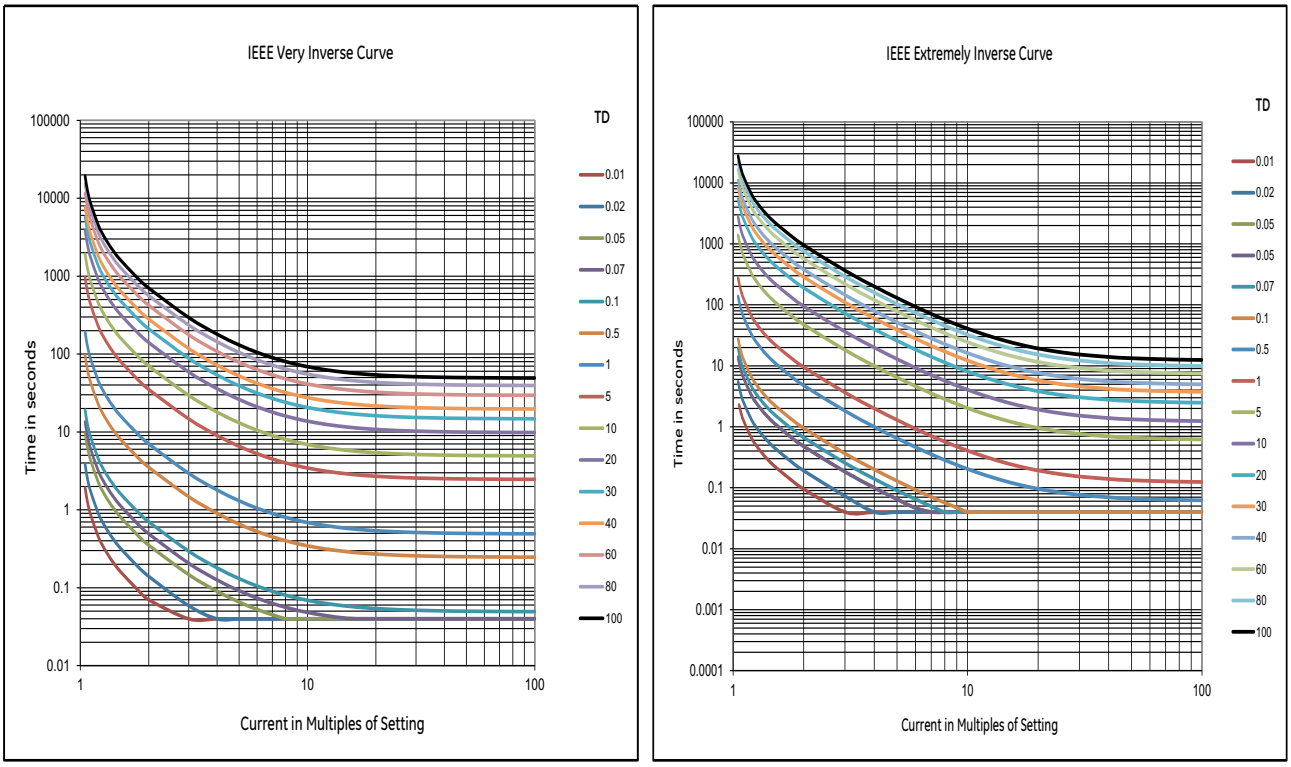
E00757

Figure 18: IEC standard and very inverse curves



E00758

Figure 19: IEC Extremely inverse and IEEE moderate inverse curves



E00759

Figure 20: IEEE very and extremely inverse curves

2.1.5 DIFFERENCES BETWEEN THE NORTH AMERICAN AND EUROPEAN STANDARDS

The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is used for the IEEE/US curves. The menu is arranged such that if an IEC/UK curve is selected, the ***I> Time Dial*** cell is not visible and vice versa for the TMS setting. For both IEC and IEEE/US type curves, a definite time adder setting is available, which will increase the operating time of the curves by the set value.

2.1.6 PROGRAMMABLE CURVES

As well as the standard curves as defined by various countries and standardising bodies, it is possible to program custom curves using the User Programmable Curve Tool, described in the Settings Application Software chapter. This is a user-friendly tool by which you can create curves either by formula or by entering data points. Programmable curves help you to match more closely the withstand characteristics of the electrical equipment than standard curves.

2.2 PRINCIPLES OF IMPLEMENTATION

The range of protection products provides a very wide range of protection functionality. Despite the diverse range of functionality provided, there is some commonality between the way many of the protection functions are implemented. It is important to describe some of these basic principles before going deeper into the individual protection functions.

A simple representation of protection functionality is shown in the following diagram:

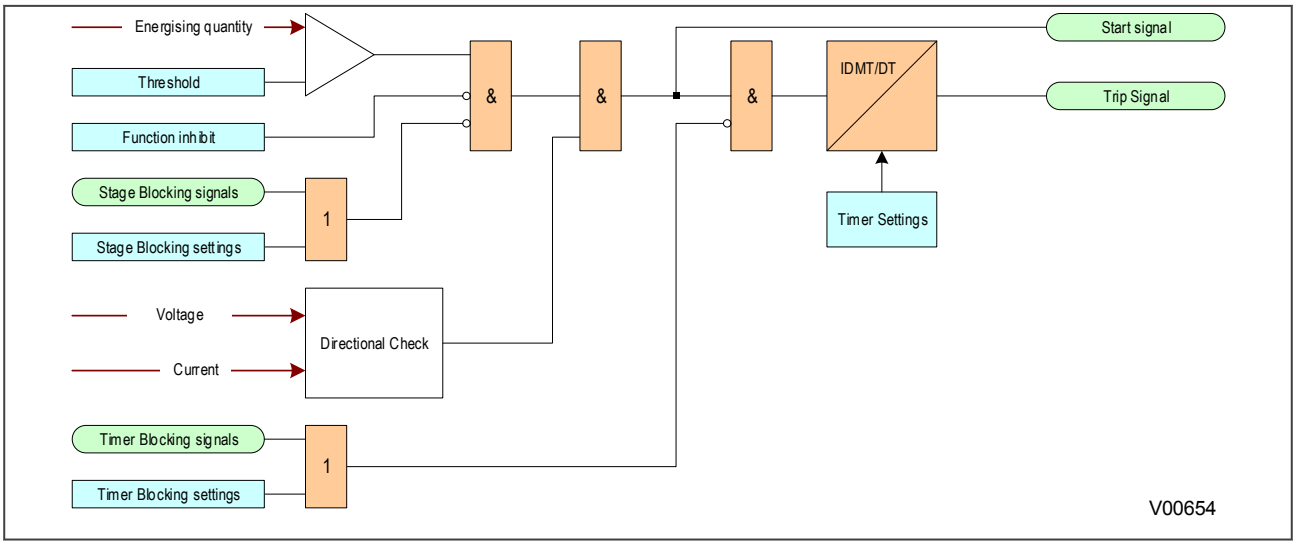


Figure 21: Principle of protection function implementation

An energising quantity is either a voltage input from a system voltage transformer, a current input from a system current transformer or another quantity derived from one or both of these. The energising quantities are extracted from the power system. The signals are converted to digital quantities where they can be processed by the IEDs internal processor.

In general, an energising quantity, be it a current, voltage, power, frequency, or phase quantity, is compared with a threshold value, which may be settable, or hard-coded depending on the function. If the quantity exceeds (for overvalues) or falls short of (for undervalues) the threshold, a signal is produced, which when gated with the various inhibit and blocking functions becomes the Start signal for that protection function. This Start signal is generally made available to Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL) for further processing. It is also passed through a timer function to produce the Trip signal. The timer function may be an IDMT curve, or a Definite Time delay, depending on the function. This timer may also be blocked with timer blocking signals and settings. The timer can be configured by a range of settings to define such parameters as the type of curve, The Time Multiplier Setting, the IDMT constants, the Definite Time delay etc.

In General Electric products, there are usually several independent stages for each of the functions, and for three-phase functions, there are usually independent stages for each of the three phases.

Typically some stages use an Inverse Definite Minumum time (IDMT) timer function, and others use a Definite Time timer (DT) function. If the DT time delay is set to '0', then the function is known to be "instantaneous". In many instances, the term 'instantaneous protection" is used loosely to describe Definite Time protection stages, even when the stage may not theoretically be instantaneous.

Many protection functions require a direction-dependent decision. Such functions can only be implemented where both current and voltage inputs are available. For such functions, a directional check is required, whose output can block the Start signal should the direction of the fault be wrong.

Note:
In the logic diagrams and descriptive text, it is usually sufficient to show only the first stage, as the design principles for subsequent stages are usually the same (or at least very similar). Where there are differences between the functionality of different stages, this is clearly indicated.

2.2.1 TIMER HOLD FACILITY

The Timer Hold facility is available for stages with IDMT functionality , and is controlled by the timer reset settings for the relevant stages (e.g. ***I>1 tReset***, ***I>2 tReset***). These cells are not visible for the IEEE/US curves if an inverse time reset characteristic has been selected, because in this case the reset time is determined by the time dial setting (TDS).

This feature may be useful in certain applications, such as when grading with upstream electromechanical overcurrent relays, which have inherent reset time delays. If you set the hold timer to a value other than zero, the resetting of the protection element timers will be delayed for this period. This allows the element to behave in a similar way to an electromechanical relay. If you set the hold timer to zero, the overcurrent timer for that stage will reset instantaneously as soon as the current falls below a specified percentage of the current setting (typically 95%).

Another situation where the timer hold facility may be used to reduce fault clearance times is for intermittent faults. An example of this may occur in a plastic insulated cable. In this application it is possible that the fault energy melts and reseals the cable insulation, thereby extinguishing the fault. This process repeats to give a succession of fault current pulses, each of increasing duration with reducing intervals between the pulses, until the fault becomes permanent.

When the reset time is instantaneous, the device will repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the device will integrate the fault current pulses, thereby reducing fault clearance time.

3 PHASE OVERCURRENT PROTECTION

Phase current faults are faults where fault current flows between two or more phases of a power system. The fault current may be between the phase conductors only or, between two or more phase conductors and earth.

Although not as common as earth faults (single phase to earth), phase faults are typically more severe.

3.1 PHASE OVERCURRENT PROTECTION IMPLEMENTATION

Phase Overcurrent Protection is configured in the *OVERCURRENT* column of the relevant settings group.

The product provides six stages of segregated three-phase overcurrent protection, each with independent time delay characteristics. The settings are independent for each stage, but for each stage, the settings apply to all phases.

Stages 1, 2 and 5 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves based on IEC and IEEE standards
- A range of programmable user-defined curves
- DT (Definite Time) characteristic

For stage 1, this is achieved using the following settings:

- ***I>1 Function*** for the overcurrent operate characteristic
- ***I>1 Reset Char*** for the overcurrent reset characteristic
- ***I>1 Usr Rst Char*** for the reset characteristic for user-defined curves

The setting names for other stages follow the same principles.

The IDMT-equipped stages, (1,2 and 5) also provide a Timer Hold facility. Stage 1 for example, is configured using the cells ***I>1 tReset***. This setting does not apply to IEEE curves.

Stages 3, 4 and 6 have definite time characteristics only.

3.2 NON-DIRECTIONAL OVERCURRENT LOGIC

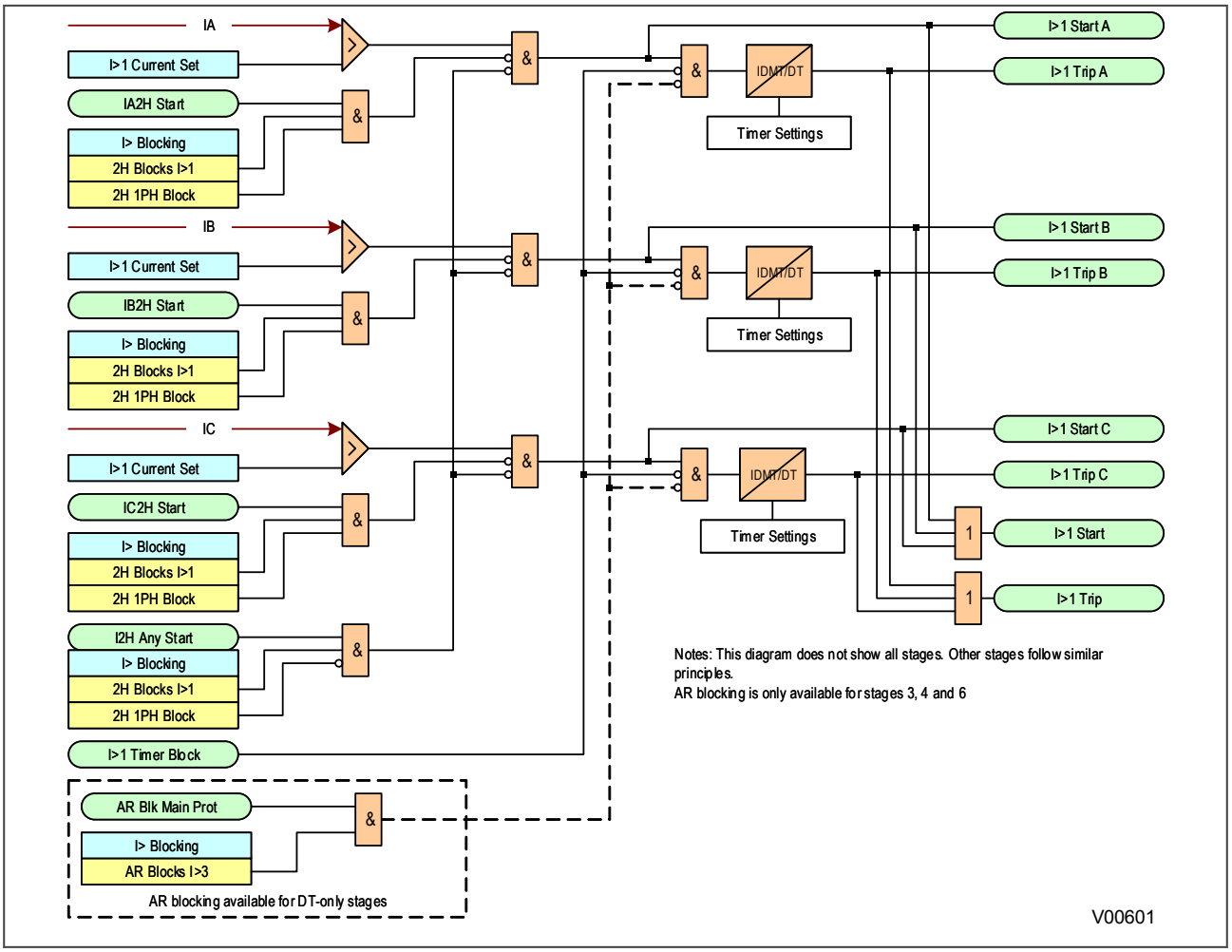


Figure 22: Non-directional Overcurrent Logic diagram

Phase Overcurrent Modules are level detectors that detect when the current magnitude exceeds a set threshold. When this happens, a Start signal is generated unless it is inhibited by a blocking signal. This Start signal initiates the timer module, which can be configured as an IDMT timer or DT timer, depending on the stage number. The Start signal is also available for use in the PSL. For each stage, there are three Phase Overcurrent Modules, one for each phase. The three Start signals from each of these phases are combined to form a 3-phase Start signal.

The Start signals can be blocked by the Second Harmonic blocking function; on a per phase basis (single-phase blocking) or for all three phases at once (three-phase blocking). The relevant bits are set in the ***I> Blocking*** cell and this is combined with the relevant second harmonic blocking DDBs.

The timer can be configured with several settings depening on which type of timer is selected. Taking stage 1 as an example:

The setting ***I>1 Time Delay*** sets the DT time delay

The setting ***I>1 TMS*** sets the Time Multiplier setting for IEC IDMT curves

The setting ***I>1 Time Dial*** sets the Time Multiplier setting for IEEE/US IDMT curves

The setting ***I>1 DT Adder*** adds a fixed time delay to the IDMT operate characteristic

The setting ***I>1 tRESET*** determines the reset time for the DT characteristic

The outputs of the timer modules are the single-phase trip signals. These trip signals are combined to form a 3-phase Trip signal.

The timer modules can be blocked by a Phase Overcurrent Timer Block (for example ***I>1 Timer Block***).

For DT-only stages, the DT timer can be blocked by the Autoreclose function. An Autoreclose blocking signal is produced by the DDB signal ***AR Blk Main Prot*** and the relevant settings in the ***I> Blocking*** cell.

3.3 DIRECTIONAL ELEMENT

If fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Once the direction has been determined the device can decide whether to allow tripping or to block tripping. To determine the direction of a phase overcurrent fault, the device must compare the phase angle of the fault current with that of a known reference quantity. The phase angle of this known reference quantity must be independent of the faulted phase. Typically this will be the line voltage between the other two phases.

The phase fault elements of the IEDs are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of protection	Operate current	Polarizing voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Under system fault conditions, the fault current vector lags its nominal phase voltage by an angle depending on the system X/R ratio. The IED must therefore operate with maximum sensitivity for currents lying in this region. This is achieved using the IED characteristic angle (RCA) setting. The RCA is the angle by which the current applied to the IED must be displaced from the voltage applied to the IED to obtain maximum sensitivity.

There are two ways you can change set the characteristic and trip angles. This is controlled by the ***Dir Char Setting*** cell in the SECURITY CONFIG column. This setting provides two options: `Simple` and `Advanced`.

In `Advanced` mode, the characteristic angle can be set independently for each stage. For stage 1, for example, this would be the setting ***I>1 Char Angle***. It is possible to set characteristic angles anywhere in the range – 180° to + 180°.

The opening angle of the forward or reverse trip zone can also be set independently for each stage. This allows you to set a tripping angle of less than 180° for each stage. For stage 1, for example, you do this using the ***I>1 Trip Angle*** setting.

In `Simple` mode, the angle can only be changed globally for all overcurrent stages.

A directional check is performed based on the following criteria:

Directional forward

$$\angle V + RCA - 90° + (180° - tripping\ angle)/2 < \angle I < \angle V + RCA + 90° - (180° - tripping\ angle)/2$$

Directional reverse

$$\angle V + RCA - 90° - (180° - tripping\ angle)/2 > \angle I > \angle V + RCA + 90° + (180° - tripping\ angle)/2$$

This can be best visualised with reference to the following diagram:

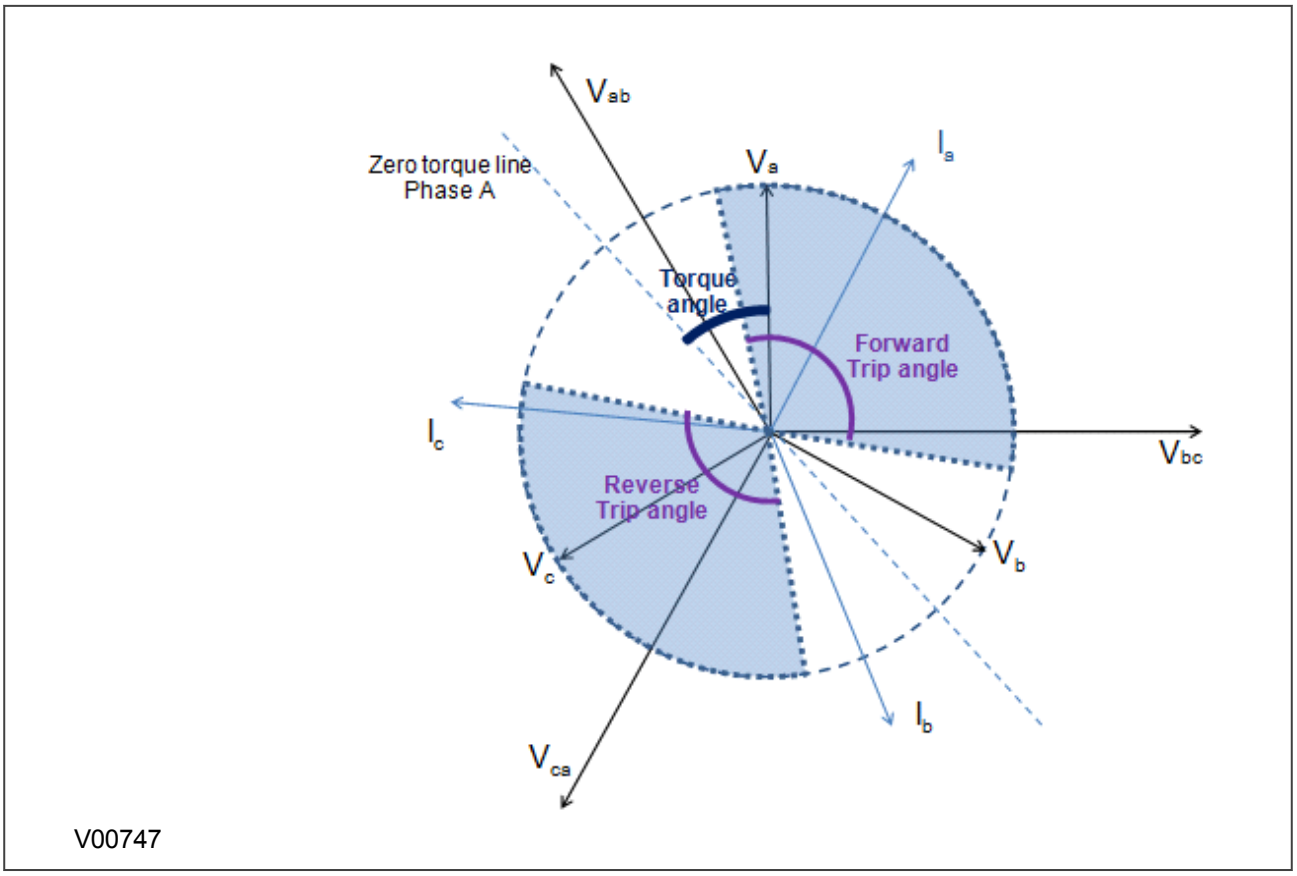


Figure 23: Directional trip angles

For close up three-phase faults, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the device includes a synchronous polarisation feature that stores the pre-fault voltage information and continues to apply this to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

3.3.1 DIRECTIONAL OVERCURRENT LOGIC

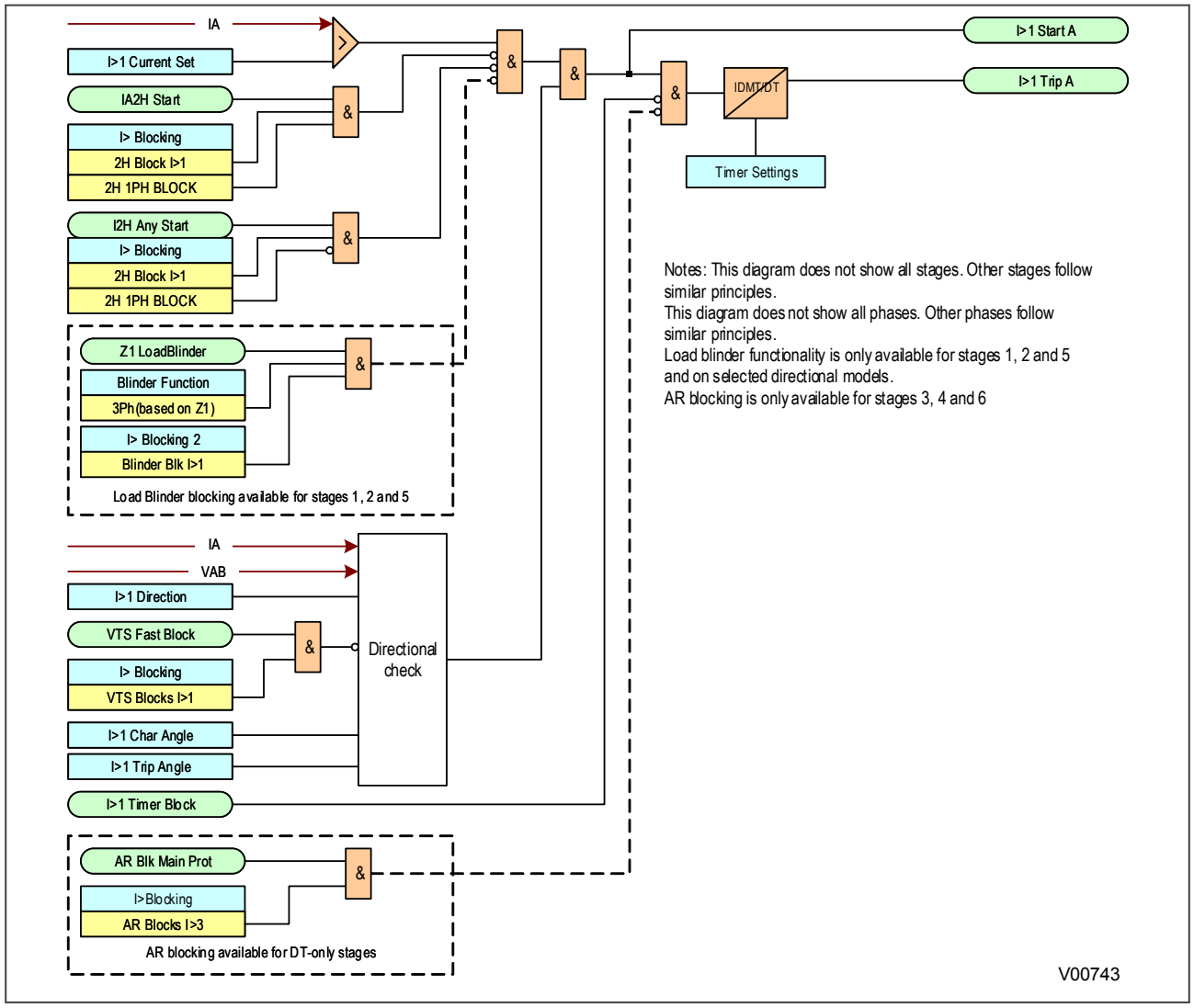


Figure 24: Directional Overcurrent Logic diagram (Phase A shown only)

Voltage Transformer Supervision (VTS) can be used to block operation of directional overcurrent elements.

This is achieved using the ***I> Blocking*** cell. When the relevant bit is set to 1, operation of the VTS will block the stage if directionalised. When set to 0, the stage will revert to non-directional upon operation of the VTS.

3.4 PHASE OVERCURRENT SETTINGS FOR MODEL H

Note:
This section only applies to Model H.

In P14D model H, the following stage 1 overcurrent settings have been modified:

- The maximum time delay setting for stage 1 (***I>1 Time Delay***) has been increased to 8 hours (28800 seconds).
- The maximum time dial setting for stage 1 (***I>1 Time Dial***) has been increased to 8 hours (28800 seconds).
- The maximum definite time adder setting for stage 1 (***I>1 DT Adder***) has been increased to 8 hours (28800 seconds).
- The maximum definite time reset time for stage 1 (***I>1 DT Adder***) has been increased to 8 hours (28800 seconds).

3.5 APPLICATION NOTES

3.5.1 PARALLEL FEEDERS

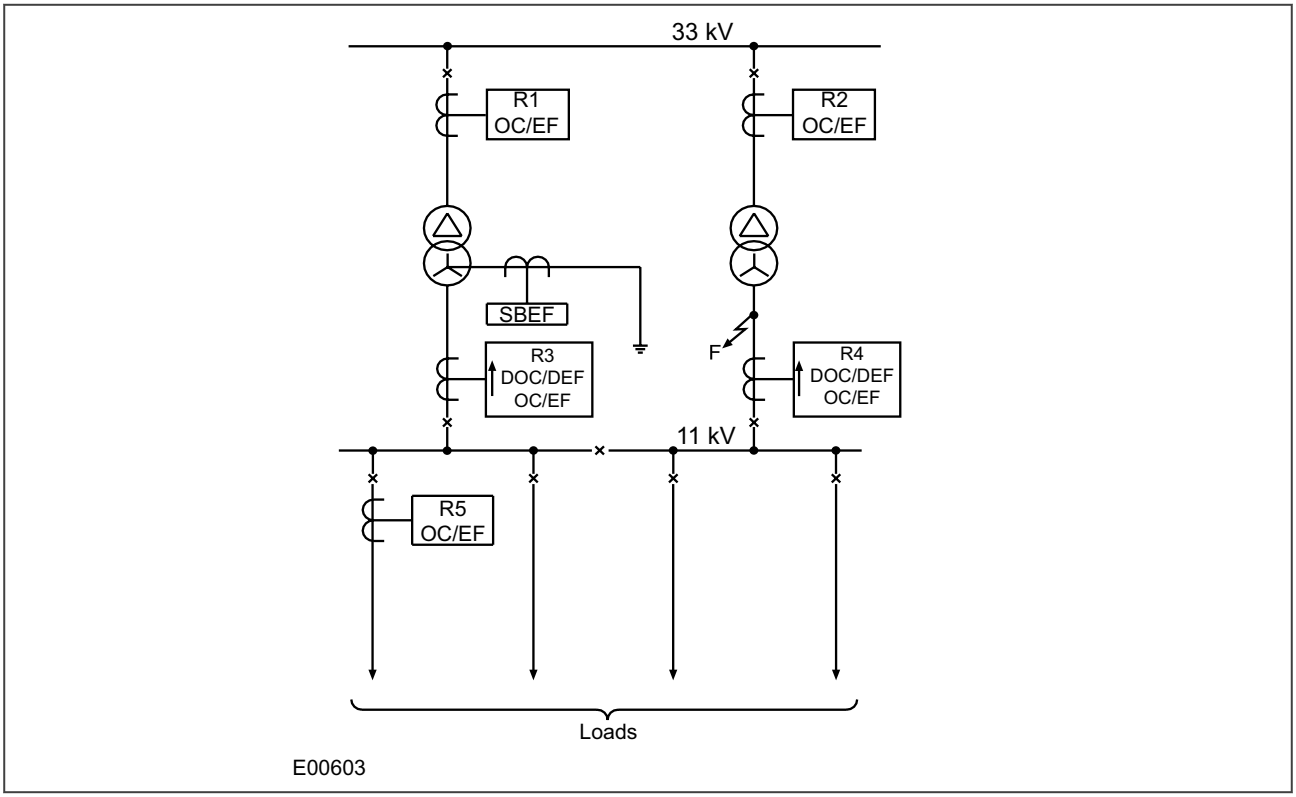


Figure 25: Typical distribution system using parallel transformers

In the application shown in the diagram, a fault at 'F' could result in the operation of both R3 and R4 resulting in the loss of supply to the 11 kV busbar. Hence, with this system configuration, it is necessary to apply directional protection devices at these locations set to 'look into' their respective transformers. These devices should co-ordinate with the non-directional devices, R1 and R2, to ensure discriminative operation during such fault conditions.

In such an application, R3 and R4 may commonly require non-directional overcurrent protection elements to provide protection to the 11 kV busbar, in addition to providing a back-up function to the overcurrent devices on the outgoing feeders (R5).

For this application, stage 1 of the R3 and R4 overcurrent protection would be set to non-directional and time graded with R5, using an appropriate time delay characteristic. Stage 2 could then be set to directional (looking back into the transformer) and also have a characteristic which provides correct co-ordination with R1 and R2. Directionality for each of the applicable overcurrent stages can be set in the directionality cells (***I>1 Direction***).

Note:
The principles outlined for the parallel transformer application are equally applicable for plain feeders that are operating in parallel.

3.5.2 RING MAIN ARRANGEMENTS

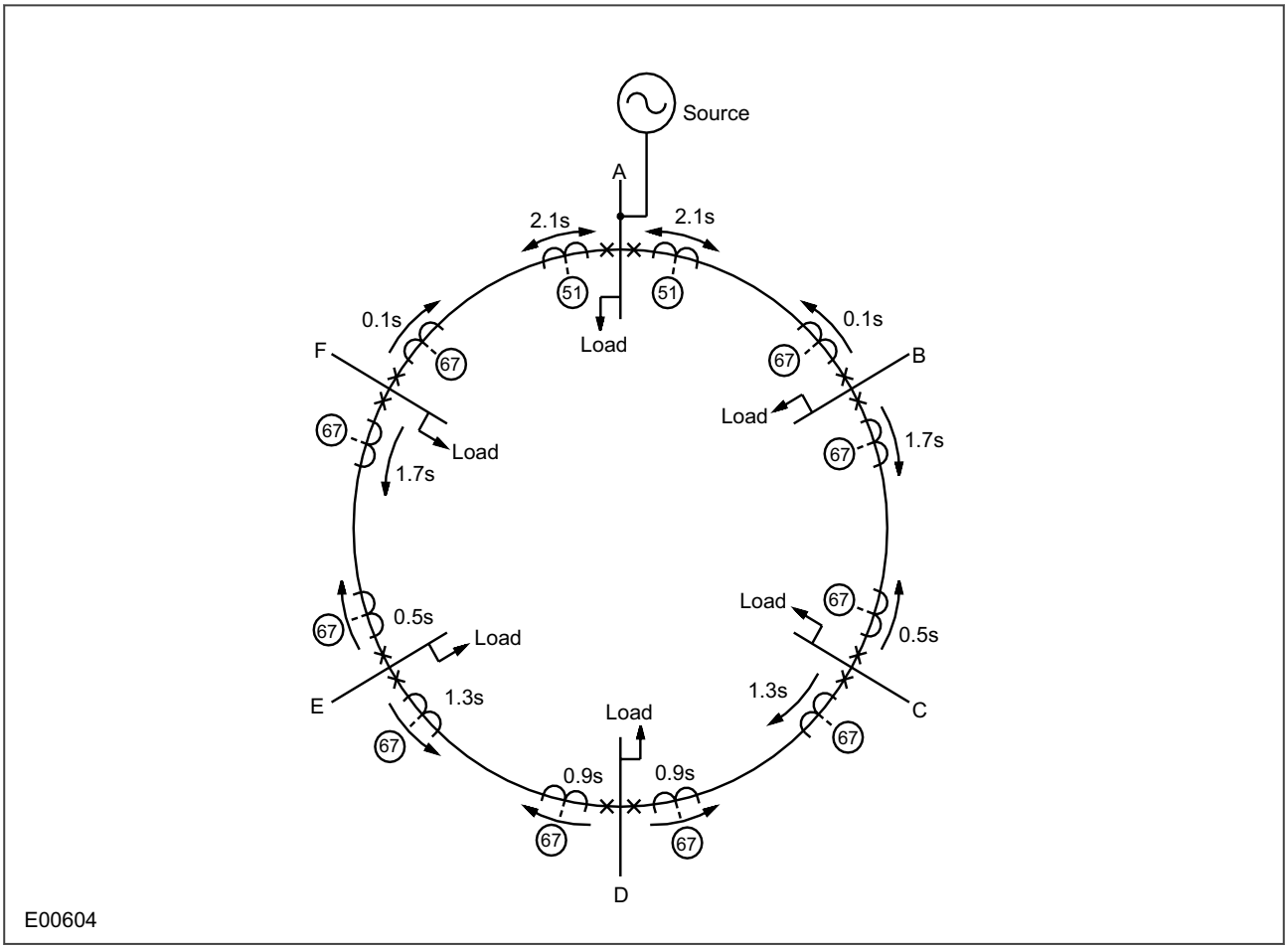


Figure 26: Typical ring main with associated overcurrent protection

In a ring main arrangement, current may flow in either direction through the various device locations, therefore directional overcurrent devices are needed to achieve correct discrimination.

The normal grading procedure for overcurrent devices protecting a ring main circuit is to consider the ring open at the supply point and to grade the devices first clockwise and then anti-clockwise. The arrows shown at the various device locations depict the direction for forward operation of the respective devices (i.e. the directional devices are set to look into the feeder that they are protecting).

The diagram shows typical time settings (assuming definite time co-ordination is used), from which it can be seen that any faults on the interconnections between stations are cleared discriminatively by the devices at each end of the feeder.

Any of the overcurrent stages may be configured to be directional and co-ordinated, but bear in mind that IDMT characteristics are not selectable on all the stages.

3.5.3 SETTING GUIDELINES

Standard principles should be applied in calculating the necessary current and time settings. The example detailed below shows a typical setting calculation and describes how the settings are applied.

This example is for a device feeding a LV switchboard and makes the following assumptions:

- CT Ratio = 500/1
- Full load current of circuit = 450A
- Slowest downstream protection = 100A Fuse

The current setting on the device must account for both the maximum load current and the reset ratio, therefore:

I> must be greater than: 450/drop-off = 450/0.95 = 474A.

The device allows the current settings to be applied in either primary or secondary quantities. This is done by setting the ***Setting Values*** cell of the *CONFIGURATION* column. When this cell is set to primary, all phase overcurrent setting values are scaled by the programmed CT ratio.

In this example, assuming primary currents are to be used, the ratio should be programmed as 500/1.

The required setting is therefore 0.95A in terms of secondary current or 475A in terms of primary.

A suitable time delayed characteristic will now need to be chosen. When co-ordinating with downstream fuses, the applied characteristic should be closely matched to the fuse characteristic. Therefore, assuming IDMT co-ordination is to be used, an Extremely Inverse (EI) characteristic would normally be chosen. This is found under the ***I>1 Function*** cell as `IEC E Inverse`.

Finally, a suitable time multiplier setting (TMS) must be calculated and entered in cell ***I>1 TMS.***

3.5.4 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

The applied current settings for directional overcurrent devices are dependent upon the application in question. In a parallel feeder arrangement, load current is always flowing in the non-operate direction. Hence, the current setting may be less than the full load rating of the circuit.

You need to observe some setting constraints when applying directional overcurrent protection at the receiving-end of parallel feeders. These minimum safe settings are designed to ensure that there is no possibility of undesired tripping during clearance of a source fault. For a linear system load, these settings are as follows:

We recommend the following settings to ensure that there is no possibility of malaoperation:

- Parallel plain feeders: Set to 50% pre-fault load current
- Parallel transformer feeders: Set to 87% pre-fault load current

In a ring main application, the load current can flow in either direction. The current setting must be above the maximum load current.

The required characteristic angle settings for directional devices depend on the application. We recommend the following settings:

- Plain feeders, or applications with an earthing point behind the device location, should use a +30° RCA setting
- Transformer feeders, or applications with a zero sequence source in front of the device location, should use a +45° RCA setting

Although it is possible to set the RCA to exactly match the system fault angle, we recommend that you adhere to the above guidelines, as these settings provide satisfactory performance and stability under a wide range of system conditions.

4 VOLTAGE DEPENDENT OVERCURRENT ELEMENT

An overcurrent protection scheme is co-ordinated throughout a system such that cascaded operation is achieved. This means that if for some reason a downstream circuit breaker fails to trip for a fault condition, the next upstream circuit breaker should trip.

However, where long feeders are protected by overcurrent protection, the detection of remote phase-to-phase faults may prove difficult due to the fact that the current pick-up of phase overcurrent elements must be set above the maximum load current, thereby limiting the minimum sensitivity.

If the current seen by a local device for a remote fault condition is below its overcurrent setting, a voltage dependent element may be used to increase the sensitivity to such faults. As a reduction in system voltage will occur during overcurrent conditions, this may be used to enhance the sensitivity of the overcurrent protection by reducing the pick up level.

Voltage dependent overcurrent devices are often applied in generator protection applications in order to give adequate sensitivity for close up fault conditions. The fault characteristic of this protection must then co-ordinate with any of the downstream overcurrent devices that are responsive to the current decrement condition. It therefore follows that if the device is to be applied to an outgoing feeder from a generator station, the use of voltage dependent overcurrent protection in the feeder device may allow better co-ordination with the Voltage Dependent device on the generator.

4.1 VOLTAGE DEPENDENT OVERCURRENT PROTECTION IMPLEMENTATION

Voltage Dependent Overcurrent Protection (VDep OC) is set in the *OVERCURRENT* column of the relevant settings group, under the sub-heading *V DEPENDANT O/C*.

The function is available for stages 1, 2 and 5 of the main overcurrent element. When VDep OC is enabled, the overcurrent threshold setting is modified when the voltage falls below a set threshold.

If voltage dependant overcurrent operation is selected, the element can be set in one of two modes, voltage controlled overcurrent or voltage restrained overcurrent.

4.1.1 VOLTAGE CONTROLLED OVERCURRENT PROTECTION

In Voltage Controlled Operation (VCO) mode of operation, the under voltage detector is used to produce a step change in the current setting, when the voltage falls below the voltage setting ***V Dep OC V<1 Set***. The operating characteristic of the current setting when voltage controlled mode is selected is as follows:

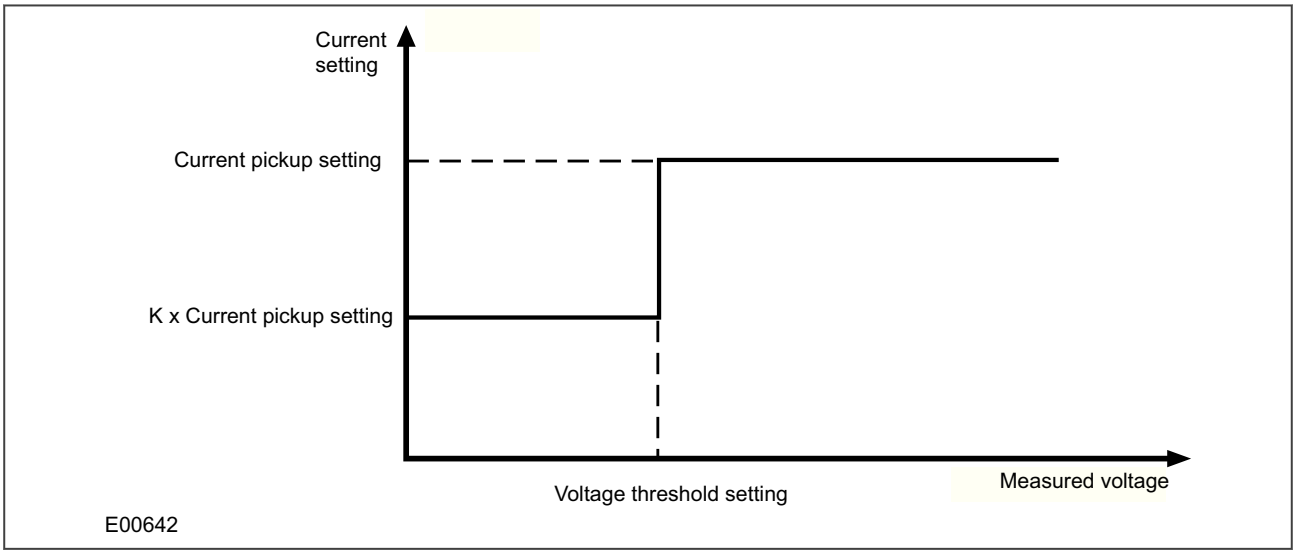


Figure 27: Modification of current pickup level for voltage controlled overcurrent protection

4.1.2 VOLTAGE RESTRAINED OVERCURRENT PROTECTION

In Voltage Restrained Operation (VRO) mode the effective operating current of the protection element is continuously variable as the applied voltage varies between two voltage thresholds. This protection mode is considered to be better suited to applications where the generator is connected to the system via a generator transformer.

With indirect connection of the generator, a solid phase-phase fault on the local busbar will result in only a partial phase-phase voltage collapse at the generator terminals.

The voltage-restrained current setting is related to measured voltage as follows:

- If V is greater than ***V<1***, the current setting (Is) = I>
- If V is greater than ***V<2*** but less than ***V<1***, the current setting (Is) =

$$KI> + (I> - KI)\frac{V - V<2}{V<1 - V<2}$$

- If V is less than ***V<2***, the current setting (Is) = K.I>

where:

- I> = Over current stage setting
- Is = Current setting at voltage V
- V = Voltage applied to relay element
- V<1 = V Dep OC V<1 Set
- V<2 = V Dep OC V<2 Set

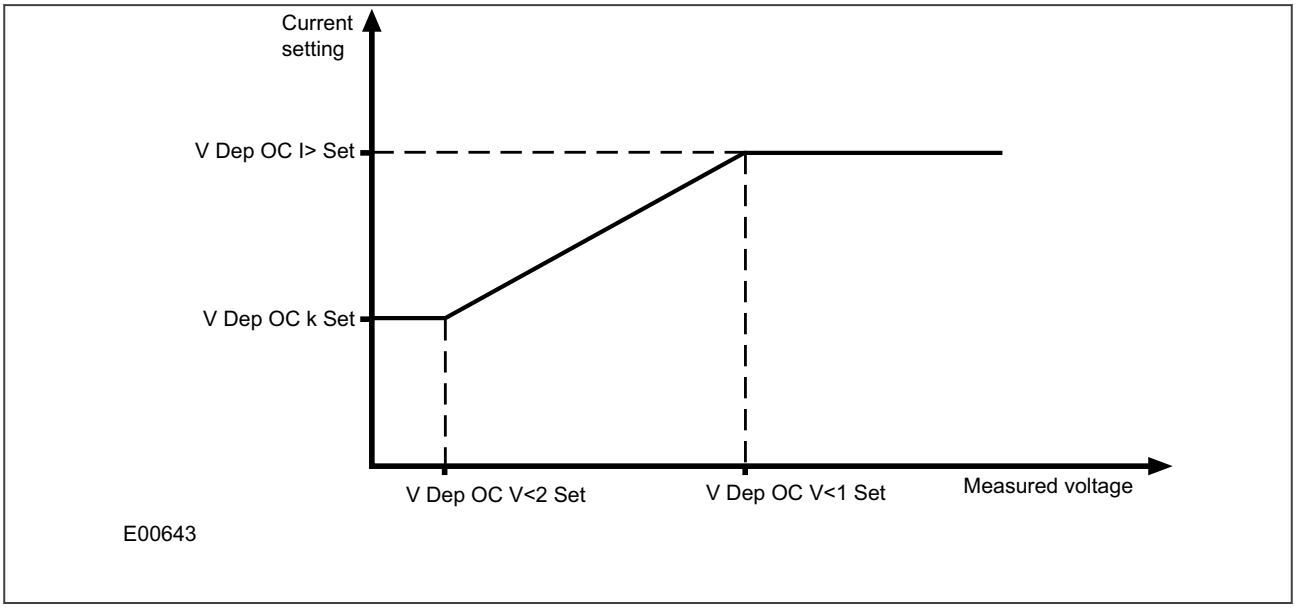


Figure 28: Modification of current pickup level for voltage restrained overcurrent protection

4.2 VOLTAGE DEPENDENT OVERCURRENT LOGIC

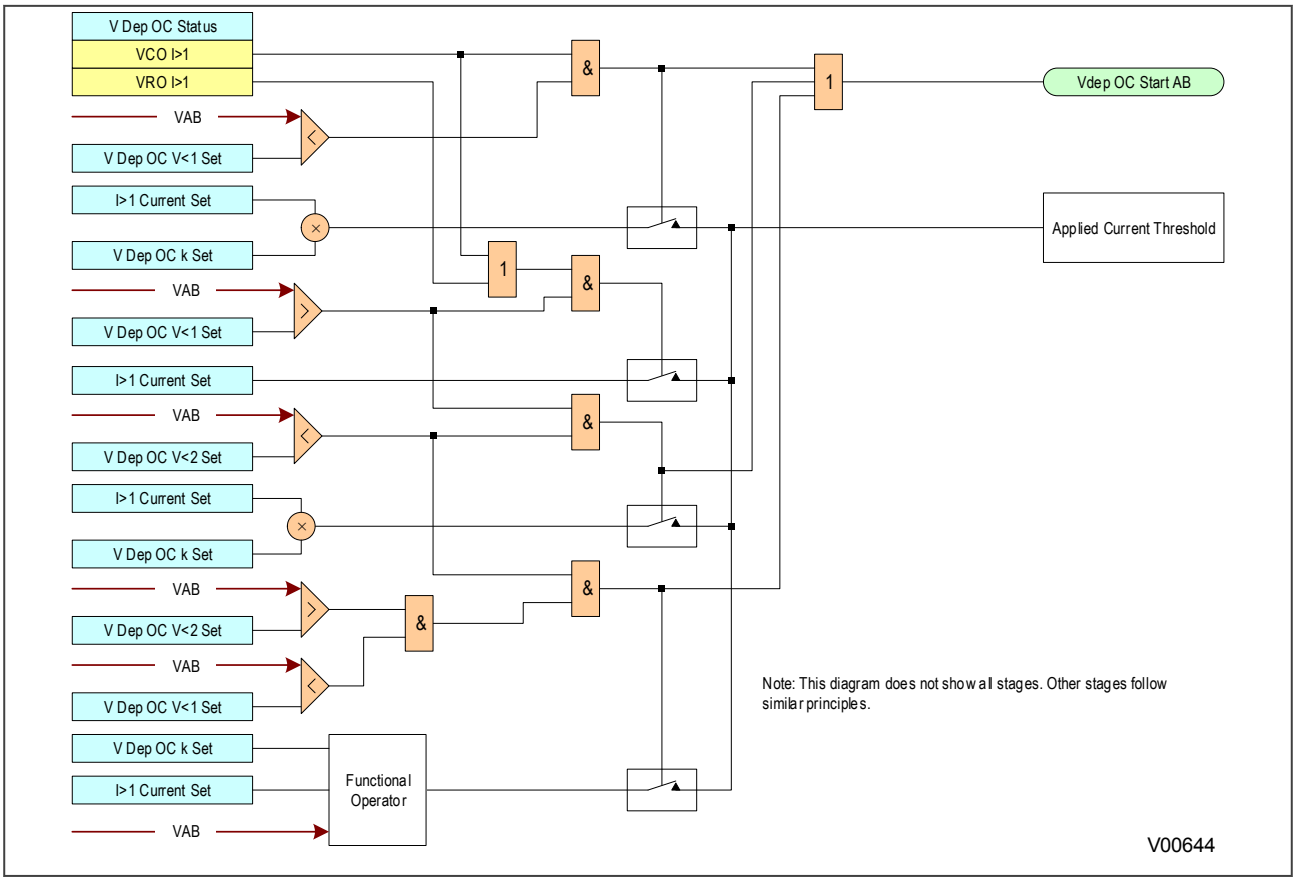


Figure 29: Voltage dependant overcurrent logic (Phase A to phase B)

The current threshold setting for the Overcurrent function is determined by the voltage.

If the voltage is greater than ***V Dep OC V<1 Set***, the normal overcurrent setting ***I>1 current set*** is used. this applies to both VCO and VRO modes.

If the voltage is less than ***V Dep OC V<1 Set*** AND it is in VCO mode, the overcurrent setting ***I>1 current set*** is multiplied by the factor set by ***V Dep OC k set***.

If the voltage is less than ***V Dep OC V<2 Set*** AND it is in VRO mode, the overcurrent setting ***I>1 current set*** is multiplied by the factor set by ***V Dep OC k set.***

If the voltage is between ***V Dep OC V<1 Set*** and ***V Dep OC V<2 Set*** AND it is in VRO mode, the overcurrent setting is multiplied by a functional operator to determine the setting.

4.3 APPLICATION NOTES

4.3.1 SETTING GUIDELINES

The ***V Dep OC k set*** setting should be set low enough to allow operation for remote phase-to-phase faults, typically:

$$k = \frac{I_F}{1.2I>}$$

where:

- I_F = Minimum fault current expected for the remote fault
- I> = Phase current setting for the element to have VCO control

Example

If the overcurrent device has a setting of 160% In, but the minimum fault current for the remote fault condition is only 80% In, then the required k factor is given by:

$$k = \frac{0.8}{1.6 \times 1.2} = 0.42$$

The voltage threshold, ***V Dep OC V<(n) Set*** setting would be set below the lowest system voltage that may occur under normal system operating conditions, whilst ensuring correct detection of the remote fault.

5 CURRENT SETTING THRESHOLD SELECTION

The Phase Overcurrent protection threshold setting can be influenced by the Cold Load Pickup (CLP)and the Voltage Dependent Overcurrent (V DepOC) functions, should this functionality be used.

The Overcurrent function selects the threshold setting according to the following diagram:

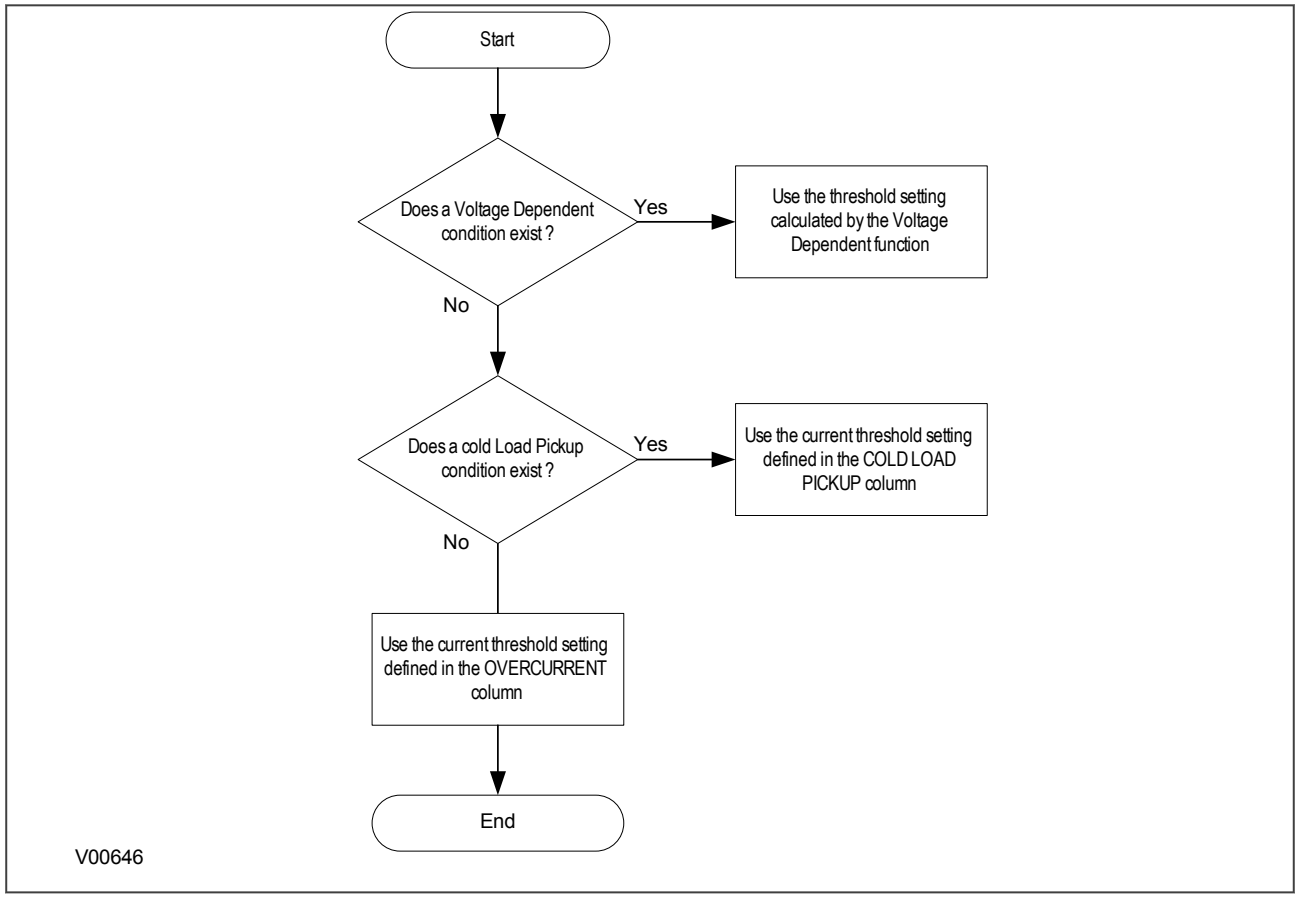


Figure 30: Selecting the current threshold setting

6 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

When applying standard phase overcurrent protection, the overcurrent elements must be set significantly higher than the maximum load current. This limits the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes. Negative Phase Sequence Overcurrent elements can help in such cases.

Any unbalanced fault condition will produce a negative sequence current component. Therefore, a negative phase sequence overcurrent element can be used for both phase-to-phase and phase-to-earth faults. Negative Phase Sequence Overcurrent protection offers the following advantages:

- Negative phase sequence overcurrent elements are more sensitive to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault element due to the system configuration. For example, an earth fault element applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element may be used to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

6.1 NEGATIVE SEQUENCE OVERCURRENT PROTECTION IMPLEMENTATION

Negative Sequence Overcurrent Protection is implemented in the *NEG SEQ O/C* column of the relevant settings group.

The product provides four stages of negative sequence overcurrent protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- A range of User-defined curves
- DT (Definite Time)

For stage 1, this is achieved using the following settings:

- ***I2>1 Function*** for the overcurrent operate characteristic
- ***I2>1 Reset Char*** for the overcurrent reset characteristic
- ***I2>1 Usr RstChar*** for the reset characteristic for user-defined curves

The setting names for other stages follow the same principles.

The IDMT-equipped stages, (1 and 2) also provide a Timer Hold facility. Stage 1, for example, is configured using the cells ***I2>1 tRESET***. This setting is not applicable for curves based on the IEEE standard.

Stages 3 and 4 have definite time characteristics only.

6.2 NON-DIRECTIONAL NEGATIVE SEQUENCE OVERCURRENT LOGIC

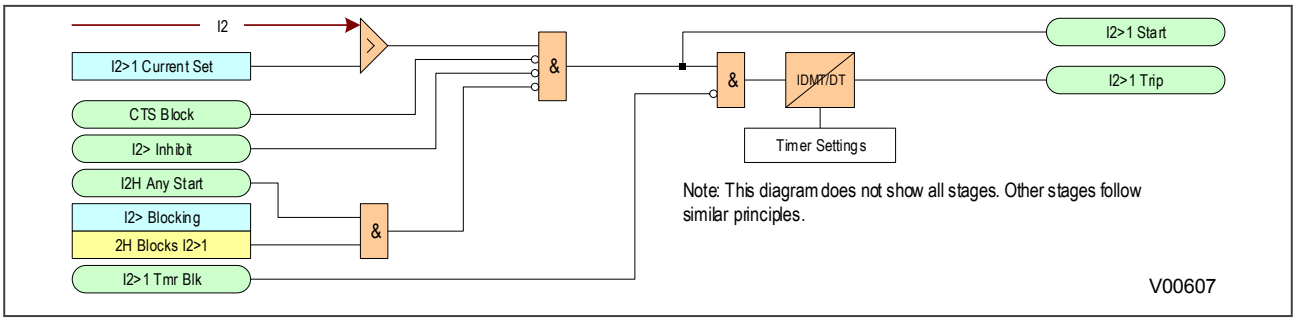


Figure 31: Negative Sequence Overcurrent logic - non-directional operation

For Negative Phase Sequence Overcurrent Protection, the energising quanitity ***I2>*** is compared with the threshold voltage ***I2>1 Current Set***. If the value exceeds this setting a Start signal (***I2>1 Start***) is generated, provided there are no blocks.

The function can be blocked if a CTS or second harmonic condition is detected.

The ***I2>1 Start*** signal is fed into a timer to produce the ***I2>1 trip*** signal. The timer can be blocked by the timer block signal ***I2>1 Tmr Blk***.

This diagram and description applies to each stage.

6.3 DIRECTIONAL ELEMENT

Where negative phase sequence current may flow in either direction, directional control should be used.

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. A directional element is available for all of the negative sequence overcurrent stages. This is found in the ***I2> Direction*** cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

A suitable characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (**–V2**), in order to be at the centre of the directional characteristic.

6.3.1 DIRECTIONAL NEGATIVE SEQUENCE OVERCURRENT LOGIC

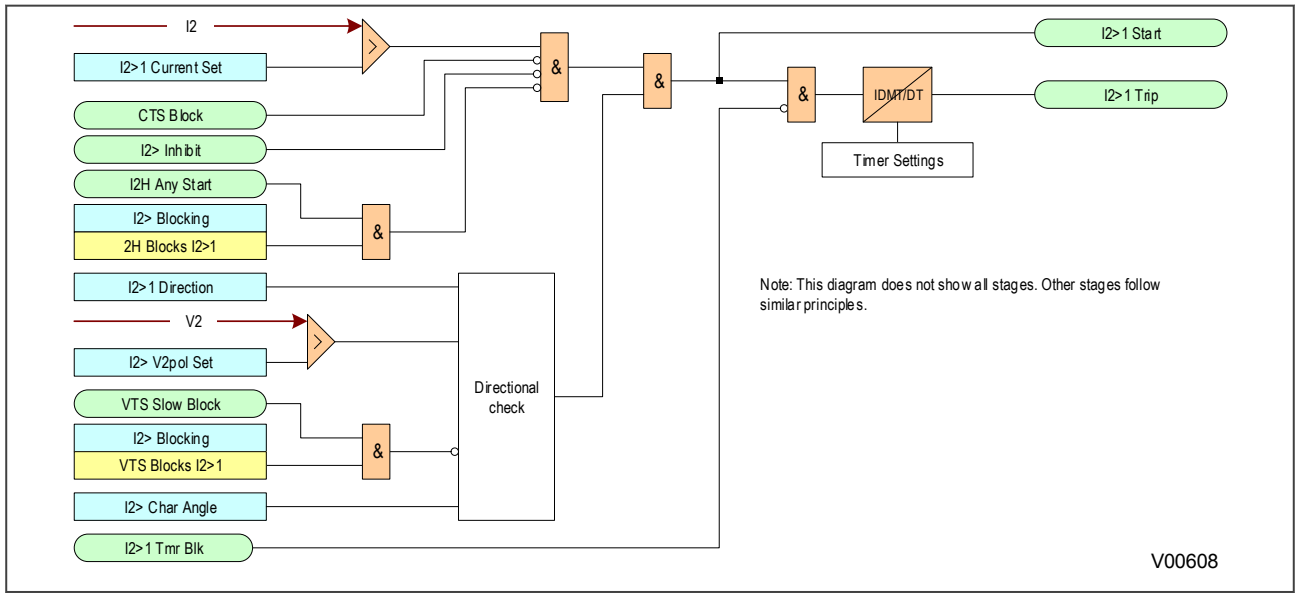


Figure 32: Negative Sequence Overcurrent logic - directional operation

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. The element may be selected to operate in either the forward or reverse direction. A suitable characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2> V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

When the element is selected as directional (directional devices only), a VTS Block option is available. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS) will block the stage. When set to 0, the stage will revert to non-directional.

6.4 APPLICATION NOTES

6.4.1 SETTING GUIDELINES (CURRENT THRESHOLD)

A negative phase sequence element can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-earth or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and earth elements for phase-to-earth and phase-to-phase faults.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load imbalance. This can be set practically at the commissioning stage, making use of the measurement function to display the standing negative phase sequence current. The setting should be at least 20% above this figure.

Where the negative phase sequence element needs to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

6.4.2 SETTING GUIDELINES (TIME DELAY)

Correct setting of the time delay for this function is vital. You should also be very aware that this element is applied primarily to provide back-up protection to other protection devices or to provide an alarm. It would therefore normally have a long time delay.

The time delay set must be greater than the operating time of any other protection device (at minimum fault level) that may respond to unbalanced faults such as phase overcurrent elements and earth fault elements.

6.4.3 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control of the element should be employed (VT models only).

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the relay characteristic angle (RCA) should be set equal to –60°
- For a distribution system the relay characteristic angle (RCA) should be set equal to –45°

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2> V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

7 EARTH FAULT PROTECTION

Earth faults are overcurrent faults where the fault current flows to earth. Earth faults are the most common type of fault.

Earth faults can be measured directly from the system by means of:

- A separate current Transformer (CT) located in a power system earth connection
- A separate Core Balance Current Transformer (CBCT), usually connected to the SEF transformer input
- A residual connection of the three line CTs, where the Earth faults can be derived mathematically by summing the three measured phase currents.

Depending on the device model, it will provide one or more of the above means for Earth fault protection.

7.1 EARTH FAULT PROTECTION ELEMENTS

Earth fault protection is implemented in the columns *EARTH FAULT 1* and *EARTH FAULT 2* of the relevant settings group.

Each column contains an identical set of elements. *EARTH FAULT 1* (EF1) is used for earth fault current that is measured directly from the system (measured). *EARTH FAULT 2* (EF2) uses quantities derived internally from summing the three-phase currents.

The product provides four stages of Earth Fault protection with independent time delay characteristics, for each *EARTH FAULT* column.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- A range of User-defined curves
- DT (Definite Time)

For the EF1 column, this is achieved using the cells:

- ***IN1>(n) Function*** for the overcurrent operate characteristics
- ***IN1>(n) Reset Char*** for the overcurrent reset characteristic
- ***IN1>(n) Usr RstChar*** for the reset characteristic for user-defined curves

For the EF2 column, this is achieved using the cells:

- ***IN2>(n) Function*** for the overcurrent operate characteristics
- ***IN2>(n) Reset Char*** for the overcurrent reset characteristic
- ***IN2>(n) Usr RstChar*** for the reset characteristic for user-defined curves

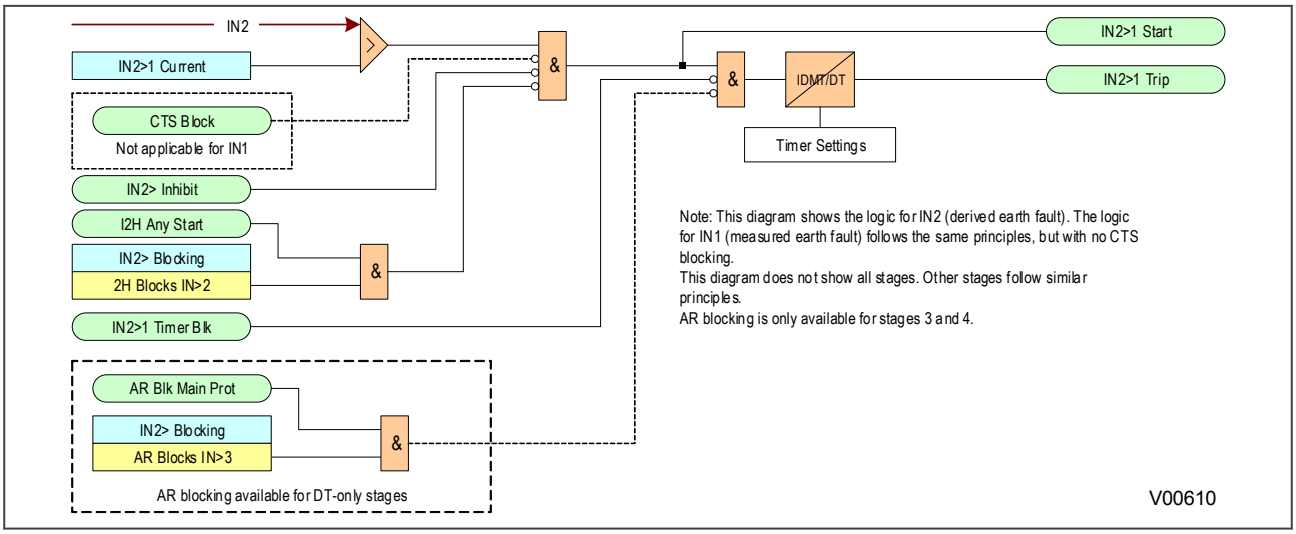
where (n) is the number of the stage.

Stages 1 and 2 provide a Timer Hold facility. This is configured using the cells ***IN1>(n) tReset*** for EF1 and ***IN2>(n) tReset*** for EF2.

Stages 3 and 4 can have definite time characteristics only.

The fact that both EF1 and EF2 elements may be enabled at the same time leads to a number of applications advantages. For example, some applications may require directional earth fault protection for upstream equipment and backup earth fault protection for downstream equipment. This can be achieved with a single IED, rather than two.

7.2 NON-DIRECTIONAL EARTH FAULT LOGIC



Note:
1 If a CLP condition exists, the **I>(n) Current Set threshold is taken from the COLD LOAD PICKUP column*
**2 Autoreclose blocking is only available for stages 3,4 and 6 and on selected models*
**3 The CTS blocking is not applicable for IN1, however this can be achieved using the PSL*

Figure 33: Non-directional EF logic (single stage)

The Earth Fault current is compared with a set threshold (***IN1>(n) Current***) for each stage. If it exceeds this threshold, a Start signal is triggered, providing it is not blocked. This can be blocked by the second harmonic blocking function, or an Inhibit Earth Fault DDB signal.

The autoreclose logic can be set to block the Earth Fault trip after a prescribed number of shots (set in *AUTORECLOSE* column). This is achieved using the ***AR Blk Main Prot*** setting. this can also be blocked by the relevant timer block signal ***IN1>(n)TimerBlk*** DDB signal.

Earth Fault protection can follow the same IDMT characteristics as described in the Overcurrent Protection Principles section. Please refer to that section for details of IDMT characteristics.

The diagram and description also applies to the Earth Fault 2 element (IN2).

7.3 IDG CURVE

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

$$t_{op} = 5.8 - 1.35 log_e \left(\frac{I}{IN > Setting} \right)$$

where:

t_{op} is the operating time

I is the measured current

IN> Setting is an adjustable setting, which defines the start point of the characteristic

Note:
Although the start point of the characteristic is defined by the "IN>" setting, the actual current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

Note:
When using an IDG Operate characteristic, DT is always used with a value of zero for the Rest characteristic.

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

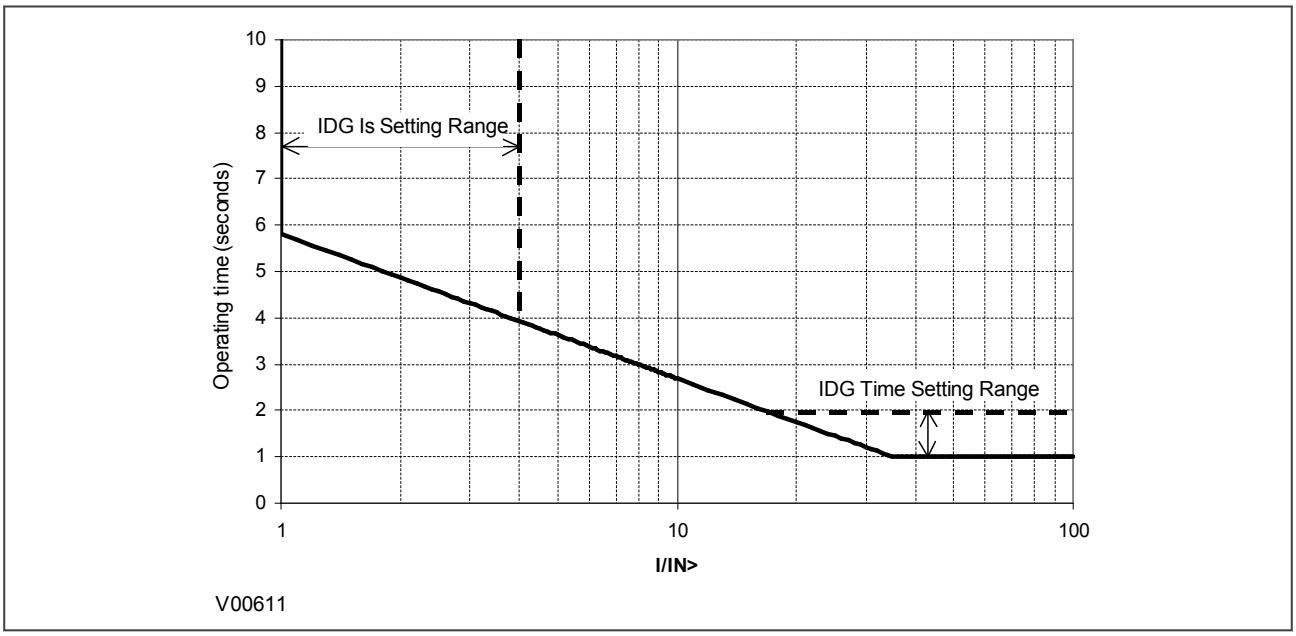


Figure 34: IDG Characteristic

7.4 DIRECTIONAL ELEMENT

If Earth fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Typical systems that require such protection are parallel feeders and ring main systems.

A directional element is available for all of the Earth Fault stages. These are found in the direction setting cells for the relevant stage. They can be set to non-directional, directional forward, or directional reverse.

Directional control can be blocked by the VTS element if required.

For standard earth fault protection, two options are available for polarisation; Residual Voltage (zero sequence) or Negative Sequence.

7.4.1 RESIDUAL VOLTAGE POLARISATION

With earth fault protection, the polarising signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise directional earth fault elements. This is known as Zero Sequence Voltage polarisation, Residual Voltage polarisation or Neutral Displacement Voltage (NVD) polarisation.

Small levels of residual voltage could be present under normal system conditions due to system imbalances, VT inaccuracies, device tolerances etc. For this reason, the device includes a user settable threshold (***IN> VNPol Set***), which must be exceeded in order for the DEF function to become operational. The residual voltage measurement provided in the *MEASUREMENTS 1* column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note:
Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the "-Vres" quantity. This 180° phase shift is automatically introduced within the device.

The directional criteria with residual voltage polarisation is given below:

Directional forward

$$(\angle VN + 180°) + RCA - 90° + (180° - \text{tripping angle})/2 < \angle IN < (\angle VN + 180°) + RCA + 90° - (180° - \text{tripping angle})/2$$

Directional reverse

$$(\angle VN + 180°) + RCA - 90° - (180° - \text{tripping angle})/2 > \angle IN > (\angle VN + 180°) + RCA + 90° + (180° - \text{tripping angle})/2$$

This can be best visualised with reference to the following diagram:

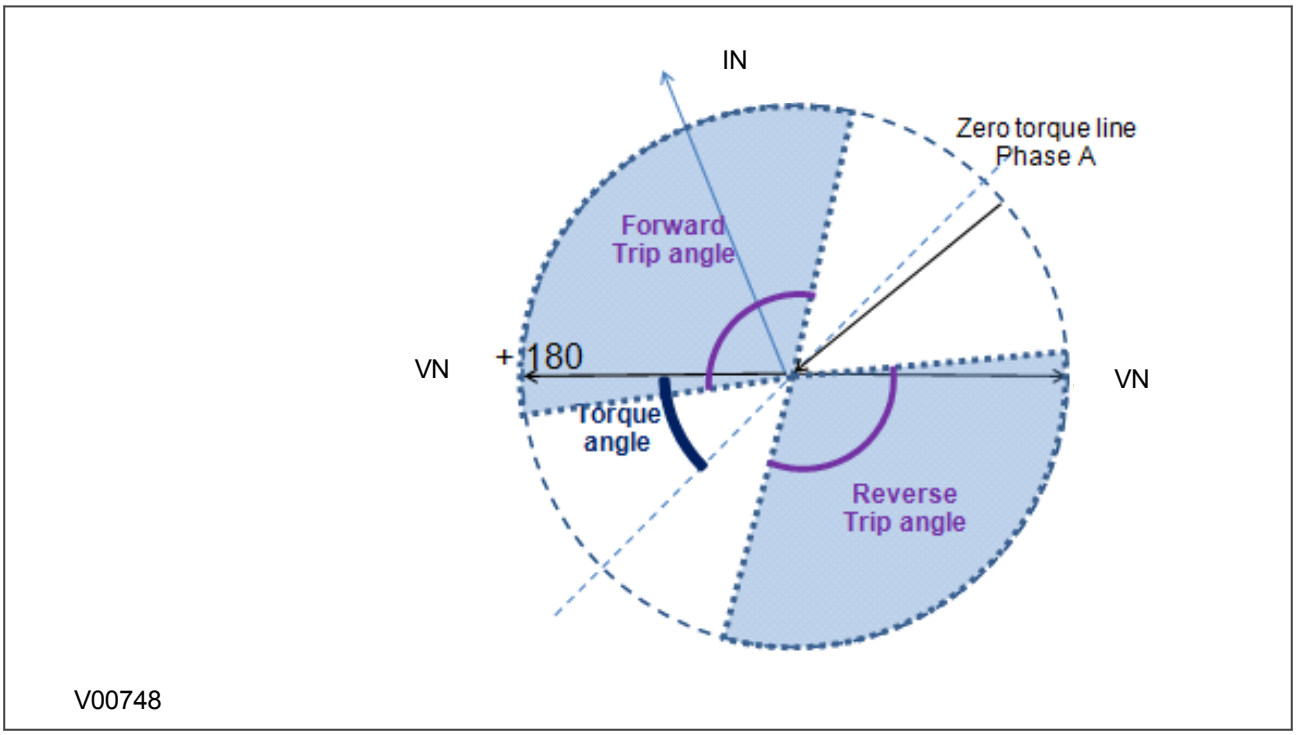


Figure 35: Directional angles

Some of the models derive the Residual Voltage quantity internally, from the 3-phase voltage input supplied from either a 5-limb or three single-phase VTs.On models with 4th VT input, this feature can be used for Check Sync or to measure the Residual Voltage VN. The 4th VT input can be configured for measured or derived voltage.

7.4.1.1 DIRECTIONAL EARTH FAULT LOGIC WITH RESIDUAL VOLTAGE POLARISATION

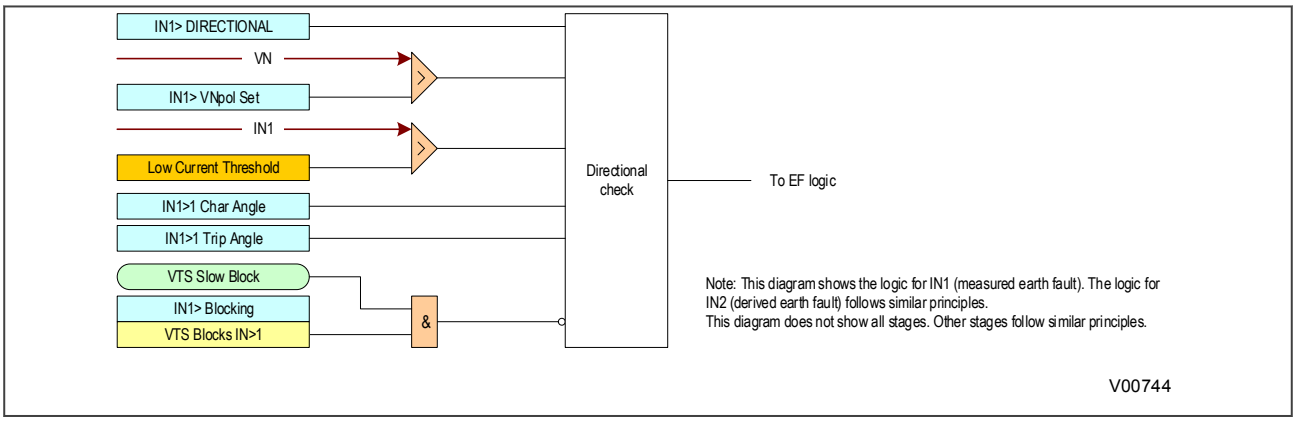


Figure 36: Directional EF logic with neutral voltage polarization (single stage)

Voltage Transformer Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the Start outputs as well.

7.4.2 NEGATIVE SEQUENCE POLARISATION

In some applications, the use of residual voltage polarisation may be not possible to achieve, or at the very least, problematic. For example, a suitable type of VT may be unavailable, or an HV/EHV parallel line application may present problems with zero sequence mutual coupling.

In such situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarisation. This method determines the fault direction by comparing the NPS voltage with the NPS current. The operating quantity, however, is still residual current.

This can be used for both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells ***IN> V2pol Set*** and ***IN> I2pol set*** respectively.

Negative phase sequence polarising is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance to negligible levels. If this voltage is less than 0.5 volts the device will stop providing directionalisation.

The directional criteria with negative sequence polarisation is given below:

Directional forward

$$(\angle V2 + 180°) + RCA - 90° + (180° - \text{tripping angle})/2 < \angle I2 < (\angle V2 + 180°) + RCA + 90° - (180° - \text{tripping angle})/2$$

Directional reverse

$$(\angle V2 + 180°) + RCA - 90° - (180° - \text{tripping angle})/2 > \angle I2 > (\angle V2 + 180°) + RCA + 90° + (180° - \text{tripping angle})/2$$

This can be best visualised with reference to the following diagram:

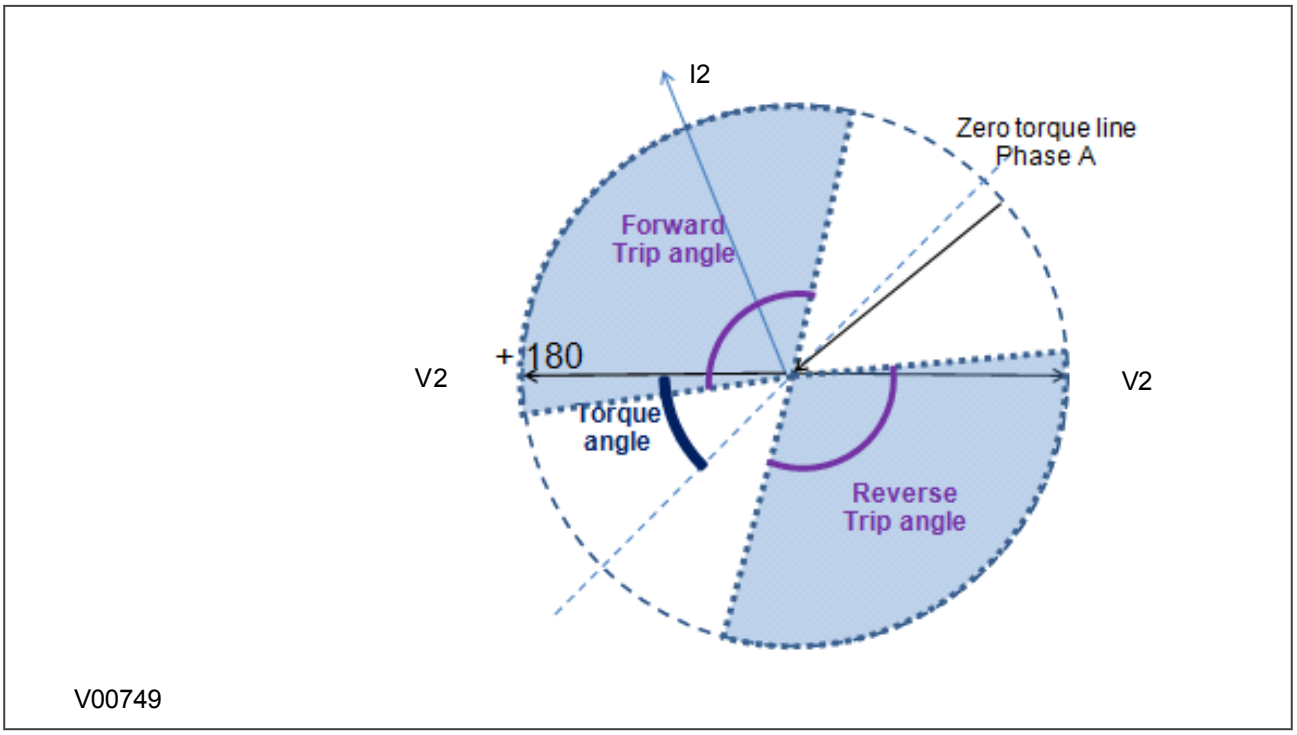


Figure 37: Directional angles

7.4.2.1 DIRECTIONAL EARTH FAULT LOGIC WITH NPS POLARISATION

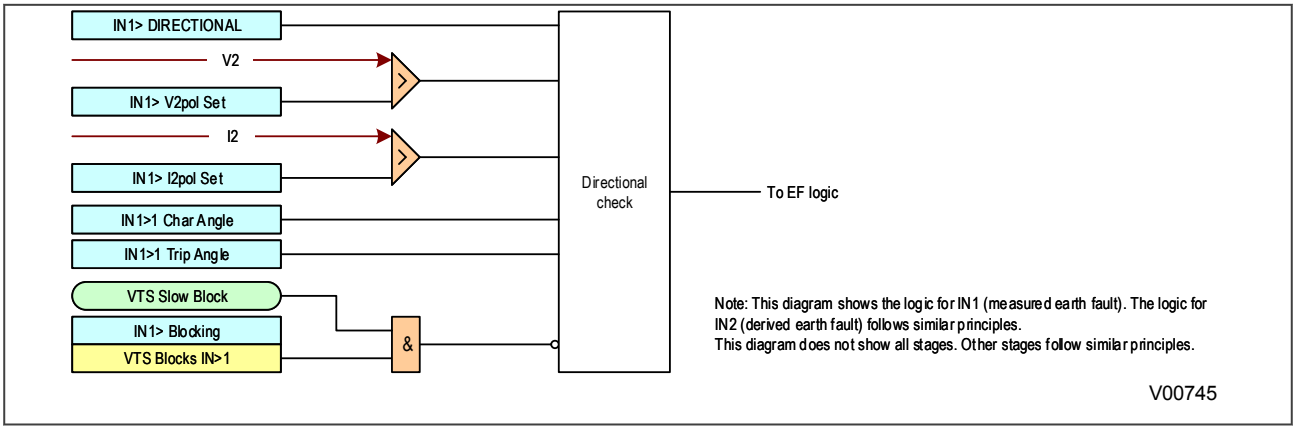


Figure 38: *Directional Earth Fault logic with negative sequence polarisation (single stage)

Voltage Transformer Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the Start outputs as well.

7.5 APPLICATION NOTES

7.5.1 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

With directional earth faults, the residual current under fault conditions lies at an angle lagging the polarising voltage. Hence, negative RCA settings are required for DEF applications. This is set in the cell ***I> Char Angle*** in the relevant earth fault menu.

We recommend the following RCA settings:

- Resistance earthed systems: 0°
- Distribution systems (solidly earthed): -45°
- Transmission systems (solidly earthed): -60°

7.5.2 PETERSEN COIL EARTHED SYSTEMS

A Petersen Coil earthing system is used in compensated earthing systems, as well as being used in cases of high impedance earthing. Petersen Coil earthed systems (also called compensated or resonant systems) are commonly found in areas where the system consists mainly of rural overhead lines. They are particularly beneficial in locations which are subject to a high incidence of transient faults. In a Petersen Coil earthed system, the network is earthed via a reactor, whose reactance is tuned to be nominally equal to the total system capacitance to earth. Similar to insulated systems, if a single-phase to earth fault is applied to a Petersen Coil earthed system, under steady state conditions no earth fault current flows. The effectiveness of the method in reducing the current to zero is dependent on the accuracy of the tuning of the reactance value and any changes in system capacitance (for example due to system configuration changes) require changes to the coil reactance. In practice, perfect matching of the coil reactance to the system capacitance is difficult to achieve, so that a small earth fault current will flow.

In isolated and compensated earthed systems, if an earth fault current is below a certain level, then the fault will self-extinguish due to the low current magnitude. It therefore appears as a transient phenomenon. The figure below shows earth fault current levels, below which they self-extinguish on these types of system. Statistics demonstrate that around 80% of earth faults in Petersen Coil earthed systems self-extinguish. This, in part, explains their popularity.

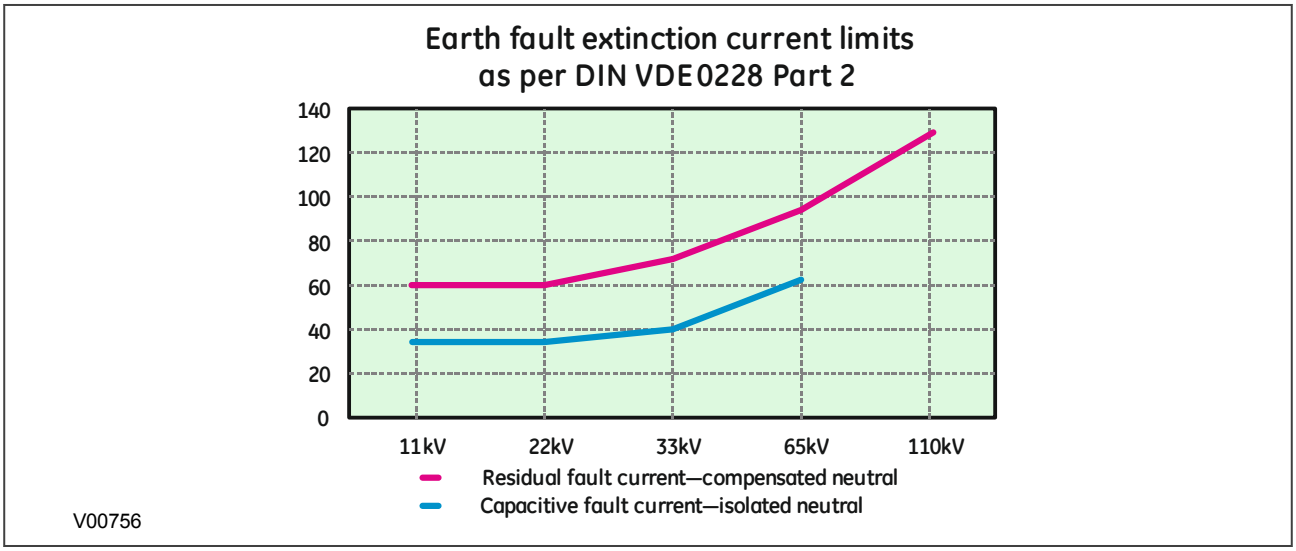


Figure 39: Current level (amps) at which transient faults are self-extinguishing

The following figure depicts a simple network earthed through a Petersen Coil reactance. It can be shown that if the reactor is correctly tuned, theoretically no earth fault current will flow.

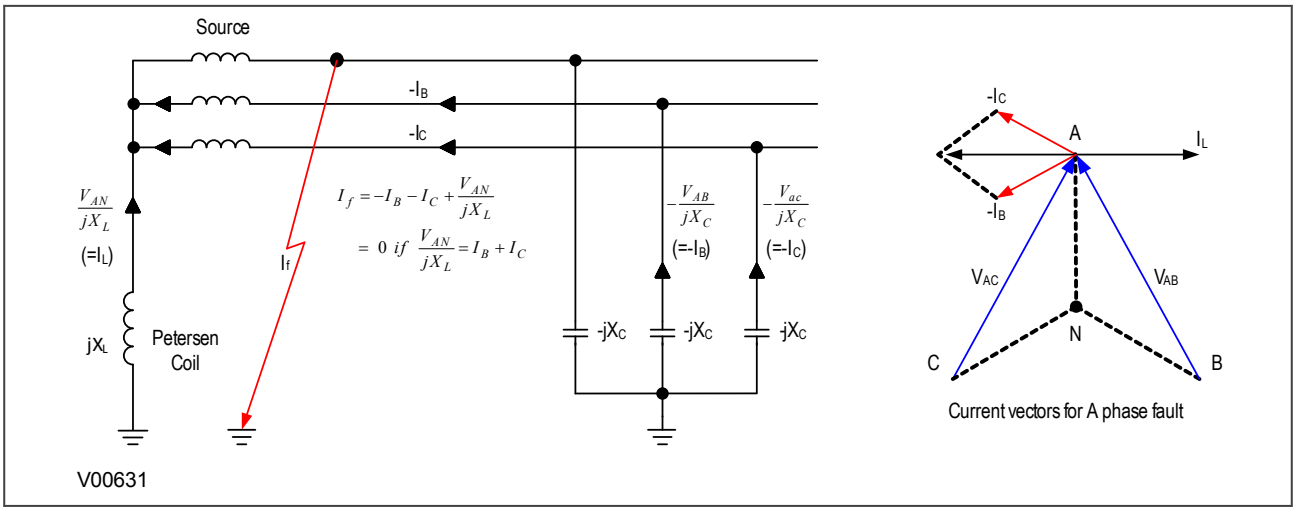


Figure 40: Earth fault in Petersen Coil earthed system

Consider a radial distribution system earthed using a Petersen Coil with a phase to earth fault on phase C, shown in the figure below:

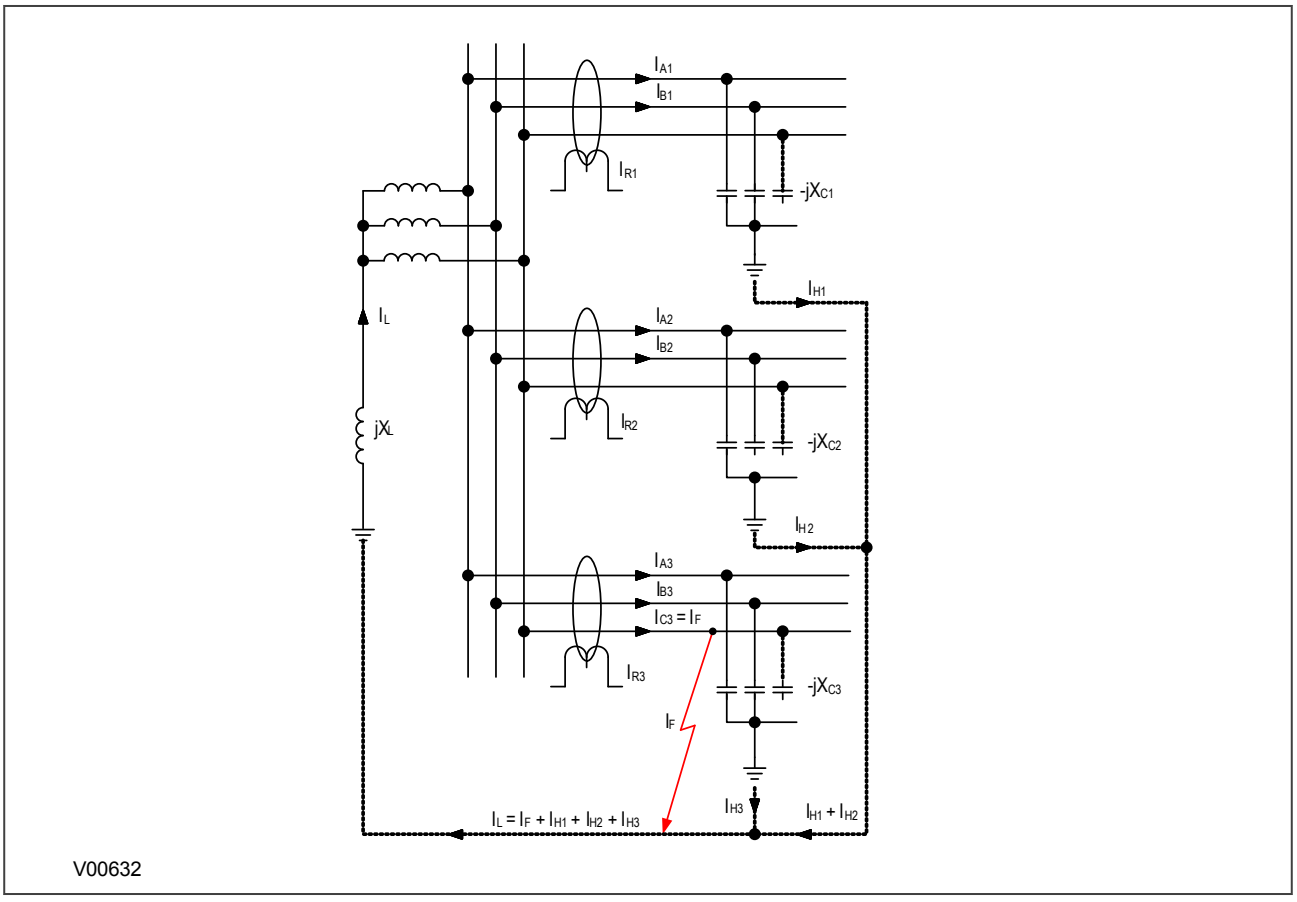


Figure 41: Distribution of currents during a Phase C fault

Assuming that no resistance is present in X_L or X_C, the resulting phasor diagrams will be as shown in the figure below:

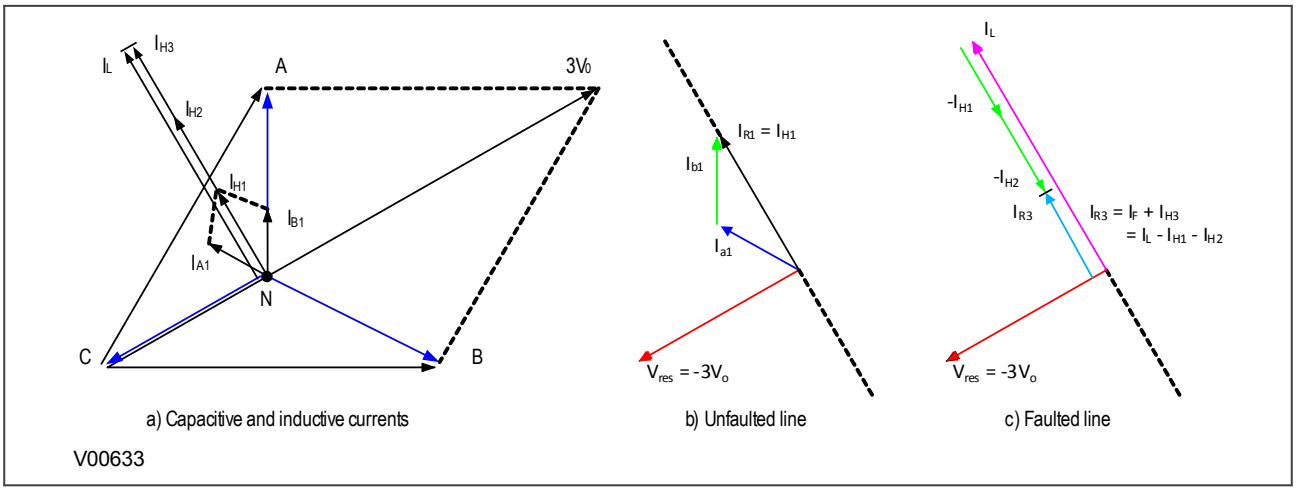


Figure 42: Phasors for a phase C earth fault in a Petersen Coil earthed system

It can be seen that:

- The voltage in the faulty phase reduces to almost 0V
- The healthy phases raise their phase to earth voltages by a factor of √3
- The triangle of voltages remains balanced
- The charging currents lead the voltages by 90°

Using a core-balance current transformer (CBCT), the current imbalances on the healthy feeders can be measured. They correspond to simple vector addition of I_{A1} and I_{B1}, I_{A2} and I_{B2}, I_{A3} and I_{B3}, and they lag the residual voltage by exactly 90º.

The magnitude of the residual current I_{R1} is equal to three times the steady-state charging current per phase. On the faulted feeder, the residual current is equal to I_L - I_{H1} - I_{H2} (C). This is shown in the zero sequence network shown in the following figure:

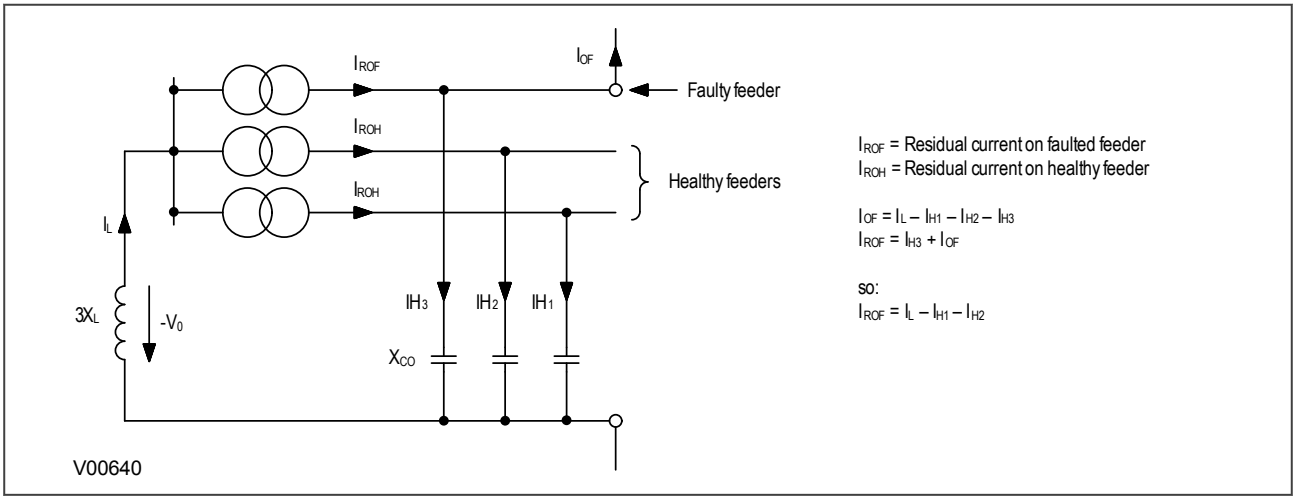


Figure 43: Zero sequence network showing residual currents

In practical cases, however, resistance is present, resulting in the following phasor diagrams:

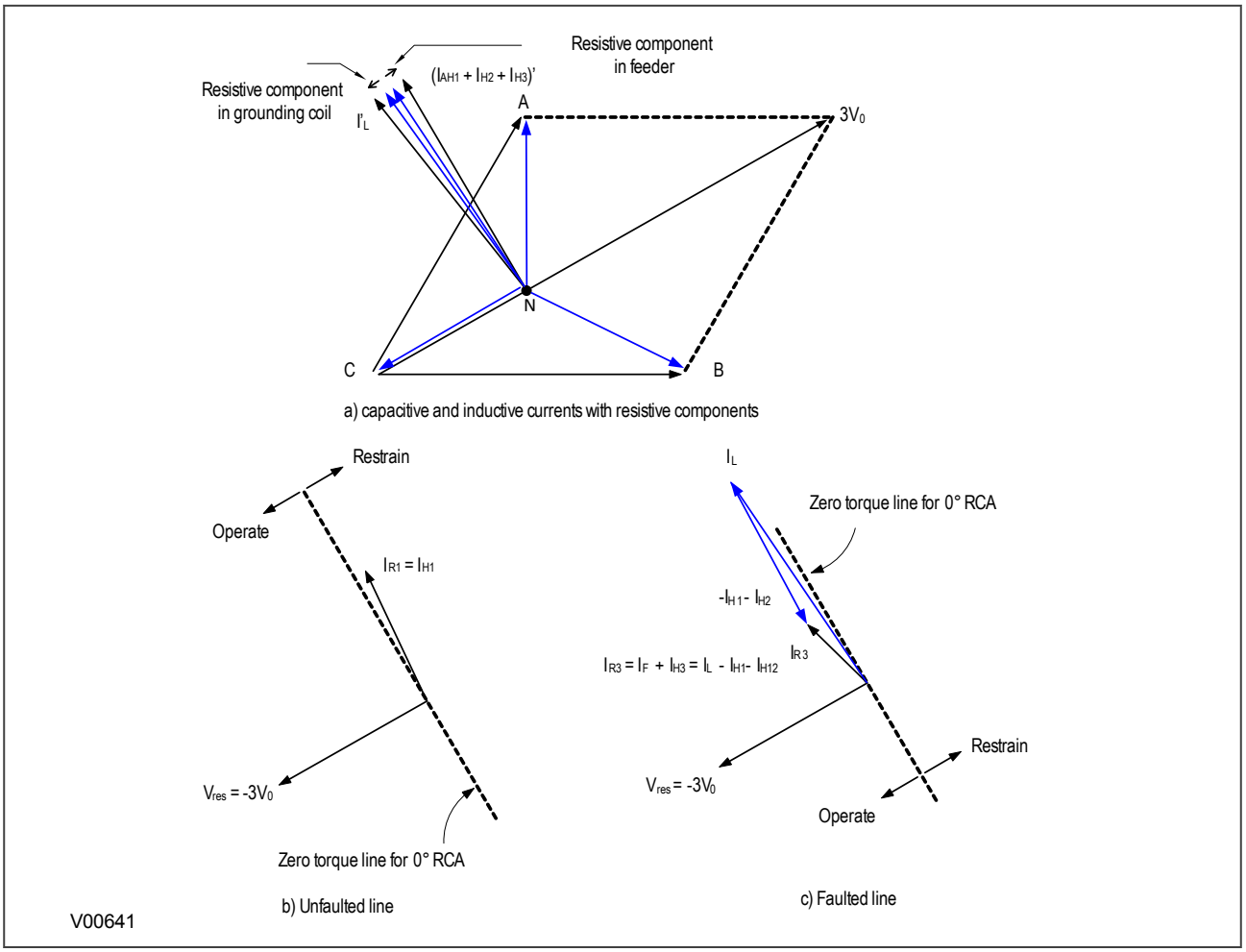


Figure 44: Phase C earth fault in Petersen Coil earthed system: practical case with resistance present

If the residual voltage is used as the polarising voltage, the residual current is phase shifted by an angle less than 90° on the faulted feeder, and greater than 90° on the healthy feeders. With an RCA of 0°, the healthy feeder residual current will fall in the 'restrain' area of the characteristic while the faulted feeder residual current falls in the 'operate' area.

Often, a resistance is deliberately inserted in parallel with the Petersen Coil to ensure a measurable earth fault current and increase the angular difference between the residual signals to reinforce the directional decision.

Directionality is usually implemented using a Wattmetric function, or a transient earth fault detection function (TEFD), rather than a simple directional function, since they are more sensitive. For further information about TEFD, refer to Transient Earth Fault Detection in the Current Protection Functions chapter.

7.5.3 SETTING GUIDELINES (COMPENSATED NETWORKS)

The directional setting should be such that the forward direction is looking down into the protected feeder (away from the busbar), with a 0° RCA setting.

For a fully compensated system, the residual current detected by the relay on the faulted feeder is equal to the coil current minus the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the steady state per phase value. Therefore, for a fully compensated system, the detected unbalanced current is equal to three times the per phase charging current of the faulted circuit. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the faulted circuit. In practise, the exact settings may well be determined on site, where system faults can be applied and suitable settings can be adopted based on practically obtained results.

In most situations, the system will not be fully compensated and consequently a small level of steady state fault current will be allowed to flow. The residual current seen by the protection on the faulted feeder may therefore be a larger value, which further emphasises the fact that the protection settings should be based upon practical current levels, wherever possible.

The above also holds true for the RCA setting. As has been shown, a nominal RCA setting of 0º is required. However, fine-tuning of this setting on-site may be necessary in order to obtain the optimum setting in accordance with the levels of coil and feeder resistances present. The loading and performance of the CT will also have an effect in this regard. The effect of CT magnetising current will be to create phase lead of current. Whilst this would assist with operation of faulted feeder IEDs, it would reduce the stability margin of healthy feeder IEDs. A compromise can therefore be reached through fine adjustment of the RCA. This is adjustable in 1° steps.

8 SENSITIVE EARTH FAULT PROTECTION

With some earth faults, the fault current flowing to earth is limited by either intentional resistance (as is the case with some HV systems) or unintentional resistance (e.g. in very dry conditions and where the substrate is high resistance, such as sand or rock).

To provide protection in such cases, it is necessary to provide an earth fault protection system with a setting that is considerably lower than for normal line protection. Such sensitivity cannot be provided with conventional CTs, therefore the SEF input would normally be fed from a core balance current transformer (CBCT) mounted around the three phases of the feeder cable. The SEF transformer should be a special measurement class transformer.

8.1 SEF PROTECTION IMPLEMENTATION

The product provides four stages of SEF protection with independent time delay characteristics.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of IDMT (Inverse Definite Minimum Time) curves
- A range of User-defined curves
- DT (Definite Time)

This is achieved using the cells

- ***ISEF>(n) Function*** for the overcurrent operate characteristic
- ***ISEF>(n) Reset Char*** for the overcurrent reset characteristic
- ***ISEF>(n) Usr RstChar*** for the reset characteristic for user -defined curves

where (n) is the number of the stage.

Stages 1 and 2 also provide a Timer Hold facility. This is configured using the cells ***ISEF>(n) tReset***.

Stages 3 and 4 have definite time characteristics only.

8.2 NON-DIRECTIONAL SEF LOGIC

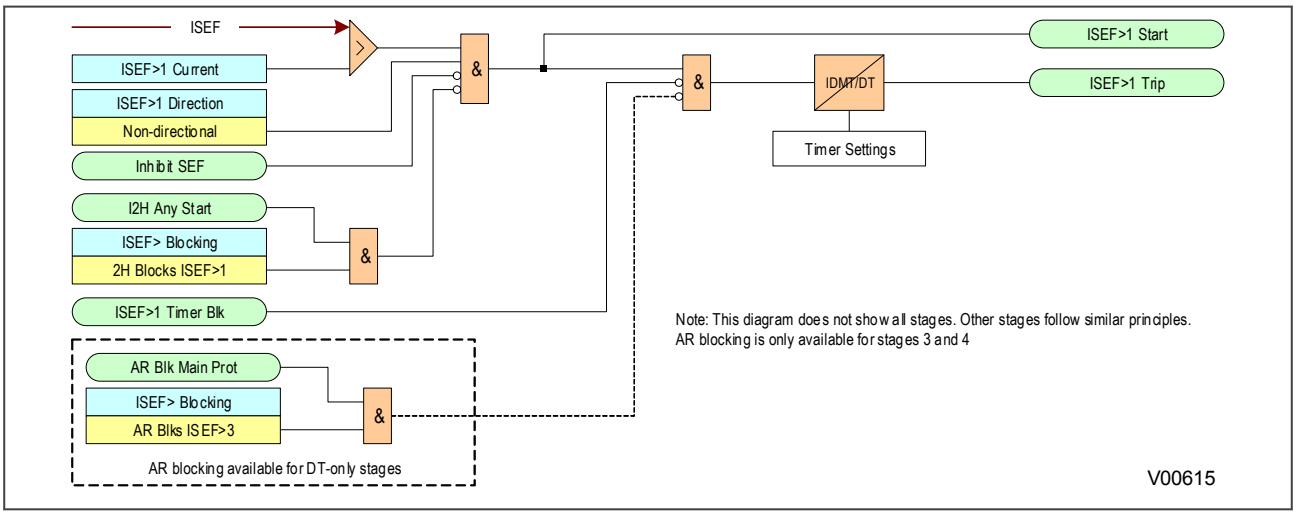


Figure 45: Non-directional SEF logic

The SEF current is compared with a set threshold (***ISEF>(n) Current***) for each stage. If it exceeds this threshold, a Start signal is triggered, providing it is not blocked. This can be blocked by the second harmonic blocking function, or an Inhibit SEF DDB signal.

The autoreclose logic can be set to block the SEF trip after a prescribed number of shots (set in *AUTORECLOSE* column). This is achieved using the ***AR Blk Main Prot*** setting. This can also be blocked by the relevant timer block signal ***ISEF>(n)TimerBlk*** DDB signal.

SEF protection can follow the same IDMT characteristics as described in the Overcurrent Protection Principles section. Please refer to this section for details of IDMT characteristics.

8.3 EPATR B CURVE

The EPATR B curve is commonly used for time-delayed Sensitive Earth Fault protection in certain markets. This curve is only available in the Sensitive Earth Fault protection stages 1 and 2. It is based on primary current settings, employing a SEF CT ratio of 100:1 A.

The EPATR_B curve has 3 separate segments defined in terms of the primary current. It is defined as follows:

Segment	Primary Current Range Based on 100A:1A CT Ratio	Current/Time Characteristic
1	ISEF = 0.5A to 6.0A	t = 432 x TMS/ISEF 0.655 secs
2	ISEF = 6.0A to 200A	t = 800 x TMS/ISEF secs
3	ISEF above 200A	t = 4 x TMS secs

where TMS (time multiplier setting) is 0.025 - 1.2 in steps of 0.025.

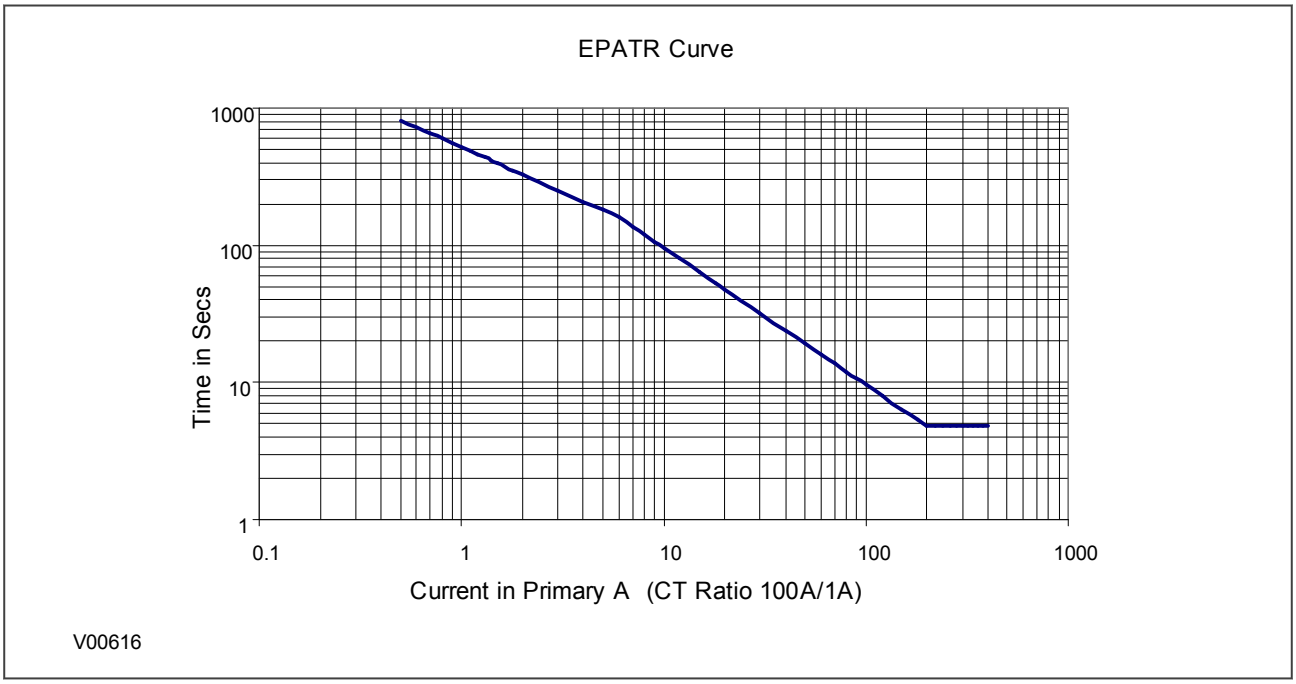


Figure 46: EPATR B characteristic shown for TMS = 1.0

Note:
SEF CT ratios are user settable.

8.4 DIRECTIONAL ELEMENT

Where current may flow in either direction, directional control should be used.

A directional element is available for all of the SEF overcurrent stages. This is found in the ***ISEF>(n) Direction*** cell for the relevant stage. It can be set to non-directional, directional forward, or directional reverse.

Directionality is achieved by using different techniques depending on the application. With reference to the figure below, you can see that directional SEF can be used for:

- Solidly earthed systems
- Unearthed systems (insulated systems)
- Compensated systems
- Resistance earthed systems

The following diagram shows which type of directional control can be used for which systems.

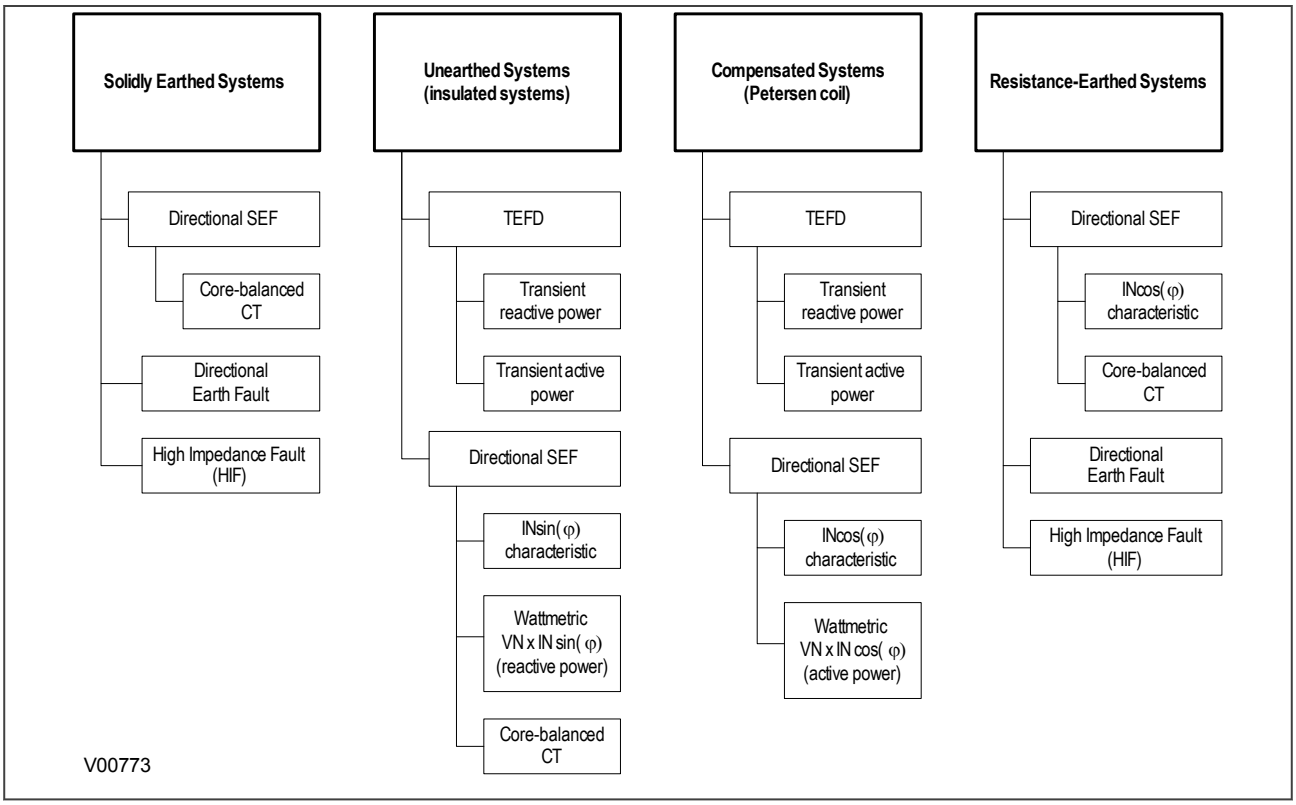


Figure 47: Types of directional control

The device supports standard core-balanced directional control as well as Isin(ϕ), Icos(ϕ) and Wattmetric characteristics.

If you are using directional SEF protection, you select the required polarisation using the ***SEF Options*** setting in the *SEF PROTECTION* column.

8.4.1 WATTMETRIC CHARACTERISTIC

Analysis has shown that a small angular difference exists between the spill current on healthy and faulted feeders for earth faults on compensated networks. This angular difference gives rise to active components of current which are in anti-phase to one another.

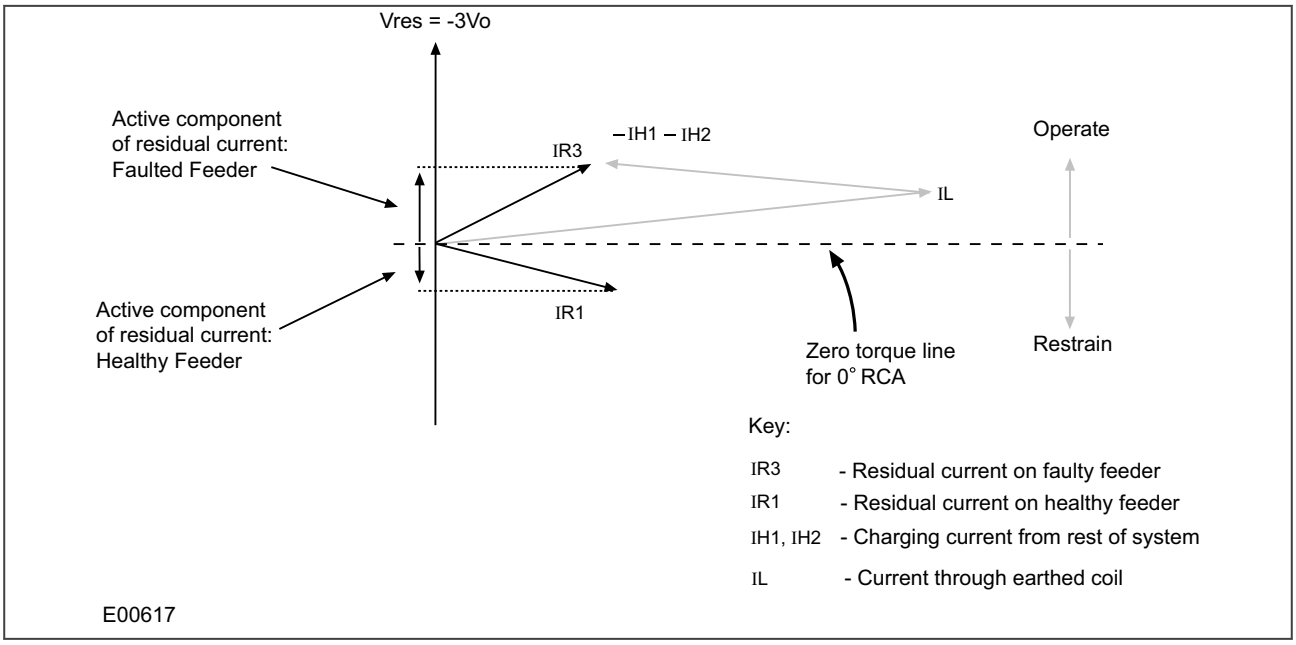


Figure 48: Resistive components of spill current

Consequently, the active components of zero sequence power will also lie in similar planes, meaning an IED capable of detecting active power can make discriminatory decisions. If the Wattmetric component of zero sequence power is detected in the forward direction, then this would indicate fault on that feeder. If power is detected in the reverse direction, then the fault must be present on an adjacent feeder or at the source.

For operation of the directional earth fault element, all three of the settable thresholds must be exceeded; namely the current ISEF>, the voltage ***ISEF>VNpol Set*** and the power ***PN> Setting***.

The power setting is called PN> and is calculated using residual quantities. The formula for operation is as follows:

The PN> setting corresponds to:

$$V_{res}I_{res}cos(\phi - \phi_c) = 9V_oI_ocos(\phi - \phi_c)$$

where:

- ϕ = Angle between the Polarising Voltage (**-Vres**) and the Residual Current
- ϕ_c = Relay Characteristic Angle (RCA) Setting (***ISEF> Char Angle***)
- V_{res} = Residual Voltage
- I_{res} = Residual Current
- V_o = Zero Sequence Voltage
- I_o = Zero Sequence Current

The action of setting the PN> threshold to zero would effectively disable the wattmetric function and the device would operate as a basic, sensitive directional earth fault element. However, if this is required, then the SEF option can be selected from the ***SEF/REF Options*** cell in the menu.

Note:
The residual power setting, PN>, is scaled by the programmed Transformer ratios.

A further point to note is that when a power threshold other than zero is selected, a slight alteration is made to the angular boundaries of the directional characteristic. Rather than being ±90° from the RCA, they are made slightly narrower at ±85°.

The directional check criteria is as follows:

Directional forward: -85° < (angle(IN) - angle(VN + 180°) - RCA) < 85°

Directional reverse: -85° > (angle(IN) - angle(VN + 180°) - RCA) > 85°

8.4.2 ICOS PHI / ISIN PHI CHARACTERISTIC

In some applications, the residual current on the healthy feeder can lie just inside the operating boundary following a fault condition. The residual current for the faulted feeder lies close to the operating boundary.

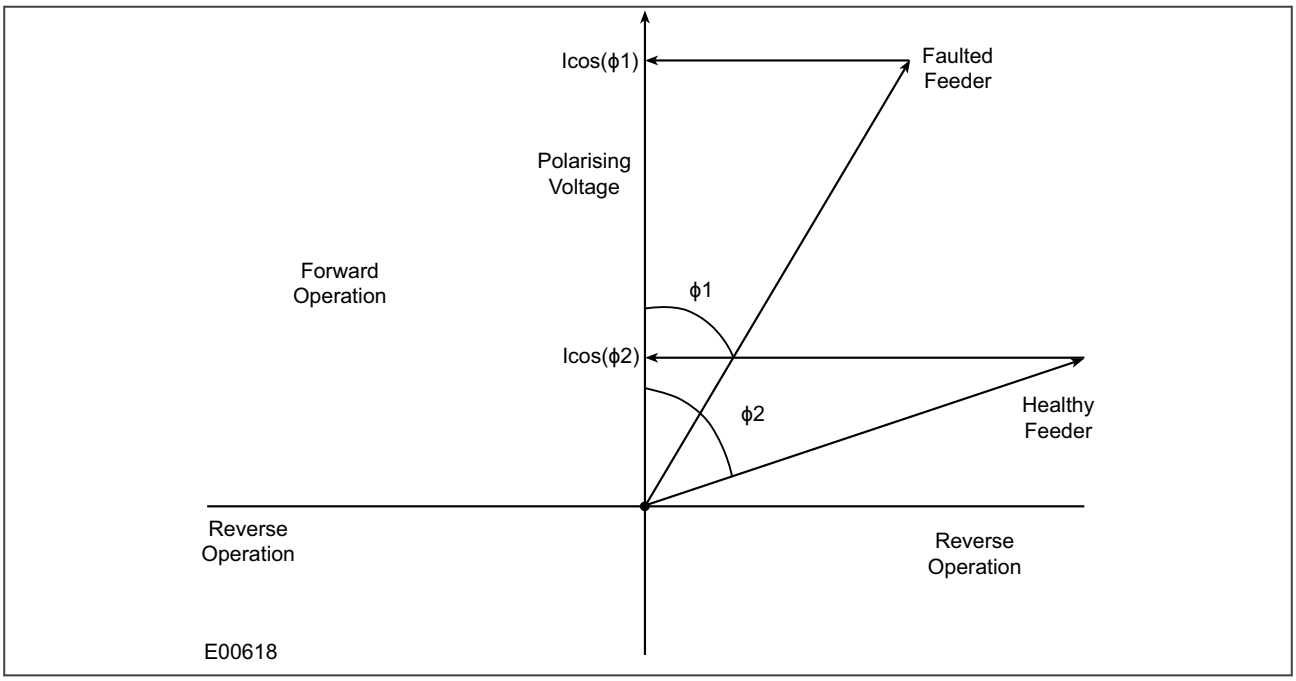


Figure 49: Operating characteristic for Icos

The diagram illustrates the method of discrimination when the real (cosϕ) component is considered. Faults close to the polarising voltage will have a higher magnitude than those close to the operating boundary. In the diagram, we assume that the current magnitude I is in both the faulted and non-faulted feeders.

- For the active component Icos, the criterion for operation is: Icosϕ > ***ISEF>(n) current***
- For the reactive component Isin, the criterion for operation is: Isinϕ > ***ISEF>(n) current***

Where ***ISEF>(n) current*** is the sensitive earth fault current setting for the stage in question

If any stage is set to non-directional, the element reverts back to normal operation based on current magnitude I with no directional decision. In this case, correct discrimination is achieved by means of an Icos characteristic as the faulted feeder will have a large active component of residual current, whilst the healthy feeder will have a small value.

For insulated earth applications, it is common to use the Isin characteristic.

All of the relevant settings can be found under the *SEF PROTECTION* column.

8.4.3 DIRECTIONAL SEF LOGIC

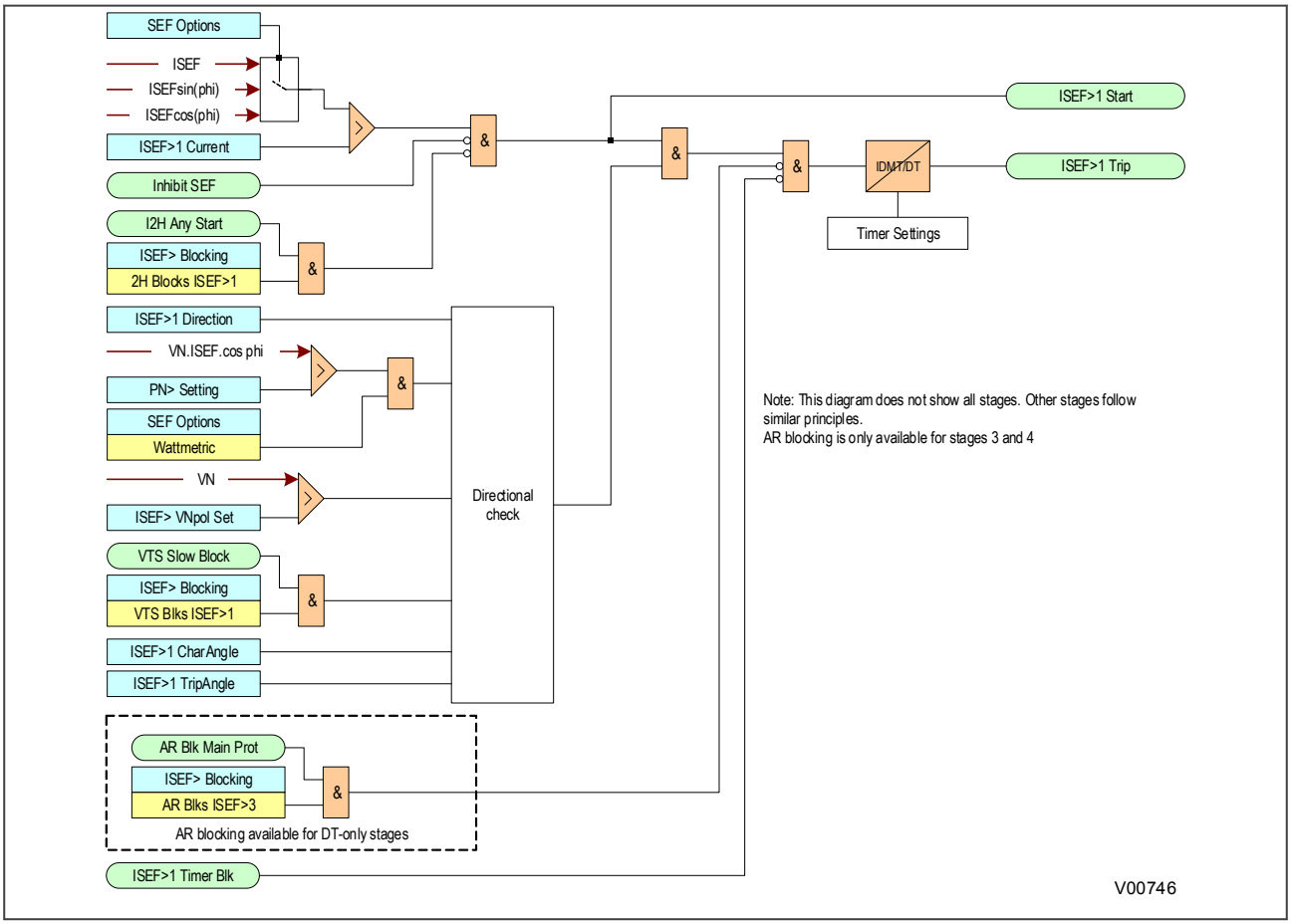


Figure 50: Directional SEF with VN polarisation (single stage)

The sensitive earth fault protection can be set IN/OUT of service using the appropriate DDB inhibit signal, which can be operated from an opto-input or control command. VT Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the start outputs as well.

The directional check criteria are given below for the standard directional sensitive earth fault element:

- Directional forward: -90° < (angle(IN) - angle(VN + 180°) - RCA) < 90°
- Directional reverse: -90° > (angle(IN) - angle(VN + 180°) - RCA) > 90°

Three possibilities exist for the type of protection element that you can use for sensitive earth fault detection:

- A suitably sensitive directional earth fault protection element having a characteristic angle setting (RCA) of zero degrees, with the possibility of fine adjustment about this threshold.
- A sensitive directional zero sequence wattmetric protection element having a characteristic angle setting (RCA) of zero degrees, with the possibility of fine adjustment about this threshold.
- A sensitive directional earth fault protection element having Icosϕ and Isinϕ characteristics.

All stages of the sensitive earth fault element can be set down to 0.5% of rated current.

8.5 APPLICATION NOTES

8.5.1 INSULATED SYSTEMS

When insulated systems are used, it is not possible to detect faults using standard earth fault protection. It is possible to use a residual overvoltage device to achieve this, but even with this method full discrimination is not possible. Fully discriminative earth fault protection on this type of system can only be achieved by using a SEF (Sensitive Earth Fault) element. This type of protection detects the resultant imbalance in the system charging currents that occurs under earth fault conditions. A core balanced CT must be used for this application. This eliminates the possibility of spill current that may arise from slight mismatches between residually connected line CTs. It also enables a much lower CT ratio to be applied, thereby allowing the required protection sensitivity to be more easily achieved.

The following diagram shows an insulated system with a C-phase fault.

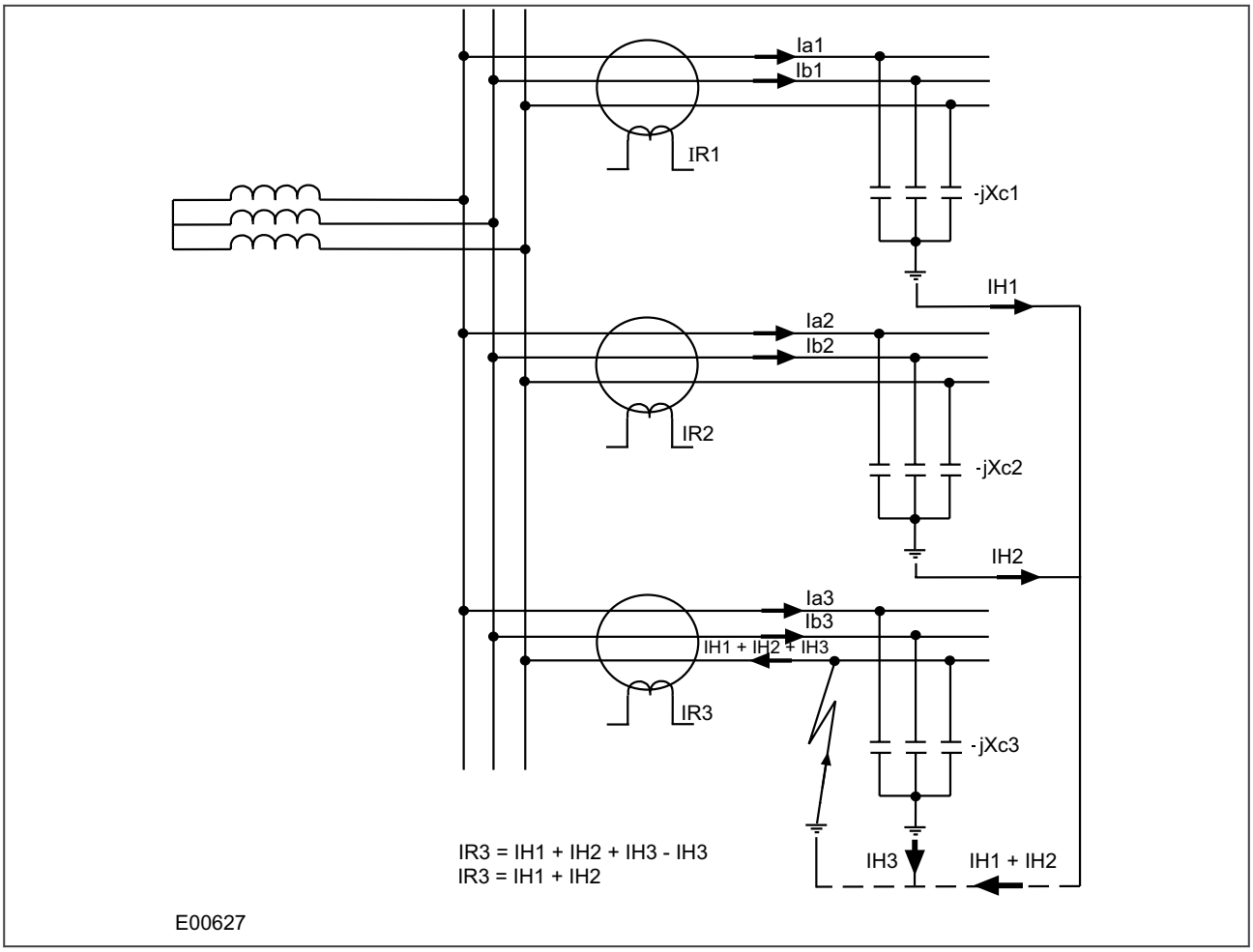


Figure 51: Current distribution in an insulated system with C phase fault

The protection elements on the healthy feeder see the charging current imbalance for their own feeder. The protection element on the faulted feeder, however, sees the charging current from the rest of the system (IH1 and IH2 in this case). Its own feeder's charging current (IH3) is cancelled out.

With reference to the associated vector diagram, it can be seen that the C-phase to earth fault causes the voltages on the healthy phases to rise by a factor of √3. The A-phase charging current (Ia1), leads the resultant A phase voltage by 90°. Likewise, the B-phase charging current leads the resultant Vb by 90°.

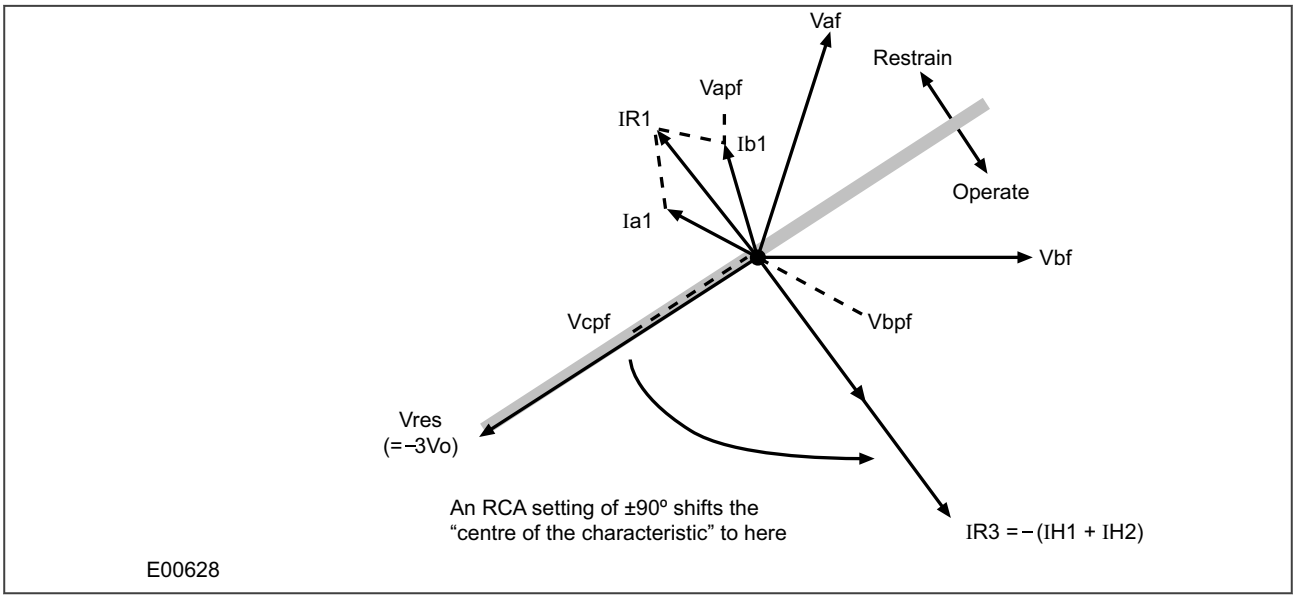


Figure 52: Phasor diagrams for insulated system with C phase fault

The current imbalance detected by a core balanced current transformer on the healthy feeders is the vector addition of Ia1 and Ib1. This gives a residual current which lags the polarising voltage (–3Vo) by 90°. As the healthy phase voltages have risen by a factor of √3, the charging currents on these phases are also √3 times larger than their steady state values. Therefore, the magnitude of the residual current IR1, is equal to 3 times the steady state per phase charging current.

The phasor diagram indicates that the residual currents on the healthy and faulted feeders (IR1 and IR3 respectively) are in anti-phase. A directional element (if available) could therefore be used to provide discriminative earth fault protection.

If the polarising is shifted through +90°, the residual current seen by the relay on the faulted feeder will lie within the operate region of the directional characteristic and the current on the healthy feeders will fall within the restrain region.

The required characteristic angle setting for the SEF element when applied to insulated systems, is +90°. This is for the case when the protection is connected such that its direction of current flow for operation is from the source busbar towards the feeder. If the forward direction for operation were set such that it is from the feeder into the busbar, then a –90° RCA would be required.

Note:
Discrimination can be provided without the need for directional control. This can only be achieved, however, if it is possible to set the IED in excess of the charging current of the protected feeder and below the charging current for the rest of the system.

8.5.2 SETTING GUIDELINES (INSULATED SYSTEMS)

The residual current on the faulted feeder is equal to the sum of the charging currents flowing from the rest of the system. Further, the addition of the two healthy phase charging currents on each feeder gives a total charging current which has a magnitude of three times the per phase value. Therefore, the total imbalance current is equal to three times the per phase charging current of the rest of the system. A typical setting may therefore be in the order of 30% of this value, i.e. equal to the per phase charging current of the remaining system. Practically though, the required setting may well be determined on site, where suitable settings can be adopted based on practically obtained results.

When using a core-balanced transformer, care must be taken in the positioning of the CT with respect to the earthing of the cable sheath:

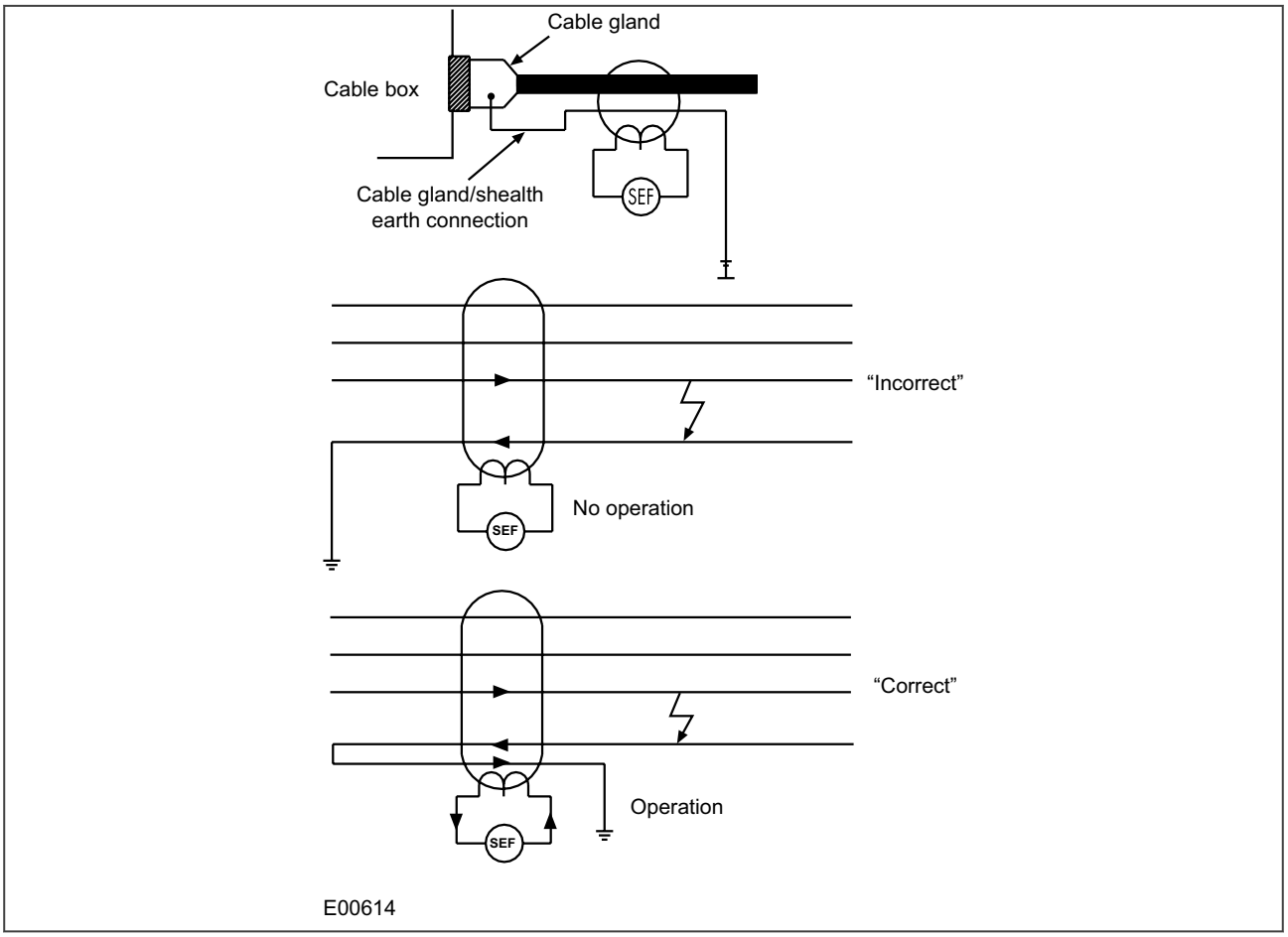


Figure 53: Positioning of core balance current transformers

If the cable sheath is terminated at the cable gland and directly earthed at that point, a cable fault (from phase to sheath) will not result in any unbalanced current in the core balance CT. Therefore, prior to earthing, the connection must be brought back through the CBCT and earthed on the feeder side. This then ensures correct relay operation during earth fault conditions.

9 COLD LOAD PICKUP

When a feeder circuit breaker is closed in order to energise a load, the current levels that flow for a period of time following energisation may be far greater than the normal load levels. Consequently, overcurrent settings that have been applied to provide overcurrent protection may not be suitable during this period of energisation (cold load), as they may initiate undesired tripping of the circuit breaker. This scenario can be prevented with Cold Load Pickup (CLP) functionality.

The Cold Load Pick-Up (CLP) logic works by either:

- Blocking one or more stages of the overcurrent protection for a set duration
- Raising the overcurrent settings of selected stages, for the cold loading period.

The CLP logic therefore provides stability, whilst maintaining protection during the start-up.

9.1 IMPLEMENTATION

Cold Load Pickup Protection is configured in the *COLD LOAD PICKUP* column of the relevant settings group.

This function acts upon the following protection functions:

- All overcurrent stages (both non-directional and directional if applicable)
- All Earth Fault 1 stages (both non-directional and directional if applicable)
- All Earth Fault 2 stages (both non-directional and directional if applicable)

The principle of operation is identical for the 3-phase overcurrent protection and the first stages of Earth Fault overcurrent protection for both EF1 and EF2.

CLP operation occurs when the circuit breaker remains open for a time greater than ***tcold*** and is subsequently closed. CLP operation is applied after ***tcold*** and remains for a set time delay of ***tclp*** following closure of the circuit breaker. The status of the circuit breaker is provided either by means of the CB auxiliary contacts or by means of an external device via logic inputs. Whilst CLP operation is in force, the CLP settings are enabled After the time delay ***tclp*** has elapsed, the normal overcurrent settings are applied and the CLP settings are disabled.

If desired, instead of applying different current setting thresholds for the cold load time, it is also possible to completely block the overcurrrent operation during this time, for any of the overcurrent stages.

Voltage-dependent operation can also affect the overcurrent settings. If a Voltage Dependent condition arises, this takes precedence over the CLP function. If the CLP condition prevails and the Voltage Dependent function resets, the device will operate using the CLP settings. Time-delayed elements are reset to zero if they are disabled during the transitions between normal settings and CLP settings.

9.2 CLP LOGIC

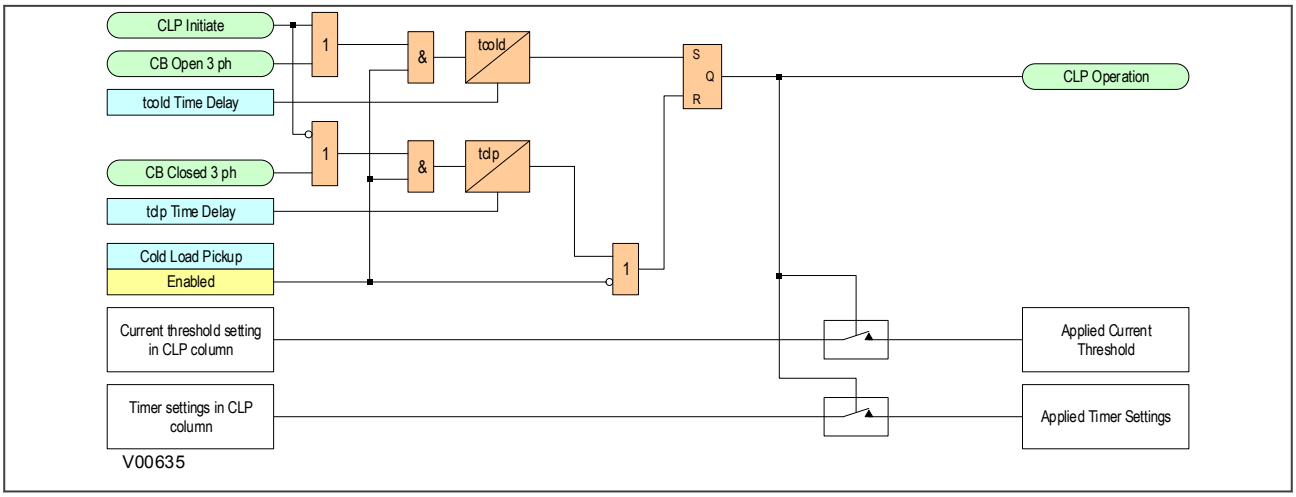


Figure 54: Cold Load Pickup logic

The CLP Operation signal indicates that CLP logic is in operation. This only happens when CLP is enabled AND CLP is initiated either externally or from a CB Open condition after the ***tcold*** period has elapsed. The CLP Operation indicator goes low when CLP is disabled or when the external CLP trigger is removed or when there is a CB closed condition.

tcold and ***tclp*** are initiated via the CB open and CB closed signals generated within the device. These signals are produced by connecting auxiliary contacts from the circuit breaker or starting device to the IED's opto-inputs

If dual CB contacts are not available (one for Open (52a) and for Close (52b)) you can configure the device to be driven from a single contact (either 52a or 52b). The device would then simply invert one signal to provide the other. This option is available using the ***CB status input*** cell in the *CB CONTROL* column. The setting can be set to `None`, `52a`, `52b` or `52a` and `52b`.

9.3 APPLICATION NOTES

9.3.1 CLP FOR RESISTIVE LOADS

A typical example of where CLP logic may be used is for resistive heating loads such as such as air conditioning systems. Resistive loads typically offer less resistance when cold than when warm, hence the start-up current will be higher.

To set up the CLP, you need to select `Enable` from the ***I> status*** option to enable the settings of the temporary current and time settings. These settings should be chosen in accordance with the expected load profile. Where it is not necessary to alter the setting of a particular stage, the CLP settings should be set to the same level as the standard overcurrent settings.

It may not be necessary to alter the protection settings following a short supply interruption. In this case a suitable ***tcold*** timer setting can be used.

9.3.2 CLP FOR MOTOR FEEDERS

In general, a dedicated motor protection device would protect feeders supplying motor loads. However, if CLP logic is available in a feeder device, this may be used to modify the overcurrent settings during start-up.

Depending on the magnitude and duration of the motor starting current, it may be sufficient to simply block operation of instantaneous elements. If the start duration is long, the time-delayed protection settings may also need to be raised. A combination of both blocking and raising of the overcurrent settings may be adopted. The CLP overcurrent settings in this case must be chosen with regard to the motor starting characteristic.

This may be useful where instantaneous earth fault protection needs to be applied to the motor. During motor start-up conditions, it is likely that incorrect operation of the earth fault element would occur due to asymmetric CT saturation. This is due to the high level of starting current causing saturation of one or more of the line CTs feeding the overcurrent/earth fault protection. The resultant transient imbalance in the secondary line current quantities is therefore detected by the residually connected earth fault element. For this reason, it is normal to either apply a nominal time delay to the element, or to use a series stabilising resistor.

The CLP logic may be used to allow reduced operating times or current settings to be applied to the earth fault element under normal running conditions. These settings could then be raised prior to motor starting, by means of the logic.

9.3.3 CLP FOR SWITCH ONTO FAULT CONDITIONS

In some feeder applications, fast tripping may be required if a fault is already present on the feeder when it is energised. Such faults may be due to a fault condition not having been removed from the feeder, or due to earthing clamps having been left on following maintenance. In either case, it is desirable to clear the fault condition quickly, rather than waiting for the time delay imposed by IDMT overcurrent protection.

The CLP logic can cater for this situation. Selected overcurrent/earth fault stages could be set to instantaneous operation for a defined period following circuit breaker closure (typically 200 ms). Therefore, instantaneous fault clearance would be achieved for a switch onto fault (SOTF) condition.

10 SELECTIVE LOGIC

With Selective Logic you can use the Start signals to control the time delays of upstream IEDs, as an alternative to simply blocking them. This provides an alternative approach to achieving non-cascading types of overcurrent scheme.

10.1 SELECTIVE LOGIC IMPLEMENTATION

Selective Logic is set in the *SELECTIVE LOGIC* column of the relevant settings group.

The Selective Logic function works by temporarily increasing the time delay settings of the chosen overcurrent elements. This logic is initiated by issuing signals to an upstream IED.

This function acts on the following protection functions:

- Non-Directional/Directional phase overcurrent (3rd, 4th and 6th stages)
- Non-Directional/Directional earth fault – 1 (3rd and 4th stages)
- Non-Directional/Directional earth fault – 2 (3rd and 4th stages)
- Non-Directional/Directional sensitive earth fault (3rd and 4th stages)

Note:
In the event of a conflict between Selective Logic and CLP, Selective Logic takes precedence.

10.2 SELECTIVE LOGIC DIAGRAM

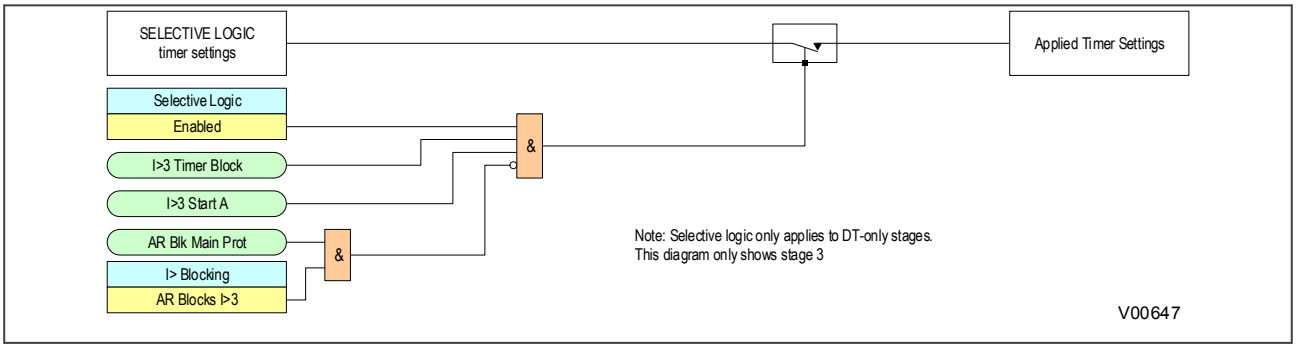


Figure 55: Selective Logic

The logic diagram is shown for overcurrent phase A, but is valid for all three phases for each of the stages. The principle of operation is also identical for earth fault protection.

When the selective logic function is enabled, the action of the blocking input is as follows:

No block applied

In the event of a fault condition that continuously asserts the start output, the function will assert a trip signal after the normal time delay has elapsed.

Logic input block applied

In the event of a fault condition that continuously asserts the start output, the function will assert a trip signal after the selective logic time delay has elapsed.

Auto-reclose input block applied

In the event of a fault condition that continuously asserts the start output, when an auto-reclose block is applied the function will not trip. The auto-reclose block also overrides the logic input block and will block the selective logic timer.

> *Note:*
> *The Auto-reclose function outputs two signals that block protection, namely;* ***AR Blk Main Prot*** *and* ***AR Blk SEF Prot****.*

AR Blk Main Prot is common to Phase Overcurrent, Earth Fault 1 and Earth Fault 2, whereas ***AR Blk SEF Prot*** is used for SEF protection.

11 TIMER SETTING SELECTION

The timer settings used depend on whether there is a Selective Overcurrent condition or a Cold Load Pickup condition (if this functionality is used). The protection function selects the settings according to the following flow diagram:

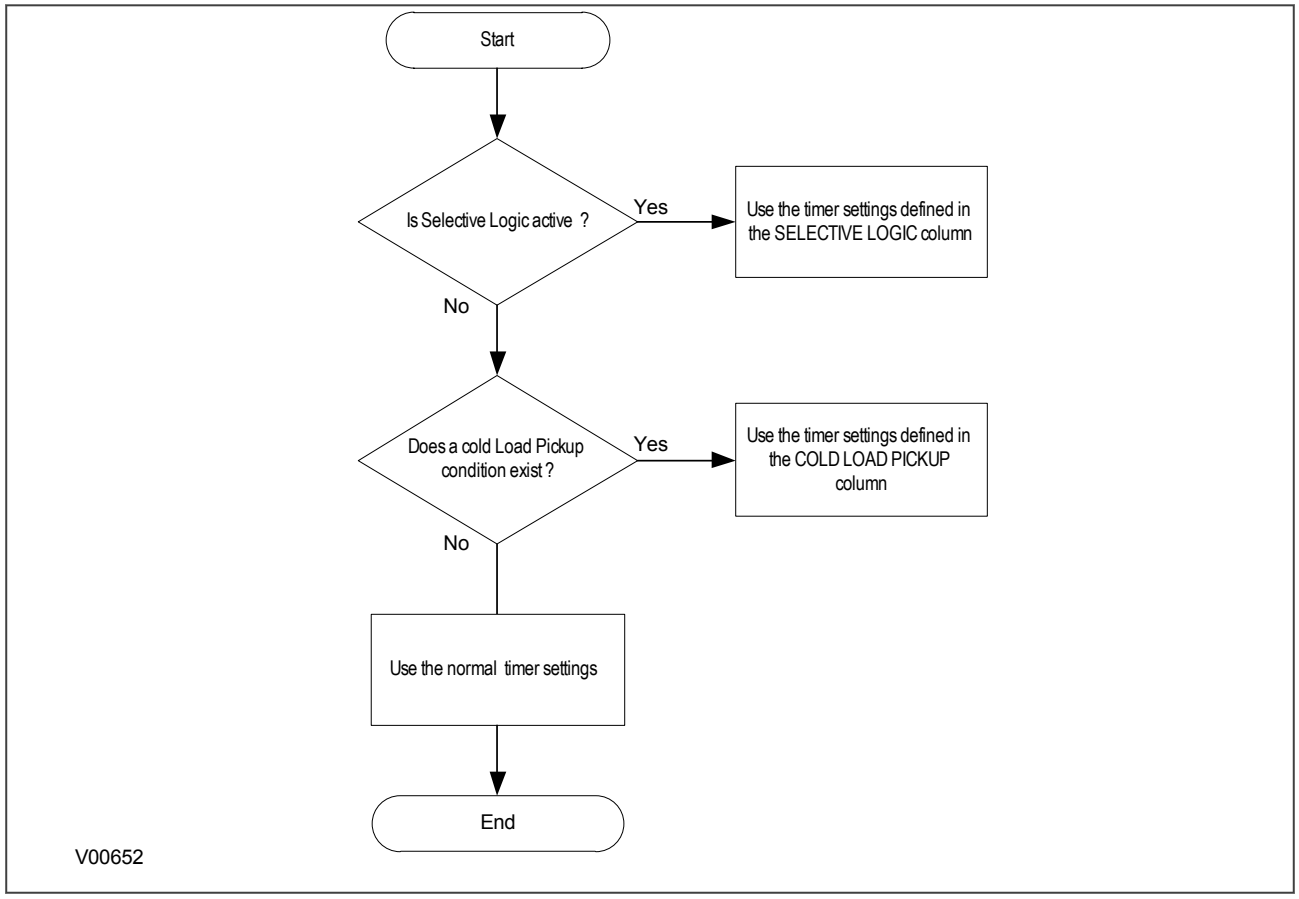


Figure 56: Selecting the timer settings

12 THERMAL OVERLOAD PROTECTION

The heat generated within an item of plant is the resistive loss. The thermal time characteristic is therefore based on the equation I^2Rt. Over-temperature conditions occur when currents in excess of their maximum rating are allowed to flow for a period of time.

Temperature changes during heating follow exponential time constants. The device provides two characteristics for thermal overload protection; a single time constant characteristic and a dual time constant characteristic. You select these according to the application.

12.1 SINGLE TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect cables, dry type transformers and capacitor banks.

The single constant thermal characteristic is given by the equation:

$$t = -\tau \log_e \left[\frac{I^2 - (KI_{FLC})^2}{I^2 - I_p^2} \right]$$

where:

- t = time to trip, following application of the overload current I
- τ = heating and cooling time constant of the protected plant
- I = largest phase current
- I_{FLC} full load current rating (the Thermal Trip setting)
- I_p = steady state pre-loading before application of the overload
- K = a constant, settable between 1 and 1.5, with the default value of 1.05 (***k factor***)

12.2 DUAL TIME CONSTANT CHARACTERISTIC

This characteristic is used to protect equipment such as oil-filled transformers with natural air cooling. The thermal model is similar to that with the single time constant, except that two timer constants must be set.

For marginal overloading, heat will flow from the windings into the bulk of the insulating oil. Therefore, at low current, the replica curve is dominated by the long time constant for the oil. This provides protection against a general rise in oil temperature.

For severe overloading, heat accumulates in the transformer windings, with little opportunity for dissipation into the surrounding insulating oil. Therefore at high current levels, the replica curve is dominated by the short time constant for the windings. This provides protection against hot spots developing within the transformer windings.

Overall, the dual time constant characteristic serves to protect the winding insulation from ageing and to minimise gas production by overheated oil. Note however that the thermal model does not compensate for the effects of ambient temperature change.

The dual time constant thermal characteristic is given by the equation:

$$0.4e^{(-t/\tau_1)} + 0.6e^{(-t/\tau_2)} = \left[\frac{I^2 - (KI_{FLC})^2}{I^2 - I_p^2} \right]$$

where:

- τ_1 = heating and cooling time constant of the transformer windings
- τ_2 = heating and cooling time constant of the insulating oil

12.3 THERMAL OVERLOAD PROTECTION IMPLEMENTATION

The device incorporates a current-based thermal characteristic, using RMS load current to model heating and cooling of the protected plant. The element can be set with both alarm and trip stages.

Thermal Overload Protection is implemented in the *THERMAL OVERLOAD* column of the relevant settings group.

This column contains the settings for the characteristic type, the alarm and trip thresholds and the time constants.

12.4 THERMAL OVERLOAD PROTECTION LOGIC

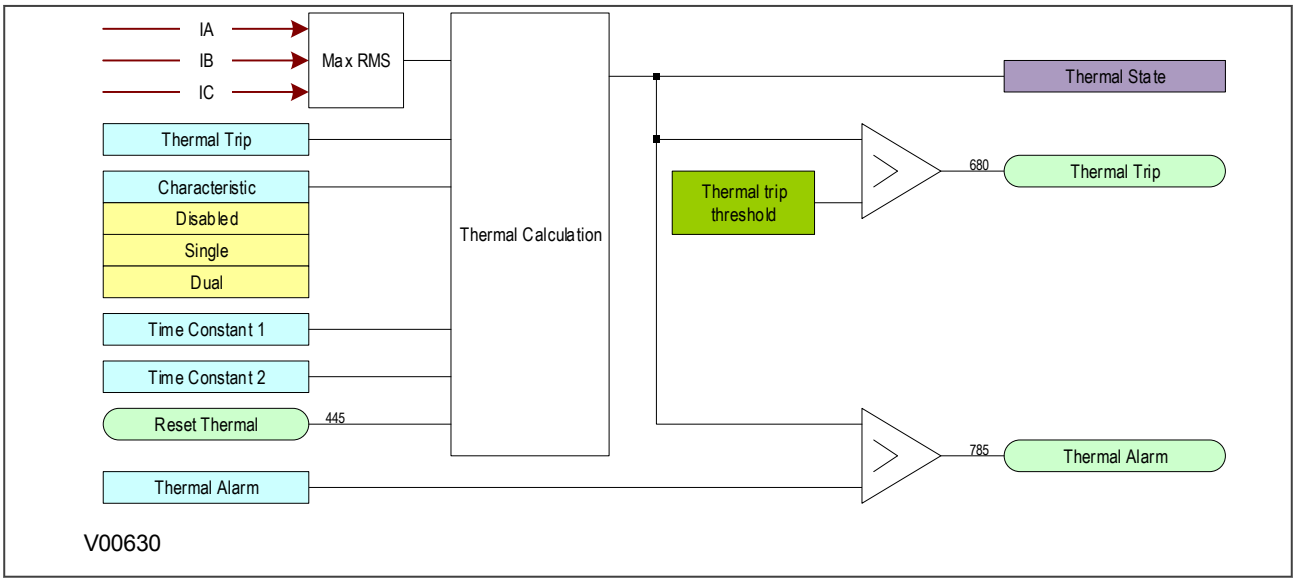


Figure 57: Thermal overload protection logic diagram

The magnitudes of the three phase input currents are compared and the largest magnitude is taken as the input to the thermal overload function. If this current exceeds the thermal trip threshold setting a start condition is asserted.

The Start signal is applied to the chosen thermal characteristic module, which has three outputs signals; alarm trip and thermal state measurement. The thermal state measurement is made available in one of the *MEASUREMENTS* columns.

The thermal state can be reset by either an opto-input (if assigned to this function using the programmable scheme logic) or the HMI panel menu.

12.5 APPLICATION NOTES

12.5.1 SETTING GUIDELINES FOR DUAL TIME CONSTANT CHARACTERISTIC

The easiest way of solving the dual time constant thermal equation is to express the current in terms of time and to use a spreadsheet to calculate the current for a series of increasing operating times using the following equation, then plotting a graph.

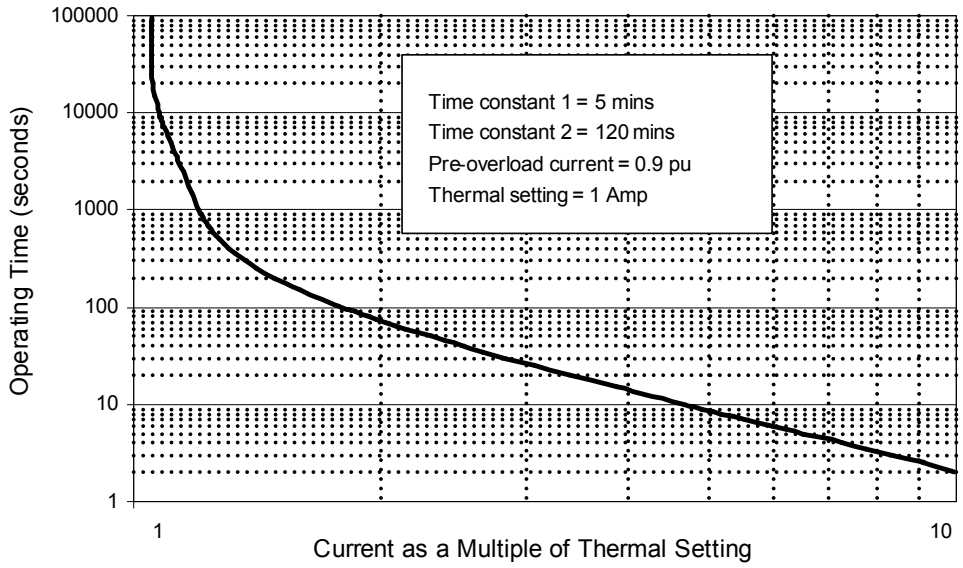
$$I = \sqrt{\frac{0.4I_p^{\,2}.e^{(-t/\tau 1)} + 0.6I_p^{\,2}.e^{(-t/\tau 2)} - k^2.I_{FLC}^{\,2}}{0.4e^{(-t/\tau 1)} + 0.6e^{(-t/\tau 2)} - 1}}$$

	A	B	C	D	E	F
1						
2	**Time constant 1 =**		**300**	seconds		
3	**Time constant 2 =**		**7200**	seconds		
4	**Pre-overload current Ip =**		**0.9**	per unit		
5	**Full load current =**		**1**	Amps		
6						
7	**OP Time (t)**	**Overload current (I)**				
8	1	14.40852032				
9	1.5	11.7805774				
10	2	10.21617905				
11	2.5	9.150045407				
12	3	8.364131776				
13	3.5	7.754150044				
14	4	7.263123888				
15	4.5	6.856949012				

Figures based on equation

E00728

Figure 58: Spreadsheet calculation for dual time constant thermal characteristic



V00629

Figure 59: Dual time constant thermal characteristic

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the transformer item/CT ratio.

For an oil-filled transformer with rating 400 to 1600 kVA, the approximate time constants are:

- τ_1 = 5 minutes
- τ_2 = 120 minutes

An alarm can be raised on reaching a thermal state corresponding to a percentage of the trip threshold. A typical setting might be "Thermal Alarm" = 70% of thermal capacity.

Note:
The thermal time constants given in the above tables are typical only. Reference should always be made to the plant manufacturer for accurate information.

12.5.2 SETTING GUIDELINES FOR SINGLE TIME CONSTANT CHARACTERISTIC

The time to trip varies depending on the load current carried before application of the overload, i.e. whether the overload was applied from hot or cold.

The thermal time constant characteristic may be rewritten as:

$$e^{(-t/\tau)} = {}_{e}\left[\frac{\theta-\theta_p}{\theta-1}\right]$$

where:

- θ = thermal state = $I^2/K^2I_{FLC}^2$
- θ_p = pre-fault thermal state = $I_p^2/K^2I_{FLC}^2$
- I_p is the pre-fault thermal state
- I_{FLC} is the full load current

Note:
A current of 105%Is (KI_{FLC}) has to be applied for several time constants to cause a thermal state measurement of 100%.

The current setting is calculated as:

Thermal Trip = Permissible continuous loading of the plant item/CT ratio.

The following tables show the approximate time constant in minutes, for different cable rated voltages with various conductor cross-sectional areas, and other plant equipment.

Area mm^2	6 - 11 kV	22 kV	33 kV	66 kV
25 – 50	10 minutes	15 minutes	40 minutes	–
70 – 120	15 minutes	25 minutes	40 minutes	60 minutes
150	25 minutes	40 minutes	40 minutes	60 minutes
185	25 minutes	40 minutes	60 minutes	60 minutes
240	40 minutes	40 minutes	60 minutes	60 minutes
300	40 minutes	60 minutes	60 minutes	90 minutes

Plant type	Time Constant (Minutes)
Dry-type transformer <400 kVA	40
Dry-type transformers 400 – 800 kVA	60 - 90
Air-core Reactors	40
Capacitor Banks	10
Overhead Lines with cross section > 100 mm^2	10
Overhead Lines	10
Busbars	60

13 BROKEN CONDUCTOR PROTECTION

One type of unbalanced fault is the 'Series' or 'Open Circuit' fault. This type of fault can arise from, among other things, broken conductors. Series faults do not cause an increase in phase current and so cannot be detected by overcurrent protection. However, they do produce an imbalance, resulting in negative phase sequence current, which can be detected.

It is possible to apply a negative phase sequence overcurrent element to detect broken conductors. However, on a lightly loaded line, the negative sequence current resulting from a series fault condition may be very close to, or less than, the full load steady state imbalance arising from CT errors and load imbalances, making it very difficult to distinguish. A regular negative sequence element would therefore not work at low load levels. To overcome this, the device incorporates a special Broken Conductor protection element.

The Broken Conductor element measures the ratio of negative to positive phase sequence current (I2/I1). This ratio is approximately constant with variations in load current, therefore making it more sensitive to series faults than standard negative sequence protection.

13.1 BROKEN CONDUCTOR PROTECTION IMPLEMENTATION

Broken Conductor protection is implemented in the *BROKEN CONDUCTOR* column of the relevant settings group.

This column contains the settings to enable the function, for the pickup threshold and the time delay.

13.2 BROKEN CONDUCTOR PROTECTION LOGIC

The ratio of I_2/I_1 is calculated and compared with the threshold setting. If the threshold is exceeded, the delay timer is initiated. The CTS block signal is used to block the operation of the delay timer.

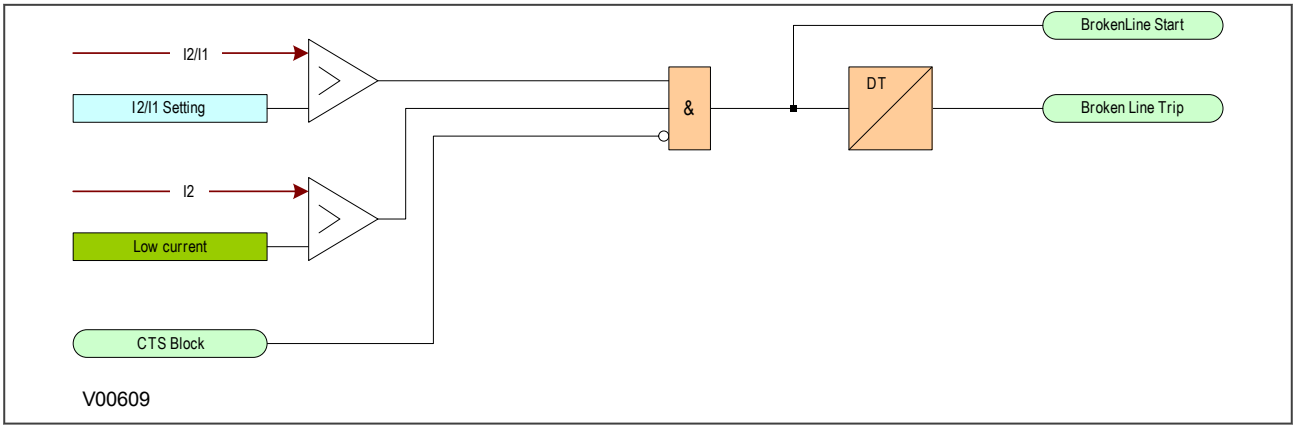


Figure 60: Broken conductor logic

13.3 APPLICATION NOTES

13.3.1 SETTING GUIDELINES

For a broken conductor affecting a single point earthed power system, there will be little zero sequence current flow and the ratio of I_2/I_1 that flows in the protected circuit will approach 100%. In the case of a multiple earthed power system (assuming equal impedance's in each sequence network), the ratio I_2/I_1 will be 50%.

In practise, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for.

Note:
A minimum value of 8% negative phase sequence current is required for successful operation.

Since sensitive settings have been employed, we can expect that the element will operate for any unbalanced condition occurring on the system (for example, during a single pole autoreclose cycle). For this reason, a long time delay is necessary to ensure co-ordination with other protection devices. A 60 second time delay setting may be typical.

The following example was recorded by an IED during commissioning:

$$I_{full\ load} = 500A$$

$$I_2 = 50A$$

therefore the quiescent I_2/I_1 ratio = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical: Therefore set:

$$I_2/I_1 = 0.2$$

In a double circuit (parallel line) application, using a 40% setting will ensure that the broken conductor protection will operate only for the circuit that is affected. A setting of 0.4 results in no pick-up for the parallel healthy circuit.

Set I_2/I_1 Time Delay = 60 s to allow adequate time for short circuit fault clearance by time delayed protections.

14 BLOCKED OVERCURRENT PROTECTION

With Blocked Overcurrent schemes, you connect the start contacts from downstream IEDs to the timer blocking inputs of upstream IEDs. This allows identical current and time settings to be used on each of the IEDs in the scheme, as the device nearest to the fault does not receive a blocking signal and so trips discriminatively. This type of scheme therefore reduces the number of required grading stages, and consequently fault clearance times.

The principle of Blocked Overcurrent protection may be extended by setting fast-acting overcurrent elements on the incoming feeders to a substation, which are then arranged to be blocked by start contacts from the devices protecting the outgoing feeders. The fast-acting element is thus allowed to trip for a fault condition on the busbar, but is stable for external feeder faults due to the blocking signal.

This type of scheme provides much reduced fault clearance times for busbar faults than would be the case with conventional time-graded overcurrent protection. The availability of multiple overcurrent and earth fault stages in the General Electric IEDs allows additional time-graded overcurrent protection for back-up purposes.

14.1 BLOCKED OVERCURRENT IMPLEMENTATION

Blocked Overcurrent schemes are implemented using the PSL. The start outputs, available from each stage of the overcurrent and earth fault elements (including the sensitive earth fault element) can be mapped to output relay contacts. These outputs can then be connected to the relevant timer block inputs of the upstream IEDs via opto-inputs.

14.2 BLOCKED OVERCURRENT LOGIC

To facilitate the implementation of blocked overcurrent schemes, the device provides the following logic to provide a Blocked Overcurrent Start signal ***I> BlockStart***:

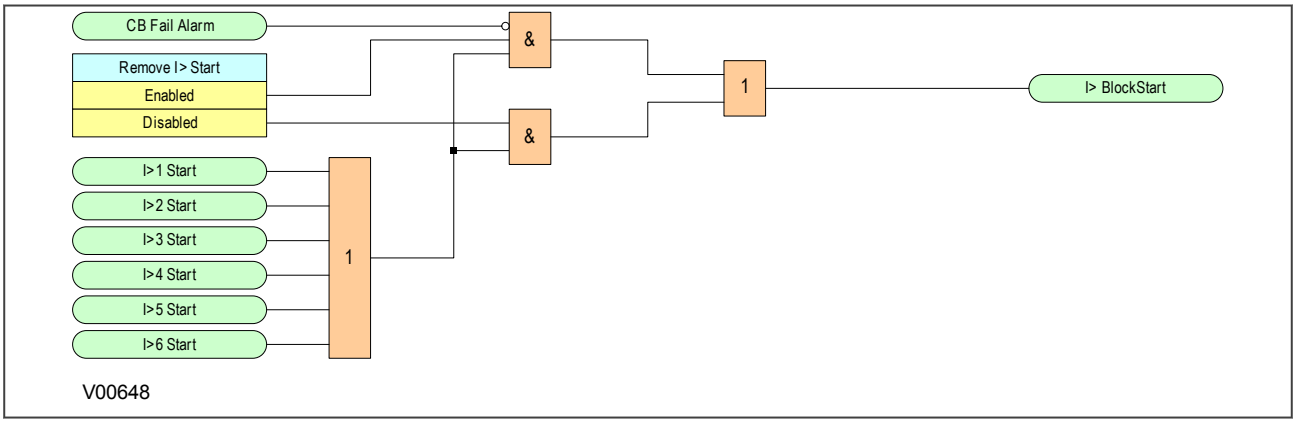


Figure 61: Blocked Overcurrent logic

The ***I> BlockStart*** signal is derived from the logical OR of the phase overcurrent start outputs. This output is then gated with the ***CB Fail Alarm*** DDB signal and the setting ***Remove I> Start*** setting.

14.3 BLOCKED EARTH FAULT LOGIC

To facilitate the implementation of blocked overcurrent schemes, the device provides the following logic to provide the Blocked Earth Fault signal ***IN/SEF>Blk Start*:**

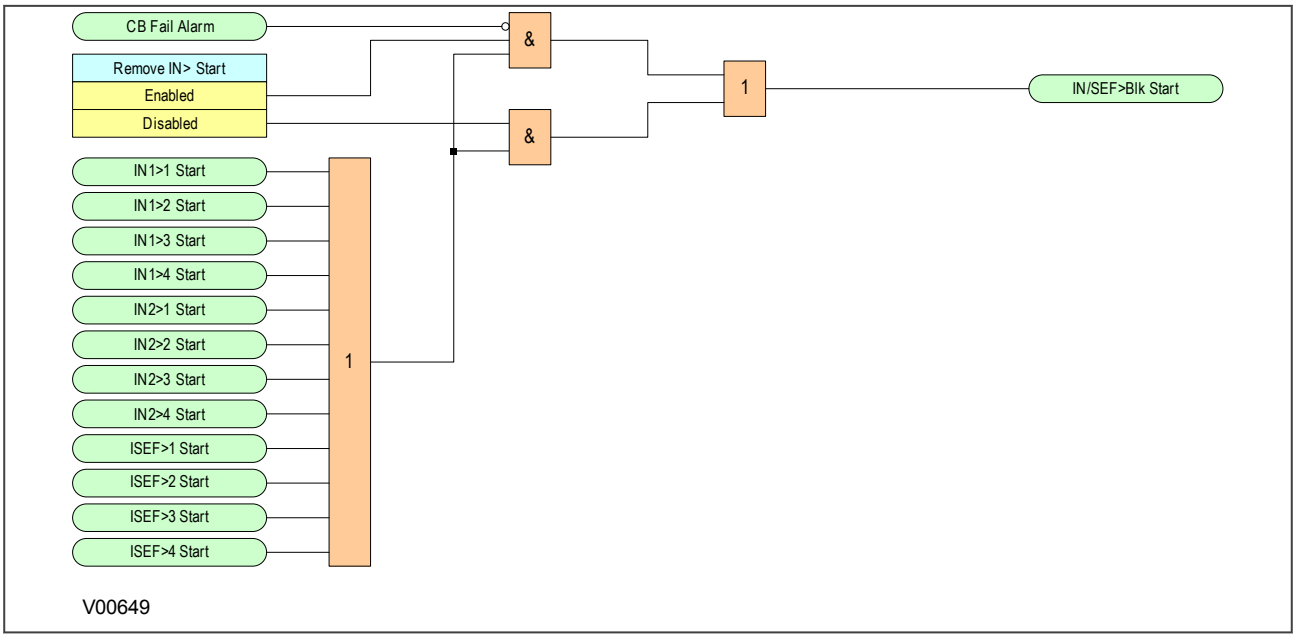


Figure 62: Blocked Earth Fault logic

The ***IN/SEF>Blk Start*** signal is derived from the logical OR of the phase overcurrent start outputs. This output is then gated with the ***CB Fail Alarm*** DDB signal and the ***Remove IN> Start*** setting.

14.4 APPLICATION NOTES

14.4.1 BUSBAR BLOCKING SCHEME

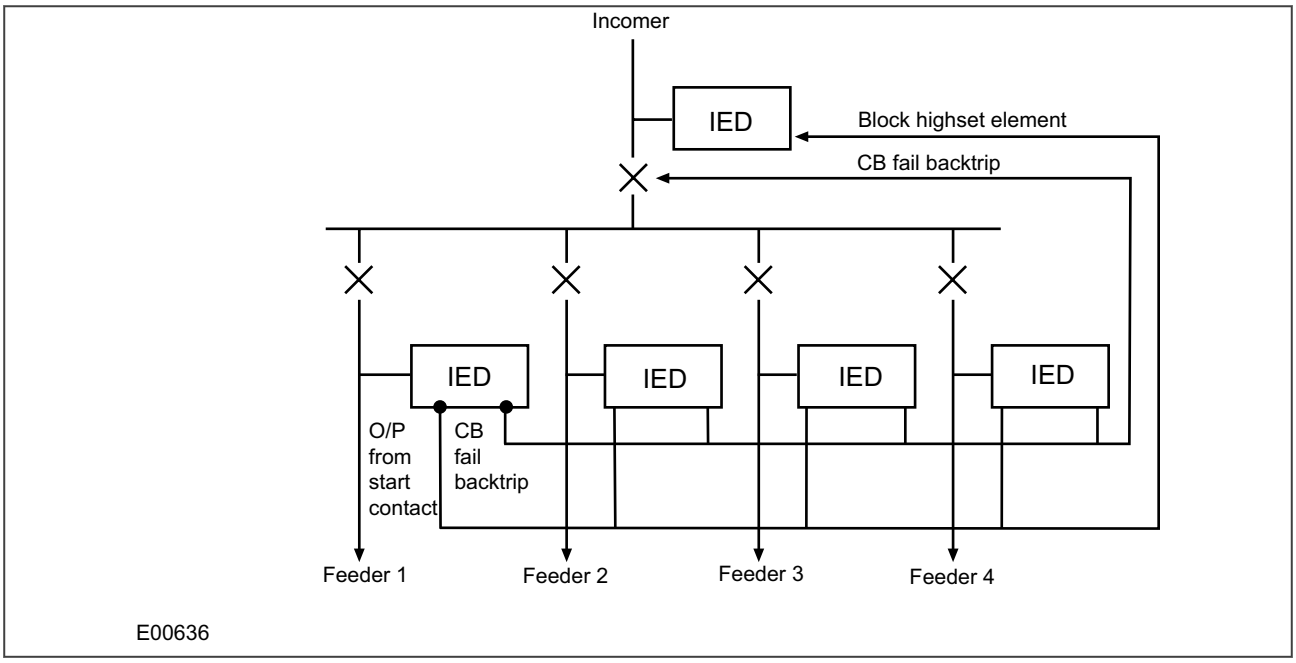


Figure 63: Simple busbar blocking scheme

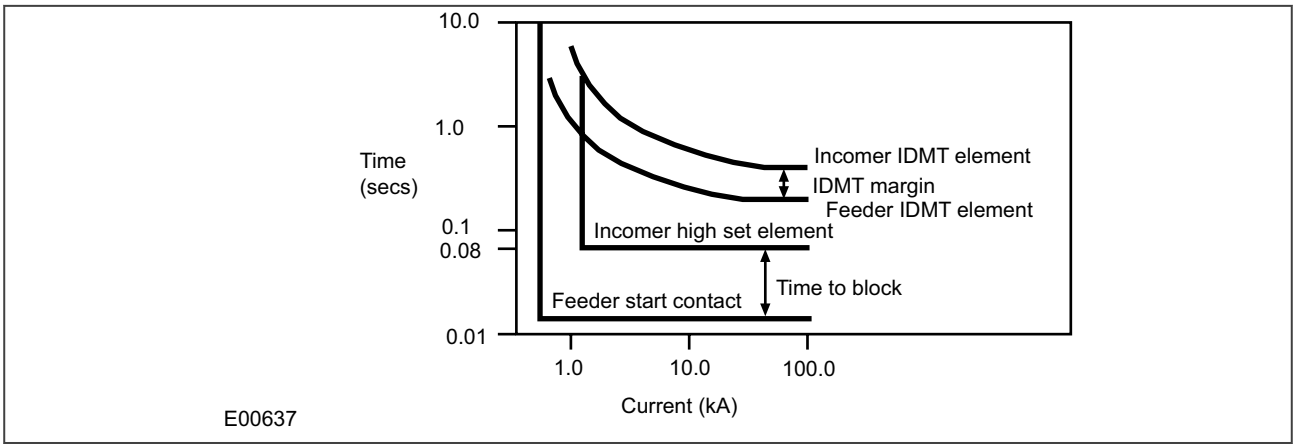


Figure 64: Simple busbar blocking scheme characteristics

For further guidance on the use of blocked busbar schemes, refer to General Electric.

15 SECOND HARMONIC BLOCKING

When a transformer is initially connected to a source of AC voltage, there may be a substantial surge of current through the primary winding called inrush current.

Inrush current is a regularly occurring phenomenon and should not be considered a fault, as we do not wish the protection device to issue a trip command whenever a transformer, or machine is switched on. This presents a problem to the protection device, because it should always trip on an internal fault. The problem is that typical internal transformer faults may produce overcurrents which are not necessarily greater than the inrush current. Furthermore faults tend to manifest themselves on switch on, due to the high inrush currents. For this reason, we need to find a mechanism that can distinguish between fault current and inrush current. Fortunately this is possible due to the different natures of the respective currents. An inrush current waveform is rich in harmonics (particularly the second), whereas an internal fault current consists only of the fundamental. We can thus develop a restraining method based on the harmonic content of the inrush current. The mechanism by which this is achieved is called second harmonic blocking.

15.1 SECOND HARMONIC BLOCKING IMPLEMENTATION

Second harmonic blocking can be applied to the following overcurrent protection types:

- Phase Overcurrent protection (POC)
- Earth Fault protection (derived and measured) (EF1 and EF2)
- Sensitive Earth Fault protection (SEF)
- Negative Phase Sequence Overcurrent protection (NPSOC)

Second harmonic blocking is implemented in the *SECURITY CONFIG* column of the relevant setting group.

Second harmonic blocking is applicable to all stages of each of the elements. Each protection element has a relevant blocking setting with which the type of blocking is defined.

For phase overcurrent, 2nd harmonic blocking can be applied to each phase individually (phase segregated), or to all three phases at once (cross-block). This is determined by the ***I> Blocking*** setting.

15.2 SECOND HARMONIC BLOCKING LOGIC (POC INPUT)

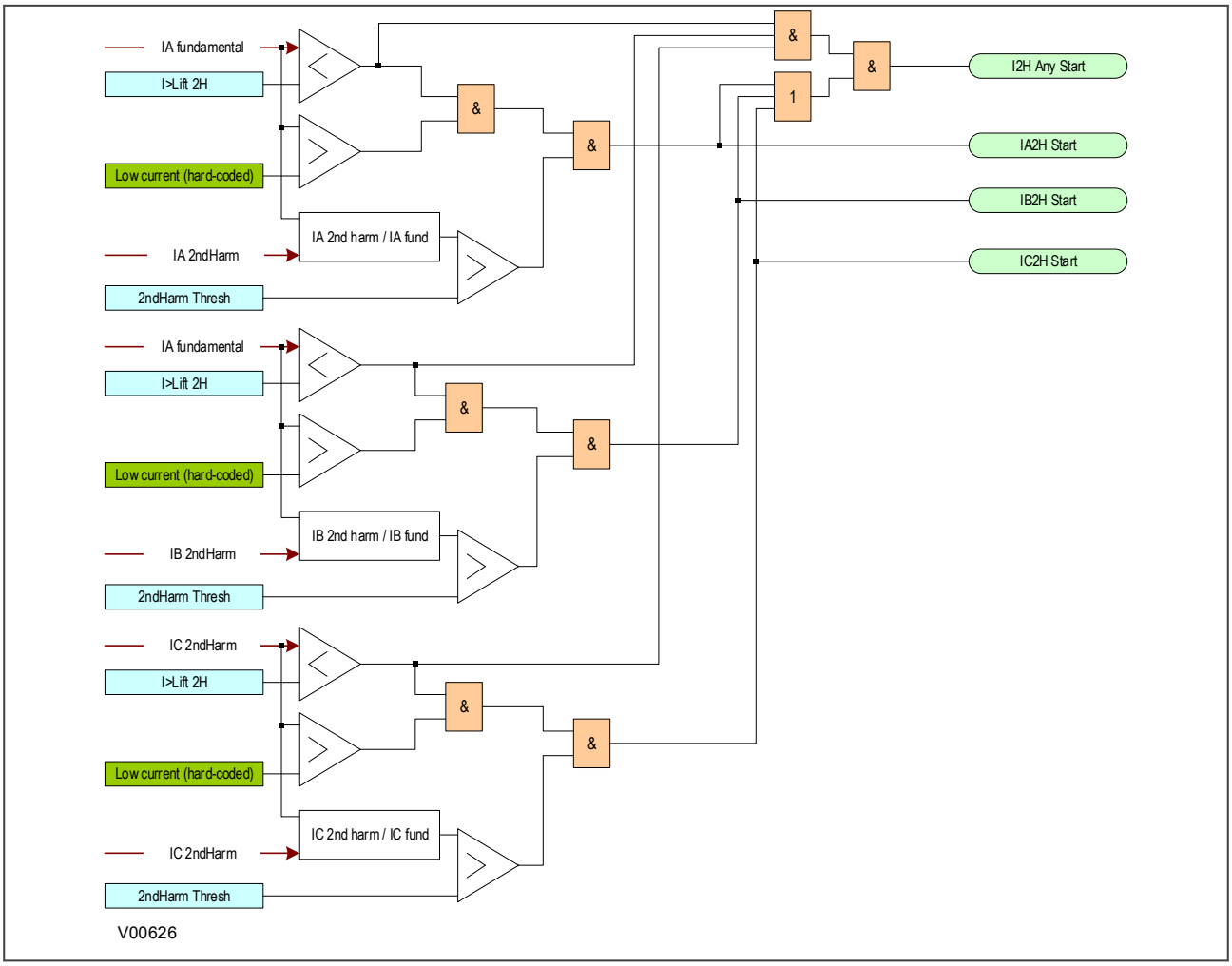


Figure 65: 2nd Harmonic Blocking Logic (POC Input)

The function works by identifying and measuring the inrush currents present in the phase currents at switch on. It does this by comparing the value of the second harmonic current components to the value of the fundamental component. If this ratio exceeds the set thresholds, then the blocking signal is generated. The threshold is defined by the ***2ndHarm Thresh*** setting.

We only want the function to block the protection if the fundamental current component is within the normal range. If this exceeds the normal range, then this is indicative of a fault, which must be protected. For this reason there is another settable trigger ***I>lift 2H***, which when exceeded, stops the 2nd harmonic blocking function.

15.3 APPLICATION NOTES

15.3.1 SETTING GUIDELINES

During the energization period, the second harmonic component of the inrush current may be as high as 70%. The second harmonic level may be different for each phase, which is why phase segregated blocking is available.

If the setting is too low, the 2nd harmonic blocking may prevent tripping during some internal transformer faults. If the setting is too high, the blocking may not operate for low levels of inrush current which could result in undesired tripping of the overcurrent element during the energization period. In general, a setting of 15% to 20% is suitable.

16 LOAD BLINDERS

Load blinding is a mechanism, where protection elements are prevented from tripping under heavy load, but healthy conditions. In the past this mechanism was mainly used for transmission systems and was rarely needed at distribution voltage levels. In the last few years, however, distribution networks have become more subject to periods of sustained heavy loads. This is due to a number of reasons, one of which is the increase of distributed generation. For this reason, it has become very desirable to equip overcurrent protection, normally targeted at distribution networks, with load blinding functionality.

Load blinders work by measuring, not only the system current levels, but also the system voltage levels and making tripping decisions based on analysis of both of these measurements. This is known as Impedance measurement.

When the measured current is higher than normal, this can be caused by one of two things; either a fault or a heavy load. If the cause is a fault, the system voltage level will reduce significantly. However, if the cause is a heavy, but healthy load, the voltage will not decrease significantly. Therefore, by measuring the both the system voltage and currents, the protection can make a decision not to trip under heavy load conditions.

The principle of a load blinder is to configure a blinder envelope, which surrounds the expected worst case load limits, and to block tripping for any impedance measured within this blinder region. Only fault impedance outside the load area is allowed to cause a trip. It is possible to set the impedance and angle setting independently for the forward and reverse regions in the Z plane.

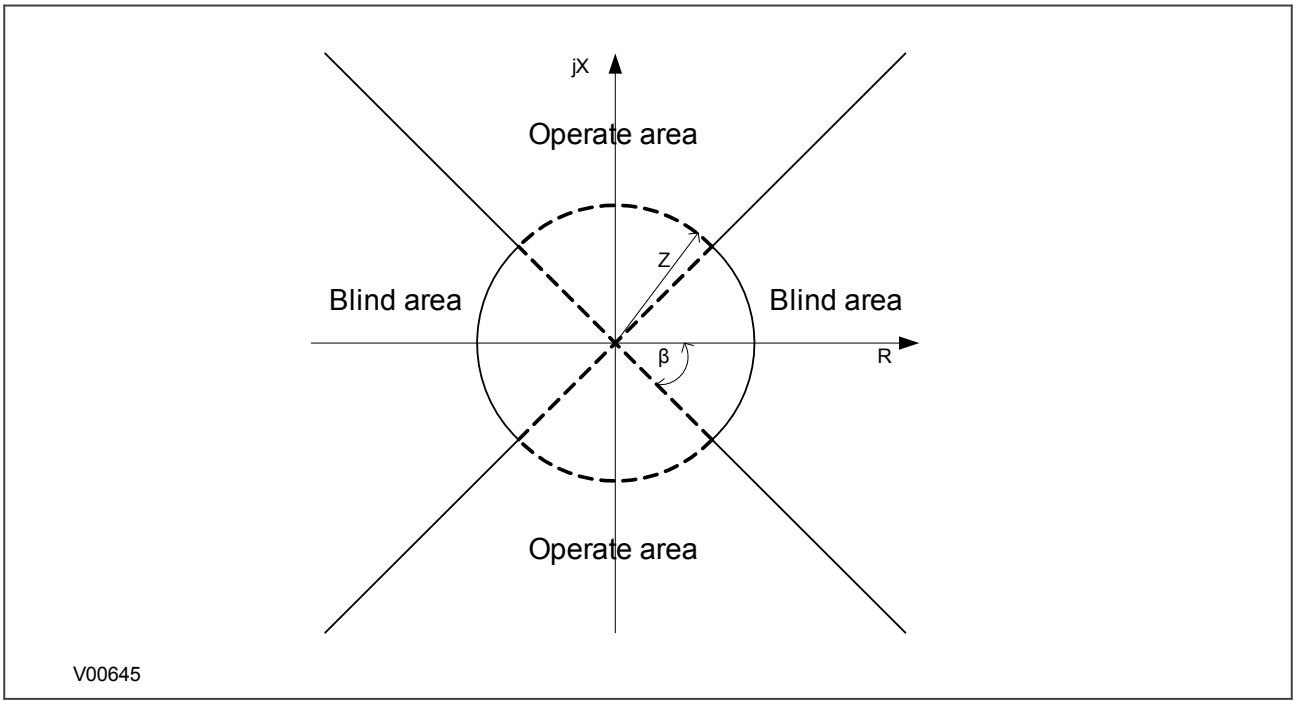


Figure 66: Load blinder and angle

16.1 LOAD BLINDER IMPLEMENTATION

The Load blinder function is implemented in the *OVERCURRENT* column of the relevant settings group, under the sub-heading *LOAD BLINDER*.

The settings allow you to set the impedance and angle limits for both reverse and forward directions, the undervoltage and negative sequence current thresholds for blocking the function, and the operation mode.

There are two modes of operation; single phase and three phase;

The single phase mode uses the normal impedance (Z) of each phase. When single phase mode is selected, the overcurrent blocking is phase segregated and is dependant on the individual overcurrent settings per phase. In single phase mode, only the undervoltage threshold (***Blinder V< Block***) can block the function.

The three phase mode uses positive sequence impedance (Z1). The three phase mode uses both the negative sequence overcurrent threshold (***Blinder I2>Block***) and the undervoltage threshold (***Blinder V< Block***) to block the function.

16.2 LOAD BLINDER LOGIC

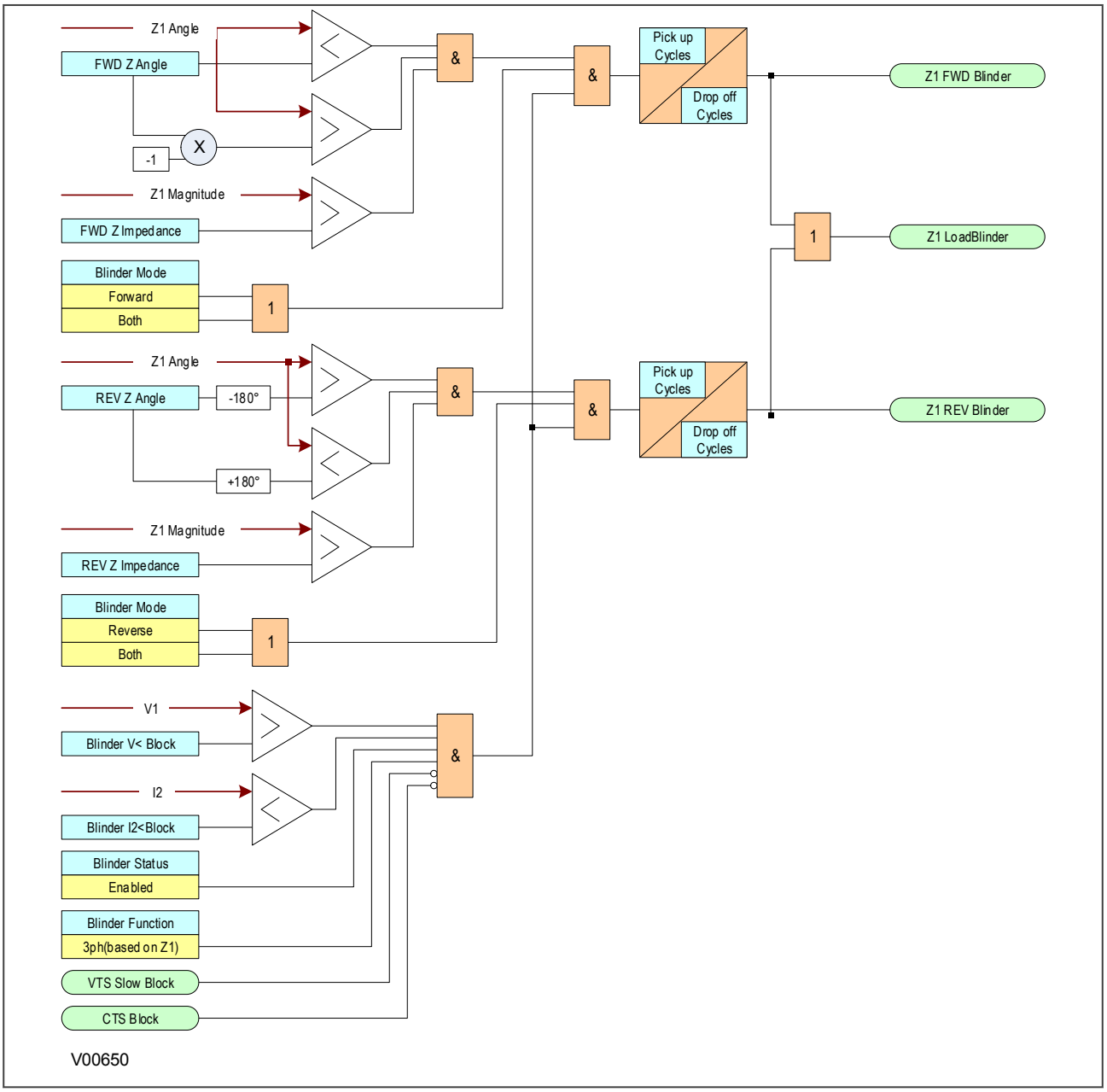


Figure 67: Load Blinder logic 3phase

For the forward direction, the positive sequence impedance magnitude is compared with a set value, and the positive sequence impedance angle is compared with two values, which define the angular range. If the criteria are satisfied and the Blinder mode is in the direction Forward or Both, the blinder signals ***Z1 FWD Blinder*** and ***Z1 LoadBlinder*** are produced.

For the reverse direction, the positive sequence impedance magnitude is compared with a set value, and the positive sequence impedance angle is compared with two values, which define the angular range. If the criteria are satisfied and the Blinder mode is in the direction Forward or Both, the blinder signals ***Z1 REV Blinder*** and ***Z1 LoadBlinder*** are produced.

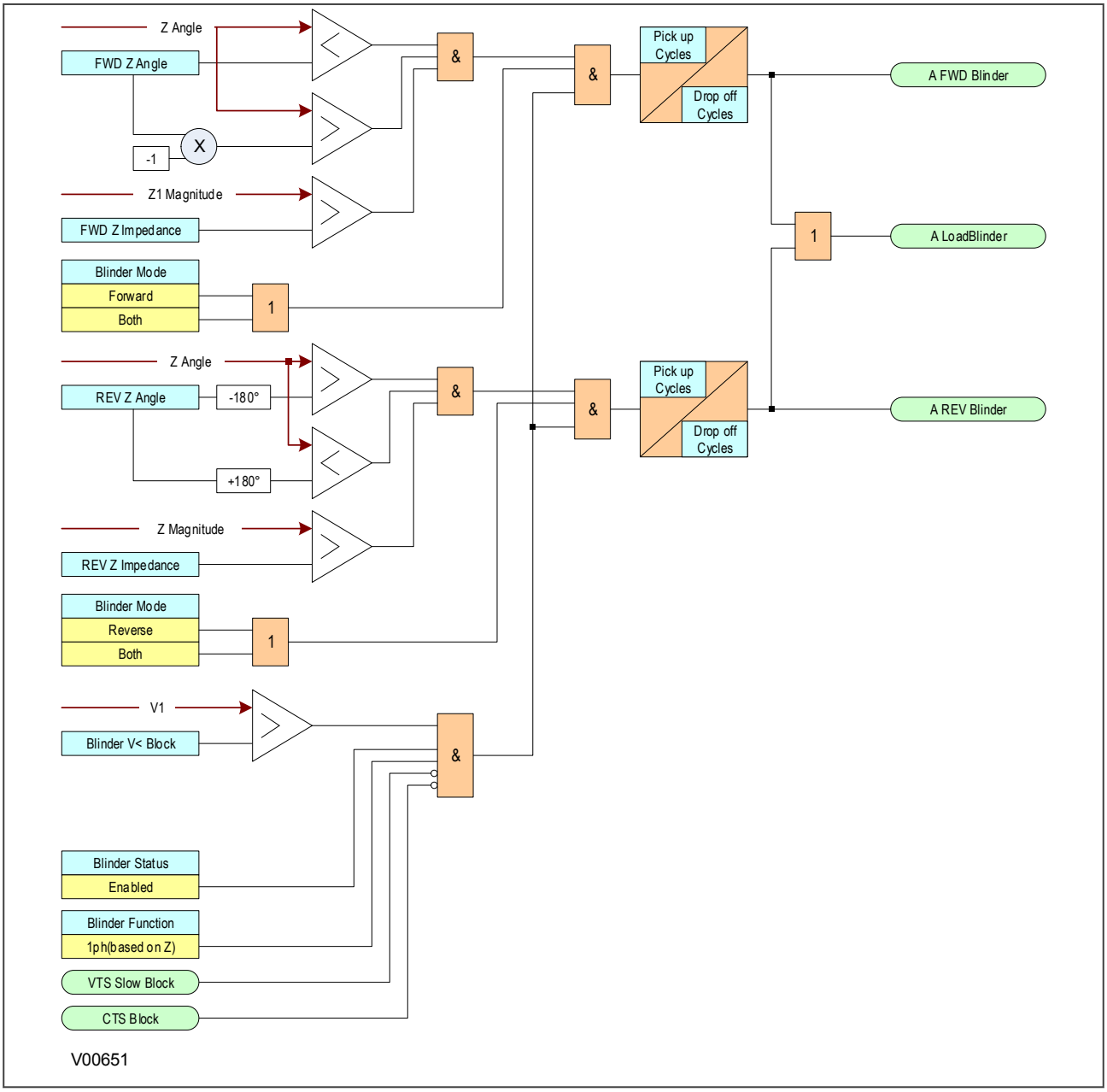


Figure 68: Load Blinder logic phase A

The diagram shows the single-phase Load Blinder logic for phase A. The same principle applies to phases B and C. The single phase Load Blinder logic is very similar to the three-phase Load Blinder logic. The main differences are:

The single-phase function does not use positive sequence impedance, it uses normal impedance measurment. It also does not use negative sequence overcurrent to block the function.

17 NEUTRAL ADMITTANCE PROTECTION

Neutral admittance protection works by calculating the neutral admittance from the neutral input current and voltage (I_N/V_N). The neutral current input is measured with an earth fault or sensitive earth fault current transformer and the neutral voltage is based on the internally derived quantity VN.

Three single stage elements are provided:

- Overadmittance YN>: This is non-directional, providing both start and time delayed trip outputs. The trip may be blocked by a logic input
- Overconductance GN>: This is non-directional or directional, providing both start and time delayed trip outputs. The trip may be blocked by a logic input
- Oversusceptance BN>: This is is non-directional or directional, providing both start and time delayed trip outputs. The trip may be blocked by a logic input

The overadmittance elements YN>, GN> and BN> will operate providing the neutral voltage remains above the set level for the set operating time of the element. They are blocked by operation of the fast VTS block signal from the VT supervision function.

The overadmittance elements provide measurements of admittance, conductance and susceptance that also appear in the fault record.

The overadmittance elements are capable of initiating auto-reclose by means of YN>, GN> and BN> settings in the AUTO-RECLOSE menu column.

17.1 NEUTRAL ADMITTANCE OPERATION

The admittance protection is non-directional. Hence, provided the magnitude of admittance exceeds the set value ***YN>*** Set and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate.

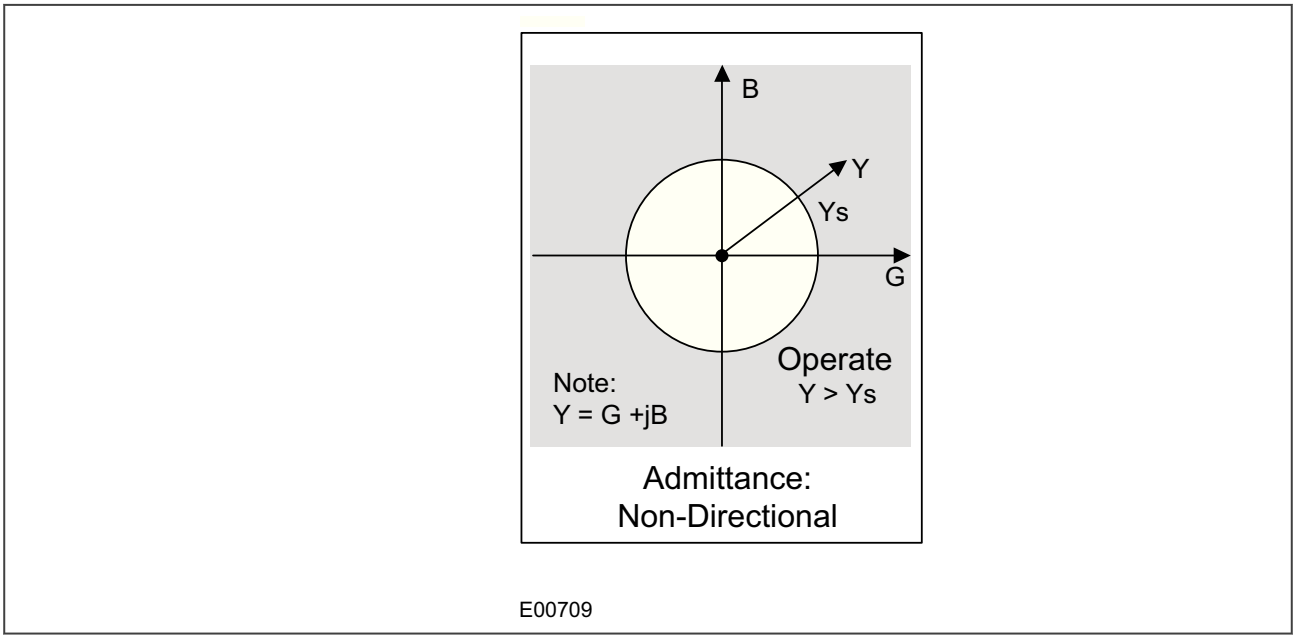


Figure 69: Admittance protection

17.2 CONDUCTANCE OPERATION

The conductance protection may be set non-directional, directional forward or directional reverse. Hence, provided the magnitude and the directional criteria are met for conductance and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate. The correction angle causes rotation of the directional boundary for conductance through the set correction angle.

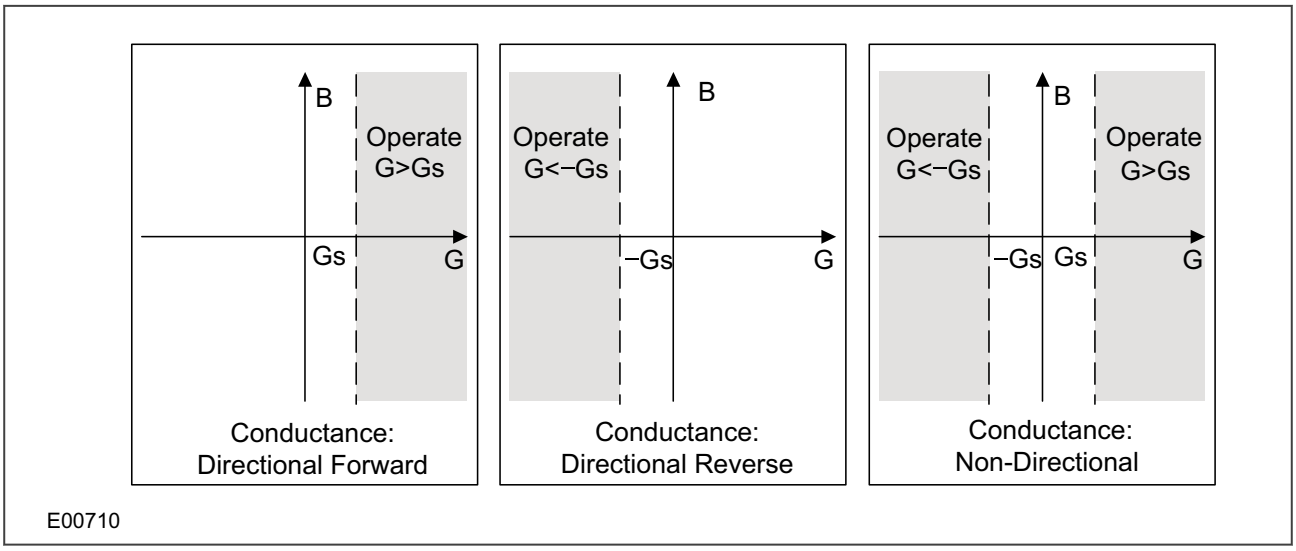


Figure 70: Conductance operation

Note:
For forward operation, the centre of characteristic occurs when IN is in phase with VN.

Note:
If the correction angle is set to +30°, this rotates the boundary from 90° - 270° to 60° - 240°. It is assumed that the direction of the G axis indicates 0°.

17.3 SUSCEPTANCE OPERATION

The susceptance protection may be set non-directional, directional forward or directional reverse. Hence, provided the magnitude and the directional criteria are met for susceptance and the magnitude of neutral voltage exceeds the set value VN Threshold, the relay will operate. The correction angle causes rotation of the directional boundary for susceptance through the set correction angle.

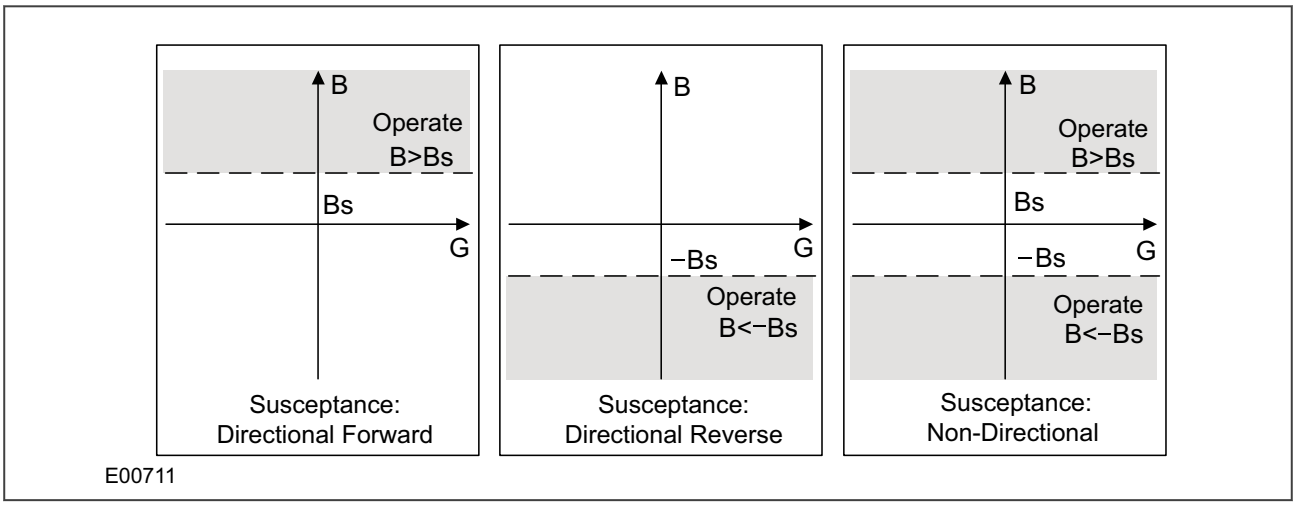


Figure 71: Susceptance operation

Note:
For forward operation, the centre of characteristic occurs when IN ieads VN by 90°.

Note:
If the correction angle is set to +30°, this rotates the boundary from 0° - 180° to 330° - 150°. It is assumed that the direction of the G axis indicates 0°.

18 HIGH IMPEDANCE FAULT DETECTION

A High Impedance Fault, also known as a *Downed Conductor*, happens when a primary conductor makes unwanted electrical contact with a road surface, pathway, tree etc., whereby due to the high impedance of the fault path, the fault current is restricted to a level below that which can be reliably detected by standard overcurrent devices. Even in cases where the instantaneous fault current may exceed the thresholds, the duration of this transient is usually so small that the standard overcurrent IED will not pick up. It is quite a challenging problem to detect such faults, and it requires a special method combining multiple techniques.

Due to the high impedance and transient nature of such faults it is not possible to derive the fault calculation from short-circuit computing. HIF detection therefore relies on the detection of the fault current and voltage waveform signatures. These waveforms may be very different from fault to fault, but they often have commonalities typified by:

- Third harmonic content
- The transient bursting (intermittent change of amplitude)

We can use these phenomena to detect the fault.

We may need to establish the direction of the fault. For this, we can use instantaneous power measurement. Hence we can see there are three components necessary to provide a reliable HIF detection function:

- Component harmonic Analysis (CHA)
- Fundamental Analysis (FA) (with or without directional analysis (DIR)

18.1 HIGH IMPEDANCE FAULT PROTECTION IMPLEMENTATION

18.1.1 FUNDAMENTAL ANALYSIS

Fundamental Analysis (FA) captures the intermittent characteristics associated with a fault current. Generally, the system current is fairly stable and it tracks the load conditions. An average of this current is calculated by continually averaging the latest samples, and this value is stored in a buffer. This value is being continually compared with latest current value. If there is a sudden increase in current, its value will significantly exceed the average value. It is this increment that is used to start the fault evaluation process.

The averaged current load tracks system load conditions using an averaging process. A discrepancy between the actual amplitude and the average amplitude starts the fault evaluation process. If the increment is greater than a start threshold, determined by the setting ***FA> Start Thresh***, the FA will start fault evaluation. A Burst Valid (BV) threshold, determined by the setting **FA> Burst *Thresh***, is used to judge whether the increment indicates conduction of fault current. By counting the changes of the BV states within a time window, an event is issued and it is possible to establish whether an intermittent fault has been detected.

FA detection can be triggered by any sudden increase of the amplitude. However, only those sustained series of changes within a specified time-window can be evaluated as a High Impedance Fault (HIF). Fault classification criteria can be determined using timing and counting of these bursts. The following table shows the classification criteria.

Counter Status	Timer Status	Result
BV state changes exceed count limit	Within time window of one FA section	HIF
BV stage changes do not exceed count limit, but are more than two	Within time window of one FA section	Transient Event
Less than two changes	While fundamental amplitude remains above BV threshold within time window	Steady Event
Others		Noises

18.1.2 COMPONENT HARMONIC ANALYSIS

The Component Harmonic Analysis (CHA) function monitors the measured SEF current, compares this with the average current value and uses the increment of the sampled value to extract the 3rd harmonic component. By evaluating the phase and amplitude differences between the fundamental and the third harmonic, it is possible to establish criteria, which can help determine the presence of a High Impedance Fault.

Note:
CHA is ONLY applicable in directly grounded or lower to medium resistance grounded systems.

An array of increment samples is obtained and used to calculate the fault characteristic. A so called Satisfied State (SS) is a value that meets the criteria to indicate HIF non-linearity. Fault evaluation and classification are mainly based on measuring the duration of the Satisfied State. The fault evaluation process can be triggered internally or externally.

The criteria determining non-linearities characteristic of high impedance faults consists of the following:

- The fundamental amplitude is above a set threshold (setting ***CHA> Fund Thresh***)
- The phase difference between 3rd harmonic and fundamental is within a range around 180° (settings ***CHA Del Ang180-x*** and ***CHA Del Ang180+x***)
- The amplitude ratio between 3rd harmonic and fundamental is above a set threshold (setting ***CHA>3rdHarmThrsh***) and not above 90% of the fundamental.
- The above requirements last for a significant time duration.

The CHA function detects a fault by timing the duration of the Satisfied State (SS). If this time duration is longer than the HIF Setting time, a HIF event is reported. If the time duration is shorter, but still longer than a Transient Setting time, a Transient event is reported.

Harmonic State	SS Timer Status	Result
Persisting Satisfied State	Lasts for HIF duration setting (CHA tDuration)	HIF established
Intermittent Satisfied State	Lasts for transient setting time (CHA tTransient)	Transient Event established
Others		Noises

Similar to Fundamental Analysis, a Transient Event needs further confirmation. Three individual timers are activated once the CHA function starts.

- A reset timer is used to reset all the procedures of CHA.
- A HIF duration timer is used to measure the duration of this Satisfied State to issue HIF.
- A Transient timer is used to detect any transient event:

If the Satisfied State lasts for the entire time duration set by the HIF timer, an HIF is reported and all procedures are reset.

If the Satisfied State lasts for less then the HIF duration but is still more than the Transient time duration, a Transient Suspicion event is reported and the detection process will evaluate another section. If any HIF requirement is satisfied within the reset time, a HIF is reported and the detection is reset.

If there are more than three Transient Suspicion events reported within the reset time, a HIF is reported.

18.1.3 DIRECTIONAL ANALYSIS

The described FA algorithm has no capability of detecting direction. It can be used in a system with limited capacitance, or a system with directly grounded neutral point. In these cases, the fault current on healthy lines are limited. However, when a system is resistance-grounded with a relatively large distributed capacitance, the fault-generated transient may be distributed along both healthy and faulted lines due to the large distributed capacitance. Therefore, a directional element is needed to enhance the FA performance.

Transient directionality is obtained by using the instantaneous power direction of the fault component. The instantaneous power is calculated directly from the samples of the fault component. In Transient situations, this is a more accurate method than using phasor based power calculations .

The fault component circuit is used for analysis. The source is the fault itself. The capacitive branch produces the reactive power while the inductance branch absorbs the reactive power. The resistance branch absorbs the active power. The active power is from the source. The reactive power from the source balances the total consumption of the reactive power by the other part of the circuit.

	Resistor in Neutral		Petersen Coil in Neutral		Isolated	
	Faulty Line	Healthy Line	Faulty Line	Healthy Line	Faulty Line	Healthy Line
P	Rev	Fwd	Rev	Fwd	Rev	Fwd
Q	Fwd	Rev	-	-	Fwd	Rev

Generally, the reactive power is more distinctive, since the distributed capacitance is often greater than the distributed conductance. Therefore, in resistance-grounded or isolated systems, the reactive power direction is used for transient direction detection.

In Petersen coil grounded systems, the active power direction is used to detect the direction because the Petersen coil distorts the reactive power flow.

The output of the direction detection function (DIR) are flags indicating the fault direction: ***FA DIR Forward*** and ***FA DIR Reverse***.

These flags are set if the algorithm is in the Start stage and the criteria have been met. The FA function uses the flag status to determine whether it is a forward fault or a reverse fault. An alarm can also be set to indicate the faulted line. When counting a spike into the FA function's counter, the FA first refers to the direction flag. Only spikes with forward direction (Forward transient) are counted for fault evaluation.

18.1.4 SUMMARY

The type of High Impedance Fault detection solution should be selected according to the different system grounding conditions. The solution consists of two major algorithms and a facility algorithm that forms a matrix to cover these different conditions.

CHA detects situations where there is a continuous earth fault harmonic. CHA should only be used for directly grounded or low resistance grounded system.

FA detects intermittent faults where the fault current is changing between conducting and non-conducting. This can be used in any system grounding conditions. However, a continuous fault will only be detected as a steady event. The solution matrix is as follows:

	Solid	Resistor	Petersen Coil	Isolated
FA+DIR(Active P)	Applicable	Applicable	Recommended	Applicable
FA+DIR(Reactive Q)	Applicable	Recommended	Not applicable	Recommended
FA (non DIR)	Recommended	Not applicable	Not applicable	Not applicable
CHA	Recommended	Recommended	Not applicable	Not applicable
Recommended Solution	CHA+FA	CHA+FA+DIR(Q)	FA+DIR(P)	FA+DIR(Q)

18.2 HIGH IMPEDANCE FAULT PROTECTION LOGIC

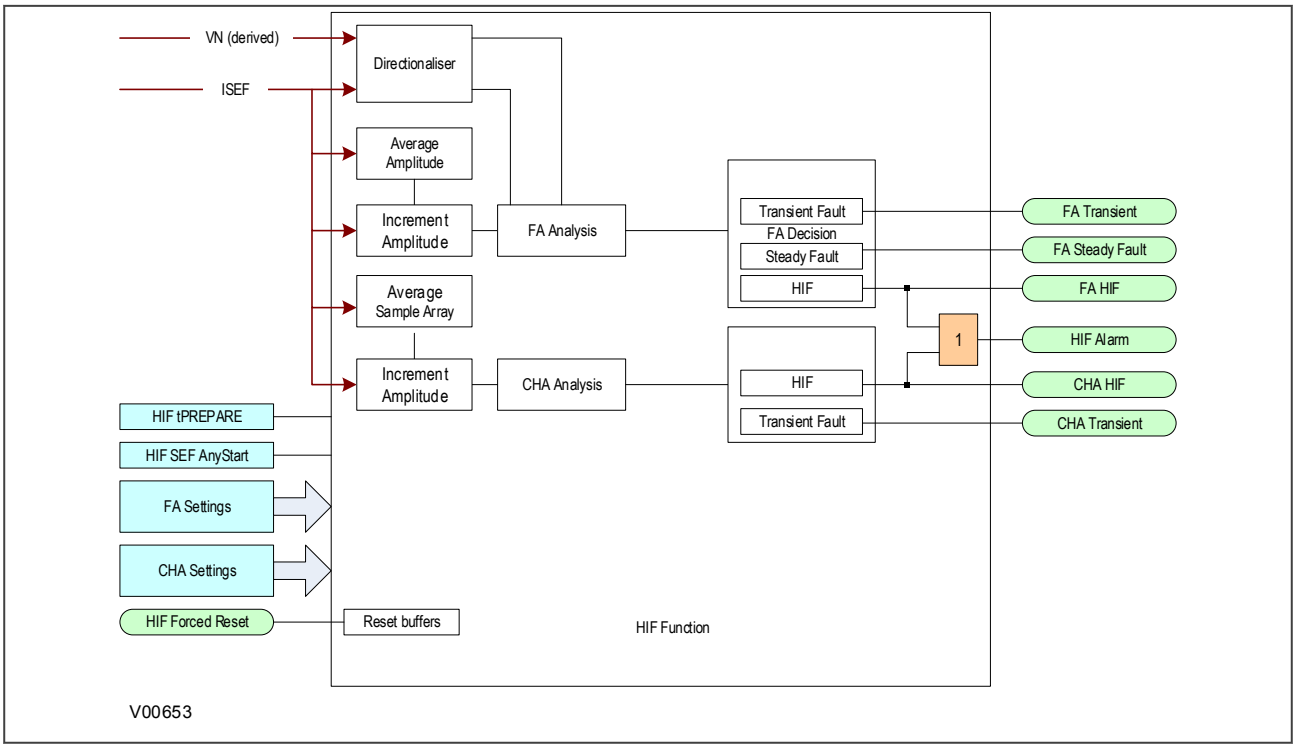


Figure 72: HIF Protection Logic

CHAPTER 7

RESTRICTED EARTH FAULT PROTECTION

1 CHAPTER OVERVIEW

The device provides extensive Restricted Earth Fault functionality. This chapter describes the operation of this function including the principles of operation, logic diagrams and applications.

This chapter contains the following sections:

2 REF PROTECTION PRINCIPLES

Winding-to-core faults in a transformer can be caused by insulation breakdown. Such faults can have very low fault currents, but they still need to be picked up. If such faults are not identified, this could result in extreme damage to very expensive equipment.

Often the associated fault currents are lower than the nominal load current. Neither overcurrent nor percentage differential protection is sufficiently sensitive in this case. We therefore require a different type of protection arrangement. Not only should the protection arrangement be sensitive, but it must create a protection zone, which is limited to each transformer winding. Restricted Earth Fault protection (REF) is the protection mechanism used to protect individual transformer winding sets.

The following figure shows a REF protection arrangement for protecting the delta side of a delta-star transformer.

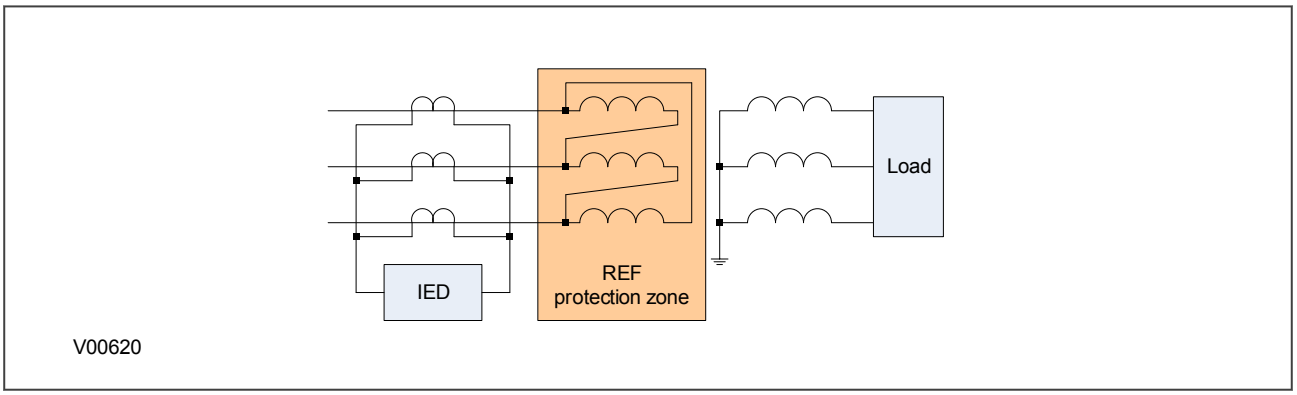


Figure 73: REF protection for delta side

The current transformers measuring the currents in each phase are connected in parallel. The currents from all three phases are summed to form a differential current, sometimes known as a spill current. Under normal operating conditions the currents of the three phases add up to zero resulting in zero spill current. A fault on the star side will also not result in a spill current, as the fault current would simply circulate in the delta windings. However, if any of the three delta windings were to develop a fault, the impedance of the faulty winding would change and that would result in a mismatch between the phase currents, resulting in a spill current. If the spill current is large enough, it will trigger a trip command.

The following figure shows a REF protection arrangement for the star side of a delta-star transformer.

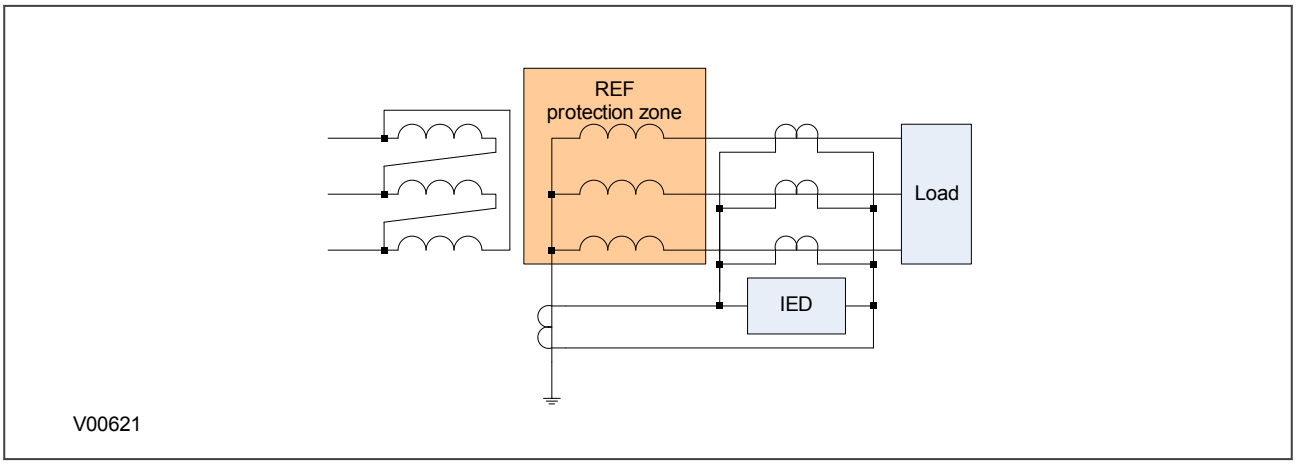


Figure 74: REF protection for star side

Here we have a similar arrangement of current transformers connected in parallel. The difference is that we need to measure the zero sequence current in the neutral line as well. An external unbalanced fault causes zero sequence current to flow through the neutral line, resulting in uneven currents in the phases, which could cause

the protection to maloperate. By measuring this zero sequence current and placing it in parallel with the other three, the currents are balanced, resulting in stable operation. Now only a fault inside the star winding can create an imbalance sufficient to cause a trip.

2.1 RESISTANCE-EARTHED STAR WINDINGS

Most distribution systems use resistance-earthed systems to limit the fault current. Consider the diagram below, which depicts an earth fault on the star winding of a resistance-earthed Dyn transformer (Dyn = Delta-Star with star-point neutral connection).

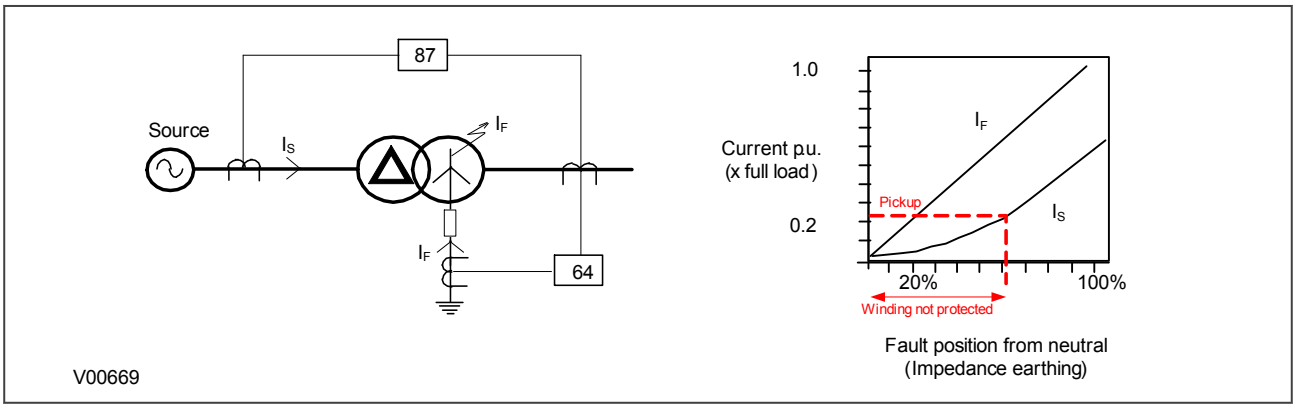


Figure 75: REF Protection for resistance-earthed systems

The value of fault current (I_F) depends on two factors:

- The value of earthing resistance (which makes the fault path impedance negligible)
- The fault point voltage (which is governed by the fault location).

Because the fault current (I_F) is governed by the resistance, its value is directly proportional to the location of the fault.

A restricted earth fault element is connected to measure I_F directly. This provides very sensitive earth fault protection. The overall differential protection is less sensitive, since it only measures the HV current I_S. The value of I_S is limited by the number of faulty secondary turns in relation to the HV turns.

2.2 SOLIDLY-EARTHED STAR WINDINGS

Most transmission systems use solidly-earthed systems. Consider the diagram below, which depicts an earth fault on the star winding of a solidly-earthed Dyn transformer.

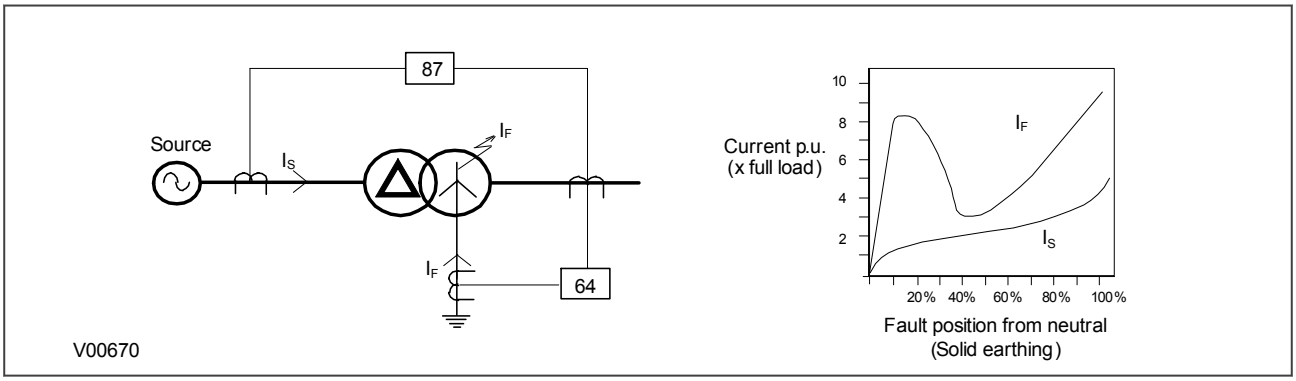


Figure 76: REF Protection for solidly earthed system

In this case, the fault current I_F is dependent on:

- The leakage reactance of the winding
- The impedance in the fault path
- The fault point voltage (which is governed by the fault location)

In this case, the value of fault current (I_F) varies with the fault location in a complex manner.

A restricted earth fault element is connected to measure I_F directly. This provides very sensitive earth fault protection.

For solidly earthed systems, the operating current for the transformer differential protection is still significant for faults over most of the winding. For this reason, independent REF protection may not have been previously considered, especially where an additional device would have been needed. But with this product, it can be applied without extra cost.

2.3 THROUGH FAULT STABILITY

In an ideal world, the CTs either side of a differentially protected system would be identical with identical characteristics to avoid creating a differential current. However, in reality CTs can never be identical, therefore a certain amount of differential current is inevitable. As the through-fault current in the primary increases, the discrepancies introduced by imperfectly matched CTs is magnified, causing the differential current to build up. Eventually, the value of the differential current reaches the pickup current threshold, causing the protection element to trip. In such cases, the differential scheme is said to have lost stability. To specify a differential scheme's ability to restrain from tripping on external faults, we define a parameter called 'through-fault stability limit', which is the maximum through-fault current a system can handle without losing stability.

2.4 RESTRICTED EARTH FAULT TYPES

There are two different types of Restricted Earth Fault; Low Impedance REF (also known as Biased REF) and High Impedance REF. Each method compensates for the effect of through-fault errors in a different manner.

With Low Impedance REF, the through-fault current is measured and this is used to alter the sensitivity of the REF element accordingly by applying a bias characteristic. So the higher the through fault current, the higher the differential current must be for the device to issue a trip signal, Often a transient bias component is added to improve stability during external faults.

Low impedance protection used to be considered less secure than high impedance protection. This is no longer true as numerical IEDs apply sophisticated algorithms to match the performance of high-impedance schemes. Some advantages of using Low Impedance REF are listed below:

- There is no need for dedicated CTs. As a result CT cost is substantially reduced.
- The wiring is simpler as it does not require an external resistor or Metrosil.
- Common phase current inputs can be used.
- It provides internal CT ratio mismatch compensation. It can match CT ratios up to 1:40 resulting flexibility in substation design and reduced cost.
- Advanced algorithms make the protection secure.

With High Impedance REF, there is no bias characteristic, and the trip threshold is set to a constant level. However, the High Impedance differential technique ensures that the impedance of the circuit is sufficiently high such that the differential voltage under external fault conditions is lower than the voltage needed to drive differential current through the device. This ensures stability against external fault conditions so the device will operate only for faults occurring inside the protected zone.

High Impedance REF protection responds to a voltage across the differential junction points. During external faults, even with severe saturation of some of the CTs, the voltage does not rise above certain level, because the other

CTs will provide a lower-impedance path compared with the device input impedance. The principle has been used for more than half a century. Some advantages of using High Impedance REF are listed below:

- It provides a simple proven algorithm, which is fast, robust and secure.
- It is less sensitive to CT saturation.

2.4.1 LOW IMPEDANCE REF PRINCIPLE

Low Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED is as follows:

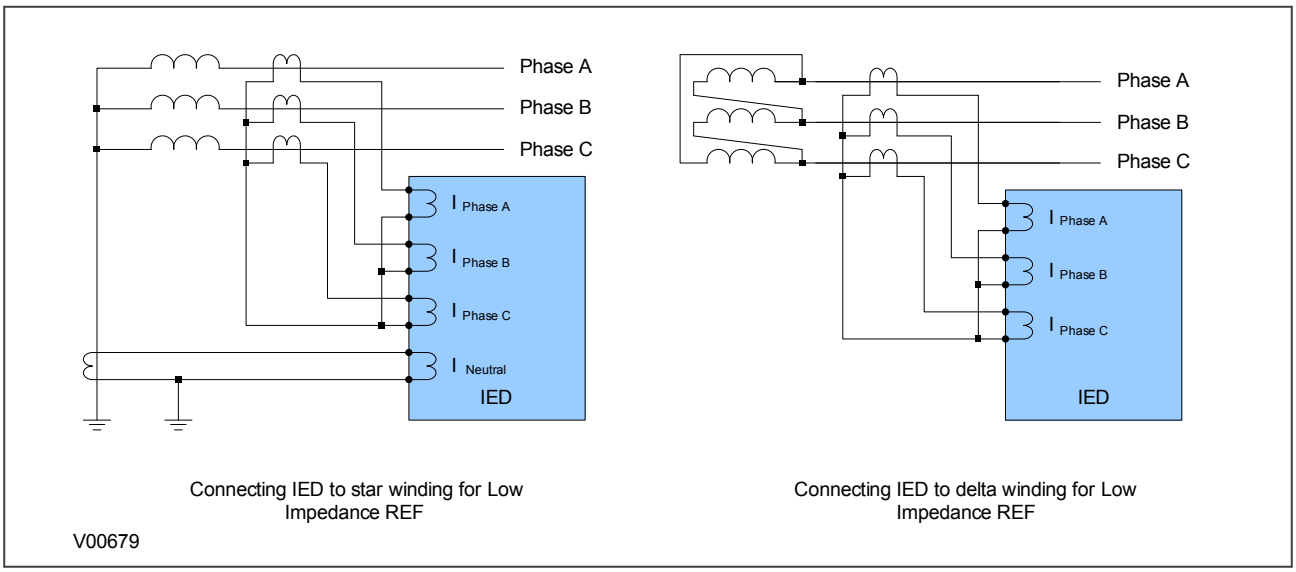


Figure 77: Low Impedance REF Connection

2.4.1.1 LOW IMPEDANCE BIAS CHARACTERISTIC

Usually, a triple slope biased characteristic is used as follows:

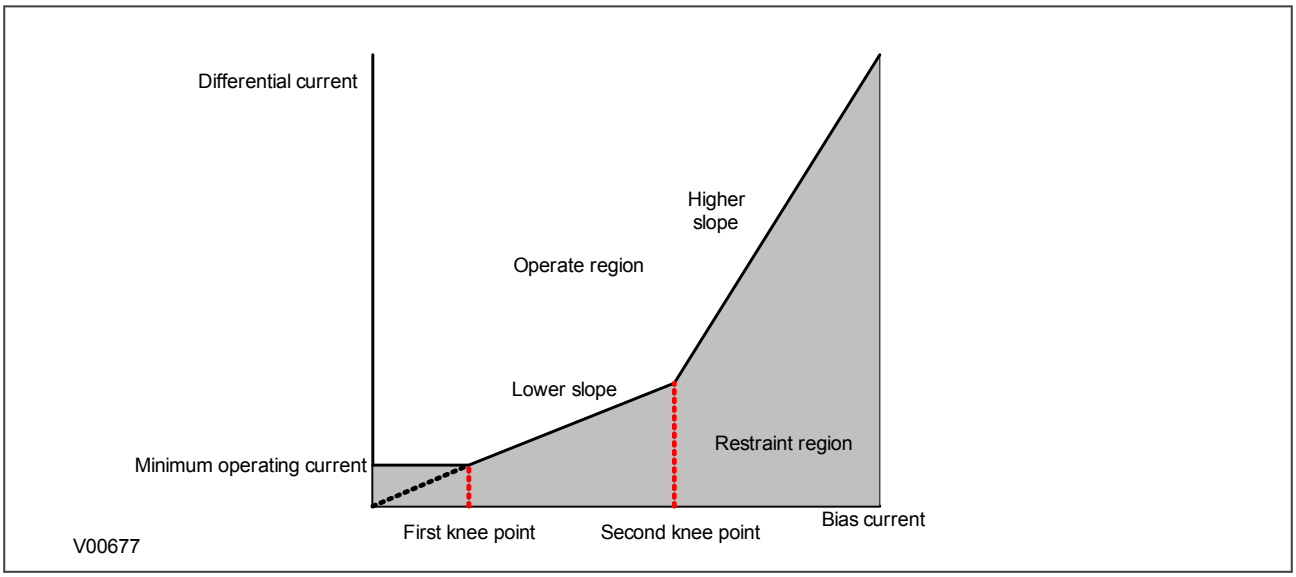


Figure 78: Three-slope REF bias characteristic

The flat area of the characteristic is the minimum differential current required to cause a trip (operate current) at low bias currents. From the first kneepoint onwards, the operate current increases linearly with bias current, as shown by the lower slope on the characteristic. This lower slope provides sensitivity for internal faults. From the

second knee point onwards, the operate current further increases linearly with bias current, but at a higher rate. The second slope provides stability under through fault conditions.

Note:
In Restricted Earth Fault applications, Bias Current Compensation is also known as Low Impedance REF.

2.4.2 HIGH IMPEDANCE REF PRINCIPLE

This scheme is very sensitive and can protect against low levels of fault current, typical of winding faults.

High Impedance REF protection is based on the differential principle. It works on the circulating current principle as shown in the following diagram.

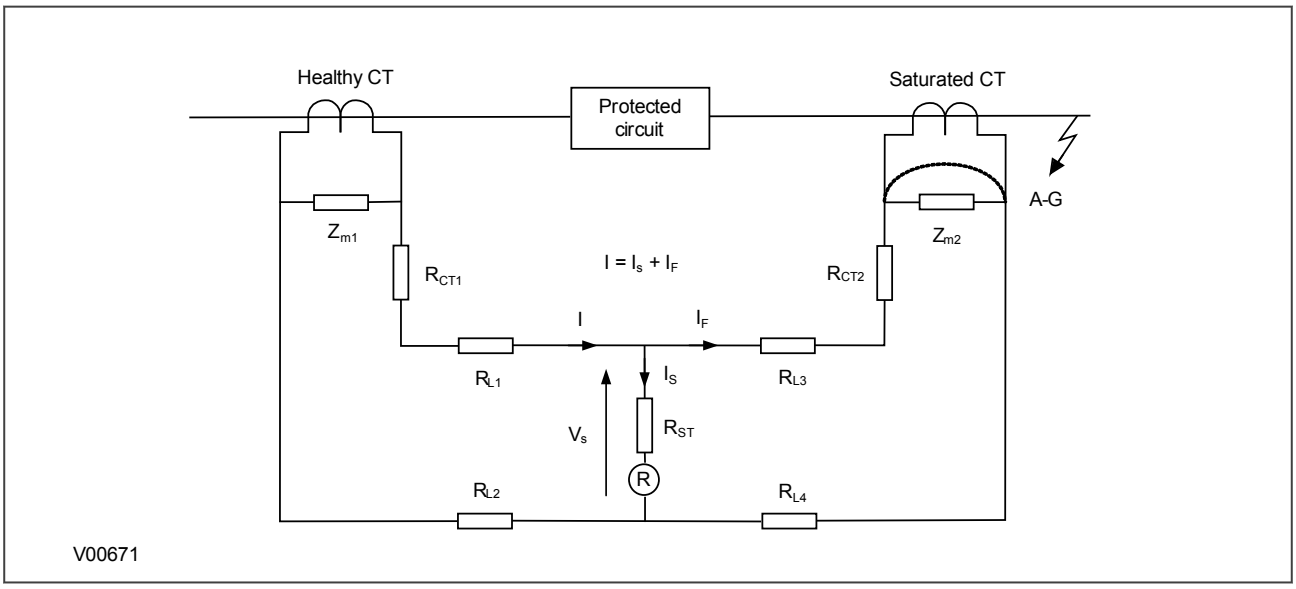


Figure 79: High Impedance REF principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in imbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the device will be less than the setting, therefore maintaining stability during external faults.

Voltage across REF element $V_S = I_F (R_{CT2} + R_{L3} + R_{L4})$

Stabilising resistor $R_{ST} = V_S/I_S - R_R$

where:

- I_F = maximum secondary through fault current
- R_R = device burden
- R_{CT} = CT secondary winding resistance
- R_{L2} and R_{L3} = Resistances of leads from the device to the current transformer
- R_{ST} = Stabilising resistor

High Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED are as follows:

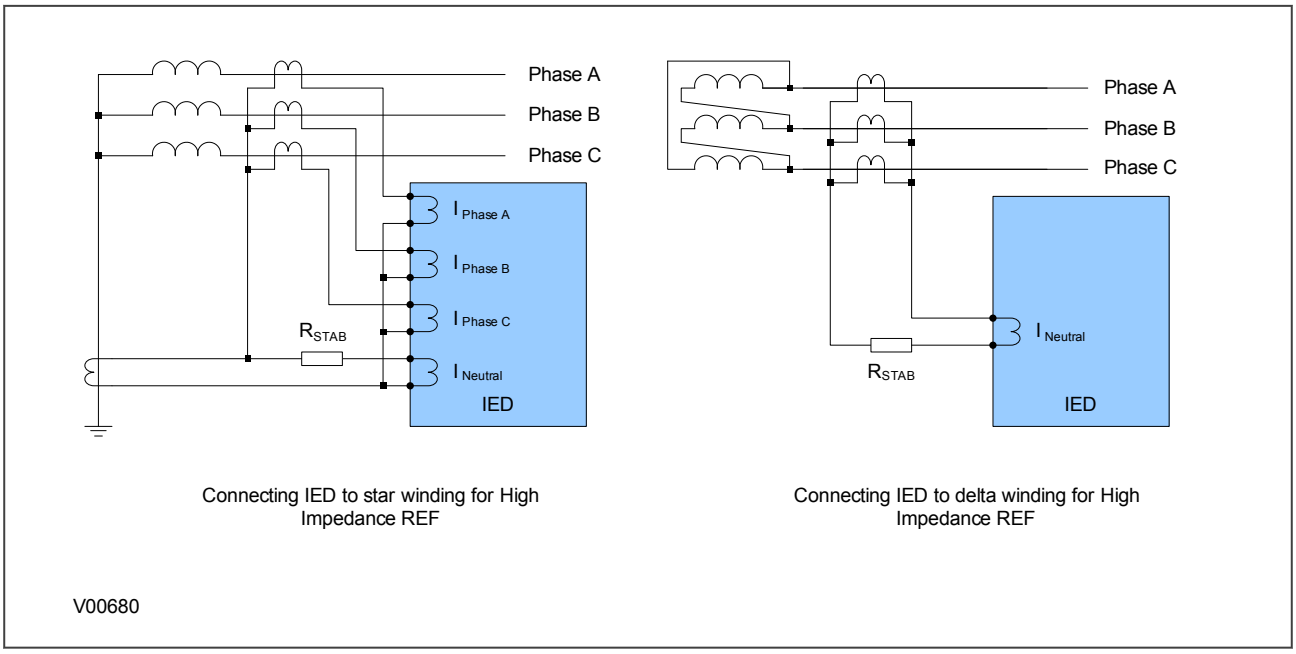


Figure 80: High Impedance REF Connection

3 RESTRICTED EARTH FAULT PROTECTION IMPLEMENTATION

3.1 RESTRICTED EARTH FAULT PROTECTION SETTINGS

Restricted Earth Fault Protection is implemented in the Restricted E/F column of the relevant settings group. It is here that the constants and bias currents are set.

The REF protection may be configured to operate as either a high impedance or biased element.

3.2 LOW IMPEDANCE REF

3.2.1 SETTING THE BIAS CHARACTERISTIC

Low impedance REF uses a bias charactersitic for increasing sensitivity and stabilising for through faults. The current required to trip the differential IED is called the Operate current. This Operate current is a function of the differential current and the bias current according to the bias characteristic.

The differential current is defined as follows:

$$I_{diff} = \left(\bar{I}_A + \bar{I}_B + \bar{I}_C\right) + K\bar{I}_N$$

The bias current is as follows:

$$I_{bias} = \frac{1}{2}\left\{\max\left[|I_A|,|I_B|,|I_C|\right] + K|I_N|\right\}$$

where:

- K = Neutral CT ratio / Line CT ratio
- IN = current measured by the neutral CT

The allowable range for K is:

$$0.05 < K < 15 \text{ for standard CTs}$$

$$0.05 < K < 20 \text{ for sensitive CTs}$$

The operate current is calculated according to the following characteristic:

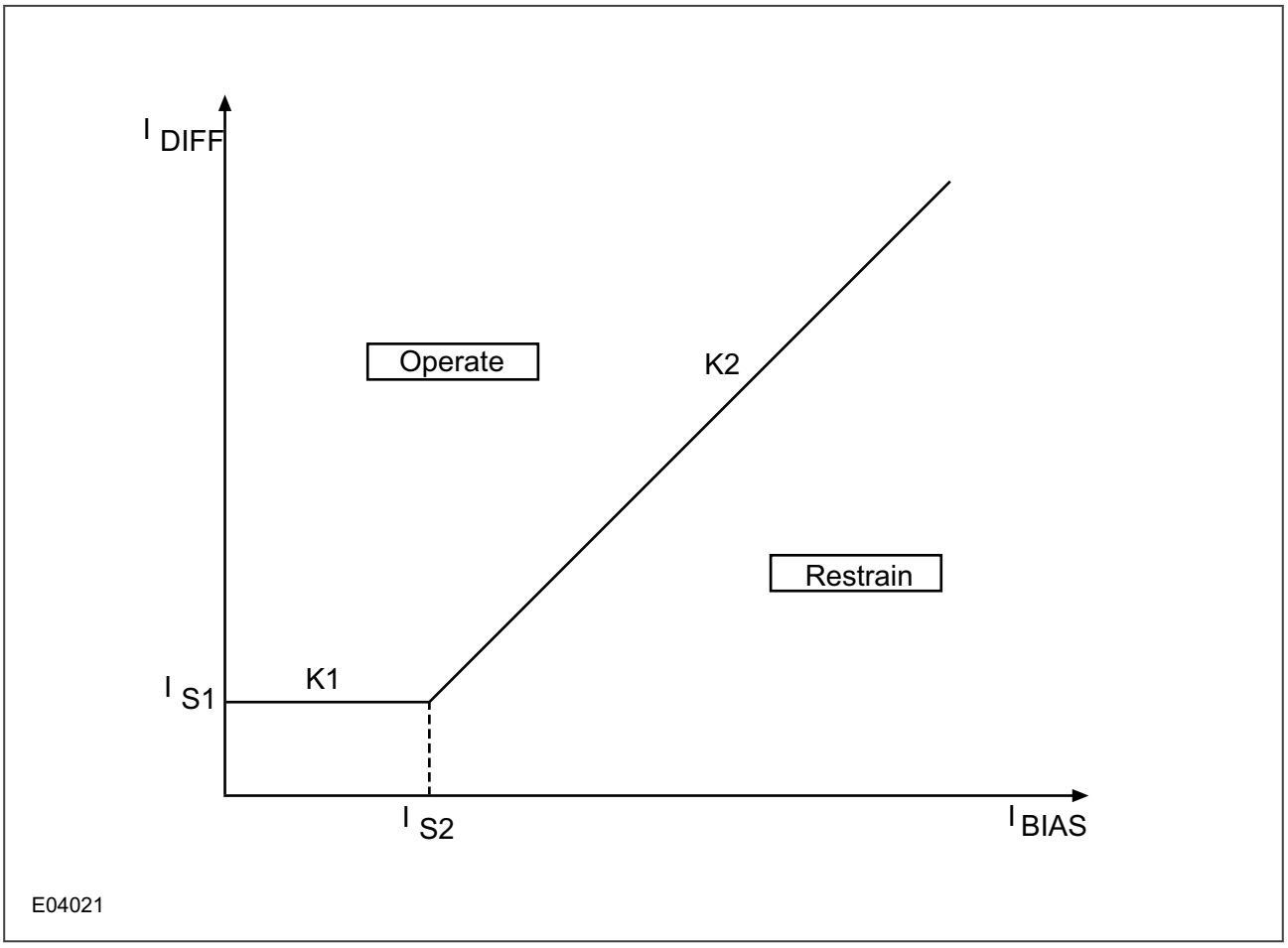


Figure 81: REF bias characteristic

The following settings are provided to define this bias characteristic:

- ***IREF> Is1***: sets the minimum trip threshold
- ***IREF> Is2***: sets the bias current kneepoint whereby the required trip current starts increasing
- ***IREF> k1***: defines the first slope (often set to 0%)
- ***IREF> k2***: defines the second slope

Note:
Is1 and Is2 are relative to the line CT, which is always the reference CT.

3.2.2 DELAYED BIAS

The bias quantity used is actually delayed by one cycle. It is the maximum value of the mean bias quantities calculated within the previous cycle, where the mean bias is the fundamental bias current. This means the bias level, and thus through-fault stability is maintained after an external fault has been cleared.

The algorithm, shown below, is executed eight times per cycle.

$$I_{bias} = Maximum\ [I_{bias}\ (n), I_{bias}\ (n\text{-}1), \ldots I_{bias},\ (n - (K\text{-}1))]$$

It is this delayed bias that is used to calculate the operating current.

3.3 HIGH IMPEDANCE REF

The device provides a high impedance restricted earth fault protection function. An external resistor is required to provide stability in the presence of saturated line current transformers. Current transformer supervision signals do not block the high impedance REF protection. The appropriate logic must be configured in PSL to block the high impedance REF when any of the above signals is asserted.

3.3.1 HIGH IMPEDANCE REF CALCULATION PRINCIPLES

The primary operating current (Iop) is a function of the current transformer ratio, the device operate current (***IREF>Is***), the number of current transformers in parallel with a REF element (n) and the magnetizing current of each current transformer (Ie) at the stability voltage (Vs). This relationship can be expressed in three ways:

1. The maximum current transformer magnetizing current to achieve a specific primary operating current with a particular operating current:

$$I_e < \frac{1}{n}\left(\frac{I_{op}}{CT\ ratio} - [IREF > Is]\right)$$

2. The maximum current setting to achieve a specific primary operating current with a given current transformer magnetizing current:

$$[IREF > Is] < \left(\frac{I_{op}}{CT\ ratio} - nI_e\right)$$

3. The protection primary operating current for a particular operating current with a particular level of magnetizing current:

$$I_{op} = (CT\ ratio)([IREF > Is] + nI_e)$$

To achieve the required primary operating current with the current transformers that are used, you must select a current setting for the high impedance element, as shown in item 2 above. You can calculate the value of the stabilising resistor (R_{ST}) in the following manner.

$$R_{st} = \frac{Vs}{[IREF > Is]} = \frac{I_F\left(R_{CT} + 2R_L\right)}{[IREF > Is]}$$

where:

- R_{CT} = the resistance of the CT winding
- R_L = the resistance of the lead from the CT to the IED.

Note:
The above formula assumes negligible relay burden.

We recommend a stabilizing resistor, which is continuously adjustable up to its maximum declared resistance.

4 APPLICATION NOTES

4.1 STAR WINDING RESISTANCE EARTHED

Consider the following resistance earthed star winding below.

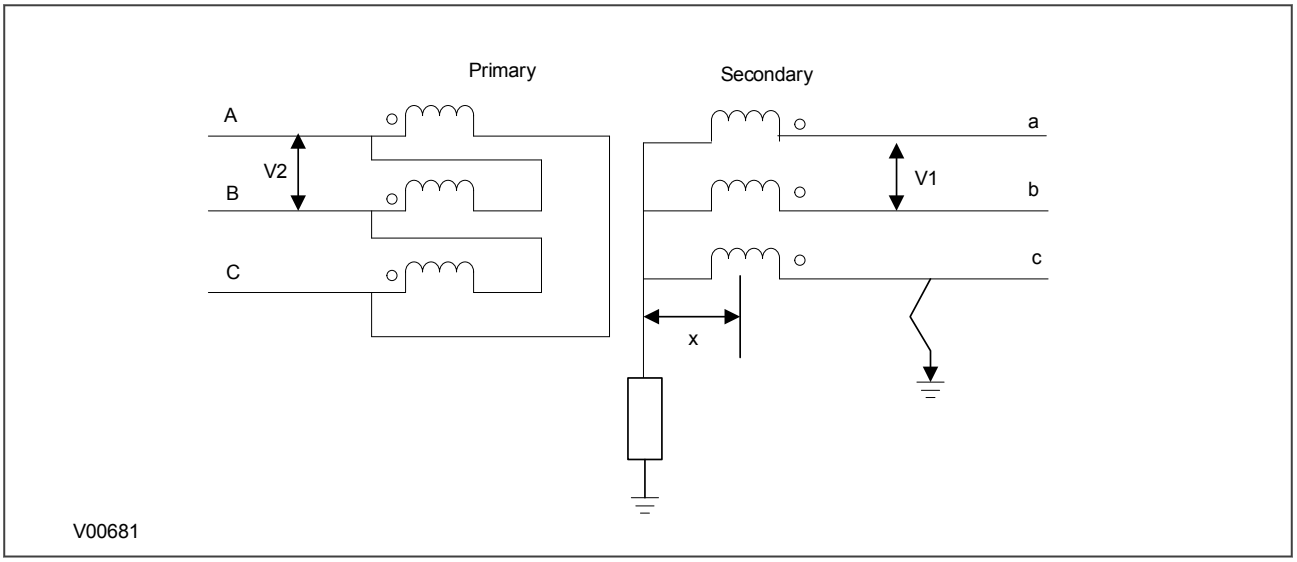


Figure 82: Star winding, resistance earthed

An earth fault on such a winding causes a current which is dependent on the value of earthing impedance. This earth fault current is proportional to the distance of the fault from the neutral point since the fault voltage is directly proportional to this distance.

The ratio of transformation between the primary winding and the short circuited turns also varies with the position of the fault. Therefore the current that flows through the transformer terminals is proportional to the square of the fraction of the winding which is short circuited.

The earthing resistor is rated to pass the full load current $I_{FLC} = V1/\sqrt{3}R$

Assuming that V1 = V2 then $T2 = \sqrt{3}T1$

For a fault at x PU distance from the neutral, the fault current $If = xV1/\sqrt{3}R$

Therefore the secondary fault current referred to the primary is $I_{primary} = x^2.I_{FLC}/\sqrt{3}$

If the fault is a single end fed fault, the primary current should be greater than 0.2 pu (Is1 default setting) for the differential protection to operate. Therefore $x^2/\sqrt{3} > 20\%$

The following diagram shows that 41% of the winding is protected by the differential element.

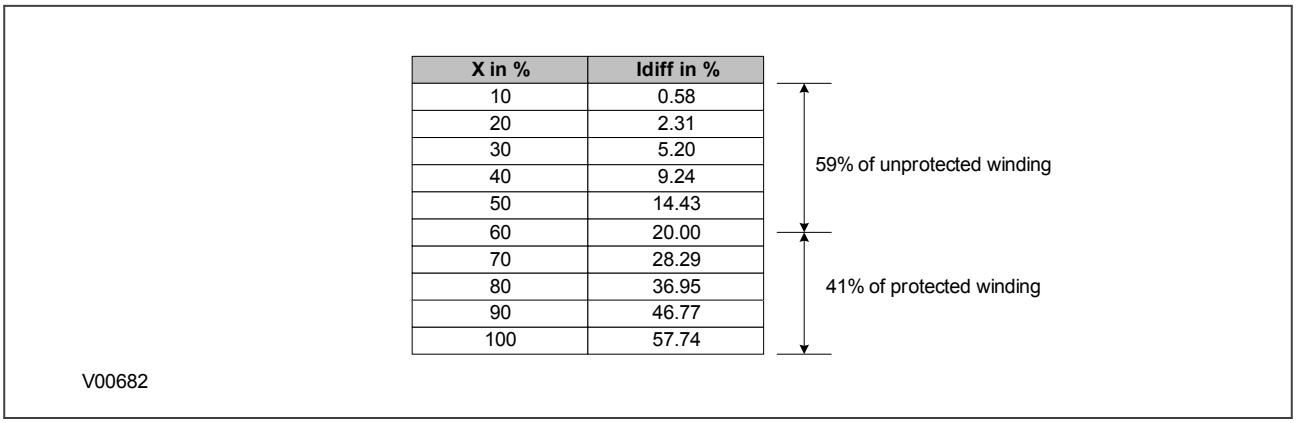


Figure 83: Percentage of winding protected

4.2 LOW IMPEDANCE REF PROTECTION APPLICATION

4.2.1 SETTING GUIDELINES FOR BIASED OPERATION

Two bias settings are provided in the REF characteristic. The K1 level of bias is applied up to through currents of Is2, which is normally set to the rated current of the transformer. K1 is normally be set to 0% to give optimum sensitivity for internal faults. However, if any CT mismatch is present under normal conditions, then K1 may be increased accordingly, to compensate. We recommend a setting of 20% in this case.

K2 bias is applied for through currents above Is2 and would typically be set to 150%.

According to ESI 48-3 1977, typical settings for the Is1 thresholds are 10-60% of the winding rated current when solidly earthed and 10-25% of the minimum earth fault current for a fault at the transformer terminals when resistance earthed.

4.2.2 LOW IMPEDANCE REF SCALING FACTOR

The three line CTs are connected to the three-phase CTs, and the neutral CT is connected to the neutral CT input. These currents are then used internally to derive both a bias and a differential current quantity for use by the low impedance REF protection. The advantage of this mode of connection is that the line and neutral CTs are not differentially connected, so the neutral CT can also be used to provide the measurement for the Standby Earth Fault Protection. Also, no external components such as stabilizing resistors or Metrosils are required.

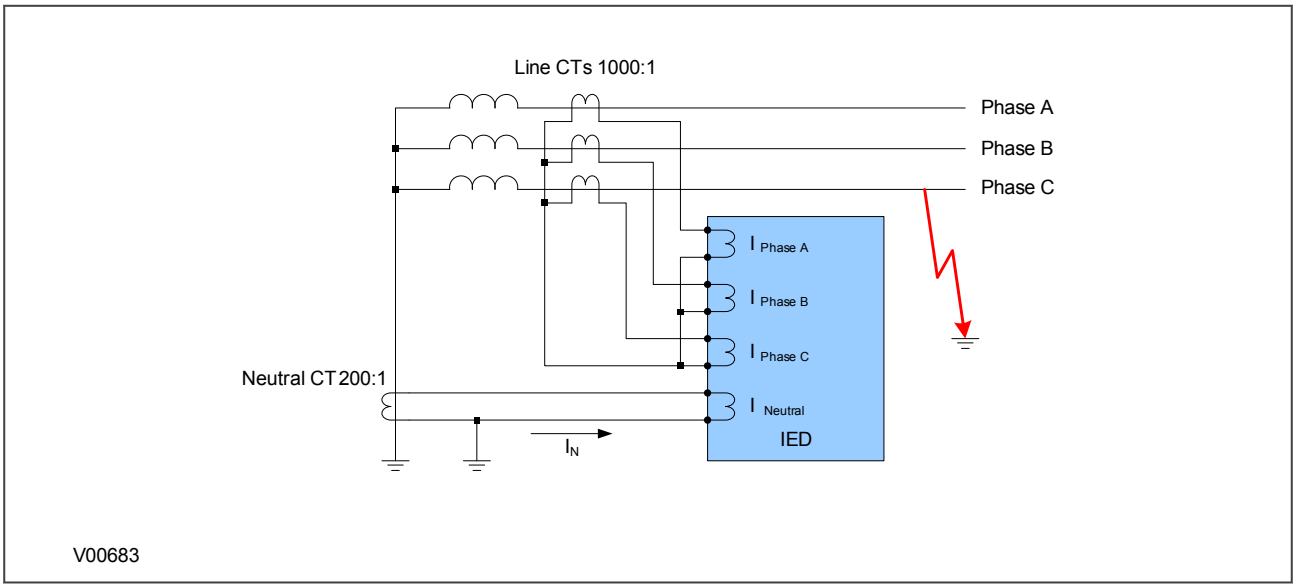


Figure 84: Low Impedance REF Scaling Factor

Another advantage of Low Impedance REF protection is that you can use a neutral CT with a lower ratio than the line CTs in order to provide better earth fault sensitivity. In the bias calculation, the device applies a scaling factor to the neutral current. This scaling factor is as follows:

$$Scaling\ factor = K = Neutral\ CT\ ratio\ /\ Line\ CT\ ratio$$

This results in the following differential and bias current equations:

$$I_{diff} = \left(\bar{I}_A + \bar{I}_B + \bar{I}_C\right) + K\bar{I}_N$$

$$I_{bias} = \frac{1}{2}\left\{\max\left[|I_A|,|I_B|,|I_C|\right] + K|I_N|\right\}$$

4.2.3 PARAMETER CALCULATIONS

Consider a solidly earthed 90 MVA 132 kV transformer with a REF-protected star winding. Assume line CTS with a ratio of 400:1.

Is1 is set to 10% of the winding nominal current:

$= (0.1 \times 90 \times 10^6) / (\sqrt{3} \times 132 \times 10^3)$

$= 39\ Amps\ primary$

$= 39/400 = 0.0975\ Amps\ secondary\ (approx\ 0.1\ A)$

Is2 is set to the rated current of the transformer:

$= 90 \times 10^6 / (\sqrt{3} \times 132 \times 10^3)$

$= 390\ Amps\ primary$

$= 390/400 = 0.975\ Amps\ secondary\ (approx\ 1\ A)$

Set ***K1*** to 0% and ***K2*** to 150%

4.3 HIGH IMPEDANCE REF PROTECTION APPLICATION

4.3.1 HIGH IMPEDANCE REF OPERATING MODES

In the examples below, the respective Line CTS and measurement CTs must have the same CT ratios and similar magnetising characteristics.

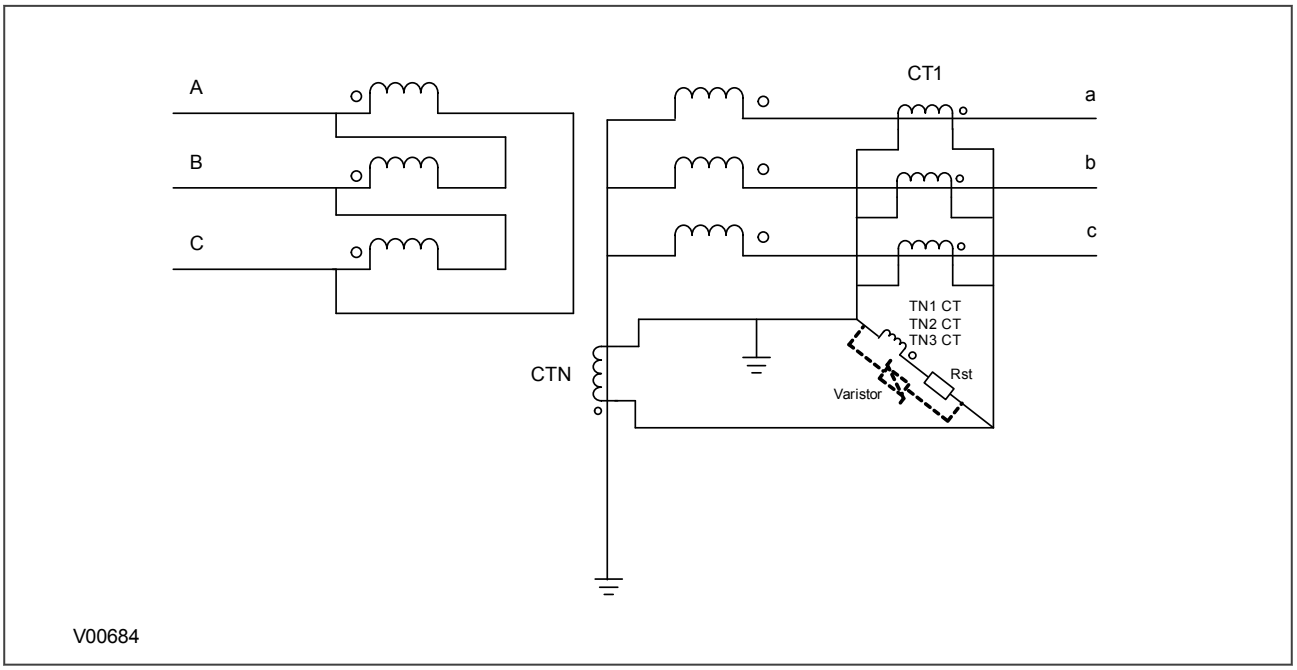


Figure 85: Hi-Z REF protection for a grounded star winding

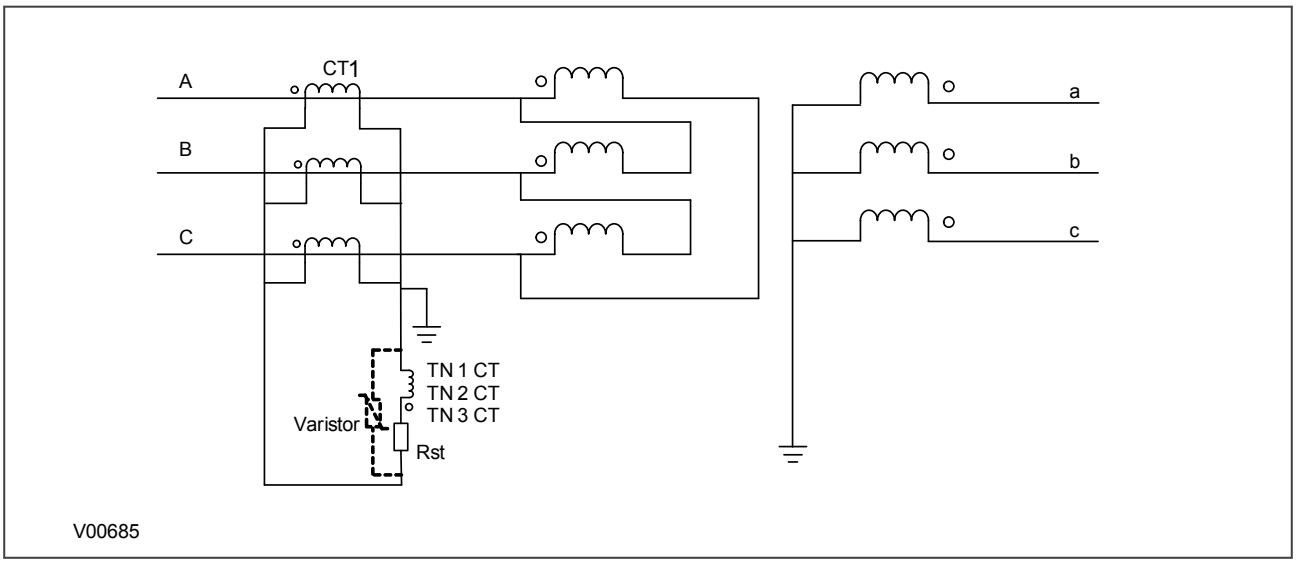


Figure 86: Hi-Z REF protection for a delta winding

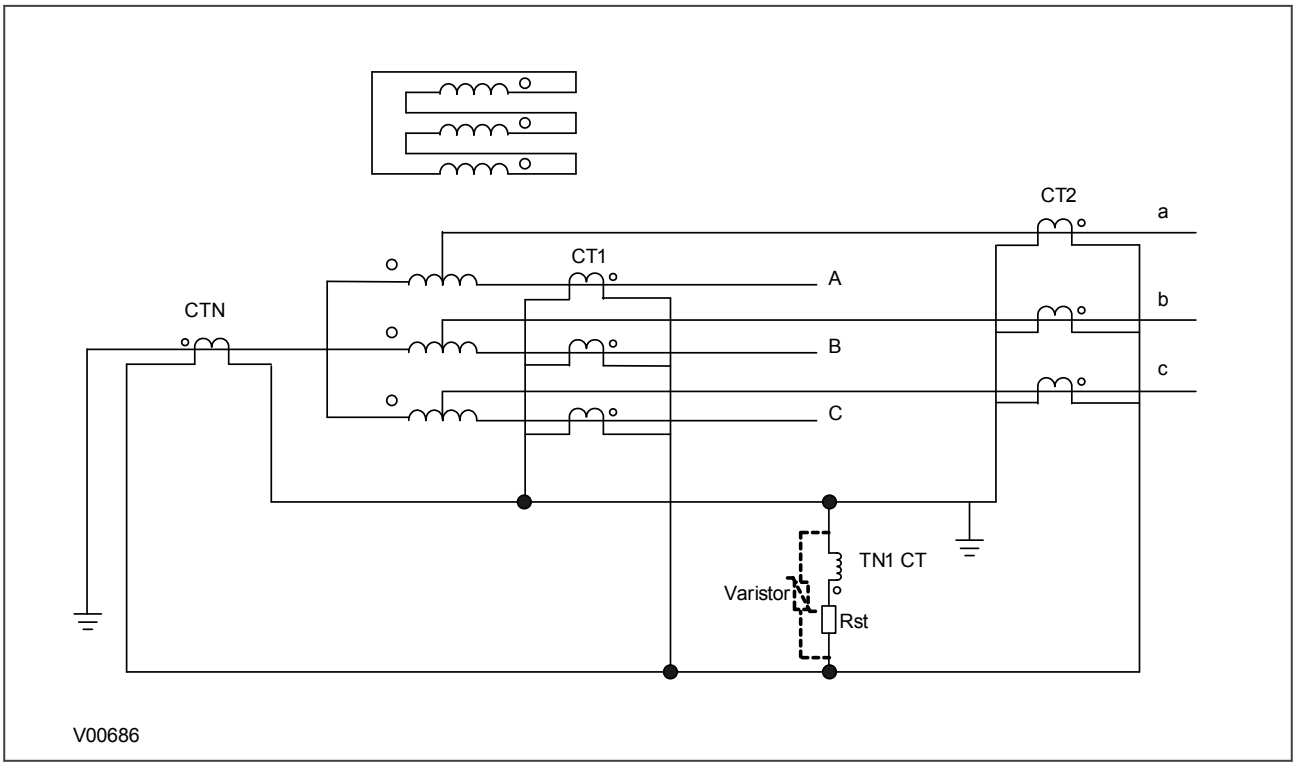


Figure 87: Hi-Z REF Protection for autotransformer configuration

4.3.2 SETTING GUIDELINES FOR HIGH IMPEDANCE OPERATION

This scheme is very sensitive and can protect against low levels of fault current in resistance grounded systems. In this application, the ***IREF>Is*** settings should be chosen to provide a primary operating current less than 10-25% of the minimum earth fault level.

This scheme can also be used in a solidly grounded system. In this application, the ***IREF>Is*** settings should be chosen to provide a primary operating current between 10% and 60 % of the winding rated current.

The following diagram shows the application of a high impedance REF element to protect the LV winding of a power transformer.

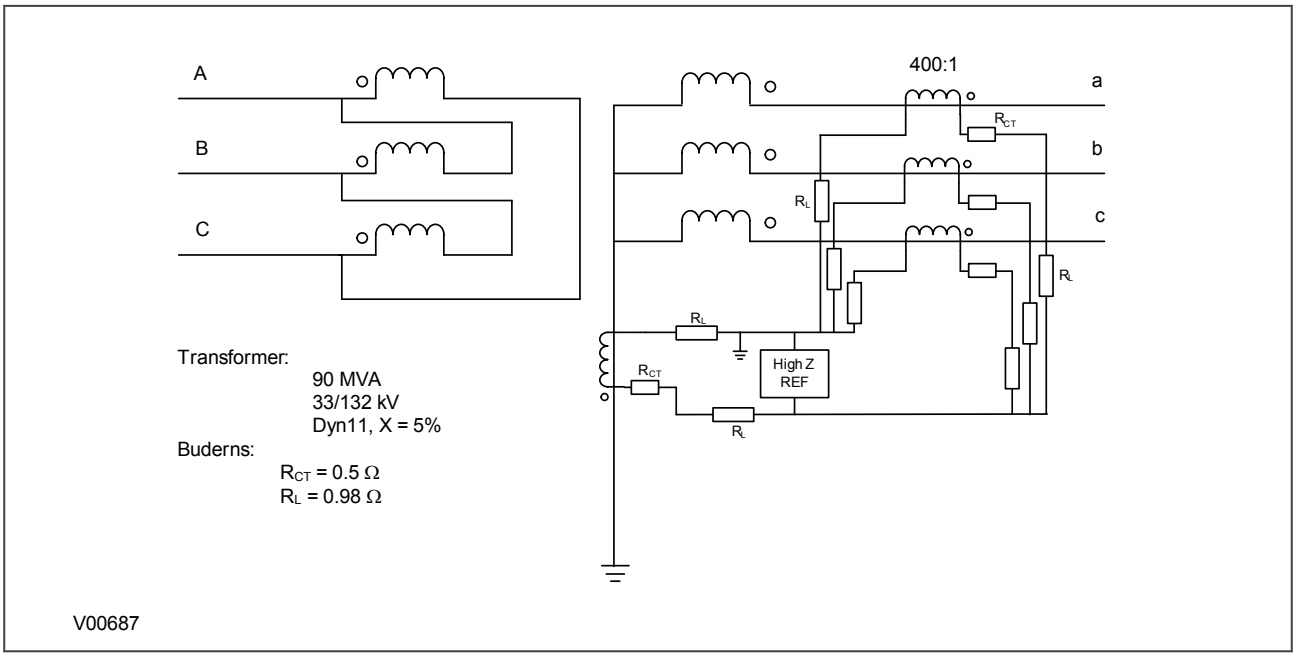


Figure 88: High Impedance REF for the LV winding

4.3.2.1 STABILITY VOLTAGE CALCULATION

The transformer full load current, IFLC, is:

$$I_{FLC} = (90 \times 10^6) / (132 \times 10^3 \times \sqrt{3}) = 394\ A$$

To calculate the stability voltage the maximum through fault level should be considered. The maximum through fault level, ignoring the source impedance, I_F, is:

$$I_F = I_{FLC} / X_{TX} = 394 / 0.05 = 7873\ A$$

The required stability voltage, VS, and assuming one CT saturated is:

$$V_s = KI_F(R_{CT} + 2R_L)$$

The following figure can be used to determine the K factor and the operating time. The K factor is valid when:

- 5 ≤ X/R ≤ 120

and

- 0.5In ≤ I f ≤ 40In

We recommend a value of VK/VS = 4.

With the transformer at full load current and percentage impedance voltage of 394A and 5% respectively, the prospective fault current is 7873 A and the required stability voltage Vs (assuming that one CT is saturated) is:

$$V_s = 0.9 \times 7873 \times (0.5 + 2 \times 0.98) / 400 = 45.5\ V$$

The CTs knee point voltage should be at least 4 times Vs so that an average operating time of 40 ms is achieved.

4.3.2.2 PRIMARY CURRENT CALCULATION

The primary operating current should be between 10 and 60 % of the winding rated current. Assuming that the relay effective setting or primary operating current is approximately 30% of the full load current, the calculation below shows that a setting of less than 0.3 A is required.

$$Effective\ setting = 0.3I_{FLC} / CT\ Ratio = 0.3 \times 394 / 400 = approximately\ 0.3\ A$$

4.3.2.3 STABILISING RESISTOR CALCULATION

Assuming that a setting of 0.1A is selected the value of the stabilizing resistor, R_{ST}, required is

$$R_{ST} = V_s / (IREF> Is1 (HV)) = 45.5 / 0.1 = 455 ohms$$

To achieve an average operating time of 40 ms, Vk/Vs should be 3.5.

The Kneepoint voltage is:

$$V_K = 4V_s = 4 \times 45.5 = 182 V.$$

If the actual V_K is greater than 4 times V_S, then the K factor increases. In this case, V_S should be recalculated.

Note:
K can reach a maximum value of approximately 1.

4.3.2.4 CURRENT TRANSFORMER CALCULATION

The effective primary operating current setting is:

$$I_P = N(I_s + nI_e)$$

By re-arranging this equation, you can calculate the excitation current for each of the current transformers at the stability voltage. This turns out to be:

$$I_e = (0.3 - 0.1) / 4 = 0.05 A$$

In summary, the current transformers used for this application must have a kneepoint voltage of 182 V or higher (note that maximum Vk/Vs that may be considered is 16 and the maximum K factor is 1), with a secondary winding resistance of 0.5 ohms or lower and a magnetizing current at 45.5 V of less than 0.05 A.

Assuming a CT kneepoint voltage of 200 V, the peak voltage can be estimated as:

$$V_P = 2\sqrt{2}V_K(V_F-V_K) = 2\sqrt{2}(200)(9004-200) = 3753 V$$

This value is above the peak voltage of 3000 V and therefore a non-linear resistor is required.

Note:
The kneepoint voltage value used in the above formula should be the actual voltage obtained from the CT magnetizing characteristic and not a calculated value.

Note:
One stabilizing resistor, part No. ZB9016 756, and one varistor, part No. 600A/S1/S256 might be used.

CHAPTER 8

CB FAIL PROTECTION

1 CHAPTER OVERVIEW

The device provides a Circuit Breaker Fail Protection function. This chapter describes the operation of this function including the principles, logic diagrams and applications.

This chapter contains the following sections:

2 CIRCUIT BREAKER FAIL PROTECTION

When a fault occurs, one or more protection devices will operate and issue a trip command to the relevant circuit breakers. Operation of the circuit breaker is essential to isolate the fault and prevent, or at least limit, damage to the power system. For transmission and sub-transmission systems, slow fault clearance can also threaten system stability.

For these reasons, it is common practice to install Circuit Breaker Failure protection (CBF). CBF protection monitors the circuit breaker and establishes whether it has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, the CBF protection will operate, whereby the upstream circuit breakers are back-tripped to ensure that the fault is isolated.

CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

3 CIRCUIT BREAKER FAIL IMPLEMENTATION

Circuit Breaker Failure Protection is implemented in the CB FAIL column of the relevant settings group.

3.1 CIRCUIT BREAKER FAIL TIMERS

The circuit breaker failure protection incorporates two timers, ***CB Fail 1 Timer*** and ***CB Fail 2 Timer***, allowing configuration for the following scenarios:

- Simple CBF, where only ***CB Fail 1 Timer*** is enabled. For any protection trip, the **CB Fail 1 *Timer*** is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, the CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to back-trip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A retripping scheme, plus delayed back-tripping. Here, ***CB Fail 1 Timer*** is used to issue a trip command to a second trip circuit of the same circuit breaker. This requires the circuit breaker to have duplicate circuit breaker trip coils. This mechanism is known as retripping. If retripping fails to open the circuit breaker, a back-trip may be issued following an additional time delay. The back-trip uses ***CB Fail 2 Timer***, which was also started at the instant of the initial protection element trip.

You can configure the CBF elements ***CB Fail 1 Timer*** and ***CBF Fail 2 Timer*** to operate for trips triggered by protection elements within the device. Alternatively you can use an external protection trip by allocating one of the opto-inputs to the ***External Trip*** DDB signal in the PSL.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***Volt Prot Reset*** and ***Ext Prot Reset***.

The resetting options are summarised in the following table:

Initiation (Menu Selectable)	CB Fail Timer Reset Mechanism
Current based protection	The resetting mechanism is fixed (e.g. 50/51/46/21/87) IA< operates AND IB< operates AND IC< operates AND IN< operates
Sensitive Earth Fault element	The resetting mechanism is fixed. ISEF< Operates
Non-current based protection (e.g. 27/59/81/32L)	Three options are available: • All I< and IN< elements operate • Protection element reset AND all I< and IN< elements operate • CB open (all 3 poles) AND all I< and IN< elements operate
External protection	Three options are available. • All I< and IN< elements operate • External trip reset AND all I< and IN< elements operate • CB open (all 3 poles) AND all I< and IN< elements operate

3.2 ZERO CROSSING DETECTION

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is to its saturation point, the higher the subsidence current.

The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the protection clears the fault, the CB Fail function should reset fast to avoid maloperation due to the subsidence current. To compensate for this the device includes a zero-crossing detection algorithm, which ensures that the CB Fail re-trip and back-trip signals are not asserted while subsidence current is flowing. If all the samples within half a cycle are greater than or smaller than 0 A (10 mS for a 50 Hz system), then zero crossing detection is asserted, thereby blocking the operation of the CB Fail function. The zero-crossing detection algorithm is used

after the circuit breaker in the primary system has opened ensuring that the only current flowing in the AC secondary circuit is the subsidence current.

4 CIRCUIT BREAKER FAIL LOGIC

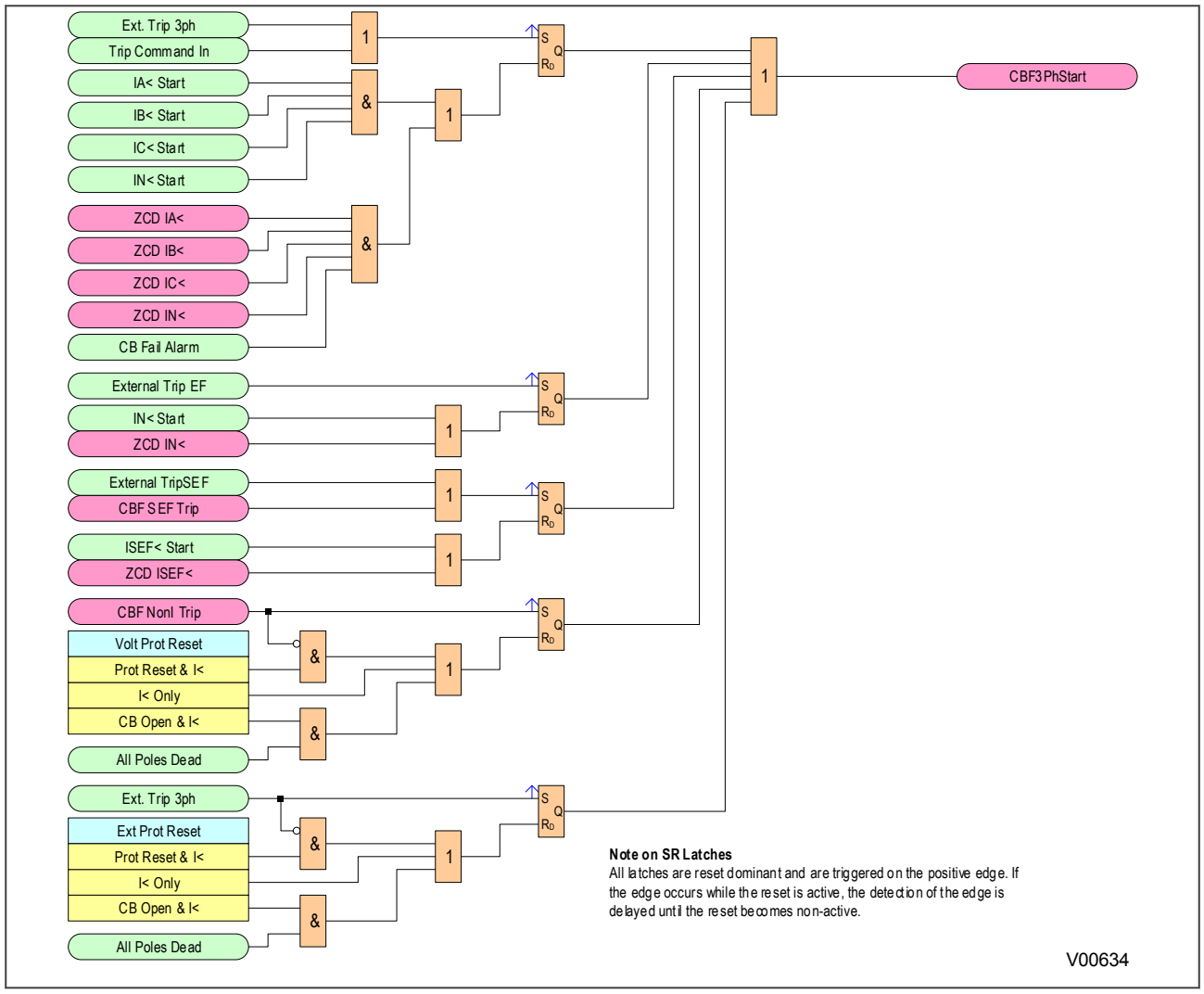


Figure 89: Circuit Breaker Fail logic - three phase start

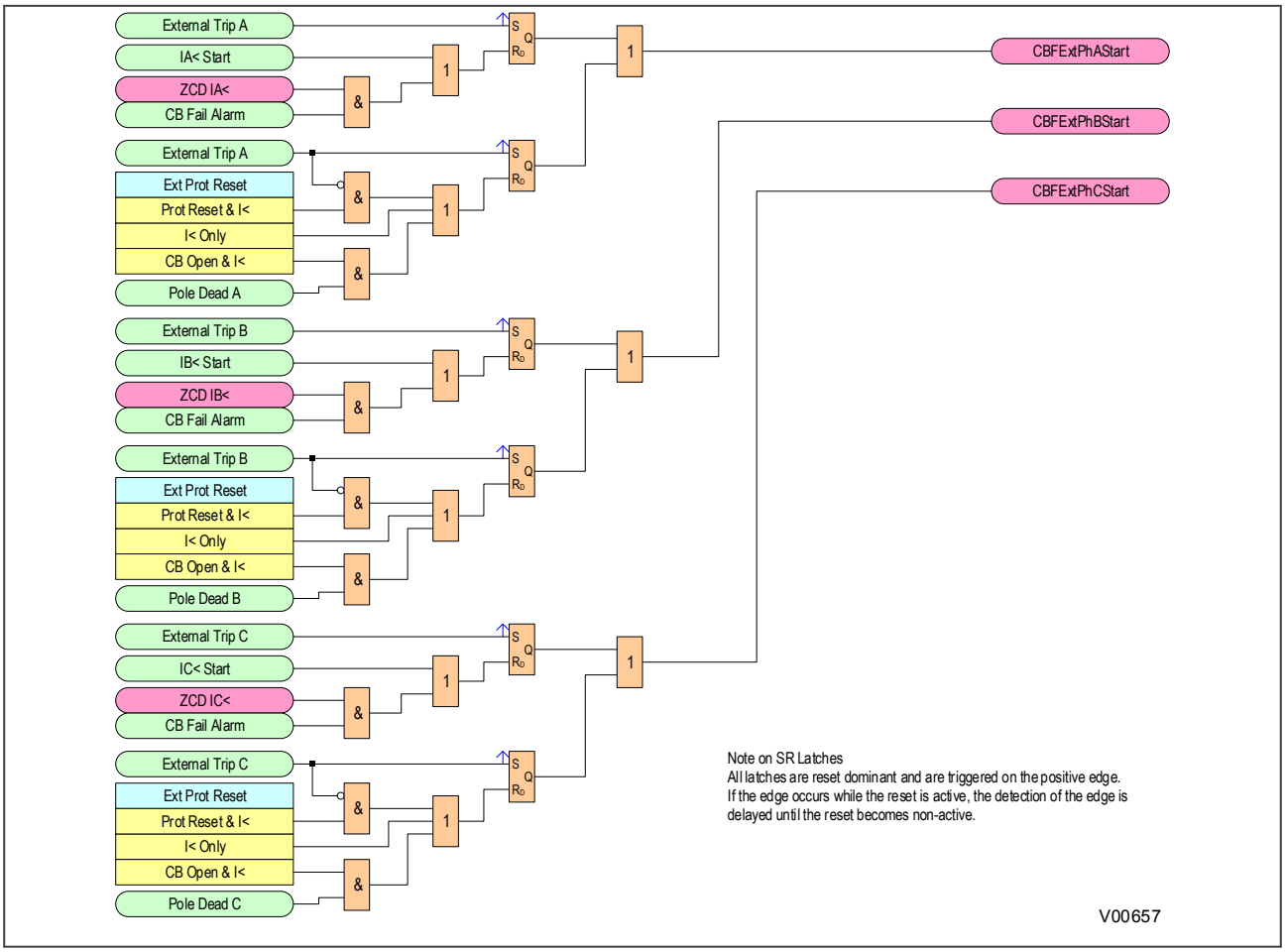


Figure 90: Circuit Breaker Fail logic - single phase start

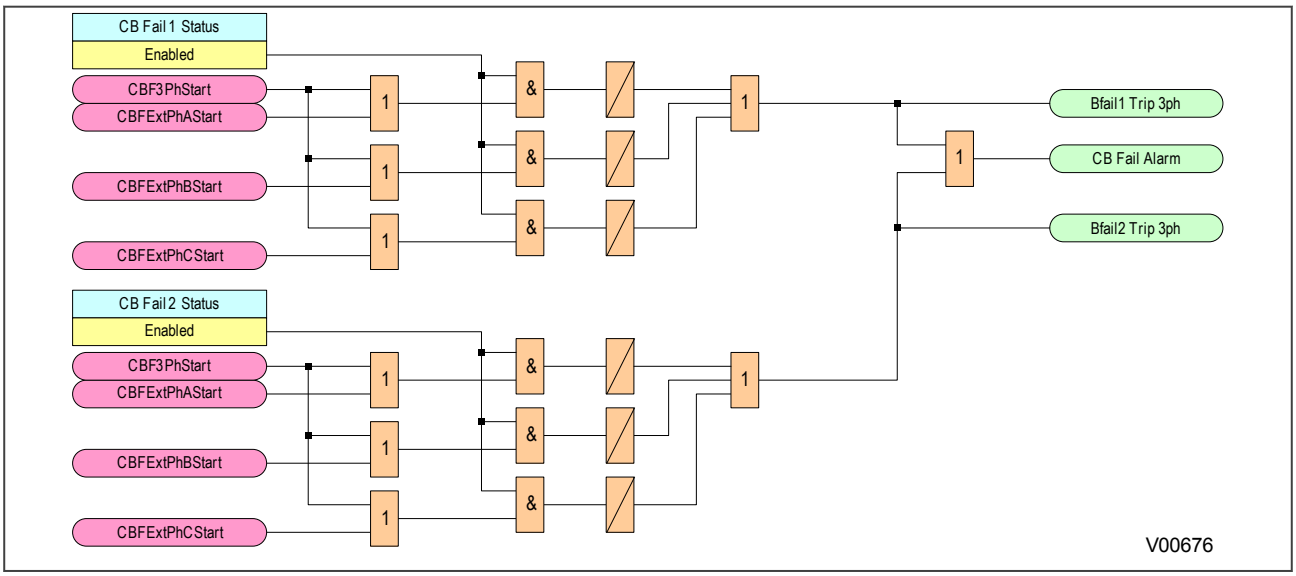


Figure 91: Circuit Breaker Fail Trip and Alarm

5 UNDERCURRENT AND ZCD LOGIC FOR CB FAIL

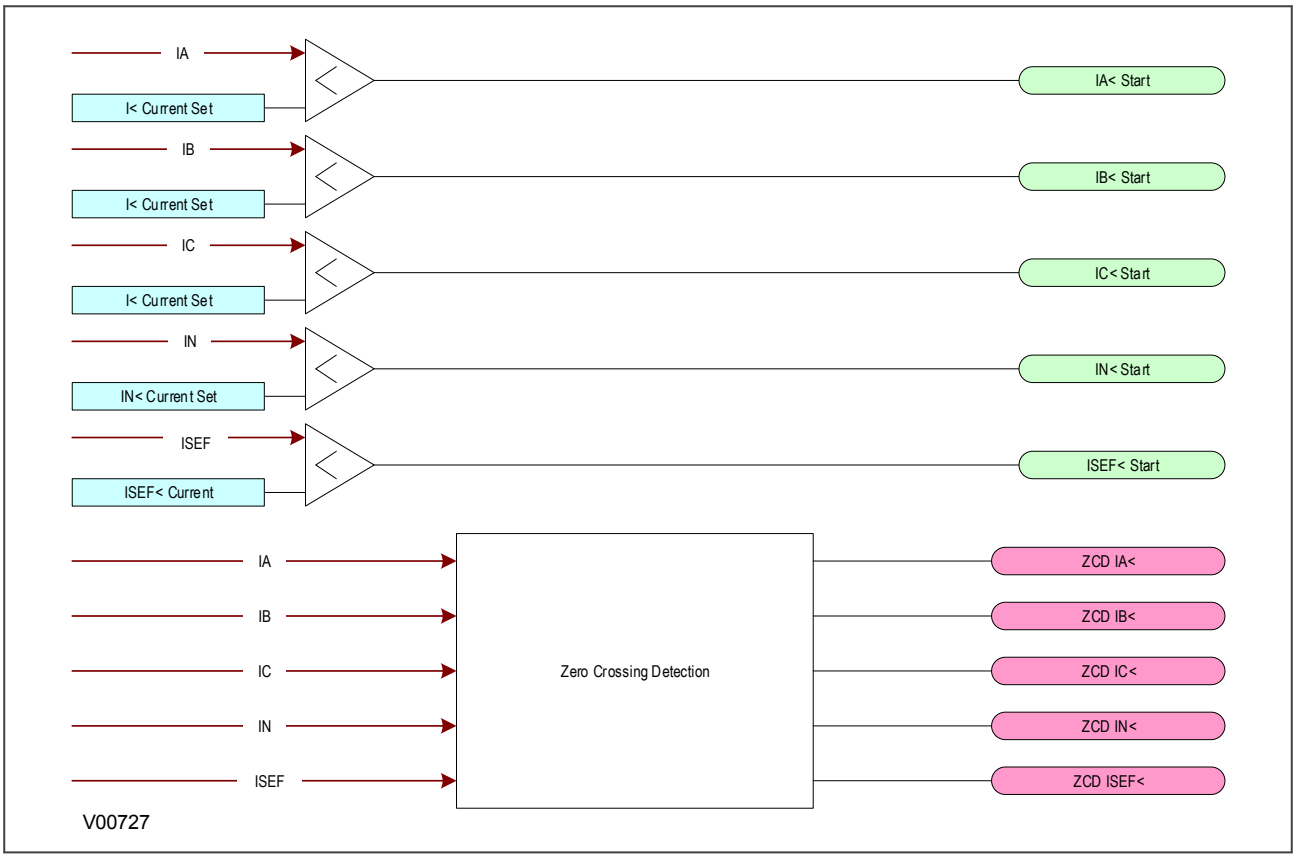


Figure 92: Undercurrent and Zero Crossing Detection Logic for CB Fail

6 CB FAIL SEF PROTECTION LOGIC

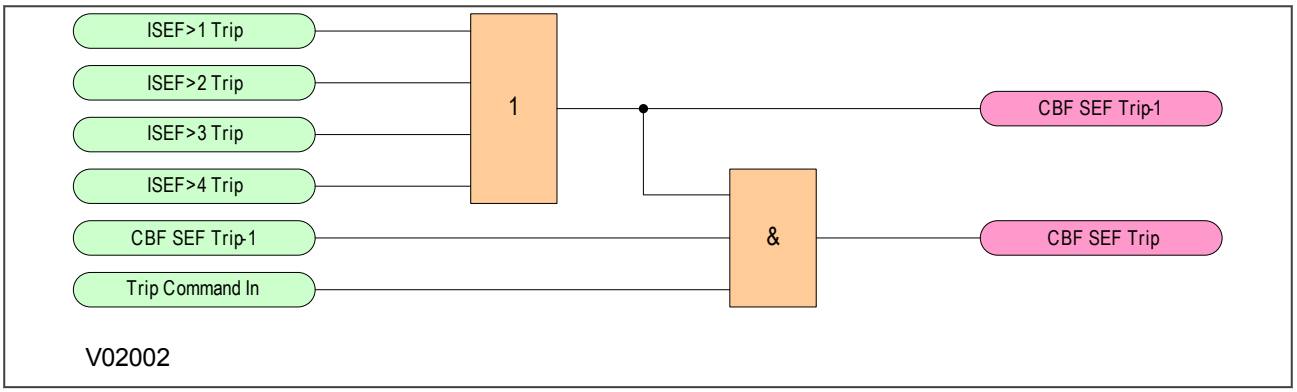


Figure 93: CB Fail SEF Protection Logic

7 CB FAIL NON CURRENT PROTECTION LOGIC

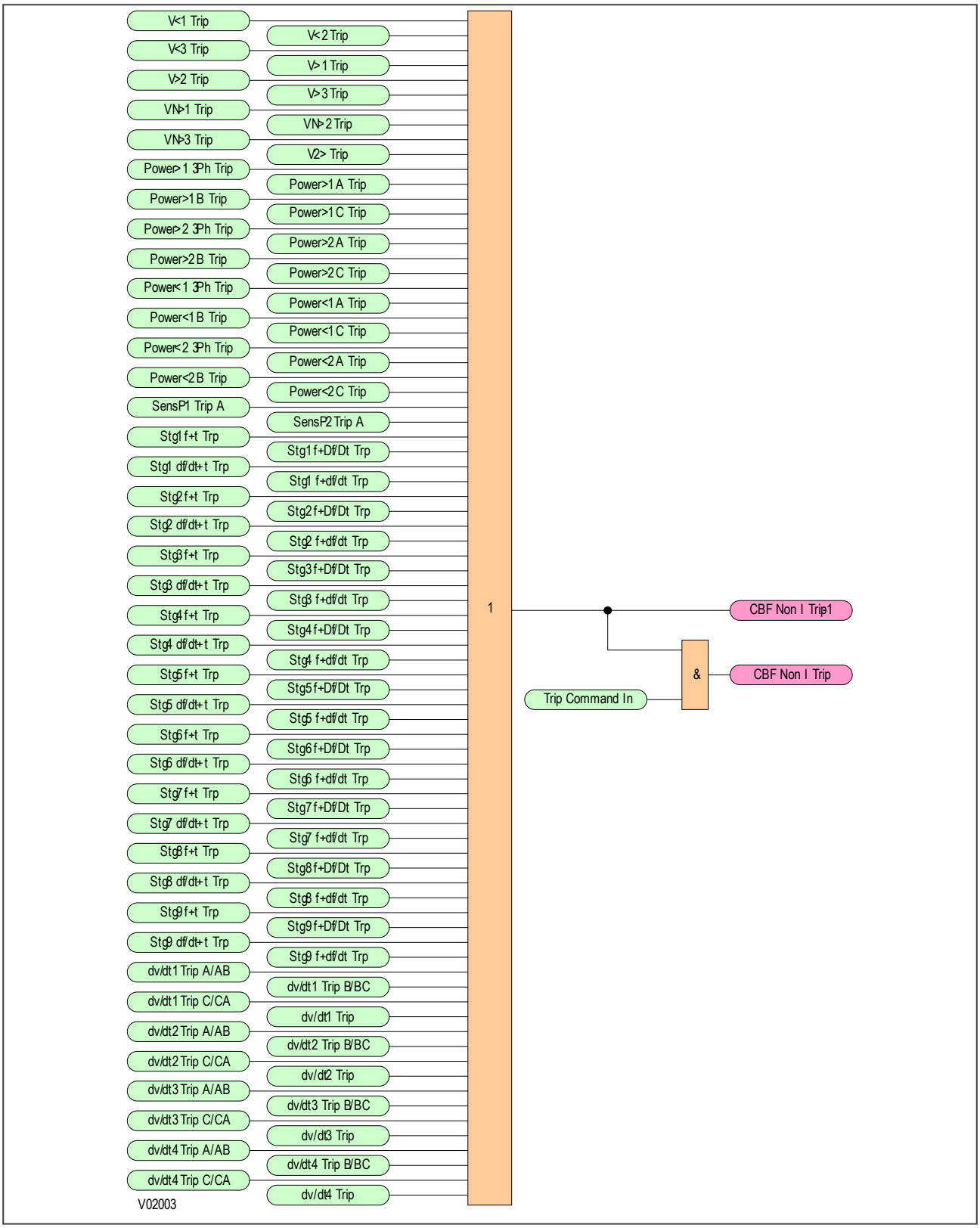


Figure 94: CB Fail Non Current Protection Logic

8 CIRCUIT BREAKER MAPPING

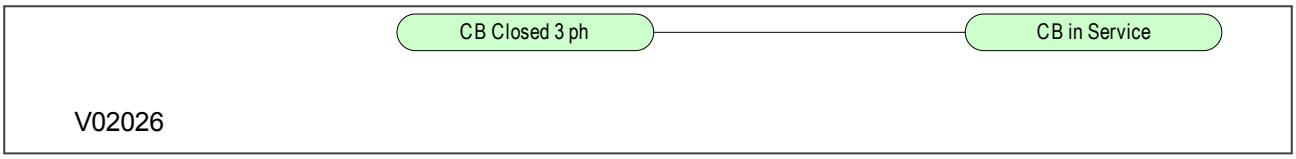


Figure 95: Circuit Breaker mapping

9 APPLICATION NOTES

9.1 RESET MECHANISMS FOR CB FAIL TIMERS

It is common practise to use low set undercurrent elements to indicate that circuit breaker poles have interrupted the fault or load current. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the device uses operation of undercurrent elements to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting CBF in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. In this case, detecting drop-off of the initiating protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

9.2 SETTING GUIDELINES (CB FAIL TIMER)

The following timing chart shows the CB Fail timing during normal and CB Fail operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CB Fail back-up trip time delay considers the maximum CB clearing time, the CB Fail reset time plus a safety margin. Typical CB clearing times are 1.5 or 3 cycles. The CB Fail reset time should be short enough to avoid CB Fail back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CB Fail to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit.

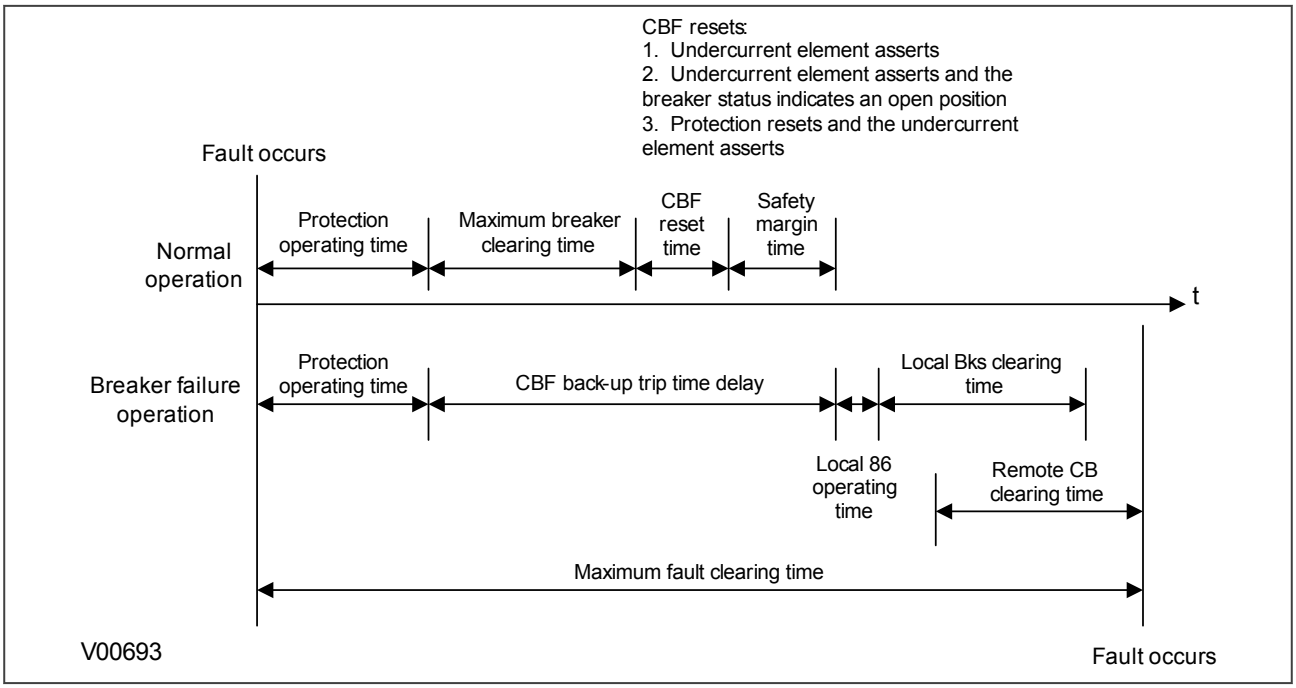


Figure 96: CB Fail timing

The following examples consider direct tripping of a 2-cycle circuit breaker. Typical timer settings to use are as follows:

CB Fail Reset Mechanism	tBF Time Delay	Typical Delay For 2 Cycle Circuit Breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Note:
All CB Fail resetting involves the operation of the undercurrent elements. Where element resetting or CB open resetting is used, the undercurrent time setting should still be used if this proves to be the worst case.
Where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.

9.3 SETTING GUIDELINES (UNDERCURRENT)

The phase undercurrent settings (I<) must be set less than load current to ensure that I< operation correctly indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20%In. Settings of 5% of In are common for generator CB Fail.

The earth fault undercurrent elements must be set less than the respective trip. For example:

$$IN< = (IN> trip)/2$$

CHAPTER 9

CURRENT TRANSFORMER REQUIREMENTS

1 CHAPTER OVERVIEW

This chapter contains the following sections:

2 CT REQUIREMENTS

The current transformer requirements are based on a maximum fault current of 50 times the rated current (In) with the device having an instantaneous overcurrent setting of 25 times the rated current. The current transformer requirements are designed to provide operation of all protection elements.

Where the criteria for a specific application are in excess of this, or the lead resistance exceeds the limiting lead resistance shown in the following table, the CT requirements may need to be modified according to the formulae in the subsequent sections:

Nominal Rating	Nominal Output	Accuracy Class	Accuracy Limited Factor	Limiting Lead Resistance
1A	2.5 VA	10P	20	1.3 ohms
5A	7.5 VA	10P	20	0.11 ohms

The formula subscripts used in the subsequent sections are as follows:

K = A constant affected by the dynamic response of the relay

I_{cn} = Maximum prospective secondary earth fault current or 31 times I> setting (whichever is lower) (amps)

I_{cp} = Maximum prospective secondary phase fault current or 31 times I> setting (whichever is lower) (amps)

I_f = Maximum through-fault current level (amps)

I_{fn} = Maximum prospective secondary earth fault current (amps)

I_{fp} = Maximum prospective secondary phase fault current (amps)

I_n = Rated secondary current (amps)

I_s = Current setting of REF elements (amps)

I_{sn} = Stage 2 & 3 earth fault setting (amps)

I_{sp} = Stage 2 and 3 setting (amps)

I_{st} = Motor start up current referred to CT secondary side (amps)

R_{CT} = Resistance of current transformer secondary winding (ohms)

R_L = Resistance of a single lead from relay to current transformer (ohms)

R_n = Impedance of the neutral current input at 30In (ohms)

R_p = Impedance of the phase current input at 30In (ohms)

R_{st} = Value of stabilising resistor for REF applications (ohms)

V_K = Required CT knee-point voltage (volts)

V_S = Required stability voltage

2.1 PHASE OVERCURRENT PROTECTION

2.1.1 DIRECTIONAL ELEMENTS

Time-delayed phase overcurrent elements

$$V_K = \frac{I_{cp}}{2}(R_{CT} + R_L + R_p)$$

Instantaneous phase overcurrent elements

$$V_K = \frac{I_{fp}}{2}(R_{CT} + R_L + R_p)$$

2.1.2 NON-DIRECTIONAL ELEMENTS

Time-delayed phase overcurrent elements

$$V_K = \frac{I_{cp}}{2}(R_{CT} + R_L + R_p)$$

Instantaneous phase overcurrent elements

$$V_K = I_{sp}(R_{CT} + R_L + R_p)$$

2.2 EARTH FAULT PROTECTION

2.2.1 DIRECTIONAL ELEMENTS

Instantaneous earth fault overcurrent elements

$$V_K = \frac{I_{fn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

2.2.2 NON-DIRECTIONAL ELEMENTS

Time-delayed earth fault overcurrent elements

$$V_K = \frac{I_{cn}}{2}(R_{CT} + 2R_L + R_p + R_n)$$

Instantaneous earth fault overcurrent elements

$$V_K = I_{sn}(R_{CT} + 2R_L + R_p + R_n)$$

2.3 SEF PROTECTION (RESIDUALLY CONNECTED)

2.3.1 DIRECTIONAL ELEMENTS

Time delayed SEF protection

$$V_K \geq \frac{I_{cn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

Instantaneous SEF protection

$$V_K \geq \frac{I_{fn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

2.3.2 NON-DIRECTIONAL ELEMENTS

Time delayed SEF protection

$$V_K \geq \frac{I_{cn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

Instantaneous SEF protection

$$V_K \geq \frac{I_{sn}}{2}(R_{CT} + 2R_L + R_p + Rn)$$

2.4 SEF PROTECTION (CORE-BALANCED CT)

2.4.1 DIRECTIONAL ELEMENTS

Instantaneous element

$$V_K \geq \frac{I_{fn}}{2}(R_{CT} + 2R_L + Rn)$$

Note:
Ensure that the phase error of the applied core balance current transformer is less than 90 minutes at 10% of rated current and less than 150 minutes at 1% of rated current.

2.4.2 NON-DIRECTIONAL ELEMENTS

Time delayed element

$$V_K \geq \frac{I_{cn}}{2}(R_{CT} + 2R_L + Rn)$$

Instantaneous element

$$V_K \geq I_{sn}(R_{CT} + 2R_L + Rn)$$

Note:
Ensure that the phase error of the applied core balance current transformer is less than 90 minutes at 10% of rated current and less than 150 minutes at 1% of rated current.

2.5 LOW IMPEDANCE REF PROTECTION

For X/R < 40 and $I_f < 15I_n$

$$V_K \geq 24I_n(R_{CT} + 2R_L)$$

For 40 < X/R < 120 and $15I_n < If < 40I_n$

$$V_K \geq 48I_n(R_{CT} + 2R_L)$$

Note:
Class x or Class 5P CTs should be used for low impedance REF applications.

2.6 HIGH IMPEDANCE REF PROTECTION

The high impedance REF element will maintain stability for through-faults and operate in less than 40ms for internal faults, provided the following equations are met:

$$R_{st} = \frac{I_f (R_{CT} + 2R_L)}{I_s}$$

$$V_K \geq 4 I_s R_{st}$$

Note:
Class x CTs should be used for high impedance REF applications.

2.7 HIGH IMPEDANCE BUSBAR PROTECTION

The high impedance bus bar protection element will maintain stability for through faults and operate for internal faults. You should select Vk/Vs based on the X/R of the system. The equation is:

$$V_s = K * I_f * (R_{CT} + R_L)$$

For X/R <= 40

$$V_k / V_s >= 2$$

$$Typical\ operating\ time = 25\ ms$$

For X/R > 40

$$V_k / V_s >= 4$$

$$Typical\ operating\ time = 30\ ms$$

Note:
K is a constant affected by the dynamic response of the device. K is always equal to 1.

2.8 USE OF METROSIL NON-LINEAR RESISTORS

Current transformers can develop high peak voltages under internal fault conditions. Metrosils are used to limit these peak voltages to a value below the maximum withstand voltage (usually 3 kV).

You can use the following formulae to estimate the peak transient voltage that could be produced for an internal fault. The peak voltage produced during an internal fault is a function of the current transformer kneepoint voltage and the prospective voltage that would be produced for an internal fault if current transformer saturation did not occur.

$$Vp = 2\sqrt{(2VK(V_F - V_K))}$$

$$Vf = I'f(R_{CT} + 2_{RL} + R_{ST})$$

where:

- Vp = Peak voltage developed by the CT under internal fault conditions
- Vk = Current transformer kneepoint voltage
- Vf = Maximum voltage that would be produced if CT saturation did not occur
- I'f = Maximum internal secondary fault current
- R_{CT} = Current transformer secondary winding resistance
- R_L = Maximum lead burden from current transformer to relay
- R_{ST} = Relay stabilising resistor

You should always use Metrosils when the calculated values are greater than 3000 V. Metrosils are connected across the circuit to shunt the secondary current output of the current transformer from the device to prevent very high secondary voltages.

Metrosils are externally mounted and take the form of annular discs. Their operating characteristics follow the expression:

$$V = CI^{0.25}$$

where:

- V = Instantaneous voltage applied to the Metrosil
- C = Constant of the Metrosil
- I = Instantaneous current through the Metrosil

With a sinusoidal voltage applied across the Metrosil, the RMS current would be approximately 0.52 x the peak current. This current value can be calculated as follows:

$$I_{RMS} = 0.52\left(\frac{\sqrt{2}V_{S(RMS)}}{C}\right)^4$$

where:

- $V_{S(RMS)}$ = RMS value of the sinusoidal voltage applied across the metrosil.

This is due to the fact that the current waveform through the Metrosil is not sinusoidal but appreciably distorted.

The Metrosil characteristic should be such that it complies with the following requirements:

- The Metrosil current should be as low as possible, and no greater than 30 mA RMS for 1 A current transformers or 100 mA RMS for 5 A current transformers.
- At the maximum secondary current, the Metrosil should limit the voltage to 1500 V RMS or 2120 V peak for 0.25 second. At higher device voltages it is not always possible to limit the fault voltage to 1500 V rms, so higher fault voltages may have to be tolerated.

The following tables show the typical Metrosil types that will be required, depending on relay current rating, REF voltage setting etc.

Metrosils for devices with a 1 Amp CT

The Metrosil units with 1 Amp CTs have been designed to comply with the following restrictions:

- The Metrosil current should be less than 30 mA rms.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms if possible.

The Metrosil units normally recommended for use with 1Amp CTs are as shown in the following table:

	Nominal Characteristic		Recommended Metrosil Type	
Device Voltage Setting	C	β	Single Pole Relay	Triple Pole Relay
Up to 125 V RMS	450	0.25	600A/S1/S256	600A/S3/1/S802
125 to 300 V RMS	900	0.25	600A/S1/S1088	600A/S3/1/S1195

Note:
Single pole Metrosil units are normally supplied without mounting brackets unless otherwise specified by the customer.

Metrosils for devices with a 5 Amp CT

These Metrosil units have been designed to comply with the following requirements:

- The Metrosil current should be less than 100 mA rms (the actual maximum currents passed by the devices shown below their type description.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms for 0.25secs. At the higher relay settings, it is not possible to limit the fault voltage to 1500 V rms so higher fault voltages have to be tolerated.

The Metrosil units normally recommended for use with 5 Amp CTs and single pole relays are as shown in the following table:

Secondary Internal Fault Current	Recommended Metrosil types for various voltage settings			
Amps RMS	Up to 200 V RMS	250 V RMS	275 V RMS	300 V RMS
50A	600A/S1/S1213 C = 540/640 35 mA RMS	600A/S1/S1214 C = 670/800 40 mA RMS	600A/S1/S1214 C =670/800 50 mA RMS	600A/S1/S1223 C = 740/870 50 mA RMS
100A	600A/S2/P/ S1217 C = 470/540 70 mA RMS	600A/S2/P/S1215 C = 570/670 75 mA RMS	600A/S2/P/S1215 C =570/670 100 mA RMS	600A/S2/P/S1196 C =620/740 100 mA RMS
150A	600A/S3/P/ S1219 C = 430/500 100 mA RMS	600A/S3/P/S1220 C = 520/620 100 mA RMS	600A/S3/P/S1221 C = 570/670 100 mA RMS	600A/S3/P/S1222 C =620/740 100 mA RMS

In some situations single disc assemblies may be acceptable, contact General Electric for detailed applications.

Note:
The Metrosils recommended for use with 5 Amp CTs can also be used with triple pole devices and consist of three single pole units mounted on the same central stud but electrically insulated from each other. To order these units please specify "Triple pole Metrosil type", followed by the single pole type reference. Metrosil for higher voltage settings and fault currents are available if required.

2.9 USE OF ANSI C-CLASS CTS

Where American/IEEE standards are used to specify CTs, the C class voltage rating can be used to determine the equivalent knee point voltage according to IEC. The equivalence formula is:

$$V_K = 1.05(C\ rating\ in\ volts) + 100R_{CT}$$

CHAPTER 10

VOLTAGE PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

The device provides a wide range of voltage protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

2 UNDERVOLTAGE PROTECTION

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Undervoltage conditions can be related to increased loads, whereby the supply voltage will decrease in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an undervoltage condition, which must be cleared.
- If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping by means of an undervoltage element is required.
- Faults occurring on the power system result in a reduction in voltage of the faulty phases. The proportion by which the voltage decreases is dependent on the type of fault, method of system earthing and its location. Consequently, co-ordination with other voltage and current-based protection devices is essential in order to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be necessary to isolate each of the outgoing circuits, such that when supply voltage is restored, the load is not connected. Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This can be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions that last longer than a pre-determined time.

2.1 UNDERVOLTAGE PROTECTION IMPLEMENTATION

Undervoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Undervoltage parameters are contained within the sub-heading *UNDERVOLTAGE*.

The product provides three stages of Undervoltage protection with independent time delay characteristics.

Stages 1 and 3 provide a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- A range of user-defined curves
- DT (Definite Time)

You set this using the ***V<1 Function*** and ***V<3 Function*** cells depending on the stage.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage

The undervoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V< Measure't mode*** cell.

There is no Timer Hold facility for Undervoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V<2*** status cell.

Three stages are included in order to provide multiple output types, such as alarm and trip stages. Alternatively, different time settings may be required depending upon the severity of the voltage dip. For example, motor loads will be able to cope with a small voltage dip for a longer time than a major one.

Outputs are available for single or three-phase conditions via the ***V< Operate Mode*** cell for each stage.

2.2 UNDERVOLTAGE PROTECTION LOGIC

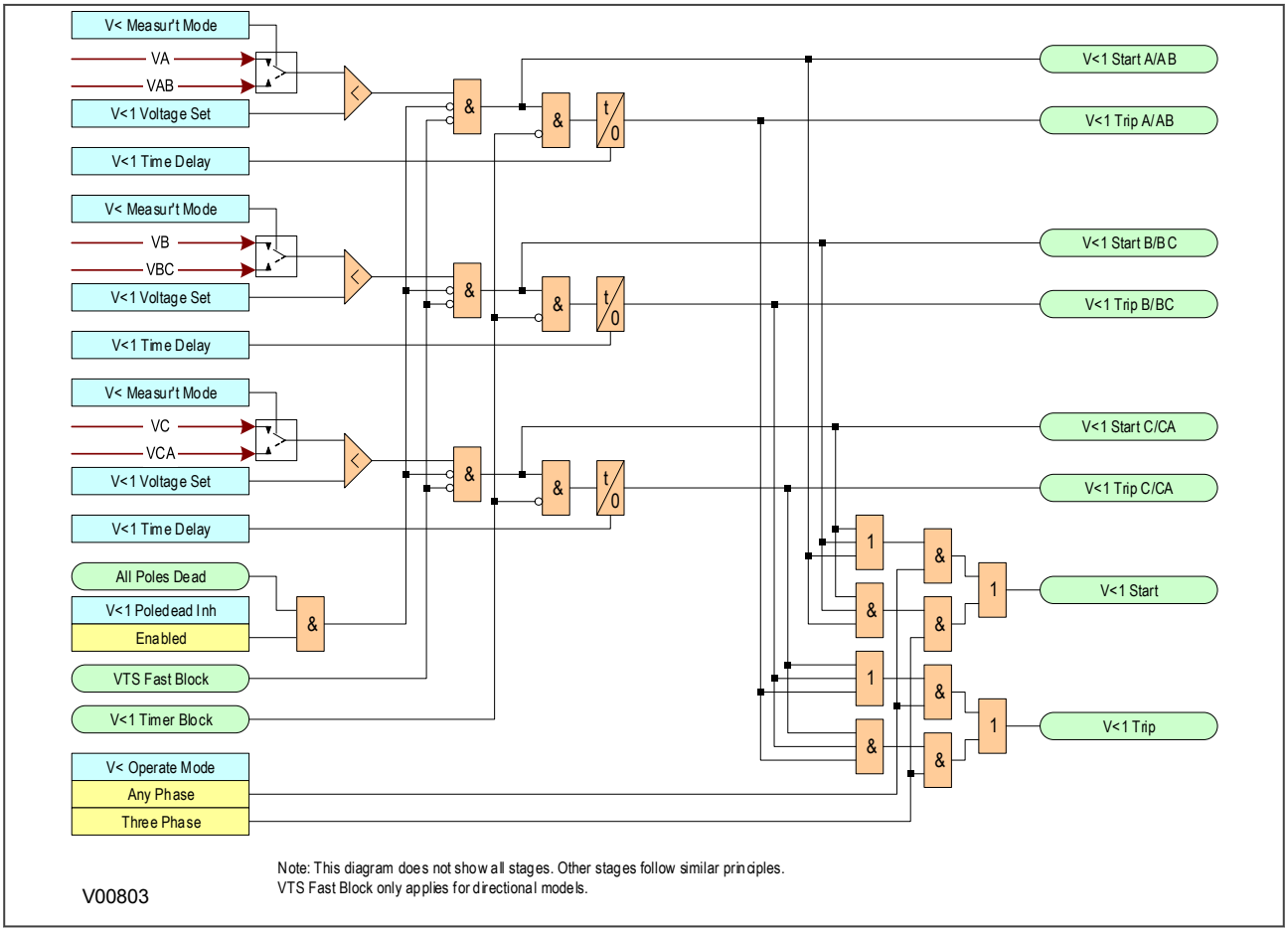


Figure 97: Undervoltage - single and three phase tripping mode (single stage)

The Undervoltage protection function detects when the voltage magnitude for a certain stage falls short of a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal and an ***All Poles Dead*** signal. This ***Start*** signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the undervoltage timer block signal (***V<(n) Timer Block***). For each stage, there are three Phase undervoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V<(n) Start***), which can be be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V< Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V< Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

In some cases, we do not want the undervoltage element to trip; for example, when the protected feeder is de-energised, or the circuit breaker is opened, an undervoltage condition would obviously be detected, but we would not want to start protection. To cater for this, an ***All Poles Dead*** signal blocks the ***Start*** signal for each phase. This is controlled by the ***V<Poledead Inh*** cell, which is included for each of the stages. If the cell is enabled, the relevant stage will be blocked by the integrated pole dead logic. This logic produces an output when it detects either an

open circuit breaker via auxiliary contacts feeding the opto-inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

2.3 APPLICATION NOTES

2.3.1 UNDERVOLTAGE SETTING GUIDELINES

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case you should select phase-to-phase voltage measurement, as this quantity is less affected by single-phase voltage dips due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependent on the system in question but typical healthy system voltage excursions may be in the order of 10% of nominal value.

The same applies to the time setting. The required time delay is dependent on the time for which the system is able to withstand a reduced voltage.

If motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

3 OVERVOLTAGE PROTECTION

Overvoltage conditions are generally related to loss of load conditions, whereby the supply voltage increases in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an overvoltage condition which must be cleared.

Note:
During earth fault conditions on a power system there may be an increase in the healthy phase voltages. Ideally, the system should be designed to withstand such overvoltages for a defined period of time.

3.1 OVERVOLTAGE PROTECTION IMPLEMENTATION

Overvoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Overvoltage parameters are contained within the sub-heading *OVERVOLTAGE*.

The product provides three stages of overvoltage protection with independent time delay characteristics.

Stages 1 and 3 provide a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- A range of user-defined curves
- DT (Definite Time)

You set this using the ***V>1 Function*** and ***V>3 Function*** cells depending on the stage.

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage setting voltage (***V> Voltage Set***)

The overvoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V> Measure't mode*** cell.

There is no Timer Hold facility for Overvoltage.

Stage 2 has definite time characteristics only. This is set in the ***V>2 status*** cell.

Three stages are included in order to provide multiple output types, such as alarm and trip stages. Alternatively, different time settings may be required depending upon the severity of the voltage increase.

Outputs are available for single or three-phase conditions via the ***V> Operate Mode*** cell for each stage.

3.2 OVERVOLTAGE PROTECTION LOGIC

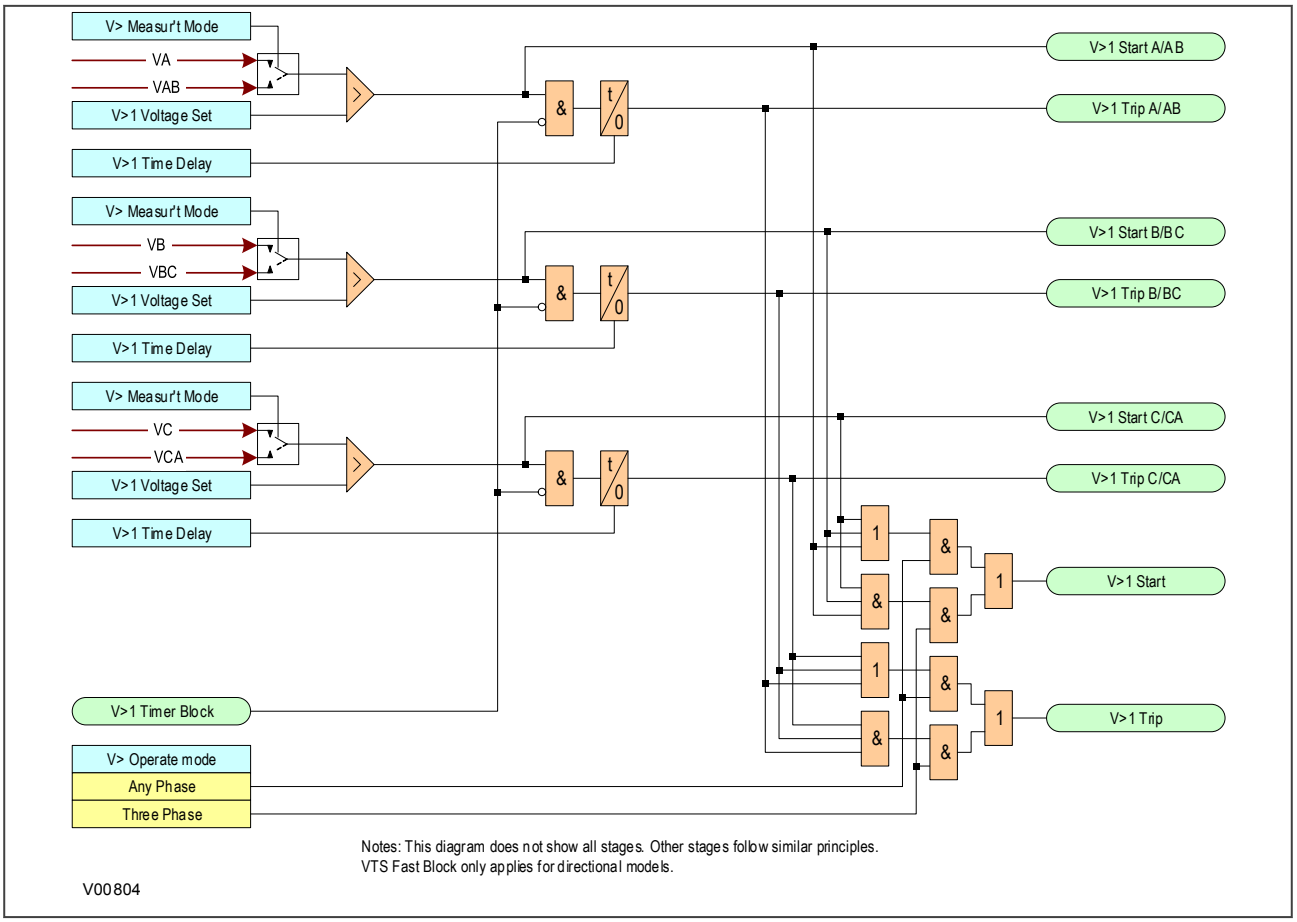


Figure 98: Overvoltage - single and three phase tripping mode (single stage)

The Overvoltage protection function detects when the voltage magnitude for a certain stage exceeds a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal. This start signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the overvoltage timer block signal (***V>(n) Timer Block***). For each stage, there are three Phase overvoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V>(n) Start***), which can then be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V> Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V> Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

3.3 APPLICATION NOTES

3.3.1 OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

4 RATE OF CHANGE OF VOLTAGE PROTECTION

Where there are very large loads, imbalances may occur, which could result in rapid decline in system voltage. The situation could be so bad that shedding one or two stages of load would be unlikely to stop this rapid voltage decline. In such a situation, standard undervoltage protection will normally have to be supplemented with protection that responds to the rate of change of voltage. An element is therefore required, which identifies the high rate of decline of voltage and adapts the load shedding scheme accordingly.

Such protection can identify voltage variations occurring close to nominal voltage thereby providing early warning of a developing voltage problem. The element can also be used as an alarm to warn operators of unusually high system voltage variations.

Rate of Change of Voltage protection is also known as dv/dt protection.

4.1 RATE OF CHANGE OF VOLTAGE PROTECTION IMPLEMENTATION

The dv/dt protection functions can be found in the the *VOLT PROTECTION* column under the sub-heading *DV/DT PROTECTION*. The dv/dt protection consists of four independent stages, which can be configured as either `Phase-Phase` or `Phase-Neutral` using the ***dv/dt Meas mode*** cell.

4.2 RATE OF CHANGE OF VOLTAGE LOGIC

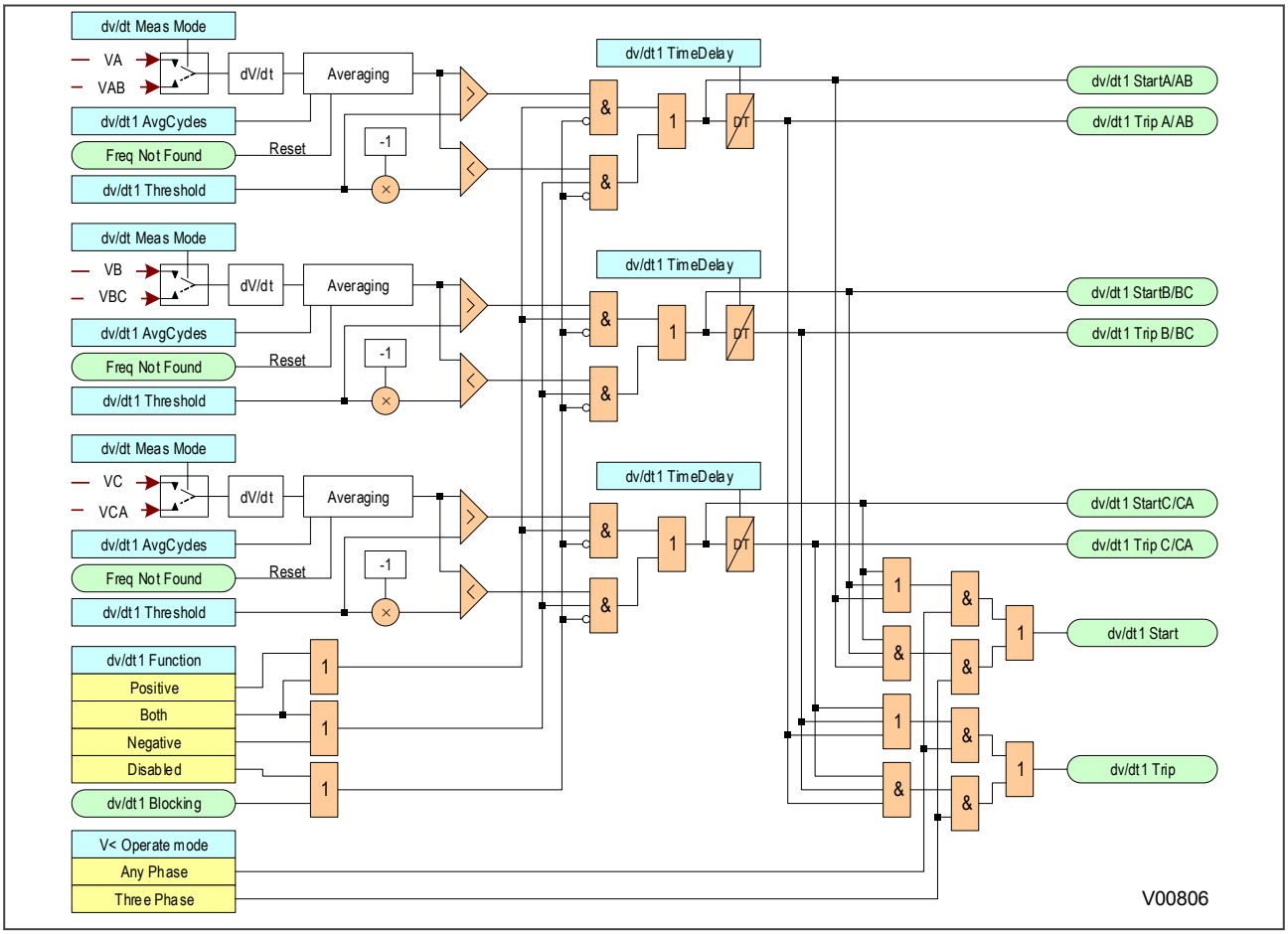


Figure 99: Rate of Change of Voltage protection logic

The dv/dt logic works by differentiating the RMS value of each phase voltage input, which can be with respect to neutral, or respect to another phase depending on the selected measurement mode. This differentiated value is

then averaged over a number of cycles, determined by the setting ***dv/dt1 AvgCycles*** and comparing this with a threshold (***dv/dt1 Threshold***) in both the positive and negative directions. A start signal is produced depending on the selected direction (positive, negative or both), set by the setting ***dv/dt1 Function***, which can also disable the function on a per stage basis. Each stage can also be blocked by the DDB signal ***dv/dt1 Blocking***. The trip signal is produced by passing the Start signal through a DT timer.

The function also produces three-phase Start and Trip signals, which can be set to *Any Phase* (where any of the phases can trigger the start) or *Three Phase* (where all three phases are required to trigger the start). The averaging buffer is reset either when the stage is disabled or no frequency is found (***Freq Not Found*** DDB signal).

5 RESIDUAL OVERVOLTAGE PROTECTION

On a healthy three-phase power system, the sum of the three-phase to earth voltages is nominally zero, as it is the vector sum of three balanced vectors displaced from each other by 120°. However, when an earth fault occurs on the primary system, this balance is upset and a residual voltage is produced. This condition causes a rise in the neutral voltage with respect to earth. Consequently this type of protection is also commonly referred to as 'Neutral Voltage Displacement' or NVD for short.

This residual voltage may be derived (from the phase voltages) or measured (from a measurement class open delta VT). Derived values will normally only be used where the model does not support measured functionality (a dedicated measurement class VT). If a measurement class VT is used to produce a measured Residual Voltage, it cannot be used for other features such as Check Synchronisation.

This offers an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balanced current transformers on each feeder may be either impractical, or uneconomic, or for providing earth fault protection for devices with no current transformers.

5.1 RESIDUAL OVERVOLTAGE PROTECTION IMPLEMENTATION

Residual Overvoltage Protection is implemented in the *RESIDUAL O/V NVD* column of the relevant settings group.

Some applications require more than one stage. For example an insulated system may require an alarm stage and a trip stage. It is common in such a case for the system to be designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The product provides three stages of Residual Overvoltage protection with independent time delay characteristics.

Stages 1 and 3 provide a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- A range of user-defined curves
- DT (Definite Time)

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K= Time multiplier setting
- t = Operating time in seconds
- M = Derived residual voltage setting voltage (***VN> Voltage Set***)

You set this using the ***VN>1 Function*** and ***VN>3 Function*** cells depending on the stage.

Stages 1 and 3 also provide a Timer Hold facility as described in Timer Hold facility (on page82)

Stage 2 can have definite time characteristics only. This is set in the ***VN>2 status*** cell

The residual voltage may be derived from the phase voltages (Vres = Va + Vb +Vc) or measured from the 4th VT input.

In the *CT AND VT RATIOS* column, the ***VN Input*** setting may be set to `Measured` or `Derived`, this is used to select the type of neutral voltage.

The device derives the residual voltage internally from the three-phase voltage inputs supplied from either a 5-limb VT or three single-phase VTs. These types of VT design provide a path for the residual flux and consequently permit

the device to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. Three-limb VTs have no path for residual flux and are therefore unsuitable for this type of protection.

5.2 RESIDUAL OVERVOLTAGE LOGIC

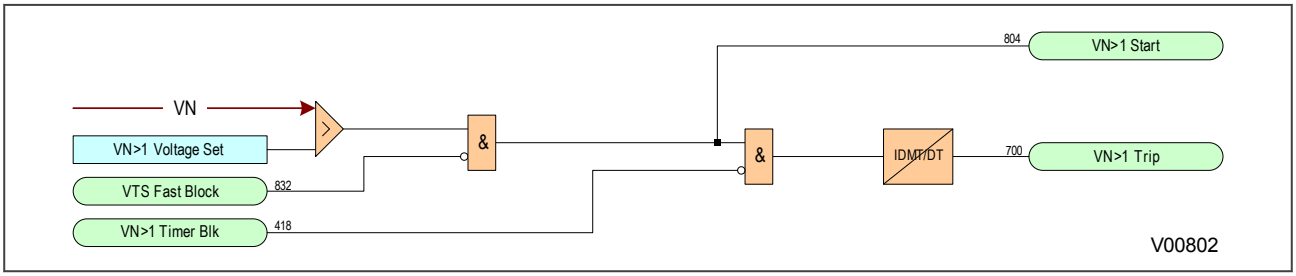


Figure 100: Residual Overvoltage logic

The Residual Overvoltage module (VN>) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***VN>(n) Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***VN> (n) Trip*** signal which is used to drive the tripping output relay.

5.3 APPLICATION NOTES

5.3.1 CALCULATION FOR SOLIDLY EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

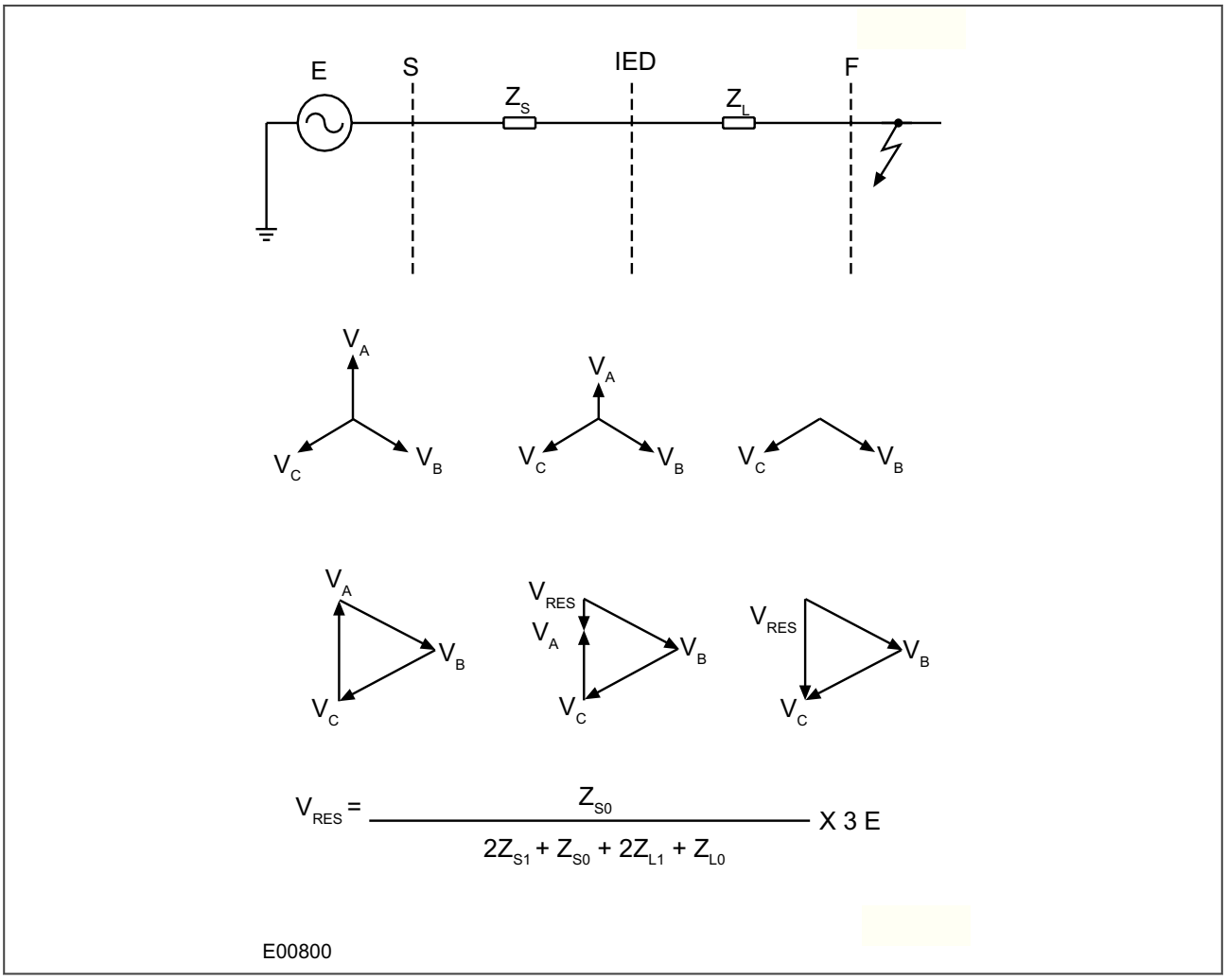


Figure 101: Residual voltage for a solidly earthed system

As can be seen from the above diagram, the residual voltage measured on a solidly earthed system is solely dependent on the ratio of source impedance behind the protection to the line impedance in front of the protection, up to the point of fault. For a remote fault far away, the Z_S/Z_L: ratio will be small, resulting in a correspondingly small residual voltage. Therefore, the protection only operates for faults up to a certain distance along the system. The maximum distance depends on the device setting.

5.3.2 CALCULATION FOR IMPEDANCE EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

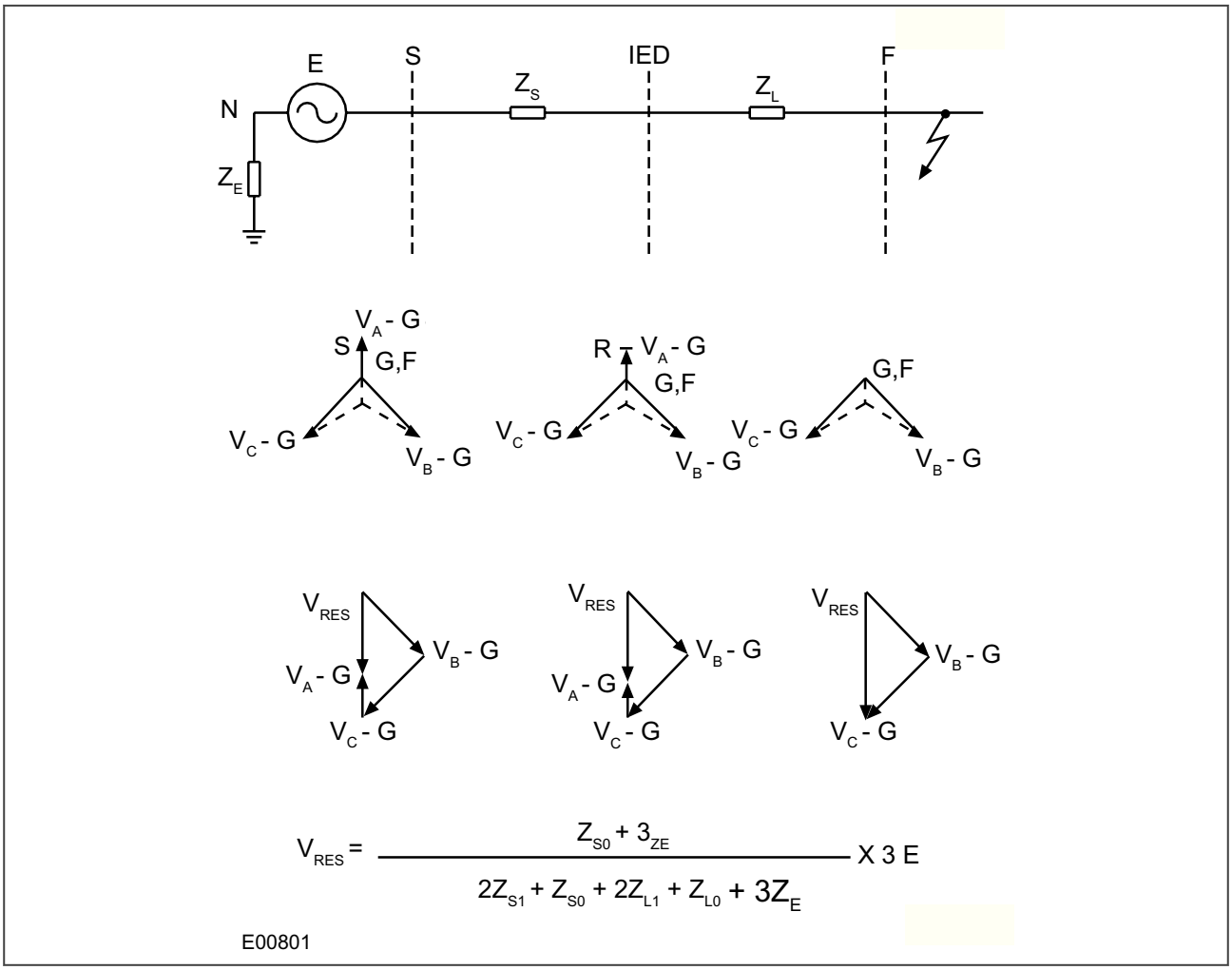


Figure 102: Residual voltage for an impedance earthed system

An impedance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

5.3.3 NEUTRAL VOLTAGE DISPLACEMENT (NVD) PROTECTION APPLIED TO CONDENSER BUSHINGS (CAPACITOR CONES)

Voltage Transformers are not fitted at distribution levels, due to their expense. Instead, capacitor cones, or condenser bushings, may be used at 11kV and 33kV substations to provide a neutral voltage displacement output to a suitable protection device.

Often, bushings are starred together, and the star point used to provide the displacement voltage to the device, as seen in the diagram, below.

Warning:
As protection method requires the device to be placed in a primary circuit location, all relevant safety measures must be in place.

Warning:
When operating in areas with restricted space, suitable protective barriers must be used where there is a risk of electric shock due to exposed terminals.

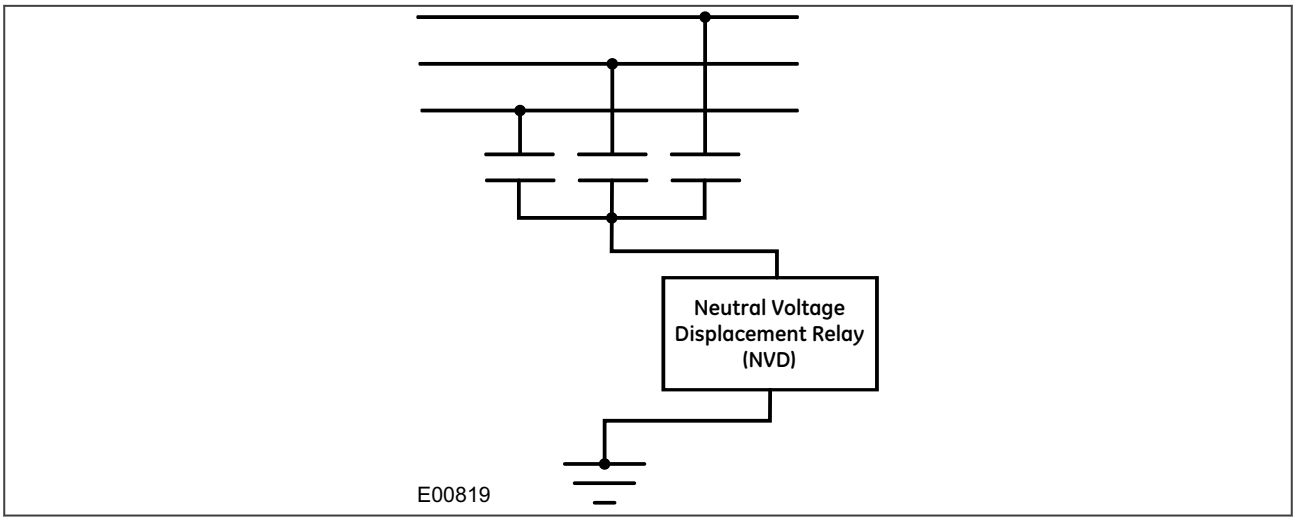


Figure 103: Star connected condenser bushings

Calculations for Condenser Bushing Systems

Consider a single-phase fault to ground on B-Phase:

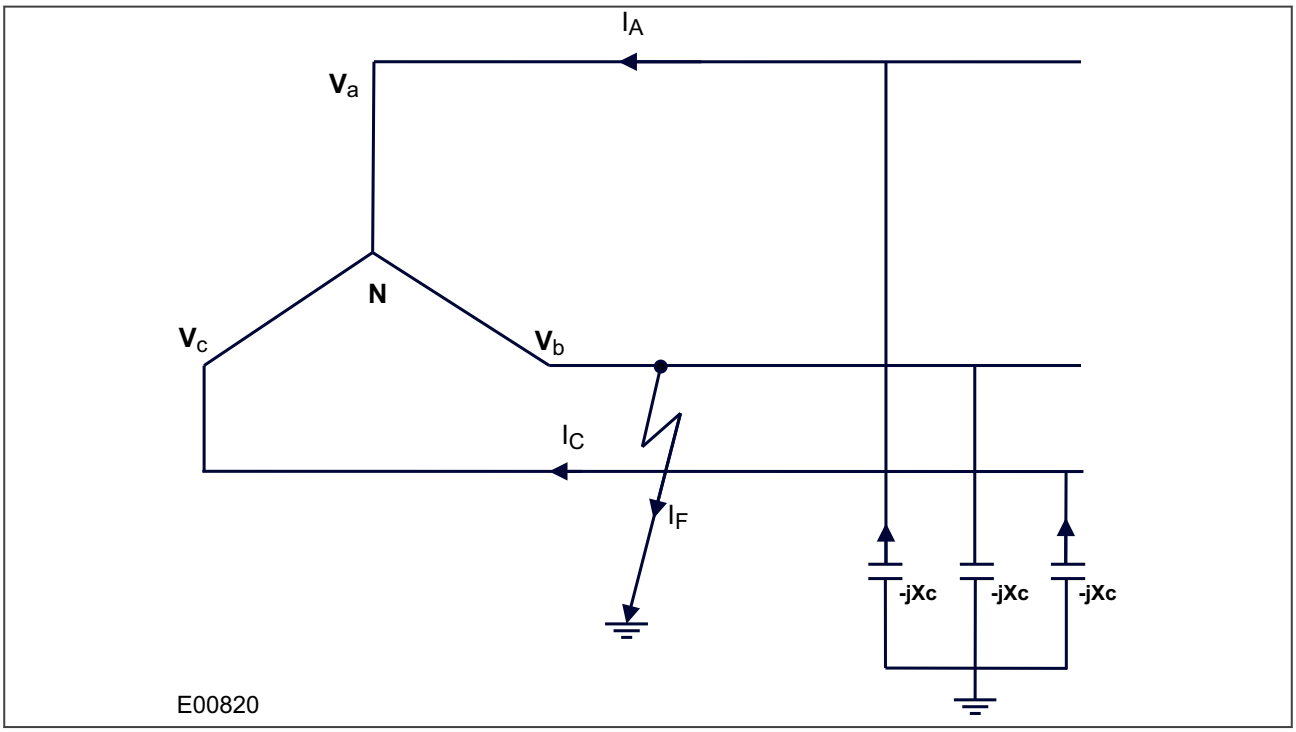


Figure 104: Theoretical earth fault in condenser bushing system

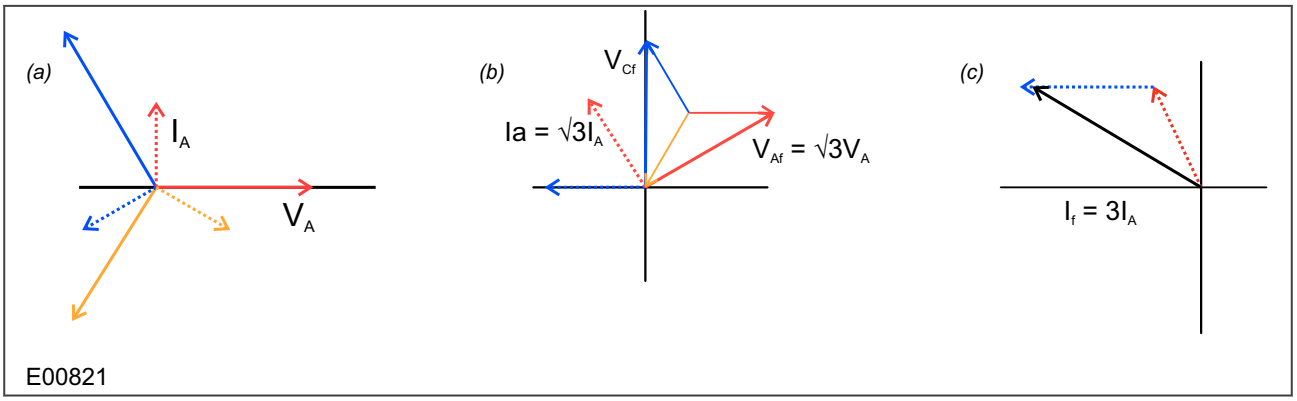


Figure 105: Condenser bushing system vectors

In the figure above:

(a) Shows three healthy voltages, three capacitor currents that lead their respective voltages by 90° and sum to zero,

(b) Shows B phase earthed, A and C voltages are √3 times their healthy magnitude & at 60° to each other, giving correspondingly altered capacitor currents Ia and Ic.

The vector sum of the A & C phase capacitor currents is:

$I_f = \sqrt{3} \times Ia$,

$= \sqrt{3} \times \sqrt{3} \times I_A$,

$= 3 \times I_A$

Therefore, the total fault current I_f equals three times a single capacitor healthy condition current I_A.

(c) Shows the vector sum of the fault condition I_f.

Therefore, I_f is the current which will flow in the Neutral Displacement Relay under fault conditions (neglecting the impedance of the relay itself).

For example, for a 60pF capacitor on a 33kV system, the single capacitor healthy condition current I_A is given by:

$I_A = V_A / X_C$

$= V_A / (1/2\pi fC)$

$= \frac{33 \times 10^3}{\sqrt{3}} / (1/(2 \times \pi \times 50 \times 60 \times 10^{-12}))$

$= 0.359mA$

Therefore, the total fault current which would flow in an NVD relay (neglecting the impedance of the relay itself):

$I_f = 3 \times 0.359 = 1.08mA$

The table below shows the total fault current I_f for a 60pF capacitor, and also I_f for a 90pF capacitor, and for a 150pF capacitor.

C (pF)	60.00	90.00	150.00
Xc (MΩ)	53.08	35.39	21.23
VA (kV)	19.00	19.00	19.00
IA (mA)	0.359	0.539	0.898
If (mA)	1.08	1.62	2.69

Where If is the total fault current which would flow in an NVD relay (neglecting the impedance of the relay itself), then knowing this current (If) and the input impedance of the relay (Rr) we can calculate the voltage produced across it (Vr) during a fault condition:

Vr = If x Rr

Therefore, we would recommend setting the relay to less than half this voltage:

Vs < Vr/2

Practical Application

In practice, the device's input impedance varies with voltage, which will have some effect on actual settings. Therefore, we recommend the use a 23½kΩ resistor combination in parallel with this input, to fix the impedance. This value is achieved by the use of two 47kΩ resistors in parallel. Utilising two resistors in parallel also gives increased security.

The resistors used must have a continuous working voltage rating of 5kVdc minimum and a minimum power rating of 1W.

Warning:
There is the risk of high voltage developing on removal of the device or PCB from its case. Fixed resistors on the device input will prevent this, but we would also recommend use of an externally connected shorting contact.

Note:
A suitable shorting contact is available on each device. Please see diagram, below.

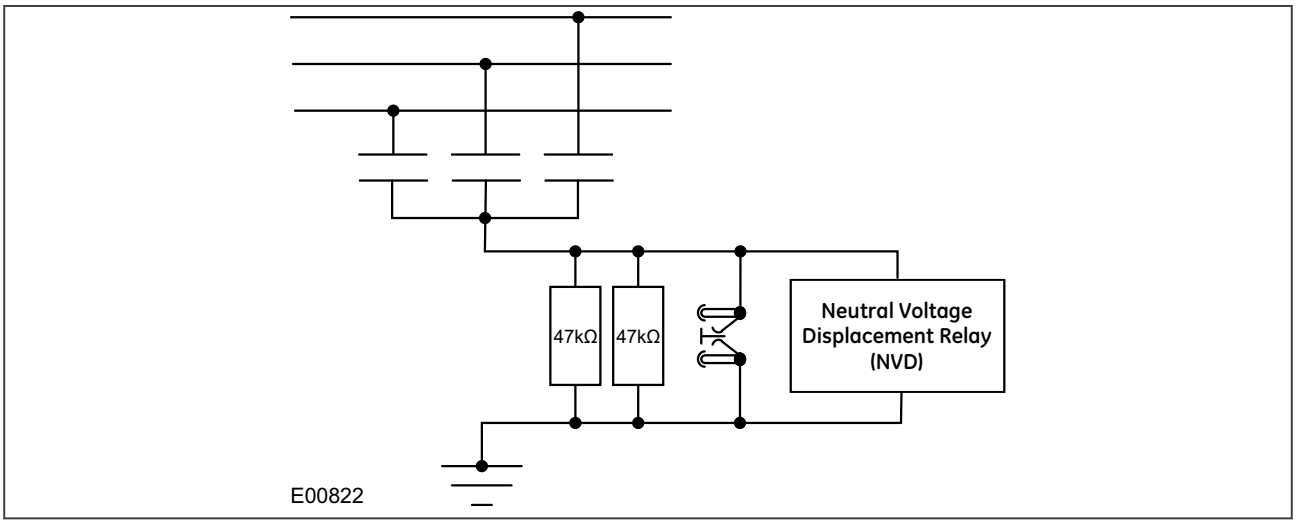


Figure 106: Device connection with resistors and shorting contact

Voltage Setting

The device has a minimum setting on the residual OV/NVD of 1V, which should provide a sensitive enough setting for most applications. The operating voltage to be applied can be calculated for various capacitor ratings, shown in calculations provided above.

For maximum settings for various capacitors (assuming 23½kΩ resistance applied in conjunction with the device), see the table below.

C (pF)	60.00	90.00	150.00
Xc (MΩ)	53.08	35.39	21.23

VA (kV)	19.00	19.00	19.00
If (mA)	1.08	1.62	2.69
Rr (kΩ)*	22.00	22.00	22.00
Vr (V)	23.63	35.44	59.06
Vs (V)	11.81	17.72	29.53

*Relay and Resistor Combination

Wiring Diagram

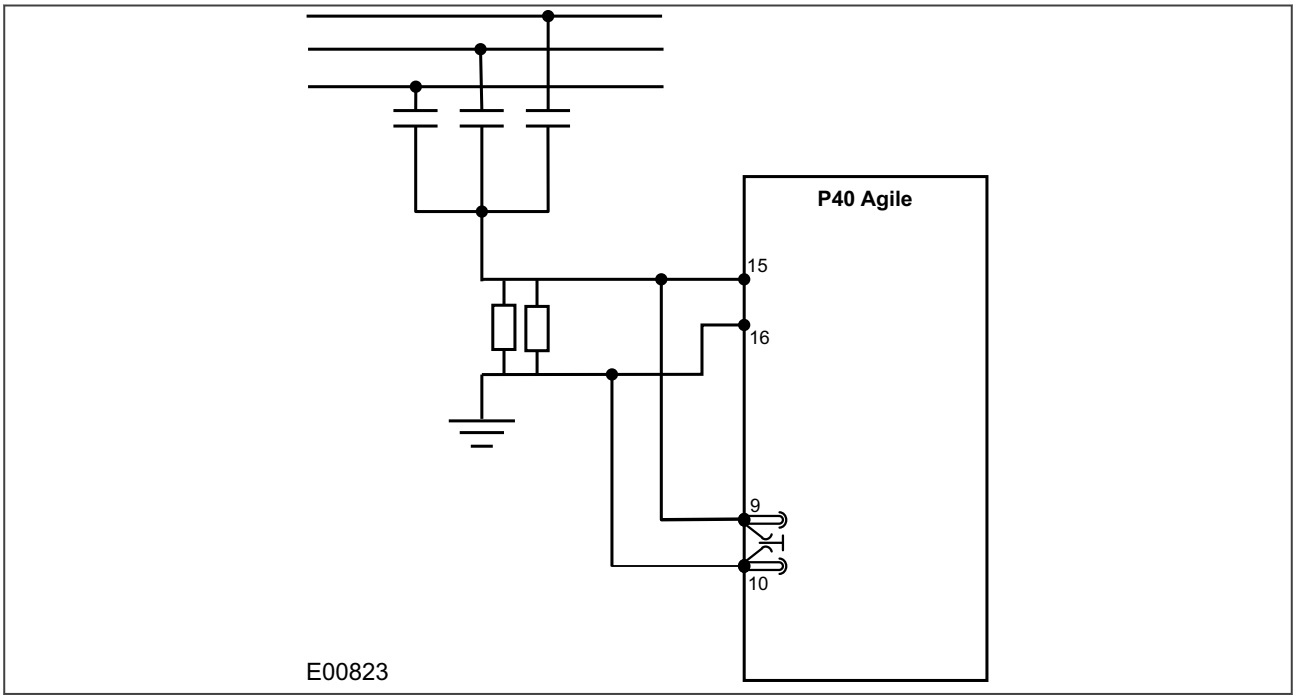


Figure 107: Device connection P14D

5.3.4 SETTING GUIDELINES

The voltage setting applied to the elements is dependent on the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependent on the method of system earthing employed.

Also, you must ensure that the protection setting is set above any standing level of residual voltage that is present on the system.

6 NEGATIVE SEQUENCE OVERVOLTAGE PROTECTION

Where an incoming feeder is supplying rotating plant equipment such as an induction motor, correct phasing and balance of the supply is essential. Incorrect phase rotation will result in connected motors rotating in the wrong direction. For directionally sensitive applications, such as elevators and conveyor belts, it is unacceptable to allow this to happen.

Imbalances on the incoming supply cause negative phase sequence voltage components. In the event of incorrect phase rotation, the supply voltage would effectively consist of 100% negative phase sequence voltage only.

6.1 NEGATIVE SEQUENCE OVERVOLTAGE IMPLEMENTATION

Negative Sequence Overvoltage Protection is implemented in the *NEG SEQUENCE O/V* column of the relevant settings group.

The device includes one Negative Phase Sequence Overvoltage element with two stages. Only Definite time is possible.

This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer) and may be interlocked with the motor contactor or circuit breaker to prevent the motor from being energised whilst incorrect phase rotation exists.

The element is enabled using the ***V2>1 status*** and ***V2>2 status*** cells.

6.2 NEGATIVE SEQUENCE OVERVOLTAGE LOGIC

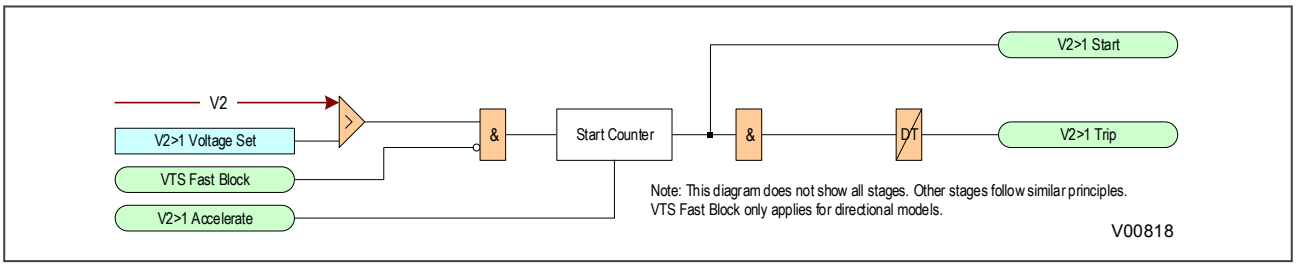


Figure 108: Negative Sequence Overvoltage logic

The Negative Voltage Sequence Overvoltage module detects when the voltage magnitude exceeds a set threshold. When this happens, the comparator output Overvoltage Module produces a ***Start*** signal (e.g. for stage 1: ***V2>1 Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the DT timer module. The output of the DT timer module is the trip signal which is used to drive the tripping output relay.

The ***V2>1 Accelerate*** signal accelerates the operating time of the function, by reducing the number of confirmation cycles needed to start the function. At 50 Hz, this means the protection Start is reduced by 20 ms.

6.3 APPLICATION NOTES

6.3.1 SETTING GUIDELINES

The primary concern is usually the detection of incorrect phase rotation (rather than small imbalances), therefore a sensitive setting is not required. The setting must be higher than any standing NPS voltage, which may be present due to imbalances in the measuring VT, device tolerances etc.

A setting of approximately 15% of rated voltage may be typical.

Note:
*Standing levels of NPS voltage (V2) are displayed in the **V2 Magnitude** cell of the MEASUREMENTS 1 column.*

The operation time of the element depends on the application, but a typical setting would be in the region of 5 seconds.

7 POSITIVE SEQUENCE UNDERVOLTAGE PROTECTION

7.1 POSITIVE SEQUENCE UNDERVOLTAGE IMPLEMENTATION

Positive Sequence Undervoltage Protection is implemented under the *POS SEQ U/V* heading in the *VOLT PROTECTION* Voltage column of the relevant settings group.

The product provides two stages of Positive Sequence Undervoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V1<1 Function*** cell.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage

There is no Timer Hold facility for Undervoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V1<2*** status cell.

Two stages are included in order to provide multiple output types, such as alarm and trip stages.

7.2 POSITIVE SEQUENCE UNDERVOLTAGE LOGIC

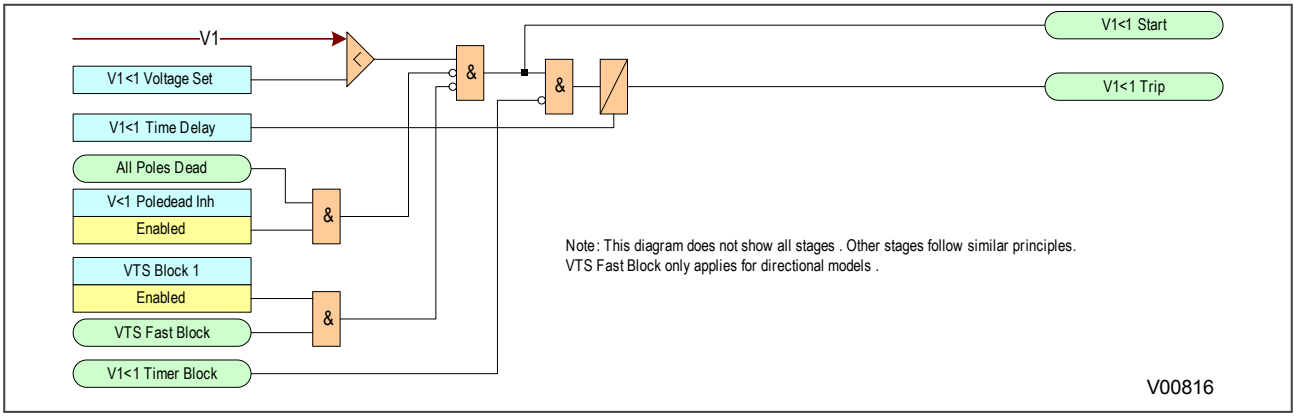


Figure 109: Positive Sequence Undervoltage logic

8 POSITIVE SEQUENCE OVERVOLTAGE PROTECTION

8.1 POSITIVE SEQUENCE OVERVOLTAGE IMPLEMENTATION

Positive Sequence Overvoltage Protection is implemented under the *POS SEQ O/V* heading in the *VOLT PROTECTION* Voltage column of the relevant settings group.

The product provides two stages of Positive Sequence Overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V1>1 Function*** cell.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage

There is no Timer Hold facility for Positive Sequence Overvoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V1>2 status*** cell.

Two stages are included in order to provide multiple output types, such as alarm and trip stages.

8.2 POSITIVE SEQUENCE OVERVOLTAGE LOGIC

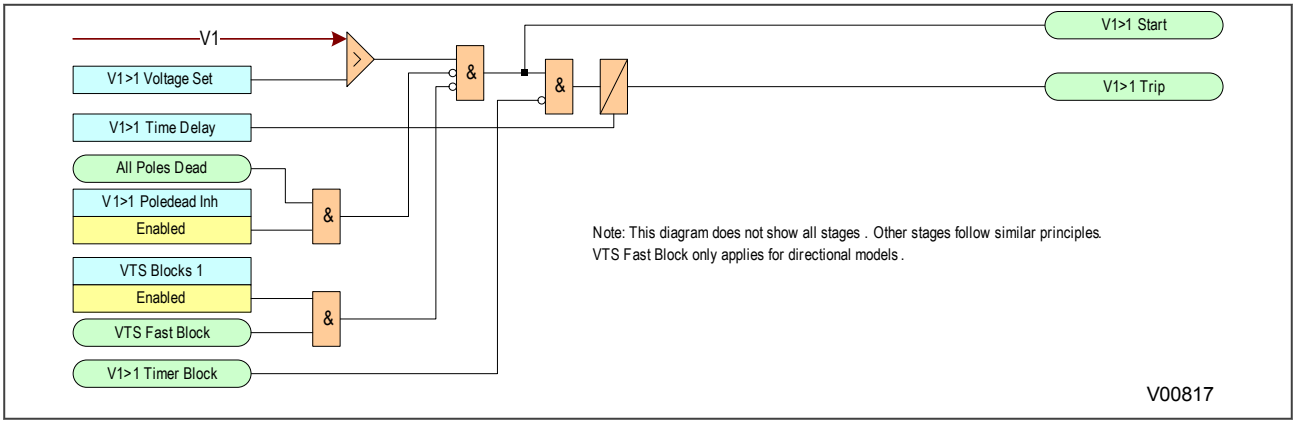


Figure 110: Positive Sequence Overvoltage logic

9 MOVING AVERAGE VOLTAGE FUNCTIONS

Moving average voltage functions are available for:

- Undervoltage (Vavg<)
- Overvoltage (Vavg>)
- Zero Sequence Voltage (V0avg>)
- Positive Sequence Voltage (V1Avg>)
- Negative Sequence Voltage (V2Avg>)

The voltage is sampled at 5 Hz (one sample every 200 ms for a 50 Hz system). The refresh period is 3 seconds, meaning 15 samples are collected every refresh period. The average voltage for the previous 10 minutes is calculated, displayed as measurements and used as energising quantities for the protection functions. The folllowing quantities are provided:

VA Mov Average: A-phase RMS average voltage

VB Mov Average: B-phase RMS average voltage

VC Mov Average: C-phase RMS average voltage

V0 Mov Average: Zero Sequence average voltage magnitude

V1 Mov Average: Positive Sequence average voltage magnitude

V2 Mov Average: Negative Sequence average voltage magnitude

9.1 MOVING AVERAGE UNDERVOLTAGE LOGIC

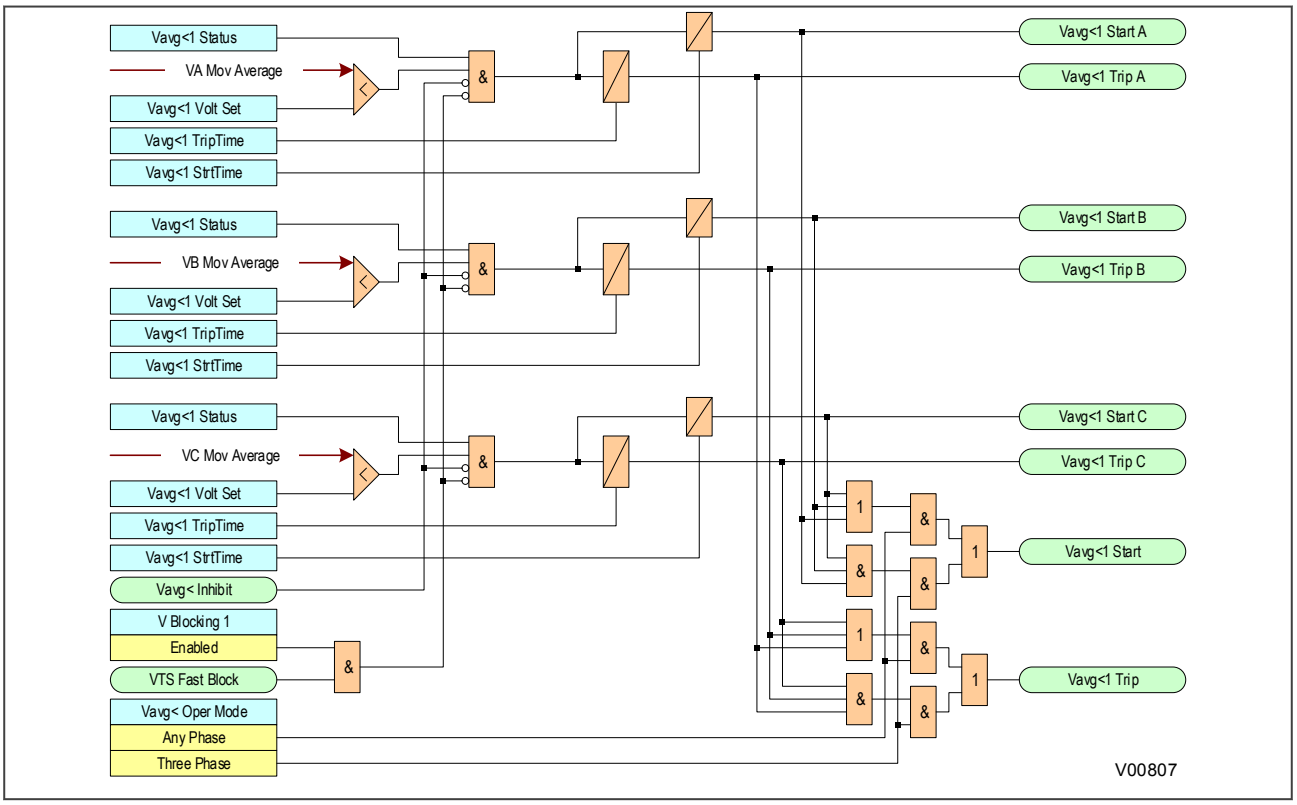


Figure 111: Moving Average undervoltage logic

9.2 MOVING AVERAGE OVERVOLTAGE LOGIC

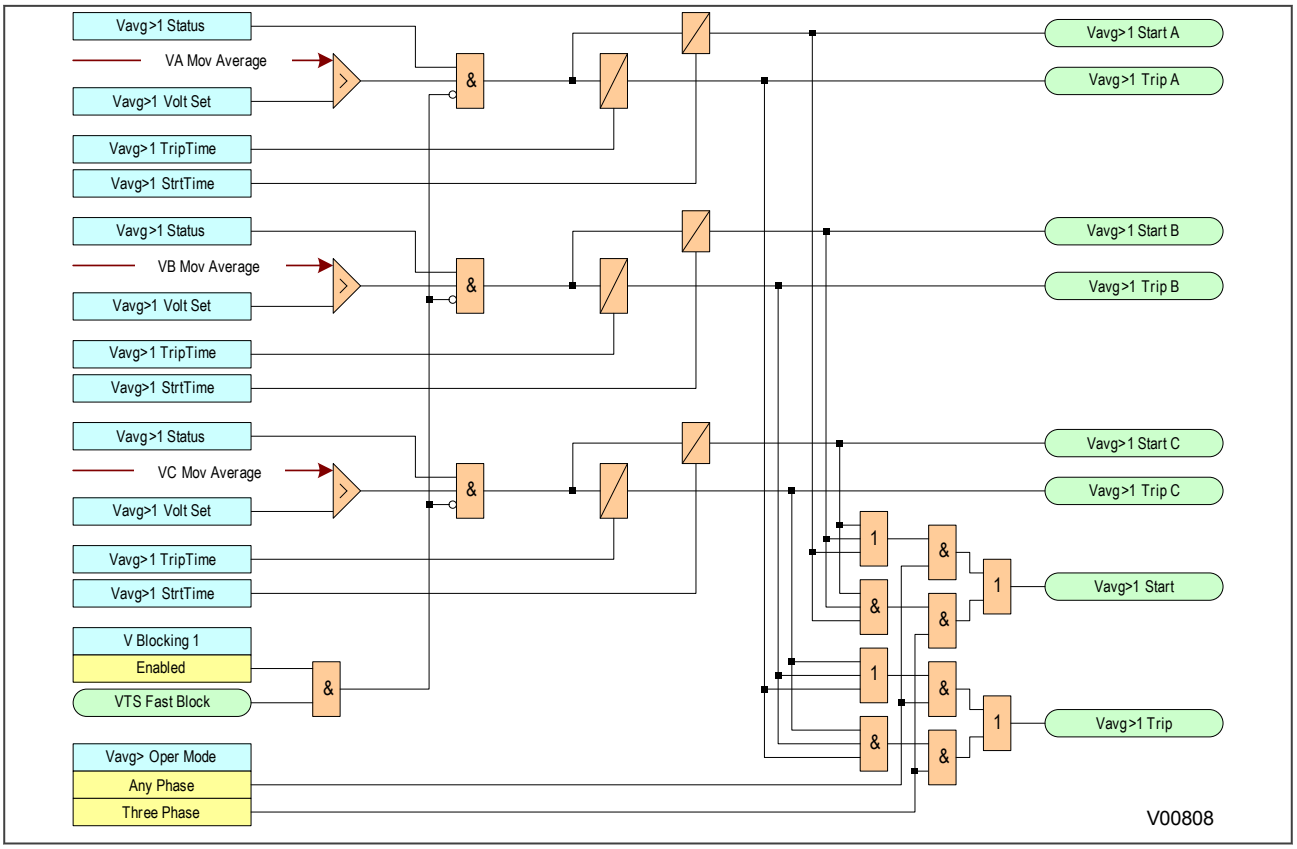


Figure 112: Moving Average overvoltage logic

9.3 MOVING AVERAGE ZERO SEQUENCE VOLTAGE LOGIC

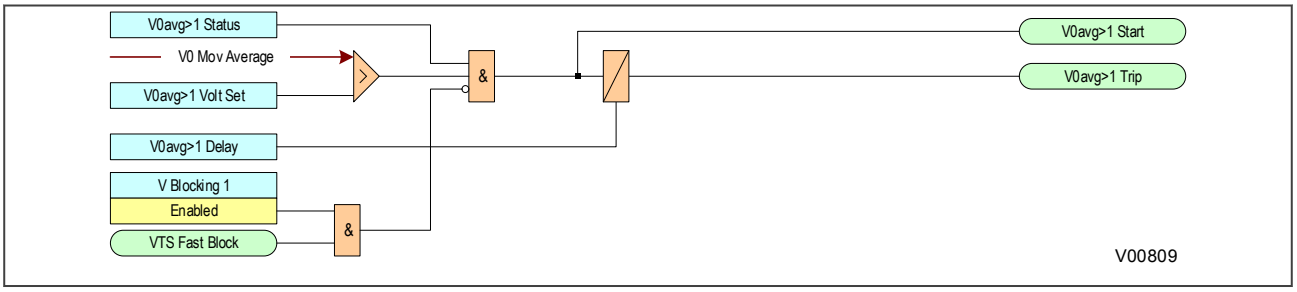


Figure 113: Moving Average zero sequence voltage logic

9.4 MOVING AVERAGE POSITIVE SEQUENCE VOLTAGE LOGIC

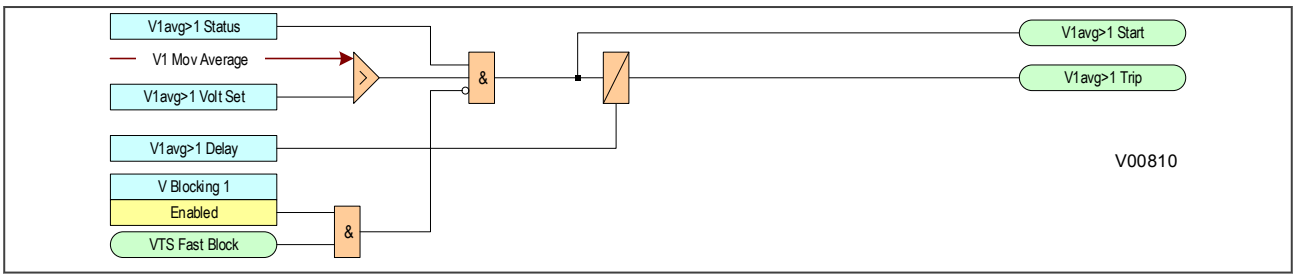


Figure 114: Moving Average positive sequence voltage logic

9.5 MOVING AVERAGE NEGATIVE SEQUENCE VOLTAGE LOGIC

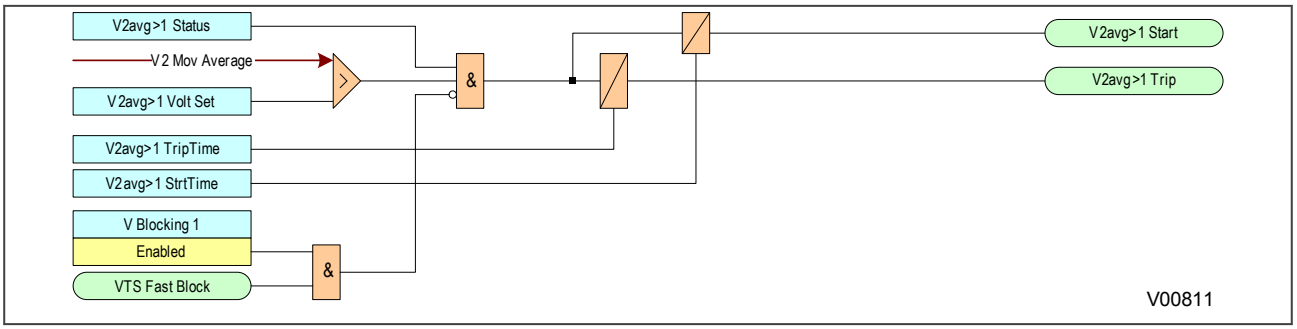


Figure 115: Moving Average negative sequence voltage logic

9.6 MOVING AVERAGE UNDERVOLTAGE BLOCKING PSL

The Moving Average Undervoltage Protection function does not provide internal blocking for Pole Dead conditions. To achieve this you must configure this in PSL as follows:

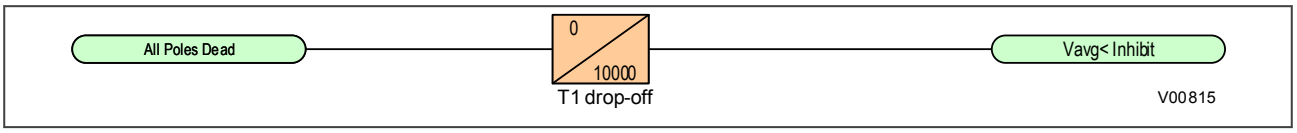


Figure 116: Average Voltage Protection blocking

10 VOLTAGE VECTOR SHIFT PROTECTION

The P14D has a single stage Voltage Vector Shift protection element. This element measures the change in voltage angle over successive power system half-cycles. The element operates by measuring the time between zero crossings on the voltage waveforms. A measurement is taken every half cycle for each phase voltage. Over a power system cycle this produces 6 results, a trip is issued if 5 of the 6 calculations for the last power system cycle are above the set threshold. Checking all three phases makes the element less susceptible to incorrect operation due to harmonic distortion or interference in the measured voltage waveform.

The DDB signal, ***V Shift Trip*** is used to indicate that the element has operated. The state of ***V Shift Trip*** can also be programmed to be viewed in the Monitor Bit x cells of the *COMMISSION TESTS* column.

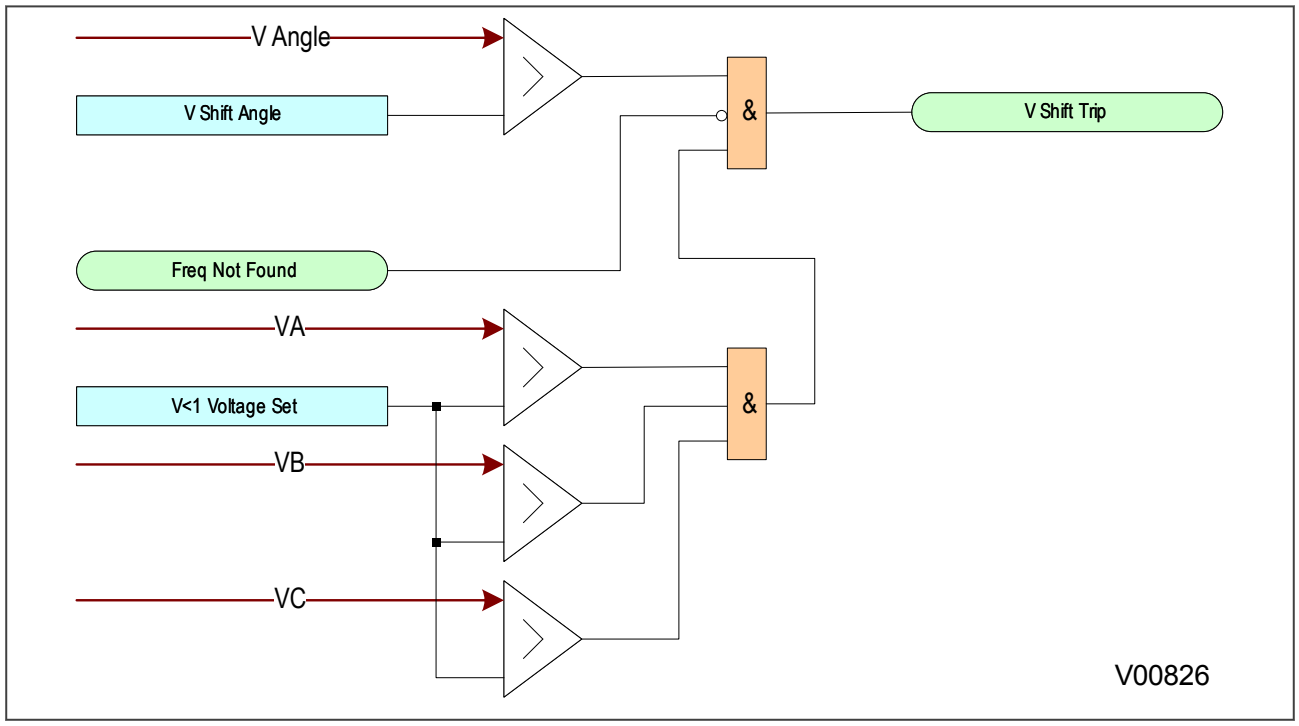


Figure 117: Voltage vector shift logic

10.1 APPLICATION NOTES

10.2 VOLTAGE VECTOR SHIFT CALCULATIONS

The P14D has a single stage Voltage Vector Shift protection element. This element measures the change in voltage angle over successive power system half-cycles. The element operates by measuring the time between zero crossings on the voltage waveforms. A measurement is taken every half cycle for each phase voltage. Over a power system cycle, this produces 6 results, a trip is issued if 5 of the 6 calculations for the last power system cycle are above the set threshold. Checking all three phases makes the element less susceptible to incorrect operation due to harmonic distortion or interference in the measured voltage waveform.

An expression for a sinusoidal mains voltage waveform is generally given by the following:

$V = Vp \sin(wt)$ or $V = Vp \sin \theta(t)$

Where:

$\theta(t) = wt = 2\pi ft$

If the frequency is changing at constant rate Rf from a frequency fo then the variation in the angle □(t) is given by:

$\theta(t) = 2\pi \int f \, dt$,

which gives:

$\theta(t) = 2\pi (f_o t + t R_f t/2)$,

and

$V = V \sin \{2\pi (f_o + t R_f/2)t\}$

Hence the angle change: $\Delta\theta(t)$ after time t is given by:

$\Delta\theta(t) = \pi R_f t^2$

Therefore, the phase of the voltage with respect to a fixed frequency reference when subject to a constant rate of change of frequency changes in proportion to t^2. This is a characteristic difference from a rate of change of frequency function, which in most conditions can be assumed as changing linearly with time.

A rate of change of frequency of 10 Hz/s results in an angular voltage vector shift of only 0.72 degrees in the first cycle after the disturbance. This is too small to be detected by vector shift relays. In fact a typical setting for a voltage vector shift relay is, normally between 6 and 13 degrees. Therefore, a voltage vector shift relay is not sensitive to the change in voltage phase brought about by change of frequency alone.

To understand the relation between the resulting voltage vector angle change following a disturbance and the embedded generator characteristics a simplified single phase equivalent circuit of a synchronous generator or induction generator is shown in the figures below. The voltage VT is the symmetrical terminal voltage of the generator and the voltage E is the internal voltage lying behind the machine impedance which is largely reactive (X). When a disturbance causes a change in current the terminal voltage will jump with respect to its steady state position. The resultant voltage vector is dependent on the rate of change in current, and the subtransient impedance of the machine, which is the impedance the generator presents to a sudden load change. In turn the current change depends on how strong the source is (short circuit capacity) and the voltage regulation at the generator terminal which is also affected by the reactive power load connected to the machine.

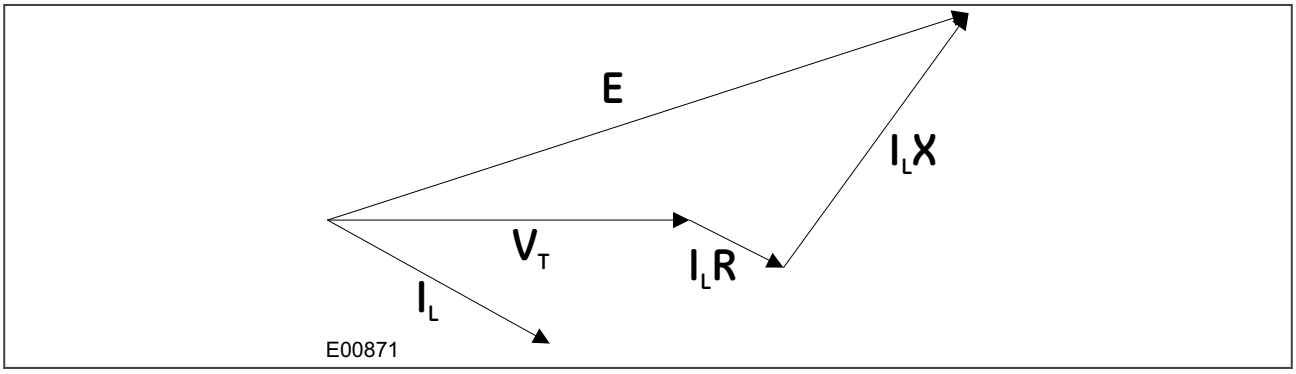


Figure 118: Vector diagram representing steady state condition

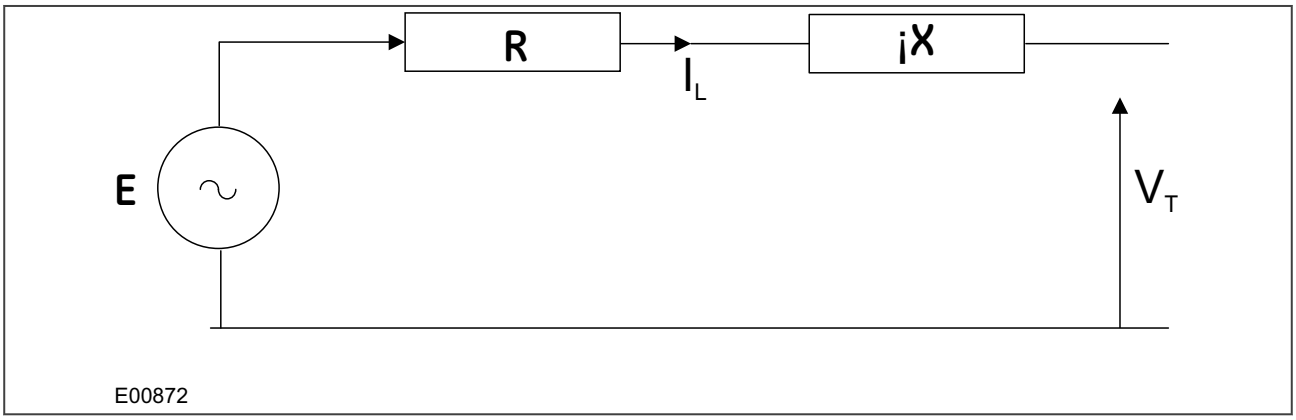


Figure 119: Single phase line diagram showing generator parameters

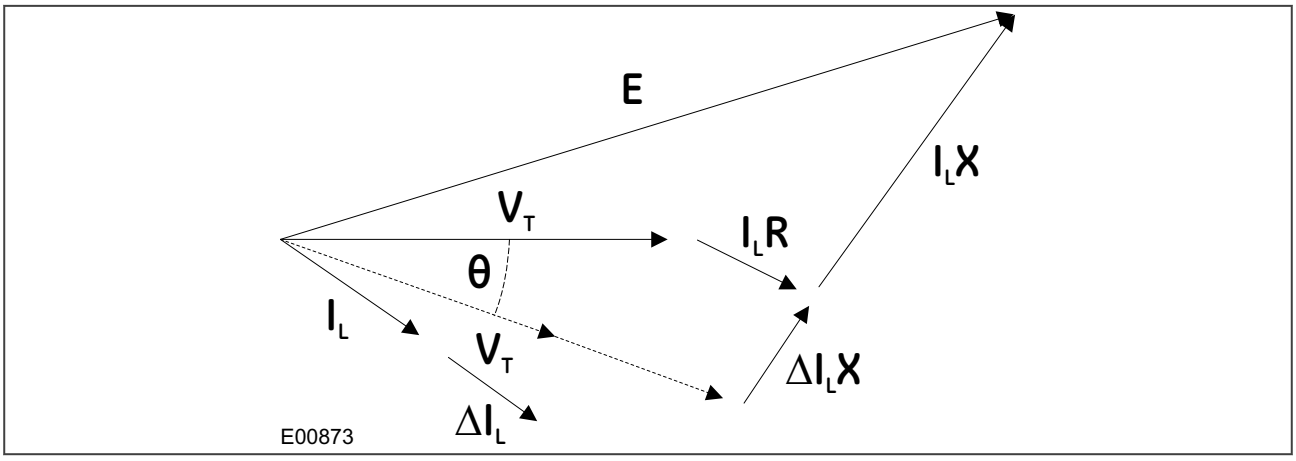


Figure 120: Transient voltage vector change θ due to change in load current $I\Delta_L$

The voltage vector shift function is designed to respond within one to two full mains cycles when its threshold is exceeded. Discrimination between a loss of mains condition and a circuit fault is therefore achievable only by selecting the angle threshold to be above expected fault levels. This setting can be quantified by calculating the angular change due to islanding. However, this angular change depends on system topology, power flows and very often also on the instant of the system faults. For example a bolted three phase short circuit which occurs close to the relay may cause a problem in that it inherently produces a vector shift angle at the instant of the fault which is bigger than any normal setting, independent of the mains condition. This kind of fault would cause the relay to trip shortly after the instant of its inception. Although this may seem to be a disadvantage of the vector shift function, isolating the embedded generator at the instant of a bolted three phase fault is of advantage to the PES. This is because the mains short circuit capacity and consequently the energy feeding the short circuit is limited by the instant operation of the relay. The fast operation of this vector shift function renders it to operate at the instant of a disturbance rather than during a gradual change caused by a gradual change of power flow. Operation can occur at the instant of inception of the fault, at fault clearance or following non-synchronized reclosure, which affords additional protection to the embedded generator.

11 VT CONNECTIONS

11.1 APPLICATION NOTES

11.1.1 OPEN DELTA (VEE CONNECTED) VTS

The P40 Agile range can be used with vee connected VTs by connecting the VT secondaries to 17, 18 and 19 input terminals, with the 20 input left unconnected.

This type of VT arrangement cannot pass zero-sequence (residual) voltage to the relay, or provide any phase to neutral voltage quantities. Therefore any protection that is dependent upon phase to neutral voltage measurements should be disabled.

The under and over voltage protection can be set as phase-to-phase measurement with vee connected VTs. The voltage dependent overcurrent use phase-phase voltages anyway, therefore the accuracy should not be affected. Directional earth fault and sensitive directional earth fault protection should be disabled as the neutral voltage will always be zero, even in the event of an earth fault. CT supervision should also be disabled as this is also dependent upon the measurement of zero sequence voltage.

The accuracy of single phase voltage measurements can be impaired when using vee connected VTs. The relay attempts to derive the phase to neutral voltages from the phase to phase voltage vectors. If the impedance of the voltage inputs were perfectly matched the phase to neutral voltage measurements would be correct, provided the phase to phase voltage vectors were balanced. However, in practice there are small differences in the impedance of the voltage inputs, which can cause small errors in the phase to neutral voltage measurements. This may give rise to an apparent residual voltage. This problem also extends to single phase power measurements that are also dependent upon their respective single phase voltages.

The phase to neutral voltage measurement accuracy can be improved by connecting three, well matched, load resistors between the phase voltage inputs (17, 18, 19) and neutral 20, thus creating a ‘virtual’ neutral point. The load resistor values must be chosen so that their power consumption is within the limits of the VT. It is recommended that 10kΩ ±1% (6W) resistors are used for the 110V (Vn) rated relay, assuming the VT can supply this burden.

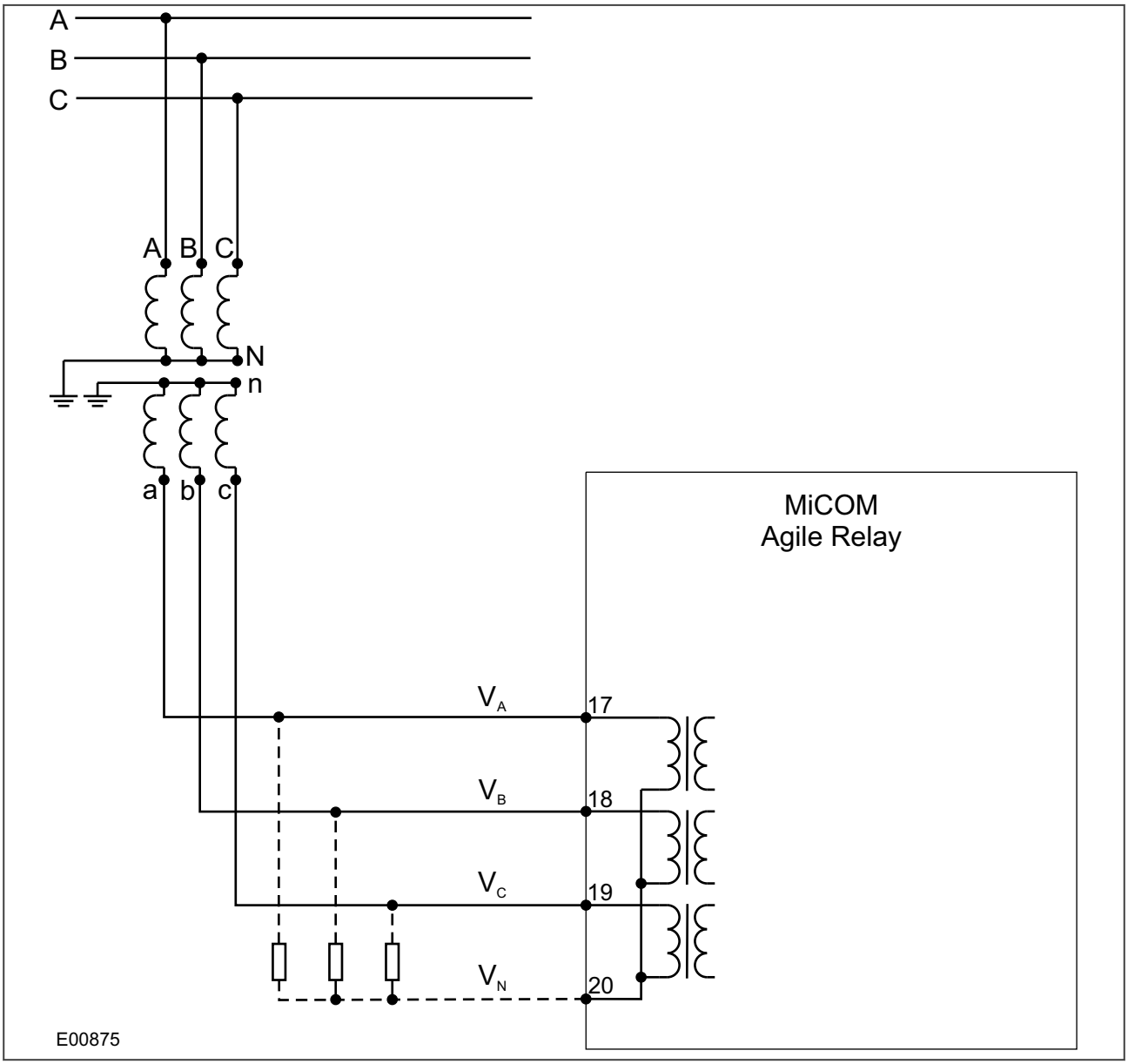


Figure 121: Virtual neutral point connected VTs

11.1.2 VT SINGLE POINT EARTHING

The P40 Agile range will function correctly with conventional 3-phase VTs earthed at any one point on the VT secondary circuit. Typical earthing examples being neutral earthing and yellow phase earthing.

CHAPTER 11

FREQUENCY PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

The device provides a range of frequency protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

2 FREQUENCY PROTECTION OVERVIEW

Power generation and utilisation needs to be well balanced in any industrial, distribution or transmission network. These electrical networks are dynamic entities, with continually varying loads and supplies, which are continually affecting the system frequency. Increased loading reduces the system frequency and generation needs to be increased to maintain the frequency of the supply. Conversely decreased loading increases the system frequency and generation needs to be reduced. Sudden fluctuations in load can cause rapid changes in frequency, which need to be dealt with quickly.

Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse, which has dire consequences.

Protection devices capable of detecting low frequency conditions are generally used to disconnect unimportant loads in order to re-establish the generation-to-load balance. However, with such devices, the action is initiated only after the event and this form of corrective action may not be effective enough to cope with sudden load increases that cause large frequency decays in very short times. In such cases a device that can anticipate the severity of frequency decay and act to disconnect loads before the frequency reaches dangerously low levels, are very effective in containing damage. This is called instantaneous rate of change of frequency protection (ROCOF).

During severe disturbances, the frequency of the system oscillates as various generators try to synchronise to a common frequency. The measurement of instantaneous rate of change of frequency can be misleading during such a disturbance. The frequency decay needs to be monitored over a longer period of time to make the correct decision for load shedding. This is called average rate of change of frequency protection.

Normally, generators are rated for a particular band of frequency. Operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken. This type of protection can be used for operator alarms or turbine trips in case of severe frequency decay.

2.1 FREQUENCY PROTECTION IMPLEMENTATION

Frequency Protection is implemented in the *FREQ PROTECTION* column of the relevant settings group.

The device includes 9 stages for the following frequency protection methods:

- Underfrequency Protection: abbreviated to f+t<
- Overfrequency Protection: abbreviated to f+t>
- Independent Rate of Change of Frequency Protection: abbreviated to Independent R.O.C.O.F, or df/dt+t
- Frequency-supervised Rate of Change of Frequency Protection: abbreviated to Frequency-supervised R.O.C.O.F, or f+df/dt
- Average Rate of Change of Frequency Protection: abbreviated to Average R.O.C.O.F, or f+Df/Dt (note the uppercase 'D')
- Load Shedding and Restoration

Each stage can be disabled or enabled with the ***Stage (n)*** setting. The frequency protection can also be blocked by an undervoltage condition if required.

3 UNDERFREQUENCY PROTECTION

A reduced system frequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the capacity of the generators in that particular subsystem. Industrial plants that are dependent on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

Many types of industrial loads have limited tolerances on the operating frequency and running speeds (e.g. synchronous motors). Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may damage equipment and even lead to blackouts. It is therefore essential to provide protection for underfrequency conditions.

3.1 UNDERFREQUENCY PROTECTION IMPLEMENTATION

The following settings are relevant for underfrequency:

- ***Stg (n) f+t Status***: determines whether the stage is underfrequency, overfrequency, or disabled
- ***Stg (n) f+t Freq***: defines the frequency pickup setting
- ***Stg (n) f+t Time***: sets the time delay

3.2 UNDERFREQUENCY PROTECTION LOGIC

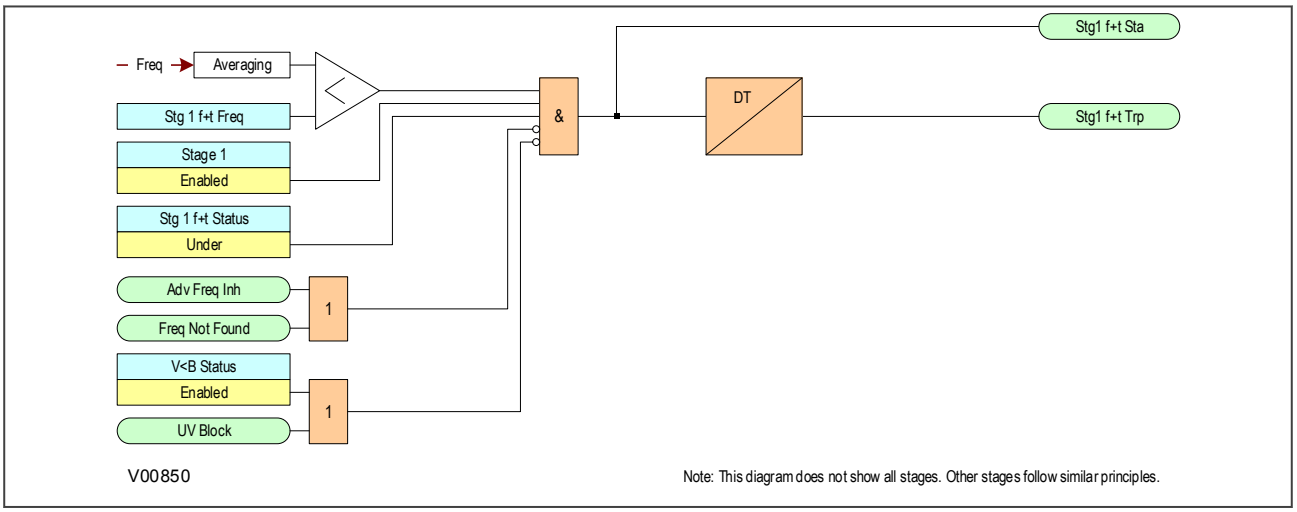


Figure 122: Underfrequency logic (single stage)

If the frequency is below the setting and not blocked the DT timer is started. If the frequency cannot be determined, the function is blocked.

3.3 APPLICATION NOTES

3.3.1 SETTING GUIDELINES

In order to minimise the effects of underfrequency, a multi-stage load shedding scheme may be used with the plant loads prioritised and grouped. During an underfrequency condition, the load groups are disconnected sequentially, with the highest priority group being the last one to be disconnected.

The effectiveness of each load shedding stage depends on the proportion of power deficiency it represents. If the load shedding stage is too small compared with the prevailing generation deficiency, then there may be no improvement in the frequency. This should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. These should not be excessive as this could jeopardize system stability. Time delay settings of 5 - 20 s are typical.

An example of a four-stage load shedding scheme for 50 Hz systems is shown below:

Stage	Element	Frequency Setting (Hz)	Time Setting (Sec)
1	Stage 1(f+t)	49.0	20 s
2	Stage 2(f+t)	48.6	20 s
3	Stage 3(f+t)	48.2	10 s
4	Stage 4(f+t)	47.8	10 s

The relatively long time delays are intended to provide sufficient time for the system controls to respond. This will work well in a situation where the decline of system frequency is slow. For situations where rapid decline of frequency is expected, this load shedding scheme should be supplemented by rate of change of frequency protection elements.

4 OVERFREQUENCY PROTECTION

An increased system frequency arises when the mechanical power input to a generator exceeds the electrical power output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such conditions, the governor would normally respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Overfrequency protection is required as a backup to cater for cases where the reaction of the control equipment is too slow.

4.1 OVERFREQUENCY PROTECTION IMPLEMENTATION

The following settings are relevant for overfrequency:

- ***Stg (n) f+t Status***: determines whether the stage is underfrequency, overfrequency, or disabled
- ***Stg (n) f+t Freq***: defines the frequency pickup setting
- ***Stg (n) f+t Time***: sets the time delay

4.2 OVERFREQUENCY PROTECTION LOGIC

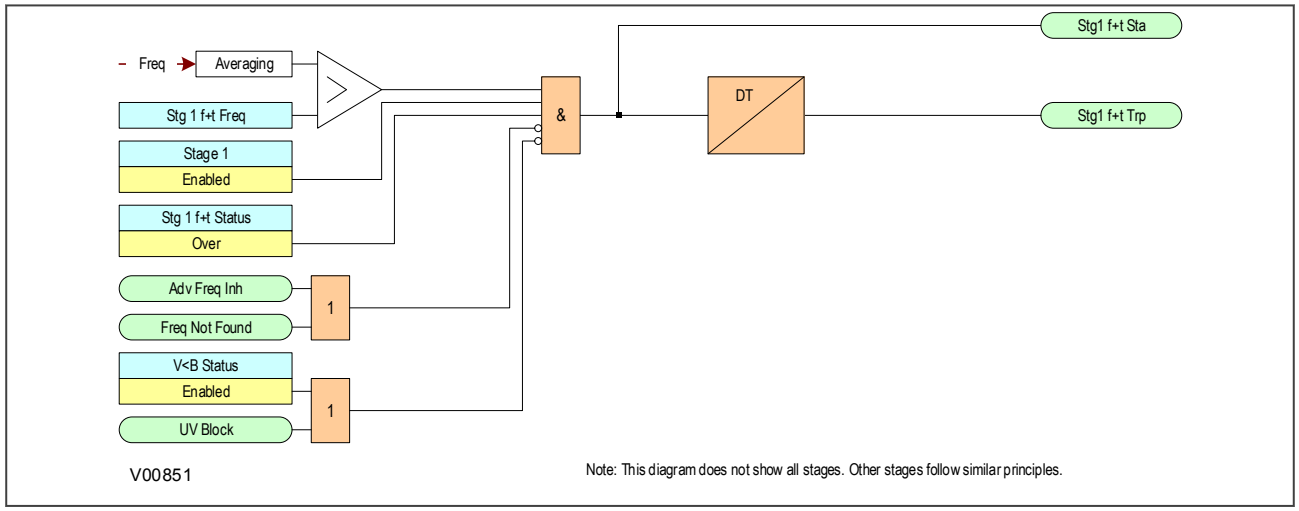


Figure 123: Overfrequency logic (single stage)

If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out, the trip is produced. If the frequency cannot be determined, the function is blocked.

4.3 APPLICATION NOTES

4.3.1 SETTING GUIDELINES

Following changes on the network caused by faults or other operational requirements, it is possible that various subsystems will be formed within the power network. It is likely that these subsystems will suffer from a generation/load imbalance. The "islands" where generation exceeds the existing load will be subject to overfrequency conditions. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element can be suitably set to sense this contingency.

An example of two-stage overfrequency protection is shown below using stages 5 and 6 of the f+t elements. However, settings for a real system will depend on the maximum frequency that equipment can tolerate for a given period of time.

Stage	Element	Frequency Setting (Hz)	Time Setting (Sec.)
1	Stage 5(f+t)	50.5	30
2	Stage 6(f+t)	51.0	20

The relatively long time delays are intended to provide time for the system controls to respond and will work well in a situation where the increase of system frequency is slow.

For situations where rapid increase of frequency is expected, the protection scheme above could be supplemented by rate of change of frequency protection elements.

In the system shown below, the generation in the MV bus is sized according to the loads on that bus, whereas the generators linked to the HV bus produce energy for export to utility. If the links to the grid are lost, the generation will cause the system frequency to rise. This rate of rise could be used to isolate the MV bus from the HV system.

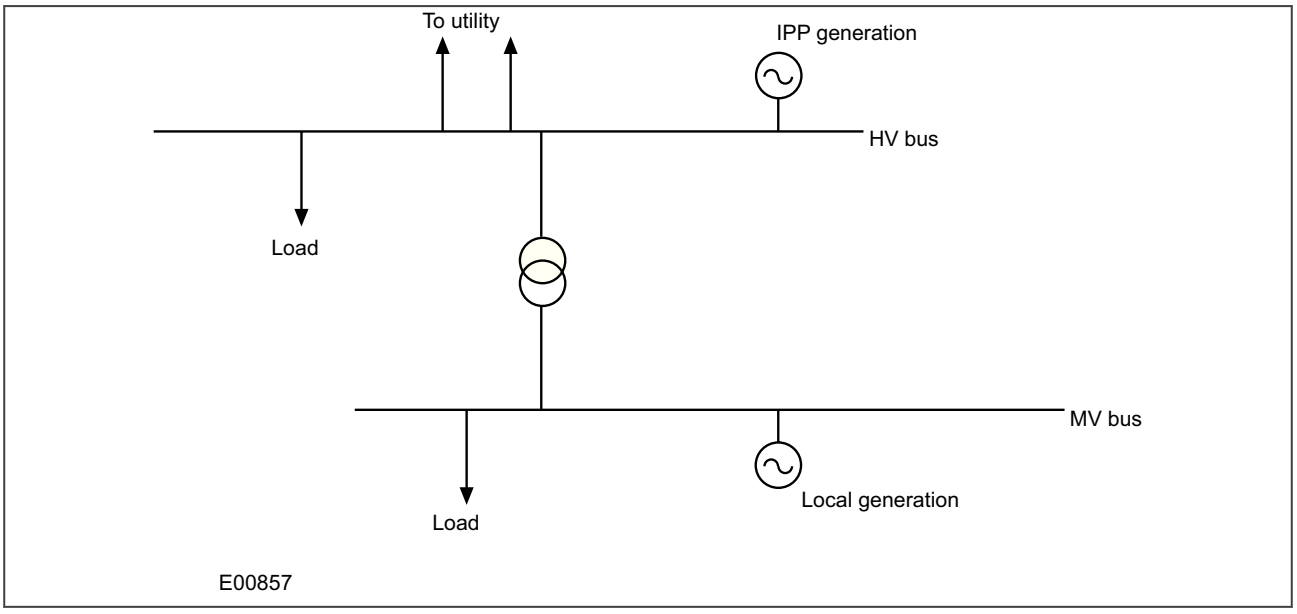


Figure 124: Power system segregation based upon frequency measurements

5 INDEPENDENT R.O.C.O.F PROTECTION

Where there are very large loads, imbalances may occur that result in rapid decline in system frequency. The situation could be so bad that shedding one or two stages of load is unlikely to stop this rapid frequency decline. In such a situation, standard underfrequency protection will normally have to be supplemented with protection that responds to the rate of change of frequency. An element is therefore required which identifies the high rate of decline of frequency, and adapts the load shedding scheme accordingly.

Such protection can identify frequency variations occurring close to nominal frequency thereby providing early warning of a developing frequency problem. The element can also be used as an alarm to warn operators of unusually high system frequency variations.

5.1 INDEPENENT R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides nine independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The following settings are relevant for df/dt+t protection:

- ***df/dt+t (n) Status***: determines whether the stage is for falling or rising frequency conditions
- ***df/dt+t (n) Set***: defines the rate of change of frequency pickup setting
- ***df/dt+t (n) Time***: sets the time delay

5.2 INDEPENDENT R.O.C.O.F PROTECTION LOGIC

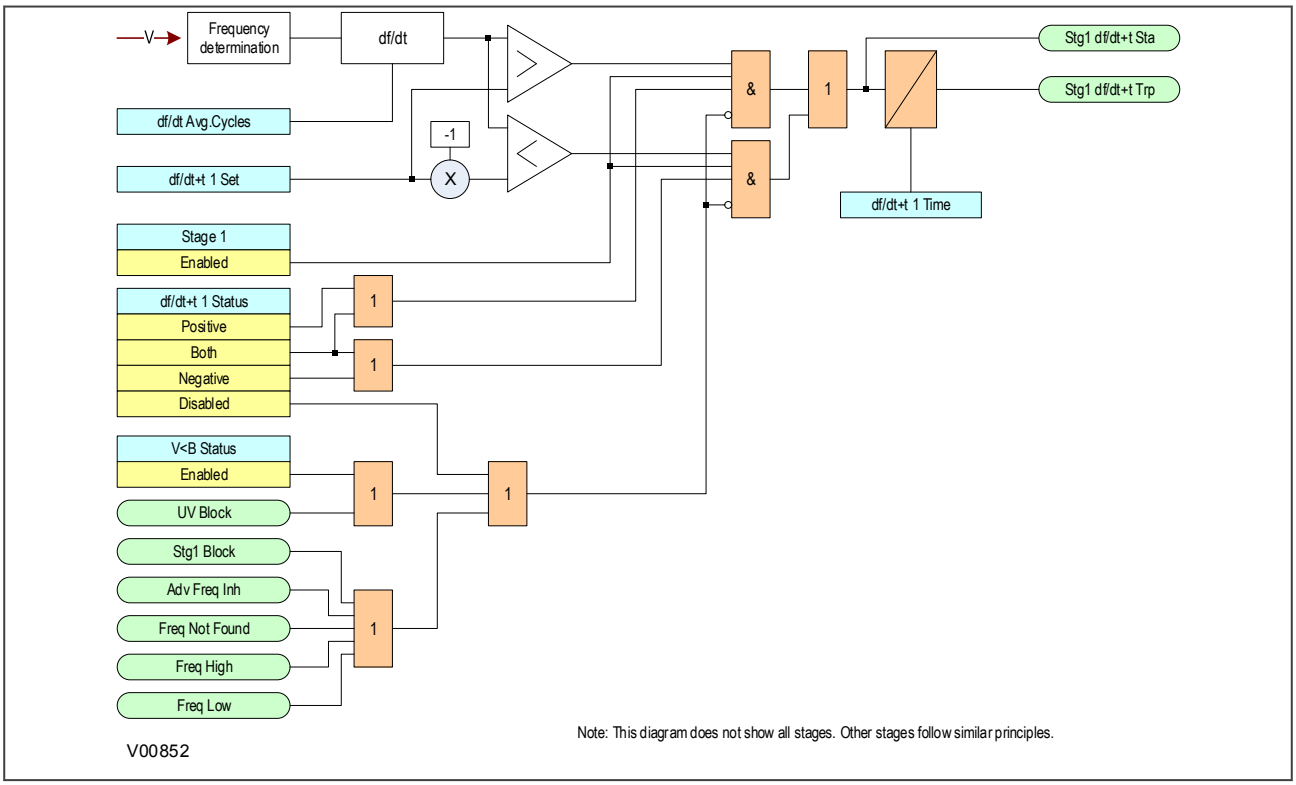


Figure 125: Independent rate of change of frequency logic (single stage)

5.3 APPLICATION NOTES

5.3.1 SETTING GUIDELINES

Considerable care should be taken when setting this element because it is not supervised by a frequency setting. Setting of the time delay or increasing the number of df/dt averaging cycles will improve stability but this is traded against reduced tripping times.

It is likely that this element would be used in conjunction with other frequency based protection elements to provide a scheme that accounts for severe frequency fluctuations. An example scheme is shown below:

	Frequency "f+t [81U/81O]" Elements		Frequency Supervised Rate of Change of Frequency "f+df/dt [81RF]" Elements	
Stage	Frequency Setting (Hz)	Time Setting (Sec.)	Frequency Setting (Hz)	Rate of Change of Frequency Setting (Hz/ Sec.)
1	49	20	49.2	1.0
2	48.6	20	48.8	1.0
3	48.2	10	48.4	1.0
4	47.8	10	48.0	1.0
5	-	-	-	-

Stage	Rate of Change of Frequency "df/dt+t [81R]" Elements	
	Rate of Change of Frequency Setting (Hz/Sec.)	Time Setting (Sec.)
1	-	-
2	-	-
3	-3.0	0.5
4	-3.0	0.5
5	-3.0	0.1

In this scheme, tripping of the last two stages is accelerated by using the independent rate of change of frequency element. If the frequency starts falling at a high rate (> 3 Hz/s in this example), then stages 3 & 4 are shed at around 48.5 Hz, with the objective of improving system stability. Stage 5 serves as an alarm and gives operators advance warning that the situation is critical.

6 FREQUENCY-SUPERVISED R.O.C.O.F PROTECTION

Frequency-supervised Rate of Change of Frequency protection works in a similar way to Independent Rate of change of Frequency Protection. The only difference is that with frequency supervision, the actual frequency itself is monitored and the protection operates when both the rate of change of frequency AND the frequency itself go outside the set limits.

Frequency-supervised Rate of Change of Frequency protection is also known as f+df/dt protection.

6.1 FREQUENCY-SUPERVISED R.O.C.O.F IMPLEMENTATION

The device provides nine independent stages of protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

The following settings are relevant for f+ df/dt protection:

- ***f+df/dt 1 Status***: determines whether the stage is for falling or rising frequency conditions
- ***f+df/dt 1 freq***: defines the frequency pickup setting
- ***f+df/dt 1 df/dt***: defines the rate of change of frequency pickup setting

The device will also indicate when an incorrect setting has been applied if the frequency threshold is set to the nominal system frequency. There is no intentional time delay associated with this element, but time delays could be applied using the PSL if required.

6.2 FREQUENCY-SUPERVISED R.O.C.O.F LOGIC

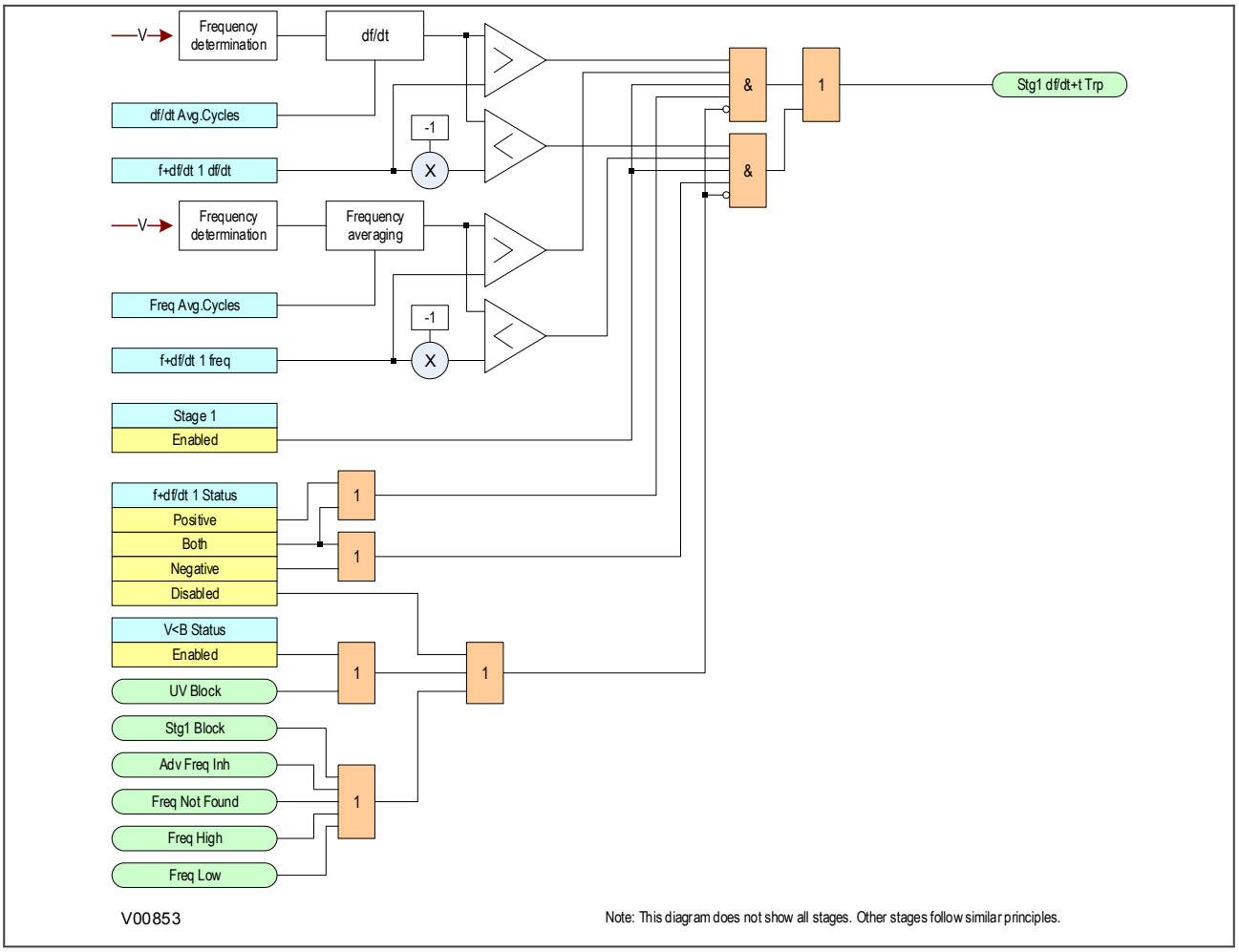


Figure 126: Frequency-supervised rate of change of frequency logic (single stage)

6.3 APPLICATION NOTES

6.3.1 FREQUENCY-SUPERVISED R.O.C.O.F EXAMPLE

In the load shedding scheme below, we assume that for falling frequency conditions, the system can be stabilised at frequency f2 by shedding a stage of load. For slow rates of decay, this can be achieved using the underfrequency protection element set at frequency f1 with a suitable time delay. However, if the generation deficit is substantial, the frequency will rapidly decrease and it is possible that the time delay imposed by the underfrequency protection will not allow for frequency stabilisation. In this case, the chance of system recovery will be enhanced by disconnecting the load stage based on a measurement of rate of change of frequency and bypassing the time delay.

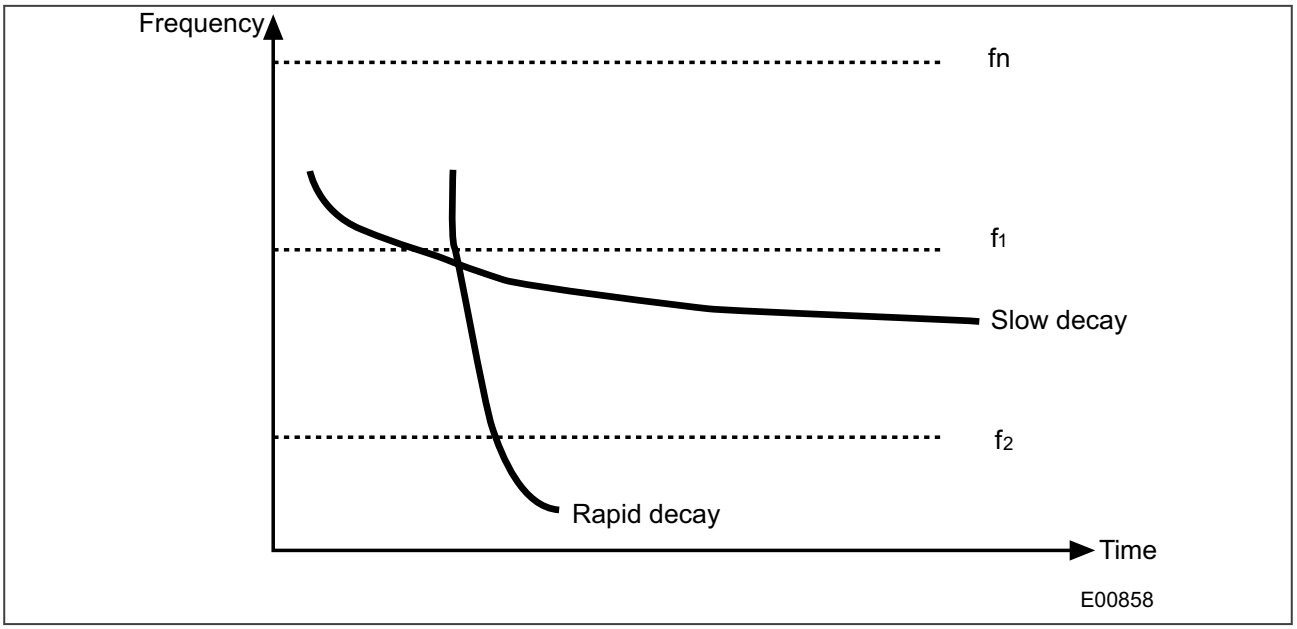


Figure 127: Frequency supervised rate of change of frequency protection

6.3.2 SETTING GUIDELINES

We recommend that the frequency supervised rate of change of frequency protection (f+df/dt) element be used in conjunction with the time delayed frequency protection (f+t) elements.

A four stage high speed load shedding scheme may be configured as indicated below, noting that in each stage, both the "f+t" and the "f+df/dt" elements are enabled.

	Frequency "f+t [81U/81O]" Elements		Frequency Supervised Rate of Change of Frequency "f+df/dt [81RF]" Elements	
Stage	Frequency Setting (Hz)	Time Setting (Sec.)	Frequency Setting (Hz)	Rate of Change of Frequency Setting (Hz/sec.)
1	49	20	49	1.0
2	48.6	20	48.6	1.0
3	48.2	10	48.2	1.0
4	47.8	10	47.8	1.0

It may be possible to further improve the speed of load shedding by changing the frequency setting on the f+df/dt element. In the settings outlined below, the frequency settings for this element have been set slightly higher than the frequency settings for the f+t element. This difference will allow for the measuring time, and will result in the tripping of the two elements at approximately the same frequency value. Therefore, the slow frequency decline and fast frequency decline scenarios are independently monitored and optimised without sacrificing system security.

	Frequency "f+t [81U/81O]" Elements		Frequency Supervised Rate of Change of Frequency "f+df/dt [81RF]" Elements	
Stage	Frequency Setting (Hz)	Time Setting (Sec.)	Frequency Setting (Hz)	Rate of Change of Frequency Setting (Hz/sec.)
1	49	20	49.2	1.0
2	48.6	20	48.8	1.0
3	48.2	10	48.4	1.0
4	47.8	10	48.0	1.0

7 AVERAGE RATE OF CHANGE OF FREQUENCY PROTECTION

Owing to the complex dynamics of power systems, variations in frequency during times of generation-to-load imbalance are highly non-linear. Oscillations will occur as the system seeks to address the imbalance, resulting in frequency oscillations typically in the order of 0.1 Hz to 1 Hz, in addition to the basic change in frequency.

The independent and frequency-supervised rate of change of frequency elements use an instantaneous measurement of the rate of change of frequency, based on a 3-cycle, filtered, rolling average technique. Due to the oscillatory nature of frequency excursions, this instantaneous value can sometimes be misleading, either causing unexpected operation or excessive instability. For this reason, the device also provides an element for monitoring the longer term frequency trend, thereby reducing the effects of non-linearity in the system.

Average Rate of Change of Frequency protection is also known as f+Df/Dt protection (note the upper-case "D").

7.1 AVERAGE R.O.C.O.F PROTECTION IMPLEMENTATION

The device provides nine independent stages of average rate of change of frequency protection. Each stage can respond to either rising or falling frequency conditions. This depends on whether the frequency threshold is set above or below the system nominal frequency. For example, if the frequency threshold is set above nominal frequency, the rate of change of frequency setting is considered as positive and the element will operate for rising frequency conditions. If the frequency threshold is set below nominal frequency, the setting is considered as negative and the element will operate for falling frequency conditions.

When the measured frequency crosses the supervising frequency threshold, a timer is initiated. At the end of this time period, the frequency difference is evaluated and if this exceeds the setting, a trip output is given.

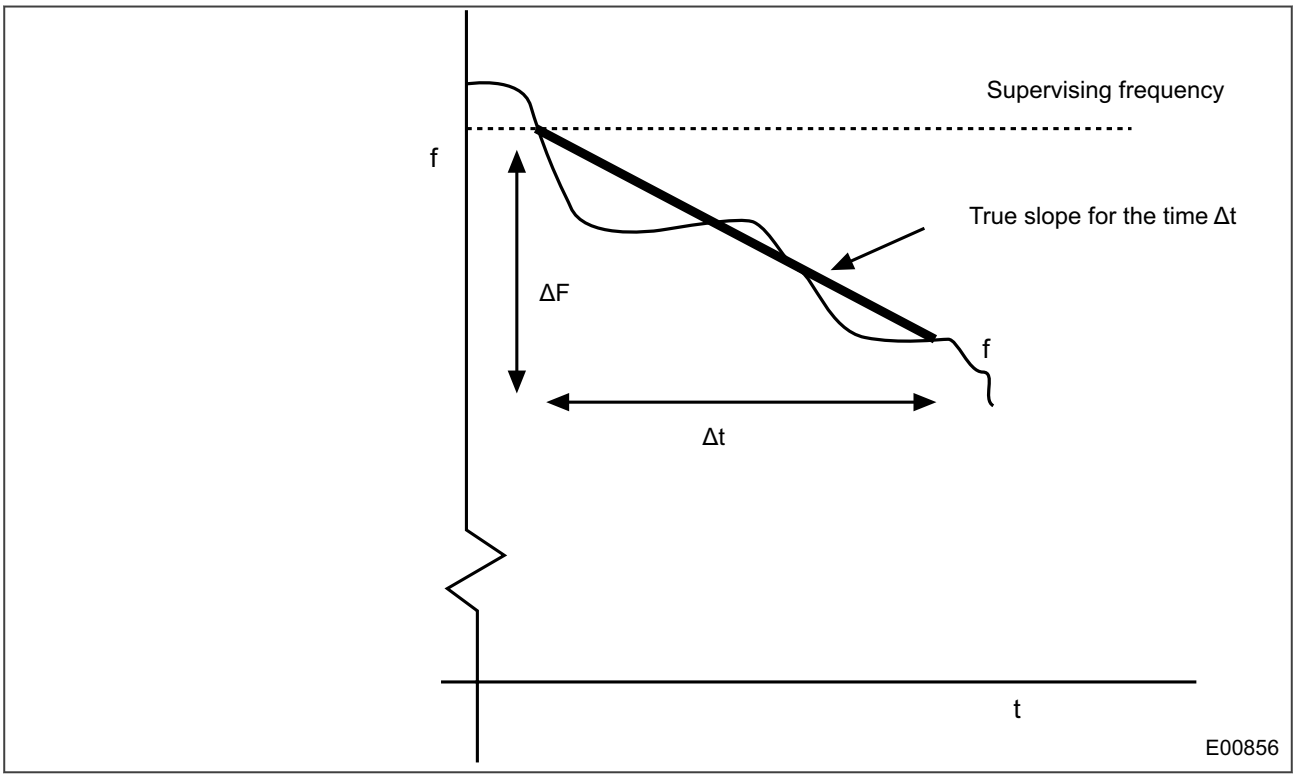


Figure 128: Average rate of change of frequency characteristic

After time Δt, the element is blocked from further operation until the frequency recovers to a value above the supervising frequency threshold. If the element has operated, the trip DDB signal will be ON until the frequency recovers to a value above the supervising frequency threshold.

The average rate of change of frequency is then measured based on the frequency difference, Δf over the settable time period, Δt.

The following settings are relevant for Df/Dt protection:

- ***f+Df/Dt (n) Status***: determines whether the stage is for falling or rising frequency conditions
- ***f+Df/Dt (n) Freq***: defines the frequency pickup setting
- ***f+Df/Dt (n) Dfreq***: defines the change in frequency that must be measured in a set time period
- ***f+Df/Dt (n) Dtime***: sets the time period over which the frequency is monitiored

7.2 AVERAGE R.O.C.O.F LOGIC

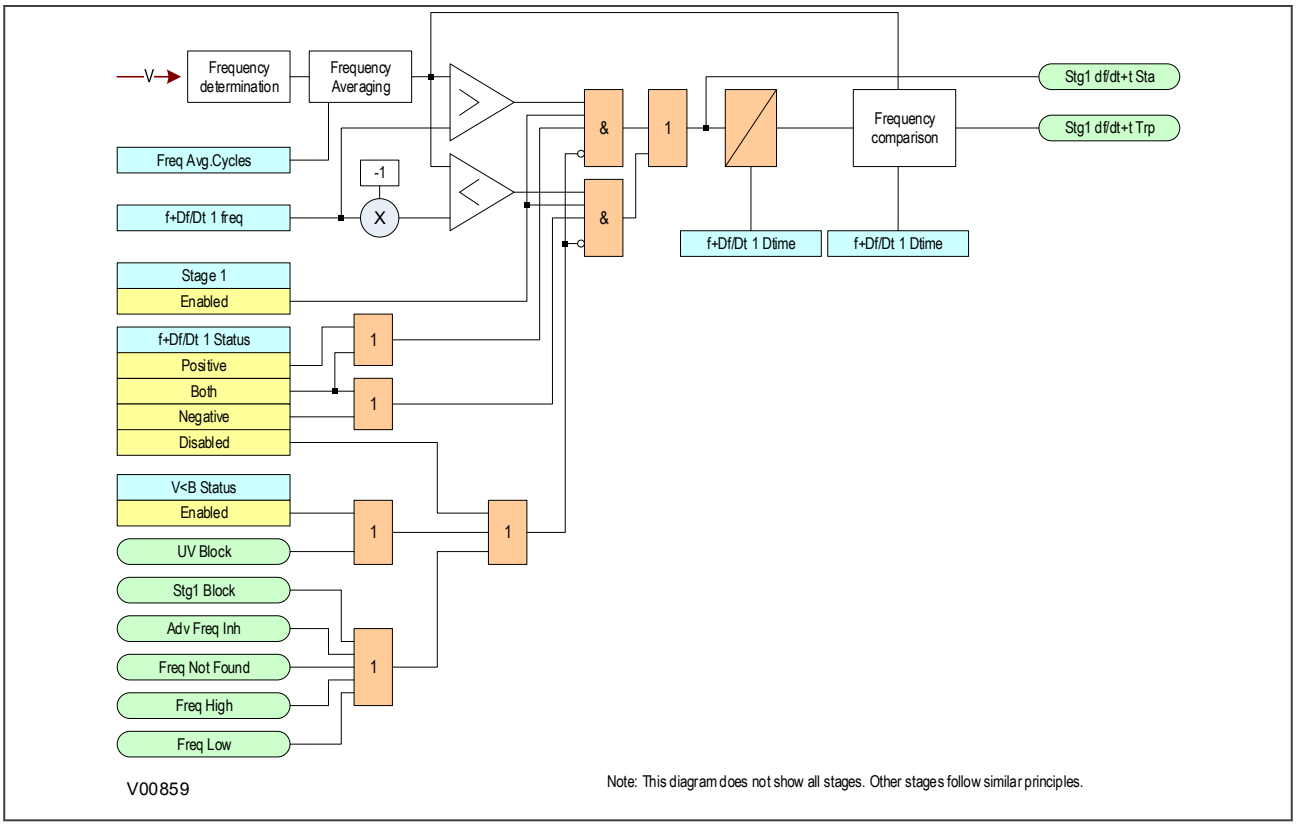


Figure 129: Average rate of change of frequency logic (single stage)

7.3 APPLICATION NOTES

7.3.1 SETTING GUIDELINES

The average rate of change of frequency element can be set to measure the rate of change over a short period as low as 20 ms (1 cycle @ 50 Hz) or a relatively long period up to 2 s (100 cycles @ 50 Hz). With a time setting, Dt, towards the lower end of this range, the element becomes similar to the frequency supervised rate of change function, "f+df/dt". With high Dt settings, the element acts as a frequency trend monitor.

Although the element has a wide range of setting possibilities we recommend that the Dt setting is set greater than 100 ms to ensure the accuracy of the element.

A possible four stage load shedding scheme using the average rate of change frequency element is shown in the following table:

	Frequency "f+t [81U/81O]" Elements		Average Rate of Change of Frequency "f+Df/Dt [81RAV]" Elements		
Stage	(f+t) f Frequency Setting (Hz)	(f+t) t Time Setting (Sec.)	(f+Df/Dt) f Frequency Setting (Hz)	(f+Df/Dt) Df Frequency Diff Setting, (Hz)	(f+Df/Dt) Dt Time Period, (Sec.)
1	49	20	49	0.5	0.5
2	48.6	20	48.6	0.5	0.5
3	48.2	10	48.2	0.5	0.5
4	47.8	10	47.8	0.5	0.5

In the above scheme, the faster load shed decisions are made by monitoring the frequency change over 500 ms. Therefore tripping takes place more slowly than in schemes employing frequency-supervised df/dt, but the difference is not very much at this setting. If the delay jeopardises system stability, then the scheme can be improved by increasing the independent "f" setting. Depending on how much this value is increased, the frequency at which the "f+Df/Dt" element will trip also increases and so reduces the time delay under more severe frequency fluctuations. For example, with the settings shown below, the first stage of load shedding would be tripped approximately 300 msecs after 49.0 Hz is reached and at a frequency of approximately 48.7 Hz.

	Frequency "f+t [81U/81O]" Elements		Average Rate of Change of Frequency "f+Df/Dt [81RAV]" Elements		
Stage	(f+t) f Frequency Setting (Hz)	(f+t) t Time Setting (Sec)	(f+Df/Dt) f Frequency Setting (Hz)	(f+Df/Dt) Df Frequency Diff Setting (Hz)	(f+Df/Dt) Dt Time Period, (Sec.)
1	49	20	49.2	0.5	0.5 s
2	48.6	20	48.8	0.5	0.5 s
3	48.2	10	48.4	0.5	0.5 s
4	47.8	10	48.0	0.5	0.5 s

8 LOAD SHEDDING AND RESTORATION

The goal of load shedding is to stabilise a falling system frequency. As the system stabilises and the generation capability improves, the system frequency will recover to near normal levels and after some time delay it is possible to consider the restoration of load onto the healthy system. However, load restoration needs to be performed carefully and systematically so that system stability is not jeopardized again.

In the case of industrial plants with captive generation, load restoration should be linked to the available generation since connecting additional load when the generation is still inadequate, will only result in declining frequency and more load shedding. If the in-plant generation is insufficient to meet the load requirements, then load restoration should be interlocked with recovery of the utility supply.

Whilst load shedding leads to an improvement in the system frequency, the disconnected loads need to be reconnected after the system is stable again. Loads should only be restored if the frequency remains stable for some period of time (minor frequency excursions can be ignored during this time period). The number of load restoration steps is normally less than the load shedding steps to reduce repeated disturbances while restoring load.

8.1 LOAD RESTORATION IMPLEMENTATION

The device uses the measurement of system frequency as the main criteria for load restoration. For each stage of load restoration, it is necessary that the same stage of load shedding has occurred previously and that no elements within that stage are configured for overfrequency or rising frequency conditions. If load shedding has not previously occurred, the load restoration for that stage is inactive.

The device provides nine independent stages of Load Restoration. It is implemented in the *FREQ PROTECTION* column of the relevant settings group. The following settings are relevant for Load Restoration:

- ***Restore(n) Status***: determines whether the stage is disabled or enabled
- ***Restore(n) Freq***: defines the frequency pickup setting
- ***Restore(n) Time***: Timer period for which the measured frequency must be higher than the stage restoration.
- ***Holding Timer***: Sets the holding timer value

8.2 HOLDING BAND

Load restoration for a given stage begins when the system frequency rises above the ***Restore(n) Freq*** setting for that stage and the stage restoration timer ***Restore(n) Time*** is initiated. If the system frequency remains above the frequency setting for the set time delay, load restoration of that stage will be triggered.

Unfortunately, frequency recovery profiles are highly non-linear and it would be reasonably common for the system frequency to fall transiently below the restoration frequency threshold. If the restoration timer immediately reset whenever a frequency dip occurred, it is likely that load restoration would never be successful. For this reason, the protection has a "holding band". This holding band is a region defined by the restoration frequency and the highest frequency setting used in the load shedding elements for that stage. The difference between these two settings must always be greater than 0.02 Hz, otherwise a ***Wrong Setting*** alarm will be generated. Whenever the system frequency dips into the holding band, operation of the stage restoration timer is suspended until the frequency rises above the restoration frequency setting, at which point timing will continue. If the system frequency dip is sufficiently large to cause any frequency element to start or trip in this stage, i.e. if the frequency falls below the lower limit of the holding band, the restoration timer will immediately be reset. This is demonstrated below.

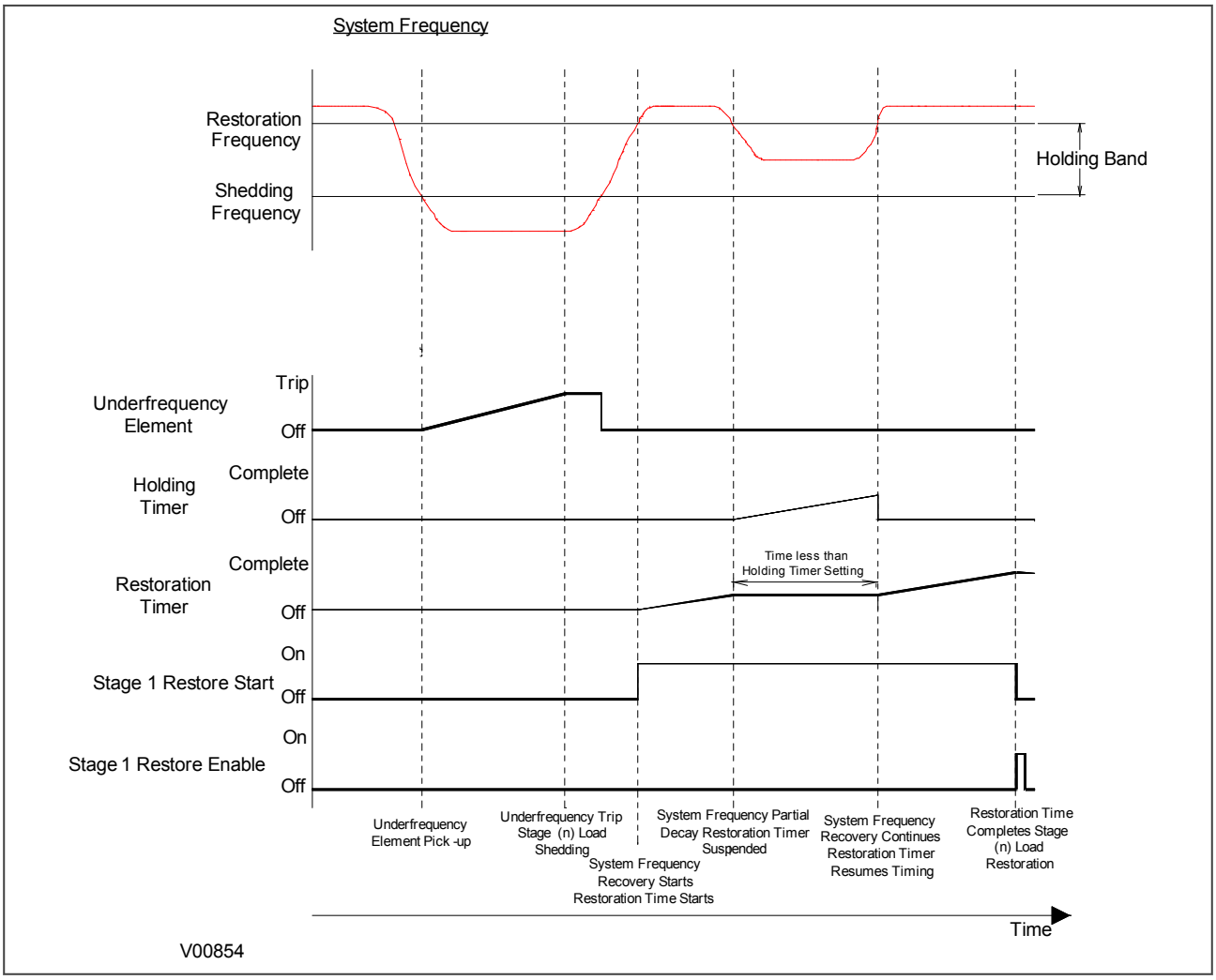


Figure 130: Load restoration with short deviation into holding band

If the system frequency remains in the holding band for too long it is likely that other system frequency problems are occurring and it would be prudent to reset the restoration timer for that stage. For this reason, as soon as the system frequency is measured to be within the holding band, the "Holding Timer" is initiated. If the system frequency doesn't leave the holding band before the holding timer setting has been exceeded, the load restoration time delay for that stage is immediately reset.

Note:
The holding timer has a common setting for all stages of load restoration.

An example of the case when the time in the holding band is excessive is shown below.

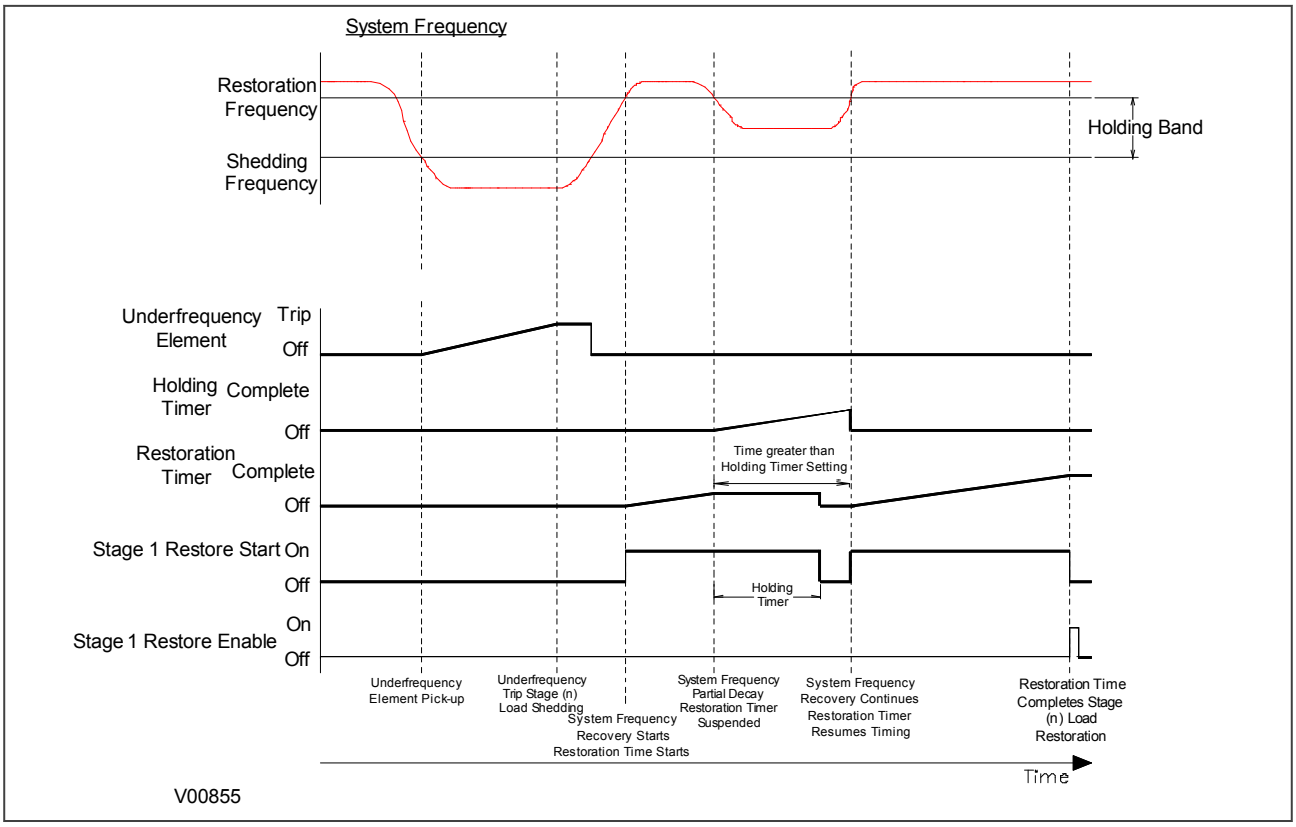


Figure 131: Load restoration with long deviation into holding band

8.3 LOAD RESTORATION LOGIC

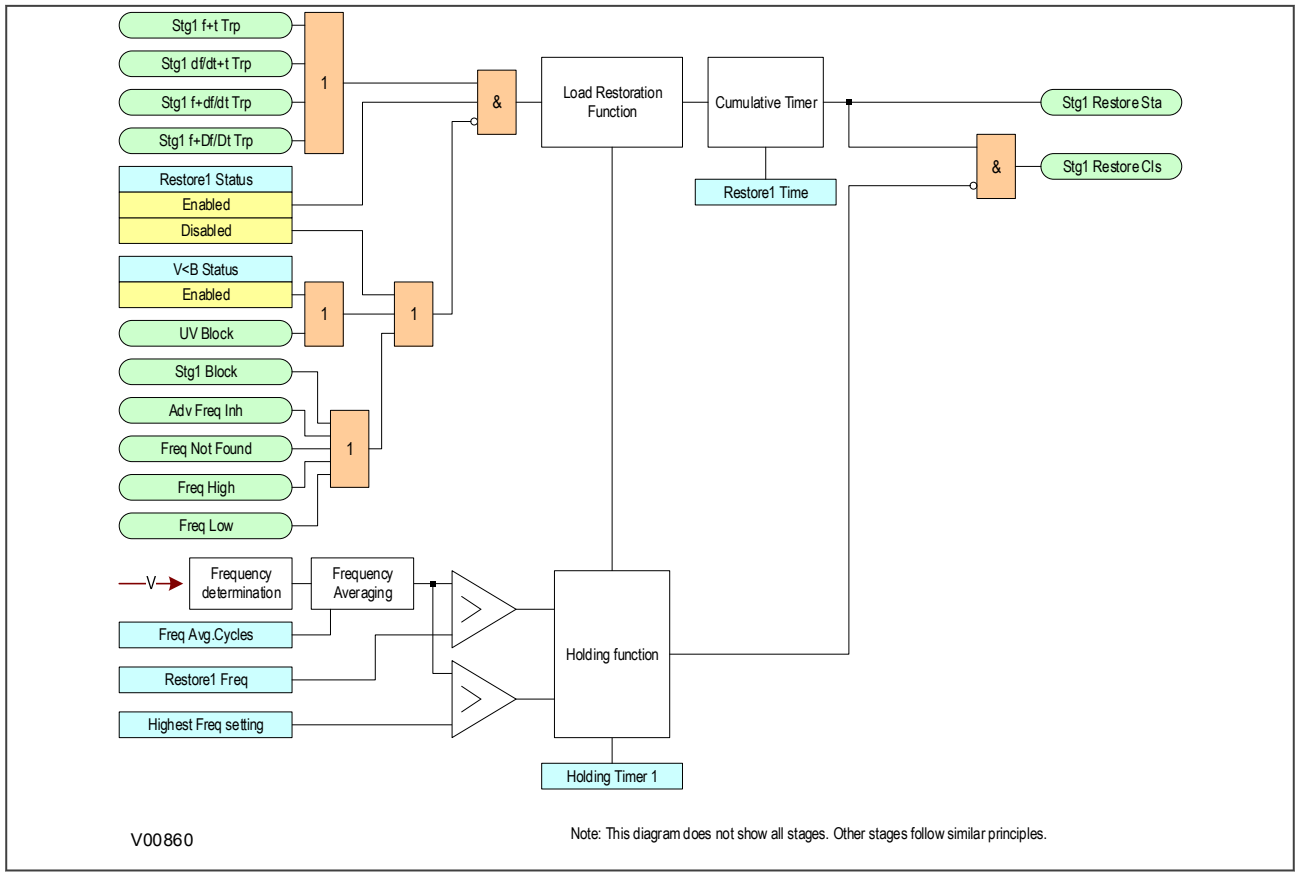


Figure 132: Load Restoration logic

8.4 APPLICATION NOTES

8.4.1 SETTING GUIDELINES

A four stage, single frequency load restoration scheme is shown below. The frequency setting has been chosen such that there is sufficient separation between the highest load shed frequency and the restoration frequency to prevent any possible hunting. A restoration frequency setting closer to nominal frequency may be chosen if an operating frequency of 49.3 Hz is unacceptable.

Stage	Restoration Frequency Setting (Hz)	Restoration Time Delay (secs)	Holding Time Delay (secs)
1	49.3 Hz	240 sec	20 sec
2	49.3 Hz	180 sec	20 sec
3	49.3 Hz	120 sec	20 sec
4	49.3 Hz	60 sec	20 sec

In this scheme, the time delays ensure that the most critical loads are reconnected (assuming that the higher stages refer to more important loads). By restoring the load sequentially, system stability should normally be maintained. These time settings are system dependent; higher or lower settings may be required depending on the particular application.

It is possible to set up restoration schemes involving multiple frequencies. This allows faster restoration of loads, but there is the possibility of continuous system operation at frequencies far removed from the nominal. A typical scheme using two frequencies is illustrated below:

Stage	Restore Freq. Restoration Frequency Setting (Hz)	Restore DelayRestoration Time Delay (S)	Holding Time Delay (S)
1	49.5 Hz	120 sec	20 sec
2	49.5 Hz	60 sec	20 sec
3	49.0 Hz	120 sec	20 sec
4	49.0 Hz	60 sec	20 sec

Staggered time settings may be used in this scheme as well, but the time separation among the restoration of stages will be a function of the frequency recovery pattern. Time coordinated restoration can only be guaranteed for those stages with a common restoration frequency setting.

CHAPTER 12

POWER PROTECTION FUNCTIONS

1 CHAPTER OVERVIEW

Power protection is used for protecting generators. Although the main function of this device is for feeder applications, it can also be used as a cost effective alternative for protecting small distributed generators, typically less than 2 MW.

This chapter contains the following sections:

2 OVERPOWER PROTECTION

With Overpower, we should consider two distinct conditions: Forward Overpower and Reverse Overpower.

A forward overpower condition occurs when the system load becomes excessive. A generator is rated to supply a certain amount of power and if it attempts to supply power to the system greater than its rated capacity, it could be damaged. Therefore overpower protection in the forward direction can be used as an overload indication. It can also be used as back-up protection for failure of governor and control equipment. Generally the Overpower protection element would be set above the maximum power rating of the machine.

A reverse overpower condition occurs if the generator prime mover fails. When this happens, the power system may supply power to the generator, causing it to motor. This reversal of power flow due to loss of prime mover can be very damaging and it is important to be able to detect this with a Reverse Overpower element.

2.1 OVERPOWER PROTECTION IMPLEMENTATION

Overpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group, under the sub-heading *OVERPOWER*.

The Overpower Protection element provides 2 stages of directional overpower for both active and reactive power. The directional element can be configured as forward or reverse and for single-phase or three-phase operation.

The elements use three-phase power or single phase power measurements (based on A Phase) as the energising quantities. A Start condition occurs when two consecutive measurements exceed the setting threshold. A trip condition occurs if the Start condition is present for the set time delay. This can be inhibited by the VTS Slow Block and Pole Dead logic if desired.

The Start and Trip timer resets if the power falls below the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality for a pecking fault condition, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

2.2 OVERPOWER LOGIC

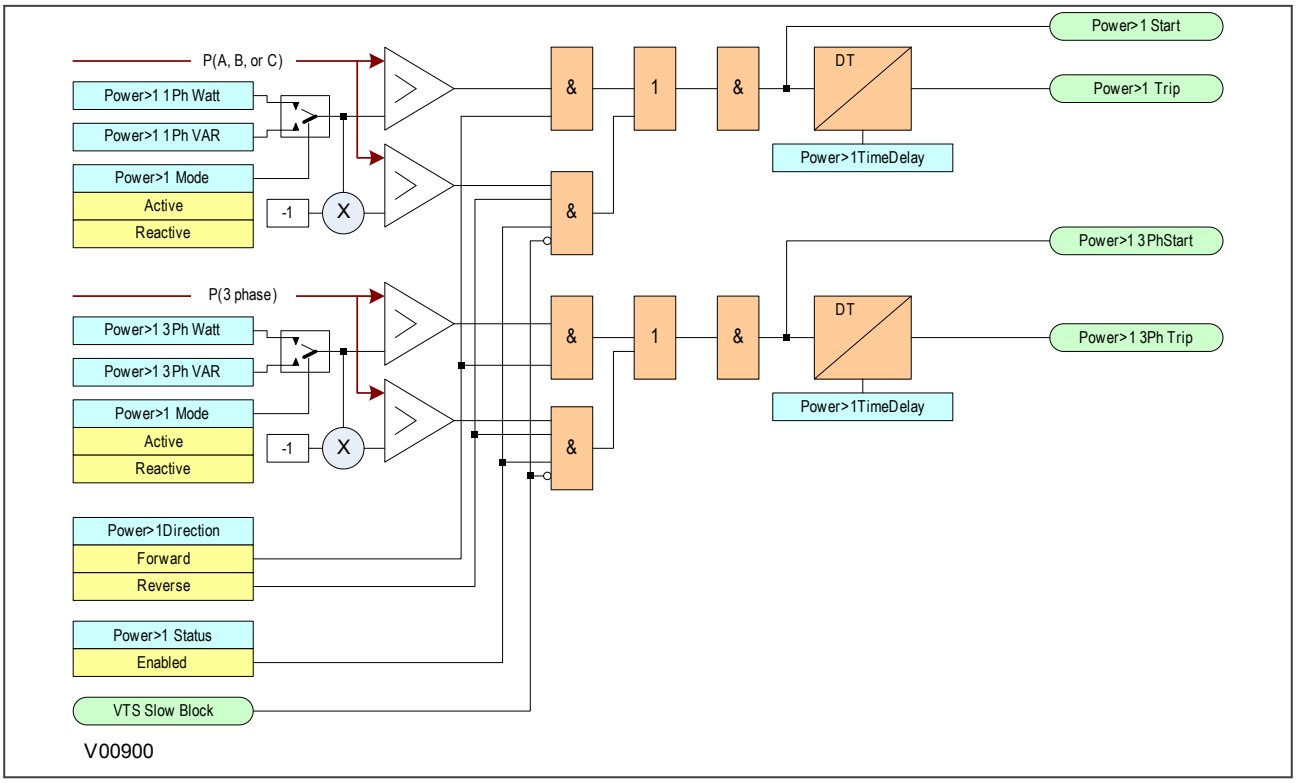


Figure 133: Overpower logic

2.3 APPLICATION NOTES

2.3.1 FORWARD OVERPOWER SETTING GUIDELINES

The relevant power threshold settings should be set greater than the full load rated power.

The operating mode should be set to Forward.

A time delay setting (***Power>(n) TimeDelay***) should be applied. This setting is dependant on the application. The delay on the reset timer (***Power>(n) tRESET***), would normally be set to zero.

2.3.2 REVERSE POWER CONSIDERATIONS

A generator is expected to supply power to the connected system in normal operation. If the generator prime mover fails, it will begin to take motoring power from the power system (if the power system to which it is connected has other generating sources). The consequences of this reversal of power and the level of power drawn from the power system will be dependent on the type of prime mover.

Typical levels of motoring power and possible motoring damage that could occur for various types of generating plant are given in the following table.

Prime mover	Motoring power	Possible damage (percentage rating)
Diesel Engine	5% - 25%	Risk of fire or explosion from unburned fuel
Motoring level depends on compression ratio and cylinder bore stiffness. Rapid disconnection is required to limit power loss and risk of damage.		
Gas Turbine	10% - 15% (Split-shaft) >50% (Single-shaft)	With some gear-driven sets, damage may arise due to reverse torque on gear teeth.

Prime mover	Motoring power	Possible damage (percentage rating)
Compressor load on single shaft machines leads to a high motoring power compared to split-shaft machines. Rapid disconnection is required to limit power loss or damage.		
Hydraulic Turbines	0.2 - >2% (Blades out of water) >2.0% (Blades in water)	Blade and runner damage may occur with a long period of motoring
Power is low when blades are above tail-race water level. Hydraulic flow detection devices are often the main means of detecting loss of drive. Automatic disconnection is recommended for unattended operation.		
Steam Turbines	0.5% - 3% (Condensing sets) 3% - 6% (Non-condensing sets)	Thermal stress damage may be inflicted on low-pressure turbine blades when steam flow is not available to dissipate losses due to air resistance.
Damage may occur rapidly with non-condensing sets or when vacuum is lost with condensing sets. Reverse power protection may be used as a secondary method of detection and might only be used to raise an alarm.		

In some applications, the level of reverse power in the case of prime mover failure may fluctuate. This may be the case for a failed diesel engine. To prevent cyclic initiation and reset of the main trip timer, an adjustable reset time delay is provided. You will need to set this time delay longer than the period for which the reverse power could fall below the power setting. This setting needs to be taken into account when setting the main trip time delay.

Note:
A delay in excess of half the period of any system power swings could result in operation of the reverse power protection during swings.

2.3.3 REVERSE OVERPOWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a reverse power stage by selecting the ***Power>(n) Direction*** cell to `Reverse`.

The relevant power threshold settings should be set to less than 50% of the motoring power.

The operating mode should be set to Reverse.

The reverse power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation.

A time delay setting, of approximately 5 s would be typically applied.

The delay on the reset timer, ***Power>1 tRESET*** or ***Power>2 tRESET***, would normally be set to zero.

When settings of greater than zero are used for the reset time delay, the pick-up time delay setting may need to be increased to ensure that false tripping does not result in the event of a stable power swinging event.

Reverse overpower protection can also be used for loss of mains applications. If the distributed generator is connected to the grid but not allowed to export power to the grid, it is possible to use reverse power detection to switch off the generator. In this case, the threshold setting should be set to a sensitive value, typically less than 2% of the rated power. It should also be time-delayed to prevent false trips or alarms being given during power system disturbances, or following synchronisation. A typical time delay is 5 seconds.

3 UNDERPOWER PROTECTION

Although the Underpower protection is directional and can be configured as forward or reverse, the most common application is for Low Forward Power protection.

When a machine is generating and the circuit breaker connecting the generator to the system is tripped, the electrical load on the generator is cut off. This could lead to overspeeding of the generator if the mechanical input power is not reduced quickly. Large turbo-alternators, with low-inertia rotor designs, do not have a high over speed tolerance. Trapped steam in a turbine, downstream of a valve that has just closed, can rapidly lead to over speed. To reduce the risk of over speed damage, it may be desirable to interlock tripping of the circuit breaker and the mechanical input with a low forward power check. This ensures that the generator circuit breaker is opened only after the mechanical input to the prime mover has been removed, and the output power has reduced enough such that overspeeding is unlikely. This delay in tripping the circuit breaker may be acceptable for non-urgent protection trips (e.g. stator earth fault protection for a high impedance earthed generator). For urgent trips however (e.g. stator current differential protection), this Low Forward Power interlock should not be used.

3.1 UNDERPOWER PROTECTION IMPLEMENTATION

Underpower Protection is implemented in the *POWER PROTECTION* column of the relevant settings group, under the sub-heading *UNDERPOWER*.

The *UNDERPOWER* Protection element provides 2 stages of directional underpower for both active and reactive power. The directional element can be configured as forward or reverse and can for single-phase or three-phase operation.

The elements use three-phase power or single phase power measurements (based on A Phase) as the energising quantity. A start condition occurs when two consecutive measurements fall below the setting threshold. A trip condition occurs if the start condition is present for the set trip time. This can be inhibited by the VTS slow block and pole dead logic if desired.

The Start and Trip timer resets if the power exceeds the drop-off level or if an inhibit condition occurs. The reset mechanism is similar to the overcurrent reset functionality, where the percentage of elapsed time for the operate timer is memorised for a set reset time delay. If the Start condition returns before the reset timer has timed out, the operate time initialises from the memorised travel value. Otherwise the memorised value is reset to zero after the reset time times out.

3.2 UNDERPOWER LOGIC

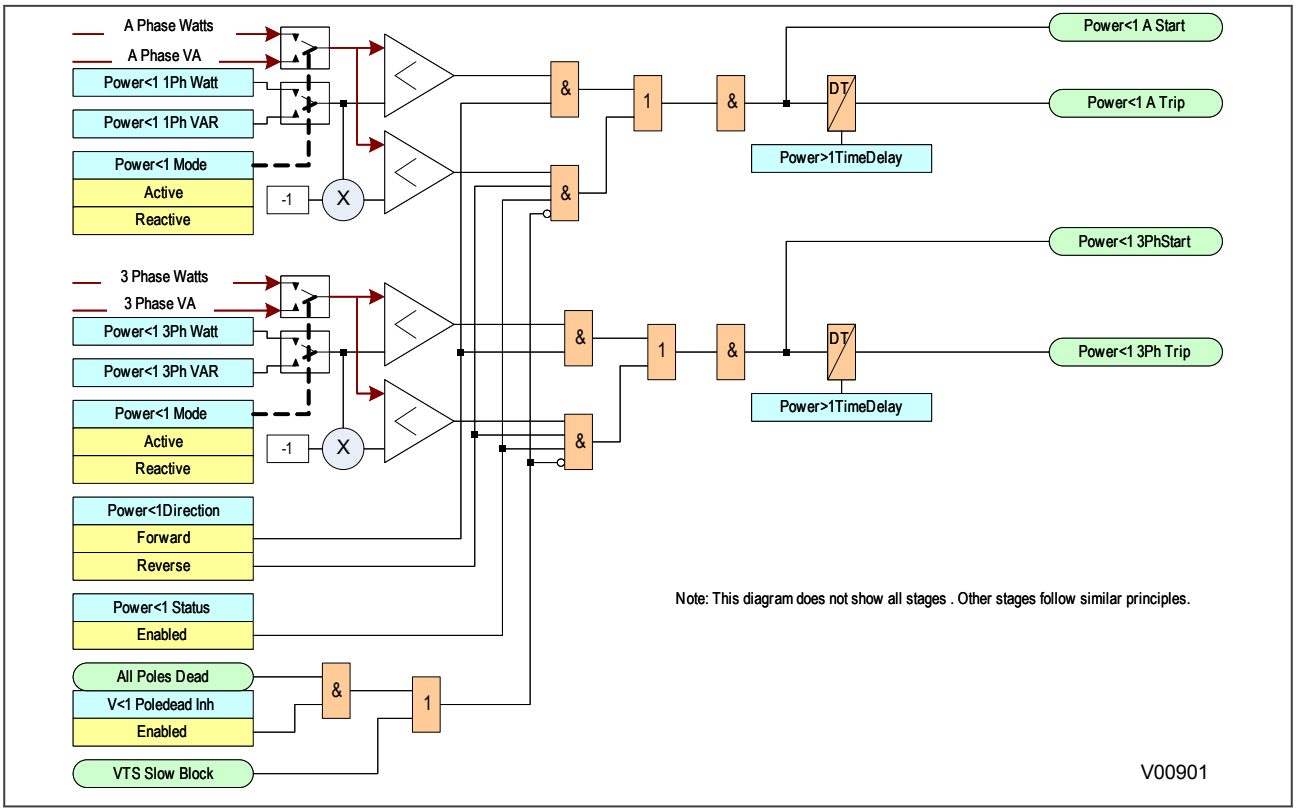


Figure 134: Underpower logic

3.3 APPLICATION NOTES

3.3.1 LOW FORWARD POWER CONSIDERATIONS

The Low Forward Power protection can be arranged to interlock 'non-urgent' protection tripping using the programmable scheme logic. It can also be arranged to provide a contact for external interlocking of manual tripping. To prevent unwanted alarms and flags, a Low Forward Power protection element can be disabled when the circuit breaker is opened via Pole Dead logic.

The Low Forward Power protection can also be used to provide loss of load protection when a machine is motoring. It can be used for example to protect a machine which is pumping from becoming unprimed, or to stop a motor in the event of a failure in the mechanical transmission.

A typical application would be for pump storage generators operating in the motoring mode, where there is a need to prevent the machine becoming unprimed which can cause blade and runner damage. During motoring conditions, it is typical for the protection to switch to another setting group with the low forward power enabled and correctly set and the protection operating mode set to `Reverse`.

A low forward power element may also be used to detect a loss of mains or loss of grid condition for applications where the distributed generator is not allowed to export power to the system.

3.3.2 LOW FORWARD POWER SETTING GUIDELINES

Each stage of power protection can be selected to operate as a forward power stage by selecting the ***Power<(n) Direction*** cell to `Forward`.

When required for interlocking of non-urgent tripping applications, the threshold setting of the low forward power protection function should be less than 50% of the power level that could result in a dangerous overspeed condition on loss of electrical loading.

When required for loss of load applications, the threshold setting of the low forward power protection function, is system dependent, however, it is typically set to 10 - 20% below the minimum load. The operating mode should be set to operate for the direction of the load current, which would typically be reverse for a pump storage machine application where *Forward* is the Generating direction and *Reverse* is the motoring direction.

For interlocking non-urgent trip applications the time delay associated with the low forward power protection function could be set to zero. However, some delay is desirable so that permission for a non-urgent electrical trip is not given in the event of power fluctuations arising from sudden steam valve/throttle closure. A typical time delay is 2 seconds.

For loss of load applications the pick-up time delay is application dependent but is normally set in excess of the time between motor starting and the load being established. Where rated power cannot be reached during starting (for example where the motor is started with no load connected) and the required protection operating time is less than the time for load to be established then it will be necessary to inhibit the power protection during this period. This can be done in the PSL using AND logic and a pulse timer triggered from the motor starting to block the power protection for the required time.

When required for loss of mains or loss of grid applications where the distributed generator is not allowed to export power to the system, the threshold setting of the reverse power protection function, should be set to a sensitive value, typically <2% of the rated power.

The low forward power protection function should be time-delayed to prevent false trips or alarms being given during power system disturbances or following synchronisation. A time delay setting, of 5 s should be applied typically.

The delay on the reset timers would normally be set to zero.

To prevent unwanted alarms and flags, the protection element can be disabled when the circuit breaker is open via Pole Dead logic.

4 SENSITIVE POWER PROTECTION

In some applications, it is necessary to have very high accuracy when applying power protection. For such applications it is possible to use metering class CTs and separate Sensitive Power elements.

The Sensitive Power protection is a single-phase power element using phase A current and voltage. It provides two independent stages of Low Forward Power, Reverse Power and Over Power protection with timer and pole-dead blocking.

Note:
Sensitive Power Protection is only available for models equipped with a SEF transformer.

4.1 SENSITIVE POWER PROTECTION IMPLEMENTATION

Sensitive Power Protection is implemented in the *POWER PROTECTION* column of the relevant settings group, under the sub-heading *SENSITIVE POWER*. It is a single phase power element using the A-phase voltage and sensitive current ISEF.

There are two stages of Sensitive Power protection, which can be independently selected as Low Forward Power, Reverse Power and Overpower.

Note:
When the sensitive power function is used, the SEF CT must be connected to Phase A current, making the measured power ISEF x VA.

4.2 SENSITIVE POWER MEASUREMENTS

Three sensitive power related measurements are added to the Measurements column, the visibility of which will depend on the protection configuration.

- A-Phase Sensitive Active Power in Watts (***APh Sen Watts***)
- A-Phase Sensitive Re-active Power in VArs (***APh Sen VARs***)
- A-Phase Sensitive Power Angle (***APh Power Angle***)

4.3 SENSITIVE POWER LOGIC

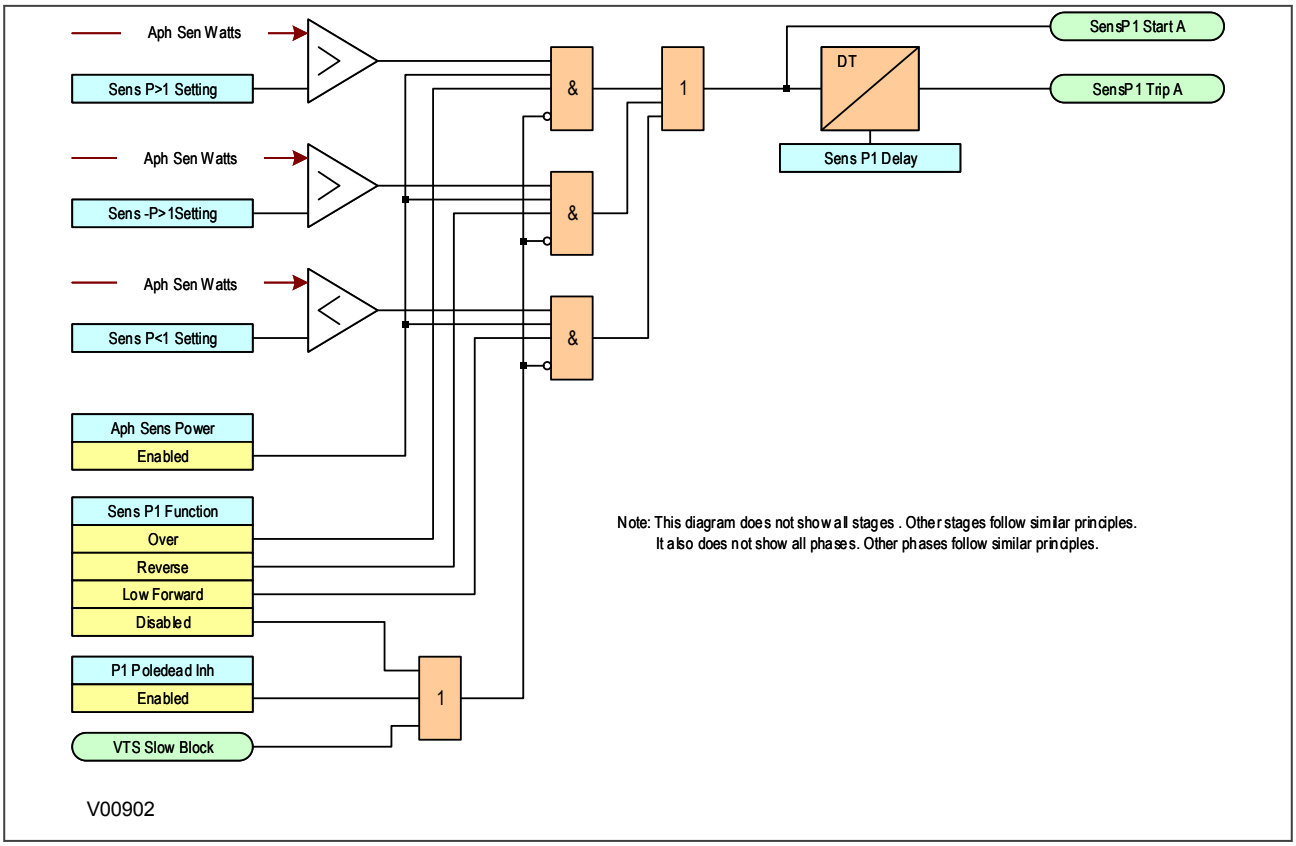


Figure 135: Sensitive Power logic diagram

4.4 APPLICATION NOTES

4.4.1 SENSITIVE POWER CALCULATION

Input Quantities

Sensitive power is calculated from the A-phase-neutral voltage and the A-phase sensitive current input.

The calculation for active power with the correction angle is:

$$P_A = I_{AS} V_A \cos(\varphi - \theta_C)$$

where:

- P_A = sensitive power
- V_A = A-phase voltage
- I_{AS} = A-phase sensitive current
- Φ= the angle of I_{AS} with respect to V_A
- θ_C = the CT correction angle

Calculations within the device are based upon quadrature components obtained from the Fourier analysis of the input signals. The quadrature values for V_A and I_{AS} are used for the sensitive power calculation as shown:

$$\bar{V}_A = V_{Ar} + jV_{Ai}$$

$$\bar{I}_{AS} = I_{ASr} + jI_{ASi}$$

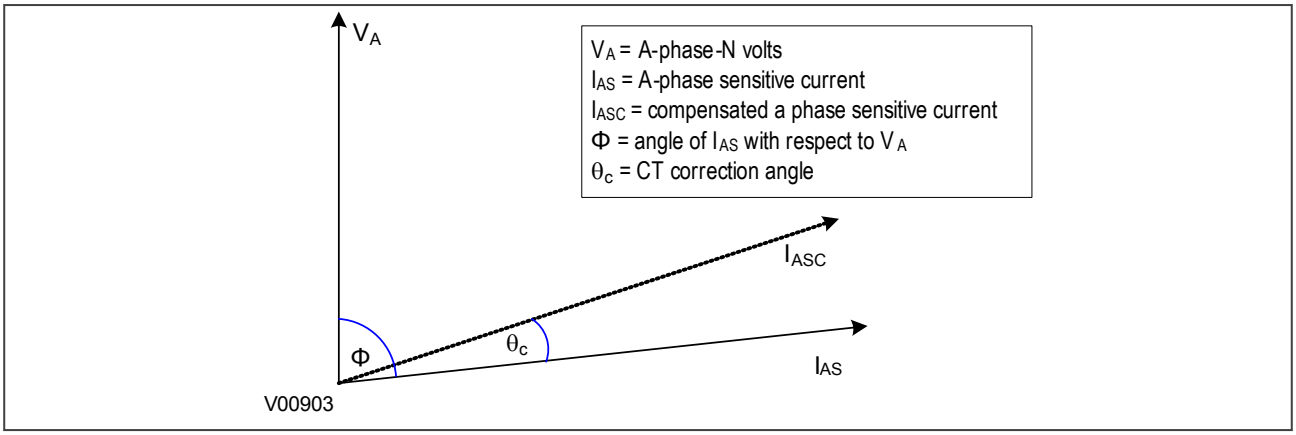


Figure 136: Sensitive Power input vectors

CT Compensation

The CT correction rotates the I_{AS} vector by the correction angle. This correction is performed before the power calculation and can be achieved with the use of a rotation matrix:

$$\begin{bmatrix} \cos\theta_C & -\sin\theta_C \\ \sin\theta_C & \cos\theta_C \end{bmatrix}$$

The corrected phase-A sensitive current I_{ASC} is therefore:

$$\bar{I}_{ASC} = \begin{bmatrix} I_{ASCr} \\ I_{ASCi} \end{bmatrix} = \bar{I}_{AS} = \begin{bmatrix} I_{ASr} \\ I_{ASi} \end{bmatrix} \begin{bmatrix} \cos\theta_C & -\sin\theta_C \\ \sin\theta_C & \cos\theta_C \end{bmatrix} = \begin{bmatrix} I_{ASr}\cos\theta_C - I_{ASi}\sin\theta_C \\ I_{ASr}\sin\theta_C + I_{ASi}\cos\theta_C \end{bmatrix}$$

therefore:

$$I_{ASCr} = I_{ASr}\cos\theta_C - I_{ASi}\sin\theta_C$$

and

$$I_{ASCi} = I_{ASr}\sin\theta_C + I_{ASi}\cos\theta_C$$

Active Power Calculation

The compensated A-phase sensitive current vector is used to calculate the sensitive A-Phase active power P_{AS}.

Using the equation:

$$P_{AS} = Re\bar{V}_A\bar{I}^*_{ASC}$$

we can derive:

$$P_{AS} = Re\left(V_{Ar} + jV_{Ai}\right)\left(I_{ASCr} + jI_{ASCi}\right)$$

$$= Re\left(V_{Ar} + jV_{Ai}\right)\left(I_{ASCr} - jI_{ASCi}\right) = Re\left(V_{Ar}I_{ASCr} + V_{Ai}I_{ASCi}\right) + j\left(V_{Ai}I_{ASCr} - V_{Ar}I_{ASCi}\right)$$

$$= V_{Ar}I_{ASCr} + V_{Ai}I_{ASCi}$$

4.4.2 SENSITIVE POWER SETTING GUIDELINES

For reverse and low forward power protection, if settings greater than 3% Pn are used, the phase angle errors of suitable protection class current transformers will not result in any risk of maloperation. If settings of less than 3% are used, however, we recommend that the current input is driven by a correctly loaded metering class current transformer.

The sensitive power protection has a minimum setting accuracy of 0.5% Pn. It uses the In sensitive CT to calculate single-phase active power. It also provides phase compensation to remove errors introduced by the primary input transformers.

5 WATTMETRIC DIRECTIONAL EARTH FAULT PROTECTION

Note:
Wattmetric Earth Fault Protection (WDE) is only available in P14D Model H.

Some distribution systems run completely insulated from earth. Such systems are called unearthed systems. The advantage of an unearthed system is that a single phase to earth fault does not cause an earth fault current to flow. This means the whole system remains operational and the supply is not interrupted. The system must be designed to withstand high transient and steady state overvoltages, however, and so its use is generally restricted to low and medium voltage distribution systems.

When there is an earth fault in an unearthed 3-phase system, the voltage of the faulted phase is reduced to the earth potential. This causes the phase voltage in the other two phases to increase, which causes a significant charging current between the phase-to-earth capacitances. This can cause arcing at the fault location. Many systems use a Petersen coil to compensate for this, thus eliminating the arcing problem. Such systems are called compensated networks. The network is earthed with an inductive reactor, where its reactance is made nominally equal to the total system capacitance to earth. Under this condition, a single-phase earth fault does not result in any steady state earth fault current.

The introduction of a Petersen coil introduces major difficulties when it comes to determining the direction of the fault. This is because the faulted line current is the sum of the inductive current introduced by the Petersen coil and the capacitive current of the line, which are in anti-phase with each other. If they are equal in magnitude, the current in the faulted line is zero. If the inductive current is larger than capacitance current, the direction of the faulted line current will appear to be in the same direction as that of the healthy line.

Standard directionalizing techniques used by conventional feeder protection devices are not adequate for this scenario, therefore we need a different method for determining the direction of the fault. Two commonly used methods are the First Half Wave method and the Residual Active Power method.

First Half Wave Method

The initial transient wave, generated at the fault point travels towards the bus along the faulted line, until it reaches the healthy line. For forward faults the high frequency fault voltage and current components are in opposite directions during the first half wave, whereas for reverse faults, they are in phase. This fact can be used to determine the fault direction. This method, however, is subject to the following disadvantages:

- The time duration of the characteristic is very short, in most cases not more than 3 ms. Because of this, it requires a high sampling frequency (3000Hz or even higher)
- It requires an analogue high pass filter, necessitating special hardware
- It is affected by the fault inception angle. For example, when the fault inception angle is 0°, there are no initial travelling waves.

Residual Active Power Method

Residual Active power, which is sometimes used to detect the instance of a fault can also in some cases be used for detecting the fault direction. Although the capacitive currents can be compensated by an inductive current generated by a Petersen coil, the active (instantaneous) current can never be compensated for and this is still opposite to that of the healthy line. This fact can also be used to directionalise the fault.

For a forward directional fault, the zero-sequence active power is the power loss of Petersen's coil, which is negative. For a reverse fault, the zero-sequence active power is the power loss of the transmission line, which is positive. This method, however, is subject to the following disadvantages:

- The zero-sequence active power will be very small in magnitude for a reverse directional fault. Its value depends on the power loss of transmission line.
- The zero-sequence active power may be too small in magnitude to be detected for a forward directional fault. Its value depends on the power loss of Petersen coil.
- High resolution CTs are required

Due to the low magnitude of measured values, reliability is compromised

This product does not use the above techniques for directionalisation. This product uses an innovative patented technique to determine the fault direction of earth faults in compensated networks. This method involves the use of Residual Active Power (RAP) in combination with Transient Reactive Power (TRP).

5.1 WDE IMPLEMENTATION

The P14D model provides two stages of Wattmetric Earth Fault protection (WDE). Each stage can be enabled or disabled with the settings ***WDE>1 Function*** and ***WDE>2 Function***.

Stage 1 always uses the Neutral CT input, but stage 2 can use either the Neutral CT input, or one of the phase CT inputs. You can select which CT input to use with the setting ***WDE>2 Res Cur***.

Cold Load Pickup

The WDE function can also be used with Cold Load Pickup (see Current Protection Functions chapter).

5.2 WDE LOGIC

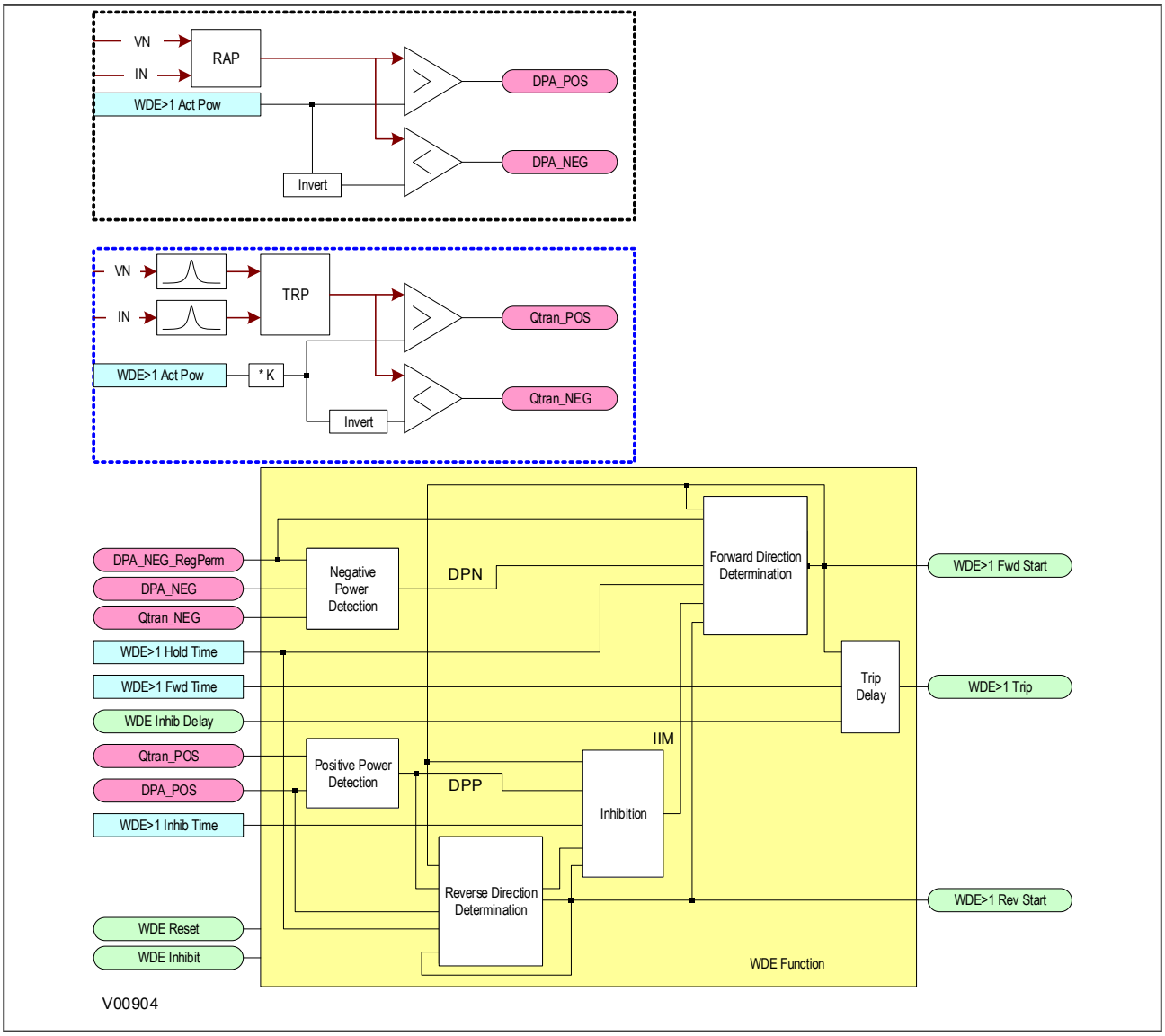


Figure 137: Wattmetric Earth Fault protection logic diagram

The Residual Active Power (RAP) is calculated and compared with the active power threshold setting to produce the internal signal **DPA_POS** (positive residual active power). It is compared with the inverse of the active power threshold to produce the internal signal **DPA_NEG** (negative residual active power).

Due to the fact the Petersen coil inductive impedance is very large for high frequencies, the high frequency components associated with the fault transients cannot be filtered out. Therefore by selecting the correct high frequency voltage and current components, we can directionalise the earth fault. We do this by passing the Residual Voltage and Current signals through bandpass filters. The resulting Transient Reactive Power (TRP) is calculated and compared with a quantity proportional to the active power threshold (K****WDE>(n) Act Pow***) to produce the internal signal **Qtran_POS** (positive transient reactive power). It is compared with the inverse of this quantity to produce the internal signal **Qtran_NEG** (negative transient reactive power).

The above signals are then fed into the WDE logic (shown above) to produce reverse and forward start signals and a trip signal.

Settings are also available for the three different timers:

WDE>1 Hold Time, ***WDE>2 Hold Time***: Settings for the hold timer stage 1 and stage 2.

WDE>1 Fwd Time, ***WDE>2 Fwd Time***: Settings for the forward time delay stage 1 and stage 2.

WDE>1 Inhib Time, ***WDE>2 Inhib Time***: Settings for the inhibit time stage 1 and stage 2.

6 TRANSIENT EARTH FAULT DETECTION

Some distribution systems run completely insulated from earth. Such systems are called unearthed systems. The advantage of an unearthed system is that a single phase to earth fault does not cause an earth fault current to flow. This means the whole system remains operational and the supply is not interrupted. The system must be designed to withstand high transient and steady state overvoltages, however, and so its use is generally restricted to low and medium voltage distribution systems.

When there is an earth fault in an unearthed 3-phase system, the voltage of the faulted phase is reduced to the earth potential. This causes the phase voltage in the other two phases to increase, which causes a significant charging current between the phase-to-earth capacitances. This can cause arcing at the fault location. Many systems use a Petersen coil to compensate for this, thus eliminating the arcing problem. Such systems are called compensated networks. The network is earthed with an inductive reactor, where its reactance is made nominally equal to the total system capacitance to earth. Under this condition, a single-phase earth fault does not result in any steady state earth fault current.

The introduction of a Petersen coil introduces major difficulties when it comes to determining the direction of the fault. This is because the faulted line current is the sum of the inductive current introduced by the Petersen coil and the capacitive current of the line, which are in anti-phase with each other. If they are equal in magnitude, the current in the faulted line is zero. If the inductive current is larger than capacitance current, the direction of the faulted line current will appear to be in the same direction as that of the healthy line.

Standard directionalizing techniques used by conventional feeder protection devices are not adequate for this scenario, therefore we need a different method for determining the direction of the fault. Two commonly used methods are the First Half Wave method and the Residual Active Power method.

First Half Wave Method

The initial transient wave, generated at the fault point travels towards the bus along the faulted line, until it reaches the healthy line. For forward faults the high frequency fault voltage and current components are in opposite directions during the first half wave, whereas for reverse faults, they are in phase. This fact can be used to determine the fault direction. This method, however, is subject to the following disadvantages:

- The time duration of the characteristic is very short, in most cases not more than 3 ms. Because of this, it requires a high sampling frequency (3000Hz or even higher)
- It requires an analogue high pass filter, necessitating special hardware
- It is affected by the fault inception angle. For example, when the fault inception angle is 0°, there are no initial travelling waves.

Residual Active Power Method

Residual Active power, which is sometimes used to detect the instance of a fault can also in some cases be used for detecting the fault direction. Although the capacitive currents can be compensated by an inductive current generated by a Petersen coil, the active (instantaneous) current can never be compensated for and this is still opposite to that of the healthy line. This fact can also be used to directionalise the fault.

For a forward directional fault, the zero-sequence active power is the power loss of Petersen's coil, which is negative. For a reverse fault, the zero-sequence active power is the power loss of the transmission line, which is positive. This method, however, is subject to the following disadvantages:

- The zero-sequence active power will be very small in magnitude for a reverse directional fault. Its value depends on the power loss of transmission line.
- The zero-sequence active power may be too small in magnitude to be detected for a forward directional fault. Its value depends on the power loss of Petersen coil.
- High resolution CTs are required

Due to the low magnitude of measured values, reliability is compromised

This product does not use the above techniques for directionalisation. This product uses an innovative patented technique called Transient Reactive Power method to determine the fault direction of an earth fault in a compensated network.

6.1 TEF OPERATION

A neutral ungrounded distribution power network could improve reliability of power supply. When a single phase to earth fault occurs, there is no closed circuit and no significant short-circuit current either, as the phase to phase voltages are still symmetrical. Therefore, immediate clearance of the fault is not required and the system is permitted to run for a relative long period during a single phase to earth fault. In most cases, a single-phase-to-earth fault is generally a temporary fault, so the power supply may not need to be interrupted. The circuit and the voltage diagrams are shown below:

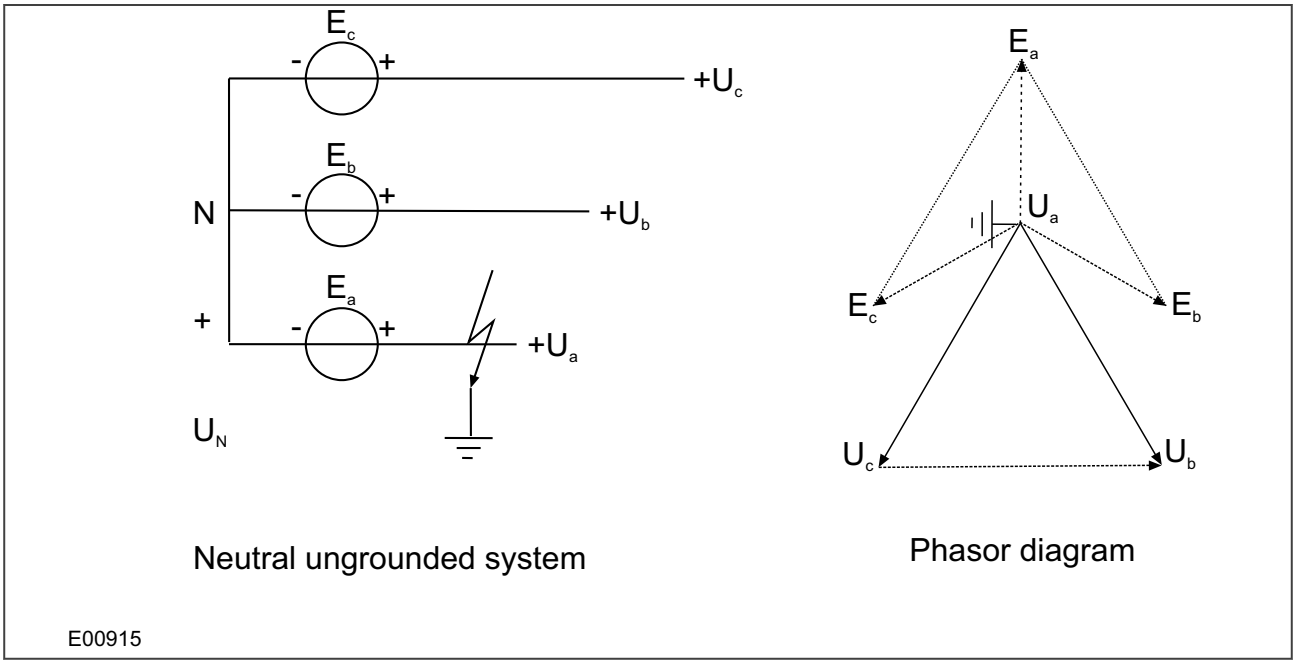


Figure 138: The neutral ungrounded system and phasor diagram of a single phase to earth fault

The disadvantage of neutral ungrounded system is that the overvoltage of non-fault phases are 1.732 times of rated voltage.

In practise, a closed circuit is made by the shunt capacitance of each phase, with single phase to earth faults being mostly arc faults. Where an extinguished arc reignites, it will cause a significant transient overvoltage (this could reach 2 to 3 times rated voltage) at the neutral point of the ungrounded system. In order to limit the overvoltage and avoid the reignition of an extinguished arc, the Petersen coil (which is also called arc suppression coil) is connected between the neutral point and earth.

6.2 TEFD IMPLEMENTATION

The figure below shows the connection of a Petersen coil. The function of the Petersen coil is to compensate the capacitive current, decreasing the fault arc current, as well as to limit the voltage of neutral point, and, limit the recovery voltage of the arc. Therefore, reducing the probability of arc reignition, and, at the same time limit the over-voltage caused by arc reignition.

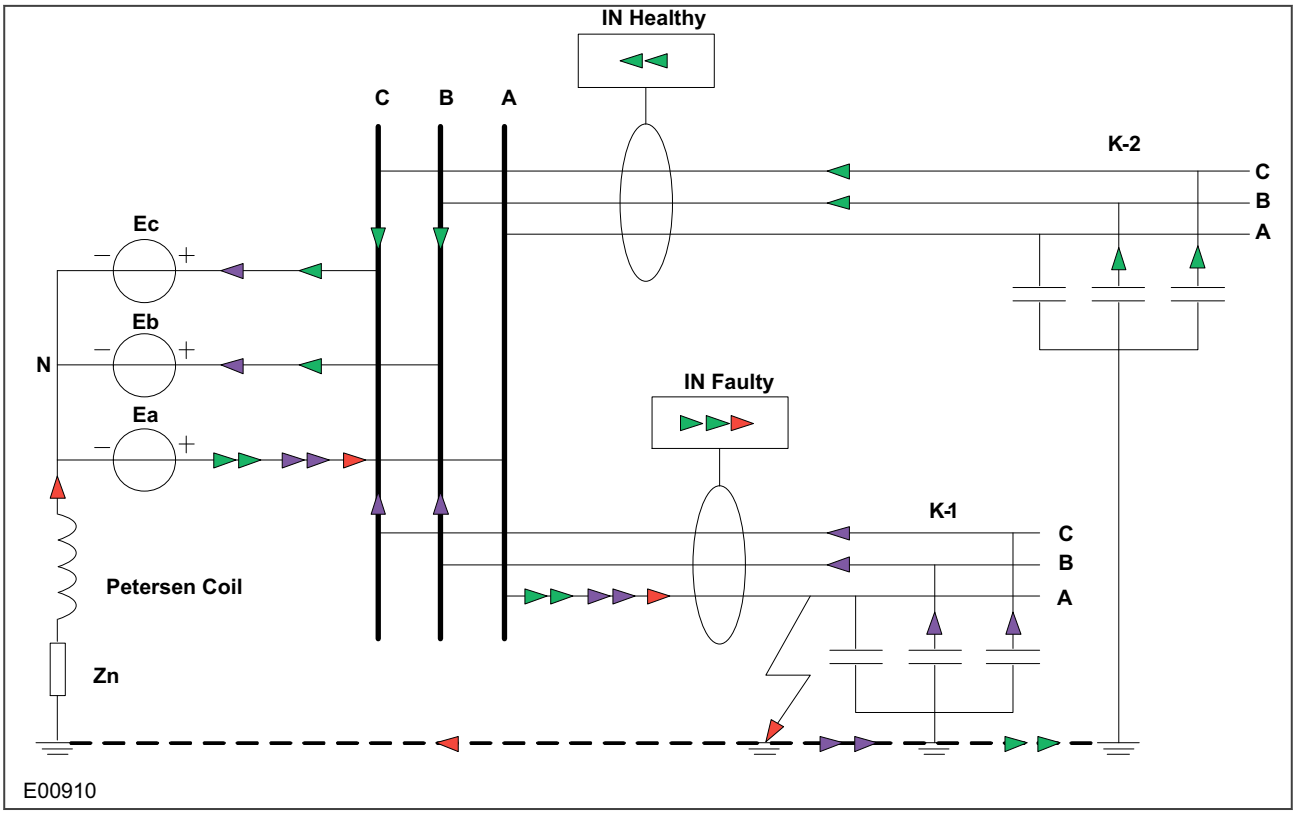


Figure 139: Petersen coil connection example

Earth fault detection for systems with Petersen coil grounded systems presents a particular technical difficulty due to small residual current after compensation. The figure above shows, in the case of a single-phase-to-earth fault occurring on feeder K-1, the relay on that feeder detects a fault in forward direction. However, the relays on other feeders detect the fault in reverse direction.

Note:
Zn is Petersen coil equivalent resistance.

In the above diagram, with the Petersen coil we have:

- Red: inductive (Petersen coil) current
- Purple: capacitive (faulty feeder) current
- Green: capacitive (healthy feeder) current

If Petersen coil inductance is calculated as |Red| = |Purple| + |Green|, then it is resonant compensation and there is no fault current.

According to the degree of compensation , there are three categories of Petersen coil compensation. These are: resonant compensation, under (capacitive) compensation and over (inductive) compensation.

A patented algorithm is used, which does not require special hardware or high acquisition frequency, to precisely determine the fault direction.

220Hz/264Hz residual voltage and current band pass filters are implemented in the TEFD design. Where voltage exceeds the current approaching 90 degrees, a forward directional fault is detected, and where current exceeds voltage approaching 90 degrees, a reverse directional fault is detected. Directional faults are detected regardless of the type of compensation used--ungrounded, Petersen coil or resistance grounded system.

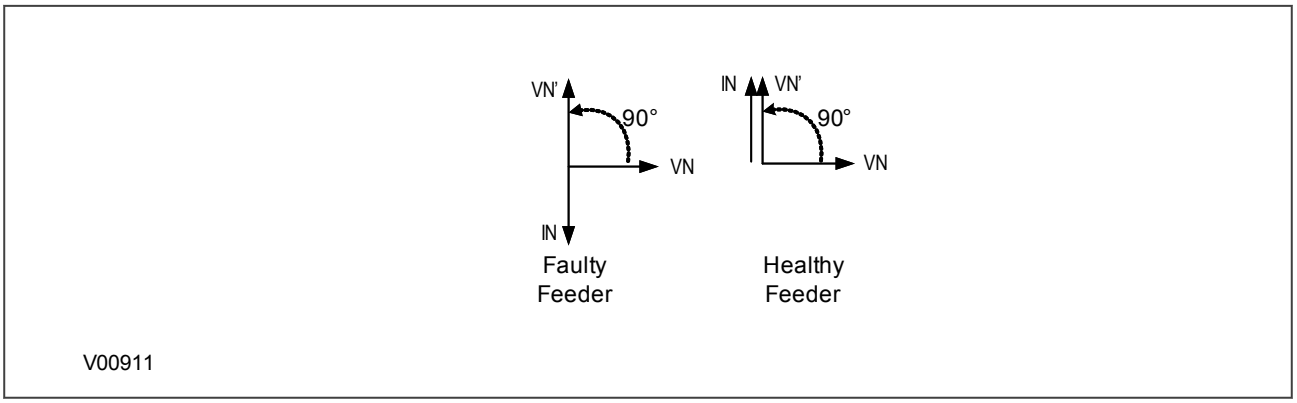


Figure 140: The relationship between VN and IN

The sampled residual voltage and current pass through a band pass voltage filter and current filter respectively, where frequency is fixed at 220Hz/264Hz internally for 50Hz/60Hz power systems. The band pass voltage filter also gets a 90-degree phase shift.

After residual voltage and current signals pass through the band pass filter, the average transient reactive power (AverageTransientQ) will be computed. If the fault is in opposite direction (faulty feeder), the result of AverageTransientQ will be negative, otherwise it will be positive.

The direction and power (AverageTransientQ and AverageTransientP) diagram is as follows:

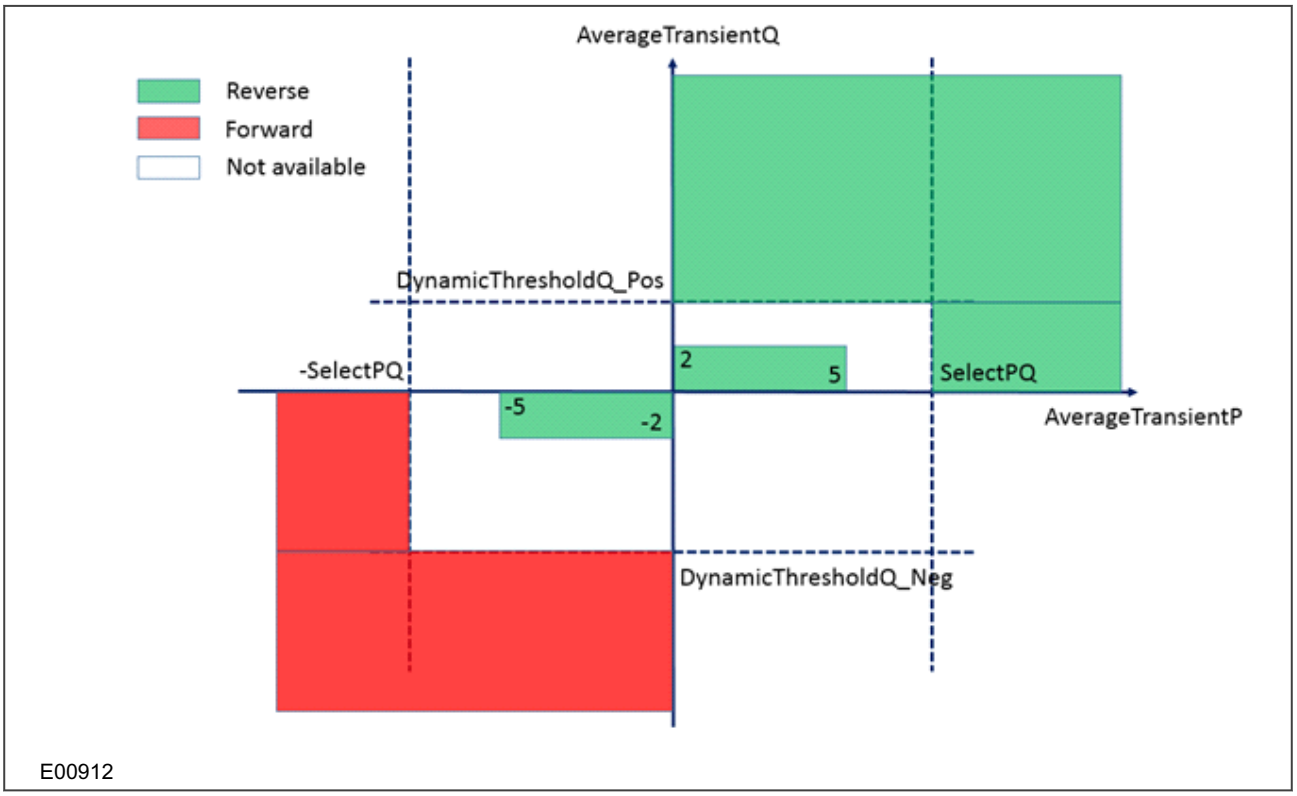


Figure 141: The relationship between direction and power

Note:
Q_Pos is internal DynamicThresholdQ_Pos, Q_Neg is internal DynamicThresholdQ_Neg
P_Pos is internal DynamicThresholdP_Pos, and P_Neg is internal DynamicThresholdP_neg--described below.
Refer to the TEFD Logic section for functional descriptions.

Taking the above diagram as an example:

- DynamicThresholdQ_Neg is less than -2 (VAr), DynamicThresholdQ_Pos is more than 2 (VAr).
- SelectPQ is more than 5 (W), and is more than |DynamicThresholdP_Neg|.
- Threshold of 2 (W) and 5 (W) are fixed in SmallP_Q block, when |MaximumQ|<2 and |MaximumP|<5, signal smallP_Q will be triggered internally 0.5s delayed from start signal, which leads to Reverse.
- "Not available" means this area does not exist or direction can not be determined.
- If the settings (Active Power and Select PQ) are different, the diagram maybe a little different, there might be some overlap area. Remember the priority is: Q>selectP>smallP_Q.

6.3 TEFD LOGIC

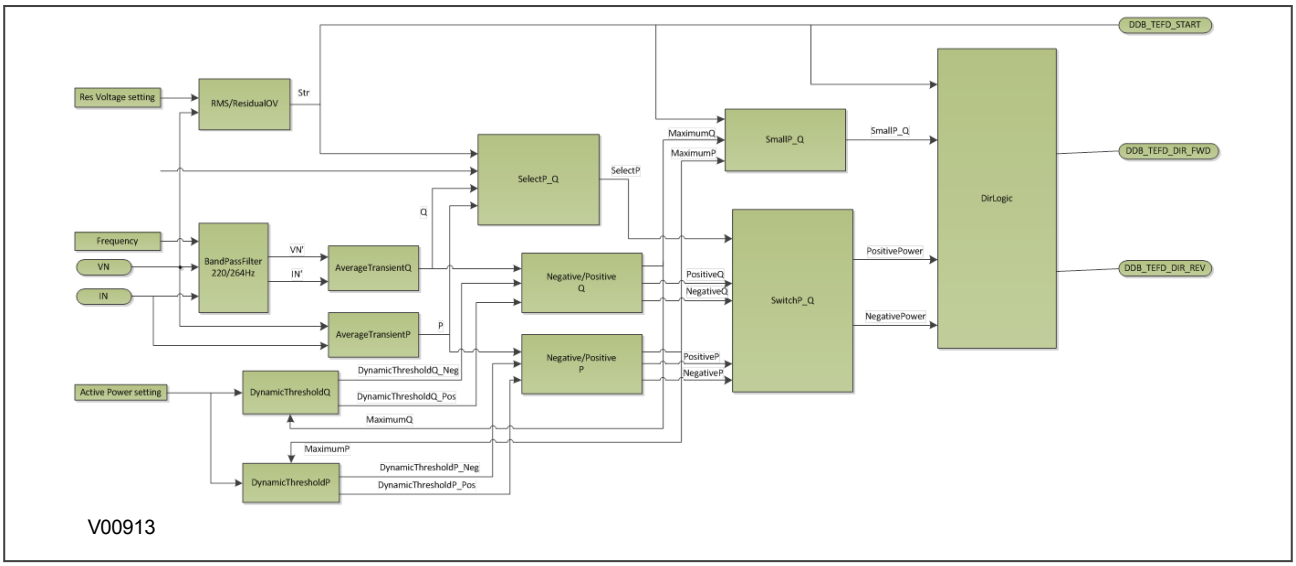


Figure 142: Transient earth fault logic overview

The AverageTransientP is computed as an average of active power of the residual voltage raw samples and the residual current raw samples. The AverageTransientQ is computed as an average of reactive power of the 220/264Hz band pass filtered residual voltage and residual current.

To avoid noise affecting our determination, we produce a dynamic threshold for the ***Active Power*** setting when the input signal is very large.

Mostly we can determine the direction by comparing AverageTransientQ with DynamicThresholdQ_Neg (the negative average transient reactive power leads to Forward), and DynamicThresholdQ_Pos (the positive average transient reactive power leads to Reverse).

However, in some cases the reactive power of AverageTransientQ is a little small, and the active power of AverageTransientP is a little large, we then switch to AverageTransientP to determine direction. In a similar way we can determine the direction by comparing AverageTransientP with DynamicThresholdP_Neg (the negative average transient active power leads to Forward), and DynamicThresholdP_Pos (the positive average transient active power leads to Reverse).

In some extreme cases, the AverageTransientQ and AverageTransientP are all very small, so then we produce the smallP_Q signal, which will lead to Reverse.

The internal negativePower, positivePower and smallP_Q signals are fed into DirLogic to produce forward and reverse signals.

Residual overvoltage start

The RMS value is calculated from the sampled residual voltage to produce DDB_TEFD_START (***TEFD Start***).

Dynamic threshold (The same logic for P and Q)

To avoid maloperation by noise when power is very large, we generate dynamic threshold for AverageTransientP and AverageTransientQ.

DynamicThresholdQ_Neg is computed from 2 x ***Active Power*** plus 10% of the maximum transient Q.
DynamicThresholdQ_Pos is computed from 1 x ***Active Power*** plus 10% of the maximum transient Q.
DynamicThresholdP_Neg is computed from 2 x ***Active Power*** plus 10% of the maximum transient P.
DynamicThresholdP_Pos is computed from 1 x ***Active Power*** plus 10% of the maximum transient P.

Power polarity (The same logic for P and Q)

- If AverageTransientQ is less than "-DynamicThresholdQ_Neg", that means it is negative (which leads to forward direction – faulty feeder)
- If AverageTransientQ is greater than DynamicThresholdQ_Pos, that means AverageTransientQ is positive (which leads to reverse direction – healthy feeder)

Select P and Q

The ***Select PQ*** setting is used to select AverageTransientP to estimate the direction instead of

AverageTransientQ in certain conditions. Internally, the selectP signal will issue after 0.01s delay timer from Start signal.

Switch P and Q

If selectP is false, the internal signals of negativeQ and positiveQ are used to decide the direction. Otherwise, if selectP is true, negativeP and positiveP are used to decide the fault direction.

Small P and Q

In specific conditions (e.g. high faulty resistance), the AverageTransientQ and AverageTransientP are all too small to decide the direction, to avoid maloperation, the direction will default as ***TEFD Dir Rev*** after 0.5s delay timer from ***TEFD Start***.

Direction logic

Negative power (Q or P) will lead to DDB_TEFD_DIR_FWD (***TEFD Dir Fwd***)--faulty, and positive power (positiveQ or positiveP) will lead to DDB_TEFD_DIR_REV (***TEFD Dir Rev***)--healthy. The direction will be held until the DDB_TEFD_START (***TEFD Start***) signal resets.

6.4 TEFD INTERFACE

Analogue Inputs

Input Name	Description
Residual Voltage	Residual voltage raw sample.
Residual Current	Residual current raw sample.

Digital Inputs

Input Name	Description
DDB_TEFD_INHIBIT (***TEFD Inhibit***)	This inhibit signal is used to halt TEFD.
DDB_TEFD_RESET (***TEFD Reset***)	This reset signal is used to reset whole TEFD function.

Settings

Setting Name	Description	Default	Min	Max	Step	Unit
Active Power	Power threshold, which is used to determine residual fault direction.	1.25	0.25	100	0.25	W
Res Voltage	Residual voltage start threshold, which is used to determine if TEFD starts or not.	15	5	100	0.25	V
Select PQ	Select PQ threshold, in certain situation the reactive power is very small (less than the select PQ threshold), but the active power is large (more than select PQ threshold), then we shift to use the active power to determine fault direction.	5	0.25	100	0.25	W
Frequency	Setting of system frequency, from *SYSTEM DATA*	50	50 or 60	50 or 60	10	Hz

DDB Outputs

Input Name	Description
DDB_TEFD_START (***TEFD Start***)	***TEFD Start*** is triggered when residual voltage is more than residual voltage threshold.
DDB_TEFD_FORWARD (***TEFD Dir Fwd***)	***TEFD Dir Fwd*** is triggered when forward direction (fault) is detected with residual voltage start.
DDB_TEFD_REVERSE (***TEFD Dir Rev***)	***TEFD Dir Rev*** is triggered when reverse direction (healthy) is detected with residual voltage start.

6.5 TEFD SETTING GUIDELINES

Res Voltage

We take 10% of the nominal voltage, which is 110 x 10%=11V as residual overvoltage threshold. Because the VT tolerance is 2%-5% and we need to avoid the tolerance range.

Active Power

We take 10% of the nominal current, which is 1 x 10%=0.1A as residual overcurrent threshold. Because CT tolerance is 2%-5% and we need to avoid the tolerance range.

From the above, we can select 11 x 0.1=1.1W or above as the ***Active Power*** threshold.

Select PQ

Assuming a secondary CT tolerance of 1 x 5%=0.05A, and a secondary VT tolerance of 110 x 5%=5.5V, minimum setting should be above 5.5 x 0.05=0.275W. The suggestion is to keep the default value of 5W as the recommended setting.

6.6 TEFD APPLICATION NOTE

As TEFD is designed to work with ungrounded or Petersen coil earthed systems, customers may not want to trip when TEFD detects a fault. Therefore, we should not have a trip DDB connected to ANY_TRIP DDB (Trip Command In) by default. To allow for this, the user can create a signal via the PSL. The figure below shows examples of TEFD detection raising both alarm and trip signals.

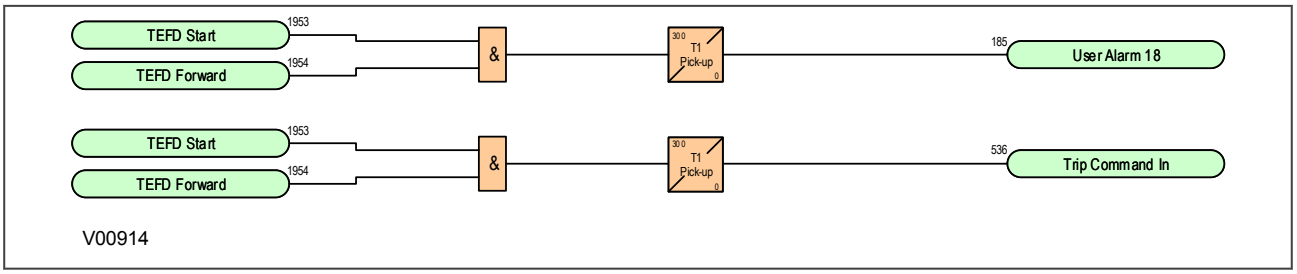


Figure 143: Transient earth fault alarm and trip examples

CHAPTER 13

AUTORECLOSE

1 CHAPTER OVERVIEW

Selected models of this product provide sophisticated Autoreclose (AR) functionality. The purpose of this chapter is to describe the operation of this functionality including the principles, logic diagrams and applications.

This chapter contains the following sections:

2 INTRODUCTION TO 3-PHASE AUTORECLOSE

It is known that approximately 80 - 90% of faults are transient in nature. This means that most faults do not last long and are self-clearing. A common example of a transient fault is an insulator flashover, which may be caused for example by lightning, clashing conductors or wind-blown debris.

A transient fault, such as an insulator flashover, is a self-clearing 'non-damage' fault. The flashover will cause one or more circuit breakers to trip, but it may also have the effect of clearing the fault. If the fault clears itself, the fault does not recur when the line is re-energised.

The remaining 10 – 20% of faults are either semi-permanent or permanent. A small tree branch falling on the line could cause a semi-permanent fault. Here the cause of the fault would not be removed by the immediate tripping of the circuit, but could be burnt away during a time-delayed trip. Permanent faults could be broken conductors, transformer faults, cable faults or machine faults, which must be located and repaired before the supply can be restored.

In the majority of fault incidents, if the faulty line is immediately tripped out, and time is allowed for the fault arc to deionise, reclosure of the circuit breakers will result in the line being successfully re-energised.

Autoreclose schemes are used to automatically reclose a circuit breaker a set time after it has been opened due to operation of a protection element.

On HV/MV distribution networks, autoreclosing is applied mainly to radial feeders, where system stability problems do not generally arise. The main advantages of using Autoreclose are:

- Minimal interruption in supply to the consumer
- Reduction of operating costs - fewer man hours in repairing fault damage and the possibility of running unattended substations
- With Autoreclose, instantaneous protection can be used which means shorter fault durations. This in turn means less fault damage and fewer permanent faults

Autoreclosing provides an important benefit on circuits using time-graded protection, in that it allows the use of instantaneous protection to provide a high speed first trip. With fast tripping, the duration of the power arc resulting from an overhead line fault is reduced to a minimum. This lessens the chance of damage to the line, which might otherwise cause a transient fault to develop into a permanent fault. Using instantaneous protection also prevents blowing of fuses in teed feeders, as well as reducing circuit breaker maintenance by eliminating pre-arc heating.

When instantaneous protection is used with autoreclosing, the scheme is normally arranged to block the instantaneous protection after the first trip. Therefore, if the fault persists after re-closure, the time-graded protection will provide discriminative tripping resulting in the isolation of the faulted section. However, for certain applications, where the majority of the faults are likely to be transient, it is common practise to allow more than one instantaneous trip before the instantaneous protection is blocked.

Some schemes allow a number of re-closures and time-graded trips after the first instantaneous trip, which may result in the burning out and clearance of semi-permanent faults. Such a scheme may also be used to allow fuses to operate in teed feeders where the fault current is low.

When considering feeders that are partly overhead line and partly underground cable, any decision to install auto-reclosing should be subject to analysis of the data (knowledge of the frequency of transient faults). This is because this type of arrangement probably has a greater proportion of semi-permanent and permanent faults than for purely overhead feeders. In this case, the advantages of autoreclosing are small. It can even be disadvantageous because re-closing on to a faulty cable is likely to exacerbate the damage.

3 IMPLEMENTATION

Autoreclose functionality is a software option, which is selected when ordering the device, so this description only applies to models with this option.

Autoreclose works for phase overcurrent (POC) earth fault (EF) and sensitive earth fault (SEF) protection. It is implemented in the *AUTORECLOSE* column of the relevant settings group. In addition to the settings contained in this column, you will also need to make some settings in the blocking cells of the relevant protection columns.

The Autoreclose function can be set to perform a single-shot, two-shot, three-shot or four-shot cycle. You select this by the ***Number of Shots*** cell in the *AUTORECLOSE* column. You can also initiate a separate Autoreclose cycle for the SEF protection, with a different number of shots, selected by the ***Number SEF Shots*** cell. Dead times for all shots can be adjusted independently.

An Autoreclose cycle can be initiated internally by operation of a protection element, or externally by a separate protection device. The dead time starts in one of two cases; when the circuit breaker has tripped, or when the protection has reset. You select this using the ***Start Dead t On*** cell.

At the end of the relevant dead time, a ***CB Closed 3 ph*** signal is given, providing it is safe for the circuit breaker to close. This is determined by checking that certain system conditions are met as specified by the **System *Checks*** functionality.

It is safe to close the circuit breaker providing that:

- only one side of the circuit breaker is live (either dead line / live bus, or live line / dead bus), or
- if both bus and line sides of the circuit breaker are live, the system voltages are synchronised.

In addition, the energy source powering the circuit breaker (for example the closing spring) must be fully charged. This is indicated from the ***CB Healthy*** DDB input.

When the CB has closed, the reclaim time starts. If the circuit breaker does not trip again, the Autoreclose function resets at the end of the set reclaim time. If the protection operates during the reclaim time the device either advances to the next shot in the Autoreclose cycle, or if all reclose attempts have been made, goes to lockout.

CB Status signals must also be available, so the default setting for ***CB Status Input*** should be modified according to the application. The default PSL requires 52A, 52B and CB Healthy logic inputs, so a setting of both **52A and 52B** would be required for the ***CB Status Input*** if used with the default PSL.

4 AUTORECLOSE FUNCTION INPUTS

The Autoreclose function has several logic inputs, which can be mapped to any of the opto-inputs or to one or more of the DDB output signals generated by the PSL. The functions of these inputs are described below.

4.1 CB HEALTHY

It is necessary to establish if there is sufficient energy in the circuit breaker (spring charged, gas pressure healthy, etc.) before the CB can be closed. This ***CB Healthy*** input is used to ensure this before initiating a ***CB closed 3ph*** command. If on completion of the dead time, the ***CB Healthy*** input is low, and remains low for a period given by the ***CB Healthy Time*** timer, lockout will result and the circuit breaker will remain open.

The majority of circuit breakers are only capable of providing a single trip-close-trip cycle, in which case the ***CB Healthy*** signal would stay low after one Autoreclose shot, resulting in lockout.

This check can be disabled by not allocating an opto-input for the ***CB Healthy*** signal, whereby the signal defaults to a High state.

4.2 BLOCK AR

The ***Block AR*** input blocks the Autoreclose function and causes a lockout. It can be used when protection operation without Autoreclose is required. A typical example is on a transformer feeder, where Autoreclose may be initiated by the feeder protection but blocked by the transformer protection.

4.3 RESET LOCKOUT

The ***Reset Lockout*** input can be used to reset the Autoreclose function following lockout. It also resets any Autoreclose alarms, provided that the signals that initiated the lockout have been removed.

4.4 AR AUTO MODE

The ***AR Auto Mode*** input is used to select the Auto operating mode. In this mode, the Autoreclose function is in service.

4.5 AR LIVELINE MODE

The ***AR LiveLine Mode*** input is used to select the Live Line operating mode when Autoreclose is out of service and all blocking of instantaneous protection by Autoreclose is disabled. This operating mode takes precedence over all other operating modes for safety reasons, as it indicates that utility personnel are working near live equipment.

4.6 TELECONTROL MODE

The ***Telecontrol*** input is used to select the Telecontrol operating mode so that the Auto and Non-auto modes of operation can be selected remotely.

4.7 LIVE/DEAD CCTS OK (LIVE/DEAD CIRCUITS OK)

The ***LiveDead Ccts OK*** signal is a signal indicating the status of the Live Line / Dead Bus or Live Bus / Dead Line system conditions (High = OK, Low = Not OK). The logic required can be derived in the PSL from the Live Line, Dead Line, Live Bus and Dead Bus signals in the System Check logic (if applicable), or it can come from an external source depending on the application.

4.8 AR SYS CHECKS (AR SYSTEM CHECKS)

The ***AR Sys Checks*** signal can be mapped from the system checks output ***SysChks Inactive***, to enable auto-reclosing without any system checks, providing the ***System Checks*** setting in the *CONFIGURATION* column is

disabled. This mapping is not essential, because the ***No System Checks*** setting in the *AUTORECLOSE* column can be enabled to achieve the same effect.

This DDB can also be mapped to an opto-input, to allow the IED to receive a signal from an external system monitoring device, indicating that the system conditions are suitable for CB closing. This should not normally be necessary, since the IED has comprehensive built in system check functionality.

4.9 EXT AR PROT TRIP (EXTERNAL AR PROTECTION TRIP)

The ***Ext AR Prot Trip*** signal allows Autoreclose initiation by a Trip from a separate protection device.

4.10 EXT AR PROT START (EXTERNAL AR PROTECTION START)

The ***Ext AR Prot Strt*** signal allows Autoreclose initiation by a Start from a separate protection device.

4.11 DAR COMPLETE (DELAYED AUTORECLOSE COMPLETE)

Some utilities require Delayed Autoreclose (DAR) functionality.

The ***DAR Complete*** signal can, if required, be mapped in PSL to provide a short pulse when a CB Close command is given at the end of the dead time. If ***DAR Complete*** is activated during an Autoreclose cycle, the output signal ***DAR in Progress*** resets, even though the reclaim time may still be running, and ***AR in Progress*** remains set until the end of the reclaim time.

For most applications, ***DAR complete*** can be ignored (not mapped in PSL). In such cases, **DAR in *Progress*** operates and resets in parallel with ***AR in Progress***.

4.12 CB IN SERVICE (CIRCUIT BREAKER IN SERVICE)

The ***CB In Service*** signal must remain asserted when protection operates if autoreclose is to be initiated. For most applications, it can be mapped to ***CB Closed 3ph***. More complex PSL mapping can be programmed if required, for example where it is necessary to confirm not only that the CB is closed but also that the line and/or bus VT is actually live up to the instant of protection operation.

4.13 AR RESTART

In some applications, it is sometimes necessary to initiate an Autoreclose cycle by means of connecting an external signal to an opto-input. This would be when the normal interlock conditions are not all satisfied, i.e. when the CB is open and the associated feeder is dead. If the ***AR Restart*** input is mapped to an opto-input, activation of that opto-input will initiate an Autoreclose cycle irrespective of the status of the ***CB in Service*** input, provided the other interlock conditions, are still satisfied.

4.14 DT OK TO START (DEAD TIME OK TO START)

This is an optional extra interlock in the dead time initiation logic. In addition to the CB being open and the protection reset, ***DT OK To Start*** has to be set high to allow the dead time function to be primed after an AR cycle has started. Once the dead time function is primed, this signal has no further affect – the dead time function stays primed even if the signal subsequently goes low. A typical PSL mapping for this input is from the ***Dead Line*** signal from the System Check logic. This would enable dead time priming only when the feeder has gone dead after CB tripping. If this extra dead time priming interlock is not required, ***DT OK To Start*** can be left unmapped, and it will default to a high state.

4.15 DEADTIME ENABLED

This is an optional interlock in the dead time logic. This signal has to be high to allow the dead time to run. If this signal goes low, the dead time stops and resets, but stays primed, and will restart from zero when it goes high again. A typical PSL mapping is from the ***CB Healthy*** input or from selected signals from the System Check logic. It

could also be mapped to an opto-input to provide a 'hold off' function for the follower CB in a 'master/follower' application with 2 CBs. If this optional interlock is not required, ***DeadTime Enabled*** can be left unmapped, and it will default to a high state.

4.16 AR INIT TRIPTEST (INITIATE TRIP TEST)

If ***AR Init TripTest*** is mapped to an opto-input, and that input is activated momentarily, the IED generates a CB trip output via ***AR Trip Test***. The default PSL then maps this to output to the trip output relay and initiates an Autoreclose cycle.

4.17 AR SKIP SHOT 1

If ***AR Skip Shot 1*** is mapped to an opto-input, and that input is activated momentarily, the IED logic will cause the Autoreclose sequence counter to increment by 1. This will decrease the available number of reclose shots and will lockout the re-closer.

4.18 INH RECLAIM TIME (INHIBIT RECLAIM TIME)

If ***Inh Reclaim Time*** is mapped to an opto-input, and that input is active at the start of the reclaim time, the IED logic will cause the reclaim timers to be blocked.

5 AUTORECLOSE FUNCTION OUTPUTS

The Autoreclose function has several logic outputs, which can be assigned to output relay contacts, monitor bits in the *COMMISSION TESTS* column, or the PSL. The functions of these outputs are described below.

5.1 AR IN PROGRESS

This signal is present during the complete re-close cycle from the start of protection to the end of the reclaim time or lockout.

5.2 DAR IN PROGRESS

This operates together with the ***AR In Progress*** signal at the start of Autoreclose. If ***DAR Complete*** does not operate, ***DAR in Progress*** remains operated until ***AR In Progress*** resets at the end of the cycle. If ***DAR Complete*** goes high during the Autoreclose cycle, ***DAR in Progress*** resets.

5.3 SEQUENCE COUNTER STATUS DDB SIGNALS

During each Autoreclose cycle a sequence Counter increments by 1 after each fault trip and resets to zero at the end of the cycle.

- ***AR SeqCounter 0*** is set when the counter is at zero
- ***AR SeqCounter 1*** is set when the counter is at 1
- ***AR SeqCounter 2*** is set when the counter is at 2
- ***AR SeqCounter 3*** is set when the counter is at 3
- ***AR SeqCounter 4*** is set when the counter is at 4

5.4 SUCCESSFUL CLOSE

The ***Successful Close*** output indicates that an Autoreclose cycle has been successfully completed. A successful Autoreclose signal is given after the protection has tripped the CB and it has reclosed successfully. The successful Autoreclose output is reset at the next CB trip or from one of the reset lockout methods.

5.5 AR IN SERVICE

The ***AR In Service*** output indicates whether the Autoreclose is in or out of service. Autoreclose is In Service when the device is in ***Auto*** mode and Out of Service when in the ***Non Auto*** and ***Live Line*** modes.

5.6 AR BLK MAIN PROT (BLOCK MAIN PROTECTION)

The ***AR Blk Main Prot*** signal blocks the DT-only stages (instantaneous stages) of the main current protection elements. These are ***I>3, I>4, I>6, IN1>3, IN1>4, IN2>3,*** and ***IN2>4.*** You block the instantaneous stages for each trip of the Autoreclose cycle using the Overcurrent and Earth Fault 1 and 2 settings, ***I> Blocking, IN1> Blocking, IN2> Blocking*** and the ***Trip 1 Main, Trip 2 Main, Trip 3 Main, Trip 4 Main*** and ***Trip 5 Main*** settings.

5.7 AR BLK SEF PROT (BLOCK SEF PROTECTION)

The ***AR Blk SEF Prot*** signal blocks the DT-only stages (instantaneous stages) of the SEF protection elements. These are ***ISEF>3***, and ***ISEF>4***. You block the instantaneous SEF stages for each trip of the Autoreclose cycle using the *SEF PROTECTION* setting ***ISEF> Blocking***, and the ***Trip 1 SEF***, ***Trip 2 SEF***, ***Trip 3 SEF***, ***Trip 4 SEF*** and ***Trip 5 SEF*** settings.

5.8 RECLOSE CHECKS

The ***Reclose Checks*** output indicates that the AR System Checks are in progress.

5.9 DEADTIME IN PROG

The ***DeadTime in Prog*** output indicates that the dead time is in progress. This signal is set when ***Reclose Checks*** is set AND input ***Dead TimeEnabled*** is high. This may be useful during commissioning to check the operation of the Autoreclose cycle.

5.10 DT COMPLETE (DEAD TIME COMPLETE)

DT *Complete* (Dead time complete) operates at the end of the set dead time, and remains operated until either the scheme resets at the end of the reclaim time or a further protection operation or Autoreclose initiation occurs. It can be applied purely as an indication, or included in PSL mapping to logic input ***DAR Complete***.

5.11 AR SYNC CHECK (AR SYNCHRONISATION CHECK)

AR Sync Check indicates that the Autoreclose Synchronism checks are satisfactory. This is when either of the synchronisation check modules (CS1 or CS2), confirms an In-Synchronism condition.

5.12 AR SYSCHECKS OK (AR SYSTEM CHECKS OK)

AR SysChecks OK indicates that the Autoreclose System checks are satisfactory. This is when any selected system check condition (synchronism check, live bus/dead line etc.) is confirmed.

This DDB signal ihas the number 463 and is an output from the Autoreclose function (i.e. a PSL input). It should not be confused with DDB signal 403, which is an input to the Autoreclose function (i.e. a PSL output).

5.13 AUTO CLOSE

The ***Auto Close*** output indicates that the Autoreclose logic has issued a `Close` signal to the CB. This output feeds a signal to the control close pulse timer and remains on until the CB has closed. This signal may be useful during commissioning to check the operation of the Autoreclose cycle.

5.14 PROTECTION LOCKT (PROTECTION LOCKOUT)

Protection Lockt (Protection Lockout) operates if ***AR lockout*** is triggered by protection operation either during the inhibit period following a manual CB close or when the device is in ***Non-auto*** or ***Live Line*** mode.

5.15 RESET LCKOUT ALM (RESET LOCKOUT ALARM)

Reset Lckout Alm operates when the device is in ***Non-auto mode***, if the ***Reset Lockout*** setting is set to `Select Non Auto`.

5.16 RECLAIM IN PROG

Reclaim in Prog output indicates that a reclaim timer is in progress and will drop-off once the reclaim timer resets.

5.17 RECLAIM COMPLETE

Reclaim Complete operates at the end of the set reclaim time and is a fast reset. To maintain the output indication a dwell timer has to be implemented in PSL.

6 AUTORECLOSE FUNCTION ALARMS

The following DDB signals will produce an alarm. These are described below.

6.1 AR NO SYS CHECK

The ***AR No Sys Check*** alarm indicates that the system voltages are not suitable for autoreclosing at the end of the system check time (setting ***Sys Check Time***), leading to a lockout condition. This alarm is latched and must be reset manually.

6.2 AR CB UNHEALTHY

The ***AR CB Unhealthy*** alarm indicates that the **CB *Healthy*** input was not energised at the end of the *CB Healthy Time*, leading to a lockout condition. This alarm is latched and must be reset manually.

6.3 AR LOCKOUT

The ***AR Lockout*** alarm indicates that the device is in a lockout status and that further re-close attempts will not be made. This alarm can configured to reset automatically (self-reset) or manually as determined by the setting ***Reset Lockout by*** in the *CB CONTROL* column.

7 AUTORECLOSE OPERATION

The Autoreclose function is a complex function consisting of several modules interacting with one another. This is described in terms of separate logic diagrams, which link together by means of Internal signals (depicted by the pink-coloured boxes. To help you with the analysis of the various Autoreclose modules, the following table describes how these internal signals link up in the various logic diagrams. Each internal signal is allocated with an ID, and the diagrams on which they appear are also identified.

Internal signal ID	Input to AR function	Appearing in diagrams	Output from AR function	Appearing in diagrams
1	Autoreclose Disabled	V00505, V00507	Autoreclose Disabled	V00501
2	Live Line Mode	V00505, V00507, V00514	Live Line Mode	V00501
3	Non Auto Mode	V00505, V00507, V00514	Non Auto Mode	V00501
4	Auto Mode (int)	V00505, V00507, V00512	Auto Mode (int)	V00501
5	Main Protection Start	V00504, V00505, V00507, V00511, V00512	Main Protection Start	V00502
6	SEF Protection Start	V00504, V00505, V00511, V00512	SEF Protection Start	V00502
7	Main Protection Trip	V00505, V00513, V00514	Main Protection Trip	V00503
8	SEF Protection Trip	V00505, V00507, V00513, V00514	SEF Protection Trip	V00503
9	Block Autoreclose	V00513	Block Autoreclose	V00515
10	SC Count >= Main Shots	V00504	SC Count >= Main Shots	V00505
11	SC Count >= SEF Shots	V00504	SC Count >= SEF Shots	V00505
12	Main High Shots	V00505, V00513	Main High Shots	V00504
13	SEF High Shots	V00505, V00513	SEF High Shots	V00504
14	Autoreclose Inhibit	V00505, V00507, V00514	Autoreclose Inhibit	V00512
15	Autoreclose Start	V00508, V00509, V00511, V00513	Autoreclose Start	V00505
16	Autoreclose Initiate	V00508, V00513	Autoreclose Initiate	V00505
17	SC Count > 4	V00506	SC Count > 4	V00505
18	Block Main Prot Trips	V00507	Block Main Prot Trips	V00506
19	Block SEF Prot Trips	V00507	Block SEF Prot Trips	V00506
20	Hold Reclaim Output	V00511	Hold Reclaim Output	V00509

7.1 OPERATING MODES

The Autoreclose function has three operating modes:

- Auto Mode: Autoreclose is in service
- Non-auto Mode: Autoreclose is out of service AND the chosen protection functions are blocked if setting ***AR Deselected*** = `Block Inst Prot.`
- Live Line Mode: Autoreclose is out of service, but protection functions are NOT blocked, even if setting ***AR Deselected*** = `Block Inst Prot.`

Note:
Live Line Mode provides extra security for live line working on the protected feeder.

The Autoreclose function must first be enabled in the *CONFIGURATION* column. You can then select the operating mode according to application requirements. The basic method of mode selection is determined by the setting ***AR Mode Select*** in the *AUTORECLOSE* column, as summarised in the following table:

AR Mode Select Setting	Description
Command Mode	Auto or Non-auto mode selection is determined by the command cell ***Autoreclose Mode*** in the *CB CONTROL* column.
Opto Set Mode	Auto or Non-auto mode selection is determined by an opto-input mapped to ***AR Auto Mode*** If the ***AR Auto Mode*** input is high, Auto operating mode is selected. If the ***AR Auto Mode*** input is low, Non-Auto operating mode is selected.
User Set Mode	Auto or Non-auto mode selection is controlled by the ***Telecontrol Mode*** input. If the ***Telecontrol Mode*** input is high, the setting ***Autoreclose Mode*** in the *CB CONTROL* column is used to select Auto or Non Auto operating mode. If the ***Telecontrol Mode*** input is low, it behaves as for the `Opto Set Mode` setting.
Pulse Set Mode	Auto or Non-auto mode selection is determined by the falling edge of ***AR Auto Mode*** signal. If the Telecontrol input is high, the operating mode is toggled between Auto and Non Auto Mode on the falling edge of the ***AR Auto Mode*** signal as it goes low. The Auto Mode pulses are produced by the SCADA system. If the Telecontrol input is low, it behaves as for the ***Opto Set Mode*** setting.

The Live Line Mode is controlled by ***AR LiveLine Mode***. If this is high, the scheme is forced into Live Line Mode irrespective of the other signals.

7.1.1 FOUR-POSITION SELECTOR SWITCH IMPLEMENTATION

It is quite common for some utilities to apply a four position selector switch to control the mode of operation. This application can be implemented using the DDB signals ***AR LiveLine Mode***, ***AR Auto Mode*** and ***Telecontrol Mode***. This is demonstrated in the following diagram.

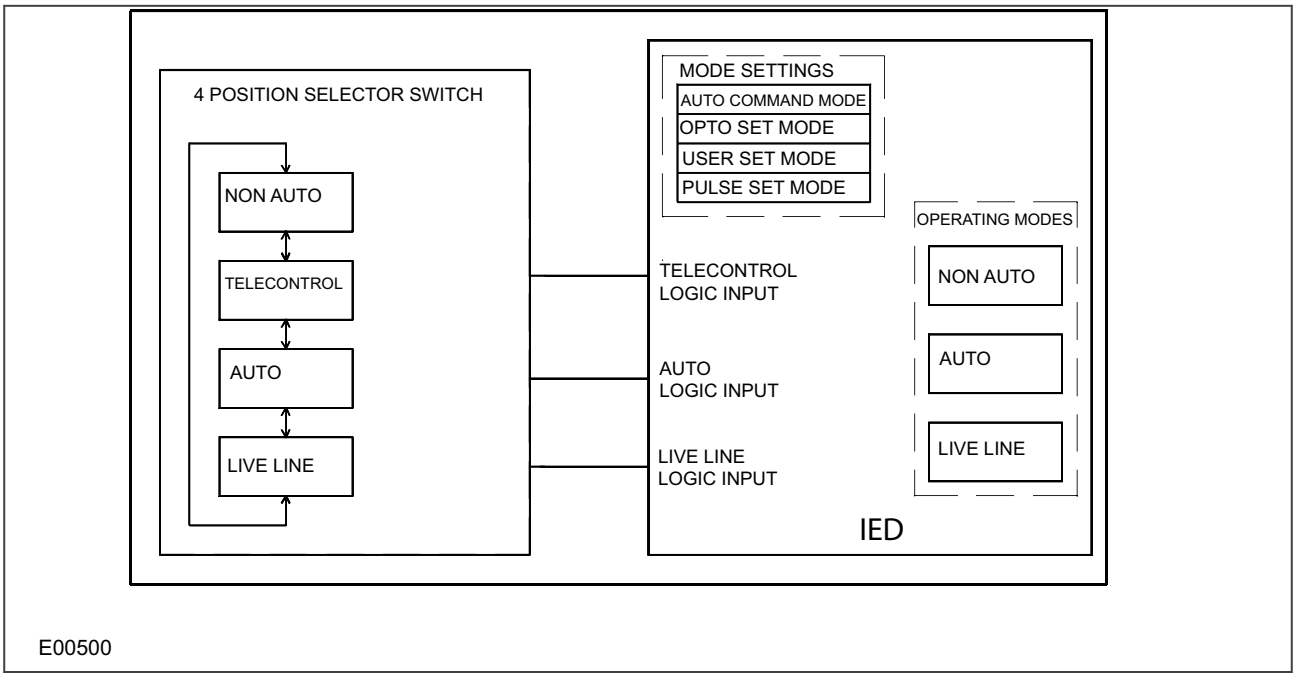


Figure 144: Four-position selector switch implementation

The required logic truth table for this arrangement is as follows:

Switch position	AR Auto Mode	Telecontrol Mode	AR Live Line Mode
Non-auto	0	0	0
Telecontrol	0 or SCADA pulse	1	0
Auto	1	0	0
Live Line	0	0	1

7.1.2 OPERATING MODE SELECTION LOGIC

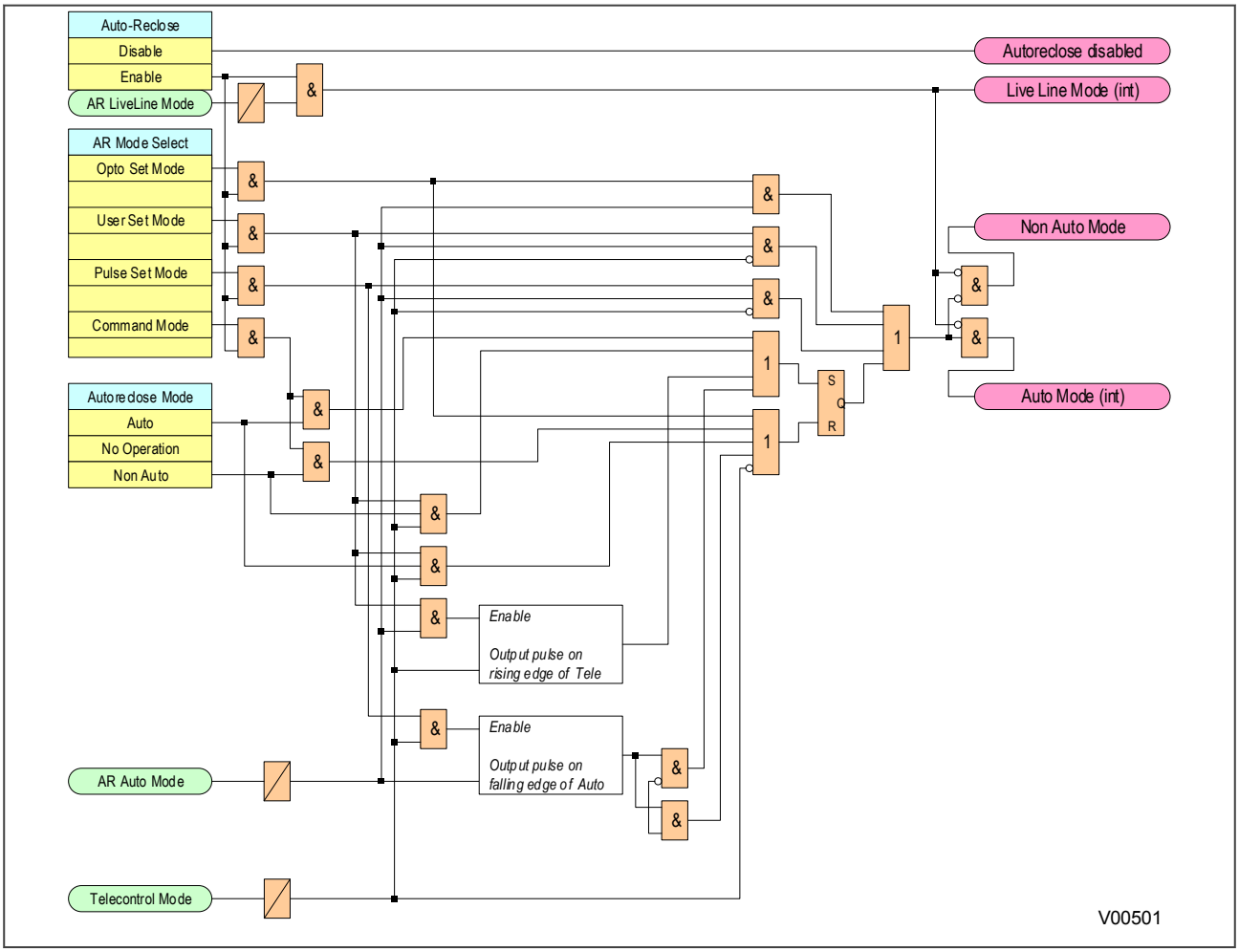


Figure 145: Autoreclose mode select logic

The mode selection logic includes a 100 ms delay for ***Auto Mode***, ***Telecontrol*** and ***Live Line*** logic inputs, to ensure a predictable change of operating modes. This is of particular importance for the case when the four position switch does not have 'make-before-break' contacts. The logic also ensures that when the switch is moved from Auto or Non-Auto position to Telecontrol, the scheme remains in the previously selected mode (Auto or Non-Auto) until a different mode is selected by remote control.

For applications where live line operating mode and remote selection of Auto/Non-auto modes are not required, a simple two position switch can be arranged to activate ***Auto Mode*** input. In this case, the ***Live Line*** and ***Telecontrol*** inputs would be unused.

7.2 AUTORECLOSE INITIATION

Autoreclose is usually initiated from the IED's internal protection function. Different stages of phase overcurrent and earth fault protection can be programmed to initiate or block the main Autoreclose function. The stages of sensitive earth fault protection can also be programmed to initiate or block both the Main Autoreclose function or the SEF Autoreclose function.

The associated settings are found in the *AUTORECLOSE* column under the sub-heading *AR INITIATION*.

For example:

If ***I>1 AR*** is set to `Initiate Main AR`, operation of the ***I>1*** protection stage will initiate Autoreclose

If ***ISEF>1 AR*** is set to `No Action`, operation of the ***ISEF>1*** protection stage will lead to a CB trip but no reclose. Otherwise it can be used to initiate Main autoreclose or SEF autoreclose.

> *Note:*
> *A selection must be made for each protection stage that is enabled.*

A separate protection device may also initiate Autoreclose. The Autoreclose can be initiated from a protection Trip, or when sequence coordination is required from a protection Start. If external triggering of Autoreclose is required, the following DDB signals should be mapped to opto-inputs:

- ***Ext AR Prot Trip***
- ***Ext AR Prot Strt*** (if applicable)

In addition, the setting ***Ext Prot*** should be set to `Initiate Main AR`.

Although a protection start and a protection trip can initiate an AR cycle, several checks still have to be performed before the initialisation signal is given. Some of the checks are listed below:

- ***Auto Mode*** has been selected
- ***Live line mode*** is disabled
- The number of main protection and SEF shots have not been reached
- Sequence co-ordination is enabled (for protection start to initiate AR. This is not necessary if a protection trip is doing the initiating)
- The ***CB Ops Lockout*** DDB signal is not set
- The ***CB in Service*** DDB signal is high

> *Note:*
> *The relevant protection trip must be mapped to the **Trip Command In** DDB.*

7.2.1 START SIGNAL LOGIC

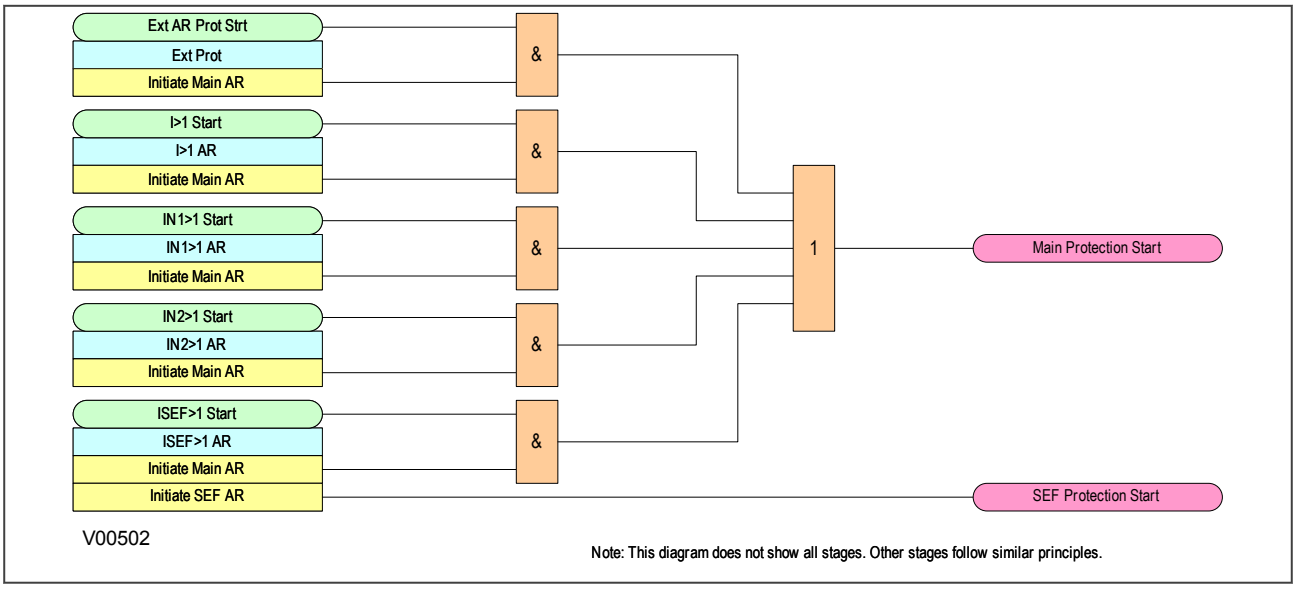


Figure 146: Start signal logic

7.2.2 TRIP SIGNAL LOGIC

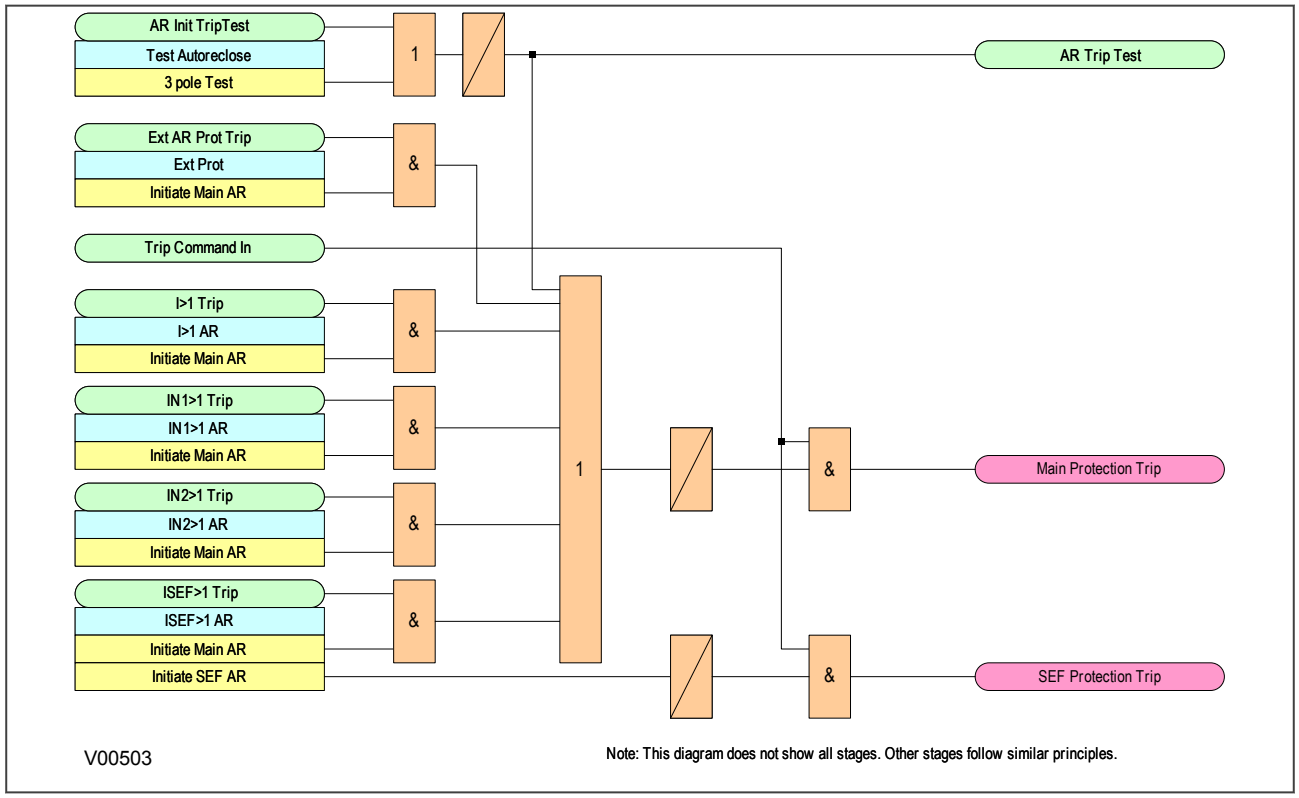


Figure 147: Trip signal logic

7.2.3 BLOCKING SIGNAL LOGIC

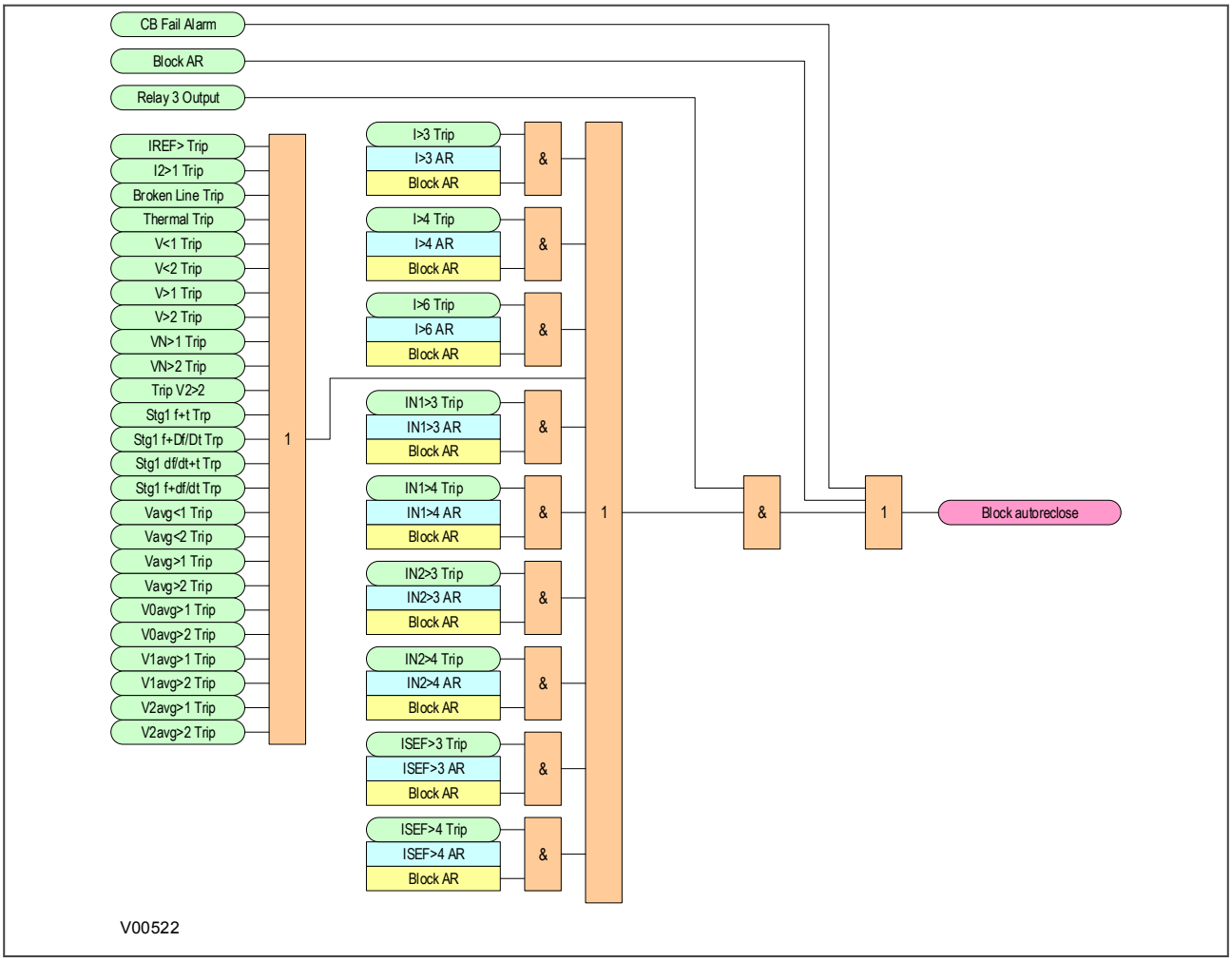


Figure 148: Blocking signal logic

7.2.4 SHOTS EXCEEDED LOGIC

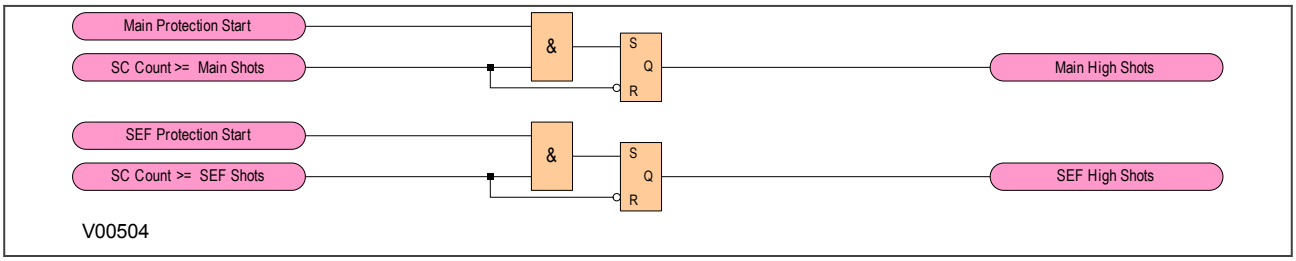


Figure 149: Shots Exceeded logic

7.2.5 AR INITIATION LOGIC

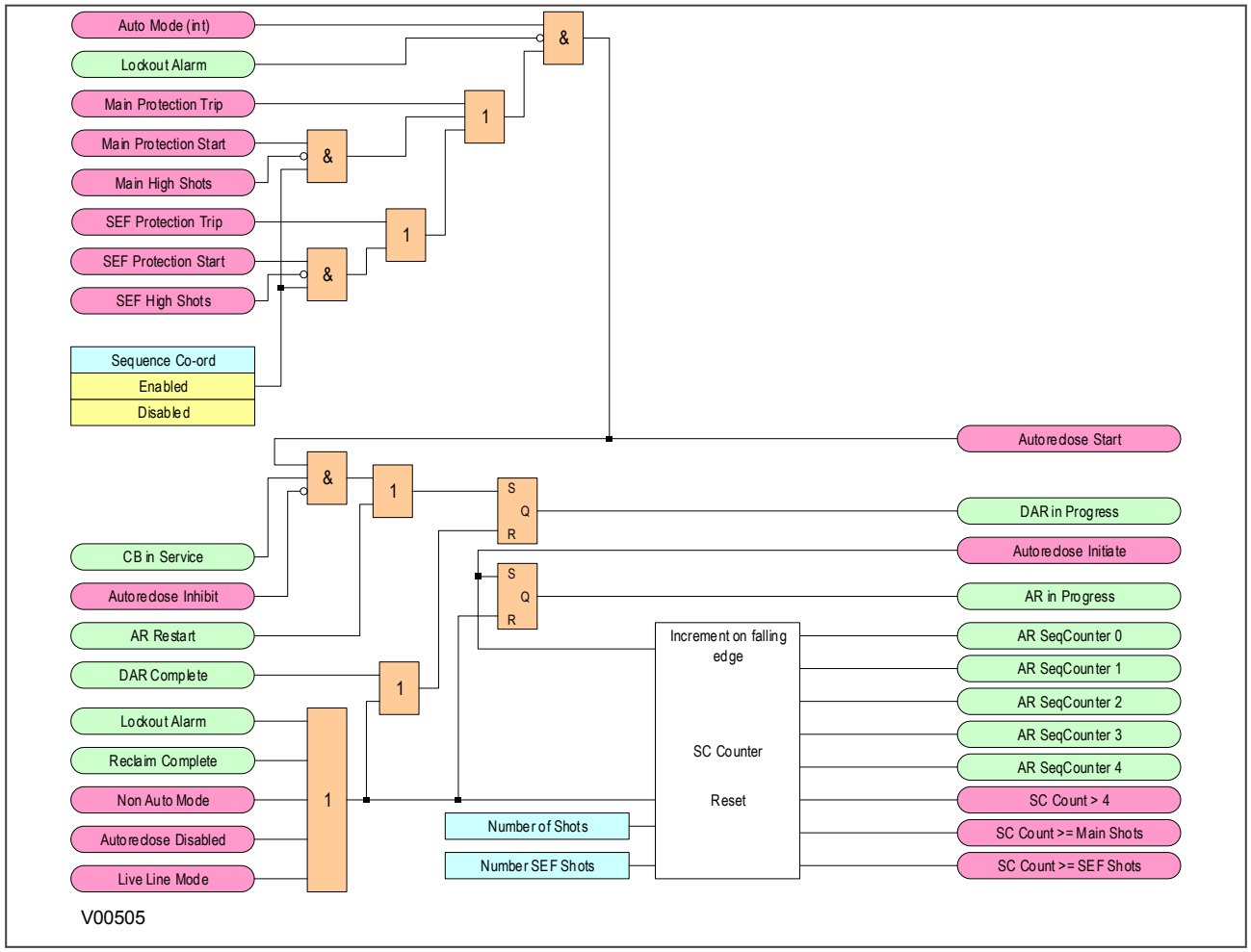


Figure 150: AR initiation logic

7.3 BLOCKING INSTANTANEOUS PROTECTION FOR SELECTED TRIPS

Instantaneous protection may be blocked or not blocked for each trip in an Autoreclose cycle. This is selected using the ***Trip (n) Main*** and ***Trip (n) SEF*** settings, where n is the number of the trip in the autoreclose cycle. These allow the instantaneous elements of phase, earth fault and SEF protection to be selectively blocked for a CB trip sequence. For example, if ***Trip 1 Main*** is set to `No Block` and ***Trip 2 Main*** is set to `Block Inst Prot`, the instantaneous elements of the phase and earth fault protection will be available for the first trip but blocked afterwards for the second trip during the Autoreclose cycle. The logic for this is shown below.

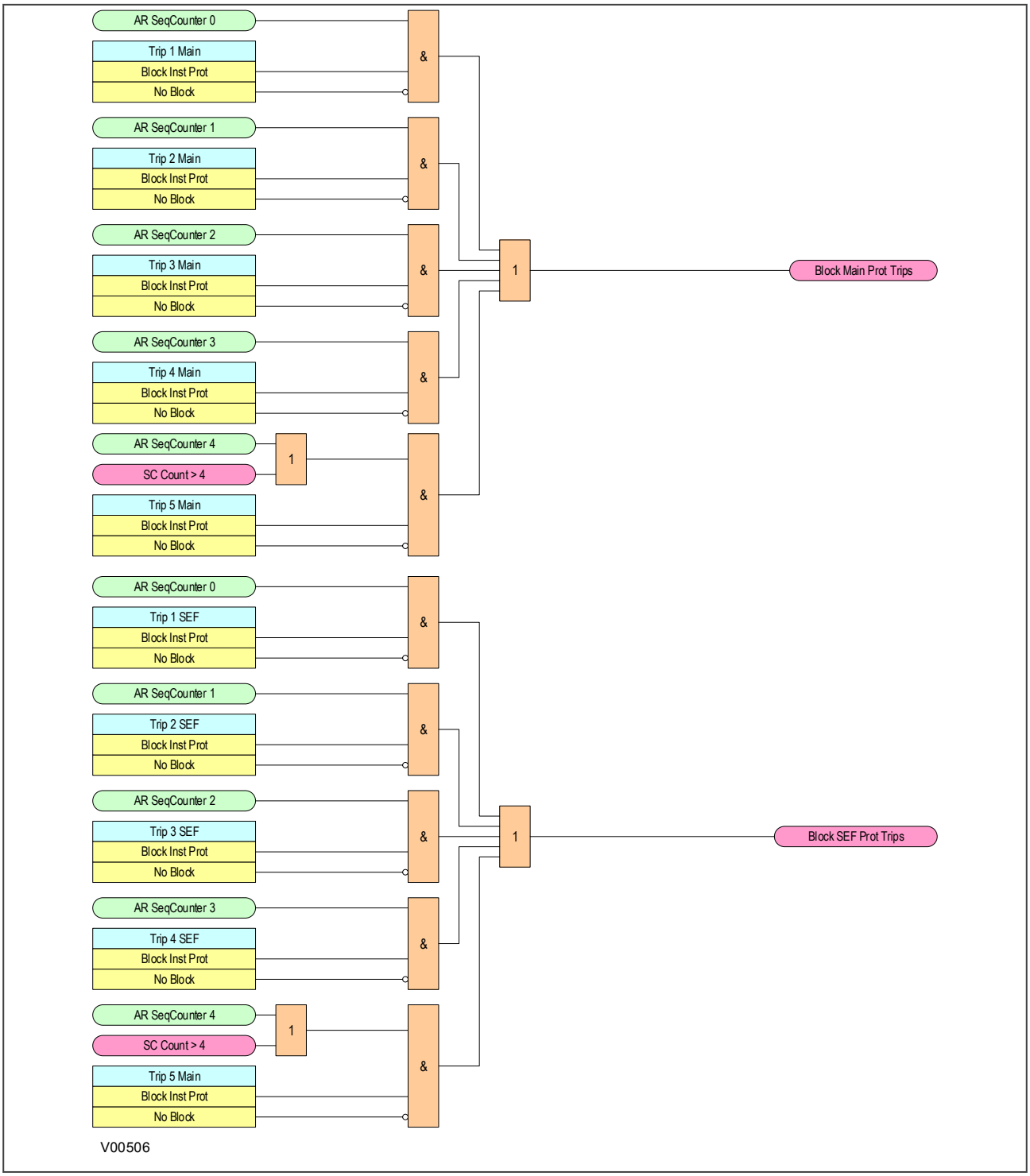


Figure 151: Blocking instantaneous protection for selected trips

7.4 BLOCKING INSTANTANEOUS PROTECTION FOR LOCKOUTS

Instantaneous protection can also be blocked for certain lockout conditions:

It is blocked when the CB maintenance lockout counter or excessive fault frequency lockout has reached its penultimate value.

For example, if the setting ***No. CB Ops Lock*** in the *CB MONITOR SETUP* column is set to 100 and the ***No. CB Ops Maint*** = '99', the instantaneous protection can be blocked to ensure that the last CB trip before lockout will be due

to discriminative protection operation. This is controlled using the ***EFF Maint Lock*** setting (Excessive Fault Frequency maintenance lockout). If this is set to `Block Inst Prot`, the instantaneous protection will be blocked for the last CB Trip before lockout occurs.

Instantaneous protection can also be blocked when the IED is locked out, using the ***AR Lockout*** setting. It can also be blocked after a manual close using the ***Manual Close*** setting. When the IED is in the Non-auto mode it can be blocked by using the ***AR Deselected*** setting. The logic for these features is shown below.

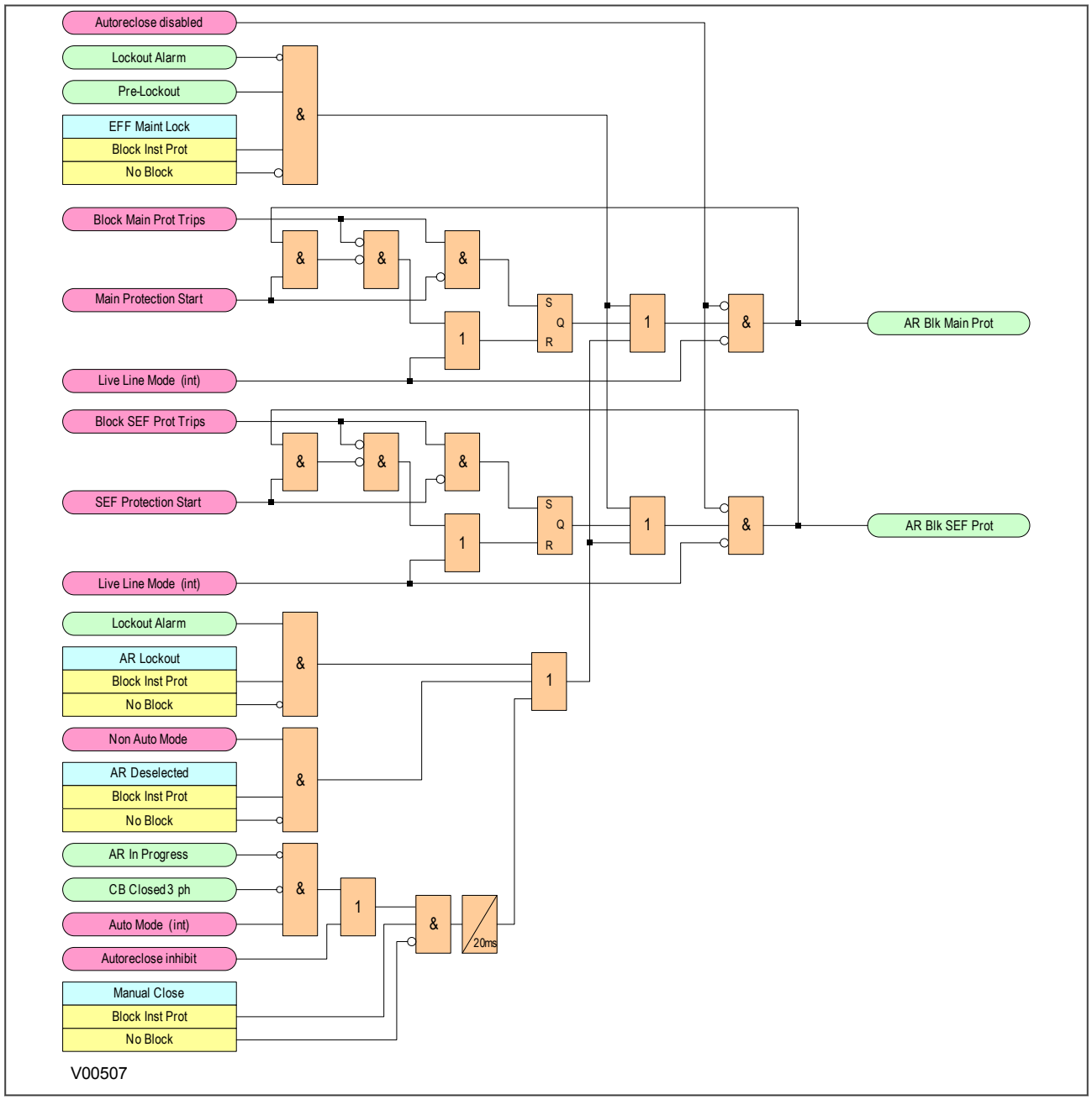


Figure 152: Blocking instantaneous protection for lockouts

7.5 DEAD TIME CONTROL

When the setting ***CS AR Immediate*** is enabled, immediate re-closure of the circuit breaker is allowed providing that both sides of the circuit breaker are live and in synchronism at any time after the dead time has started. This allows for quicker load restoration, as it is not necessary to wait for the full dead time to expire.

If ***CS AR Immediate*** is disabled, or neither Line nor Bus are live, the dead timer will continue to run, if the ***DeadTime Enabled*** signal is high. The ***DeadTime Enabled*** function could be mapped to an opto-input to indicate that the circuit breaker is healthy. Mapping the ***DeadTime Enabled*** function in PSL increases the flexibility by allowing it to be triggered by other conditions such as Live Line/Dead Bus. If ***DeadTime Enabled*** is not mapped in PSL, it defaults to high, so the dead time can run.

The dead time control logic is shown below.

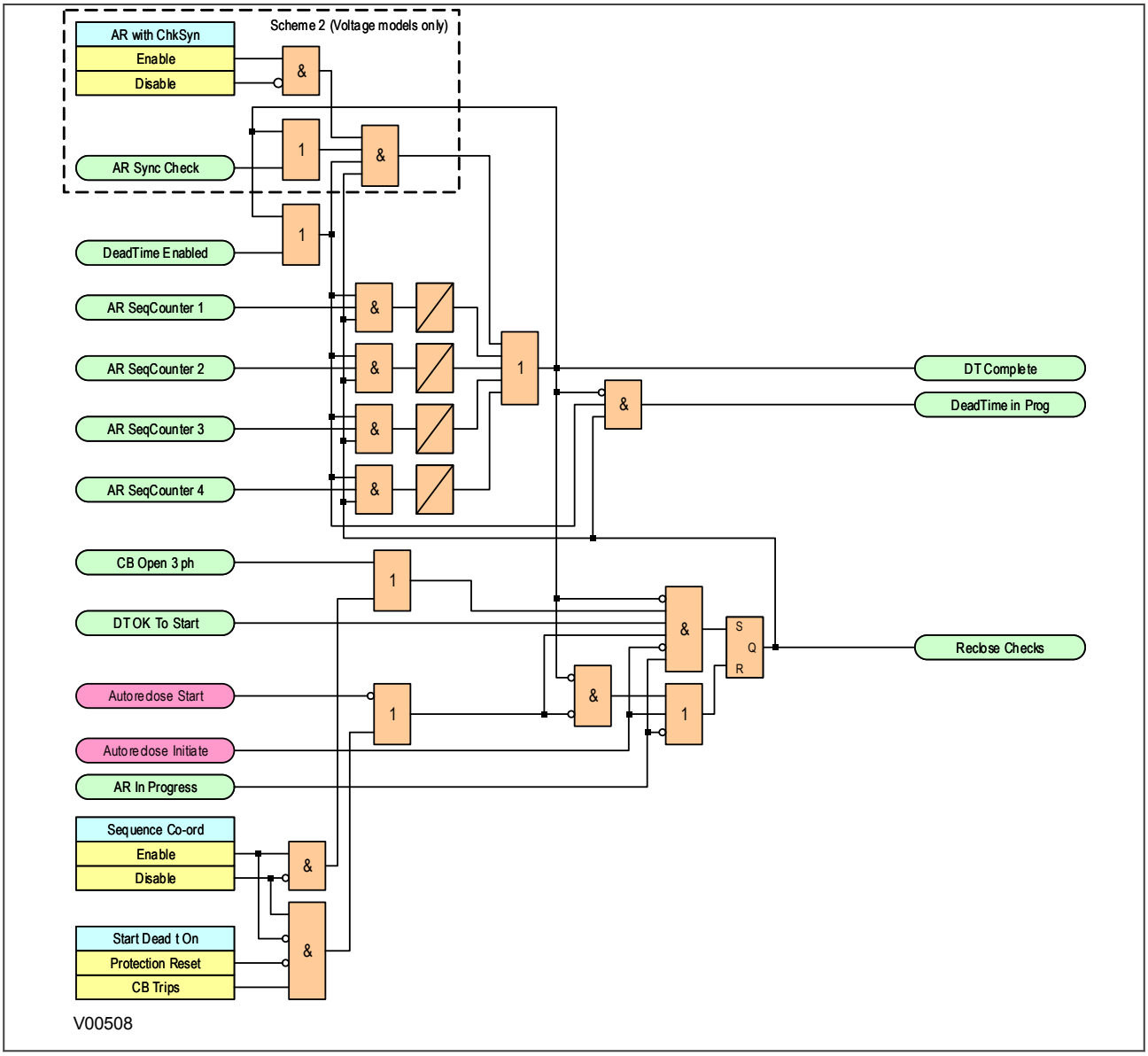


Figure 153: Dead Time Control logic

7.5.1 AR CB CLOSE CONTROL

Once the dead time is completed or a synchronism check is confirmed, the ***Auto Close*** signal is given, provided both the ***CB Healthy*** and the ***System Checks*** are satisfied. The ***Auto Close*** signal triggers a CB Close command via the CB Control functionality.

The AR CB Close Control Logic is as follows:

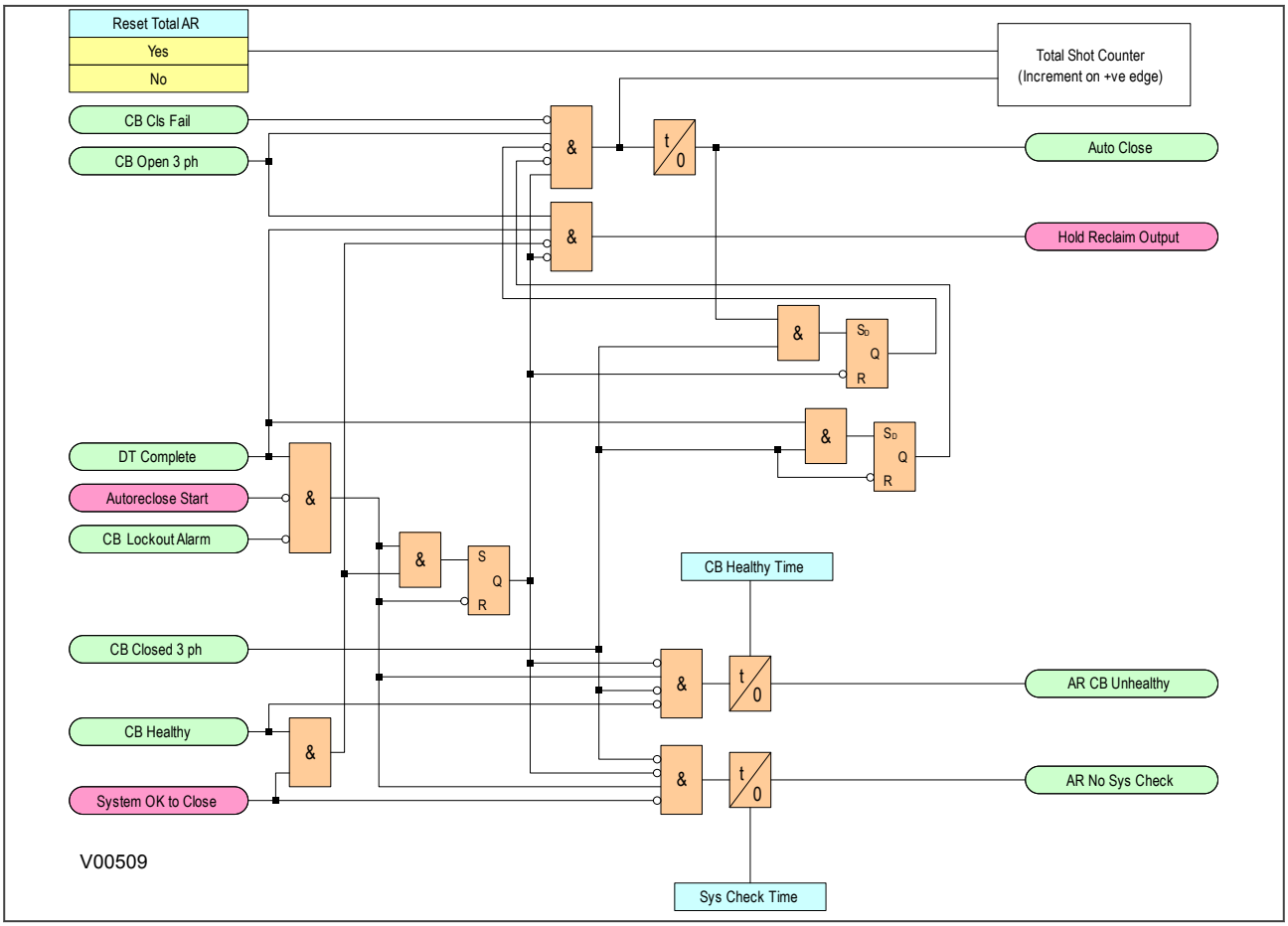


Figure 154: AR CB Close Control logic

7.6 AR SYSTEM CHECKS

The permission to initiate an Autoreclose depends on the following AR system check settings. These are found in the *AUTORECLOSE* column under the *AR SYSTEM CHECKS* sub-heading and are not to be confused with the main system check settings in the *SYSTEM CHECKS* column.

The *AR SYSTEM CHECKS* are as follows:

- ***Live/Dead Ccts***: When enabled this setting will give an ***AR Check OK*** signal when the ***LiveDead Ccts OK*** signal is high. This logic input DDB would normally be mapped in PSL to appropriate combinations of Line Live, Line Dead, Bus Live and Bus Dead DDB signals.
- ***No System Checks***: When enabled this setting completely disables system checks thus allowing Autoreclose initiation under any system conditions.
- ***SysChk on Shot 1***: Can be used to disable system checks on the first AR shot.
- ***AR with ChkSyn***: Only allows Autoreclose when the system satisfies the Check Sync Stage 1 (CS1) settings in the main *SYSTEM CHECKS* menu.
- ***AR with SysSyn***: Only allows Autoreclose when the system satisfies the Check Sync Stage 2 (CS2) settings in the main *SYSTEM CHECKS* menu.

The AR System Check logic is as follows:

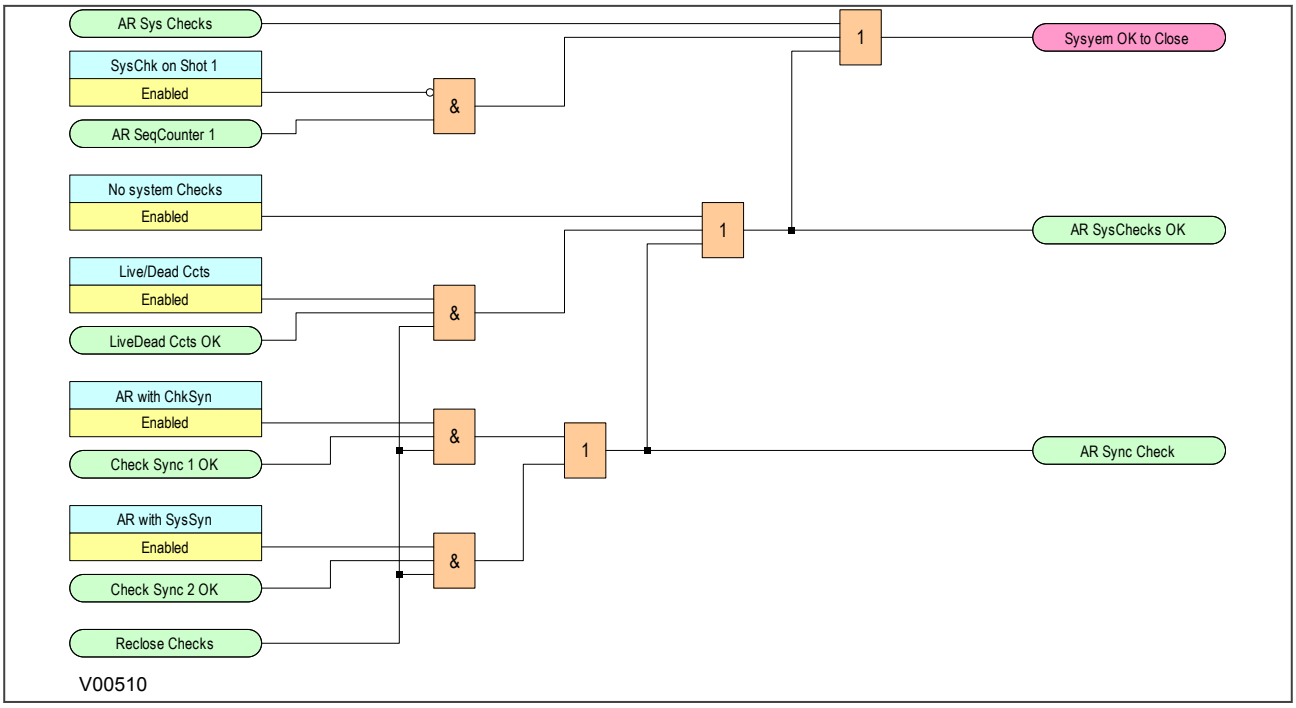


Figure 155: AR System Check logic

7.7 RECLAIM TIMER INITIATION

The ***tReclaim Extend*** setting allows you to control whether the timer is suspended from the protection start contacts or not. When a setting of `No Operation` is used, the reclaim timer operates from the instant the CB is closed and will continue until the timer expires. The ***Reclaim Time*** must therefore be set in excess of the time-delayed protection operating time, to ensure that the protection can operate before the Autoreclose function is reset.

For certain applications it is advantageous to set ***tReclaim Extend*** to `On Prot Start`. This facility allows the operation of the reclaim timer to be suspended after CB re-closure by a signal from the main protection start or SEF protection start signals. This feature ensures that the reclaim time cannot time out and reset the Autoreclose before the time delayed protection has operated.

Since the reclaim timer will be suspended, it is unnecessary to use a timer setting in excess of the protection operating time, therefore a short reclaim time can be used. Short reclaim time settings can help to prevent unnecessary lockout for a succession of transient faults in a short period, for example during a thunderstorm.

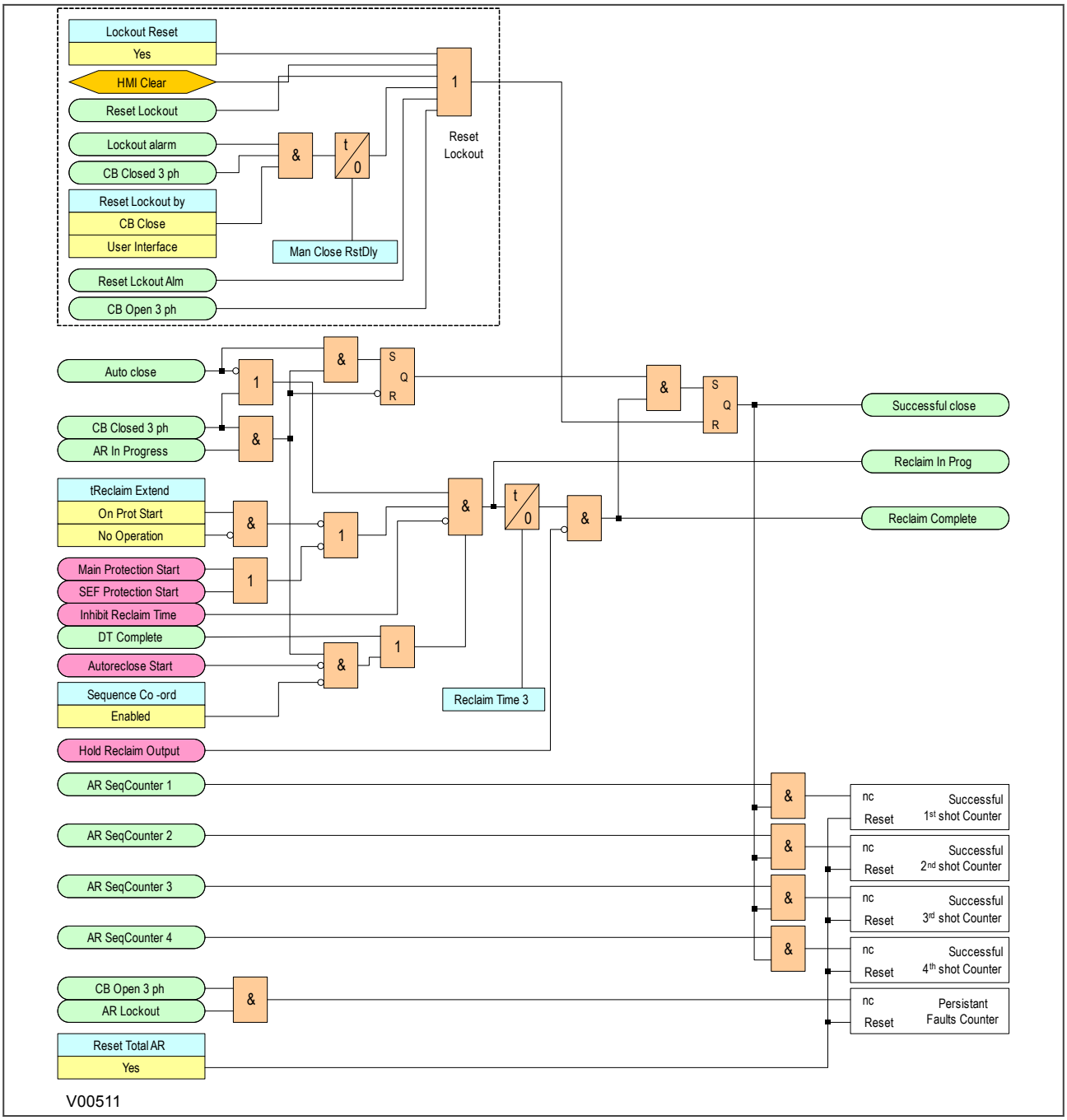


Figure 156: Reclaim Time logic

7.8 AUTORECLOSE INHIBIT

To ensure that autoreclosing is not initiated for a manual CB closure on to a pre-existing fault (switch on to fault), the ***AR on Man Close*** setting can be set to Inhibited. With this setting, Autoreclose initiation is inhibited for a period equal to setting ***AR Inhibit Time*** following a manual CB closure. The logic for AR Inhibit is as follows:

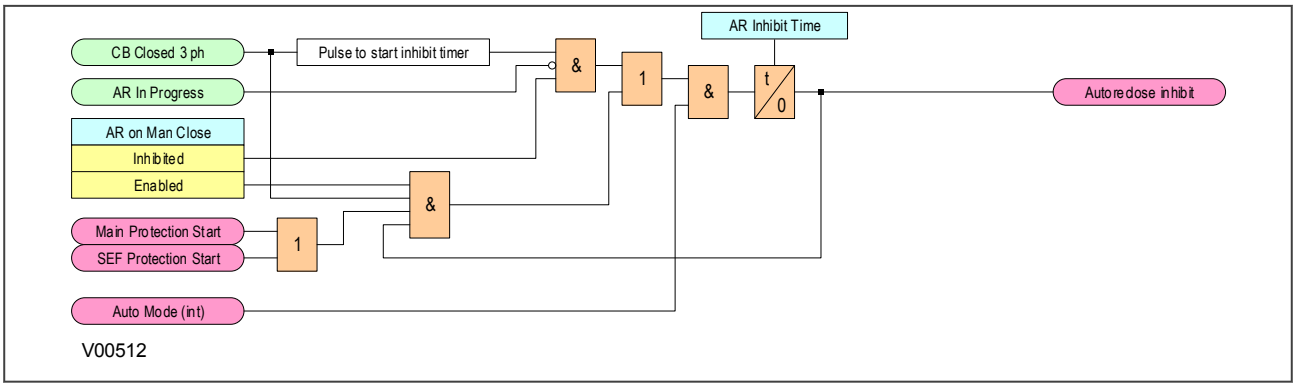


Figure 157: AR Initiation inhibit

If a protection operation occurs during the inhibit period, Autoreclose is not initiated. A further option is provided by setting ***Man Close on Flt***. If this is set to `Lockout`, Autoreclose is locked out (***AR Lockout***) for a fault during the inhibit period following manual CB closure. If ***Man Close on Flt*** is set to `No Lockout`, the CB trips without reclosure, but Autoreclose is not locked out.

You may need to block selected fast non-discriminating protection in order to obtain fully discriminative tripping during the AR initiation inhibit period following CB manual close. You can do this by setting ***Manual Close*** to `Block Inst Prot`. A `No Block` setting will enable all protection elements immediately on CB closure.

If setting ***AR on Man Close*** is set to `Enabled`, Autoreclose can be initiated immediately on CB closure, and settings ***AR Inhibit Time***, ***Man Close on Flt*** and ***Manual Close*** are irrelevant.

7.9 AUTORECLOSE LOCKOUT

If protection operates during the reclaim time following the final reclose attempt, the IED is driven to lockout and the Autoreclose function is disabled until the lockout condition is reset. This produces the alarm, ***AR Lockout***. The ***Block AR*** input blocks Autoreclose and causes a lockout if Autoreclose is in progress.

Autoreclose lockout can also be caused by the CB failing to close due to an unhealthy circuit breaker (CB springs not charged or low gas pressure) or if there is no synchronisation between the system voltages. These two conditions are indicated by the alarms ***CB Unhealthy*** and ***AR No Sys Check*** This is shown in the AR Lockout logic diagram as follows:

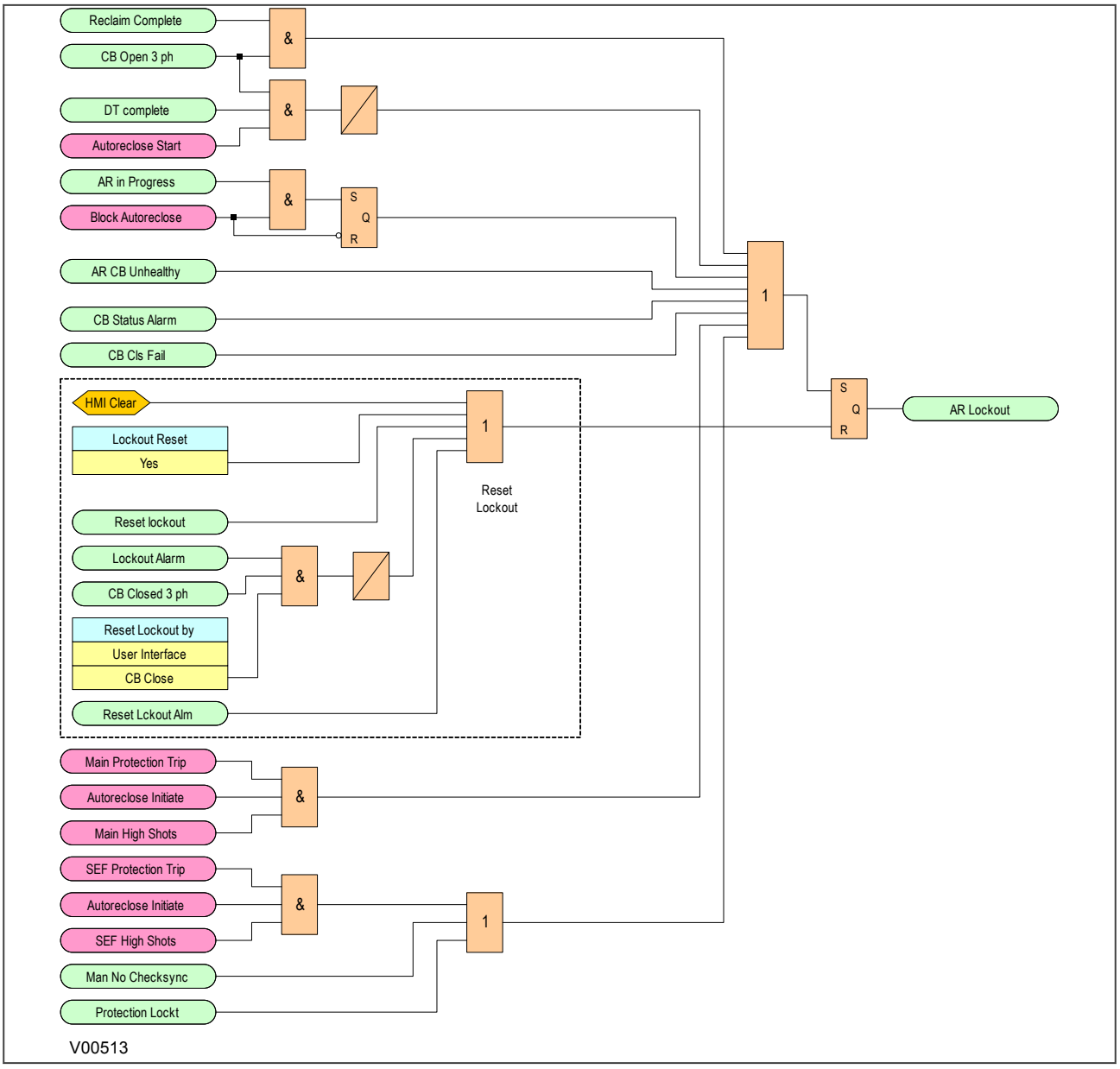


Figure 158: Overall Lockout logic

AR lockout may also be due to a protection operation when the IED is in the Live Line or Non-auto modes when the setting ***Trip AR Inactive*** is set to `Lockout`. Autoreclose lockout can also be caused by a protection operation after manual closing during the ***AR Inhibit Time*** when the ***Man Close on Flt*** setting is set to `Lockout`. This is shown as follows:

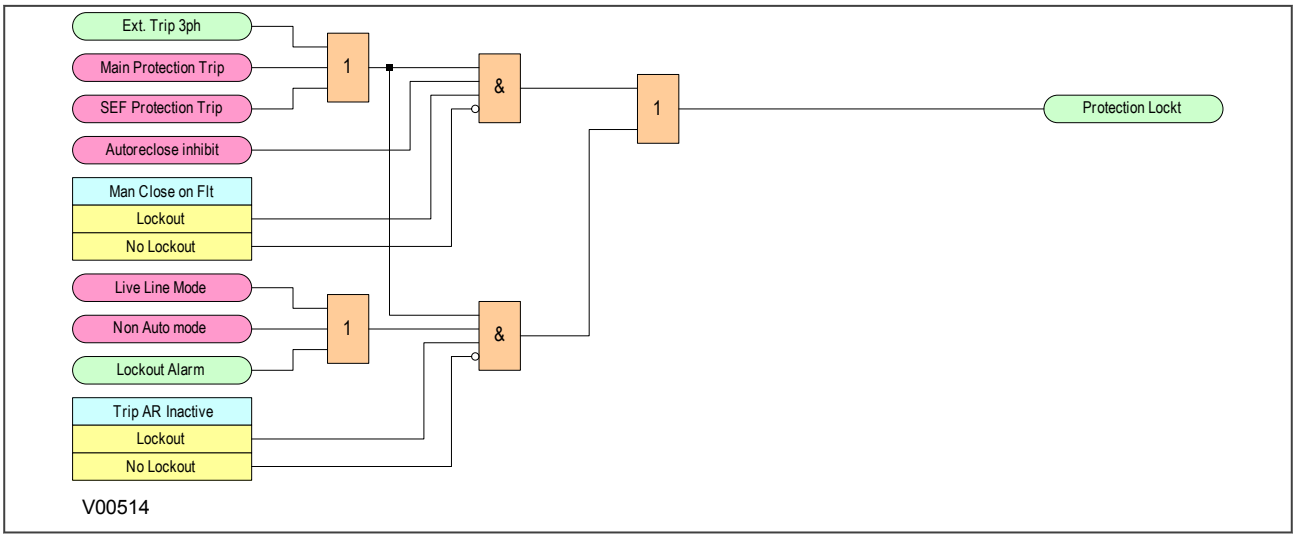


Figure 159: Lockout for protection trip when AR is not available

Note:
Lockout can also be caused by the CB condition monitoring functions in the CB MONITOR SETUP column.

The ***Reset Lockout*** input can be used to reset the Autoreclose function following lockout and reset any Autoreclose alarms, provided that the signals that initiated the lockout have been removed. Lockout can also be reset from the clear key or the command ***Lockout Reset*** from the *CB CONTROL* column.

There are two different ***Reset Lockout by*** settings. One in the *CB CONTROL* column and one in the *AUTORECLOSE* column.

The ***Reset Lockout by*** setting in the *CB CONTROL* column is used to enable or disable reset of lockout automatically from a manual close after the manual close time ***Man Close RstDly***.

The ***Reset Lockout by*** setting in the *AUTORECLOSE* column is used to enable/disable the resetting of lockout when the IED is in the Non-auto operating mode. The reset lockout methods are summarised in the following table:

Reset Lockout Method	When Available?
User Interface via the Clear key. Note: This will also reset all other protection flags	Always
User interface via *CB CONTROL* command Lockout Reset	Always
Opto-input Reset lockout	Always
Following a successful manual close if *CB CONTROL* setting Reset Lockout by is set to `CB Close`	Only when set
By selecting Non-Auto mode, provided *AUTORECLOSE* setting Reset Lockout by is set to `Select NonAuto`	Only when set

7.10 SEQUENCE CO-ORDINATION

The ***Sequence Co-ord*** setting in the *AUTORECLOSE* menu allows sequence co-ordination with other protection devices, such as downstream pole-mounted reclosers.

The main protection start or SEF protection start signals indicate when fault current is present, advance the sequence count by one and start the dead time, whether the CB is open or closed. When the dead time is complete and the protection start inputs are low, the reclaim timer is initiated.

You should program both the upstream and downstream Autoreclose IEDs with the same number of shots to lockout and number of instantaneous trips before instantaneous protection is blocked. This will ensure that for a persistent downstream fault, both Autoreclose IEDs will be on the same sequence count and will block

instantaneous protection at the same time. When sequence co-ordination is disabled, the circuit breaker has to be tripped to start the dead time, and the sequence count is advanced by one.

When using sequence co-ordination for some applications such as downstream pole-mounted reclosers, it may be desirable to re-enable instantaneous protection when the recloser has locked out. When the downstream recloser has locked out there is no need for discrimination. This allows you to have instantaneous, then IDMT, then instantaneous trips again during an Autoreclose cycle. Instantaneous protection may be blocked or not blocked for each trip in an Autoreclose cycle using the ***Trip (n) Main*** and ***Trip (n) SEF*** settings, where n is the number of the trip in the autoreclose cycle.

7.11 SYSTEM CHECKS FOR FIRST RECLOSE

The ***SysChk on Shot 1*** setting in the *SYSTEM CHECKS* sub menu of the *AUTORECLOSE* column is used to enable or disable system checks for the first reclose attempt in an Autoreclose cycle. This may be preferred when high speed Autoreclose is applied, to avoid the extra time for a synchronism check. Subsequent reclose attempts in a multi-shot cycle will, however, still require a synchronism check.

8 SETTING GUIDELINES

8.1 NUMBER OF SHOTS

There are no clear cut rules for defining the number of shots for a particular application. Generally medium voltage systems use only two or three shot Autoreclose schemes. However, in certain countries, for specific applications, a four-shot scheme is used. A four-shot scheme has the advantage that the final dead time can be set sufficiently long to allow any thunderstorms to pass before reclosing for the final time. This arrangement prevents unnecessary lockout for consecutive transient faults.

Typically, the first trip, and sometimes the second, will result from instantaneous protection. Since most faults are transient, the subsequent trips will be time delayed, all with increasing dead times to clear semi-permanent faults.

An important consideration is the ability of the circuit breaker to perform several trip-close operations in quick succession and the affect of these operations on the circuit maintenance period.

On EHV transmission circuits with high fault levels, only one re-closure is normally applied, because of the damage that could be caused by multiple re-closures.

8.2 DEAD TIMER SETTING

The choice of dead time is dependent on the system. The main factors that can influence the choice of dead time are:

- Stability and synchronism requirements
- Operational convenience
- Load
- The type of circuit breaker
- Fault deionising time
- The protection reset time

8.2.1 STABILITY AND SYNCHRONISM REQUIREMENTS

It may be that the power transfer level on a specific feeder is such that the systems at either end of the feeder could quickly fall out of synchronism if the feeder is opened. If this is the case, it is usually necessary to reclose the feeder as quickly as possible to prevent loss of synchronism. This is called high speed autoreclosing (HSAR). In this situation, the dead time setting should be adjusted to the minimum time necessary. This time setting should comply with the minimum dead time limitations imposed by the circuit breaker and associated protection, which should be enough to allow complete deionisation of the fault path and restoration of the full voltage withstand level. Typical HSAR dead time values are between 0.3 and 0.5 seconds.

On a closely interconnected transmission system, where alternative power transfer paths usually hold the overall system in synchronism even when a specific feeder opens, or on a radial supply system where there are no stability implications, it is often preferred to leave a feeder open for a few seconds after fault clearance. This allows the system to stabilise, and reduces the shock to the system on re-closure. This is called slow or delayed auto-reclosing (DAR). The dead time setting for DAR is usually selected for operational convenience.

8.2.2 OPERATIONAL CONVENIENCE

When HSAR is not required, the dead time chosen for the first re-closure following a fault trip is not critical. It should be long enough to allow any resulting transients resulting to decay, but not so long as to cause major inconvenience to consumers who are affected by the loss of the feeder. The setting chosen often depends on service experience with the specific feeder.

Typical first shot dead time settings on 11 kV distribution systems are 5 to 10 seconds. In situations where two parallel circuits from one substation are carried on the same towers, it is often arranged for the dead times on the

two circuits to be staggered, e.g. one at 5 seconds and the other at 10 seconds, so that the two circuit breakers do not reclose simultaneously following a fault affecting both circuits.

For multi-shot Autoreclose cycles, the second shot and subsequent shot dead times are usually longer than the first shot, to allow time for semi-permanent faults to burn clear, and for the CB to recharge. Typical second and third shot dead time settings are 30 seconds and 60 seconds respectively.

8.2.3 LOAD REQUIREMENTS

Some types of electrical load might have specific requirements for minimum and/or maximum dead time, to prevent damage and minimise disruption. For example, synchronous motors are only capable of tolerating extremely short supply interruptions without losing synchronism. In practise it is desirable to disconnect the motor from the supply in the event of a fault; the dead time would normally be sufficient to allow a controlled shutdown. Induction motors, on the other hand, can withstand supply interruptions up to typically 0.5 seconds and re-accelerate successfully.

8.2.4 CIRCUIT BREAKER

For HSAR, the minimum dead time of the power system will depend on the minimum time delays imposed by the circuit breaker during a tripping and reclose operation.

After tripping, time must be allowed for the mechanism to reset before applying a closing pulse, otherwise the circuit breaker might fail to close correctly. This resetting time will vary depending on the circuit breaker, but is typically 0.1 seconds.

Once the mechanism has reset, a CB Close signal can be applied. The time interval between energising the closing mechanism and making the contacts is called the closing time. A solenoid closing mechanism may take up to 0.3 seconds. A spring-operated breaker, on the other hand, can close in less than 0.1 seconds.

Where HSAR is required, for the majority of medium voltage applications, the circuit breaker mechanism reset time itself dictates the minimum dead time. This would be the mechanism reset time plus the CB closing time. A solenoid mechanism is not suitable for high speed Autoreclose as the closing time is generally too long.

For most circuit breakers, after one reclosure, it is necessary to recharge the closing mechanism energy source before a further reclosure can take place. Therefore the dead time for second and subsequent shots in a multi-shot sequence must be set longer than the spring or gas pressure recharge time.

8.2.5 FAULT DE-IONISATION TIME

For HSAR, the fault deionising time may be the most important factor when considering the dead time. This is the time required for ionised air to disperse around the fault position so that the insulation level of the air is restored. You cannot accurately predict this, but you can obtain an approximation from the following formula:

Deionising time = (10.5 + ((system voltage in kV)/34.5))/frequency

Examples:

At 66 kV 50 Hz, the deionising time is approximately 0.25 s

At 132 kV 60 Hz, the deionising time is approximately 0.29 s

8.2.6 PROTECTION RESET TIME

It is essential that any time-graded protection fully resets during the dead time, so that correct time discrimination will be maintained after reclosing on to a fault. For HSAR, instantaneous reset of protection is required. However at distribution level, where the protection is predominantly made up of overcurrent and earth fault devices, the protection reset time may not be instantaneous. In the event that the circuit breaker recloses on to a fault and the protection has not fully reset, discrimination may be lost with the downstream protection. To avoid this condition the dead time must be set in excess of the slowest reset time of either the local device or any downstream protection.

Typical 11/33 kV dead time settings are as follows:

1st dead time = 5 - 10 seconds

2nd dead time = 30 seconds

3rd dead time = 60 - 180 seconds

4th dead time = 1 - 30 minutes

8.3 RECLAIM TIMER SETTING

A number of factors influence the choice of the reclaim timer:

- Supply continuity: Large reclaim times can result in unnecessary lockout for transient faults.
- Fault incidence/Past experience: Small reclaim times may be required where there is a high incidence of lightning strikes to prevent unnecessary lockout for transient faults.
- Spring charging time: For HSAR the reclaim time may be set longer than the spring charging time to ensure there is sufficient energy in the circuit breaker to perform a trip-close-trip cycle. For delayed Autoreclose there is no need as the dead time can be extended by an extra CB healthy check window time if there is insufficient energy in the CB. If there is insufficient energy after the check window time the IED will lockout.
- Switchgear maintenance: Excessive operation resulting from short reclaim times can mean shorter maintenance periods. A minimum reclaim time of more than 5 seconds may be needed to allow the circuit breaker time to recover after a trip and close before it can perform another trip-close-trip cycle. This time will depend on the circuit breaker's duty rating.

The reclaim time must be long enough to allow any time-delayed protection initiating Autoreclose to operate. Failure to do so would result in premature resetting of the Autoreclose scheme and re-enabling of instantaneous protection. If this condition arose, a permanent fault would effectively look like a number of transient faults, resulting in continuous autoreclosing, unless additional measures are taken such as excessive fault frequency lockout protection.

Sensitive earth fault protection is applied to detect high resistance earth faults and usually has a long time delay, typically 10 - 15 seconds. This longer time may have to be taken into consideration, if autoreclosing from SEF protection. High resistance earth faults are rarely transient and may be a danger to the public. It is therefore common practise to block Autoreclose by operation of sensitive earth fault protection and lockout the circuit breaker.

A typical 11/33 kV reclaim time is 5 - 10 seconds. This prevents unnecessary lockout during thunderstorms. However, reclaim times of up to 60 - 180 seconds may be used elsewhere in the world.

CHAPTER 14

MONITORING AND CONTROL

1 CHAPTER OVERVIEW

As well as providing a range of protection functions, the product includes comprehensive monitoring and control functionality.

This chapter contains the following sections:

2 EVENT RECORDS

General Electric devices record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

The event records are detailed in the *VIEW RECORDS* column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

If viewing the event with the settings application software, simply open the extracted event file. All the events are displayed chronologically. Each event is summarised with a time stamp (obtained from the ***Time & Date*** cell) and a short description relating to the event (obtained from the ***Event Text*** cell. You can expand the details of the event by clicking on the **+** icon to the left of the time stamp.

The following table shows the correlation between the fields in the setting application software's event viewer and the cells in the menu database.

Field in Event Viewer	Equivalent cell in menu DB	Cell reference	User settable?
Left hand column header	VIEW RECORDS → Time & Date	01 03	No
Right hand column header	VIEW RECORDS → Event Text	01 04	No
Description	SYSTEM DATA → Description	00 04	Yes
Plant reference	SYSTEM DATA → Plant Reference	00 05	Yes
Model number	SYSTEM DATA → Model Number	00 06	No
Address	Displays the Courier address relating to the event	N/A	No
Event type	VIEW RECORDS → Menu Cell Ref	01 02	No
Event Value	VIEW RECORDS → Event Value	01 05	No
Evt Unique Id	VIEW RECORDS → Evt Unique ID	01 FE	No

The device is capable of storing up to 2048 event records.

In addition to the event log, there are two additional logs which contain duplicates of the last 10 maintenance records and the last 10 fault records. The purpose of this is to provide convenient access to the most recent fault and maintenance events.

2.1 EVENT TYPES

There are several different types of event:

- Opto-input events (Change of state of opto-input)
- Contact events (Change of state of output relay contact)
- Alarm events
- Fault record events
- Standard events
- Security events

Standard events are further sub-categorised internally to include different pieces of information. These are:

- Protection events (starts and trips)
- Maintenance record events
- Platform events

Note:
The first event in the list (event 0) is the most recent event to have occurred.

2.1.1 OPTO-INPUT EVENTS

If one or more of the opto-inputs has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all opto-inputs. You can tell which opto-input has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Logic Inputs #` where # is the batch number of the opto-inputs. This is '1', for the first batch of opto-inputs and '2' for the second batch of opto-inputs (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the opto-inputs, where the Least Significant Bit (LSB), on the right corresponds to the first opto-input `Input L1`.

The same information is also shown in the ***Opto I/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

2.1.2 CONTACT EVENTS

If one or more of the output relays (also known as output contacts) has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all output relays. You can tell which output relay has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Output Contacts #` where # is the batch number of the output relay contacts. This is '1', for the first batch of output contacts and '2' for the second batch of output contacts (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the output relays, where the LSB (on the right) corresponds to the first output contact `Output R1`.

The same information is also shown in the ***Relay O/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

2.1.3 ALARM EVENTS

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event.

The description of this event type, as shown in the ***Event Text*** cell is cell dependent on the type of alarm and will be one of those shown in the following tables, followed by `OFF` or `ON`.

The event value shown in the ***Event Value*** cell for this type of event is a 32 bit binary string. There are one or more banks 32 bit registers, depending on the device model. These contain all the alarm types and their logic states (`ON` or `OFF`).

The same information is also shown in the ***Alarm Status (n)*** cells in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

Alarm Status 1

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 0	0x0000, 0x0001	Thermal Lockout
Bit 1	0x0000, 0x0002	HIF Alarm
Bit 2	0x0000, 0x0004	SG-opto Invalid ON/OFF
Bit 3	0x0000, 0x0008	Prot'n Disabled ON/OFF
Bit 4	0x0000, 0x0010	F out of Range ON/OFF
Bit 5	0x0000, 0x0020	VT Fail Alarm ON/OFF
Bit 6	0x0000, 0x0040	CT Fail Alarm ON/OFF
Bit 7	0x0000, 0x0080	CB Fail Alarm ON/OFF
Bit 8	0x0000, 0x0100	I^ Maint Alarm ON/OFF
Bit 9	0x0000, 0x0200	I^ Lockout Alarm ON/OFF
Bit 10	0x0000, 0x0400	CB Ops Maint ON/OFF
Bit 11	0x0000, 0x0800	CB Ops Lockout ON/OFF
Bit 12	0x0000, 0x1000	CB Op Time Maint ON/OFF
Bit 13	0x0000, 0x2000	CB Op Time Lock ON/OFF
Bit 14	0x0000, 0x4000	Fault Freq Lock ON/OFF
Bit15	0x0000, 0x8000	CB Status Alarm ON/OFF
Bit 16	0x0001, 0x0000	Man CB Trip Fail ON/OFF
Bit17	0x0002, 0x0000	Man CB Cls Fail ON/OFF
Bit 18	0x0004, 0x0000	Man CB Unhealthy ON/OFF
Bit 19	0x0008, 0x0000	Man No Checksync ON/OFF
Bit 20	0x0010, 0x0000	A/R Lockout ON/OFF
Bit 21	0x0020, 0x0000	A/R CB Unhealthy ON/OFF
Bit 22	0x0040, 0x0000	A/R No Checksync ON/OFF
Bit 23	0x0080, 0x0000	System Split ON/OFF
Bit 24	0x0100, 0x0000	UV Block ON/OFF
Bit 25	0x0200, 0x0000	User Alarm 1 ON/OFF
Bit 26	0x0400, 0x0000	User Alarm 2 ON/OFF
Bit 27	0x0800, 0x0000	User Alarm 3 ON/OFF
Bit 28	0x1000, 0x0000	User Alarm 4 ON/OFF
Bit 29	0x2000, 0x0000	User Alarm 5 ON/OFF
Bit 30	0x4000, 0x0000	User Alarm 6 ON/OFF
Bit 31	0x8000, 0x0000	User Alarm 7 ON/OFF

Alarm Status 2

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 1	0x0000, 0x0001	Time Betwe Start (motor protection models only)
Bit 2	0x0000, 0x0002	Hot Start Nb. (motor protection models only)
Bit 3	0x0000, 0x0004	Cold Start Nb. (motor protection models only)

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 4	0x0000, 0x0008	Antibkspin Alarm (motor protection models only)
Bit 5	0x0000, 0x0010	User Alarm 8
Bit 6	0x0000, 0x0020	User Alarm 9
Bit 7	0x0000, 0x0040	User Alarm 10
Bit 8	0x0000, 0x0080	User Alarm 11
Bit 9	0x0000, 0x0100	User Alarm 12
Bit 10	0x0000, 0x0200	User Alarm 13
Bit 11	0x0000, 0x0400	User Alarm 14
Bit 12	0x0000, 0x0800	User Alarm 15
Bit 13	0x0000, 0x1000	User Alarm 16
Bit 14	0x0000, 0x2000	User Alarm 17
Bit 15	0x0000, 0x4000	User Alarm 18
Bit 16	0x0000, 0x8000	User Alarm 19
Bit 17	0x0001, 0x0000	User Alarm 20
Bit 18	0x0002, 0x0000	User Alarm 21
Bit 19	0x0004, 0x0000	User Alarm 22
Bit 20	0x0008, 0x0000	User Alarm 23
Bit 21	0x0010, 0x0000	User Alarm 24
Bit 22	0x0020, 0x0000	User Alarm 25
Bit 23	0x0040, 0x0000	User Alarm 26
Bit 24	0x0080, 0x0000	User Alarm 27
Bit 25	0x0100, 0x0000	User Alarm 28
Bit 26	0x0200, 0x0000	User Alarm 29
Bit 27	0x0400, 0x0000	User Alarm 30
Bit 28	0x0800, 0x0000	User Alarm 31
Bit 29	0x1000, 0x0000	User Alarm 32
Bit 30	0x2000, 0x0000	MR User Alarm 33
Bit 31	0x4000, 0x0000	MR User Alarm 34
Bit 32	0x8000, 0x0000	MR User Alarm 35

Alarm Status 3

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 1	0x00000001	DC Supply Fail
Bit 2	0x00000002	Unused
Bit 3	0x00000004	Unused
Bit 4	0x00000008	GOOSE IED Absent
Bit 5	0x00000010	NIC Not Fitted
Bit 6	0x00000020	NIC No Response
Bit 7	0x00000040	NIC Fatal Error

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 8	0x00000080	Unused
Bit 9	0x00000100	Bad TCP/IP Cfg.
Bit 10	0x00000200	Unused
Bit 11	0x00000400	NIC Link Fail
Bit 12	0x00000800	NIC SW Mis-Match
Bit 13	0x00001000	IP Addr Conflict
Bit 14	0x00002000	Unused
Bit 15	0x00004000	Unused
Bit 16	0x00008000	Unused
Bit 17	0x00010000	Unused
Bit 18	0x00020000	Unused
Bit 19	0x00040000	Bad DNP Settings
Bit 20	0x00080000	Unused
Bit 21	0x00100000	Unused
Bit 22	0x00200000	Unused
Bit 23	0x00400000	Unused
Bit 24	0x00800000	Unused
Bit 25	0x01000000	Unused
Bit 26	0x02000000	Unused
Bit 27	0x04000000	Unused
Bit 28	0x08000000	Unused
Bit 29	0x10000000	Unused
Bit 30	0x20000000	Unused
Bit 31	0x40000000	Unused
Bit 32	0x80000000	Unused

Alarm Status 4

Alarm Status 4 setting values are reserved.

User Alarms

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 1	0x0000,0x0001	User Alarm 1 (0=Self-reset, 1=Manual reset)
Bit 2	0x0000,0x0002	User Alarm 2 (0=Self-reset, 1=Manual reset)
Bit 3	0x0000,0x0004	User Alarm 3 (0=Self-reset, 1=Manual reset)
Bit 4	0x0000,0x0008	User Alarm 4 (0=Self-reset, 1=Manual reset)
Bit 5	0x0000,0x0010	User Alarm 5 (0=Self-reset, 1=Manual reset)
Bit 6	0x0000,0x0020	User Alarm 6 (0=Self-reset, 1=Manual reset)
Bit 7	0x0000,0x0040	User Alarm 7 (0=Self-reset, 1=Manual reset)

Bit No.	Bit Mask 2nd register, 1st register	Alarm Description
Bit 8	0x0000,0x0080	User Alarm 8 (0=Self-reset, 1=Manual reset)
Bit 9	0x0000,0x0100	User Alarm 9 (0=Self-reset, 1=Manual reset)
Bit 10	0x0000,0x0200	User Alarm 10 (0=Self-reset, 1=Manual reset)
Bit 11	0x0000,0x0400	User Alarm 11 (0=Self-reset, 1=Manual reset)
Bit 12	0x0000,0x0800	User Alarm 12 (0=Self-reset, 1=Manual reset)
Bit 13	0x0000,0x1000	User Alarm 13 (0=Self-reset, 1=Manual reset)
Bit 14	0x0000,0x2000	User Alarm 14 (0=Self-reset, 1=Manual reset)
Bit 15	0x0000,0x4000	User Alarm 15 (0=Self-reset, 1=Manual reset)
Bit 16	0x0000,0x8000	User Alarm 16 (0=Self-reset, 1=Manual reset)
Bit 17	0x0001,0x0000	User Alarm 17 (0=Self-reset, 1=Manual reset)
Bit 18	0x0002,0x0000	User Alarm 18 (0=Self-reset, 1=Manual reset)
Bit 19	0x0004,0x0000	User Alarm 19 (0=Self-reset, 1=Manual reset)
Bit 20	0x0008,0x0000	User Alarm 20 (0=Self-reset, 1=Manual reset)
Bit 21	0x0010,0x0000	User Alarm 21 (0=Self-reset, 1=Manual reset)
Bit 22	0x0020,0x0000	User Alarm 22 (0=Self-reset, 1=Manual reset)
Bit 23	0x0040,0x0000	User Alarm 23 (0=Self-reset, 1=Manual reset)
Bit 24	0x0080,0x0000	User Alarm 24 (0=Self-reset, 1=Manual reset)
Bit 25	0x0100,0x0000	User Alarm 25 (0=Self-reset, 1=Manual reset)
Bit 26	0x0200,0x0000	User Alarm 26 (0=Self-reset, 1=Manual reset)
Bit 27	0x0400,0x0000	User Alarm 27 (0=Self-reset, 1=Manual reset)
Bit 28	0x0800,0x0000	User Alarm 28 (0=Self-reset, 1=Manual reset)
Bit 29	0x1000,0x0000	User Alarm 29 (0=Self-reset, 1=Manual reset)
Bit 30	0x2000,0x0000	User Alarm 30 (0=Self-reset, 1=Manual reset)
Bit 31	0x4000,0x0000	User Alarm 31 (0=Self-reset, 1=Manual reset)
Bit 32	0x8000,0x0000	User Alarm 32 (0=Self-reset, 1=Manual reset)

Note:
User Alarms 1 to 32 are fully settable in the USER ALARMS column:

Note:
Alarm texts can be changed via menu

Note:
Alarm types can changed via menu (Self-reset or Manual reset

2.1.4 FAULT RECORD EVENTS

An event record is created for every fault the IED detects. This is also known as a fault record.

The event type description shown in the ***Event Text*** cell for this type of event is always `Fault Recorded`.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the ***Select Fault*** setting, where fault number 0 is the latest fault.

A fault record is triggered by the ***Fault REC TRIG*** signal DDB, which is assigned in the PSL. The fault recorder records the values of all parameters associated with the fault for the duration of the fault. These parameters are stored in separate Courier cells, which become visible depending on the type of fault.

The fault recorder stops recording only when:

The Start signal is reset AND the undercurrent is ON OR the Trip signal is reset, as shown below:

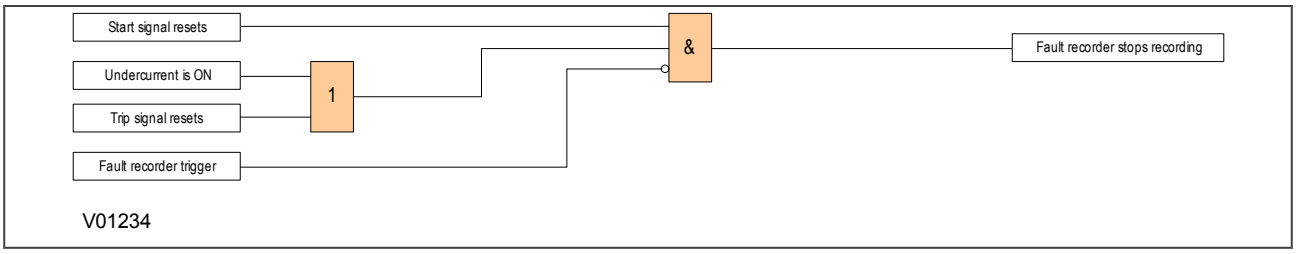


Figure 160: Fault recorder stop conditions

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The timestamp assigned to the fault record event corresponds to the time when the fault recorder stops.

Note:
We recommend that you do not set the triggering contact to latching. This is because if you use a latching contact, the fault record would not be generated until the contact has been fully reset.

2.1.5 SECURITY EVENTS

An event record is generated each time a setting that requires an access level is executed.

The event type description shown in the ***Event Text*** cell displays the type of change.

2.1.6 MAINTENANCE EVENTS

Internal failures detected by the self-test procedures are logged as maintenance records. Maintenance records are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is always `Maint Recorded`.

The ***Event Value*** cell also provides a unique binary code.

The IED contains a separate register containing the latest maintenance records. This provides a convenient way of viewing the latest maintenance records and saves searching through the event log. You access these fault records using the ***Select Maint*** setting.

The maintenance record has a number of extra menu cells relating to the maintenance event. These parameters are ***Maint Text***, ***Maint Type*** and ***Maint Data***. They contain details about the maintenance event selected with the ***Select Maint*** cell.

2.1.7 PROTECTION EVENTS

The IED logs protection starts and trips as individual events. Protection events are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is dependent on the protection event that occurred. Each time a protection event occurs, a DDB signal changes state. It is the name of this DDB signal followed by 'ON' or 'OFF' that appears in the ***Event Text*** cell.

The ***Event Value*** cell for this type of event is a 32 bit binary string representing the state of the relevant DDB signals. These binary strings can also be viewed in the *COMMISSION TESTS* column in the relevant DDB batch cells.

Not all DDB signals can generate an event. Those that can are listed in the *RECORD CONTROL* column. In this column, you can set which DDBs generate events.

2.1.8 PLATFORM EVENTS

Platform events are special types of standard events.

The event type description shown in the ***Event Text*** cell displays the type of change.

3 DISTURBANCE RECORDER

The disturbance recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals. The digital signals may be inputs, outputs, or internal DDB signals. The disturbance records can be extracted using the disturbance record viewer in the settings application software. The disturbance record file can also be stored in the COMTRADE format. This allows the use of other packages to view the recorded data.

The integral disturbance recorder has an area of memory specifically set aside for storing disturbance records. The number of records that can be stored is dependent on the recording duration. The minimum duration is 0.1 s and the maximum duration is 10.5 s.

When the available memory is exhausted, the oldest records are overwritten by the newest ones.

Each disturbance record consists of a number of analogue data channels and digital data channels. The relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities.

The fault recording times are set by a combination of the ***Duration*** and ***Trigger Position*** cells. The ***Duration*** cell sets the overall recording time and the ***Trigger Position*** cell sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

With the ***Trigger Mode*** set to *Single*, if further triggers occurs whilst a recording is taking place, the recorder will ignore the trigger. However, with the ***Trigger Mode*** set to *Extended*, the post trigger timer will be reset to zero, extending the recording time.

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

You may choose any of the digital channels to trigger the disturbance recorder on either a low to high or a high to low transition, via the ***Input Trigger*** cell. The default settings are such that any dedicated trip output contacts will trigger the recorder.

It is not possible to view the disturbance records locally via the front panel LCD. You must extract these using suitable setting application software such as MiCOM S1 Agile.

4 MEASUREMENTS

4.1 MEASURED QUANTITIES

The device measures directly and calculates a number of system quantities, which are updated every second. You can view these values in the relevant MEASUREMENT columns or with the Measurement Viewer in the settings application software. Depending on the model, the device may measure and display some or more of the following quantities:

- Measured and calculated analogue current and voltage values
- Power and energy quantities
- Peak, fixed and rolling demand values
- Frequency measurements
- Thermal measurements

4.1.1 MEASURED AND CALCULATED CURRENTS

The device measures phase-to-phase and phase-to-neutral current values. The values are produced by sampling the analogue input quantities, converting them to digital quantities to present the magnitude and phase values. Sequence quantities are produced by processing the measured values. These are also displayed as magnitude and phase angle values.

These measurements are contained in the *MEASUREMENTS 1* column.

4.1.2 MEASURED AND CALCULATED VOLTAGES

The device measures phase-to-phase and phase-to-neutral voltage values. The values are produced by sampling the analogue input quantities, converting them to digital quantities to present the magnitude and phase values. Sequence quantities are produced by processing the measured values. These are also displayed as magnitude and phase angle values.

These measurements are contained in the *MEASUREMENTS 1* column.

4.1.3 POWER AND ENERGY QUANTITIES

Using the measured voltages and currents the device calculates the apparent, real and reactive power quantities. These are produced on a phase by phase basis together with three-phase values based on the sum of the three individual phase values. The signing of the real and reactive power measurements can be controlled using the measurement mode setting. The four options are defined in the following table:

Measurement Mode	Parameter	Signing
0 (Default)	Export Power Import Power Lagging Vars Leading VArs	+ – + –
1	Export Power Import Power Lagging Vars Leading VArs	– + + –
2	Export Power Import Power Lagging Vars Leading VArs	+ – – +

Measurement Mode	Parameter	Signing
3	Export Power Import Power Lagging Vars Leading VArs	– + – +

The device also calculates the per-phase and three-phase power factors.

These power values increment the total real and total reactive energy measurements. Separate energy measurements are maintained for the total exported and imported energy. The energy measurements are incremented up to maximum values of 1000 GWhr or 1000 GVARhr at which point they reset to zero. It is possible to reset these values using the menu or remote interfaces using the Reset demand cell.

These measurements are contained in the *MEASUREMENTS 2* column.

4.1.4 DEMAND VALUES

The device produces fixed, rolling, and peak demand values. You reset these quantities using the ***Reset demand*** cell.

The fixed demand value is the average value of a quantity over the specified interval. Values are produced for three phase real and reactive power. The fixed demand values displayed are those for the previous interval. The values are updated at the end of the fixed demand period according to the ***Fix Dem Period*** setting in the *MEASURE'T SETUP* column.

The rolling demand values are similar to the fixed demand values, but a sliding window is used. The rolling demand window consists of a number of smaller sub-periods. The resolution of the sliding window is the sub-period length, with the displayed values being updated at the end of each of the sub-periods according to the ***Roll Sub Period*** setting in the *MEASURE'T SETUP* column.

Peak demand values are produced for each phase current and the real and reactive power quantities. These display the maximum value of the measured quantity since the last reset of the demand values.

These measurements are contained in the *MEASUREMENTS 2* column.

> *Note:*
> *A **Reset Demand** opto-input DDB signal is available.*

4.1.5 FREQUENCY MEASUREMENTS

The device produces a range of frequency statistics and measurements relating to the Frequency Protection function. These include Check synchronisation and Slip frequency measurements found in the *MEASUREMENTS 1* column, Rate of Change of Frequency measurements found in the *MEASUREMENTS 3* column, and Frequency Protection statistics found in the *FREQUENCY STAT.* column.

The device produces the slip frequency measurement by measuring the rate of change of phase angle between the bus and line voltages, over a one-cycle period. The slip frequency measurement assumes the bus voltage to be the reference phasor.

4.1.6 OTHER MEASUREMENTS

Depending on the model, the device produces a range of other measurements such as thermal measurements.

These measurements are contained in the *MEASUREMENTS 3* column.

4.2 MEASUREMENT SETUP

You can define the way measurements are set up and displayed using the *MEASURE'T SETUP* column and the measurements are shown in the relevant MEASUREMENTS tables.

4.3 FAULT LOCATOR

Some models provide fault location functionality. It is possible to identify the fault location by measuring the fault voltage and current magnitude and phases and presenting this information to a Fault Locator function. The fault locator is triggered whenever a fault record is generated, and the subsequent fault location data is included as part of the fault record. This information is also displayed in the ***Fault Location*** cell in the *VIEW RECORDS* column. This cell will display the fault location in metres, miles ohms or percentage, depending on the chosen units in the ***Fault Location*** cell of the *MEASURE'T SETUP* column.

The Fault Locator uses pre-fault and post-fault analogue input signals to calculate the fault location. The result is included it in the fault record. The pre-fault and post-fault voltages are also presented in the fault record.

4.3.1 FAULT LOCATOR SETTINGS EXAMPLE

Assuming the following data for the protected line:

Parameter	Value
CT Ratio	1200/5
VT Ratio	230000/115
Line Length	10 km
Positive sequence line impedance ZL1 (per km|)	0.089+j0.476 Ohms/km
Zero sequence line impedance ZL0	0.34+j1.03 ohms/km
Zero sequence mutual impedance ZM0	0.1068+j0.5712 Ohms/km

The line impedance magnitude and angle settings are calculated as follows:

- Ratio of secondary to primary impedance = CT ratio/VT ratio = 0.12
- Positive sequence line impedance ZL1 (total) = 0.12 × 10(0.484∠79.4°) = 0.58 ∠79.4°
- Therefore set line length = 0.58
- Line angle = 79°

The residual impedance compensation magnitude and angle are calculated using the following formula:

$$KZn = \frac{ZL0 - ZL1}{3ZL1} = \frac{(0.34 + j1.03) - (0.089 + j0.476)}{3(0.484\angle 79.4°)} = \frac{0.6\angle 65.2°}{1.45\angle 79.4°} = 0.41\angle -14.2°$$

Therefore the settings are:

- KZN Residual = 0.41
- KZN Res Angle = -14

4.4 OPTO-INPUT TIME STAMPING

Each opto-input sample is time stamped within a tolerance of +/- 1 ms with respect to the Real Time Clock. These time stamps are used for the opto event logs and for the disturbance recording. The device needs to be synchronised accurately to an external clock source such as an IRIG-B signal or a master clock signal provided in the relevant data protocol.

For both the filtered and unfiltered opto-inputs, the time stamp of an opto-input change event is the sampling time at which the change of state occurred. If multiple opto-inputs change state at the same sampling interval, these state changes are reported as a single event.

5 CB CONDITION MONITORING

The device records various statistics related to each circuit breaker trip operation, allowing an accurate assessment of the circuit breaker condition to be determined. The circuit breaker condition monitoring counters are incremented every time the device issues a trip command.

These statistics are available in the *CB CONDITION* column. The menu cells are counter values only, and cannot be set directly. The counters may be reset, however, during maintenance. This is achieved with the setting ***Reset CB Data.***

Note:
When in Commissioning test mode the CB condition monitoring counters are not updated.

5.1 APPLICATION NOTES

5.1.1 SETTING THE THRESHOLDS FOR THE TOTAL BROKEN CURRENT

Where power lines use oil circuit breakers (OCBs), changing of the oil accounts for a significant proportion of the switchgear maintenance costs. Often, oil changes are performed after a fixed number of CB fault operations. However, this may result in premature maintenance where fault currents tend to be low, because oil degradation may be slower than would normally be expected. The Total Current Accumulator (I^ counter) cumulatively stores the total value of the current broken by the circuit breaker providing a more accurate assessment of the circuit breaker condition.

The dielectric withstand of the oil generally decreases as a function of I^2t, where 'I' is the broken fault current and 't' is the arcing time within the interrupter tank. The arcing time cannot be determined accurately, but is generally dependent on the type of circuit breaker being used. Instead, you set a factor (***Broken I^***) with a value between 1 and 2, depending on the circuit breaker.

Most circuit breakers would have this value set to '2', but for some types of circuit breaker, especially those operating on higher voltage systems, a value of 2 may be too high. In such applications ***Broken I^*** may be set lower, typically 1.4 or 1.5.

The setting range for ***Broken I^*** is variable between 1.0 and 2.0 in 0.1 steps.

Note:
Any maintenance program must be fully compliant with the switchgear manufacturer's instructions.

5.1.2 SETTING THE THRESHOLDS FOR THE NUMBER OF OPERATIONS

Every circuit breaker operation results in some degree of wear for its components. Therefore routine maintenance, such as oiling of mechanisms, may be based on the number of operations. Suitable setting of the maintenance threshold will allow an alarm to be raised, indicating when preventative maintenance is due. Should maintenance not be carried out, the device can be set to lockout the autoreclose function on reaching a second operations threshold (***No. CB ops Lock***). This prevents further reclosure when the circuit breaker has not been maintained to the standard demanded by the switchgear manufacturer's maintenance instructions.

Some circuit breakers, such as oil circuit breakers (OCBs) can only perform a certain number of fault interruptions before requiring maintenance attention. This is because each fault interruption causes carbonising of the oil, degrading its dielectric properties. The maintenance alarm threshold (setting ***No. CB Ops Maint***) may be set to indicate the requirement for oil dielectric testing, or for more comprehensive maintenance. Again, the lockout threshold ***No. CB Ops Lock*** may be set to disable autoreclosure when repeated further fault interruptions could not be guaranteed. This minimises the risk of oil fires or explosion.

5.1.3 SETTING THE THRESHOLDS FOR THE OPERATING TIME

Slow CB operation indicates the need for mechanism maintenance. Alarm and lockout thresholds (***CB Time Maint*** and ***CB Time Lockout***) are provided to enforce this. They can be set in the range of 5 to 500 ms. This time relates to the interrupting time of the circuit breaker.

5.1.4 SETTING THE THRESHOLDS FOR EXCESSSIVE FAULT FREQUENCY

Persistent faults will generally cause autoreclose lockout, with subsequent maintenance attention. Intermittent faults such as clashing vegetation may repeat outside of any reclaim time, and the common cause might never be investigated. For this reason it is possible to set a frequent operations counter, which allows the number of operations ***Fault Freq Count*** over a set time period ***Fault Freq Time*** to be monitored. A separate alarm and lockout threshold can be set.

6 CB STATE MONITORING

CB State monitoring is used to verify the open or closed state of a circuit breaker. Most circuit breakers have auxiliary contacts through which they transmit their status (open or closed) to control equipment such as IEDs. These auxiliary contacts are known as:

- 52A for contacts that follow the state of the CB
- 52B for contacts that are in opposition to the state of the CB

This device can be set to monitor both of these types of circuit breaker state indication. If the state is unknown for some reason, an alarm can be raised.

Some CBs provide both sets of contacts. If this is the case, these contacts will normally be in opposite states. Should both sets of contacts be open, this would indicate one of the following conditions:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective
- CB is in isolated position

Should both sets of contacts be closed, only one of the following two conditions would apply:

- Auxiliary contacts/wiring defective
- Circuit Breaker (CB) is defective

If any of the above conditions exist, an alarm will be issued after a 5 s time delay. An output contact can be assigned to this function via the programmable scheme logic (PSL). The time delay is set to avoid unwanted operation during normal switching duties.

In the CB CONTROL column there is a setting called ***CB Status Input***. This cell can be set at one of the following four options:

- None
- 52A
- 52B
- Both 52A and 52B

Where *None* is selected no CB status is available. Where only 52A is used on its own then the device will assume a 52B signal opposite to the 52A signal. Circuit breaker status information will be available in this case but no discrepancy alarm will be available. The above is also true where only a 52B is used. If both 52A and 52B are used then status information will be available and in addition a discrepancy alarm will be possible, according to the following table:

Auxiliary Contact Position		CB State Detected	Action
52A	52B		
Open	Closed	Breaker open	Circuit breaker healthy
Closed	Open	Breaker closed	Circuit breaker healthy
Closed	Closed	CB failure	Alarm raised if the condition persists for greater than 5 s
Open	Open	State unknown	Alarm raised if the condition persists for greater than 5 s

6.1 CB STATE MONITORING LOGIC

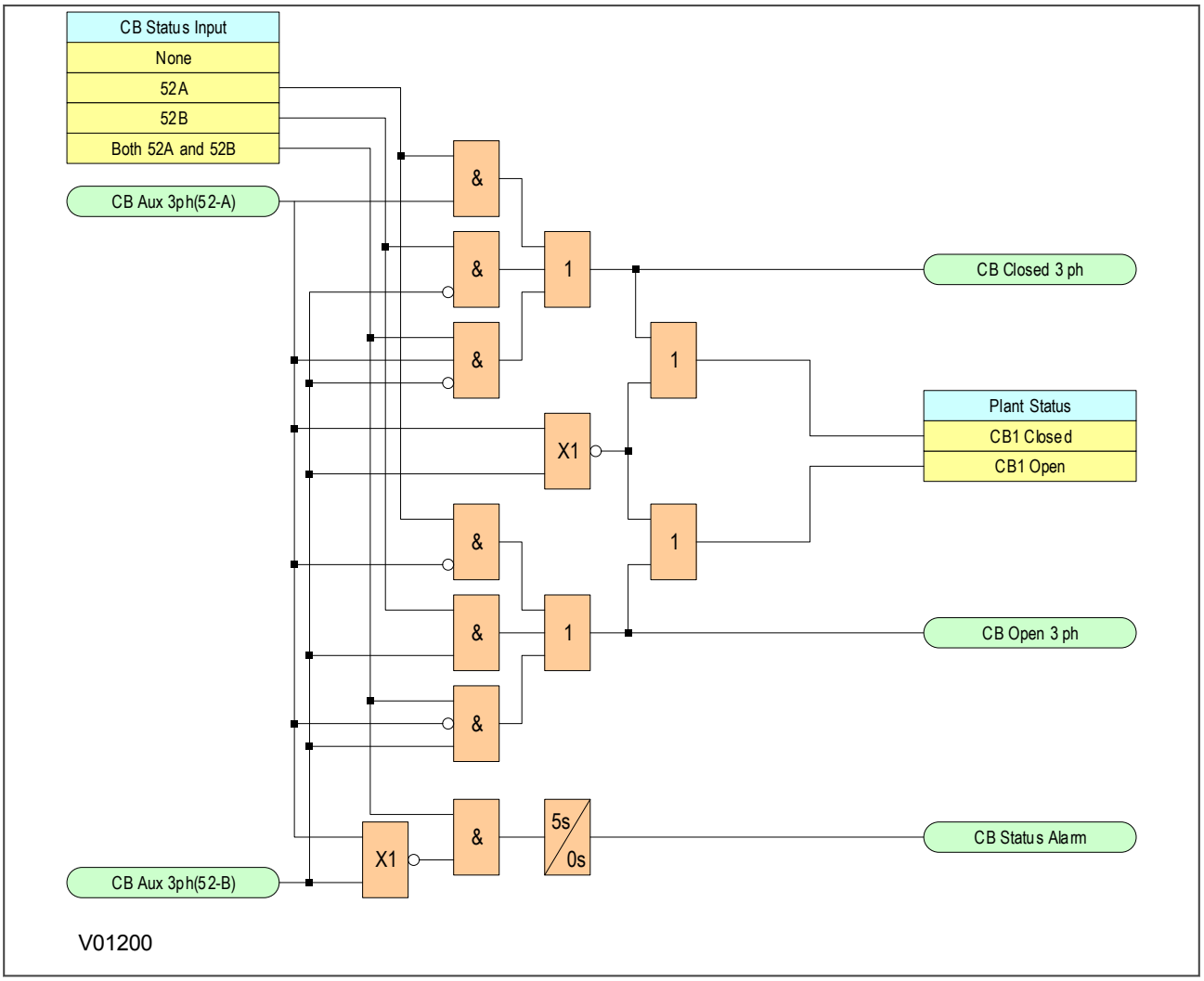


Figure 161: CB State Monitoring logic

7 CIRCUIT BREAKER CONTROL

Although some circuit breakers do not provide auxiliary contacts, most provide auxiliary contacts to reflect the state of the circuit breaker. These are:

- CBs with 52A contacts (where the auxiliary contact follows the state of the CB)
- CBs with 52B contacts (where the auxiliary contact is in the opposite state from the state of the CB)
- CBs with both 52A and 52B contacts

Circuit Breaker control is only possible if the circuit breaker in question provides auxiliary contacts. The ***CB Status Input*** cell in the *CB CONTROL* column must be set to the type of circuit breaker. If no CB auxiliary contacts are available then this cell should be set to `None`, and no CB control will be possible.

For local control, the ***CB control by*** cell should be set accordingly.

The output contact can be set to operate following a time delay defined by the setting ***Man Close Delay***. One reason for this delay is to give personnel time to safely move away from the circuit breaker following a CB close command.

The control close cycle can be cancelled at any time before the output contact operates by any appropriate trip signal, or by activating the ***Reset Close Dly*** DDB signal.

The length of the trip and close control pulses can be set via the ***Trip Pulse Time*** and **Close Pulse Time** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

The ***Reset Lockout by*** setting is used to enable or disable the resetting of lockout automatically from a manual close after the time set by ***Man Close RstDly***.

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) an alarm is generated after the relevant trip or close pulses have expired. These alarms can be viewed on the LCD display, remotely, or can be assigned to output contacts using the programmable scheme logic (PSL).

> *Note:*
> *The **CB Healthy Time** and **Sys Check time** set under this menu section are applicable to manual circuit breaker operations only. These settings are duplicated in the AUTORECLOSE menu for autoreclose applications.*

The ***Lockout Reset*** and ***Reset Lockout by*** settings are applicable to CB Lockouts associated with manual circuit breaker closure, CB Condition monitoring (Number of circuit breaker operations, for example) and autoreclose lockouts.

The device includes the following options for control of a single circuit breaker:

- The IED menu (local control)
- The Hotkeys (local control)
- The function keys (local control)
- The opto-inputs (local control)
- SCADA communication (remote control)

7.1 CB CONTROL USING THE IED MENU

You can control manual trips and closes with the ***CB Trip/Close*** command in the *SYSTEM DATA* column. This can be set to `No Operation`, `Trip`, or `Close` accordingly.

For this to work you have to set the ***CB control by*** cell to option 1 `Local`, option 3 `Local + Remote`, option 5 `Opto+Local`, or option 7 `Opto+Local+Remote` in the *CB CONTROL* column.

7.2 CB CONTROL USING THE HOTKEYS

The hotkeys allow you to manually trip and close the CB without the need to enter the *SYSTEM DATA* column. For this to work you have to set the ***CB control by*** cell to option 1 `Local`, option 3 `Local+Remote`, option 5 `Opto +Local`, or option 7 `Opto+Local+Remote` in the *CB CONTROL* column.

CB control using the hotkey is achieved by pressing the right-hand button directly below LCD screen. This button is only enabled if:

- The ***CB Control by*** setting is set to one of the options where local control is possible (option 1,3,5, or 7)
- The ***CB Status Input*** is set to '52A', '52B', or 'Both 52A and 52B'

If the CB is currently closed, the command text on the bottom right of the LCD screen will read `Trip`. Conversely, if the CB is currently open, the command text will read `Close`.

If you execute a `Trip`, a screen with the CB status will be displayed once the command has been completed. If you execute a `Close`, a screen with a timing bar will appear while the command is being executed. This screen also gives you the option to cancel or restart the close procedure. The time delay is determined by the ***Man Close Delay*** setting in the *CB CONTROL* menu. When the command has been executed, a screen confirming the present status of the circuit breaker is displayed. You are then prompted to select the next appropriate command or exit.

If no keys are pressed for a period of 5 seconds while waiting for the command confirmation, the device will revert to showing the CB Status. If no key presses are made for a period of 25 seconds while displaying the CB status screen, the device will revert to the default screen.

To avoid accidental operation of the trip and close functionality, the hotkey CB control commands are disabled for 10 seconds after exiting the hotkey menu.

The hotkey functionality is summarised graphically below:

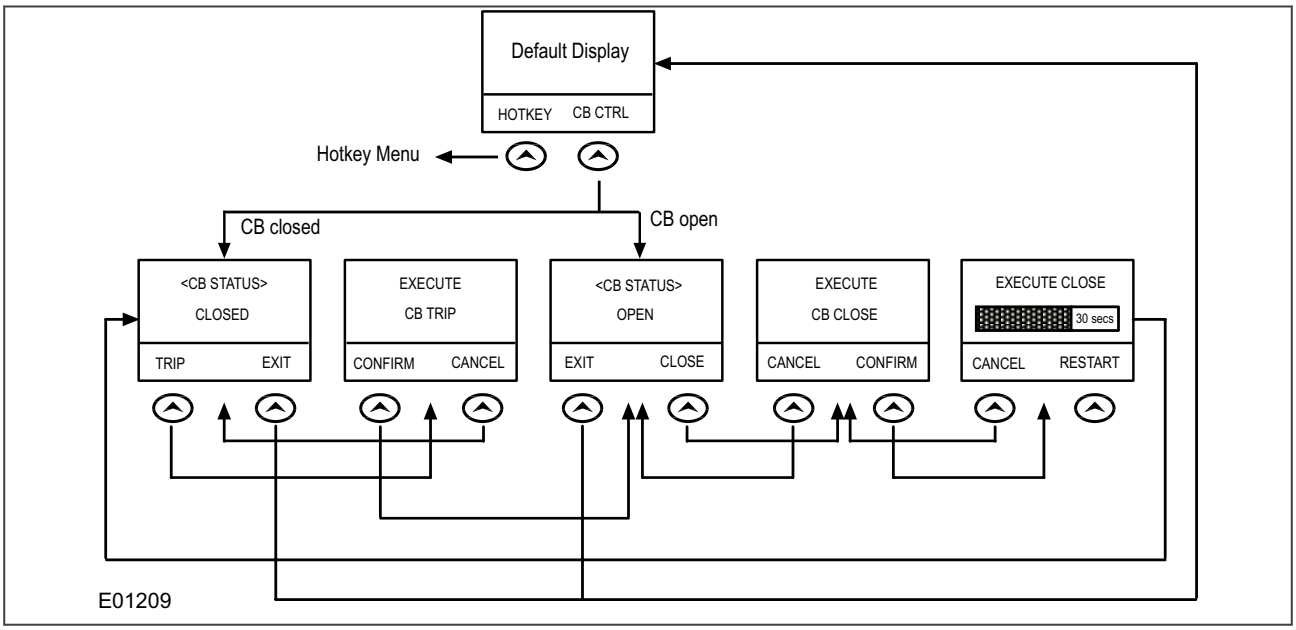


Figure 162: Hotkey menu navigation

7.3 CB CONTROL USING THE FUNCTION KEYS

For most models, you can also use the function keys to allow direct control of the circuit breaker. This has the advantage over hotkeys, that the LEDs associated with the function keys can indicate the status of the CB. The

default PSL is set up such that Function key 2 initiates a trip and Function key 3 initiates a close. For this to work you have to set the CB control by cell to option 5 *Opto+Local*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

As shown below, function keys 2 and 3 have already been assigned to CB control in the default PSL.

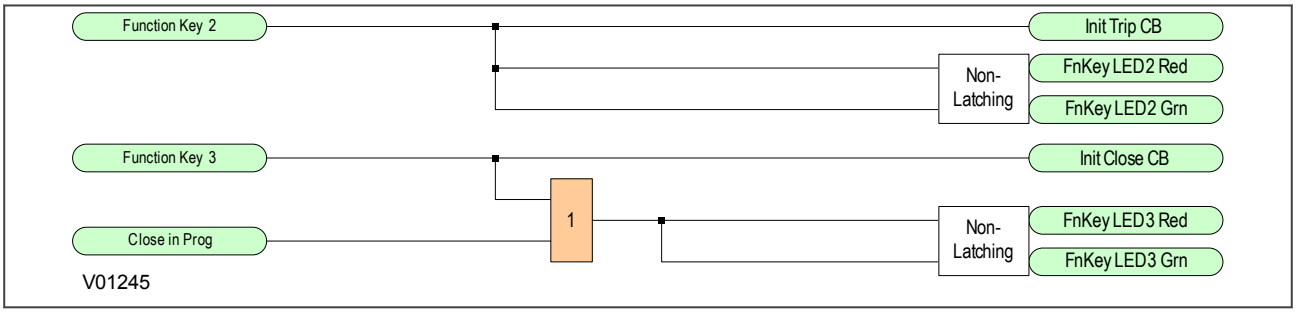


Figure 163: Default function key PSL

The programmable function key LEDs have been mapped such that they will indicate yellow whilst the keys are activated.

Note:
Not all models provide function keys.

7.4 CB CONTROL USING THE OPTO-INPUTS

Certain applications may require the use of push buttons or other external signals to control the various CB control operations. It is possible to connect such push buttons and signals to opto-inputs and map these to the relevant DDB signals.

For this to work, you have to set the ***CB control by*** cell to option 4 *opto*, option 5 *Opto+Local*, option 6 *Opto +Remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

7.5 REMOTE CB CONTROL

Remote CB control can be achieved by setting the ***CB Trip/Close*** cell in the *SYSTEM DATA* column to trip or close by using a command over a communication link.

For this to work, you have to set the ***CB control by*** cell to option 2 *Remote*, option 3 *Local+Remote*, option 6 *Opto+remote*, or option 7 *Opto+Local+Remote* in the *CB CONTROL* column.

We recommend that you allocate separate relay output contacts for remote CB control and protection tripping. This allows you to select the control outputs using a simple local/remote selector switch as shown below. Where this feature is not required the same output contact(s) can be used for both protection and remote tripping.

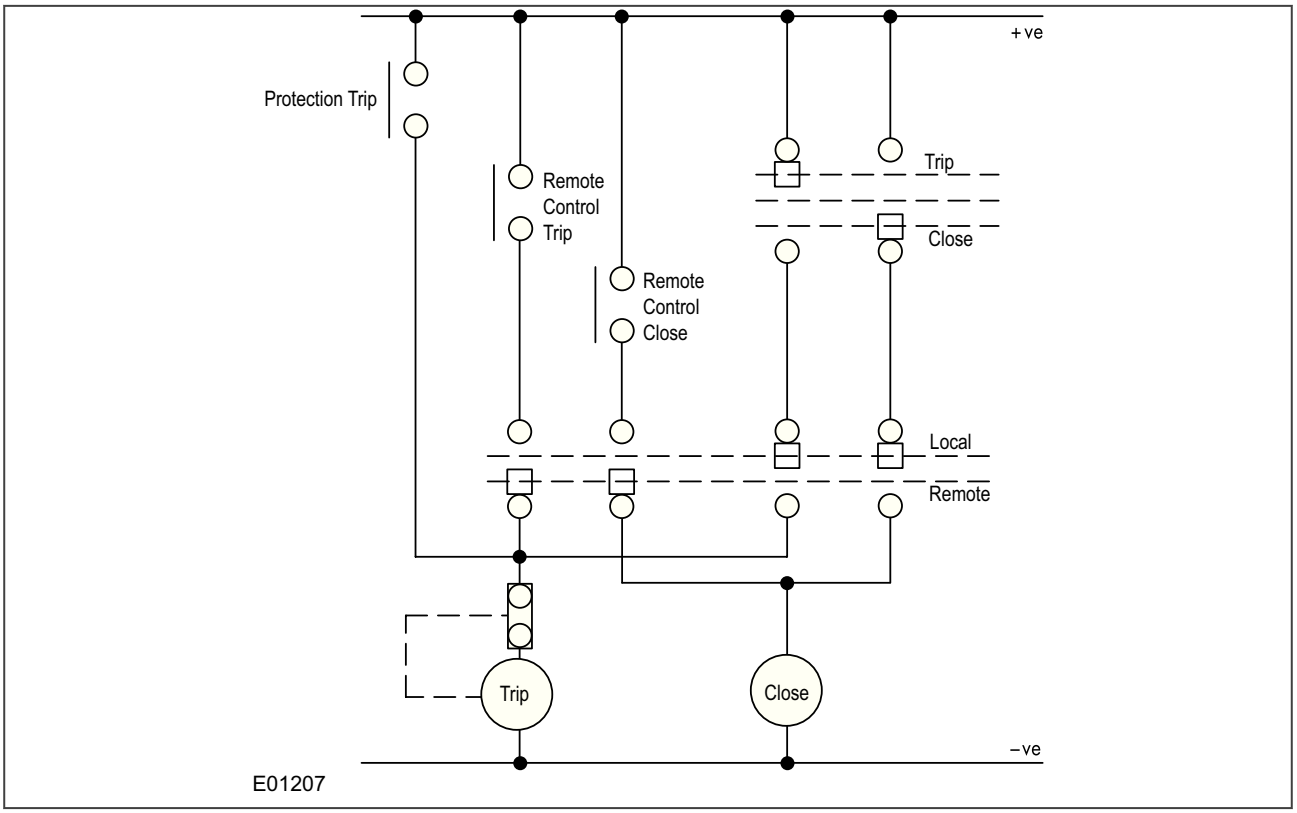


Figure 164: Remote Control of Circuit Breaker

7.6 SYNCHRONISATION CHECK

Where the check synchronism function is set, this can be enabled to supervise manual circuit breaker Close commands. A circuit breaker Close command will only be issued if the Check Synchronisation criteria are satisfied. A time delay can be set with the setting ***Sys Check time.*** If the Check Synchronisation criteria are not satisfied within the time period following a Close command the device will lockout and alarm.

7.7 CB HEALTHY CHECK

A CB Healthy check is available if required. This facility accepts an input to one of the opto-inputs to indicate that the breaker is capable of closing (e.g. that it is fully charged). A time delay can be set with the setting ***CB Healthy Time***. If the CB does not indicate a healthy condition within the time period following a Close command, the device will lockout and alarm.

7.8 CB CONTROL LOGIC

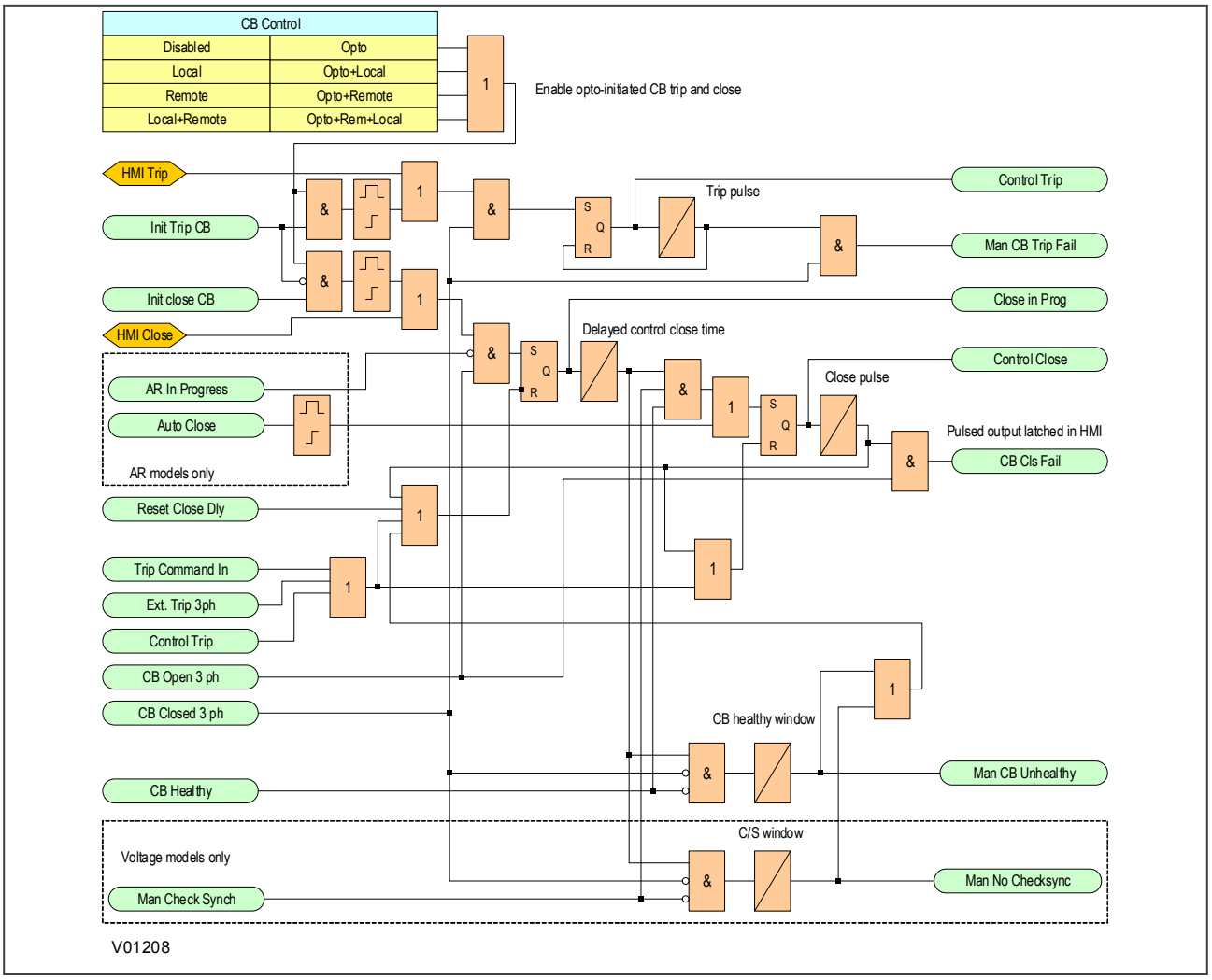


Figure 165: CB Control logic

8 POLE DEAD FUNCTION

The Pole Dead Logic is used to determine and indicate that one or more phases of the line are not energised. A Pole Dead condition is determined either by measuring:

- the line currents and/or voltages, or
- by monitoring the status of the circuit breaker auxiliary contacts, as shown by dedicated DDB signals.

It can also be used to block operation of underfrequency and undervoltage elements where applicable.

8.1 POLE DEAD LOGIC

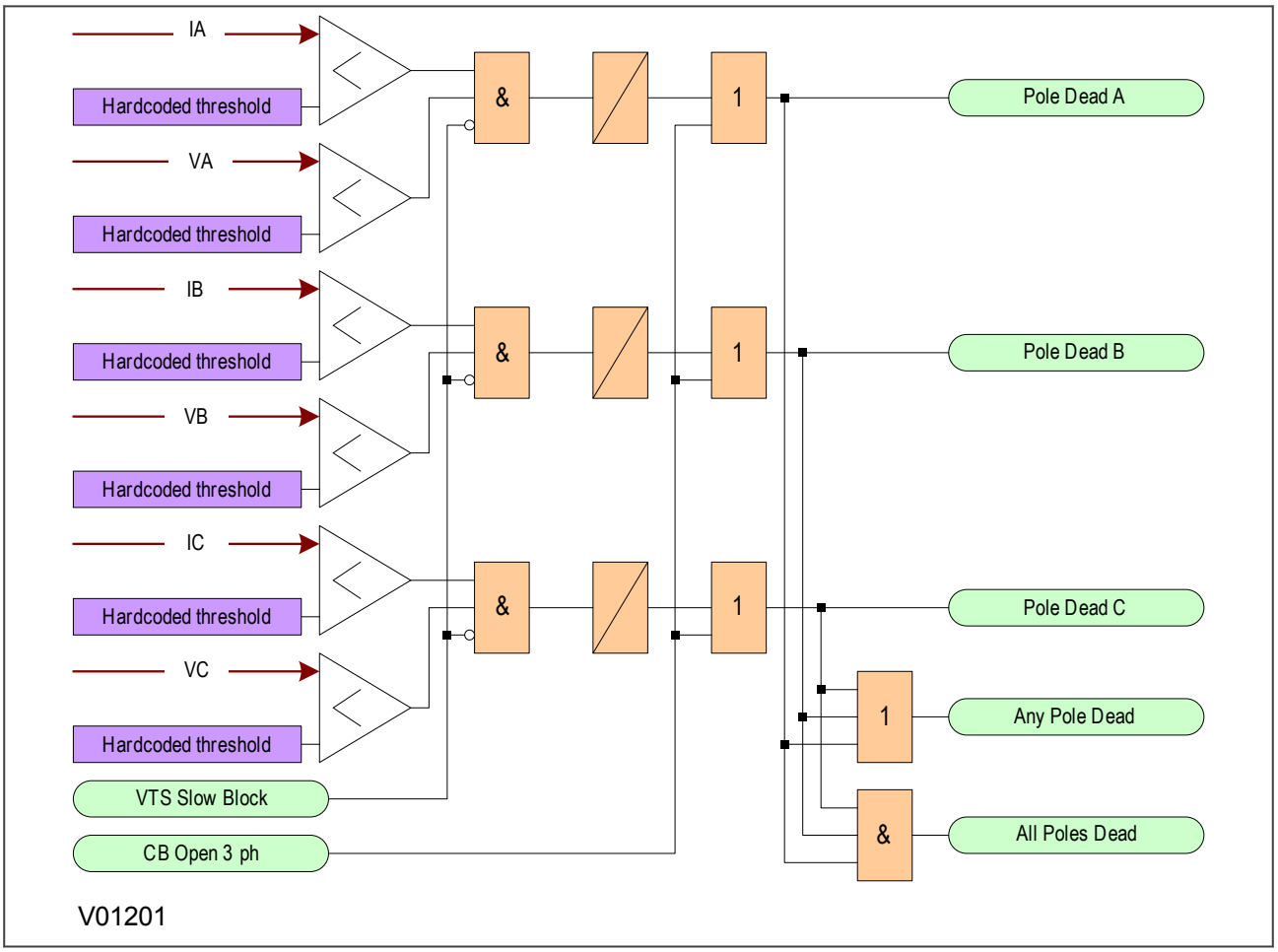


Figure 166: Pole Dead logic

If both the line current and voltage fall below certain thresholds, the device will initiate a Pole Dead condition. The undervoltage (V<) and undercurrent (I<) thresholds are hardcoded internally.

If one or more poles are dead, the device will indicate which phase is dead and will also assert the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal would be accompanied by the ***All Poles Dead*** signal.

If a VT fails, a ***VTS Slow Block*** signal is generated to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds. However, the VTS logic will not block the Pole Dead indications if they are initiated by a ***CB Open 3 ph*** signal. A ***CB Open 3 ph*** signal automatically initiates a Pole Dead condition regardless of the current and voltage measurement.

9 SYSTEM CHECKS

In some situations it is possible for both "bus" and "line" sides of a circuit breaker to be live when a circuit breaker is open - for example at the ends of a feeder that has a power source at each end. Therefore, it is normally necessary to check that the network conditions on both sides are suitable, before closing the circuit breaker. This applies to both manual circuit breaker closing and autoreclosing. If a circuit breaker is closed when the line and bus voltages are both live, with a large phase angle, frequency or magnitude difference between them, the system could be subjected to an unacceptable shock, resulting in loss of stability, and possible damage to connected machines.

The System Checks functionality involves monitoring the voltages on both sides of a circuit breaker, and if both sides are live, performing a synchronisation check to determine whether any differences in voltage magnitude, phase angle or frequency are within permitted limits.

The pre-closing system conditions for a given circuit breaker depend on the system configuration, and for autoreclosing, on the selected autoreclose program. For example, on a feeder with delayed autoreclosing, the circuit breakers at the two line ends are normally arranged to close at different times. The first line end to close usually has a live bus and a dead line immediately before reclosing. The second line end circuit breaker now sees a live bus and a live line.

If there is a parallel connection between the ends of the tripped feeder the frequencies will be the same, but any increased impedance could cause the phase angle between the two voltages to increase. Therefore just before closing the second circuit breaker, it may be necessary to perform a synchronisation check, to ensure that the phase angle between the two voltages has not increased to a level that would cause unacceptable shock to the system when the circuit breaker closes.

If there are no parallel interconnections between the ends of the tripped feeder, the two systems could lose synchronism altogether and the frequency at one end could "slip" relative to the other end. In this situation, the second line end would require a synchronism check comprising both phase angle and slip frequency checks.

If the second line-end busbar has no power source other than the feeder that has tripped; the circuit breaker will see a live line and dead bus assuming the first circuit breaker has re-closed. When the second line end circuit breaker closes the bus will charge from the live line (dead bus charge).

9.1 SYSTEM CHECKS IMPLEMENTATION

The System Checks function provides *Live/Dead Voltage Monitoring*, two stages of *Check Synchronisation* and *System Split* indication.

The System Checks function is enabled or disabled by the ***System Checks*** setting in the *CONFIGURATION* column. If ***System Checks*** is disabled, the *SYSTEM CHECKS* menu becomes invisible, and a ***SysChks Inactive*** DDB signal is set.

9.1.1 VT CONNECTIONS

The device provides inputs for a three-phase "Main VT" and at least one single-phase VT for check synchronisation or residual voltage. Depending on the primary system arrangement, the Main VT may be located on either the line-side of the busbar-side of the circuit breaker, with the 4th VT on the other. Normally, the Main VT is located on the line-side (as per the default setting), but this is not always the case. For this reason, a setting is provided where you can define this. This is the ***Main VT Location*** setting, which is found in the *CT AND VT RATIOS* column.

The 4th VT may be connected to one of the phase-to-phase voltages or phase-to-neutral voltages. This needs to be defined using the ***CS Input*** setting in the *CT AND VT RATIOS* column. Options are, A-B, B-C, C-A, A-N, B-N, or C-N.

9.1.2 VOLTAGE MONITORING

The settings in the *VOLTAGE MONITORS* sub-heading in the *SYSTEM CHECKS* column allow you to define the threshold at which a voltage is considered live, and a threshold at which the voltage is considered dead. These thresholds apply to both line and bus sides. If the measured voltage falls below the ***Dead Voltage*** setting, a DDB signal is generated (***Dead Bus***, or ***Dead Line***, depending on which side is being measured). If the measured voltage

exceeds the ***Live Voltage*** setting, a DDB signal is generated (***Live Bus***, or ***Live Line***, depending on which side is being measured).

9.1.3 CHECK SYNCHRONISATION

The device provides two stages of Check Synchronisation. The first stage (CS1) is intended for use in synchronous systems. This means, where the frequencies and phase angles of both sides are compared and if the difference is within set limits, the circuit breaker is allowed to close. The second stage (CS2) is similar to stage, but has an additional adaptive setting. The second stage CS2 is intended for use in asynchronous systems, i.e. where the two sides are out of synchronism and one frequency is slipping continuously with respect to another. If the closing time of the circuit breaker is known, the CB Close command can be issued at a definite point in the cycle such that the CB closes at the point when both sides are in phase.

In situations where it is possible for the voltages on either side of a circuit breaker to be either synchronous or asynchronous, both CS1 and CS2 can be enabled to provide a CB Close signal if either set of permitted closing conditions is satisfied.

Each stage can also be set to inhibit circuit breaker closing if selected blocking conditions such as overvoltage, undervoltage or excessive voltage magnitude difference are detected. CS2 requires the phase angle difference to be decreasing in magnitude before permitting the circuit breaker to close. CS2 has an optional "Adaptive" closing feature, which issues the permissive close signal when the predicted phase angle difference immediately prior to the instant of circuit breaker main contacts closing (i.e. after CB Close time) is as close as practicable to zero.

Slip frequency is the rate of change of phase between each side of the circuit breaker, which is measured by the difference between the voltage signals on either side of the circuit breaker.

Having two system synchronism check stages available allows the circuit breaker closing to be enabled under different system conditions (for example, low slip / moderate phase angle, or moderate slip / small phase angle).

The settings specific to Check Synchronisation are found under the sub-heading *CHECK SYNC* in the *SYSTEM CHECKS* column. The only difference between the CS1 settings and the CS2 settings is that ***CS2 Slip Control*** setting has an option for predictive closure of CB (*Freq + CB Comp*).

9.1.4 CHECK SYNCRONISATION VECTOR DIAGRAM

The following vector diagram represents the conditions for the System Check functionality. The Dead Volts setting is represented as a circle around the origin whose radius is equal to the maximum voltage magnitude, whereby the voltage can be considered dead. The nominal line voltage magnitude is represented by a circle around the origin whose radius is equal to the nominal line voltage magnitude. The minimum voltage magnitude at which the system can be considered as Live, is the magnitude difference between the bus and line voltages.

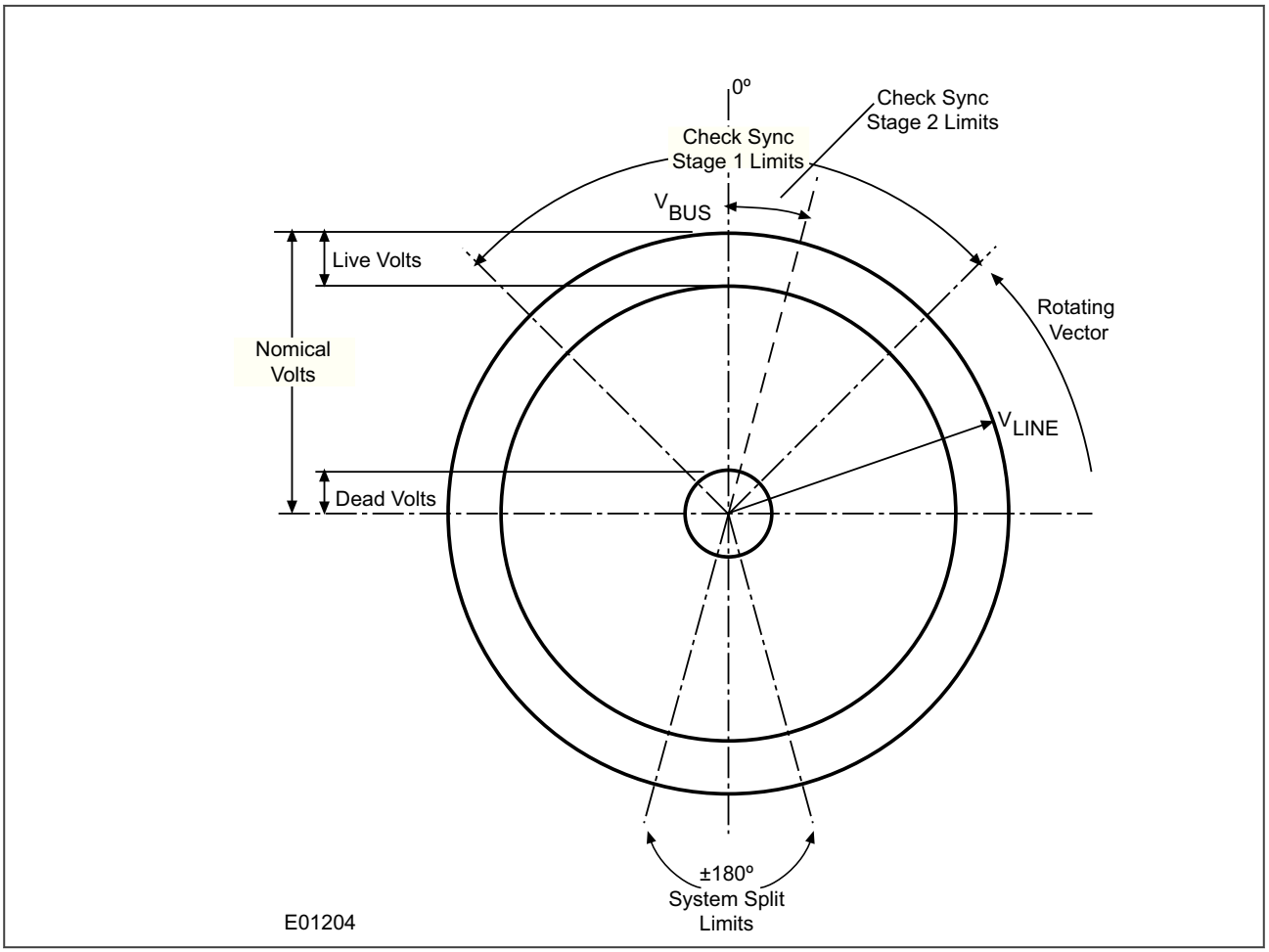


Figure 167: Check Synchronisation vector diagram

9.1.5 SYSTEM SPLIT

If the line side and bus side are of the same frequency (i.e. in synchronism) but have a large phase angle between them (180° +/- the set limits), the system is said to be 'Split'. If this is the case, the device will detect this and issue an alarm signal indicating this.

The settings specific to System Split functionality are found under the sub-heading *SYSTEM SPLIT* in the *SYSTEM CHECKS* column.

9.2 SYSTEM CHECK LOGIC

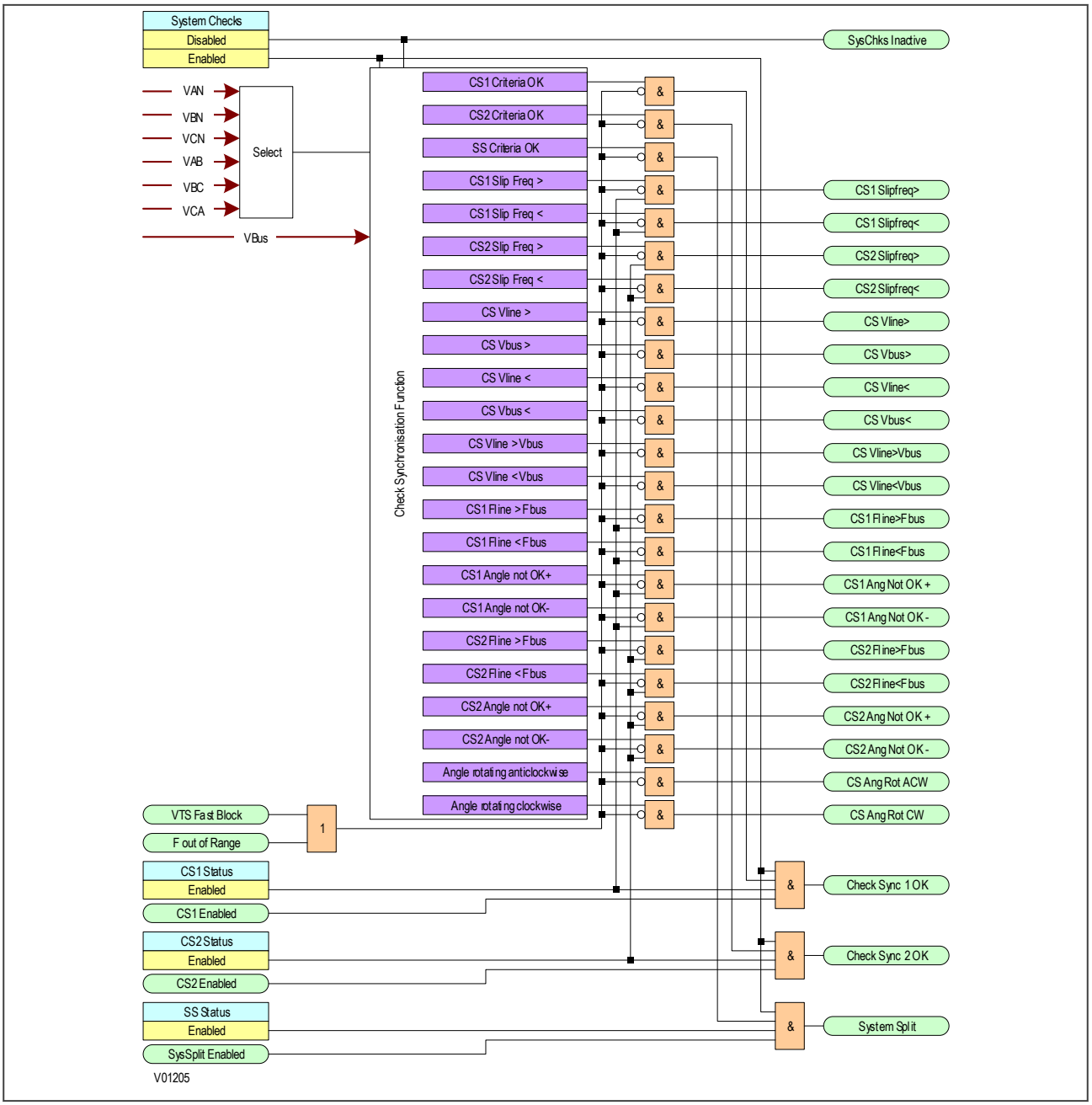


Figure 168: System Check logic

9.3 SYSTEM CHECK PSL

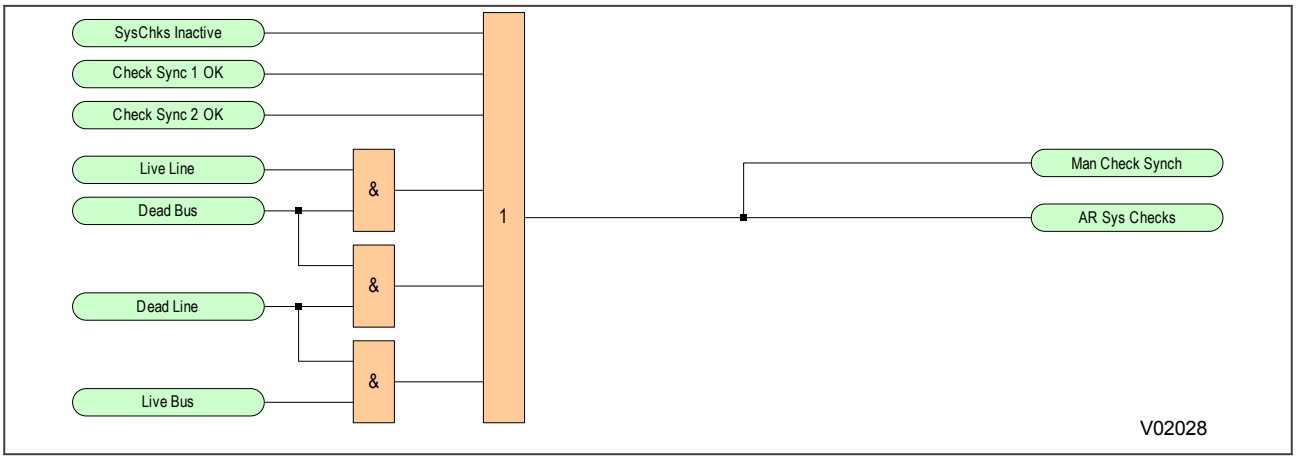


Figure 169: System Check PSL

9.4 APPLICATION NOTES

9.4.1 SLIP CONTROL

Slip control can be achieved by timer, by frequency or by both. The settings CS1 Slip Control and CS2 Slip Control are used to determine which type of slip control is to be used. As the device supports direct measurement of frequency, you would normally use frequency.

If you are using Slip Control by Timer, the combination of Phase Angle and Timer settings determines an effective maximum slip frequency, calculated as:

$$2A/360T - for\ CS1$$

$$A/360T - for\ CS2$$

where:

- A = Phase Angle setting in degrees
- T = Slip Timer setting in seconds

Examples

For CS1, where the Phase Angle setting is 30° and the Timer setting is 3.3 s, the "slipping" vector has to remain within +/- 30° of the reference vector for at least 3.3 seconds. Therefore a synchronisation check output will not be given if the slip is greater than 2 x 30° in 3.3 seconds.

Therefore, the maximum slip frequency = 2x30/360x3.3 = 0.0505 hz.

For CS2, where the Phase Angle setting is 10° and the Timer setting is 0.1 sec., the slipping vector has to remain within 10° of the reference vector, with the angle decreasing, for 0.1 sec. When the angle passes through zero and starts to increase, the synchronisation check output is blocked. Therefore an output will not be given if the slip is greater than 10° in 0.1 second.

Therefore, the maximum slip frequency = 10/360x0.1 = 0.278 Hz.

Slip control by Timer is not practical for "large slip/small phase angle" applications, because the timer settings required are very small, sometimes less than 0.1 seconds. For these situations, slip control by frequency is better.

If Slip Control by Frequency + Timer is selected, for an output to be given, the slip frequency must be less than BOTH the set Slip Freq. value and the value determined by the Phase Angle and Timer settings.

9.4.2 USE OF CHECK SYNC 2 AND SYSTEM SPLIT

Check Sync 2 (CS2) and System Split functions are included for situations where the maximum permitted slip frequency and phase angle for synchronism checks can change due to adverse system conditions. A typical application is on a closely interconnected system, where synchronism is normally retained when a feeder is tripped. But under some circumstances, with parallel interconnections out of service, the feeder ends can drift out of synchronism when the feeder is tripped. Depending on the system and machine characteristics, the conditions for safe circuit breaker closing could be, for example:

Condition 1: For synchronized systems, with zero or very small slip:

- Slip <50 mHz; phase angle <30°

Condition 2: For unsynchronized systems, with significant slip:

- Slip < 250 mHz; phase angle <10° and decreasing

By enabling both CS1 and CS2, the device can be configured to allow CB closure if either of the two conditions is detected.

For manual circuit breaker closing with synchronism check, some utilities might prefer to arrange the logic to check initially for condition 1 only. However, if a System Split is detected before the condition 1 parameters are satisfied, the device will switch to checking for condition 2 parameters instead, based on the assumption that a significant degree of slip must be present when system split conditions are detected. This can be arranged by suitable PSL logic, using the System Check DDB signals.

9.4.3 PREDICTIVE CLOSURE OF CIRCUIT BREAKER

The setting ***CS2 Slip Control*** setting contains an option (freq + CB comp) for compensating the time taken to close the CB. When set to provide CB Close Time compensation, a predictive approach is used to close the circuit breaker ensuring that closing occurs at close to 0º therefore minimising the impact to the power system. The actual closing angle is subject to the constraints of the existing product architecture, i.e. the protection task runs twice per power system cycle, based on frequency tracking over the frequency range of 40 Hz to 70 Hz.

9.4.4 VOLTAGE AND PHASE ANGLE CORRECTION

For the Check Synchronisation function, the device needs to convert measured secondary voltages into primary voltages. In some applications, VTs either side of the circuit breaker may have different VT Ratios. In such cases, a magnitude correction factor is required.

There are some applications where the main VT is on the HV side of a transformer and the 4th VT (used for Check Sync) is on the LV side, or vice-versa. If the vector group of the transformer is not "0", the voltages are not in phase, so phase correction is also necessary.

The correction factors are as follows and are located in the *CT AND VT RATIOS* column:

- 4th VT V kSM, where kSM is the voltage correction factor.
- 4th VT Phase kSA, where kSA is the angle correction factor.

Assuming the ***C/S input*** setting is A-N, then:

The line and bus voltage magnitudes are matched if $V_{a\ sec} = V_{cs\ sec} \times$ 4th VT V kSA

The line and bus voltage angles are matched if $\angle V_{a\ sec} = \angle V_{cs\ sec}$ + 4th VT Phase kSA

The following application scenarios show where the voltage and angular correction factors are applied to match different VT ratios:

Scenario	Physical Ratios (ph-N Values)				Setting Ratios				CS Correction Factors	
	Main VT Ratio		4th VT Ratio		Main VT Ratio (ph-ph) Always		4th VT Ratio		kSM	kSA
	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)	Pri (kV)	Sec (V)		
1	220/√3	110/√3	132/√3	100/√3	220	110	132	100	1.1	30º
2	220/√3	110/√3	220/√3	110	220	110	127	110	0.577	0º
3	220/√3	110/√3	220/√3	110/3	220	110	381	110	1.732	0º

10 SWITCH STATUS AND CONTROL

All P40 Agile products support Switch Status and Control for up to 8 switchgear elements in an IEC61850 substation. The device is able to monitor the status of and control up to eight switches. The types of switch that can be controlled are:

- Load Break switch
- Disconnector
- Earthing Switch
- High Speed Earthing Switch

Consider the following feeder bay:

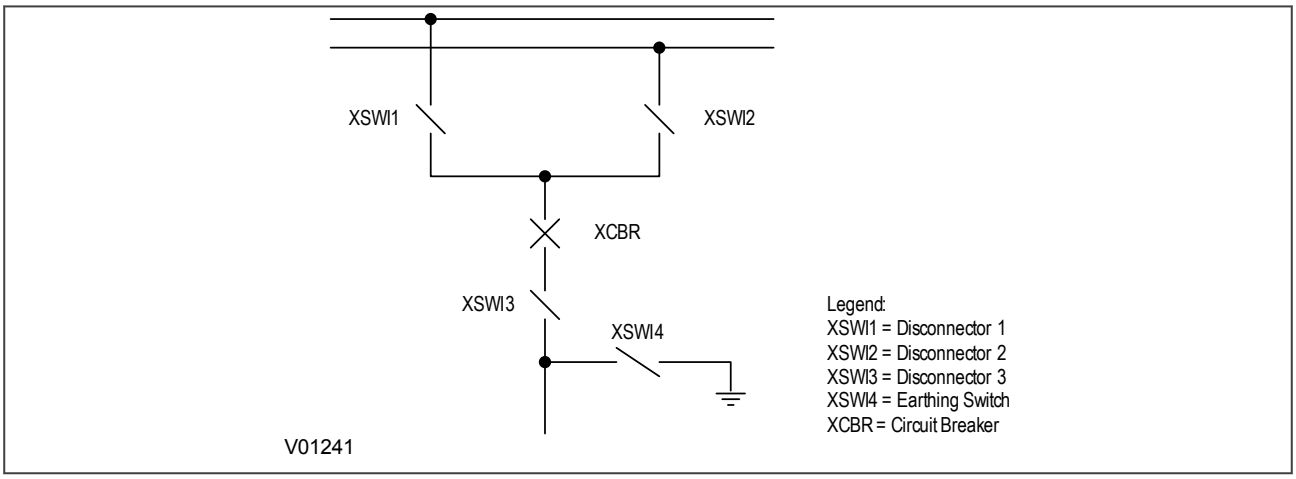


Figure 170: Representation of typical feeder bay

This bay shows four switches of the type LN XSWI and one circuit breaker of type LN XCBR. In this example, the switches XSWI1 – XSWI3 are disconnectors and XCSWI4 is an earthing switch.

For the device to be able to control the switches, the switches must provide auxiliary contacts to indicate the switch status. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers.

There are eight sets of settings in the *SWITCH CONTROL* column, which allow you to set up the Switch control, one set for each switch. These settings are as follows:

SWITCH1 Type

This setting defines the type of switch. It can be a load breaking switch, a disconnector, an earthing switch or a high speed earthing switch.

SWI1 Status Inpt

This setting defines the type of auxiliary contacts that will be used for the control logic. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers. "A" contacts match the status of the primary contacts, whilst "B" contacts are of the opposite polarity.

SWI1 Control by

This setting determines how the switch is to be controlled. This can be Local (using the device directly) remote (using a communications link), or both.

SWI1 Trip/Close

This is a command to directly trip or close the switch.

SWI1 Trp Puls T and ***SWI1 Cls Puls T***

These settings allow you to control the width of the open and close pulses.

SWI1 Sta Alrm T

This setting allows you to define the duration of wait timer before the relay raises a status alarm.

SWI1 Trp Alrm T and ***SWI1 Cls Alrm T***

These settings allow you to control the delay of the open and close alarms when the final switch status is not in line with expected status.

SWI1 Operations

This is a data cell, which displays the number of switch operations that have taken place. It is an accumulator, which you can reset using the ***Reset SWI1 Data*** setting

Reset SWI1 Data

This setting resets the switch monitoring data.

Note:
Settings for switch 1 are shown, but settings for all other switch elements are the same.

10.1 SWITCH STATUS LOGIC

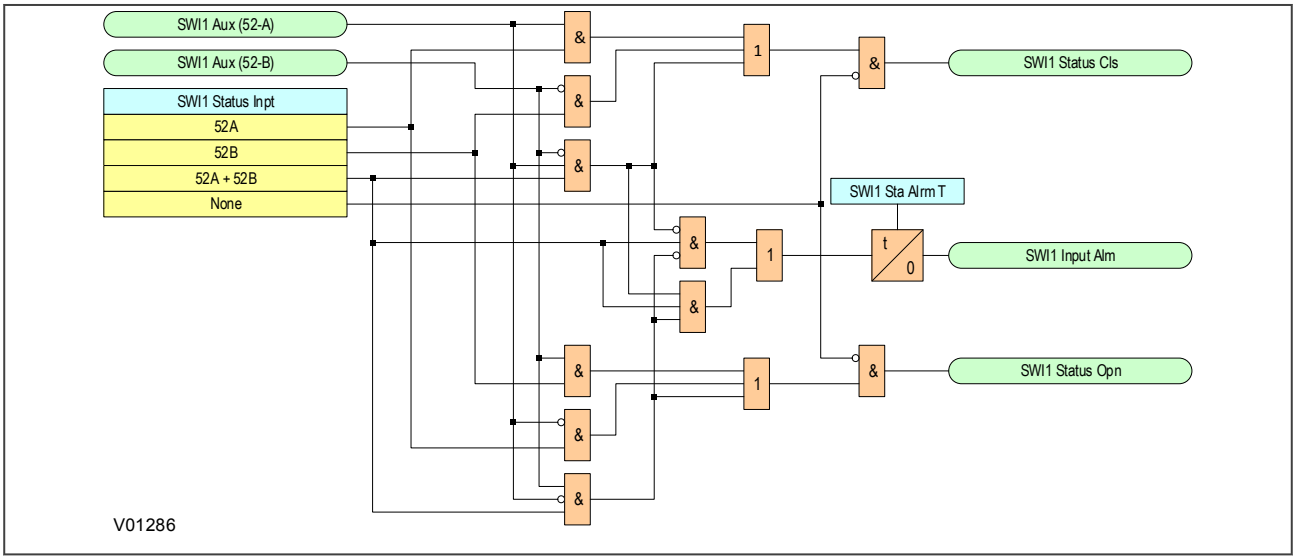


Figure 171: Switch Status logic

10.2 SWITCH CONTROL LOGIC

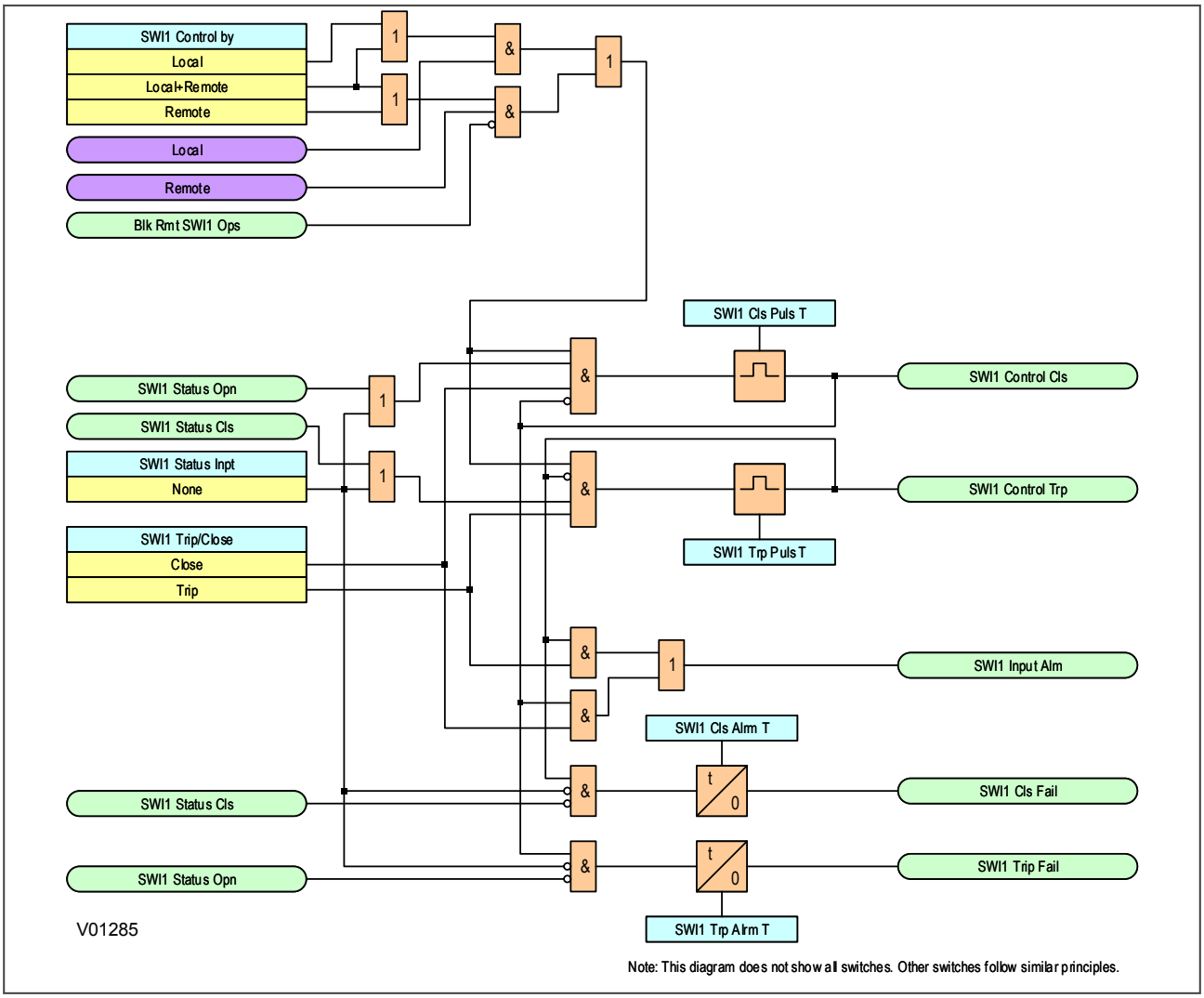


Figure 172: Switch Control logic

CHAPTER 15

SUPERVISION

1 CHAPTER OVERVIEW

This chapter describes the supervison functions.

This chapter contains the following sections:

2 DC SUPPLY MONITOR

This product can be powered using either a DC or AC supply. As a DC supply is normally used, a DC Supply Monitoring feature is included to indicate the DC supply status. The nominal DC Station supply is 48 V DC, which is provided by a bank of batteries. It is sometimes possible for this nominal supply to fall below or rise above acceptable operational limits. If the voltage is too high, it may indicate overcharging. If the voltage is too low, it may indicate a failing battery.

In such cases it is very useful to have DC supply monitoring functionality. The P40 Agile products provide such functionality by measuring the auxiliary DC supply fed into the device and processing this information using settings to define certain limits. In addition, the DC Auxiliary Supply value can be displayed on the front panel LCD to a resolution of 0.1 V DC. The measuring range is from 19 V DC to 300 V DC.

2.1 DC SUPPLY MONITOR IMPLEMENTATION

The P40Agile products provide three DC supply monitoring zones; zone 1, zone 2, and zone 3. This allows you to have multiple monitoring criteria. Each zone must be configured to correspond to either an overvoltage condition or an undervoltage condition. A single zone cannot be configured to provide an alarm for both undervoltage and overvoltage conditions. Typically, you would configure zones 1 and 2 for undervoltage conditions, whereby the lowest limit is set very low, and zone 3 for an overvoltage condition whereby the upper limit is very high.

This is best illustrated diagrammatically:

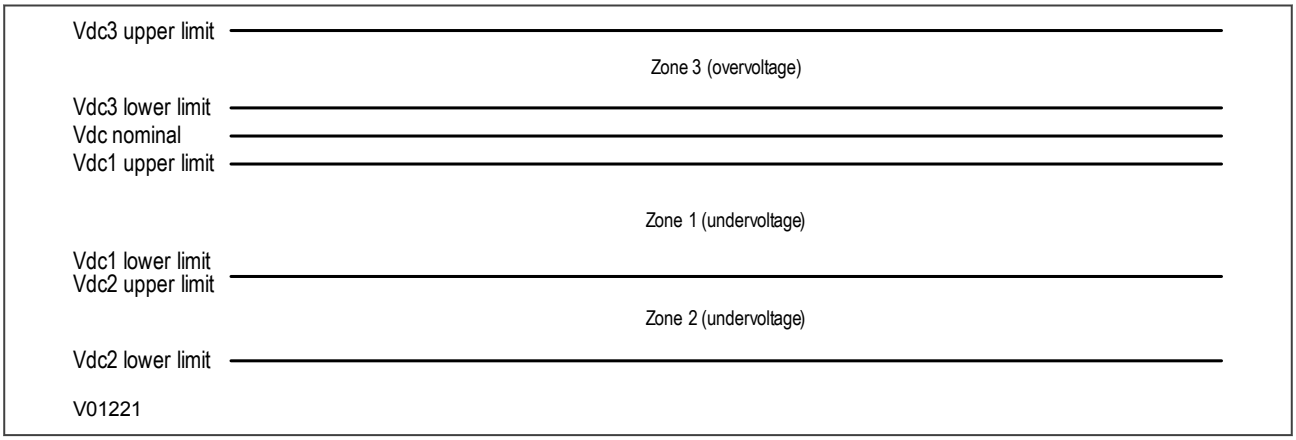


Figure 173: DC Supply Monitor zones

It is possible to have overlapping zones whereby zone 2 upper limit is lower than zone 1 lower limit in the above example.

The DC Supply Monitoring function is implemented using settings in the *DC SUP. MONITOR* column. There are three sets of settings; one for each of the zones. The settings allow you to:

- Enable or disable the function for each zone
- Set a lower voltage limit for each zone
- Set an upper voltage limit for each zone
- Set a time delay for each zone

2.2 DC SUPPLY MONITOR LOGIC

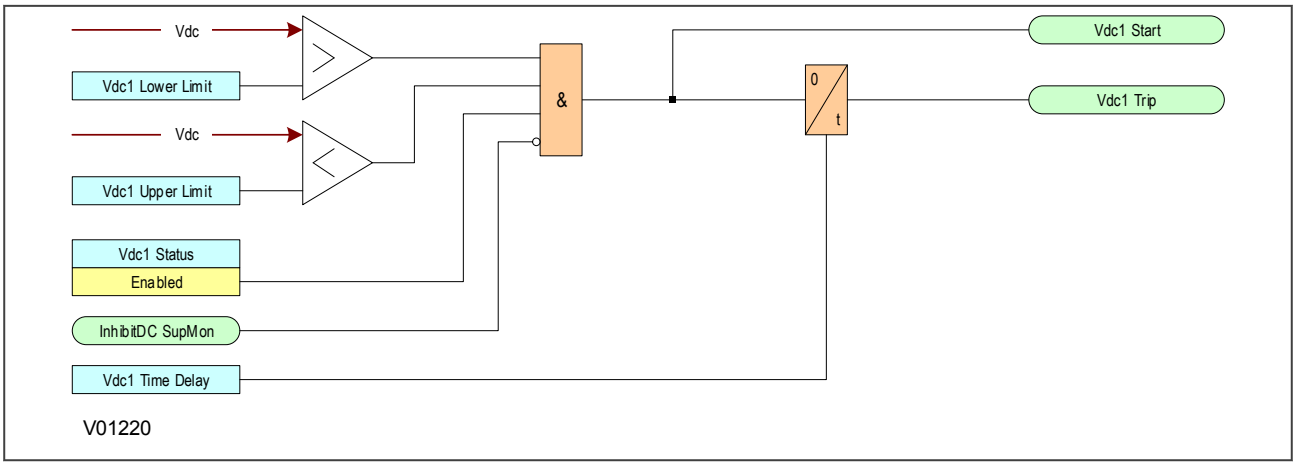


Figure 174: DC Supply Monitor logic

The diagram above shows the DC supply monitoring logic for stage 1 only. Stages 2 and 3 are identical in principle.

The logic function will work when the ***Vdc1 status*** setting cell is `Enabled` and the DC Supply Monitoring inhibit signal (***InhibitDC SupMon***) is low.

If the auxiliary supply voltage (Vdc) exceeds the lower limit AND falls below the upper limit, the voltage is in the healthy zone and a Start signal is generated.

The Vdc(n) Trip signals from all stages are OR'd together to produce an alarm signal ***DC Supply Fail***.

Note:
The device's supercapacitor uses Vdc to provide charge and so may cause the voltage to dip below the Vdc lower limit (19.2 V) during a system power-up sequence if fully discharged. This will trigger a lockout error. In this case, it will be necessary to allow the supercapacitor to charge before attempting another power-up sequence. The supercapacitor may take several minutes to become fully charged, depending on the AC/DC supply specification. With the supercapacitor charged, the next relay power cycle will clear the lockout and the relay will boot and operate normally.

3 VOLTAGE TRANSFORMER SUPERVISION

The Voltage Transformer Supervision (VTS) function is used to detect failure of the AC voltage inputs to the protection. This may be caused by voltage transformer faults, overloading, or faults on the wiring, which usually results in one or more of the voltage transformer fuses blowing.

If there is a failure of the AC voltage input, the IED could misinterpret this as a failure of the actual phase voltages on the power system, which could result in unnecessary tripping of a circuit breaker.

The VTS logic is designed to prevent such a situation by detecting voltage input failures, which are NOT caused by power system phase voltage failure, and automatically blocking associated voltage dependent protection elements. A time-delayed alarm output is available to warn of a VTS condition.

The following scenarios are possible with respect to the failure of the VT inputs.

- Loss of one or two-phase voltages
- Loss of all three-phase voltages under load conditions
- Absence of three-phase voltages upon line energisation

3.1 LOSS OF ONE OR TWO PHASE VOLTAGES

If the power system voltages are healthy, no Negative Phase Sequence (NPS) current will be present. If however, one or two of the AC voltage inputs are missing, there will be Negative Phase Sequence voltage present, even if the actual power system phase voltages are healthy. VTS works by detecting Negative Phase Sequence (NPS) voltage without the presence of Negative Phase Sequence current. So if there is NPS voltage present, but no NPS current, it is certain that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

3.2 LOSS OF ALL THREE PHASE VOLTAGES

If all three voltage inputs are lost, there will be no Negative Phase Sequence quantities present, but the device will see that there is no voltage input. If this is caused by a power system failure, there will be a step change in the phase currents. However, if this is not caused by a power system failure, there will be no change in any of the phase currents. So if there is no measured voltage on any of the three phases and there is no change in any of the phase currents, this indicates that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation.

3.3 ABSENCE OF ALL THREE PHASE VOLTAGES ON LINE ENERGISATION

On line energization there should be a change in the phase currents as a result of loading or line charging current. Under this condition we need an alternative method of detecting three-phase VT failure.

If there is no measured voltage on all three phases during line energization, two conditions might apply:

- A three-phase VT failure
- A close-up three-phase fault.

The first condition would require VTS to block the voltage-dependent functions.

In the second condition, voltage dependent functions should not be blocked, as tripping is required.

To differentiate between these two conditions overcurrent level detectors are used (***VTS I> Inhibit*** and ***VTS I2> Inhibit***). These prevent a VTS block from being issued in case of a genuine fault. These elements should be set in excess of any non-fault based currents on line energisation (load, line charging current, transformer inrush current if applicable), but below the level of current produced by a close-up three-phase fault.

If the line is closed where a three-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

3.4 VTS IMPLEMENTATION

VTS is implemented in the *SUPERVISION* column of the relevant settings group.

The following settings are relevant for VT Supervision:

- ***VTS Status***: determines whether the VTS Operate output will be a blocking output or an alarm indication only
- ***VTS PickupThresh***: determines the threshold at which the phase voltage detectors pick up
- ***VTS Reset Mode***: determines whether the Reset is to be manual or automatic
- ***VTS Time delay***: determines the operating time delay
- ***VTS I> Inhibit***: inhibits VTS operation in the case of a phase overcurrent fault
- ***VTS I2> Inhibit***: inhibits VTS operation in the case of a negative sequence overcurrent fault

VTS is only enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions.

3.5 VTS LOGIC

This logic will only be enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions (i.e. where no voltage will be present and the ***VTS I> Inhibit*** overcurrent element will not be picked up).

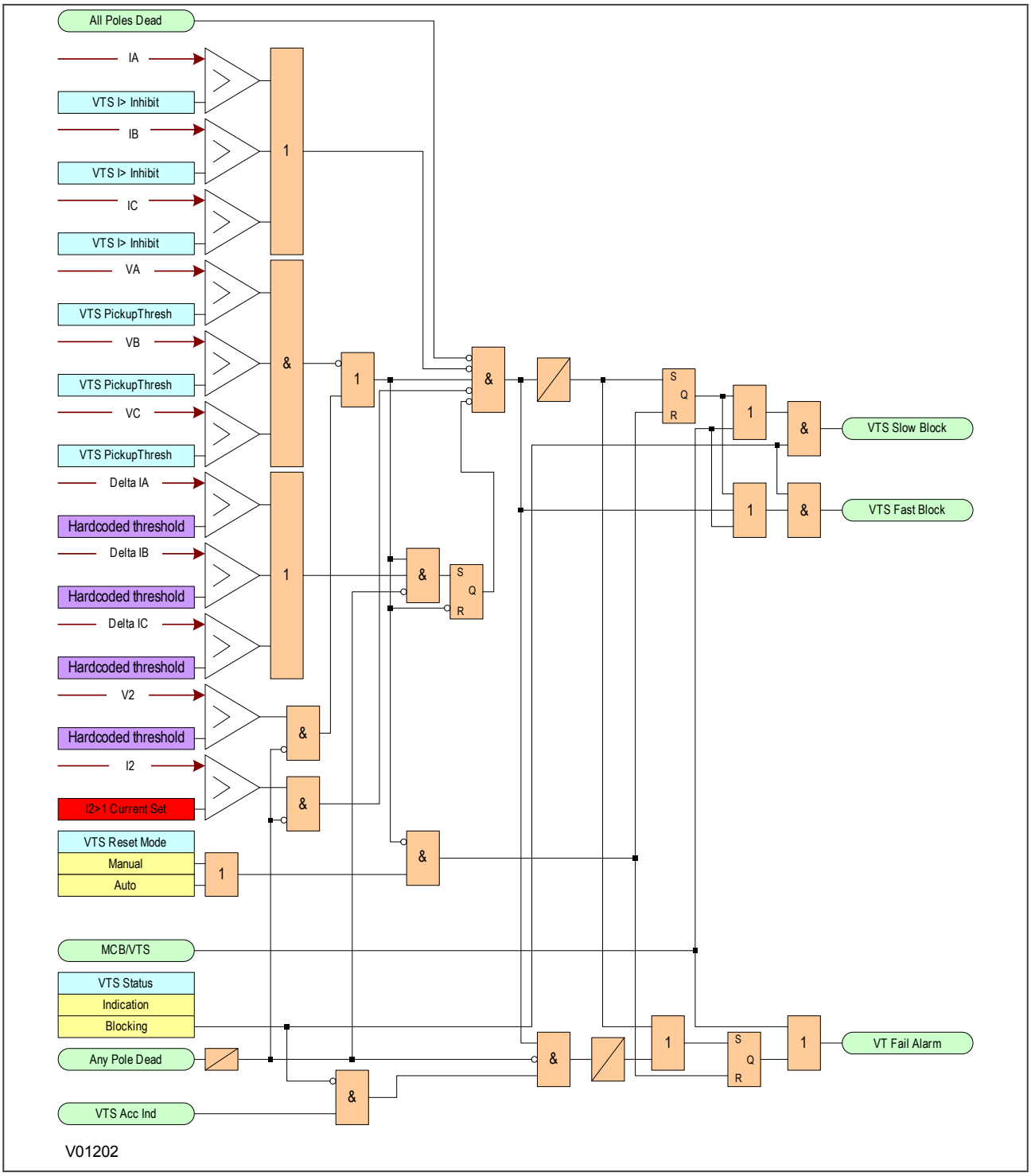


Figure 175: VTS logic

As can be seen from the diagram, the VTS function is inhibited if:

- An ***All Poles Dead*** DDB signal is present
- Any phase overcurrent condition exists
- A Negative Phase Sequence current exists
- If the phase current changes over the period of 1 cycle

3.6 VTS ACCELERATION INDICATION LOGIC

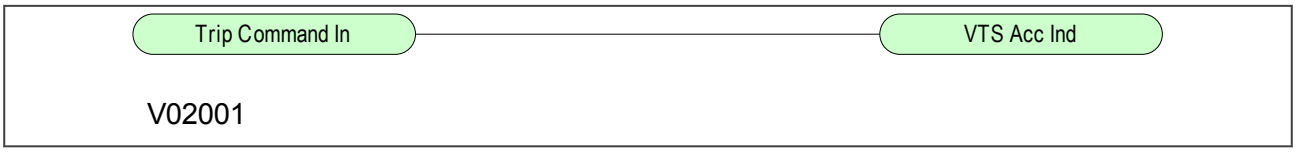


Figure 176: VTS Acceleration Indication Logic

4 CURRENT TRANSFORMER SUPERVISION

The Current Transformer Supervision function (CTS) is used to detect failure of the AC current inputs to the protection. This may be caused by internal current transformer faults, overloading, or faults on the wiring. If there is a failure of the AC current input, the protection could misinterpret this as a failure of the actual phase currents on the power system, which could result in maloperation. Also, an open circuit in the AC current circuits can cause dangerous CT secondary voltages to be generated.

4.1 CTS IMPLEMENTATION

If the power system currents are healthy, no zero sequence voltage are derived. However, if one or more of the AC current inputs are missing, a zero sequence current would be derived, even if the actual power system phase currents are healthy. Standard CTS works by detecting a derived zero sequence current where there is no corresponding derived zero sequence voltage.

The voltage transformer connection used must be able to refer zero sequence voltages from the primary to the secondary side. Therefore, this element should only be enabled where the VT is of a five-limb construction, or comprises three single-phase units with the primary star point earthed.

The CTS function is implemented in the *SUPERVISION* column of the relevant settings group, under the sub-heading *CT SUPERVISION*.

The following settings are relevant for CT Supervision:

- ***CTS Status***: to disable or enable CTS
- ***CTS VN< Inhibit***: inhibits CTS if the zero sequence voltage exceeds this setting
- ***CTS IN> Set***: determines the level of zero sequence current
- ***CTS Time Delay***: determines the operating time delay

4.2 CTS LOGIC

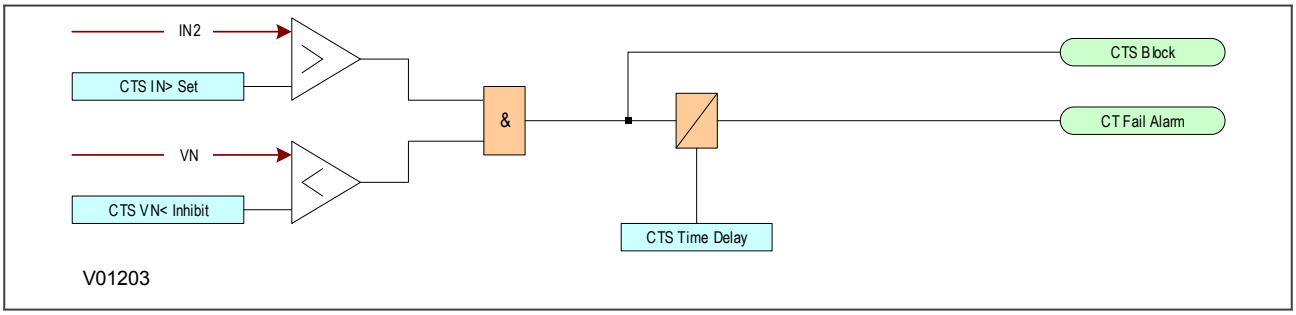


Figure 177: CTS logic diagram

If the derived earth fault current (zero sequence current) exceeds the threshold set by ***CTS IN> Set***, a CTS block DDB signal is produced, provided it is not inhibited. the signal is inhibited if the residual voltage is less than the threshold set by ***CTS VN< Inhibit***. A CTS alarm is generated after a short time delay defined by the setting ***CTS Time Delay***.

4.3 APPLICATION NOTES

4.3.1 SETTING GUIDELINES

The residual voltage setting, ***CTS VN< Inhibit*** and the residual current setting, ***CTS IN> Set***, should be set to avoid unwanted operation during healthy system conditions. For example:

- ***CTS VN< Inhibit*** should be set to 120% of the maximum steady state residual voltage.
- ***CTS IN> Set*** will typically be set below minimum load current.
- ***CTS Time Delay*** is generally set to 5 seconds.

Where the magnitude of residual voltage during an earth fault is unpredictable, the element can be disabled to prevent protection elements being blocked during fault conditions.

5 TRIP CIRCUIT SUPERVISION

In most protection schemes, the trip circuit extends beyond the IED enclosure and passes through components such as links, relay contacts, auxiliary switches and other terminal boards. Such complex arrangements may require dedicated schemes for their supervision.

There are two distinctly separate parts to the trip circuit; the trip path, and the trip coil. The trip path is the path between the IED enclosure and the CB cubicle. This path contains ancillary components such as cables, fuses and connectors. A break in this path is possible, so it is desirable to supervise this trip path and to raise an alarm if a break should appear in this path.

The trip coil itself is also part of the overall trip circuit, and it is also possible for the trip coil to develop an open-circuit fault.

This product supports a number of trip circuit supervision (TCS) schemes.

5.1 TRIP CIRCUIT SUPERVISION SCHEME 1

This scheme provides supervision of the trip coil with the CB open or closed, however, it does not provide supervision of the trip path whilst the breaker is open. The CB status can be monitored when a self-reset trip contact is used. However, this scheme is incompatible with latched trip contacts, as a latched contact will short out the opto-input for a time exceeding the recommended Delayed Drop-off (DDO) timer setting of 400 ms, and therefore does not support CB status monitoring. If you require CB status monitoring, further opto-inputs must be used.

Note:
A 52a CB auxiliary contact follows the CB position. A 52b auxiliary contact is the opposite.

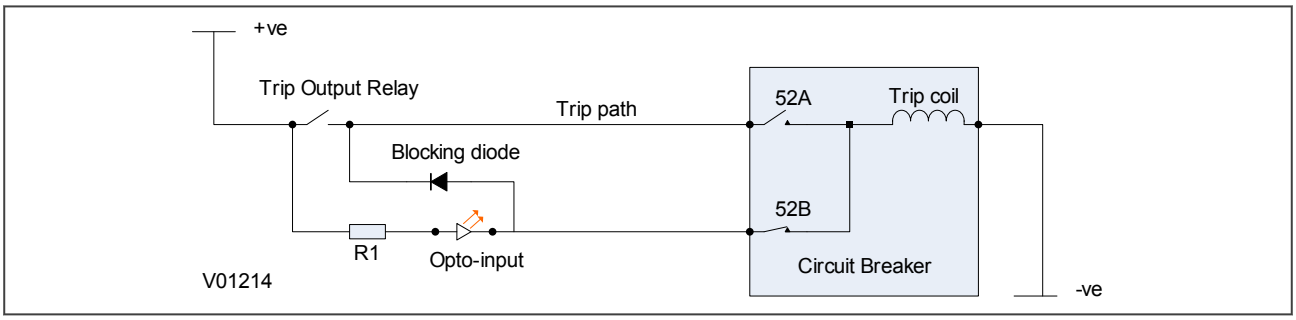


Figure 178: TCS Scheme 1

When the CB is closed, supervision current passes through the opto-input, blocking diode and trip coil. When the CB is open, supervision current flows through the opto-input and into the trip coil via the 52b auxiliary contact. This means that *Trip Coil* supervision is provided when the CB is either closed or open, however *Trip Path* supervision is only provided when the CB is closed. No supervision of the trip path is provided whilst the CB is open (pre-closing supervision). Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

5.1.1 RESISTOR VALUES

The supervision current is a lot less than the current required by the trip coil to trip a CB. The TCS opto-input limits this supervision current to less than 10 mA. If the TCS opto-input were to be short-circuited however, it could be possible for the supervision current to reach a level that could trip the CB. For this reason, a resistor R1 is often used to limit the current in the event of a short-circuited TCS opto-input. This limits the current to less than 60 mA. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Resistor R1
24/27	620 Ohms at 2 Watts

Trip Circuit Voltage	Resistor R1
30/34	820 Ohms at 2 Watts
48/54	1.2 kOhms at 5 Watts
110/125	2.7 kOhms at 10 Watts
220/250	5.2 kOhms at 15 Watts

Warning:
If your IED has Opto Mode settings available in the *OPTO CONFIG* column, these MUST be set to *TCS* for any corresponding Opto Inputs(s) used for Trip Circuit Supervision.

5.1.2 PSL FOR TCS SCHEME 1

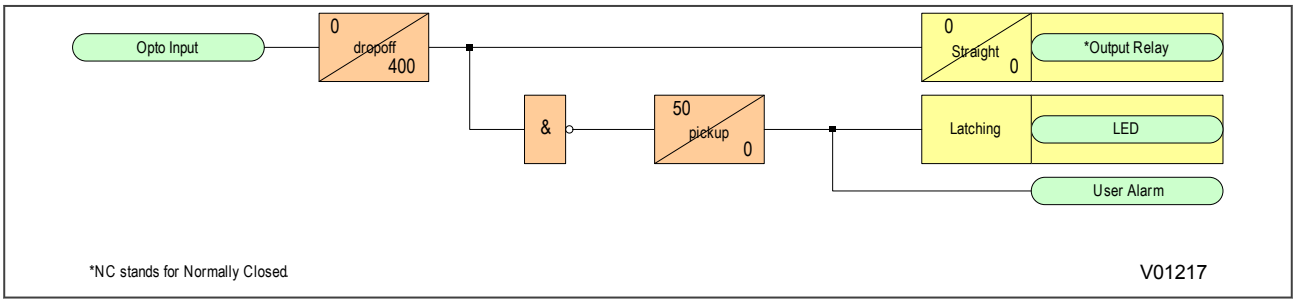


Figure 179: PSL for TCS Scheme 1

The opto-input can be used to drive a Normally Closed Output Relay, which in turn can be used to drive alarm equipment. The signal can also be inverted to drive a latching programmable LED and a user alarm DDB signal.

The DDO timer operates as soon as the opto-input is energised, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto-input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the power up time, following a voltage supply interruption.

5.2 TRIP CIRCUIT SUPERVISION SCHEME 2

This scheme provides supervision of the trip coil with the breaker open or closed but does not provide pre-closing supervision of the trip path. However, using two opto-inputs allows the IED to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This is achieved by assigning one opto-input to the 52a contact and another opto-input to the 52b contact. Provided the ***CB Status*** setting in the *CB CONTROL* column is set to `Both 52A and 52B`, the IED will correctly monitor the status of the breaker. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

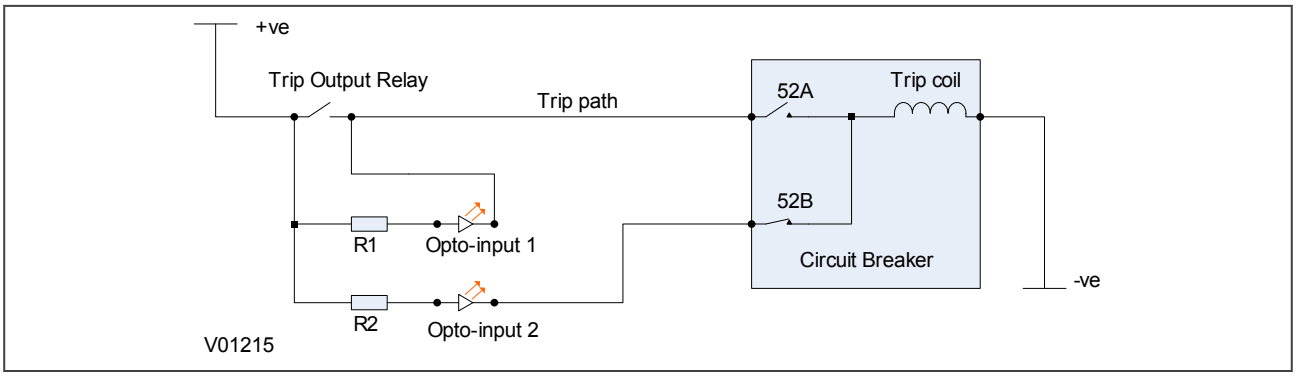


Figure 180: TCS Scheme 2

When the breaker is closed, supervision current passes through opto input 1 and the trip coil. When the breaker is open current flows through opto input 2 and the trip coil. No supervision of the trip path is provided whilst the breaker is open. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

5.2.1 RESISTOR VALUES

As with scheme 1, optional resistors R1 and R2 can be added to prevent tripping of the CB if either TCS opto-input is shorted. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Resistor R1 and R2
24/27	620 Ohms at 2 Watts
30/34	820 Ohms at 2 Watts
48/54	1.2 kOhms at 5 Watts
110/125	2.7 kOhms at 10 Watts
220/250	5.2 kOhms at 15 Watts

Warning:
If your IED has Opto Mode settings available in the *OPTO CONFIG* column, these MUST be set to *TCS* for any corresponding Opto Inputs(s) used for Trip Circuit Supervision.

5.2.2 PSL FOR TCS SCHEME 2

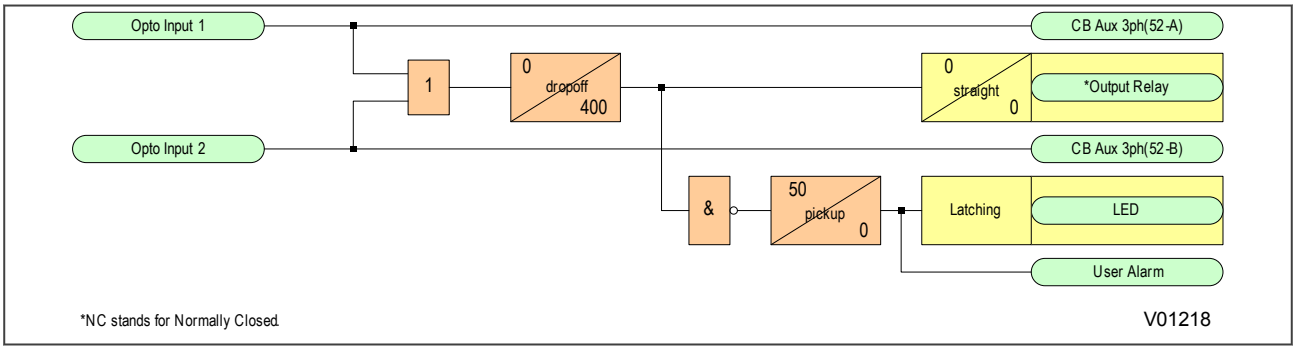


Figure 181: PSL for TCS Scheme 2

In TCS scheme 2, both opto-inputs must be low before a trip circuit fail alarm is given.

5.3 TRIP CIRCUIT SUPERVISION SCHEME 3

TCS Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed. It provides pre-closing supervision of the trip path. Since only one opto-input is used, this scheme is not compatible with latched trip contacts. If you require CB status monitoring, further opto-inputs must be used.

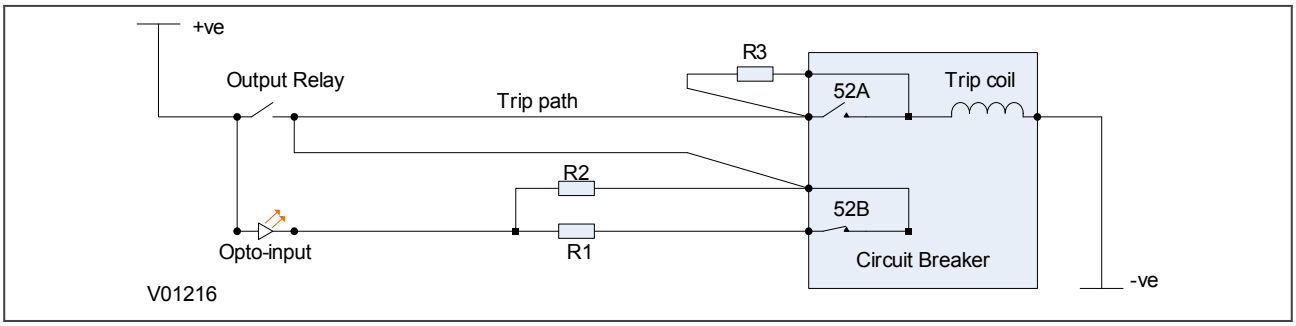


Figure 182: TCS Scheme 3

When the CB is closed, supervision current passes through the opto-input, resistor R2 and the trip coil. When the CB is open, current flows through the opto-input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. The supervision current is maintained through the trip path with the breaker in either state, therefore providing pre-closing supervision.

5.3.1 RESISTOR VALUES

As with TCS schemes 1 and 2, resistors R1 and R2 are used to prevent false tripping, if the TCS opto-input is accidentally shorted. However, unlike the other two schemes, this scheme is dependent on the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Trip Circuit Voltage	Resistor R1 and R2	Resistor R3
24/27	620 Ohms at 2 Watts	330 Ohms at 5 Watts
30/34	820 Ohms at 2 Watts	430 Ohms at 5 Watts
48/54	1.2 kOhms at 5 Watts	620 Ohms at 10 Watts
110/125	2.7 kOhms at 10 Watts	1.5 k Ohms at 15 Watts
220/250	5.2 kOhms at 15 Watts	2.7 k Ohms at 25 Watts

Warning:
If your IED has Opto Mode settings available in the *OPTO CONFIG* column, these MUST be set to *TCS* for any corresponding Opto Inputs(s) used for Trip Circuit Supervision.

5.3.2 PSL FOR TCS SCHEME 3

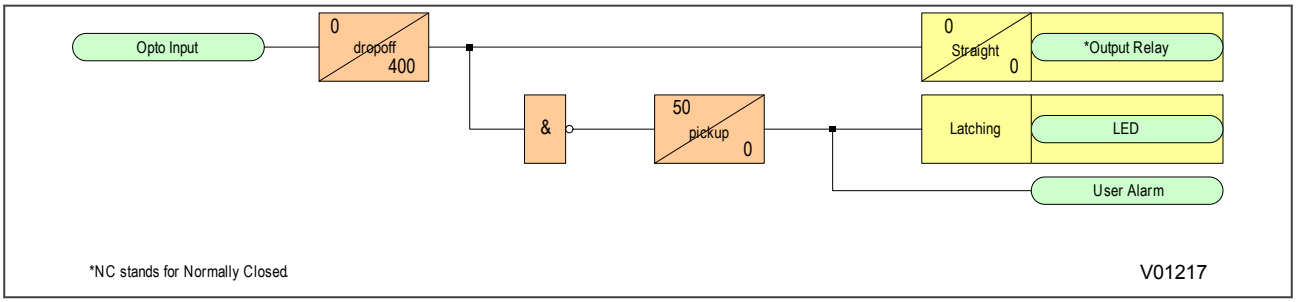


Figure 183: PSL for TCS Scheme 3

5.4 TRIP CIRCUIT SUPERVISION SCHEME 4

Scheme 4 is identical to that offered by MVAX31 (a Trip Circuit Supervision relay) and consequently is fully compliant with ENA Specification H7. To achieve this compliance, there are eight settings in the *OPTO CONFIG* column. Two of these settings (***Opto 1 Mode*** to ***Opto 11 Mode***--dependant on I/O option chosen) must be set to `TCS` before the scheme can be used, with any remaining opto-input set to `Normal` as required.

In the diagram below, Opto-input 1 and Opto-input 2 would correlate to one of the above-mentioned opto-inputs.

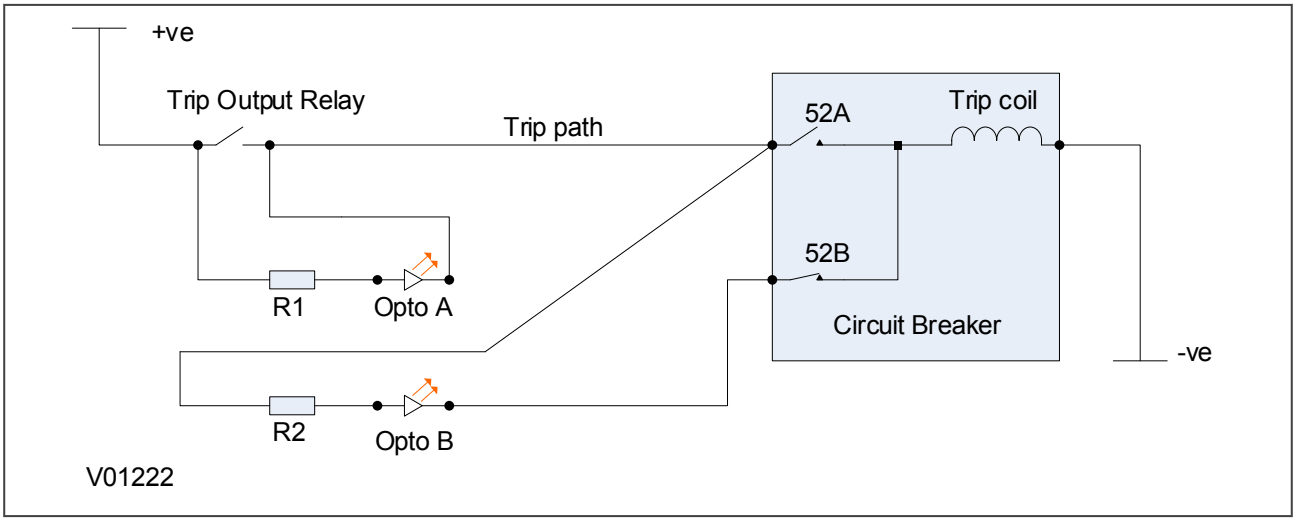


Figure 184: TCS Scheme 4

Under normal non-fault conditions, a current of 2 mA flows through one of the following paths:

a) Post Close Supervision: When the CB is in a closed state, the current flows through R1, Opto A, Contact 52A and the trip coil.

b) Pre-close Supervision: When the CB is in an open state, the current flows through R1, Opto A, Contact 52B, Opto B and the trip coil.

c) Momentary Tripping with Self-reset Contact: When a self-reset trip contact is in a closed state, the current flows through the trip contact, contact 52A and the trip coil.

d) Tripping with Latched Contact: When a latched trip contact is used and when it is in a closed state, the current flows through the trip contact, Contact 52A, the trip coil, then changing to the path trip contact, R2, Contact 52B, Opto B and the trip coil.

A current of 2 mA through the Trip Coil is insufficient to cause operation of the Trip Contact, but large enough to energise the opto-inputs. Under this condition both of the opto-inputs will output logic 1, so the output relay (TCS health) will be closed and the User Alarm will be off. If a break occurs in the trip circuit, the current ceases to flow, resulting in both opto-inputs outputting logic 0. This will open the output relay and energise the user alarm.

Recommended Scheme Opto Connections and Settings

I/O option G or J		I/O Option F			I/O Option C		
Opto Input 1 (Mode Setting)	Opto Input 2 (Mode Setting)	Opto Input 4 (Mode Setting)	Opto Input 5 (Mode Setting)	Opto Input 6 (Mode Setting)	Opto Input 9 (Mode Setting)	Opto Input 10 (Mode Setting)	Opto Input 11 (Mode Setting)
Opto A (TCS)	Opto B (TCS)	Opto A (TCS)	Opto B (TCS)	- (NORMAL)	Opto A (TCS)	Opto B (TCS)	- (NORMAL)
					I/O Option H		

5.4.1 RESISTOR VALUES

The TCS opto-inputs sink a constant current of 2 mA.The values of external resistors R1 and R2 are chosen to limit the current to a maximum of 60 mA in the event that a TCS opto-input becomes shorted. The values of these resistors depend on the trip circuit voltage.

Trip Circuit Voltage	Resistor R1 and R2 (ohms)
24/27	620 Ohms at 2 Watts
30/34	820 Ohms at 2 Watts
48/54	1.2 kOhms at 5 Watts
110/125	2.7 kOhms at 10 Watts
220/250	5.2 kOhms at 15 Watts

For the momentary tripping condition, none of the opto-inputs are energised. To tide over this normal CB operation, a dropoff time delay of about 400 ms is added in the PSL.

Warning:
If your IED has Opto Mode settings available in the *OPTO CONFIG* column, these MUST be set to *TCS* for any corresponding Opto Inputs(s) used for Trip Circuit Supervision.

5.4.2 PSL FOR TCS SCHEME 4

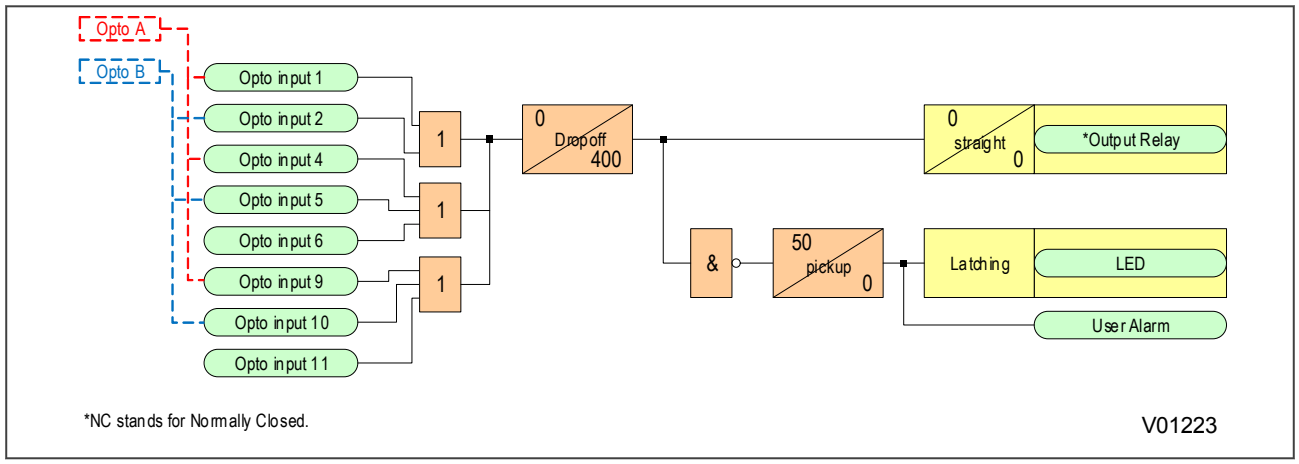


Figure 185: PSL for TCS Scheme 4

CHAPTER 16

DIGITAL I/O AND PSL CONFIGURATION

1 CHAPTER OVERVIEW

This chapter introduces the PSL (Programmable Scheme Logic) Editor, and describes the configuration of the digital inputs and outputs. It provides an outline of scheme logic concepts and the PSL Editor. This is followed by details about allocation of the digital inputs and outputs, which require the use of the PSL Editor. A separate "Settings Application Software" document is available that gives a comprehensive description of the PSL, but enough information is provided in this chapter to allow you to allocate the principal digital inputs and outputs.

This chapter contains the following sections:

2 CONFIGURING DIGITAL INPUTS AND OUTPUTS

Configuration of the digital inputs and outputs in this product is very flexible. You can use a combination of settings and programmable logic to customise them to your application. You can access some of the settings using the keypad on the front panel, but you will need a computer running the settings application software to fully interrogate and configure the properties of the digital inputs and outputs.

The settings application software includes an application called the PSL Editor (Programmable Scheme Logic Editor). The PSL Editor lets you allocate inputs and outputs according to your specific application. It also allows you to apply attributes to some of the signals such as a drop-off delay for an output contact.

In this product, digital inputs and outputs that are configurable are:

- Optically isolated digital inputs (opto-inputs). These can be used to monitor the status of associated plant.
- Output relays. These can be used for purposes such as initiating the tripping of circuit breakers, providing alarm signals, etc..
- Programmable LEDs. The number and colour of the programmable LEDs varies according to the particular product being applied.
- Function keys and associated LED indications. These are not provided on all products, but where they are, each function key has an associated tri-colour LED.
- IEC 61850 GOOSE inputs and outputs. These are only provided on products that have been specified for connection to an IEC61850 system, and the details of the GOOSE are presented in the documentation on IEC61850.

3 SCHEME LOGIC

The product is supplied with pre-loaded Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL).

The Scheme Logic is a functional module within the IED, through which all mapping of inputs to outputs is handled. The scheme logic can be split into two parts; the Fixed Scheme Logic (FSL) and the Programmable Scheme Logic (PSL). It is built around a concept called the digital data bus (DDB). The DDB encompasses all of the digital signals (DDBs) which are used in the FSL and PSL. The DDBs included digital inputs, outputs, and internal signals.

The FSL is logic that has been hard-coded in the product. It is fundamental to correct interaction between various protection and/or control elements. It is fixed and cannot be changed.

The PSL gives you a facility to develop custom schemes to suit your application if the factory-programmed default PSL schemes do not meet your needs. Default PSL schemes are programmed before the product leaves the factory. These default PSL schemes have been designed to suit typical applications and if these schemes suit your requirements, you do not need to take any action. However, if you want to change the input-output mappings, or to implement custom scheme logic, you can change these, or create new PSL schemes using the PSL editor.

The PSL consists of components such as logic gates and timers, which combine and condition DDB signals.

The logic gates can be programmed to perform a range of different logic functions. The number of inputs to a logic gate are not limited. The timers can be used either to create a programmable delay or to condition the logic outputs. Output contacts and programmable LEDs have dedicated conditioners.

The PSL logic is event driven. Only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This minimises the amount of processing time used by the PSL ensuring industry leading performance.

The following diagram shows how the scheme logic interacts with the rest of the IED.

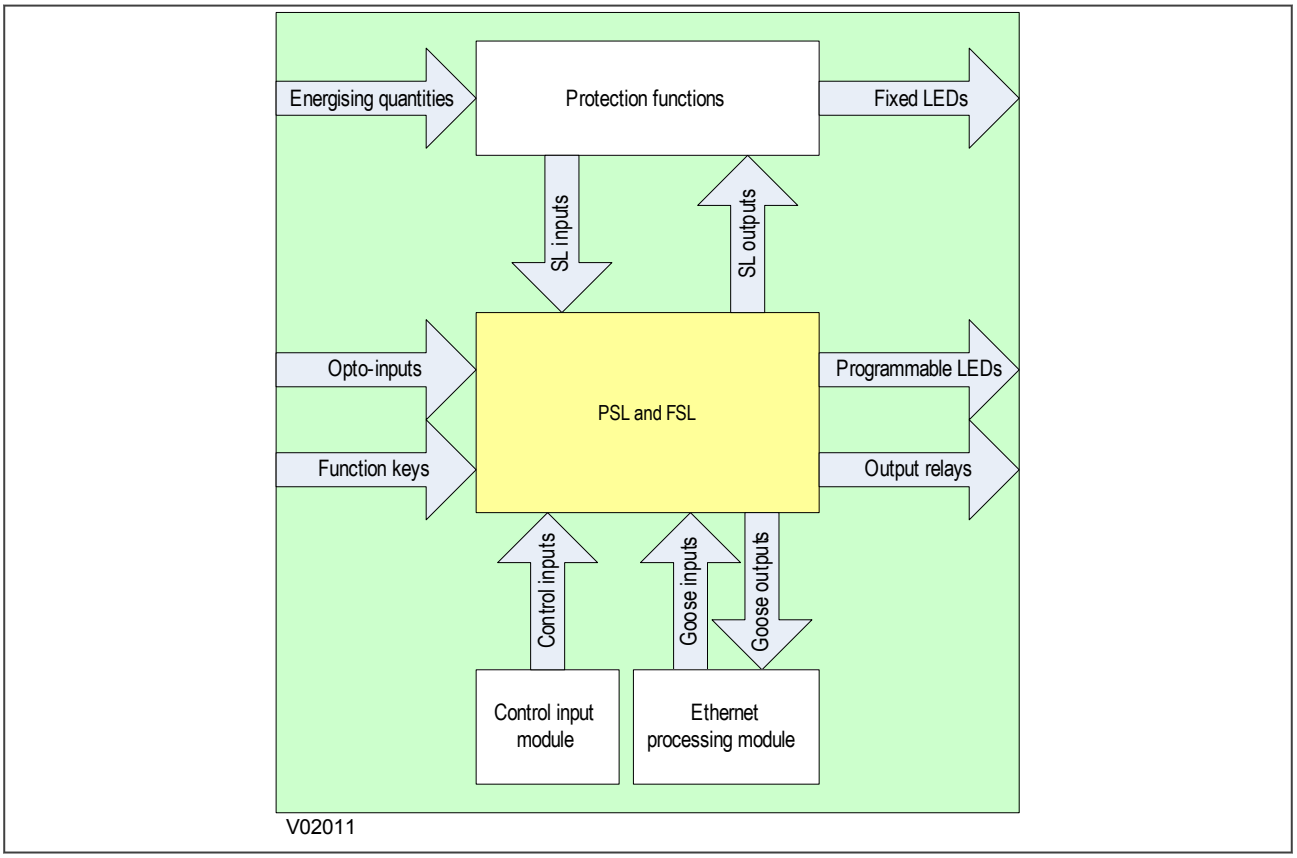


Figure 186: Scheme Logic Interfaces

3.1 PSL EDITOR

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised logic to qualify how the product manages its response to system conditions. The IED's digital inputs are combined with internally generated digital signals using logic gates, timers, and conditioners. The resultant signals are then mapped to digital outputs signals including output relays and LEDs.

The PSL Editor is a tool in the settings application software that allows you to create and edit scheme logic diagrams. You can use the default scheme logic which has been designed to suit most applications, but if it does not suit your application you can change it. If you create a different scheme logic with the software, you need to upload it to the device to apply it.

3.2 PSL SCHEMES

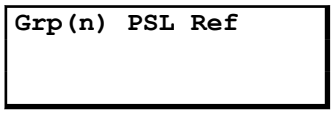
Your product is shipped with default scheme files. These can be used without modification for most applications, or you can choose to use them as a starting point to design your own scheme. You can also create a new scheme from scratch. To create a new scheme, or to modify an existing scheme, you will need to launch the settings application software. You then need to open an existing PSL file, or create a new one, for the particular product that you are using, and then open a PSL file. If you want to create a new PSL file, you should select **File** then **New** then **Blank scheme...** This action opens a default file appropriate for the device in question, but deletes the diagram components from the default file to leave an empty diagram with configuration information loaded. To open an existing file, or a default file, simply double-click on it.

3.3 PSL SCHEME VERSION CONTROL

To help you keep track of the PSL loaded into products, a version control feature is included. The user interface contains a *PSL DATA* column, which can be used to track PSL modifications. A total of 12 cells are contained in the *PSL DATA* column; 3 for each setting group.

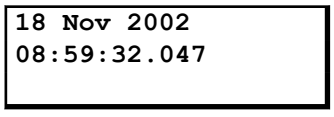
Grp(n) PSL Ref: When downloading a PSL scheme to an IED, you will be prompted to enter the relevant group number and a reference identifier. The first 32 characters of the reference identifier are displayed in this cell. The horizontal cursor keys can scroll through the 32 characters as the LCD display only displays 16 characters.

Example:



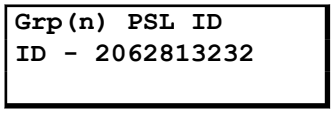
Date/time: This cell displays the date and time when the PSL scheme was downloaded to the IED.

Example:



Grp(n) PSL ID: This cell displays a unique ID number for the downloaded PSL scheme.

Example:



4 CONFIGURING THE OPTO-INPUTS

The number of optically isolated status inputs (opto-inputs) depends on the specific model supplied. The use of the inputs will depend on the application, and their allocation is defined in the programmable scheme logic (PSL). In addition to the PSL assignment, you also need to specify the expected input voltage. Generally, all opto-inputs will share the same input voltage range, but if different voltage ranges are being used, this device can accommodate them.

In the *OPTO CONFIG* column there is a global nominal voltage setting. If all opto-inputs are going to be energised from the same voltage range, you select the appropriate value with this setting. If you select `Custom` in the setting, then the cells ***Opto Input 1***, ***Opto Input 2***, etc. become visible. You use these cells to set the voltage ranges for each individual opto-input.

If you are using the recommended settings application software (MiCOM S1 Agile), the product's DC supply monitoring function detects the DC supply voltage and provides some automation for setting for the global nominal voltage. This feature is found by right clicking on **Device**, then selecting **Supervise Device → Auto-setup of Opto Voltage**. This automatic detection only works for DC inputs.

Within the *OPTO CONFIG* column there are also settings to control the filtering applied to the inputs, as well as the pick-up/drop-off characteristic.

The filter control setting provides a bit string with a bit associated with all opto-inputs. Setting the bit to '1' means that a half-cycle filter is applied to the inputs. This helps to prevent incorrect operation in the event of power system frequency interference on the wiring. Setting the field to '0' removes the filter and provides for faster operation. You should note that removing the filter reduces the AC immunity. that means it is less effective at filtering out-of-band interference.

The ***Characteristic*** setting is a single setting that applies to all the opto-inputs. It is used to set the pick-up/drop-off ratios of the input signals.

By default the drop-off is 60% of the maximum DC input value and the pick-up threshold is 80% of the minimum DC input value. You can change this to other available thresholds if required. Other available thresholds are 50% - 70% and 58% - 75%.

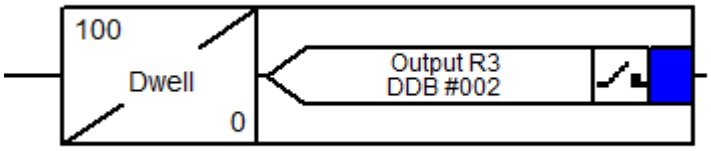
5 ASSIGNING THE OUTPUT RELAYS

Relay contact action is controlled using the PSL. DDB signals are mapped in the PSL and drive the output relays. The driving of an output relay is controlled by means of a relay output conditioner. Several choices are available for how output relay contacts are conditioned. For example, you can choose whether operation of an output relay contact is latched, has delay on pick-up, or has a delay on drop-off. You make this choice in the **Contact Properties** window associated with the output relay conditioner.

To map an output relay in the PSL you should use the Contact Conditioner button in the toolbar to import it. You then condition it according to your needs. The output of the conditioner respects the attributes you have assigned.

The toolbar button for a Contact Conditioner looks like this:

The PSL contribution that it delivers looks like this:



Note:
Contact Conditioners are only available if they have not all been used. In some default PSL schemes, all Contact Conditioners might have been used. If that is the case, and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the relay outputs. The button looks like this:

This is the "Contact Signal" button. It allows you to put replica instances of a conditioned output relay into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

6 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

6.1 TRIP LED LOGIC

When a trip occurs, the trip LED is illuminated. It is possible to reset this with a number of ways:

- Directly with a reset command (by pressing the Clear Key)
- With a reset logic input
- With self-resetting logic

You enable the automatic self-resetting with the ***Sys Fn Links*** cell in the *SYSTEM DATA* column. A '0' disables self resetting and a '1' enables self resetting.

The reset occurs when the circuit is reclosed and the ***Any Pole Dead*** signal has been reset for three seconds providing the ***Any Start*** signal is inactive. The reset is prevented if the ***Any Start*** signal is active after the breaker closes.

The Trip LED logic is as follows:

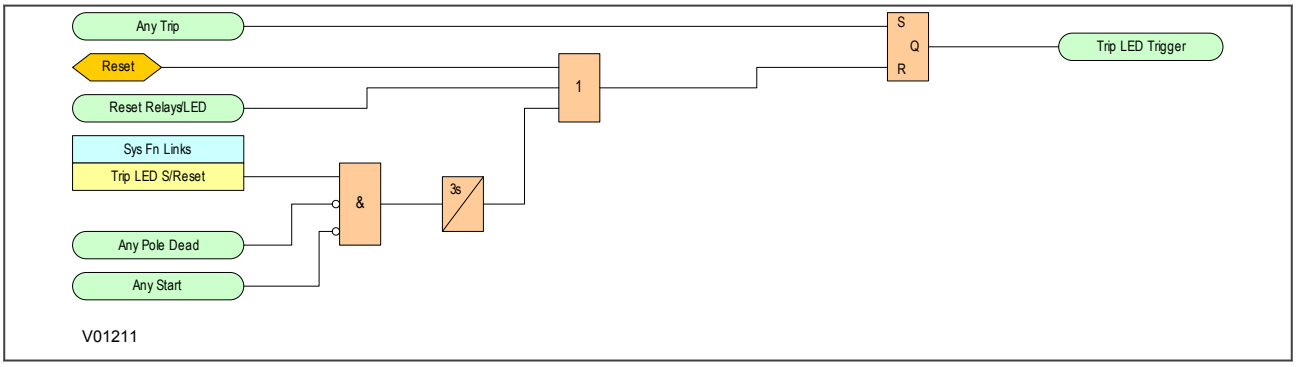


Figure 187: Trip LED logic

7 CONFIGURING PROGRAMMABLE LEDS

There are three types of programmable LED signals which vary according to the model being used. These are:

- Single-colour programmable LED. These are red when illuminated.
- Tri-colour programmable LED. These can be illuminated red, green, or amber.
- Tri-colour programmable LED associated with a Function Key. These can be illuminated red, green, or amber.

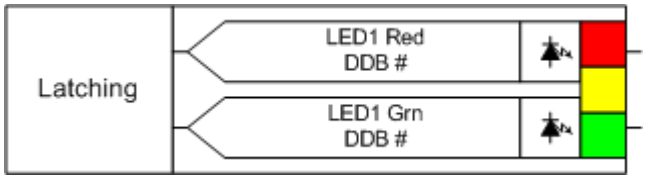
DDB signals are mapped in the PSL and used to illuminate the LEDs. For single-coloured programmable LEDs there is one DDB signal per LED. For tri-coloured LEDs there are two DDB signals associated with the LED. Asserting ***LED # Grn*** will illuminate the LED green. Asserting ***LED # Red*** will illuminate the LED red. Asserting both DDB signals will illuminate the LED amber.

The illumination of an LED is controlled by means of a conditioner. Using the conditioner, you can decide whether the LEDs reflect the real-time state of the DDB signals, or whether illumination is latched pending user intervention.

To map an LED in the PSL you should use the LED Conditioner button in the toolbar to import it. You then condition it according to your needs. The output(s) of the conditioner respect the attribute you have assigned.

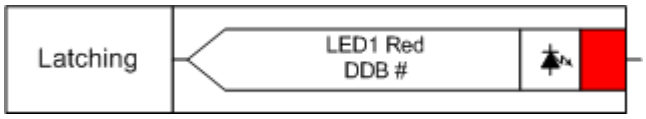
The toolbar button for a tri-colour LED looks like this:

The PSL contribution that it delivers looks like this:



The toolbar button for a single-colour LED looks like this:

The PSL contribution that it delivers looks like this.



Note:
LED Conditioners are only available if they have not all been used up, and in some default PSL schemes they might be. If that is the case and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the LEDs. For a tri-coloured LED the button looks like this:

For a single-colour LED it looks like this:

It is the "LED Signal" button. It allows you to put replica instances of a conditioned LED into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

Note:
All LED DDB signals are always shown in the PSL Editor. However, the actual number of LEDs depends on the device hardware. For example, if a small 20TE device has only 4 programmable LEDs, LEDs 5-8 will not take effect even if they are mapped in the PSL.

8 FUNCTION KEYS

For most models, a number of programmable function keys are available. This allows you to assign function keys to control functionality via the programmable scheme logic (PSL). Each function key is associated with a programmable tri-colour LED, which you can program to give the desired indication on activation of the function key.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are found in the *FUNCTION KEYS* column.

Each function key is associated with a DDB signal as shown in the DDB table. You can map these DDB signals to any function available in the PSL.

The ***Fn Key Status*** cell displays the status (energised or de-energised) of the function keys by means of a binary string, where each bit represents a function key starting with bit 0 for function key 1.

Each function key has three settings associated with it, as shown:

- ***Fn Key (n)***, which enables or disables the function key
- ***Fn Key (n) Mode***, which allows you to configure the key as toggled or normal
- ***Fn Key (n) label***, which allows you to define the function key text that is displayed

The ***Fn Key (n)*** cell is used to enable (unlock) or disable (unlock) the function key signals in PSL. The Lock setting has been provided to prevent further activation on subsequent key presses. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

When the ***Fn Key (n) Mode*** cell is set to `Toggle`, the function key DDB signal output will remain in the set state until a reset command is given. In the `Normal` mode, the function key DDB signal will remain energised for as long as the function key is pressed and will then reset automatically. In this mode, a minimum pulse duration can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The ***Fn Key Label*** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of all function keys are recorded in non-volatile memory. In case of auxiliary supply interruption their status will be maintained.

> *Note:*
> *All function key DDB signals are always shown in the PSL Editor. However, the actual number of function keys depends on the device hardware. For example, if a small 20TE device has no function keys, the function key DDBs mapped in the PSL will not take effect.*

9 CONTROL INPUTS

The control inputs are software switches, which can be set or reset locally or remotely. These inputs can be used to trigger any PSL function to which they are connected. There are three setting columns associated with the control inputs: *CONTROL INPUTS*, *CTRL I/P CONFIG* and *CTRL I/P LABELS*. These are listed in the Settings and Records appendix at the end of this manual.

10 INTER-PSL INPUTS AND OUTPUTS

To make the design of PSL schemes easier, P40 Agile provides a range of DDB signals for conncting PSL Inputs to PSL Outputs. these are called Inter-PSL inputs and outputs. This facility allows you to map many PSL input signals to a single Inter-PSL output signal, many PSL output signals to a single Inter-PSL input signal, and to join the Inter-PSL input signal to an Inter-PSL output signal. The Inter-PSL input signals can also be used to directly trigger the Disturbance Recorder.

CHAPTER 17

COMMUNICATIONS

1 CHAPTER OVERVIEW

This product supports Substation Automation System (SAS), and Supervisory Control and Data Acquisition (SCADA) communication. The support embraces the evolution of communications technologies that have taken place since microprocessor technologies were introduced into protection, control, and monitoring devices which are now ubiquitously known as Intelligent Electronic Devices for the substation (IEDs).

As standard, all products support rugged serial communications for SCADA and SAS applications. By option, any product can support Ethernet communications for more advanced SCADA and SAS applications.

This chapter contains the following sections:

2 COMMUNICATION INTERFACES

The MiCOM P40 Agile products have a number of standard and optional communication interfaces. The standard and optional hardware and protocols are summarised below:

Port	Availability	Physical Layer	Use	Data Protocols
Front	Standard	USB	Local settings Firmware download	Courier
Rear serial port 1	Standard	RS485 / K-Bus	SCADA Remote settings IRIG-B	Courier, MODBUS, IEC 60870-5-103, DNP3.0
Rear serial port 2 (order option)	Optional	RS485	SCADA Remote settings IRIG-B	Courier
Rear Ethernet port	Optional	Ethernet/copper	SCADA Remote settings	Courier, DNP3.0 over Ethernet, IEC 61850 (order option)
Rear Ethernet port	Optional	Ethernet/fibre	SCADA Remote settings	Courier or DNP3.0 over Ethernet (order option)

Note:
Optional communication boards are always fitted into slot C and only slot C.
It is only possible to fit one optional communications board, therefore Serial and Ethernet communications are mutually exclusive.

3 SERIAL COMMUNICATION

The physical layer standards that are used for serial communications for SCADA purposes are:

- Universal Serial Bus (USB)
- EIA(RS)485 (often abbreviated to RS485)
- K-Bus (a proprietary customization of RS485)

USB is a relatively new standard, which replaces EIA(RS232) for local communication with the IED (for transferring settings and downloading firmware updates)

RS485 is similar to RS232 but for longer distances and it allows daisy-chaining and multi-dropping of IEDs.

K-Bus is a proprietary protocol quite similar to RS485, but it cannot be mixed on the same link as RS485. Unlike RS485, K-Bus signals applied across two terminals are not polarised.

It is important to note that these are not data protocols. They only describe the physical characteristics required for two devices to communicate with each other.

For a description of the K-Bus standard see K-Bus (on page378) and General Electric's K-Bus interface guide reference R6509.

A full description of the RS485 is available in the published standard.

3.1 UNIVERSAL SERIAL BUS

The USB port is used for connecting computers locally for the purposes of transferring settings, measurements and records to/from the computer to the IED and to download firmware updates from a local computer to the IED.

3.2 EIA(RS)485 BUS

The RS485 two-wire connection provides a half-duplex, fully isolated serial connection to the IED. The connection is polarized but there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

The RS485 bus must be terminated at each end with 120 Ω 0.5 W terminating resistors between the signal wires.

The RS485 standard requires that each device be directly connected to the actual bus. Stubs and tees are forbidden. Loop bus and Star topologies are not part of the RS485 standard and are also forbidden.

Two-core screened twisted pair cable should be used. The final cable specification is dependent on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. The total cable length must not exceed 1000 m. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The RS485 signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product's chassis. This is for both safety and noise reasons.

It may be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master is waiting in receive mode, in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequently not responding. Symptoms of this are; poor response times (due to retries), increasing message error counts, erratic communications, and in the worst case, complete failure to communicate.

3.2.1 EIA(RS)485 BIASING REQUIREMENTS

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean to prevent noise being injected.

Note:
Some devices may be able to provide the bus bias, in which case external components would not be required.

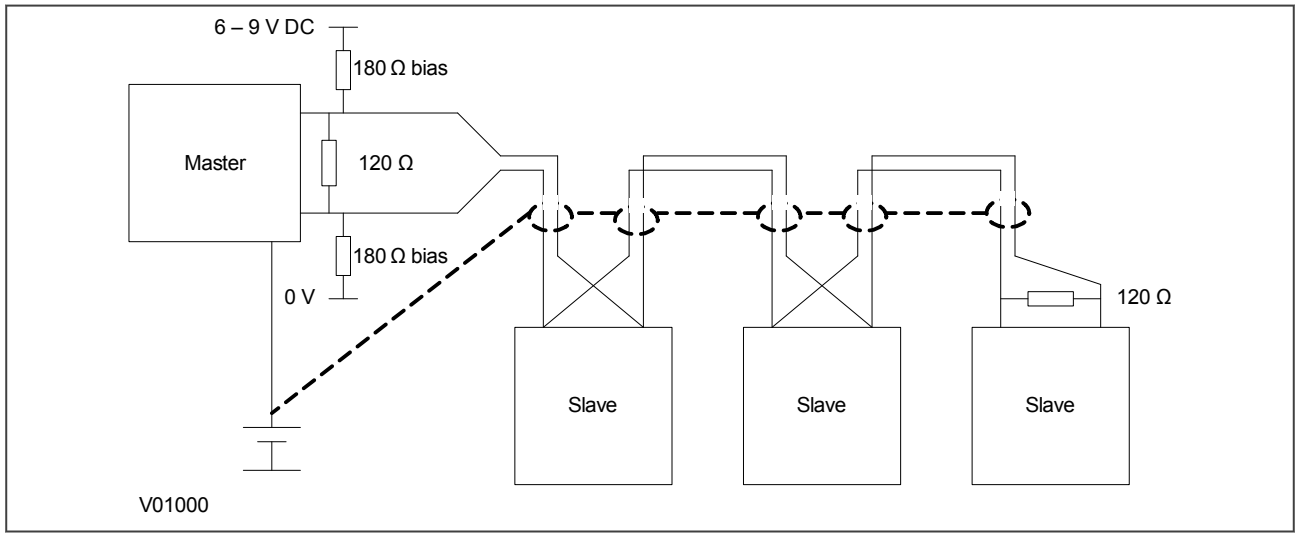


Figure 188: RS485 biasing circuit

Warning:
It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.

3.3 K-BUS

K-Bus is a robust signalling method based on RS485 voltage levels. K-Bus incorporates message framing, based on a 64 kbps synchronous HDLC protocol with FM0 modulation to increase speed and security.

The rear interface is used to provide a permanent connection for K-Bus, which allows multi-drop connection.

A K-Bus spur consists of up to 32 IEDs connected together in a multi-drop arrangement using twisted pair wiring. The K-Bus twisted pair connection is non-polarised.

It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. A protocol converter, namely the KITZ101, KITZ102 or KITZ201, must be used for this purpose. Please consult General Electric for information regarding the specification and supply of KITZ devices. The following figure demonstrates a typical K-Bus connection.

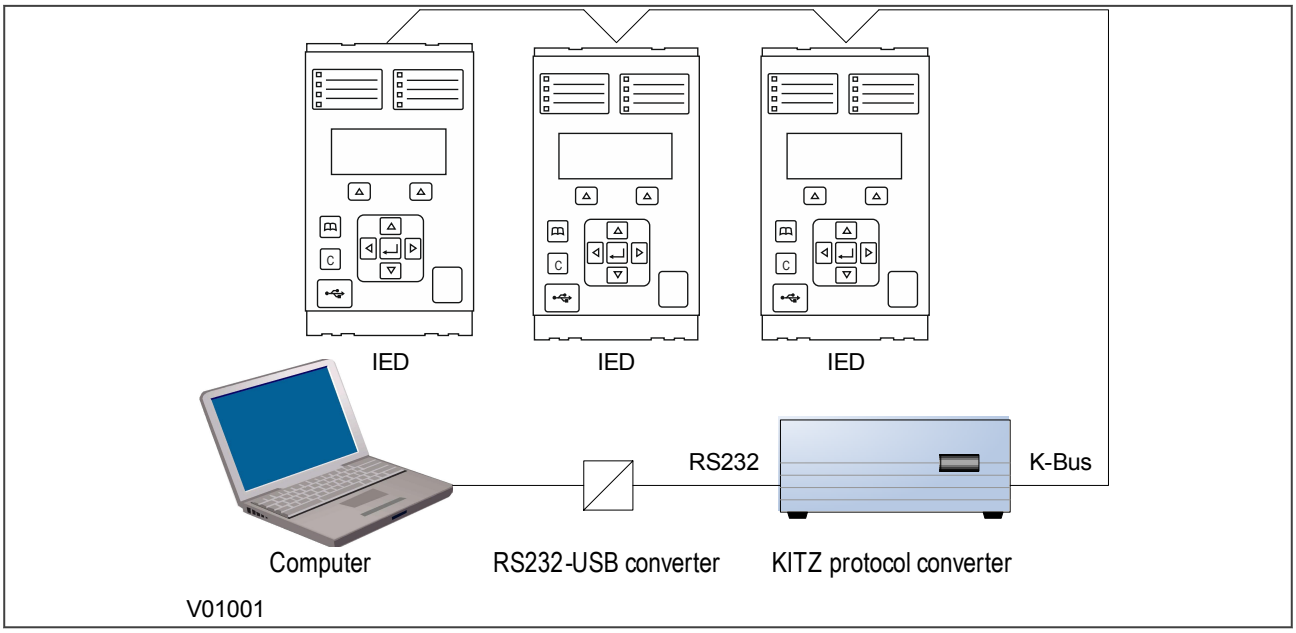


Figure 189: Remote communication using K-Bus

Note:
An RS232-USB converter is only needed if the local computer does not provide an RS232 port.

Further information about K-Bus is available in the publication R6509: K-Bus Interface Guide, which is available on request.

4 STANDARD ETHERNET COMMUNICATION

The Ethernet interface is required for either IEC 61850 and/or DNP3 over Ethernet (protocol must be selected at time of order). With either of these protocols, the Ethernet interface also offers communication with MiCOM S1 for remote configuration and record extraction.

Fibre optic connection is recommended for use in permanent connections in a substation environment, as it offers advantages in terms of noise rejection. The fibre optic port provides 100 Mbps communication and uses type LC connectors.

The device can also be connected to either a 10Base-T or a 100Base-TX Ethernet hub or switch using the RJ45 port. The port automatically senses which type of hub is connected. Due to noise and interference reasons, this connection type is only recommended for short-term connections over a short distance.

The pins on the RJ45connector are as follows:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

5 REDUNDANT ETHERNET COMMUNICATION

Redundancy is required where a single point of failure cannot be tolerated. It is required in critical applications such as substation automation. Redundancy acts as an insurance policy, providing an alternative route if one route fails.

Ethernet communication redundancy is available for most General Electric products, using a Redundant Ethernet facility. This is an in-built Network Interface Card (NIC), which incorporates an integrated Ethernet switch. The interface provides two Ethernet transmitter/receiver pairs, both of which are for the same physical medium (two copper, or two fibre). In addition to the two Ethernet transmitter/receiver pairs, the REB provides link activity indication.

Both industry standard PRP (Parallel Redundancy Protocol) and HSR (High-availability Seamless Redundancy) protocols are available by ordering option.

5.1 SUPPORTED PROTOCOLS

One of the key requirements of substation redundant communications is "bumpless" redundancy. This means the ability to transfer from one communication path to another without noticeable consequences. Standard protocols of the time could not meet the demanding requirements of network availability for substation automation solutions. Switch-over times were unacceptably long. For this reason, companies developed proprietary protocols. More recently, however, standard protocols, which support bumpless redundancy (namely PRP and HSR) have been developed and ratified.

P40Agile version 56 onwards supports redundant Ethernet. Variants for each of the following protocols are available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)

PRP and HSR are open standards, so their implementation is compatible with any standard PRP or HSR device respectively. PRP provides "bumpless" redundancy.

Note:
The protocol you require must be selected at the time of ordering.

5.2 PARALLEL REDUNDANCY PROTOCOL

PRP (Parallel Reundancy Protocol) is defined in IEC 62439-3. PRP provides bumpless redundancy and meets the most demanding needs of substation automation. The PRP implementation of the REB is compatible with any standard PRP device.

PRP uses two independent Ethernet networks operating in parallel. PRP systems are designed so that there should be no common point of failure between the two networks, so the networks have independent power sources and are not connected together directly.

Devices designed for PRP applications have two ports attached to two separate networks and are called Doubly Attached Nodes (DAN). A DAN has two ports, one MAC address and one IP address.

The sending node replicates each frame and transmits them over both networks. The receiving node processes the frame that arrives first and discards the duplicate. Therefore there is no distinction between the working and backup path. The receiving node checks that all frames arrive in sequence and that frames are correctly received on both ports.

Devices such as printers that have a single Ethernet port can be connected to either of the networks but will not directly benefit from the PRP principles. Such devices are called Singly Attached Nodes (SAN). For devices with a single Ethernet port that need to connect to both LANs, this can be achieved by employing Ethernet Redundancy

Boxes (sometimes abbreviated to RedBox). Devices with a single Ethernet port that connect to both LANs by means of a RedBox are known as Virtual DAN (VDAN).

The figure below summarises DAN, SAN, VDAN, LAN, and RedBox connectivity.

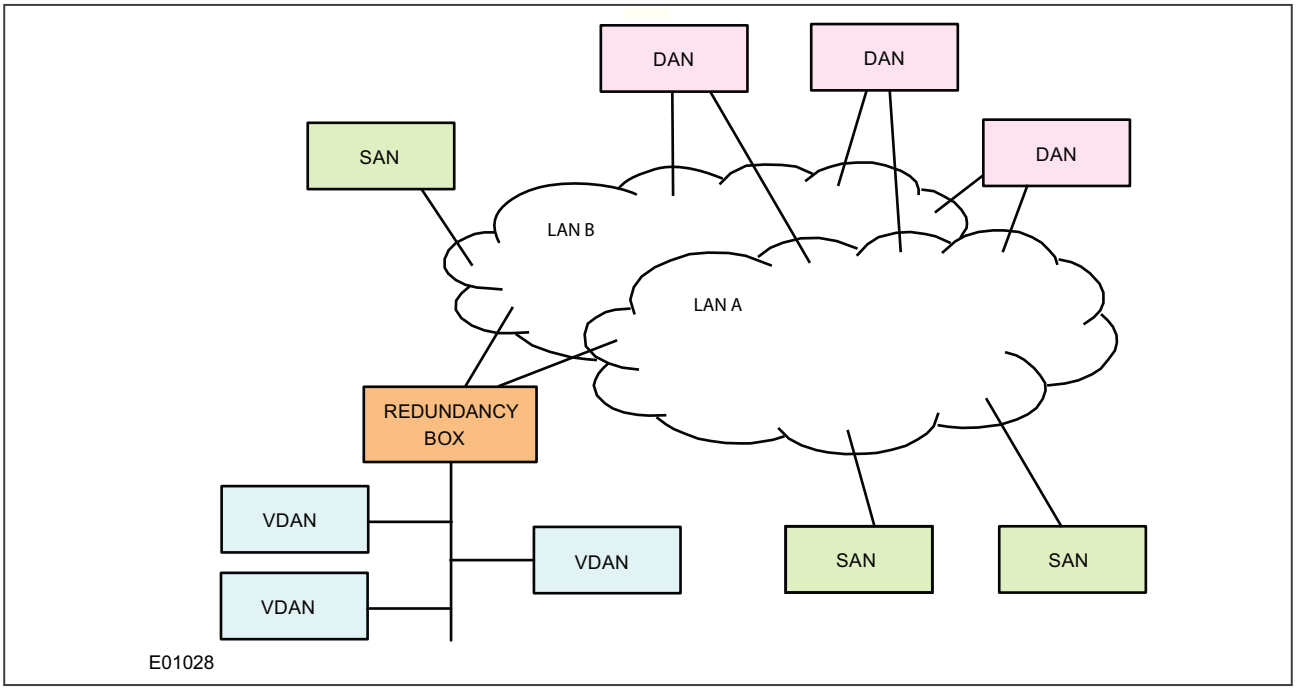


Figure 190: IED attached to separate LANs

In a DAN, both ports share the same MAC address so it does not affect the way devices talk to each other in an Ethernet network (Address Resolution Protocol at layer 2). Every data frame is seen by both ports.

When a DAN sends a frame of data, the frame is duplicated on both ports and therefore on both LAN segments. This provides a redundant path for the data frame if one of the segments fails. Under normal conditions, both LAN segments are working and each port receives identical frames.

5.3 HIGH-AVAILABILITY SEAMLESS REDUNDANCY (HSR)

HSR is standardized in IEC 62439-3 (clause 5) for use in ring topology networks. Similar to PRP, HSR provides bumpless redundancy and meets the most demanding needs of substation automation. HSR has become the reference standard for ring-topology networks in the substation environment. The HSR implementation of the redundancy Ethernet board (REB) is compatible with any standard HSR device.

HSR works on the premise that each device connected in the ring is a doubly attached node running HSR (referred to as DANH). Similar to PRP, singly attached nodes such as printers are connected via Ethernet Redundancy Boxes (RedBox).

5.3.1 HSR MULTICAST TOPOLOGY

When a DANH is sending a multicast frame, the frame (C frame) is duplicated (A frame and B frame), and each duplicate frame A/B is tagged with the destination MAC address and the sequence number. The frames A and B differ only in their sequence number, which is used to identify one frame from the other. Each frame is sent to the network via a separate port. The destination DANH receives two identical frames, removes the HSR tag of the first frame received and passes this (frame D) on for processing. The other duplicate frame is discarded. The nodes forward frames from one port to the other unless it was the node that injected it into the ring.

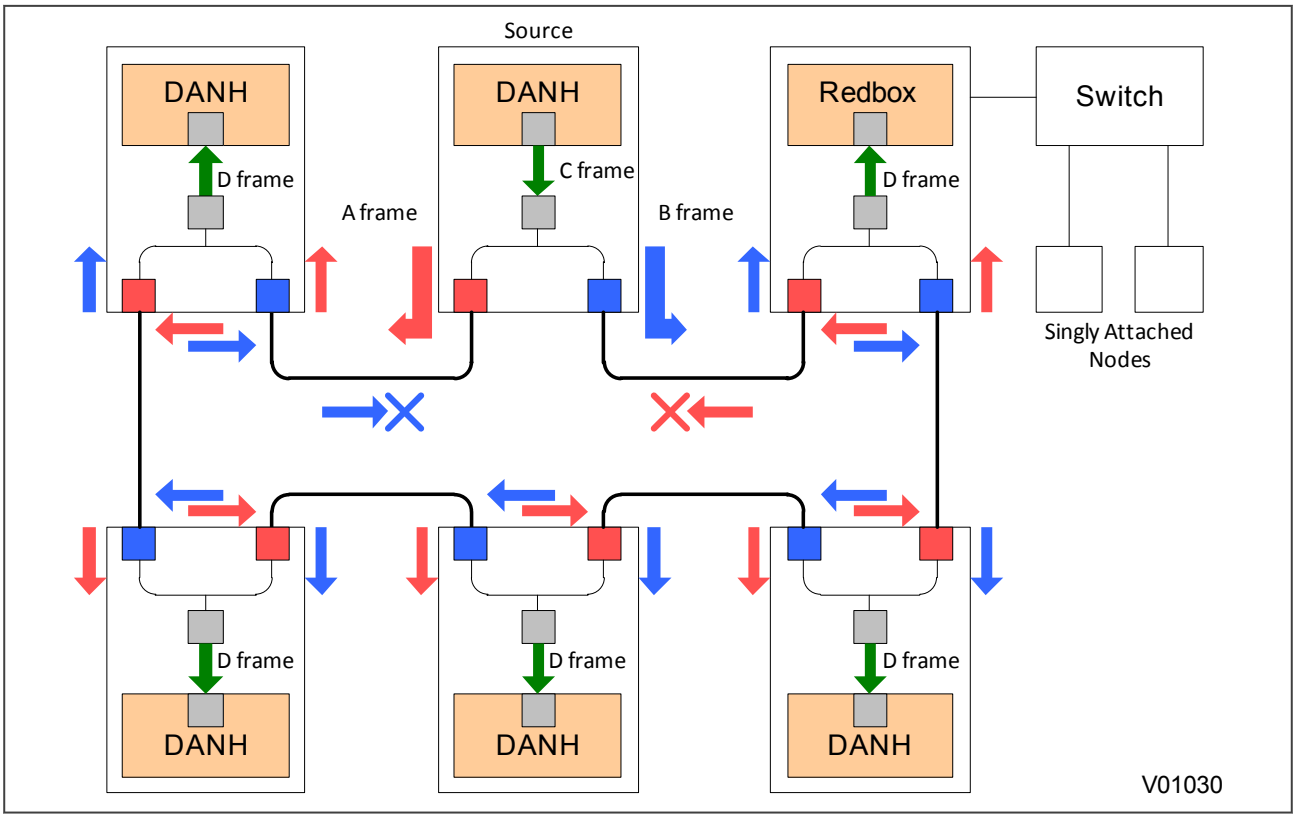


Figure 191: HSR multicast topology

Only about half of the network bandwidth is available in HSR for multicast or broadcast frames because both duplicate frames A & B circulate the full ring.

5.3.2 HSR UNICAST TOPOLOGY

With unicast frames, there is just one destination and the frames are sent to that destination alone. All non-recipient devices simply pass the frames on. They do not process them in any way. In other words, D frames are produced only for the receiving DANH. This is illustrated below.

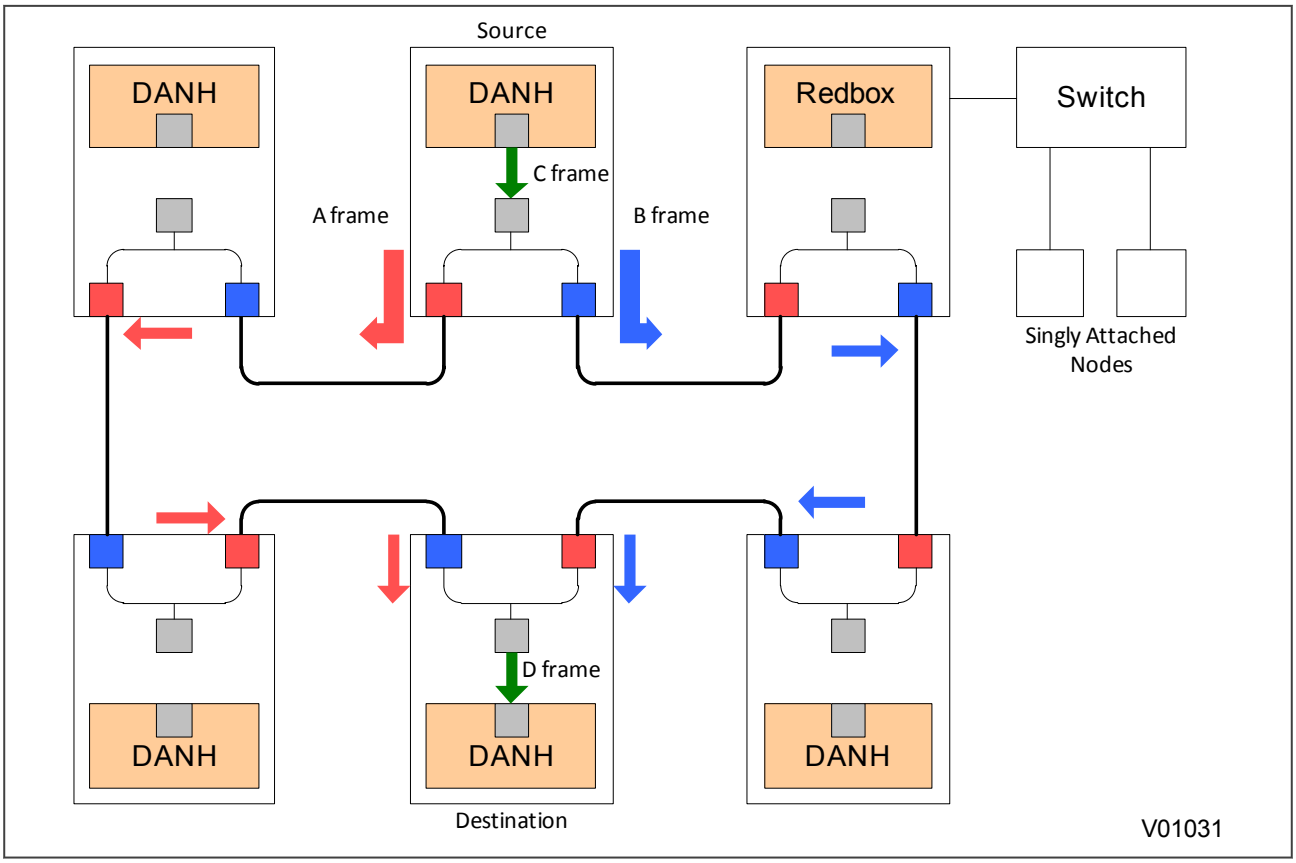


Figure 192: HSR unicast topology

For unicast frames, the whole bandwidth is available as both frames A & B stop at the destination node.

5.3.3 HSR APPLICATION IN THE SUBSTATION

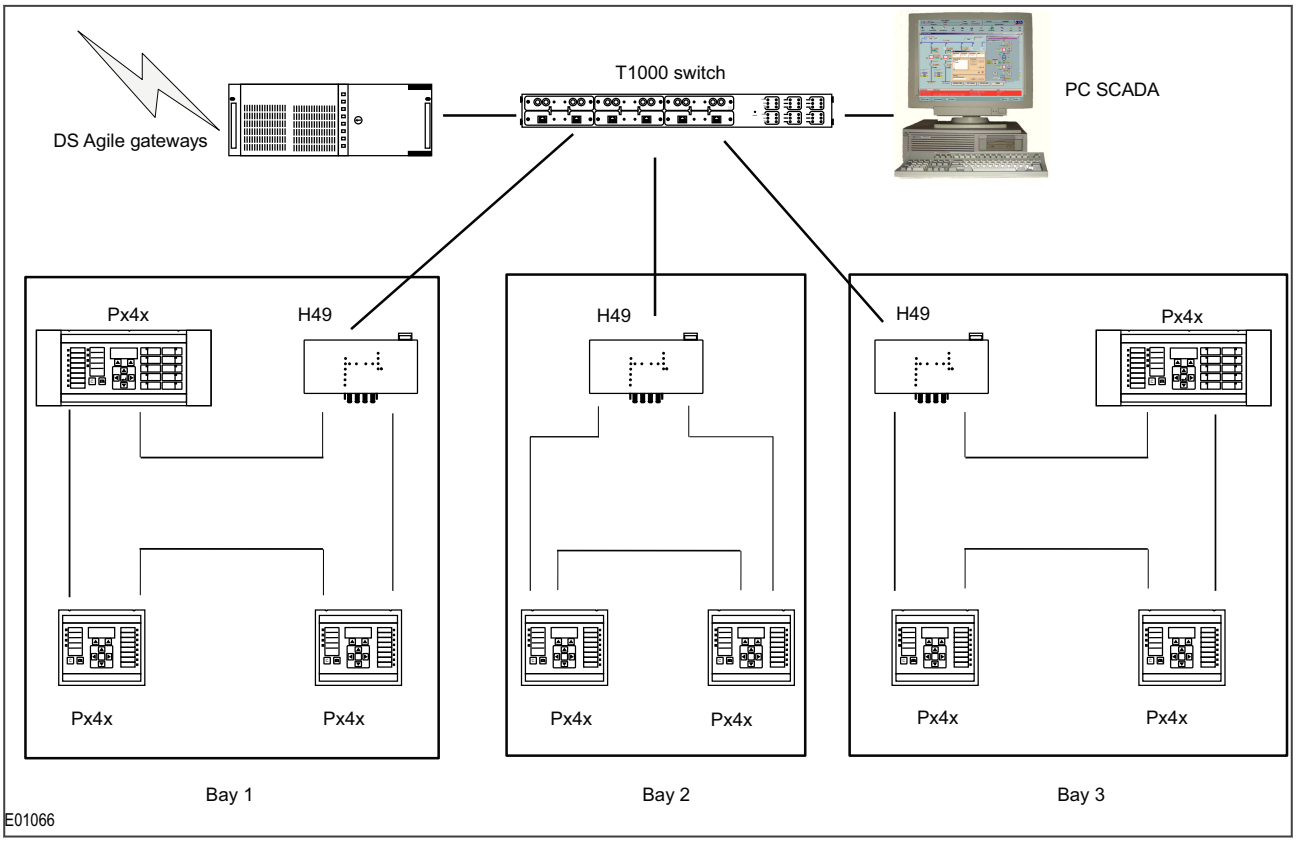


Figure 193: HSR application in the substation

5.4 RAPID SPANNING TREE PROTOCOL

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path. It stops network loops whilst enabling redundancy. It can be used in star or ring connections as shown in the following figure.

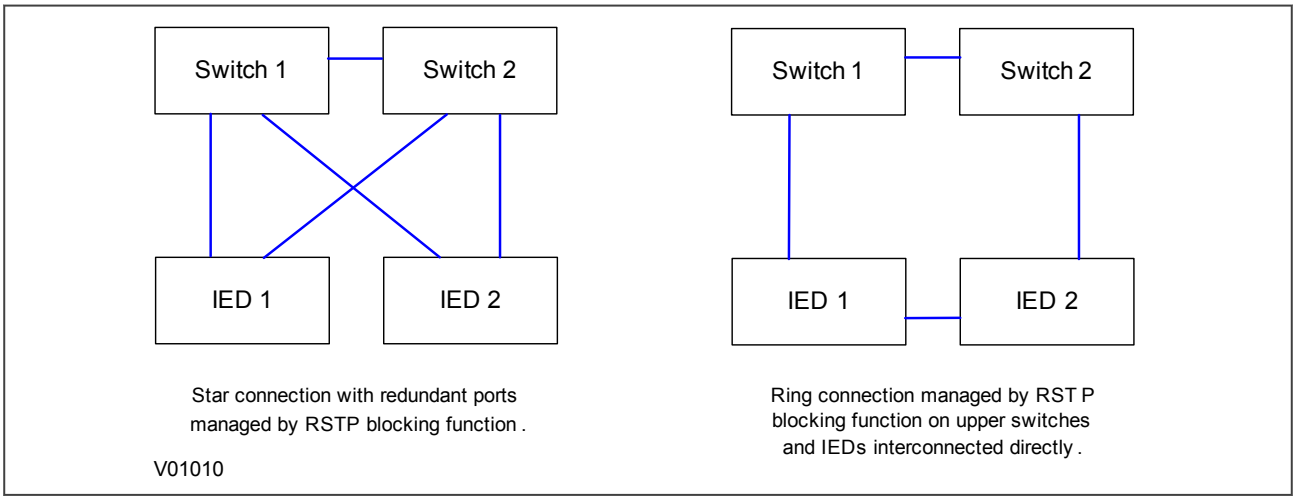


Figure 194: IED attached to redundant Ethernet star or ring circuit

The RSTP implementation in this product is compatible with any devices that use RSTP.

RSTP can recover network faults quickly, but the fault recovery time depends on the number of devices on the network and the network topology. A typical figure for the fault recovery time is 300ms. Therefore, RSTP cannot achieve the “bumpless” redundancy that some other protocols can.

Refer to IEEE 802.1D 2004 standard for detailed information about the opration of the protocol.

5.5 CONFIGURING IP ADDRESS

The redundant Ethernet facility does not have any special IP address configuration requirements. There is just one IP address for the device, which can be configured using the IEC61850 configurator as for a standard Ethernet device.

The IED configurator will automatically display the PRP/HSR configuration parameters.

6 DATA PROTOCOLS

The products supports a wide range of protocols to make them applicable to many industries and applications. The exact data protocols supported by a particular product depend on its chosen application, but the following table gives a list of the data protocols that are typically available.

SCADA data protocols

Data Protocol	Layer 1 protocol	Description
Courier	K-Bus, RS485, Ethernet, USB	Standard for SCADA communications developed by General Electric.
MODBUS	RS485	Standard for SCADA communications developed by Modicon.
IEC 60870-5-103	RS485	IEC standard for SCADA communications
DNP 3.0	RS485, Ethernet	Standard for SCADA communications developed by Harris. Used mainly in North America.
IEC 61850	Ethernet	IEC standard for substation automation. Facilitates interoperability.

The relationship of these protocols to the lower level physical layer protocols are as follows:

<table>
<tr><td rowspan="2">Data Protocols</td><td>IEC 60870-5-103
MODBUS
DNP3.0
Courier</td><td>IEC 61850
DNP3.0
Courier</td><td>Courier</td><td>Courier</td></tr>
<tr><td>Data Link Layer</td><td>EIA(RS)485</td><td>Ethernet</td><td>USB</td><td>K-Bus</td></tr>
<tr><td>Physical Layer</td><td colspan="4">Copper or Optical Fibre</td></tr>
</table>

6.1 COURIER

This section should provide sufficient detail to enable understanding of the Courier protocol at a level required by most users. For situations where the level of information contained in this manual is insufficient, further publications (R6511 and R6512) containing in-depth details about the protocol and its use, are available on request.

Courier is an General Electric proprietary communication protocol. Courier uses a standard set of commands to access a database of settings and data in the IED. This allows a master to communicate with a number of slave devices. The application-specific elements are contained in the database rather than in the commands used to interrogate it, meaning that the master station does not need to be preconfigured. Courier also provides a sequence of event (SOE) and disturbance record extraction mechanism.

6.1.1 PHYSICAL CONNECTION AND LINK LAYER

In the P40 Agile products, Courier can be used with three physical layer protocols: K-Bus, EIA(RS)485 and USB.

Three connection options are available for Courier:

- The front USB port - for connection to Settings application software on, for example, a laptop
- Rear serial port 1 - for permanent SCADA connection via RS485 or K-Bus
- The optional rear serial port 2 - for permanent SCADA connection via RS485 or K-Bus

The IED address and baud rate can be selected using the front panel menu or by a suitable application such as MiCOM S1 Agile.

6.1.2 COURIER DATABASE

The Courier database is two-dimensional and resembles a table. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255 (0000 to FFFF Hexadecimal.

Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The product-specific menu databases contain the complete database definition.

6.1.3 SETTINGS CATEGORIES

There are two main categories of settings in protection IEDs:

- Control and support settings
- Protection settings

With the exception of the Disturbance Recorder settings, changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to the Protection settings and the Disturbance Recorder settings are stored in 'scratchpad' memory and are not immediately implemented. These need to be committed by writing to the ***Save Changes*** cell in the *CONFIGURATION* column.

6.1.4 SETTING CHANGES

Courier provides two mechanisms for making setting changes. Either method can be used for editing any of the settings in the database.

Method 1

This uses a combination of three commands to perform a settings change:

First, enter Setting mode: This checks that the cell is settable and returns the limits.

1. Preload Setting: This places a new value into the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
2. Execute Setting: This confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
3. Abort Setting: This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are extracted before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

Method 2

The Set Value command can be used to change a setting directly. The response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method, however the limits are not extracted. This method is therefore most suitable for off-line setting editors such as MiCOM S1 Agile, or for issuing preconfigured control commands.

6.1.5 EVENT EXTRACTION

You can extract events either automatically (rear serial port only) or manually (either serial port). For automatic extraction, all events are extracted in sequential order using the Courier event mechanism. This includes fault and maintenance data if appropriate. The manual approach allows you to select events, faults, or maintenance data as desired.

6.1.5.1 AUTOMATIC EVENT RECORD EXTRACTION

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the ***Event*** bit is set in the ***Status*** byte. This indicates to the Master device that event information is available. The oldest, non-extracted event can be extracted from the IED using the ***Send Event*** command. The IED responds with the event data.

Once an event has been extracted, the ***Accept Event*** command can be used to confirm that the event has been successfully extracted. When all events have been extracted, the ***Event*** bit is reset. If there are more events still to be extracted, the next event can be accessed using the ***Send Event*** command as before.

6.1.5.2 MANUAL EVENT RECORD EXTRACTION

The *VIEW RECORDS* column (location 01) is used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. You can select events by event number and directly select a fault or maintenance record by number.

Event Record Selection ('Select Event' cell: 0101)

This cell can be set the number of stored events. For simple event records (Type 0), cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault Record Selection ('Select Fault' cell: 0105)

This cell can be used to select a fault record directly, using a value between 0 and 4 to select one of up to five stored fault records. (0 is the most recent fault and 4 is the oldest). The column then contains the details of the fault record selected.

Maintenance Record Selection ('Select Maint' cell: 01F0)

This cell can be used to select a maintenance record using a value between 0 and 4. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information, the number associated with a particular record changes when a new event or fault occurs.

Event Types

The IED generates events under certain circumstances such as:

- Change of state of output contact
- Change of state of opto-input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

Event Record Format

The IED returns the following fields when the Send Event command is invoked:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Menu Database contains tables of possible events, and shows how the contents of the above fields are interpreted. Fault and Maintenance records return a Courier Type 3 event, which contains the above fields plus two additional fields:

- Event extraction column
- Event number

These events contain additional information, which is extracted from the IED using column B4. Row 01 contains a ***Select Record*** setting that allows the fault or maintenance record to be selected. This setting should be set to the

event number value returned in the record. The extended data can be extracted from the IED by uploading the text and data from the column.

6.1.6 DISTURBANCE RECORD EXTRACTION

The stored disturbance records are accessible through the Courier interface. The records are extracted using column (B4).

The ***Select Record*** cell can be used to select the record to be extracted. Record 0 is the oldest non-extracted record. Older records which have been already been extracted are assigned positive values, while younger records are assigned negative values. To help automatic extraction through the rear port, the IED sets the ***Disturbance*** bit of the ***Status*** byte, whenever there are non-extracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from the ***Trigger Time*** cell (B402). The disturbance record can be extracted using the block transfer mechanism from cell B40B and saved in the COMTRADE format. The settings application software software automatically does this.

6.1.7 PROGRAMMABLE SCHEME LOGIC SETTINGS

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the IED using the block transfer mechanism.

The following cells are used to perform the extraction:

- ***Domain*** cell (B204): Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- ***Sub-Domain*** cell (B208): Used to select the Protection Setting Group to be uploaded or downloaded.
- ***Version*** cell (B20C): Used on a download to check the compatibility of the file to be downloaded.
- ***Transfer Mode*** cell (B21C): Used to set up the transfer process.
- ***Data Transfer*** cell (B120): Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the IED using this mechanism. The settings application software must be used to edit the settings. It also performs checks on the validity of the settings before they are transferred to the IED.

6.1.8 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the Courier protocol. The device will correct for the transmission delay. The time synchronization message may be sent as either a global command or to any individual IED address. If the time synchronization message is sent to an individual address, then the device will respond with a confirm message. If sent as a global command, the (same) command must be sent twice. A time synchronization Courier event will be generated/produced whether the time-synchronization message is sent as a global command or to any individual IED address.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

6.1.9 COURIER CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.

3. Move to the first cell down (***RP1 protocol***). This is a non-settable cell, which shows the chosen communication protocol – in this case *Courier*.

```
COMMUNICATIONS
RP1 Protocol
Courier
```

4. Move down to the next cell (***RP1 Address***). This cell controls the address of the RP1 port on the device. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 1 and 254 for the Relay Address. It is set to 255 by default, which has to be changed. It is important that no two IEDs share the same address.

```
COMMUNICATIONS
RP1 Address
100
```

5. Move down to the next cell (***RP1 InactivTimer***). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before revoking any password access that was enabled and discarding any changes. For the rear port this can be set between 1 and 30 minutes.

```
COMMUNICATIONS
RP1 Inactivtimer
10.00 mins.
```

6. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

```
COMMUNICATIONS
RP1 PhysicalLink
Copper
```

7. Move down to the next cell (***RP1 Card Status***). This cell is not settable. It displays the status of the chosen physical layer protocol for RP1.

```
COMMUNICATIONS
RP1 Card Status
K-Bus OK
```

8. Move down to the next cell (***RP1 Port Config***). This cell controls the type of serial connection. Select between K-Bus or RS485.

```
COMMUNICATIONS
RP1 Port Config
K-Bus
```

9. If using EIA(RS)485, the next cell (***RP1 Comms Mode***) selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity. If using K-Bus this cell will not appear.

```
COMMUNICATIONS
RP1 Comms Mode
IEC 60870 FT1.2
```

10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; 9600, 19200 and 38400. If using K-Bus this cell will not appear as the baud rate is fixed at 64 kbps.

```
COMMUNICATIONS
RP1 Baud rate
19200
```

6.2 IEC 60870-5-103

The specification IEC 60870-5-103 (Telecontrol Equipment and Systems Part 5 Section 103: Transmission Protocols), defines the use of standards IEC 60870-5-1 to IEC 60870-5-5, which were designed for communication with protection equipment

This section describes how the IEC 60870-5-103 standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 60870-5-103 standard.

This section should provide sufficient detail to enable understanding of the standard at a level required by most users.

The IEC 60870-5-103 interface is a master/slave interface with the device as the slave device. The device conforms to compatibility level 2, as defined in the IEC 60870-5-103.standard.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (reset)
- Time synchronization
- Event record extraction
- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

6.2.1 PHYSICAL CONNECTION AND LINK LAYER

There is just one option for IEC 60870-5-103:

- Rear serial port 1- for permanent SCADA connection via RS485

The IED address and baud rate can be selected using the front panel menu or by a suitable application such as MiCOM S1 Agile.

6.2.2 INITIALISATION

Whenever the device has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The device will respond to either of the two reset commands; Reset CU or Reset FCB (Communication Unit or Frame Count Bit). The difference between the two commands is that the Reset CU command will clear any unsent messages in the transmit buffer, whereas the Reset FCB command does not delete any messages.

The device will respond to the reset command with an identification message ASDU 5. The Cause of Transmission (COT) of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Menu Database, available from General Electric separately if required.

In addition to the above identification message, it will also produce a power up event.

6.2.3 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The device will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send/confirm message then the device will respond with a confirm message. A time synchronization Class 1 event will be generated/produced whether the time-synchronization message is sent as a send confirm or a broadcast (send/no reply) message.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

6.2.4 SPONTANEOUS EVENTS

Events are categorized using the following information:

- Function type
- Information Number

The IEC 60870-5-103 profile in the Menu Database contains a complete listing of all events produced by the device.

6.2.5 GENERAL INTERROGATION (GI)

The GI request can be used to read the status of the device, the function numbers, and information numbers that will be returned during the GI cycle. These are shown in the IEC 60870-5-103 profile in the Menu Database.

6.2.6 CYCLIC MEASUREMENTS

The device will produce measured values using ASDU 9 on a cyclical basis, this can be read from the device using a Class 2 poll (note ADSU 3 is not used). The rate at which the device produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu or using MiCOM S1 Agile. It is active immediately following a change.

The device transmits its measurands at 2.4 times the rated value of the analogue value.

6.2.7 COMMANDS

A list of the supported commands is contained in the Menu Database. The device will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating 'negative acknowledgement'.

6.2.8 TEST MODE

It is possible to disable the device output contacts to allow secondary injection testing to be performed using either the front panel menu or the front serial port. The IEC 60870-5-103 standard interprets this as 'test mode'. An

event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the device is in test mode will have a COT of 'test mode'.

6.2.9 DISTURBANCE RECORDS

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

> *Note:*
> *IEC 60870-5-103 only supports up to 8 records.*

6.2.10 COMMAND/MONITOR BLOCKING

The device supports a facility to block messages in the monitor direction (data from the device) and also in the command direction (data to the device). Messages can be blocked in the monitor and command directions using one of the two following methods

- The menu command ***RP1 CS103Blcking*** in the *COMMUNICATIONS* column
- The DDB signals Monitor Blocked and Command Blocked

6.2.11 IEC 60870-5-103 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 protocol***). This is a non-settable cell, which shows the chosen communication protocol – in this case `IEC 60870-5-103`.

```
COMMUNICATIONS
RP1 Protocol
IEC 60870-5-103
```

4. Move down to the next cell (***RP1 Address***). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.

```
COMMUNICATIONS
RP1 address
162
```

5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Two baud rates are supported by the IED, `9600 bits/s` and `19200 bits/s`. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
9600 bits/s
```

6. Move down to the next cell (***RP1 Meas Period***). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

```
COMMUNICATIONS
RP1 Meas Period
30.00 s
```

7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

```
COMMUNICATIONS
RP1 PhysicalLink
Copper
```

8. The next cell down (***RP1 CS103Blcking***) can be used for monitor or command blocking.

```
COMMUNICATIONS
RP1 CS103Blcking
Disabled
```

9. There are three settings associated with this cell; these are:

Setting:	Description:
Disabled	No blocking selected.
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energising an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a "Termination of general interrogation" message to the master station.
Command Blocking	When the command blocking DDB signal is active high, either by energising an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a "negative acknowledgement of command" message to the master station.

6.3 DNP 3.0

This section describes how the DNP 3.0 standard is applied in the product. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the DNP 3.0 standard.

The descriptions given here are intended to accompany the device profile document that is included in the Menu Database document. The DNP 3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP 3.0 implementation. This is the standard format DNP 3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the device using DNP 3.0. The IED operates as a DNP 3.0 slave and supports subset level 2, as described in the DNP 3.0 standard, plus some of the features from level 3.

The DNP 3.0 protocol is defined and administered by the DNP Users Group. For further information on DNP 3.0 and the protocol specifications, please see the DNP website (www.dnp.org).

6.3.1 PHYSICAL CONNECTION AND LINK LAYER

DNP 3.0 can be used with two physical layer protocols: EIA(RS)485, or Ethernet.

Several connection options are available for DNP 3.0

- Rear serial port 1 - for permanent SCADA connection via RS485
- The rear Ethernet RJ45 port on the optional Ethernet board - for permanent SCADA Ethernet connection
- The rear Ethernet fibre port on the optional Ethernet board - for permanent SCADA Ethernet connection

With DNP3 Over Ethernet, a maximum of 10 Clients can be configured. They are configured using the DNP3 Configurator

The IED address and baud rate can be selected using the front panel menu or by a suitable application such as MiCOM Agile.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 stop bit and optional configurable parity bit.

6.3.2 OBJECT 1 BINARY INPUTS

Object 1, binary inputs, contains information describing the state of signals in the IED, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and opto-inputs, alarm signals, and protection start and trip signals. The 'DDB number' column in the device profile document provides the DDB numbers for the DNP 3.0 point data. These can be used to cross-reference to the DDB definition list. See the relevant Menu Database document. The binary input points can also be read as change events using Object 2 and Object 60 for class 1-3 event data.

6.3.3 OBJECT 10 BINARY OUTPUTS

Object 10, binary outputs, contains commands that can be operated using DNP 3.0. Therefore the points accept commands of type pulse on (null, trip, close) and latch on/off as detailed in the device profile in the relevant Menu Database document, and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the Control Inputs. Described as Alias Control Inputs, they reflect the state of the Control Input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

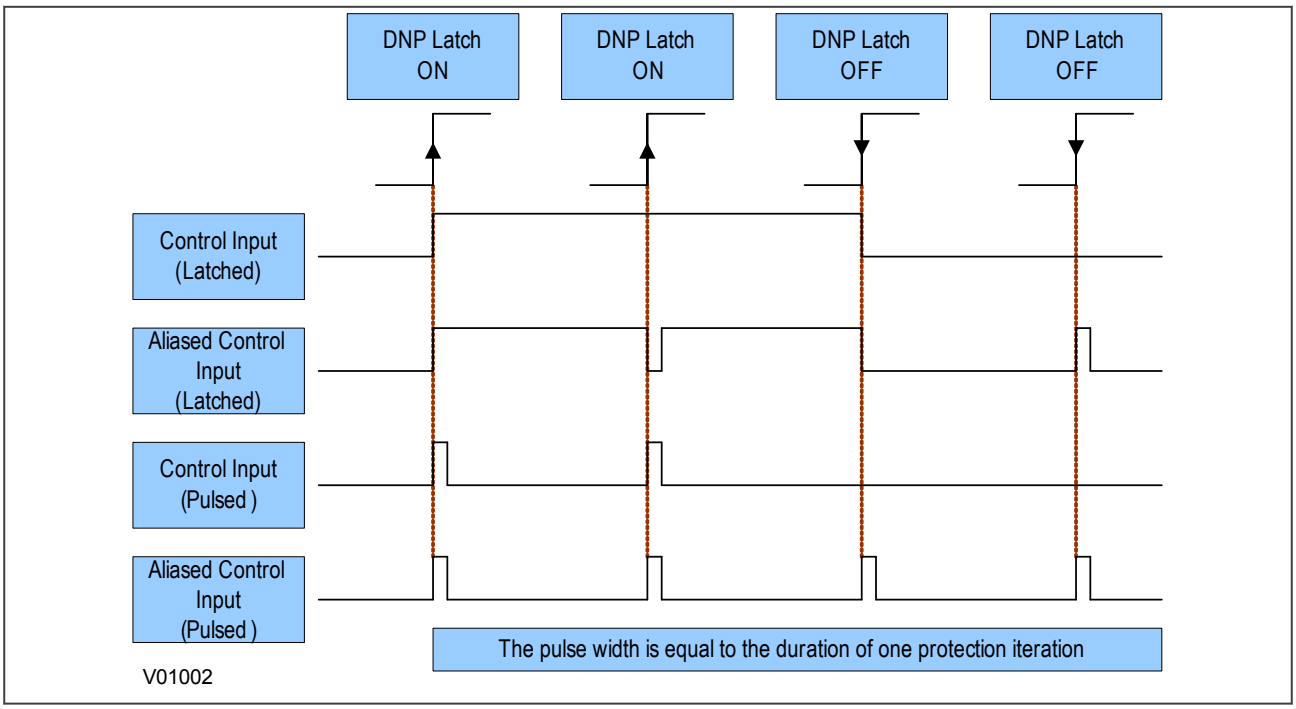


Figure 195: Control input behaviour

Many of the IED's functions are configurable so some of the Object 10 commands described in the following sections may not be available. A read from Object 10 reports the point as off-line and an operate command to Object 12 generates an error response.

Examples of Object 10 points that maybe reported as off-line are:

- Activate setting groups: Ensure setting groups are enabled
- CB trip/close: Ensure remote CB control is enabled
- Reset NPS thermal: Ensure NPS thermal protection is enabled
- Reset thermal O/L: Ensure thermal overload protection is enabled
- Reset RTD flags: Ensure RTD Inputs is enabled
- Control inputs: Ensure control inputs are enabled

6.3.4 OBJECT 20 BINARY COUNTERS

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from Object 20, or as a 'frozen' value from Object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding Object 21 frozen counter. The freeze and clear function resets the Object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from Object 22 and Object 23 respectively. Counter change events (Object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (Object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

6.3.5 OBJECT 30 ANALOGUE INPUT

Object 30, analogue inputs, contains information from the IED's measurements columns in the menu. All object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the IED's CT and VT ratios), and this is settable in the *COMMUNICATIONS* column in the IED. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analogue measurement that is unavailable when it is read is reported as offline. For example, the frequency would be offline if the current and voltage frequency is outside the tracking range of the IED. All Object 30 points are reported as secondary values in DNP 3.0 (with respect to CT and VT ratios).

6.3.6 OBJECT 40 ANALOGUE OUTPUT

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the IED such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

6.3.7 OBJECT 50 TIME SYNCHRONISATION

Function codes 1 (read) and 2 (write) are supported for Object 50 (time and date) variation 1. The DNP Need Time function (the duration of time waited before requesting another time sync from the master) is supported, and is configurable in the range 1 - 30 minutes.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

6.3.8 DNP3 DEVICE PROFILE

This section describes the specific implementation of DNP version 3.0 within General Electric MiCOM P40 Agile IEDs for both compact and modular ranges.

The devices use the DNP 3.0 Slave Source Code Library version 3 from Triangle MicroWorks Inc.

This document, in conjunction with the DNP 3.0 Basic 4 Document Set, and the DNP Subset Definitions Document, provides complete information on how to communicate with the devices using the DNP 3.0 protocol.

This implementation of DNP 3.0 is fully compliant with DNP 3.0 Subset Definition Level 2. It also contains many Subset Level 3 and above features.

6.3.8.1 DNP3 DEVICE PROFILE TABLE

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a “Document”, it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

DNP 3.0 **Device Profile Document**	
Vendor Name:	General Electric
Device Name:	MiCOM P40Agile Protection Relays – compact and modular range
Models Covered:	All models
Highest DNP Level Supported*: *This is the highest DNP level FULLY supported. Parts of level 3 are also supported	For Requests: Level 2 For Responses: Level 2
Device Function:	Slave
Notable objects, functions, and/or qualifiers supported in addition to the highest DNP levels supported (the complete list is described in the DNP 3.0 Implementation Table): For static (non-change event) object requests, request qualifier codes 00 and 01 (start-stop), 07 and 08 (limited quantity), and 17 and 28 (index) are supported in addition to the request qualifier code 06 (no range (all points)) Static object requests sent with qualifiers 00, 01, 06, 07, or 08 will be responded with qualifiers 00 or 01 Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28 For change-event object requests, qualifiers 17 or 28 are always responded 16-bit and 32-bit analogue change events with time may be requested The read function code for Object 50 (time and date) variation 1 is supported Analogue Input Deadbands, Object 34, variations 1 through 3, are supported Floating Point Analogue Output Status and Output Block Objects 40 and 41 are supported Sequential file transfer, Object 70, variations 2 through 7, are supported Device Attribute Object 0 is supported	
Maximum Data Link Frame Size (octets):	Transmitted: 292 Received: 292
Maximum Application Fragment Size (octets)	Transmitted: Configurable (100 to 2048). Default 2048 Received: 249

DNP 3.0 Device Profile Document	
Maximum Data Link Retries:	Fixed at 2
Maximum Application Layer Retries:	None
Requires Data Link Layer Confirmation:	Configurable to Never or Always
Requires Application Layer Confirmation:	When reporting event data (Slave devices only) When sending multi-fragment responses (Slave devices only)
Timeouts while waiting for:	
Data Link Confirm:	Configurable
Complete Application Fragment:	None
Application Confirm:	Configurable
Complete Application Response:	None
Others:	
Data Link Confirm Timeout:	Configurable from 0 (Disabled) to 120s, default 10s.
Application Confirm Timeout:	Configurable from 1 to 120s, default 2s.
Select/Operate Arm Timeout:	Configurable from 1 to 10s, default 10s.
Need Time Interval (Set IIN1-4):	Configurable from 1 to 30, default 10min.
Application File Timeout	60 s
Analog Change Event Scan Period:	Fixed at 0.5s
Counter Change Event Scan Period	Fixed at 0.5s
Frozen Counter Change Event Scan Period	Fixed at 1s
Maximum Delay Measurement Error:	2.5 ms
Time Base Drift Over a 10-minute Interval:	7 ms
Sends/Executes Control Operations:	
Write Binary Outputs:	Never
Select/Operate:	Always
Direct Operate:	Always
Direct Operate - No Ack:	Always
Count > 1	Never
Pulse On	Always
Pulse Off	Sometimes
Latch On	Always
Latch Off	Always
Queue	Never
Clear Queue	Never
Note: Paired Control points will accept Pulse On/Trip and Pulse On/Close, but only single point will accept the Pulse Off control command.	
Reports Binary Input Change Events when no specific variation requested:	Configurable to send one or the other
Reports time-tagged Binary Input Change Events when no specific variation requested:	Binary input change with time
Sends Unsolicited Responses:	Never
Sends Static Data in Unsolicited Responses:	Never No other options are permitted
Default Counter Object/Variation:	Configurable, Point-by-point list attached Default object: 20 Default variation: 1

DNP 3.0 Device Profile Document	
Counters Roll Over at:	32 bits
Sends multi-fragment responses:	Yes
Sequential File Transfer Support:	
Append File Mode	No
Custom Status Code Strings	No
Permissions Field	Yes
File Events Assigned to Class	No
File Events Send Immediately	Yes
Multiple Blocks in a Fragment	No
Max Number of Files Open	1

6.3.8.2 DNP3 IMPLEMENTATION TABLE

The implementation table provides a list of objects, variations and control codes supported by the device:

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
1	0	Binary Input (Variation 0 is used to request default variation)	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
1	1 (default - see note 1)	Binary Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
1	2	Binary Input with Flag	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
2	0	Binary Input Change - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
2	1	Binary Input Change without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
2	2	Binary Input Change with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
10	0	Binary Output Status - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
10	2 (default - see note 1)	Binary Output Status	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
12	1	Control Relay Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28	(index)	129	response		echo of request
20	0	Binary Counter - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
			7 8 9 10	(freeze) (freeze noack) (freeze clear) (frz. cl. Noack)	00, 01 06 07, 08	(start-stop) (no range, or all) (limited qty)				
20	1	32-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
20	2	16-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	5 (default - see note 1)	32-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	6	16-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	0	Frozen Counter - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
21	1	32-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	2	16-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	5	32-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 1)
21	6	16-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) 17, 28 (index - see note 1)
21	9 (default - see note 1)	32-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	10	16-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
`22	0	Counter Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
22	1 (default - see note 1)	32-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	2	16-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	5	32-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	6	16-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1	(read)	06 07, 08	(no range, or all) (limited qty)				
23	1 (default - see note 1)	32-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	2	16-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	5	32-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	6	16-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
30	0	Analog Input - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
30	1	32-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	2	16-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	3 (default - see note 1)	32-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	4	16-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	5	Short floating point	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
32	0	Analog Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
32	1 (default - see note 1)	32-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	2	16-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	3	32-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	4	16-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	5	Short floating point Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	7	Short floating point Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
34	0	Analog Input Deadband (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
34	1	16 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	2 (default - see note 1)	32 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	3	Short Floating Point Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
40	0	Analog Output Status (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
40	1 (default - see note 1)	32-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	2	16-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	3	Short Floating Point Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
41	1	32-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request
41	2	16-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request
41	3	Short Floating Point Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 27, 28	(index)	129	response		echo of request
50	1 (default - see note 1)	Time and Date	1	(read)	07	(limited qty = 1)	129	response	07	(limited qty = 1)
			2	(write)	07	(limited qty = 1)				
60	0	Not defined								
60	1	Class 0 Data	1	(read)	06	(no range, or all)				
60	2	Class 1 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	3	Class 2 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	4	Class 3 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	0	File Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	2	File Authentication	29	(authenticate)	5b	(free-format)	129	response		5B (free-format)
70	3	File Command	25 27	(open) (delete)	5b	(free-format)				
70	4	File Command Status	26 30	(close) (abort)	5b	(free-format)	129	response		5B (free-format)
70	5	File Transfer	1	(read)	5b	(free-format)	129	response		5B (free-format)
70	6	File Transfer Status					129	response		5B (free-format)
70	7	File Descriptor	28	(get file info)	5b	(free-format)	129	response		5B (free-format)
80	1	Internal Indications	1	(read)	00, 01	(start-stop)	129	response	00, 01	(start-stop)
		No Object (function code only)	13	(cold restart)						
		No Object (function code only)	14	(warm restart)						
		No Object (function code only)	23	(delay meas.)						

Note:
A Default variation refers to the variation responded to when variation 0 is requested and/or in class 0, 1, 2, or 3 scans.

Note:
For static (non-change-event) objects, qualifiers 17 or 28 are only responded to when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded to with qualifiers 00 or 01. For change-event objects, qualifiers 17 or 28 are always responded to.

6.3.8.3 DNP3 INTERNAL INDICATIONS

The following table lists the DNP3.0 Internal Indications (IIN) and identifies those that are supported by the device.

The IIN form an information element used to convey the internal states and diagnostic results of a device. This information can be used by a receiving station to perform error recovery or other suitable functions. The IIN is a two-octet field that follows the function code in all responses from the device. When a request cannot be processed due to formatting errors or the requested data is not available, the IIN is always returned with the appropriate bits set.

Bit	Indication	Description	Supported
Octet 1			
0	All stations message received	Set when a request is received with the destination address of the all stations address (6553510). It is cleared after the next response (even if a response to a global request is required). This IIN is used to let the master station know that a "broadcast" message was received by the relay.	Yes
1	Class 1 data available	Set when data that has been configured as Class 1 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
2	Class 2 data available	Set when data that has been configured as Class 2 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
3	Class 3 data available	Set when data that has been configured as Class 3 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
4	Time-synchronization required	The relay requires time synchronization from the master station (using the Time and Date object). This IIN is cleared once the time has been synchronized. It can also be cleared by explicitly writing a 0 into this bit of the Internal Indication object.	Yes
5	Local	Set when some or all of the relays digital output points (Object 10/12) are in the Local state. That is, the relays control outputs are NOT accessible through the DNP protocol. This IIN is clear when the relay is in the Remote state. That is, the relays control outputs are fully accessible through the DNP protocol.	No
6	Device in trouble	Set when an abnormal condition exists in the relay. This IIN is only used when the state cannot be described by a combination of one or more of the other IIN bits.	No
7	Device restart	Set when the device software application restarts. This IIN is cleared when the master station explicitly writes a 0 into this bit of the Internal Indications object.	Yes
Octet 2			
0	Function code not implemented	The received function code is not implemented within the relay.	Yes

Bit	Indication	Description	Supported
1	Requested object(s) unknown	The relay does not have the specified objects or there are no objects assigned to the requested class. This IIN should be used for debugging purposes and usually indicates a mismatch in device profiles or configuration problems.	Yes
2	Out of range	Parameters in the qualifier, range or data fields are not valid or out of range. This is a 'catch-all' for application request formatting errors. It should only be used for debugging purposes. This IIN usually indicates configuration problems.	Yes
3	Buffer overflow	Event buffer(s), or other application buffers, have overflowed. The master station should attempt to recover as much data as possible and indicate to the user that there may be lost data. The appropriate error recovery procedures should be initiated by the user.	Yes
4	Already executing	The received request was understood but the requested operation is already executing.	
5	Bad configuration	Set to indicate that the current configuration in the relay is corrupt. The master station may download another configuration to the relay.	Yes
6	Reserved	Always returned as zero.	
7	Reserved	Always returned as zero.	

6.3.8.4 DNP3 RESPONSE STATUS CODES

When the device processes Control Relay Output Block (Object 12) requests, it returns a set of status codes; one for each point contained within the original request. The complete list of codes appears in the following table:

Code Number	Identifier Name	Description
0	Success	The received request has been accepted, initiated, or queued.
1	Timeout	The request has not been accepted because the 'operate' message was received after the arm timer (Select Before Operate) timed out. The arm timer was started when the select operation for the same point was received.
2	No select	The request has not been accepted because no previous matching 'select' request exists. (An 'operate' message was sent to activate an output that was not previously armed with a matching 'select' message).
3	Format error	The request has not been accepted because there were formatting errors in the control request ('select', 'operate', or 'direct operate').
4	Not supported	The request has not been accepted because a control operation is not supported for this point.
5	Already active	The request has not been accepted because the control queue is full or the point is already active.
6	Hardware error	The request has not been accepted because of control hardware problems.
7	Local	The request has not been accepted because local access is in progress.
8	Too many operations	The request has not been accepted because too many operations have been requested.
9	Not authorized	The request has not been accepted because of insufficient authorization.
127	Undefined	The request not been accepted because of some other undefined reason.

Note:
Code numbers 10 through to 126 are reserved for future use.

6.3.9 DNP3 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 protocol***). This is a non-settable cell, which shows the chosen communication protocol – in this case `DNP3.0`.

```
COMMUNICATIONS
RP1 Protocol
DNP3.0
```

4. Move down to the next cell (***RP1 Address***). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the Relay Address. It is important that no two IEDs have the same address.

```
COMMUNICATIONS
RP1 Address
1
```

5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps and 38400 bps. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
9600 bits/s
```

6. Move down to the next cell (***RP1 Parity***). This cell controls the parity format used in the data frames. The parity can be set to be one of `None`, `Odd` or `Even`. Make sure that the parity format selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Parity
None
```

7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).

```
COMMUNICATIONS
RP1 PhysicalLink
Copper
```

8. Move down to the next cell (***RP1 Time Sync***). This cell affects the time synchronisation request from the master by the IED. It can be set to `enabled` or `disabled`. If enabled it allows the DNP3.0 master to synchronise the time on the IED.

```
COMMUNICATIONS
RP1 Time Sync
Enabled
```

6.3.9.1 DNP3 CONFIGURATOR

A PC support package for DNP3.0 is available as part of the supplied settings application software (MiCOM S1 Agile) to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new DNP3.0

configuration takes effect after the download is complete. To restore the default configuration at any time, from the *CONFIGURATION* column, select the ***Restore Defaults*** cell then select `All Settings`.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

If the device supports DNP Over Ethernet, the configuration related settings are done in the folder **DNP Over Ethernet**.

6.3.10 DNP3 UNSOLICITED REPORTING

In previous versions, DNP3 only supports data transmission based on poll requests from the master station. From this version onwards, a new mode of transmission called Unsolicited Reporting is supported. This is a mode of operation where the outstation spontaneously transmits a response without having received a specific request for data. This mode is useful when the system has many outstations and the master requires notification as soon as possible after a change occurs. Rather than waiting for a master station polling cycle, the outstation transmits the change immediately. It is thus event driven rather than poll driven.

This feature requires a new group of settings, which are found under the DNP SETTINGS column (Courier cell range 1B). These can be found in the settings tables available as an interactive PDF at the back of the manual.

Note:
We advise you not to enable Unsolicited Reporting on a serial multi-drop line. This is due the fact that collisions may result from multiple IEDs reporting concurrent events. If Unsolicited Reporting is enabled on a serial line, we recommend connecting only one IED per master link. This restriction is not applicable if DNP3 Over Ethernet is used.

6.4 MODBUS

This section describes how the MODBUS standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the MODBUS standard.

The MODBUS protocol is a master/slave protocol, defined and administered by the MODBUS Organization For further information on MODBUS and the protocol specifications, please see the Modbus web site (www.modbus.org).

6.4.1 PHYSICAL CONNECTION AND LINK LAYER

Only one option is available for connecting MODBUS

- Rear serial port 1 - for permanent SCADA connection via EIA(RS)485

The MODBUS interface uses 'RTU' mode communication rather than 'ASCII' mode as this provides more efficient use of the communication bandwidth. This mode of communication is defined by the MODBUS standard.

The IED address and baud rate can be selected using the front panel menu or by a suitable application such as MiCOM Agile.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 parity bit with 1 stop bit, or 2 stop bits (a total of 11 bits per character).

6.4.2 MODBUS FUNCTIONS

The following MODBUS function codes are supported:

- 01: Read Coil Status
- 02: Read Input Status
- 03: Read Holding Registers

- 04: Read Input Registers
- 06: Preset Single Register
- 08: Diagnostics
- 11: Fetch Communication Event Counter
- 12: Fetch Communication Event Log
- 16: Preset Multiple Registers 127 max

These are interpreted by the MiCOM IED in the following way:

- 01: Read status of output contacts (0xxxx addresses)
- 02: Read status of opto inputs (1xxxx addresses)
- 03: Read setting values (4xxxx addresses)
- 04: Read measured values (3xxxx addresses
- 06: Write single setting value (4xxxx addresses)
- 16: Write multiple setting values (4xxxx addresses)

6.4.3 RESPONSE CODES

MCode	MODBUS Description	MiCOM Interpretation
01	Illegal Function Code	The function code transmitted is not supported by the slave.
02	Illegal Data Address	The start data address in the request is not an allowable value. If any of the addresses in the range cannot be accessed due to password protection then all changes within the request are discarded and this error response will be returned. Note: If the start address is correct but the range includes non–implemented addresses this response is not produced.
03	Illegal Value	A value referenced in the data field transmitted by the master is not within range. Other values transmitted within the same packet will be executed if inside range.
06	Slave Device Busy	The write command cannot be implemented due to the database being locked by another interface. This response is also produced if the software is busy executing a previous request.

6.4.4 REGISTER MAPPING

The device supports the following memory page references:

- Memory Page: Interpretation
- 0xxxx: Read and write access of the output relays
- 1xxxx: Read only access of the opto inputs
- 3xxxx: Read only access of data
- 4xxxx: Read and write access of settings

where xxxx represents the addresses available in the page (0 to 9999).

A complete map of the MODBUS addresses supported by the device is contained in the relevant menu database, which is available on request.

Note:
The "extended memory file" (6xxxx) is not supported.

Note:
MODBUS convention is to document register addresses as ordinal values whereas the actual protocol addresses are literal values. The MiCOM relays begin their register addresses at zero. Therefore, the first register in a memory page is register address zero. The second register is register address 1 and so on.

Note:
The page number notation is not part of the address.

6.4.5 EVENT EXTRACTION

The device supports two methods of event extraction providing either automatic or manual extraction of the stored event, fault, and maintenance records.

6.4.5.1 AUTOMATIC EVENT RECORD EXTRACTION

The automatic extraction facilities allow all types of record to be extracted as they occur. Event records are extracted in sequential order including any fault or maintenance data that may be associated with the event.

The MODBUS master can determine whether the device has any events stored that have not yet been extracted. This is performed by reading the status register 30001 (G26 data type). If the event bit of this register is set then the device has non-extracted events available. To select the next event for sequential extraction, the master station writes a value of 1 to the record selection register 40400 (G18 data type). The event data together with any fault/ maintenance data can be read from the registers specified below. Once the data has been read, the event record can be marked as having been read by writing a value of '2' to register 40400.

6.4.5.2 MANUAL EVENT RECORD EXTRACTION

There are three registers available to manually select stored records and three read-only registers allowing the number of stored records to be determined.

- 40100: Select Event
- 40101: Select Fault
- 40102: Select Maintenance Record

For each of the above registers a value of 0 represents the most recent stored record. The following registers can be read to indicate the numbers of the various types of record stored.

- 30100: Number of stored records
- 30101: Number of stored fault records
- 30102: Number of stored maintenance records

Each fault or maintenance record logged causes an event record to be created. If this event record is selected, the additional registers allowing the fault or maintenance record details will also become populated.

6.4.5.3 RECORD DATA

The location and format of the registers used to access the record data is the same whether they have been selected using either automatic or manual extraction.

Event Description	MODBUS Address	Length	Comments
Time and Date	30103	4	See G12 data type description
Event Type	30107	1	See G13 data type description
Event Value	30108	2	Nature of value depends on event type. This will contain the status as a binary flag for contact, opto-input, alarm, and protection events.

Event Description	MODBUS Address	Length	Comments
MODBUS Address	30110	1	This indicates the MODBUS register address where the change occurred. Alarm 30011 Relays 30723 Optos 30725 Protection events – like the relay and opto addresses this will map onto the MODBUS address of the appropriate DDB status register depending on which bit of the DDB the change occurred. These will range from 30727 to 30785. For platform events, fault events and maintenance events the default is 0.
Event Index	30111	1	This register will contain the DDB ordinal for protection events or the bit number for alarm events. The direction of the change will be indicated by the most significant bit; 1 for 0 – 1 change and 0 for 1 – 0 change.
Additional Data Present	30112	1	0 means that there is no additional data. 1 means fault record data can be read from 30113 to 30199 (number of registers depends on the product). 2 means maintenance record data can be read from 30036 to 30039.

If a fault record or maintenance record is directly selected using the manual mechanism then the data can be read from the register ranges specified above. The event record data in registers 30103 to 30111 will not be available.

It is possible using register 40401(G6 data type) to independently clear the stored relay event/fault and maintenance records. This register also provides an option to reset the device indications, which has the same effect on the relay as pressing the clear key within the alarm viewer using the HMI panel menu.

6.4.6 DISTURBANCE RECORD EXTRACTION

The IED provides facilities for both manual and automatic extraction of disturbance records.

Records extracted over MODBUS from Px40 devices are presented in COMTRADE format. This involves extracting an ASCII text configuration file and then extracting a binary data file.

Each file is extracted by reading a series of data pages from the IED The data page is made up of 127 registers, giving a maximum transfer of 254 bytes per page.

The following set of registers is presented to the master station to support the extraction of uncompressed disturbance records:

MODBUS registers

MODBUS Register	Name	Description
3x00001	Status register	Provides the status of the relay as bit flags: b0: Out of service b1: Minor self test failure b2: Event b3: Time synchronization b4: Disturbance b5: Fault b6: Trip b7: Alarm b8 to b15: Unused A '1' on b4 indicates the presence of a disturbance
3x00800	No of stored disturbances	Indicates the total number of disturbance records currently stored in the relay, both extracted and non-extracted.
3x00801	Unique identifier of the oldest disturbance record	Indicates the unique identifier value for the oldest disturbance record stored in the relay. This is an integer value used in conjunction with the 'Number of stored disturbances' value to calculate a value for manually selecting records.

MODBUS Register	Name	Description
4x00250	Manual disturbance record selection register	This register is used to manually select disturbance records. The values written to this cell are an offset of the unique identifier value for the oldest record. The offset value, which ranges from 0 to the Number of stored disturbances - 1, is added to the identifier of the oldest record to generate the identifier of the required record.
4x00400	Record selection command register	This register is used during the extraction process and has a number of commands. These are: b0: Select next event b1: Accept event b2: Select next disturbance record b3: Accept disturbance record b4: Select next page of disturbance data b5: Select data file
3x00930 - 3x00933	Record time stamp	These registers return the timestamp of the disturbance record.
3x00802	No of registers in data page	This register informs the master station of the number of registers in the data page that are populated.
3x00803 - 3x00929	Data page registers	These 127 registers are used to transfer data from the relay to the master station. They are 16-bit unsigned integers.
3x00934	Disturbance record status register	The disturbance record status register is used during the extraction process to indicate to the master station when data is ready for extraction. See next table.
4x00251	Data file format selection	This is used to select the required data file format. This is reserved for future use.

Note:
Register addresses are provided in reference code + address format. E.g. 4x00001 is reference code 4x, address 1 (which is specified as function code 03, address 0x0000 in the MODBUS specification).

The disturbance record status register will report one of the following values:

Disturbance record states

State	Description
Idle	This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
Busy	The relay is currently processing data.
Page ready	The data page has been populated and the master station can now safely read the data.
Configuration complete	All of the configuration data has been read without error.
Record complete	All of the disturbance data has been extracted.
Disturbance overwritten	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.
No non-extracted disturbances	An attempt was made by the master station to automatically select the next oldest non-extracted disturbance when all records have been extracted.
Not a valid disturbance	An attempt was made by the master station to manually select a record that did not exist in the relay.
Command out of sequence	The master station issued a command to the relay that was not expected during the extraction process.

6.4.6.1 MANUAL EXTRACTION PROCEDURE

The procedure used to extract a disturbance manually is shown below. The manual method of extraction does not allow for the acceptance of disturbance records.

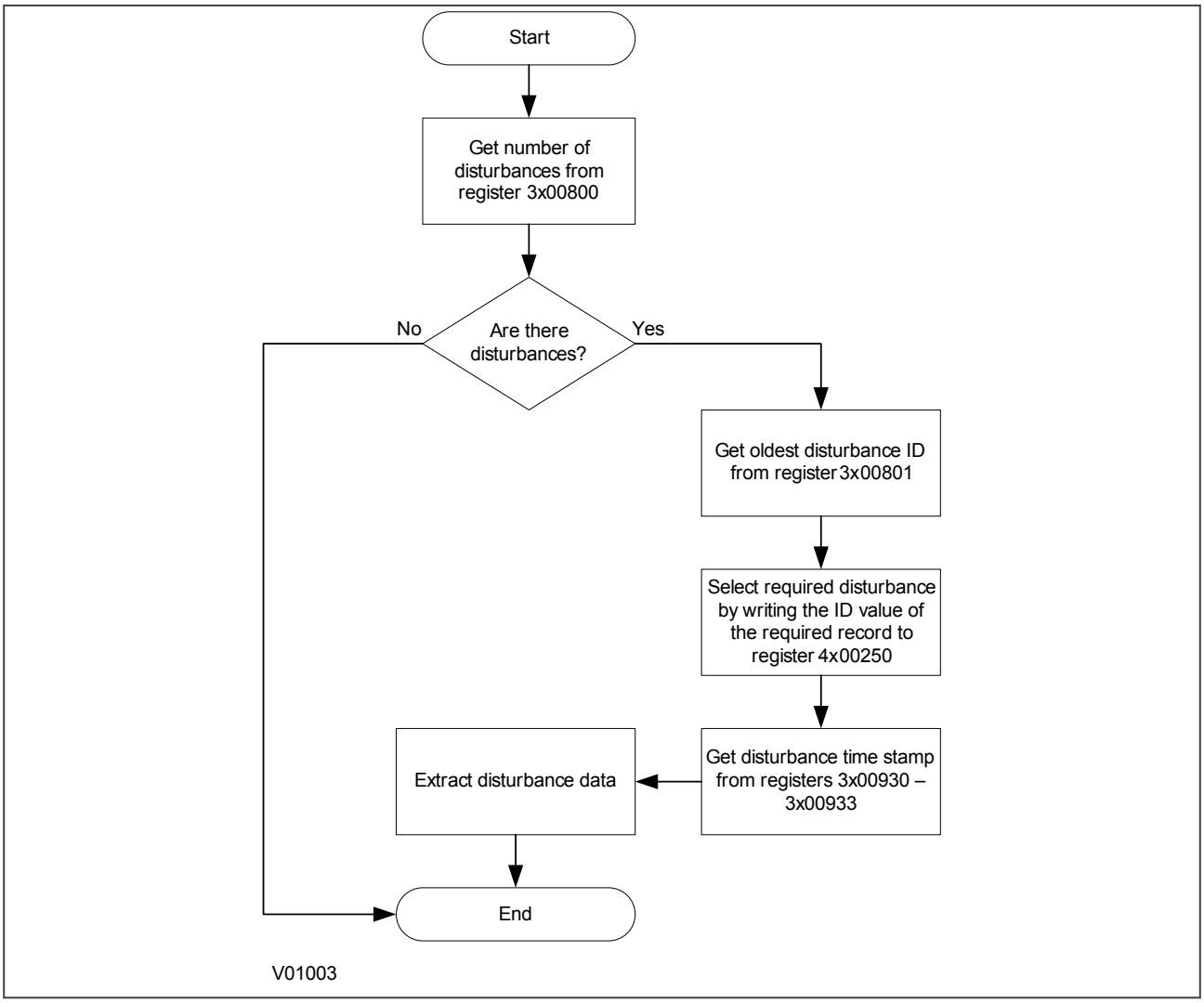


Figure 196: Manual selection of a disturbance record

6.4.6.2 AUTOMATIC EXTRACTION PROCEDURE

There are two methods that can be used for automatically extracting disturbances:

Method 1

Method 1 is simpler and is better at extracting single disturbance records (when the disturbance recorder is polled regularly).

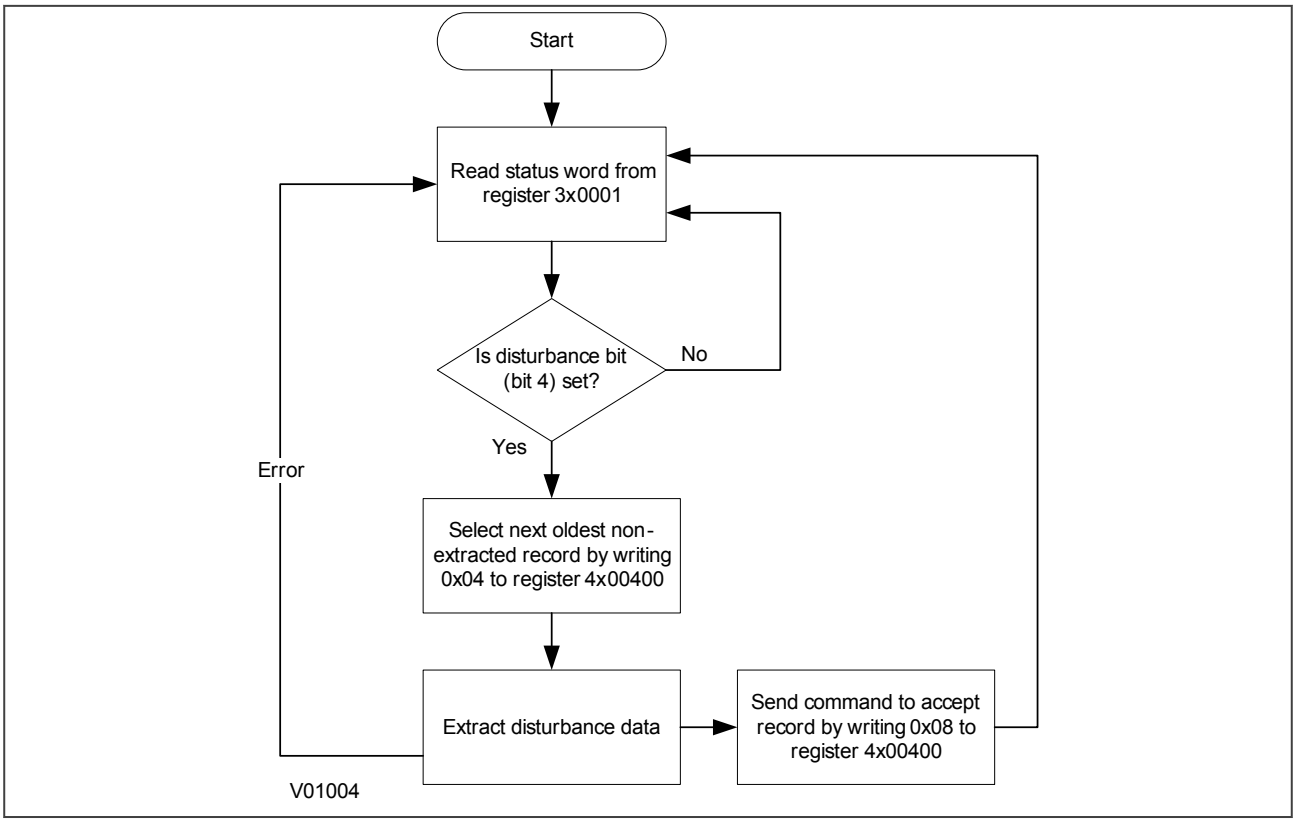


Figure 197: Automatic selection of disturbance record - method 1

Method 2

Method 2 is more complex to implement but is more efficient at extracting large quantities of disturbance records. This may be useful when the disturbance recorder is polled only occasionally and therefore may have many stored records.

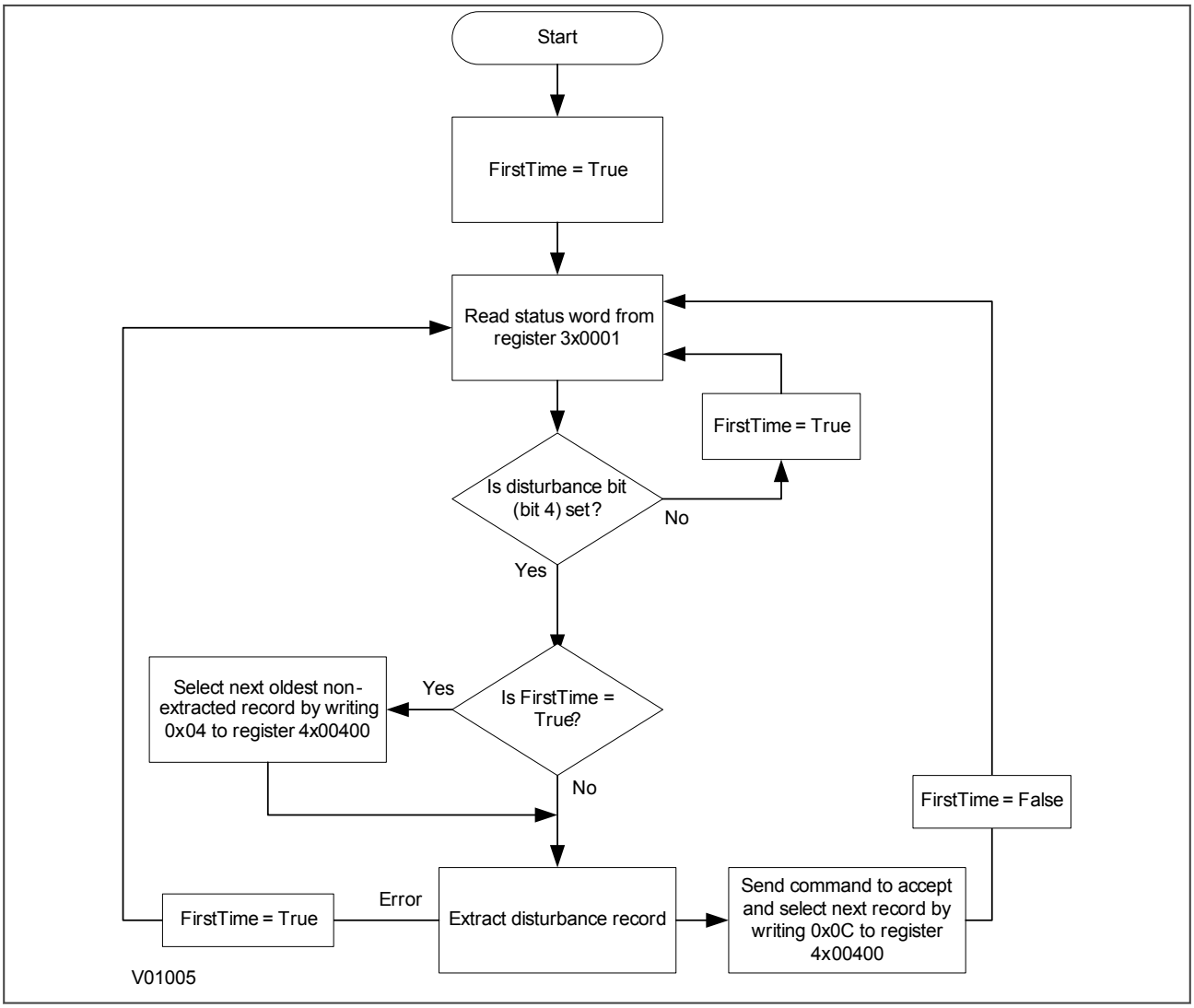


Figure 198: Automatic selection of disturbance record - method 2

6.4.6.3 EXTRACTING THE DISTURBANCE DATA

The extraction of the disturbance record is a two-stage process that involves extracting the configuration file first and then the data file. The configuration file must be extracted first, followed by the data file:

Extracting the Comtrade configuration file

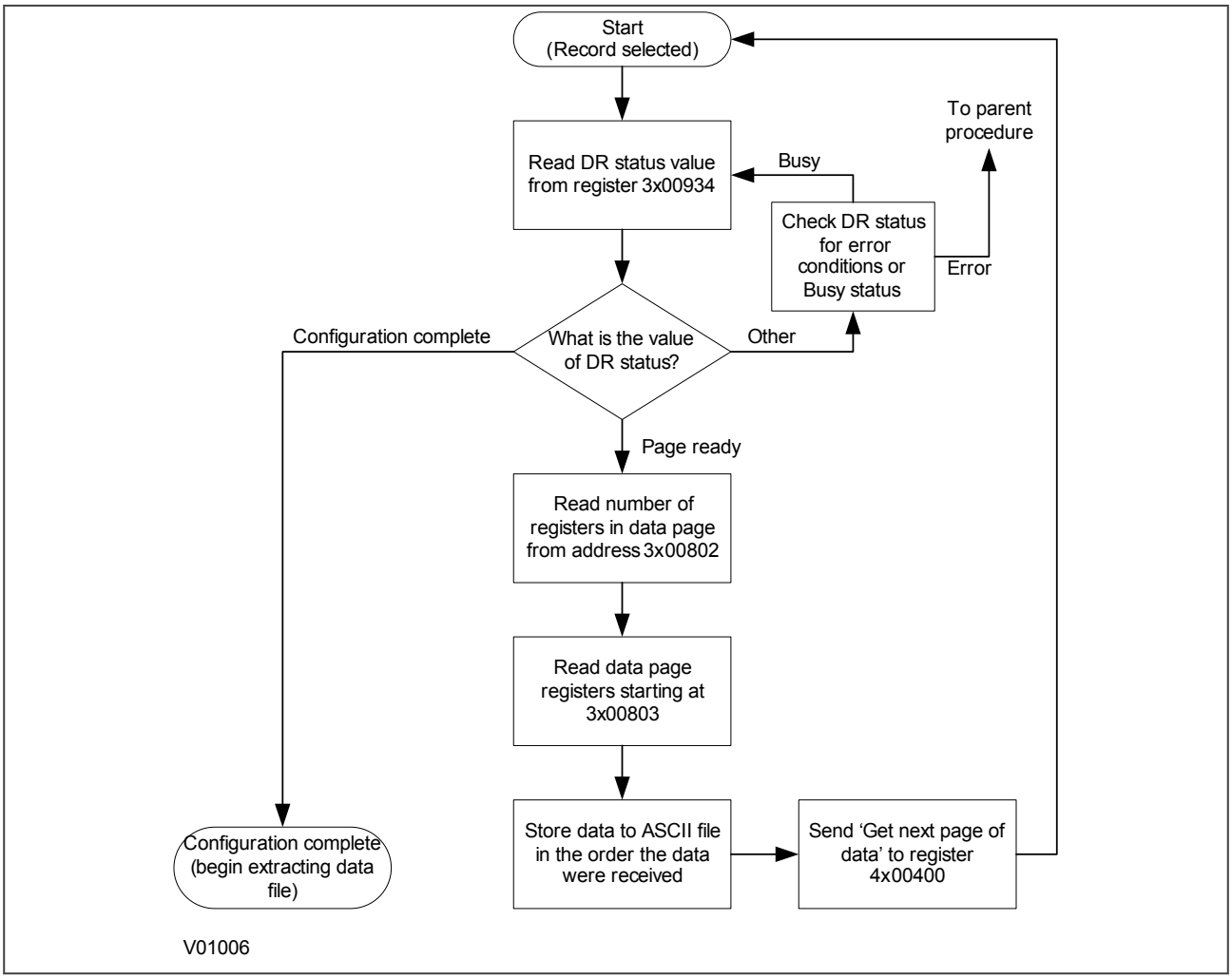


Figure 199: Configuration file extraction

Extracting the comtrade data file

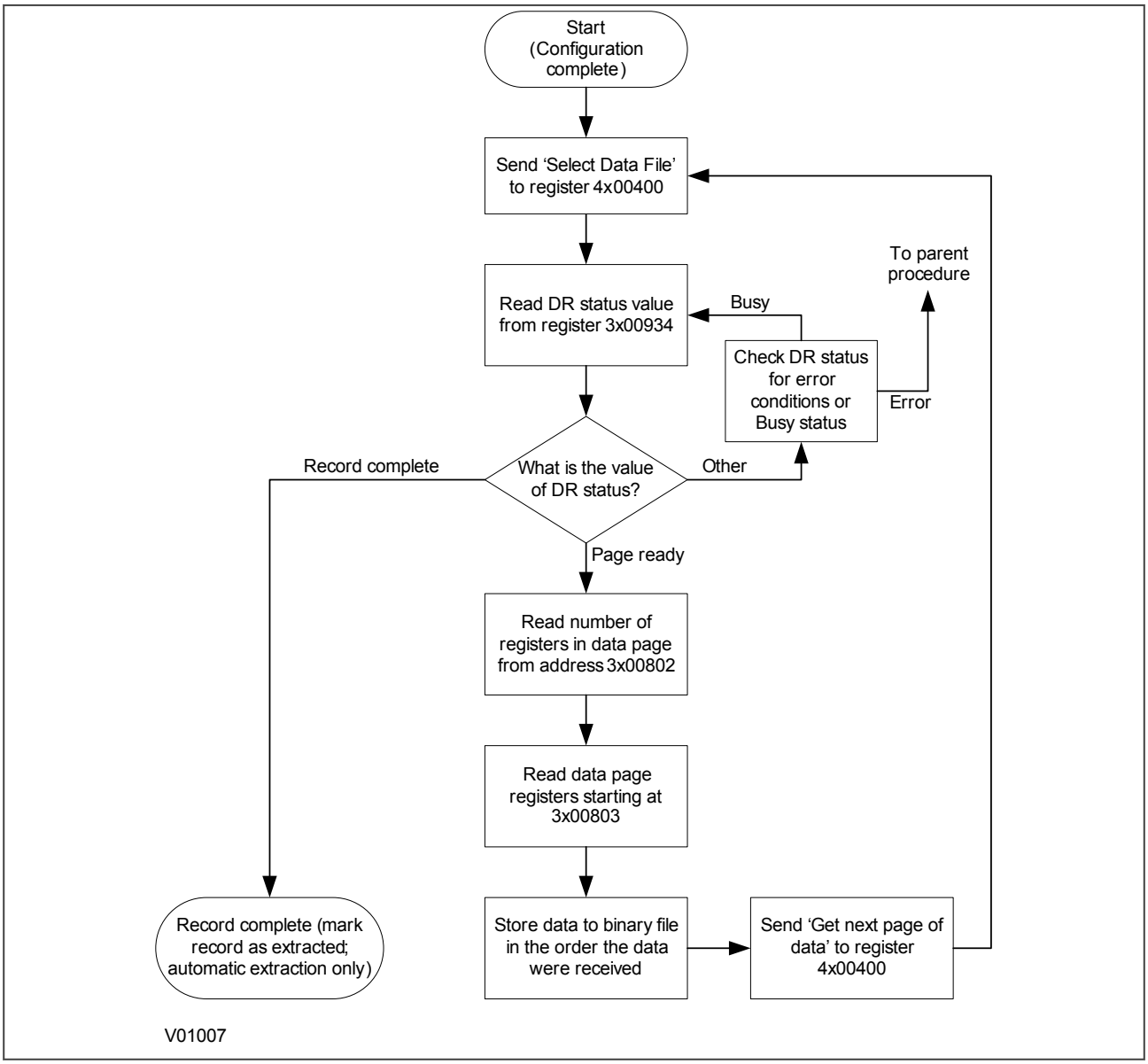


Figure 200: Data file extraction

During the extraction of the COMTRADE files, an error may occur, which will be reported on the DR Status register 3x00934. In this case, you must take action to re-start the record extraction or to abort according to the table below.

Value	State	Description
0	Idle	This will be the state reported when no record is selected; such as after power on or after a record has been marked as extracted.
1	Busy	The relay is currently processing data.
2	Page ready	The data page has been populated and the master station can now safely read the data.
3	Configuration complete	All of the configuration data has been read without error.
4	Record complete	All of the disturbance data has been extracted.
5	Disturbance overwritten	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.

Value	State	Description
6	No unextracted disturbances	An attempt was made by the master station to automatically select the next oldest unextracted disturbance when all records have been extracted.
7	Not a valid disturbance	An attempt was made by the master station to manually select a record that did not exist in the relay.
8	Command out of sequence	The master station issued a command to the relay that was not expected during the extraction process.

6.4.7 SETTING CHANGES

All the IED settings are 4xxxx page addresses. The following points should be noted when changing settings:

- Settings implemented using multiple registers must be written to using a multi-register write operation.
- The first address for a multi-register write must be a valid address. If there are unmapped addresses within the range being written to, the data associated with these addresses will be discarded.
- If a write operation is performed with values that are out of range, the illegal data response will be produced. Valid setting values within the same write operation will be executed.
- If a write operation is performed, which attempts to change registers requiring a higher level of password access than is currently enabled then all setting changes in the write operation will be discarded.

6.4.8 PASSWORD PROTECTION

The following registers are available to control password protection:

Function	MODBUS Registers
Password entry	4x00001 to 4x00002 and 4x20000 to 4x20003
Setting to change password level 1 (4 character)	4x00023 to 4x00024
Setting to change password level 1 (8 character)	4x20008 to 4x20011
Setting to change password level 2	4x20016 to 4x20019
Setting to change password level 3	4x20024 to 4x20027
Can be read to indicate current access level	3x00010

6.4.9 PROTECTION AND DISTURBANCE RECORDER SETTINGS

Setting changes to either of these areas are stored in a scratchpad area and will not be used by the IED unless confirmed. Register 40405 can be used either to confirm or abort the setting changes within the scratchpad area.

The IED supports four groups of protection settings. The MODBUS addresses for each of the four groups are repeated within the following address ranges.

- Group 1: 4x1000 - 4x2999
- Group 2: 4x3000 - 4x4999
- Group 3: 4x5000 - 4x6999
- Group 4: 4x7000 - 4x8999

In addition to the basic editing of the protection setting groups, the following functions are provided:

- Default values can be restored to a setting group or to all of the relay settings by writing to register 4x0402.
- It is possible to copy the contents of one setting group to another by writing the source group to register 40406 and the target group to 4x0407.

The setting changes performed by either of the two operations defined above are made to the scratchpad area. These changes must be confirmed by writing to register 4x0405.

The active protection setting groups can be selected by writing to register 40404. An illegal data response will be returned if an attempt is made to set the active group to one that has been disabled.

6.4.10 TIME SYNCHRONISATION

The date-time data type G12 allows *real* date and time information to be conveyed to a resolution of 1 ms. The structure of the data type is compliant with the IEC 60870-5-4 **Binary Time 2a** format.

The seven bytes of the date/time frame are packed into four 16-bit registers and are transmitted in sequence starting from byte 1. This is followed by a null byte, making eight bytes in total.

Register data is usually transmitted starting with the highest-order byte. Therefore byte 1 will be in the high-order byte position followed by byte 2 in the low-order position for the first register. The last register will contain just byte 7 in the high order position and the low order byte will have a value of zero.

G12 date & time data type structure

	Bit Position							
Byte	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	m7	m6	m5	m4	m3	m2	m1	m0
2	m15	m14	m13	m12	m11	m10	m9	m8
3	IV	R	I5	I4	I3	I2	I1	I0
4	SU	R	R	H4	H3	H2	H1	H0
5	W2	W1	W0	D4	D3	D2	D1	D0
6	R	R	R	R	M3	M2	M1	M0
7	R	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Key to table:

- m = milliseconds: 0 to 59,999
- I = minutes: 0 to 59
- H = hours: 0 to 23
- W = day of the week: 1 to 7 starting from Monday
- D = day of the month: 1 to 31
- M = month of the year: 1 to 12 starting from January
- Y = year of the century: 0 to 99
- R = reserved: 0
- SU = summertime: 0 = GMT, 1 = summertime
- IV = invalid: 0 = invalid value, 1 = valid value

Since the range of the data type is only 100 years, the century must be deduced. The century is calculated as the one that will produce the nearest time value to the current date. For example: 30-12-99 is 30-12-1999 when received in 1999 & 2000, but is 30-12-2099 when received in 2050. This technique allows 2 digit years to be accurately converted to 4 digits in a ±50 year window around the current date.

The invalid bit has two applications:

- It can indicate that the date-time information is considered inaccurate, but is the best information available.
- It can indicate that the date-time information is not available.

The summertime bit is used to indicate that summertime (day light saving) is being used and, more importantly, to resolve the alias and time discontinuity which occurs when summertime starts and ends. This is important for the correct time correlation of time stamped records.

The day of the week field is optional and if not calculated will be set to zero.

The concept of time zone is not catered for by this data type and hence by the relay. It is up to the end user to determine the time zone. Normal practice is to use UTC (universal co-ordinated time).

6.4.11 POWER AND ENERGY MEASUREMENT DATA FORMATS

The power and energy measurements are available in two data formats:

Data Type G29: an integer format using 3 registers

Data Type G125: a 32 bit floating point format using 2 registers

The G29 registers are listed in the first part of the *MEASUREMENTS 2* column of the Courier database. The G125 equivalents appear at the end of the *MEASUREMENTS 2* column.

Data type G29

Data type G29 consists of three registers:

The first register is the per unit (or normalised) power or energy measurement. It is a signed 16 bit quantity. This register is of Data Type G28.

The second and third registers contain a multiplier to convert the per unit value to a real value. These are unsigned 32-bit quantities. These two registers together are of Data Type G27.

Thee overall power or energy value conveyed by the G29 data type is therefore G29 = G28 x G27.

The IED calculates the G28 per unit power or energy value as:

G28 = (measured secondary quantity/CT *secondary)(110V/(VT secondary).*

Since data type G28 is a signed 16-bit integer, its dynamic range is constrained to +/- 32768. You should take this limitation into consideration for the energy measurements, as the G29 value will saturate a long time before the equivalent G125 does.

The associated G27 multiplier is calculated as:

G27 = (CT primary)(VT primary/110V) when primary value measurements are selected

and

G27 = (CT secondary)(VT secondary/110V) when secondary value measurements are selected.

Due to the required truncations from floating point values to integer values in the calculations of the G29 component parts and its limited dynamic range, we only recommend using G29 values when the MODBUS master cannot deal with the G125 IEEE754 floating point equivalents.

> *Note:*
> *The G29 values must be read in whole multiples of three registers. It is not possible to read the G28 and G27 parts with separate read commands.*

Example of Data Type G29

Assuming the CT/VT configurations are as follows:

- Main VT Primary 6.6 kV
- Main VT Secondary 110 V
- Phase CT Primary 3150 A
- Phase CT Secondary 1 A

The Three-phase Active Power displayed on the measurement panel on the front display of the IED would be 21.94 MW

The registers related to the Three-phase Active Power are: 3x00327, 3x00328, 3x00329

Register Address	Data read from these registers	Format of the data
3x00327	116	G28
3x00328	2	G27

Register Address	Data read from these registers	Format of the data
3x00329	57928	G27

The Equivalent G27 value = [2^{16} * Value in the address 3x00328 + Value in the address 3x00329] = 216*2 + 57928 = 189000

The Equivalent value of power G29 = G28 * Equivalent G27 =116 * 189000 =21.92 MW

Note:
The above calculated value (21.92 MW) is same as the power value measured on the front panel display.

Data type G125

Data type G125 is a short float IEEE754 floating point format, which occupies 32 bits in two consecutive registers. The high order byte of the format is in the first (low order) register and the low order byte in the second register.

The value of the G125 measurement is as accurate as the IED's ability to resolve the measurement after it has applied the secondary or primary scaling factors. It does not suffer from the truncation errors or dynamic range limitations associated with the G29 data format.

6.4.12 MODBUS CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 protocol***). This is a non settable cell, which shows the chosen communication protocol – in this case `Modbus`.

```
COMMUNICATIONS
RP1 Protocol
Modbus
```

4. Move down to the next cell (***RP1 Address***). This cell controls the Modbus address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. Modbus uses a decimal number between 1 and 247 for the Relay Address. It is important that no two IEDs have the same address.

```
COMMUNICATIONS
RP1 Address
1
```

5. Move down to the next cell (***RP1 InactivTimer***). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

```
COMMUNICATIONS
RP1 Inactivtimer
10.00 mins
```

6. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bits/s, 2400 bits/s, 4800 bits/s, 9600 bits/s, 19200 bits/s and 38400 bits/s. Make sure that the baud rate selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Baud rate
9600 bits/s
```

7. Move down to the next cell (***RP1 Parity***). This cell controls the parity format used in the data frames. The parity can be set to be one of *None*, *Odd* or *Even*. Make sure that the parity format selected on the IED is the same as that set on the master station.

```
COMMUNICATIONS
RP1 Parity
None
```

8. Move down to the next cell (***Modbus IEC Time***). This cell controls the order in which the bytes of information are transmitted. There is a choice of Standard or Reverse. When *Standard* is selected the time format complies with IEC 60870-5-4 requirements such that byte 1 of the information is transmitted first, followed by bytes 2 through to 7. If *Reverse* is selected the transmission of information is reversed.

```
COMMUNICATIONS
Modbus IEC Time
Standard
```

6.5 IEC 61850

This section describes how the IEC 61850 standard is applied to General Electric products. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 61850 standard.

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security that is so essential in substations today.

There are two editions of most parts of the IEC 61850 standard; edition 1 and edition 2. The edition which this product supports depends on the Software Version.

Software Version 70 onwards provides an IEC 61850 Edition 2 compatible implementation.

An additional section detailing the enhancements in edition 2 models is documented later in this chapter, if applicable.

6.5.1 BENEFITS OF IEC 61850

The standard provides:

- Standardised models for IEDs and other equipment within the substation
- Standardised communication services (the methods used to access and exchange data)
- Standardised formats for configuration files
- Peer-to-peer communication

The standard adheres to the requirements laid out by the ISO OSI model and therefore provides complete vendor interoperability and flexibility on the transmission types and protocols used. This includes mapping of data onto

Ethernet, which is becoming more and more widely used in substations, in favour of RS485. Using Ethernet in the substation offers many advantages, most significantly including:

- Ethernet allows high-speed data rates (currently 100 Mbps, rather than tens of kbps or less used by most serial protocols)
- Ethernet provides the possibility to have multiple clients
- Ethernet is an open standard in every-day use
- There is a wide range of Ethernet-compatible products that may be used to supplement the LAN installation (hubs, bridges, switches)

6.5.2 IEC 61850 INTEROPERABILITY

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs, which allows interoperability between products from multiple vendors.

An IEC 61850-compliant device may be interoperable, but this does not mean it is interchangeable. You cannot simply replace a product from one vendor with that of another without reconfiguration. However the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able to integrate a new device very quickly without having to map all of the new data. IEC 61850 brings improved substation communications and interoperability to the end user, at a lower cost.

6.5.3 THE IEC 61850 DATA MODEL

The data model of any IEC 61850 IED can be viewed as a hierarchy of information, whose nomenclature and categorization is defined and standardized in the IEC 61850 specification.

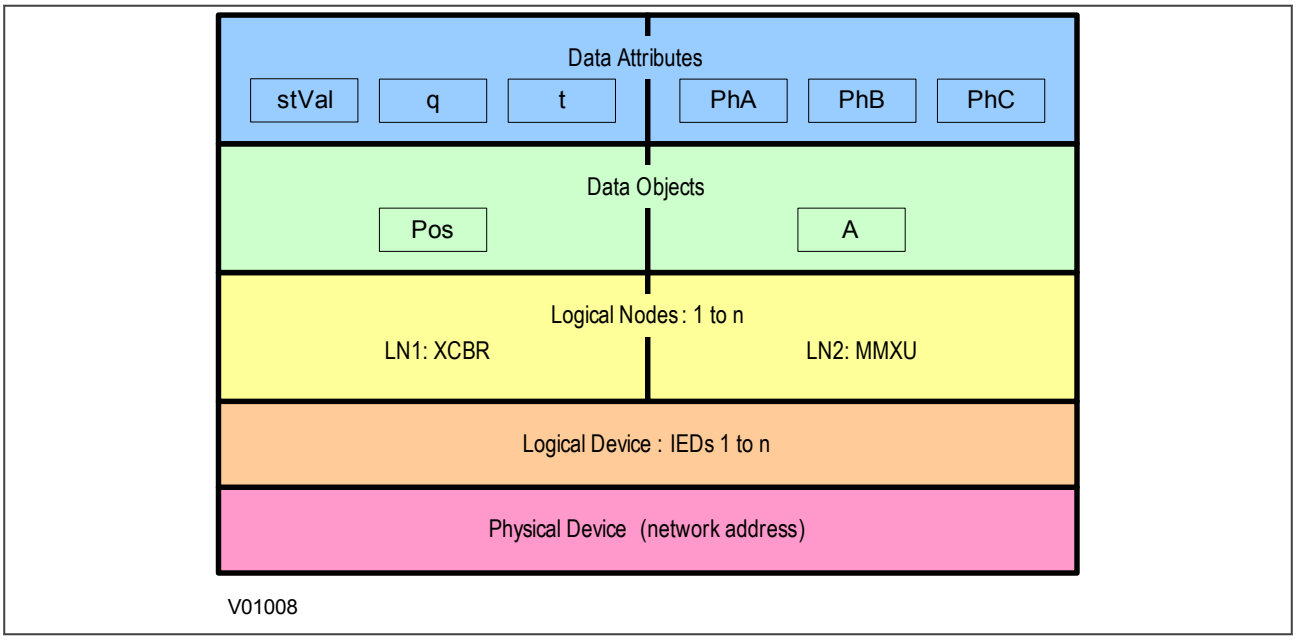


Figure 201: Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

Data Frame format

Layer	Description
Physical Device	Identifies the actual IED within a system. Typically the device's name or IP address can be used (for example Feeder_1 or 10.0.0.2.
Logical Device	Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM IEDs, 5 Logical Devices exist: Control, Measurements, Protection, Records, System.

Layer	Description
Wrapper/Logical Node Instance	Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
Data Object	This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR.
Data Attribute	This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR.

6.5.4 IEC 61850 IN MICOM IEDS

IEC 61850 is implemented by use of a separate Ethernet card. This Ethernet card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection functions.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a bay computer (MiCOM C264)
- An HMI
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge of the IED

The IEC 61850 compatible interface standard provides capability for the following:

- Read access to measurements
- Refresh of all measurements at a standard rate.
- Generation of non-buffered and buffered reports on change of status or measurement
- SNTP time synchronization over an Ethernet link. (This is used to synchronize the IED's internal real time clock.
- GOOSE peer-to-peer communication
- Disturbance record extraction by IEC 61850 MMS file transfer. The record is extracted as an ASCII format COMTRADE file
- Controls (Direct and Select Before Operate)

Note:
Setting changes are not supported in the current IEC 61850 implementation. Currently these setting changes are carried out using the settings application software.

6.5.5 IEC 61850 DATA MODEL IMPLEMENTATION

The data model naming adopted in the IEDs has been standardised for consistency. Therefore the Logical Nodes are allocated to one of the five Logical Devices, as appropriate.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available as a separate document.

6.5.6 IEC 61850 COMMUNICATION SERVICES IMPLEMENTATION

The IEC 61850 communication services which are implemented in the IEDs are described in the Protocol Implementation Conformance Statement (PICS) document, which is available as a separate document.

6.5.7 IEC 61850 PEER-TO-PEER (GOOSE) COMMUNICATIONS

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) enables faster communication between IEDs offering the possibility for a fast and reliable system-wide distribution of input and output data values. The GOOSE model uses multicast services to deliver event information. Multicast messaging means that messages are sent to selected devices on the network. The receiving devices can specifically accept frames from certain devices and discard frames from the other devices. It is also known as a publisher-subscriber system. When a device detects a change in one of its monitored status points it publishes a new message. Any device that is interested in the information subscribes to the data it contains.

6.5.8 MAPPING GOOSE MESSAGES TO VIRTUAL INPUTS

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

An IED can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

6.5.8.1 IEC 61850 GOOSE CONFIGURATION

All GOOSE configuration is performed using the IEC 61850 Configurator tool available in the MiCOM S1 Agile software application.

All GOOSE publishing configuration can be found under the **GOOSE Publishing** tab in the configuration editor window. All GOOSE subscription configuration parameters are under the **External Binding** tab in the configuration editor window.

Settings to enable GOOSE signalling and to apply Test Mode are available using the HMI.

6.5.9 ETHERNET FUNCTIONALITY

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost, and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association, and terminate any which are no longer active.

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

6.5.9.1 ETHERNET DISCONNECTION

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost, and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association, and terminate any which are no longer active.

6.5.9.2 LOSS OF POWER

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

6.5.10 IEC 61850 CONFIGURATION

You cannot configure the device for IEC 61850 edition 1 using the HMI panel on the product. For this you must use the IEC 61850 Configurator, which is part of the settings application software. If the device is compatible with edition 2, however, you can configure it with the HMI. To configure IEC61850 edition 2 using the HMI, you must first enable the IP From HMI setting, after which you can set the media (copper or fibre), IP address, subnet mask and gateway address.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IED's system configuration capabilities are determined from an IED Capability Description file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and test (using simulation tools), a substation's entire protection scheme before the products are installed into the substation.

To help with this process, the settings application software provides an IEC 61850 Configurator tool, which allows the pre-configured IEC 61850 configuration file to be imported and transferred to the IED. As well as this, you can manually create configuration files for all products, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

Note:
Some configuration data is available in the IEC61850 CONFIG. column, allowing read-only access to basic configuration data.

6.5.10.1 IEC 61850 CONFIGURATION BANKS

There are two configuration banks:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the IED is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration.

Following an upgrade, the IEC 61850 Configurator tool can be used to transmit a command, which authorises activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the *IEC61850 CONFIG.* column of the HMI.

The SCL Name and Revision attributes of both configuration banks are available in the *IEC61850 CONFIG.* column of the HMI.

6.5.10.2 IEC 61850 NETWORK CONNECTIVITY

Configuration of the IP parameters and SNTP (Simple Network Time Protocol) time synchronisation parameters is performed by the IEC 61850 Configurator tool. If these parameters are not available using an SCL (Substation Configuration Language) file, they must be configured manually.

Every IP address on the Local Area Network must be unique. Duplicate IP addresses result in conflict and must be avoided. Most IEDs check for a conflict on every IP configuration change and at power up and they raise an alarm if an IP conflict is detected.

The IED can be configured to accept data from other networks using the ***Gateway*** setting. If multiple networks are used, the IP addresses must be unique across networks.

6.5.11 IEC 61850 EDITION 2

Many parts of the IEC 61850 standard have now been released as the second edition. This offers some significant enhancements including:

- Improved interoperability
- Many new logical nodes
- Better defined testing; it is now possible to perform off-line testing and simulation of functions

Edition 2 implementation requires use of version 3.8 of the IEC 61850 configurator, which is installed with version 2.0.1 of MiCOM S1 Agile.

6.5.11.1 BACKWARD COMPATIBILITY

IEC61850 System - Backward compatibility

An Edition 1 IED can operate with an Edition 2 IEC 61850 system, provided that the Edition 1 IEDs do not subscribe to GOOSE messages with data objects or data attributes which are only available in Edition 2.

The following figure explains this concept:

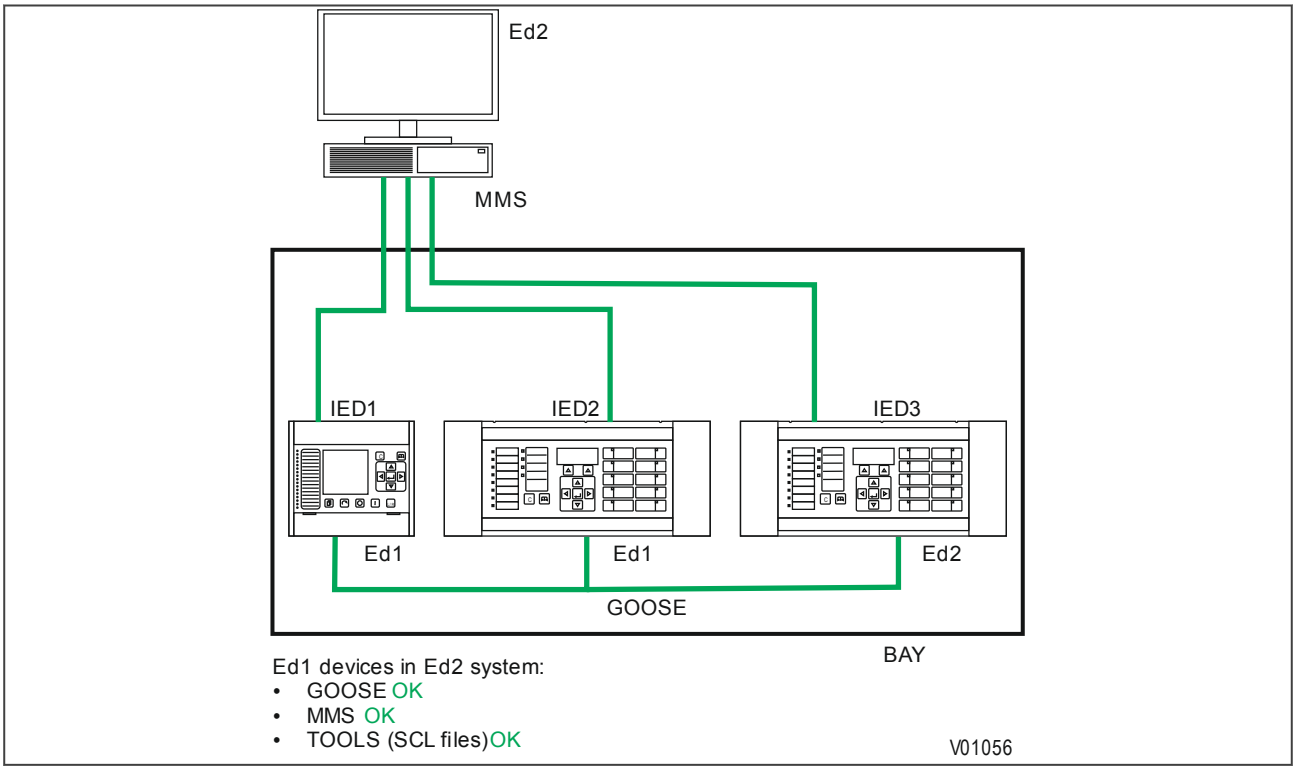


Figure 202: Edition 2 system - backward compatibility

An Edition 2 IED cannot normally operate within an Edition 1 IEC 61850 system. An Edition 2 IED can work for GOOSE messaging in a mixed system, providing the client is compatible with Edition 2.

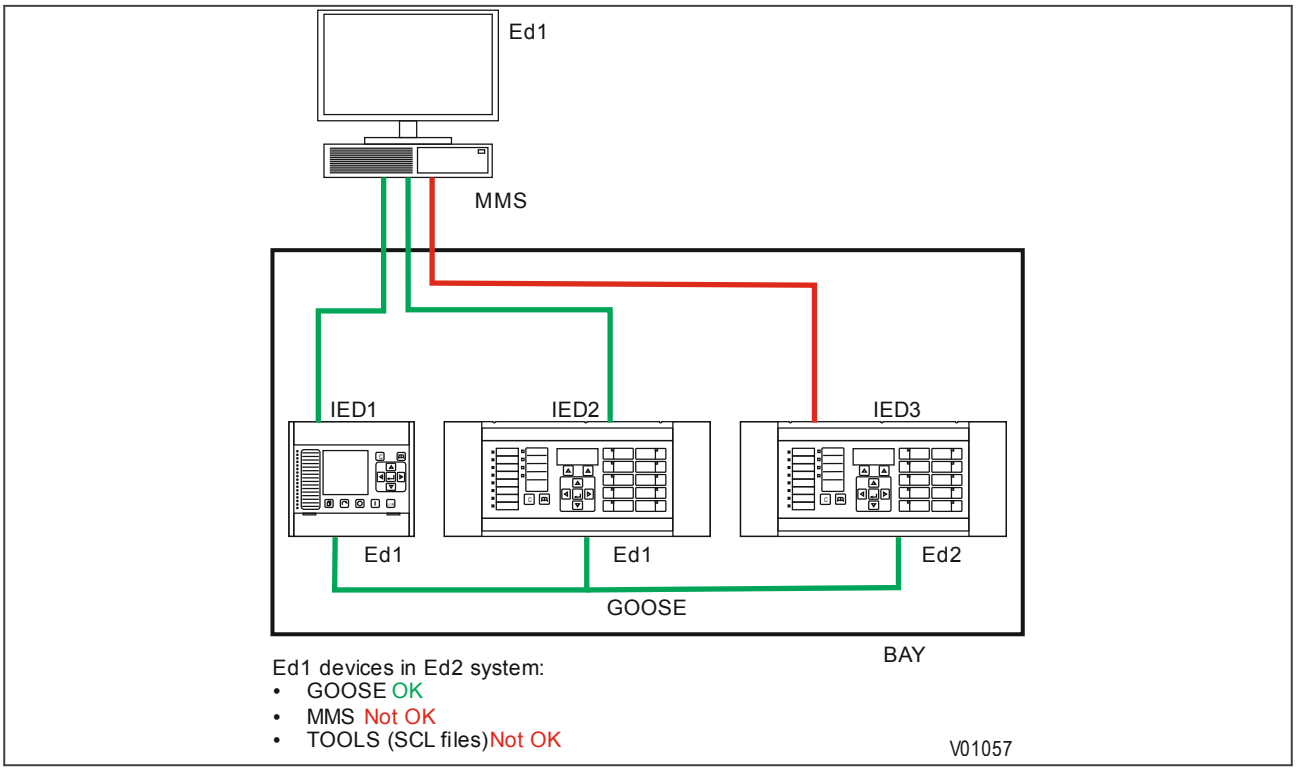


Figure 203: Edition 1 system - forward compatibility issues

6.5.11.2 EDITION-2 COMMON DATA CLASSES

The following common data classes (CDCs) are new to Edition 2 and therefore should not be used in GOOSE control blocks in mixed Edition 1 and Edition 2 systems

- Histogram (HST)
- Visible string status (VSS)
- Object reference setting (ORG)
- Controllable enumerated status (ENC)
- Controllable analogue process value (APC)
- Binary controlled analogue process value (BAC)
- Enumerated status setting (ENG)
- Time setting group (TSG)
- Currency setting group (CUG)
- Visible string setting (VSG)
- Curve shape setting (CSG)

Of these, only ENS and ENC types are available from a MiCOM P40 IED when publishing GOOSE messages, so Data Objects using these Common Data Classes should not be published in mixed Edition 1 and Edition 2 systems.

For compatibility between Edition 1 and Edition 2 IEDs, SCL files using SCL schema version 2.1 must be used. For a purely Edition 2 system, use the schema version 3.1.

6.5.11.3 STANDBY PROTECTION REDUNDANCY

With digital substation architectures, measurements can be shared freely on the process bus across the substation and between different devices without any additional wiring. This is because there are no longer any electrical connections to instruments transformers that restrict the location of IEDs.

The new IEC 61850 Edition 2 test modes enable the introduction of standby protection IEDs at any location within the substation, which has access to both station and process buses. In the case of failure, these devices can temporarily replace the protection functions inside other IEDs.

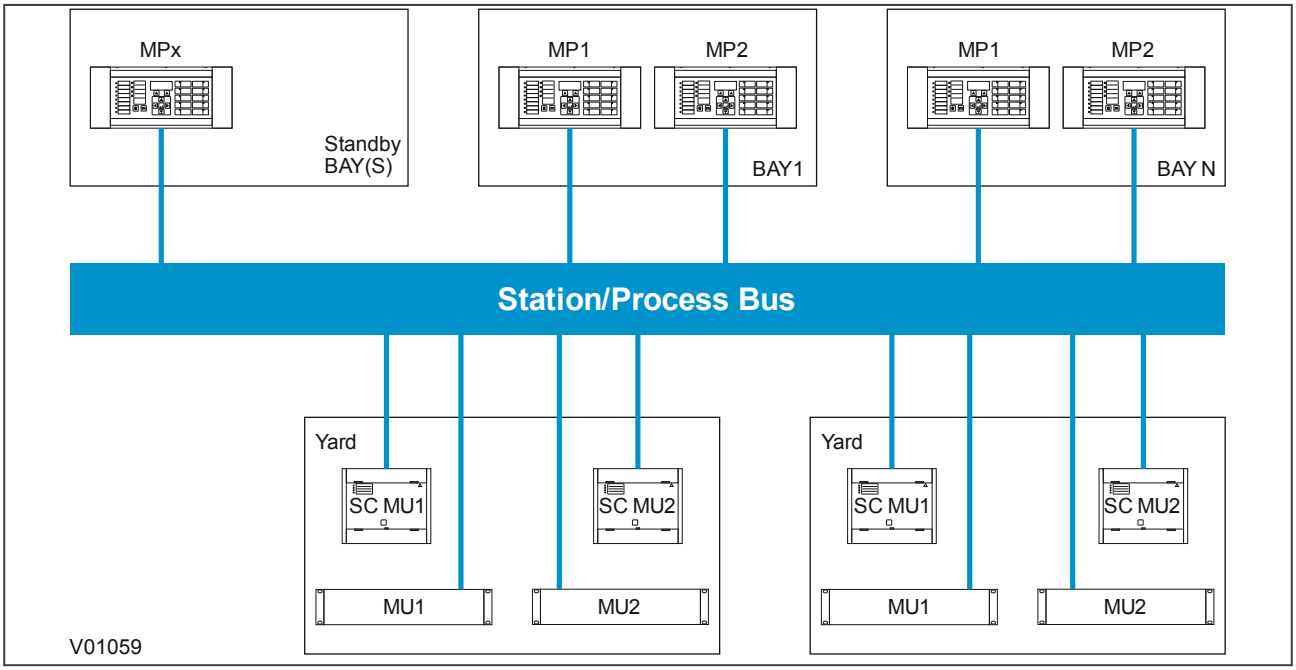


Figure 204: Example of Standby IED

See the example below. If a failure occurs in the Bay 1 protection IED (MP2), we could disable this device and activate a standby protection IED to replace its functionality.

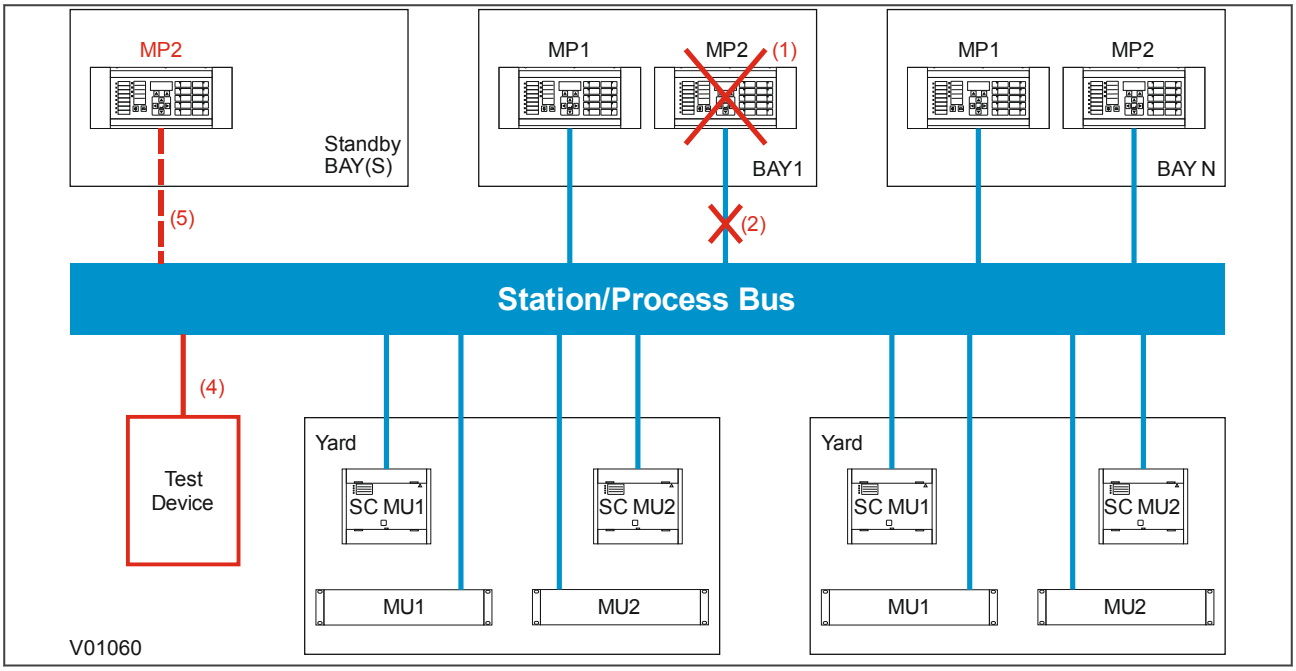


Figure 205: Standby IED Activation Process

The following sequence would occur under this scenario:

1. During the installation phase, a spare standby IED is installed in the substation. This can remain inactive, until it is needed to replace functions in one of several bays. The device is connected to the process bus, but does not have any subscriptions enabled.
2. If a failure occurs (in this example, bay 1), first isolate the faulty device by disabling its process bus and station bus interfaces. You do this by turning off the attached network interfaces.
3. Retrieve the configuration that the faulty device normally uses, and load this into the standby redundant IED.
4. Place the IED into the "Test Blocked" mode, as defined in IEC 61850-7-4 Edition Two. This allows test signals to be injected into the network, which will check that the configuration is correct. GOOSE signals issued by the device will be flagged as "test" so that subscribing switchgear controllers know not to trip during this testing. In this way the protection can be tested all the way up to the switchgear control merging units without having to operate primary circuit breakers, or by carrying out any secondary injection.
5. Take the standby IED out of "Test-Blocked" mode and activate it so that it now replaces the protection functions that were disabled from the initial device failure.

The standby IED reduces downtime in the case of device failure, as protection functions can be restored quickly before the faulted device is replaced.

6.6 CONCURRENT IEC 61850 AND DNP3.0 OPERATION

No Redundancy

Simultaneous IEC 61850 and DNP3.0 operation may be achieved using single or dual IP addresses.

Where concurrent IEC61850 & DNP3 uses a dual IP address configuration (defined via ordering option), Port A is dedicated to IEC 61850 (configured with or without SNTP), and Port B is dedicated to DNP3.0. Configuration settings are applied via IED Configurator Communications and DNP Over Ethernet Settings respectively. In this case, no Redundancy option is available.

Note:
SNTP may only be configured via the IED Configurator tool.

Note:
When concurrent IEC61850 & DNP3 uses a dual IP address configuration, the Redundancy list in the IED Configurator tool is visible but ineffective.

Where concurrent IEC61850 & DNP3 uses a single IP address setup with no redundancy required, configuration settings are applied via the IED Configurator and DNP3 settings respectively, with Redundancy set to NONE.

With Redundancy

Simultaneous IEC 61850 and DNP3.0 with FAILOVER, RSTP, PRP or HSP Redundancy is only possible where concurrent IEC61850 & DNP3 uses a single IP address. With Redundancy set to FAILOVER, either Port A or B may be selected, but when set to RSTP, PRP or HSR redundancy protocols, IEC 61850 and DNP3.0 communications (configured with or without SNTP) no port is specified.

Note:
Redundancy and SNTP may only be configured via the IED Configurator tool.

Note:
The IP address, Subnet and Gateway may be set with either configuration tool, (IED Configurator Communications or DNP3 Over Ethernet settings), but only the last values sent will be configured, as only one IP address/Subnet/Gateway is used in a single IP Address setup. It is therefore recommended that the same IP address is entered into both configuration tools.

To confirm the network interface protocol is set to concurrent IEC 61850 and DNP3, navigate to the device's *COMMUNICATIONS* column and check that ***NIC Protocol*** is set to *IEC61850 & DNP3*:

```
COMMUNICATIONS
NIC Protocol
IEC61850 & DNP3
```

To confirm the IP address setting for IEC 61850, navigate to the Device's *IEC61850 CONFIG.* column and check the ***IP Address*** setting:

```
IEC61850 CONFIG.
IP Address
192.168.1.1
```

To confirm the IP address setting for DNP, navigate to the Device's *DNP SETTINGS* column and check the ***IP Address*** setting:

```
DNP SETTINGS
IP Address
192.168.1.1
```

Note:
It is recommended that a maximum of two communication protocols are configured to operate concurrently.

7 READ ONLY MODE

With IEC 61850 and Ethernet/Internet communication capabilities, security has become an important issue. For this reason, all relevant General Electric IEDs have been adapted to comply with the latest cyber-security standards.

In addition to this, a facility is provided which allows you to enable or disable the communication interfaces. This feature is available for products using Courier, IEC 60870-5-103, or IEC 61850.

7.1 IEC 60870-5-103 PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with IEC 60870-5-103, the following commands are blocked at the interface:

- Write parameters (=change setting) (private ASDUs)
- General Commands (ASDU20), namely:
  - INF16 auto-recloser on/off
  - INF19 LED reset
  - Private INFs (for example: CB open/close, Control Inputs)

The following commands are still allowed:

- Poll Class 1 (Read spontaneous events)
- Poll Class 2 (Read measurands)
- GI sequence (ASDU7 'Start GI', Poll Class 1)
- Transmission of Disturbance Records sequence (ASDU24, ASDU25, Poll Class 1)
- Time Synchronisation (ASDU6)
- General Commands (ASDU20), namely:
  - INF23 activate characteristic 1
  - INF24 activate characteristic 2
  - INF25 activate characteristic 3
  - INF26 activate characteristic 4

Note:
For IEC 60870-5-103, Read Only Mode function is different from the existing Command block feature.

7.2 COURIER PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with Courier, the following commands are blocked at the interface:

- Write settings
- All controls, including:Reset Indication (Trip LED)
  - Operate Control Inputs
  - CB operations
  - Auto-reclose operations
  - Reset demands
  - Clear event/fault/maintenance/disturbance records
  - Test LEDs & contacts

The following commands are still allowed:

- Read settings, statuses, measurands
- Read records (event, fault, disturbance)
- Time Synchronisation
- Change active setting group

7.3 IEC 61850 PROTOCOL BLOCKING

If Read-Only Mode is enabled for the Ethernet interfacing with IEC 61850, the following commands are blocked at the interface:

- All controls, including:
  - Enable/disable protection
  - Operate Control Inputs
  - CB operations (Close/Trip, Lock)
  - Reset LEDs

The following commands are still allowed:

- Read statuses, measurands
- Generate reports
- Extract disturbance records
- Time synchronisation
- Change active setting group

7.4 READ-ONLY SETTINGS

The following settings are available for enabling or disabling Read Only Mode.

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

7.5 READ-ONLY DDB SIGNALS

The remote read only mode is also available in the PSL using three dedicated DDB signals:

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

Using the PSL, these signals can be activated by opto-inputs, Control Inputs and function keys if required.

8 TIME SYNCHRONISATION

In modern protection schemes it is necessary to synchronise the IED's real time clock so that events from different devices can be time stamped and placed in chronological order. This is achieved in various ways depending on the chosen options and communication protocols.

- Using the IRIG-B input (if fitted)
- Using the SNTP time protocol (for Ethernet IEC 61850 versions + DNP3 OE)
- By using the time synchronisation functionality inherent in the data protocols

8.1 DEMODULATED IRIG-B

IRIG stands for Inter Range Instrumentation Group, which is a standards body responsible for standardising different time code formats. There are several different formats starting with IRIG-A, followed by IRIG-B and so on. The letter after the "IRIG" specifies the resolution of the time signal in pulses per second (PPS). IRIG-B, the one which we use has a resolution of 100 PPS. IRIG-B is used when accurate time-stamping is required.

The following diagram shows a typical GPS time-synchronised substation application. The satellite RF signal is picked up by a satellite dish and passed on to receiver. The receiver receives the signal and converts it into time signal suitable for the substation network. IEDs in the substation use this signal to govern their internal clocks and event recorders.

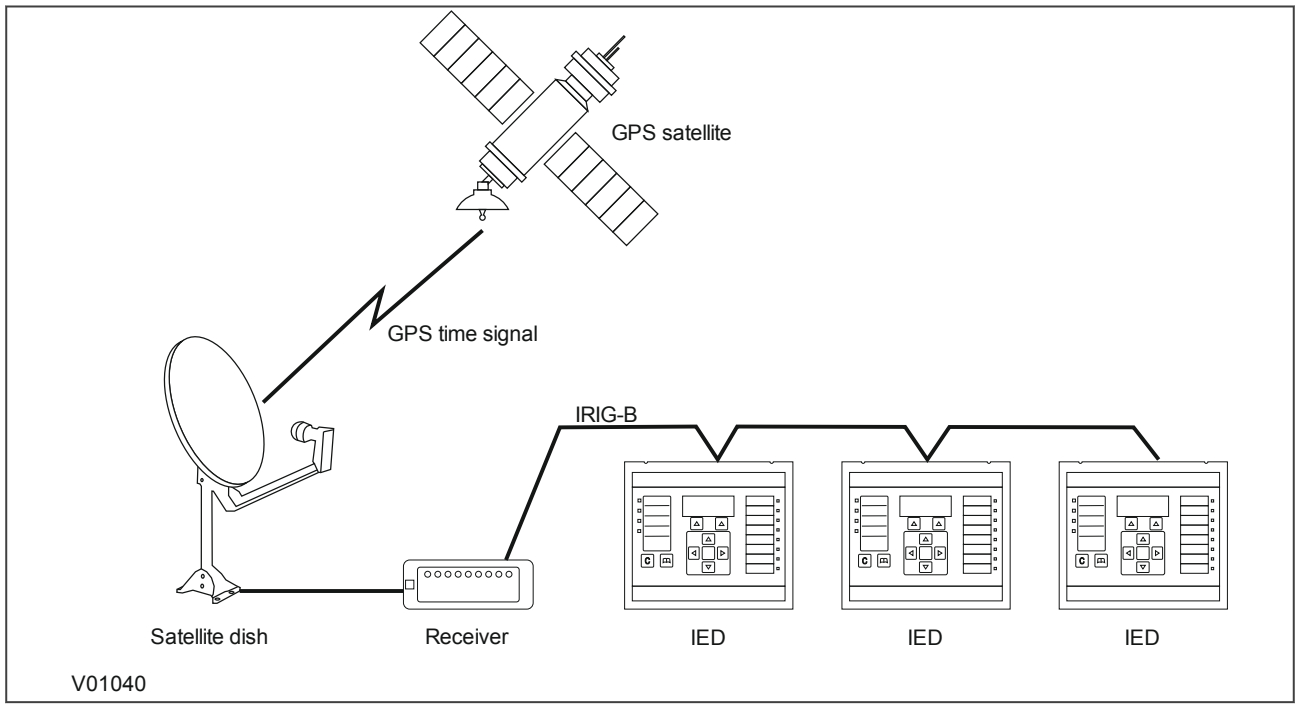


Figure 206: GPS Satellite timing signal

The IRIG-B time code signal is a sequence of one second time frames. Each frame is split up into ten 100 mS slots as follows:

- Time-slot 1: Seconds
- Time-slot 2: Minutes
- Time-slot 3: Hours
- Time-slot 4: Days
- Time-slot 5 and 6: Control functions
- Time-slots 7 to 10: Straight binary time of day

The first four time-slots define the time in BCD (Binary Coded Decimal). Time-slots 5 and 6 are used for control functions, which control deletion commands and allow different data groupings within the synchronisation strings. Time-slots 7-10 define the time in SBS (Straight Binary Second of day).

8.1.1 DEMODULATED IRIG-B IMPLEMENTATION

All models have the option of accepting a demodulated IRIG-B input. This is a hardware option and it uses the same terminals as the RP1 (or RP2 if applicable) inputs. You cannot have IRIG-B and a serial port in the same slot. This means 20Te models cannot have both IRIG-B time synchronisation and serial communications capability. For 30TE and 40TE models however, it is possible to have IRIG-B in one slot and a serial port in another, provided this option is ordered.

To set the device to use IRIG-B, use the setting ***IRIG-B Sync*** cell in the *DATE AND TIME* column. This can be set to `None` (for no IRIG-B), `RP1` (for the option where IRIG-B uses terminals 54 and 56) and `RP2` (for the option where IRIG-B uses terminals 82 and 84)

The IRIG-B status can be viewed in the ***IRIG-B Status*** cell in the *DATE AND TIME* column.

8.2 SNTP

SNTP is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. SNTP can be used as the time synchronisation method for models using IEC 61850 over Ethernet.

The device is synchronised by the main SNTP server. This is achieved by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software described in the settings application software manual. A second server is also configured with a different IP address for backup purposes.

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. This could be because there is no response or no valid clock signal.

The HMI menu does not contain any configurable settings relating to SNTP, as the only way to configure it is using the IEC 61850 Configurator. However it is possible to view some parameters in the *COMMUNICATIONS* column under the sub-heading SNTP parameters. Here you can view the SNTP server addresses and the SNTP poll rate in the cells ***SNTP Server 1***, ***SNTP Server 2*** and ***SNTP Poll rate*** respectively.

The SNTP time synchronisation status is displayed in the ***SNTP Status*** cell in the *DATE AND TIME* column.

8.2.1 LOSS OF SNTP SERVER SIGNAL ALARM

This function issues an alarm when there is a loss of time synchronization on the SNTP server. It is issued when the SNTP sever has not detected a valid time synchronisation response within its 5 second window. This is because there is no response or no valid clock. The alarm is mapped to IEC 61850.

8.3 TIME SYNCHRONISATION USING THE COMMUNICATION PROTOCOLS

All communication protocols have in-built time synchronisation mechanisms. If an external time synchronisation mechanism such as IRIG-B, SNTP, or IEEE 1588 PTP is not used to synchronise the devices, the time synchronisation mechanism within the relevant serial protocol is used. The real time is usually defined in the master station and communicated to the relevant IEDs via one of the rear serial ports using the chosen protocol. It is also possible to define the time locally using settings in the *DATE AND TIME* column.

The time synchronisation for each protocol is described in the relevant protocol description section.

CHAPTER 18

CYBER-SECURITY

1 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were often proprietary.

For these reasons, the substation environment was very secure against cyber-attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it cannot be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them).

The increasing sophistication of protection schemes, coupled with the advancement of technology and the desire for vendor interoperability, has resulted in standardisation of networks and data interchange within substations. Today, devices within substations use standardised protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardised protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for our range of Intelligent Electronic Devices (IEDs).

Note:
Cyber-security compatible devices do not enforce NERC compliance, they merely facilitate it. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary.

This chapter contains the following sections:

2 THE NEED FOR CYBER-SECURITY

Cyber-security provides protection against unauthorised disclosure, transfer, modification, or destruction of information or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorised access to information)
- Integrity (preventing unauthorised modification)
- Availability / Authentication (preventing the denial of service and assuring authorised access to information)
- Non-repudiation (preventing the denial of an action that took place)
- Traceability / Detection (monitoring and logging of activity to detect intrusion and analyse incidents)

The threats to cyber-security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber-attacks by hackers).

Good cyber-security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (users keep passwords on their computer)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Bypassing of controls (users turn off security measures)
- Inadequate technology (substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate preventing access to equipment

To help tackle these issues, standards organisations have produced various standards. Compliance with these standards significantly reduces the threats associated with lack of cyber-security.

3 STANDARDS

There are several standards, which apply to substation cyber-security. The standards currently applicable to General Electric IEDs are NERC and IEEE1686.

Standard	Country	Description
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber-security capabilities
IEC 62351	International	Power system data and Comm. protocol
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber-security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

3.1 NERC COMPLIANCE

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of 'Critical Cyber Assets', which control or have an influence on the reliability of North America's electricity generation and distribution systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

NERC CIP standards

CIP standard	Description
CIP-002-1 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003-1 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004-1 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005-1 Electronic Security	Define and document logical security perimeters where Critical Cyber Assets reside. Define and document measures to control access points and monitor electronic access
CIP-006-1 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside
CIP-007-1 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets
CIP-008-1 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber-security Incidents relating to Critical Cyber Assets are identified
CIP-009-1 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

3.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up

Power utility responsibilities:	General Electric's contribution:
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

3.1.2 CIP 003

CIP 003 requires the implementation of a cyber-security policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

Power utility responsibilities:	General Electric's contribution:
To create a Cyber-security Policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

3.1.3 CIP 004

CIP 004 requires that personnel with authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power utility responsibilities:	General Electric's contribution:
To provide appropriate training of its personnel	We can provide cyber-security training

3.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power utility responsibilities:	General Electric's contribution:
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED

3.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power utility responsibilities:	General Electric's contribution:
Provide physical security controls and perimeter monitoring. Ensure that people who have access to critical cyber assets don't have criminal records.	General Electric cannot provide additional help with this aspect.

3.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring
- An annual vulnerability assessment should be performed

Power utility responsibilities:	General Electric's contribution:
To provide an incident response team and have appropriate processes in place	Test procedures, we can provide advice and help on testing. Ports and services, our devices can disable unused ports and services Security patch management, we can provide assistance Antivirus, we can provide advise and assistance Account management, we can provide advice and assistance Monitoring, our equipment monitors and logs access

3.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power utility responsibilities:	General Electric's contribution:
To provide an incident response team and have appropriate processes in place.	General Electric cannot provide additional help with this aspect.

3.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power utility responsibilities:	General Electric's contribution:
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

3.2 IEEE 1686-2013

IEEE 1686-2013 is an IEEE Standard for substation IEDs' cyber-security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.

- IED functions and features are assigned to different password levels. The assignment is fixed.
- The audit trail is recorded, listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

4 CYBER-SECURITY IMPLEMENTATION

The General Electric IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

This section describes the current implementation of cyber-security. This is valid for the release of platform software to which this manual pertains. This current cyber-security implementation is known as Cyber-security Phase 1.

At the IED level, these cyber-security measures have been implemented:

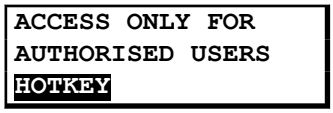
- NERC-compliant default display
- Four-level access
- Enhanced password security
- Password recovery procedure
- Disabling of unused physical and logical ports
- Inactivity timer
- Security events management

External to the IEDs, the following cyber-security measures have been implemented:

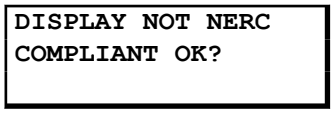
- Antivirus
- Security patch management

4.1 NERC-COMPLIANT DISPLAY

For the device to be NERC-compliant, it must provide the option for a NERC-compliant default display. The default display that is implemented in our cyber-security concept contains a warning that the IED can be accessed by authorised users. You can change this if required with the ***User Banner*** setting in the *SECURITY CONFIG* column.



If you try to change the default display from the NERC-compliant one, a further warning is displayed:



The default display navigation map shows how NERC-compliance is achieved with the product's default display concept.

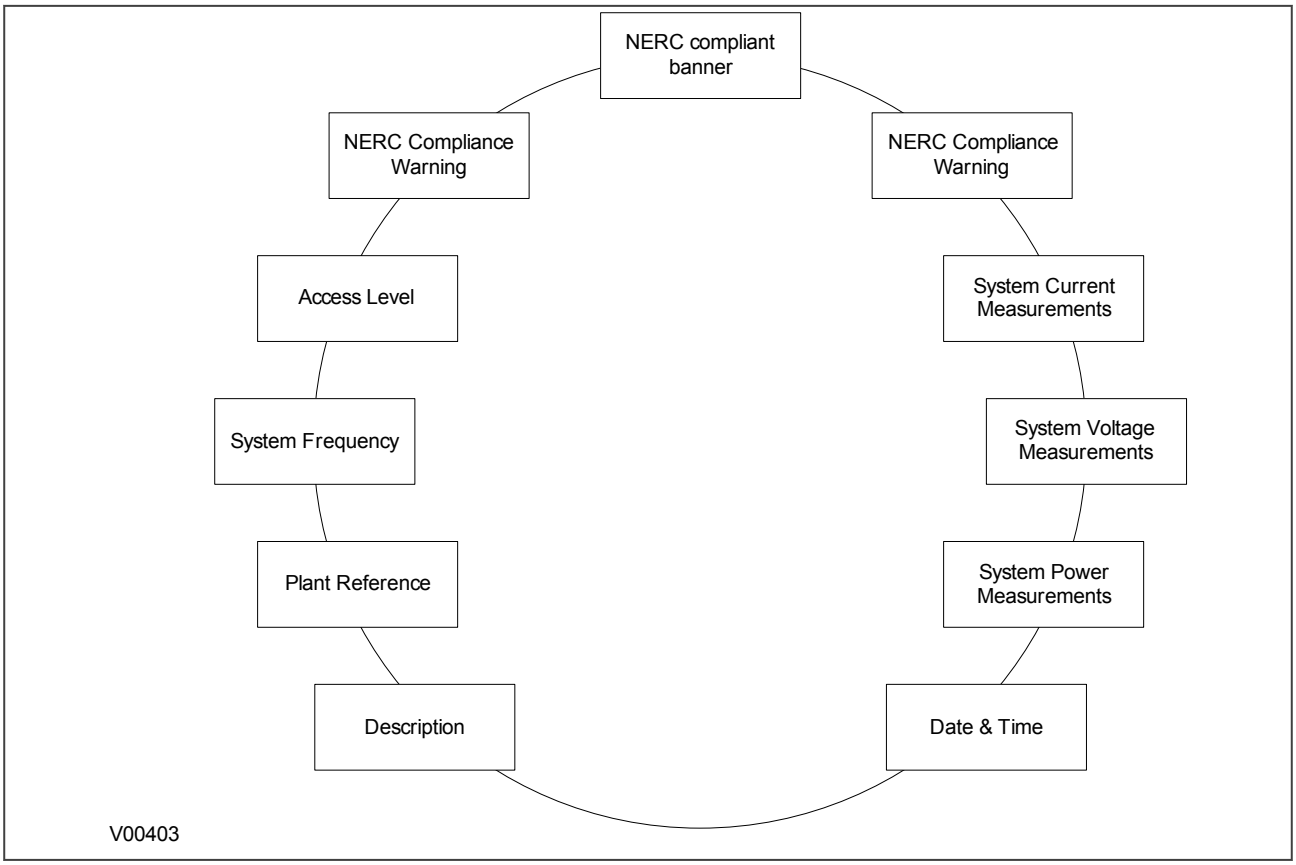


Figure 207: Default display navigation

4.2 FOUR-LEVEL ACCESS

The menu structure contains four levels of access, three of which are password protected.

Password levels

Level	Meaning	Read Operation	Write Operation
0	Read Some Write Minimal	SYSTEM DATA column: Description Plant Reference Model Number Serial Number S/W Ref. Access Level Security Feature SECURITY CONFIG column: User Banner Attempts Remain Blk Time Remain Fallback PW level Security Code (UI only)	Password Entry LCD Contrast (UI only)
1	Read All Write Few	All data and settings are readable. Poll Measurements	All items writeable at level 0. Level 1 Password setting Extract Disturbance Record Select Event, Main and Fault (upload) Extract Events (e.g. via MiCOM S1 Studio)

Level	Meaning	Read Operation	Write Operation
2	Read All Write Some	All data and settings are readable. Poll Measurements	All items writeable at level 1. Setting Cells that change visibility (Visible/Invisible). Setting Values (Primary/Secondary) selector Commands: Reset Indication Reset Demand Reset Statistics Reset CB Data / counters Level 2 Password setting
3	Read All Write All	All data and settings are readable. Poll Measurements	All items writeable at level 2. Change all Setting cells Operations: Extract and download Setting file. Extract and download PSL Extract and download MCL61850 (IEC61850 CONFIG) Auto-extraction of Disturbance Recorder Courier/Modbus Accept Event (auto event extraction, e.g. via A2R) Commands: Change Active Group setting Close / Open CB Change Comms device address. Set Date & Time Switch MCL banks / Switch Conf. Bank in UI (IEC61850 CONFIG) Enable / Disable Device ports (in SECURITY CONFIG column) Level 3 password setting

4.2.1 BLANK PASSWORDS

A blank password is effectively a zero-length password. Through the front panel it is entered by confirming the password entry without actually entering any password characters. Through a communications port the Courier and Modbus protocols each have a means of writing a blank password to the IED. A blank password disables the need for a password at the level that this password is applied.

Blank passwords have a slightly different validation procedure. If a blank password is entered through the front panel, the following text is displayed, after which the procedure is the same as already described:

```
BLANK PASSWORD
ENTERED CONFIRM
```

Blank passwords cannot be configured if the lower level password is not blank.

Blank passwords affect the fall back level after inactivity timeout or logout.

The ‘fallback level’ is the password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest-level password that is blank, or level 0 if no passwords are blank.

4.2.2 PASSWORD RULES

- Default passwords are blank for Level 1 and are AAAA for Levels 2 and 3
- Passwords may be any length between 0 and 8 characters long
- Passwords may or may not be NERC compliant
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- Only one password is required for all the IED interfaces

4.2.3 ACCESS LEVEL DDBS

In addition to having the 'Access level' cell in the 'System data' column (address 00D0), the current level of access for each interface is also available for use in the Programming Scheme Logic (PSL) by mapping to these Digital Data Bus (DDB) signals:

- ***HMI Access Lvl 1***
- ***HMI Access Lvl 2***
- ***HMI Access Lvl 3***
- ***FPort AccessLvl1***
- ***FPort AccessLvl2***
- ***FPort AccessLvl3***
- ***RPrt1 AccessLvl1***
- ***RPrt1 AccessLvl2***
- ***RPrt1 AccessLvl3***
- ***RPrt2 AccessLvl1***
- ***RPrt2 AccessLvl2***
- ***RPrt2 AccessLvl3***

Key:

HMI = Human Machine Interface

FPort = Front Port

RPrt = Rear Port

Lvl = Level

4.3 ENHANCED PASSWORD SECURITY

Cyber-security requires strong passwords and validation for NERC compliance.

4.3.1 PASSWORD STRENGTHENING

NERC compliant passwords have the following requirements:

- At least one upper-case alpha character
- At least one lower-case alpha character
- At least one numeric character
- At least one special character (%,$...)
- At least six characters long

4.3.2 PASSWORD VALIDATION

The IED checks for NERC compliance. If the password is entered through the front panel, this is briefly displayed on the LCD.

If the entered password is NERC compliant, the following text is displayed.

```
NERC COMPLIANT
P/WORD WAS SAVED
```

If the password entered is not NERC-compliant, the user is required to actively confirm this, in which case the non-compliance is logged.

If the entered password is not NERC compliant, the following text is displayed:

```
NERC COMPLIANCE
NOT MET CONFIRM?
```

On confirmation, the non-compliant password is stored and the following acknowledgement message is displayed for 2 seconds.

```
NON-NERC P/WORD
SAVED OK
```

If the action is cancelled, the password is rejected and the following message is displayed for 2 seconds.

```
NON-NERC P/WORD
NOT SAVE
```

If the password is entered through a communications port using Courier or Modbus protocols, the device will store the password, irrespective of whether it is NERC-compliant or not. It then uses appropriate response codes to inform the client of the NERC-compliancy status. You can then choose to enter a new NERC-compliant password or accept the non-NERC compliant password just entered.

4.3.3 PASSWORD BLOCKING

You are locked out temporarily, after a defined number of failed password entry attempts. Each invalid password entry attempt decrements the 'Attempts Remain' data cell by 1. When the maximum number of attempts has been reached, access is blocked. If the attempts timer expires, or the correct password is entered *before* the 'attempt count' reaches the maximum number, then the 'attempts count' is reset to 0.

An attempt is only counted if the attempted password uses only characters in the valid range, but the attempted password is not correct (does not match the corresponding password in the IED). Any attempt where one or more characters of the attempted password are not in the valid range will not be counted.

Once the password entry is blocked, a 'blocking timer' is started. Attempts to access the interface while the 'blocking timer' is running results in an error message, irrespective of whether the correct password is entered or not. Once the 'blocking timer' has expired, access to the interface is unblocked and the attempts counter is reset to zero.

If you try to enter the password while the interface is blocked, the following message is displayed for 2 seconds.

```
NOT ACCEPTED
ENTRY IS BLOCKED
```

A similar response occurs if you try to enter the password through a communications port.

The parameters can then be configured using the ***Attempts Limit***, ***Attempts Timer*** and ***Blocking Timer*** settings in the *SECURITY CONFIG* column.

Password blocking configuration

Setting	Cell col row	Units	Default Setting	Available Setting
Attempts Limit	25 02		3	0 to 3 step 1
Attempts Timer	25 03	Minutes	2	1 to 3 step 1
Blocking Timer	25 04	Minutes	5	1 to 30 step 1

4.4 PASSWORD RECOVERY

If you mislay a device's password, they can be recovered. To obtain the recovery password you must contact the Contact Centre and supply the Serial Number and its Security Code. The Contact Centre will use these items to generate a Recovery Password.

The security code is a 16-character string of upper case characters. It is a read-only parameter. The device generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

As soon as the security code is displayed on the LCD, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the contact centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the contact centre over weekends and bank holidays.

To prevent accidental reading of the IED security code, the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

The security code is displayed on confirmation. The validity timer is then started. The security code can only be read from the front panel.

4.4.1 ENTRY OF THE RECOVERY PASSWORD

The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.

Entry of the recovery password causes the IED to reset all passwords back to default. This is all it is designed to do. After the passwords have been set back to default, it is up to the user to enter new passwords. Each password should be appropriate for its intended function, ensuring NERC compliance, if required.

On this action, the following message is displayed:

```
PASSWORDS HAVE
BEEN SET TO
DEFAULT
```

The recovery password can be applied through any interface, local or remote. It will achieve the same result irrespective of which interface it is applied through.

4.4.2 PASSWORD ENCRYPTION

The IED supports encryption for passwords entered remotely. The encryption key can be read from the IED through a specific cell available only through communication interfaces, not the front panel. Each time the key is read the IED generates a new key that is valid only for the next password encryption write. Once used, the key is invalidated and a new key must be read for the next encrypted password write. The encryption mechanism is otherwise transparent to the user.

4.5 DISABLING PHYSICAL PORTS

It is possible to disable unused physical ports. A level 3 password is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example if rear port 1 is to be disabled, the following message appears:

```
REAR PORT 1 TO BE
DISABLED.CONFIRM
```

The following ports can be disabled, depending on the model.

- Front port (***Front Port*** setting)
- Rear port 1 (***Rear Port 1*** setting)
- Rear port 2 (***Rear Port 2*** setting)
- Ethernet port (***Ethernet*** setting)

Note:
It is not possible to disable a port from which the disabling port command originates.

Note:
We do not generally advise disabling the physical Ethernet port.

4.6 DISABLING LOGICAL PORTS

It is possible to disable unused logical ports. A level 3 password is needed to perform this action.

Note:
The port disabling setting cells are not provided in the settings file. It is only possible to do this using the HMI front panel.

The following protocols can be disabled:

- IEC 61850 (***IEC61850*** setting)
- DNP3 Over Ethernet (***DNP3 OE*** setting)
- Courier Tunnelling (***Courier Tunnel*** setting)

Note:
If any of these protocols are enabled or disabled, the Ethernet card will reboot.

4.7 SECURITY EVENTS MANAGEMENT

To implement NERC-compliant cyber-security, a range of Event records need to be generated. These log security issues such as the entry of a non-NERC-compliant password, or the selection of a non-NERC-compliant default display.

Security event values

Event Value	Display
PASSWORD LEVEL UNLOCKED	USER LOGGED IN ON {int} LEVEL {n}
PASSWORD LEVEL RESET	USER LOGGED OUT ON {int} LEVEL {n}
PASSWORD SET BLANK	P/WORD SET BLANK BY {int} LEVEL {p}
PASSWORD SET NON-COMPLIANT	P/WORD NOT-NERC BY {int} LEVEL {p}
PASSWORD MODIFIED	PASSWORD CHANGED BY {int} LEVEL {p}
PASSWORD ENTRY BLOCKED	PASSWORD BLOCKED ON {int}
PASSWORD ENTRY UNBLOCKED	P/WORD UNBLOCKED ON {int}
INVALID PASSWORD ENTERED	INV P/W ENTERED ON <int}
PASSWORD EXPIRED	P/WORD EXPIRED ON {int}
PASSWORD ENTERED WHILE BLOCKED	P/W ENT WHEN BLK ON {int}
RECOVERY PASSWORD ENTERED	RCVY P/W ENTERED ON {int}
IED SECURITY CODE READ	IED SEC CODE RD ON {int}
IED SECURITY CODE TIMER EXPIRED	IED SEC CODE EXP -
PORT DISABLED	PORT DISABLED BY {int} PORT {prt}
PORT ENABLED	PORT ENABLED BY {int} PORT {prt}
DEF. DISPLAY NOT NERC COMPLIANT	DEF DSP NOT-NERC
PSL SETTINGS DOWNLOADED	PSL STNG D/LOAD BY {int} GROUP {grp}

Event Value	Display
DNP SETTINGS DOWNLOADED	DNP STNG D/LOAD BY {int}
TRACE DATA DOWNLOADED	TRACE DAT D/LOAD BY {int}
IEC61850 CONFIG DOWNLOADED	IED CONFG D/LOAD BY {int}
USER CURVES DOWNLOADED	USER CRV D/LOAD BY {int} GROUP {crv}
PSL CONFIG DOWNLOADED	PSL CONFG D/LOAD BY {int} GROUP {grp}
SETTINGS DOWNLOADED	SETTINGS D/LOAD BY {int} GROUP {grp}
PSL SETTINGS UPLOADED	PSL STNG UPLOAD BY {int} GROUP {grp}
DNP SETTINGS UPLOADED	DNP STNG UPLOAD BY {int}
TRACE DATA UPLOADED	TRACE DAT UPLOAD BY {int}
IEC61850 CONFIG UPLOADED	IED CONFG UPLOAD BY {int}
USER CURVES UPLOADED	USER CRV UPLOAD BY {int} GROUP {crv}
PSL CONFIG UPLOADED	PSL CONFG UPLOAD BY {int} GROUP {grp}
SETTINGS UPLOADED	SETTINGS UPLOAD BY {int} GROUP {grp}
EVENTS HAVE BEEN EXTRACTED	EVENTS EXTRACTED BY {int} {nov} EVNTS
ACTIVE GROUP CHANGED	ACTIVE GRP CHNGE BY {int} GROUP {grp}
CS SETTINGS CHANGED	C & S CHANGED BY {int}
DR SETTINGS CHANGED	DR CHANGED BY {int}
SETTING GROUP CHANGED	SETTINGS CHANGED BY {int} GROUP {grp}
POWER ON	POWER ON -
SOFTWARE_DOWNLOADED	S/W DOWNLOADED -

where:

- int is the interface definition (UI, FP, RP1, RP2, TNL, TCP)
- prt is the port ID (FP, RP1, RP2, TNL, DNP3, IEC, ETHR)
- grp is the group number (1, 2, 3, 4)

- crv is the Curve group number (1, 2, 3, 4)
- n is the new access level (0, 1, 2, 3)
- p is the password level (1, 2, 3)
- nov is the number of events (1 – nnn)

Each new event has an incremented unique number, therefore missing events appear as 'gap' in the sequence. The unique identifier forms part of the event record that is read or uploaded from the IED.

Note:
It is no longer possible to clear Event, Fault, Maintenance, and Disturbance Records.

4.8 LOGGING OUT

If you have been configuring the IED, you should 'log out'. Do this by going up to the top of the menu tree. When you are at the Column Heading level and you press the Up button, you may be prompted to log out with the following display:

```
DO YOU WANT TO
LOG OUT?
```

You will only be asked this question if your password level is higher than the fallback level.

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT
Access Level #
```

Where # is the current fallback level.

If you decide not to log out, the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
Access Level #
```

where # is the current access level.

CHAPTER 19

INSTALLATION

1 CHAPTER OVERVIEW

This chapter provides information about installing the product.

This chapter contains the following sections:

2 HANDLING THE GOODS

Our products are of robust construction but require careful treatment before installation on site. This section discusses the requirements for receiving and unpacking the goods, as well as associated considerations regarding product care and personal safety.

Caution:
Before lifting or moving the equipment you should be familiar with the Safety Information chapter of this manual.

2.1 RECEIPT OF THE GOODS

On receipt, ensure the correct product has been delivered. Unpack the product immediately to ensure there has been no external damage in transit. If the product has been damaged, make a claim to the transport contractor and notify us promptly.

For products not intended for immediate installation, repack them in their original delivery packaging.

2.2 UNPACKING THE GOODS

When unpacking and installing the product, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any CDROMs or technical documentation (where included). These should accompany the unit to its destination substation and put in a dedicated place.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies where installation is being carried out at the same time as construction work.

2.3 STORING THE GOODS

If the unit is not installed immediately, store it in a place free from dust and moisture in its original packaging. Keep any dehumidifier bags included in the packing. The dehumidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals before replacing it in the carton. Ideally regeneration should be carried out in a ventilating, circulating oven at about 115°C. Bags should be placed on flat racks and spaced to allow circulation around them. The time taken for regeneration will depend on the size of the bag. If a ventilating, circulating oven is not available, when using an ordinary oven, open the door on a regular basis to let out the steam given off by the regenerating silica gel.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. Avoid storing in locations of high humidity. In locations of high humidity the packaging may become impregnated with moisture and the dehumidifier crystals will lose their efficiency.

The device can be stored between –25° to +70°C for unlimited periods or between -40°C to + 85°C for up to 96 hours (see technical specifications).

2.4 DISMANTLING THE GOODS

If you need to dismantle the device, always observe standard ESD (Electrostatic Discharge) precautions. The minimum precautions to be followed are as follows:

- Use an antistatic wrist band earthed to a suitable earthing point.
- Avoid touching the electronic components and PCBs.

3 MOUNTING THE DEVICE

The products are available in the following forms

- For flush panel and rack mounting
- For retrofitting K-series models
- Software only (for upgrades)

3.1 FLUSH PANEL MOUNTING

Panel-mounted devices are flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Caution:
Do not use conventional self-tapping screws, because they have larger heads and could damage the faceplate.

Alternatively, you can use tapped holes if the panel has a minimum thickness of 2.5 mm.

For applications where the product needs to be semi-projection or projection mounted, a range of collars are available.

If several products are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.

Caution:
Do not fasten products with pop rivets because this makes them difficult to remove if repair becomes necessary.

3.1.1 RACK MOUNTING

Panel-mounted variants can also be rack mounted using single-tier rack frames (our part number FX0021 001), as shown in the figure below. These frames are designed with dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm (19 inch) rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the products by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Caution:
Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS products because they have slightly larger heads.

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

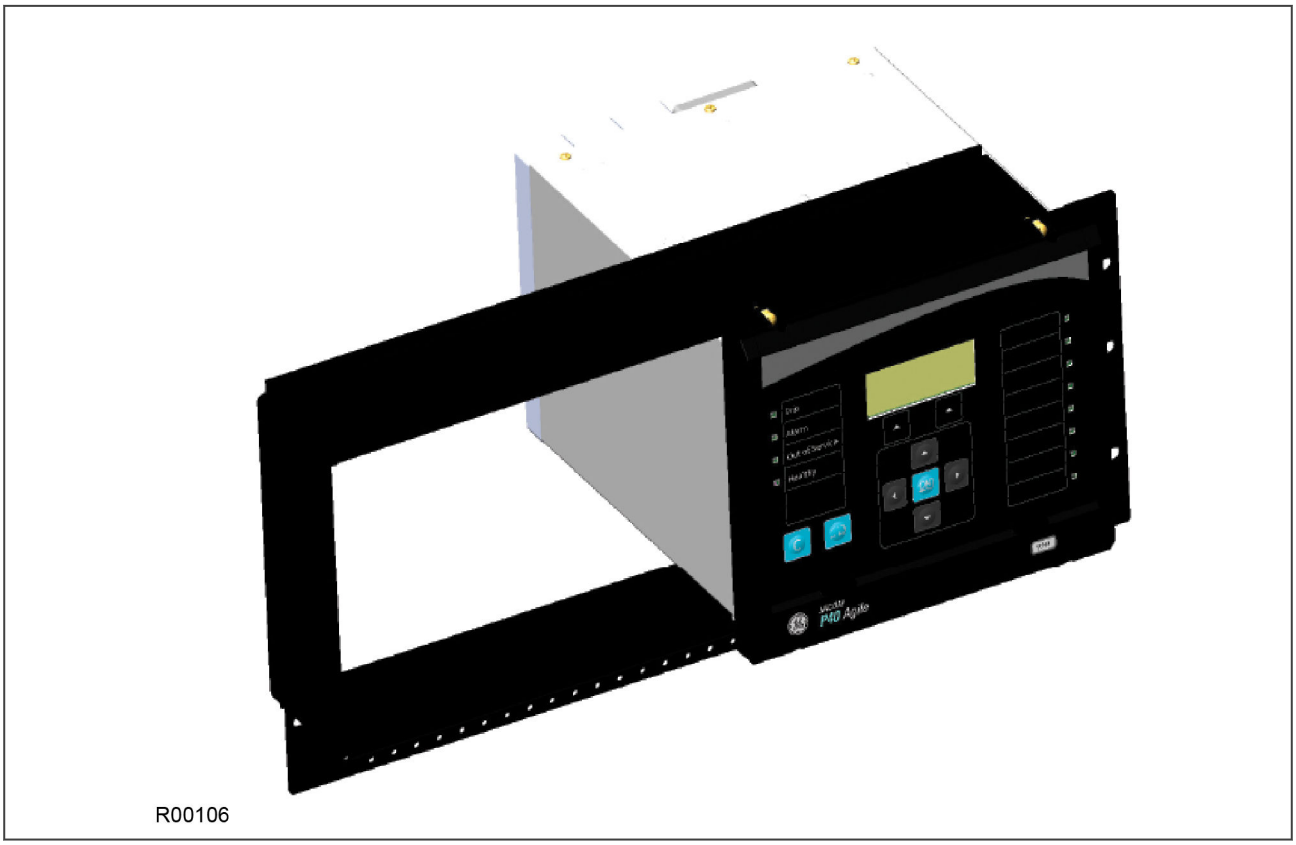


Figure 208: Rack mounting of products

Products can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from different product ranges to be pre-wired together before mounting.

Use blanking plates to fill any empty spaces. The spaces may be used for installing future products or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The part numbers are as follows:

Case size summation	Blanking plate part number
5TE	GJ2028 001
10TE	GJ2028 002
15TE	GJ2028 003
20TE	GJ2028 004
25TE	GJ2028 005
30TE	GJ2028 006
35TE	GJ2028 007
40TE	GJ2028 008
60TE	GJ2028 012
80TE	GJ2028 016

3.2 K-SERIES RETROFIT

A major advantage of the P40 Agile platform is its backward compatibility with the K-series products. The P40 Agile products have been designed such that the case, back panel terminal layout and pin-outs are identical to their K-series predecessors and can be retrofitted without the usual overhead associated with replacing and rewiring

devices. This allows easy upgrade of the protection system with minimum impact and minimum shutdown time of the feeder.

The equivalencies of the models are as follows:

Case width (TE)	Case width (mm)	Equivalent K series	Products
20TE	102.4 mm (4 inches)	KCGG140/142	P14N
30TE	154.2 mm (6 inches)	KCEG140/142	P14D

The old K-series products can be removed by sliding the cradle out of the case. The new P40 Agile cradle can then be inserted into the old case as shown below:

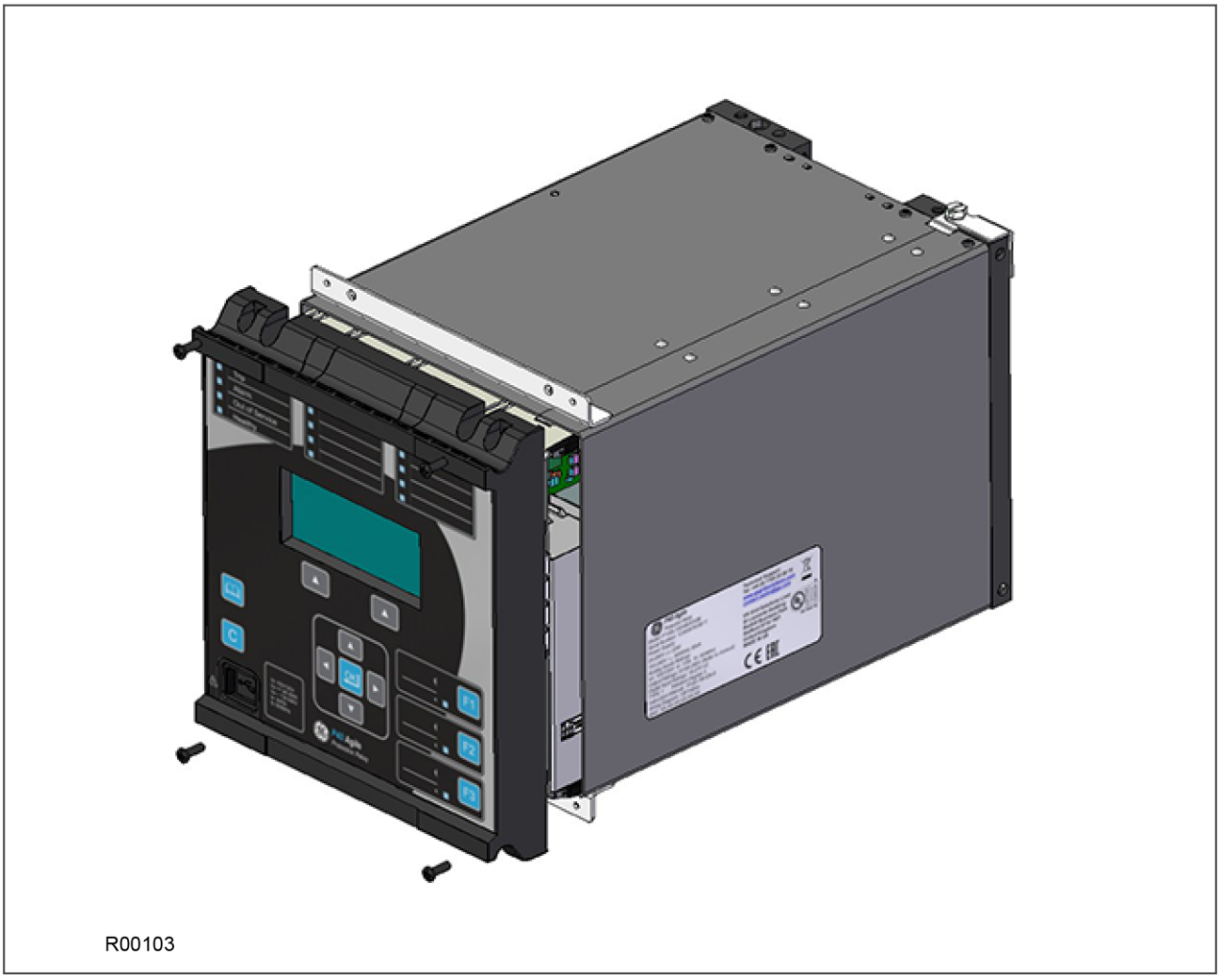


Figure 209: Inserting cradle into case

Both K-series products and P40 Agile products are equipped with CT shorting links. Depending on the model, your device may or may not be equipped with CTs. If there are CTs present, spring-loaded shorting contacts (see below) ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken, when withdrawing the cradle from the case. This ensures that no voltage is developed between the two terminals on breaking the CT connections.

If no CTs are present, the CT terminals are permanently shorted internally.

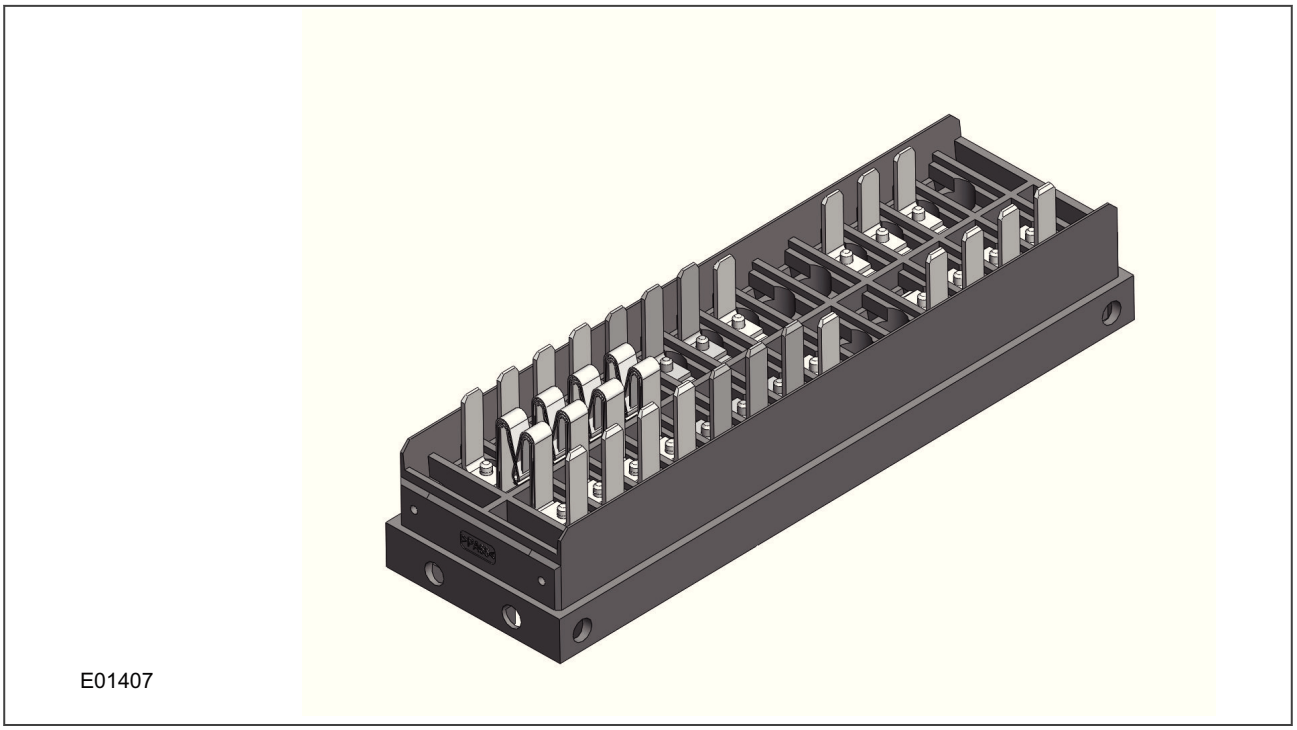


Figure 210: Spring-loaded CT shorting contacts

Before withdrawing the cradle it is important to:

- Check the existing case for any damage
- Check the wiring is in good condition, especially the earth wiring
- Check the continuity of the earth connection to the cublicle earthing bar.

If there is any doubt as to the integrity of any of these aspects, contact your local representative.

Caution:
After removing the K-series product from its case, refit it into the case that came with your device, for storage or reuse in another location.

The difference between a standard device and a K-series retrofit device is that the retrofit device has internal links between terminals 7 and 13, and terminals 8 and 14 respectively. This is so that equipment driven by the K-series field voltage conected to terminals 7 and 8, will continue to be driven indirectly via terminals 13 and 14 when replaced by P40 Agile products.

A K-series device provides a 48 V DC field voltage between terminals 7 and 8. This field voltage is intended for driving auxiliary equipment such as opto-inputs. P40 Agile devices DO NOT provide this field voltage. For this reason, P40 Agile retrofit devices have internal shorting links between terminals 7 and 13, and terminals 8 and 14 respectively. The intention of this is to provide the auxiliary supply voltage to terminals 7 and 8 in lieue of the field voltage.

Caution:
The voltage on terminals 7 and 8 mirrors that of the auxiliary supply voltage. If the auxiliary supply voltage on terminals 13 and 14 is not 48 V DC, then the voltage on terminals 7 and 8 is also not 48 V DC.

Caution:
When retrofitting a K-series device, ensure the load on terminals 7 and 8 is limited to a maximum of 5A. A jumplead with a 5A ceramic timelag fuse is fitted internally.

3.2.1 CONVENTIONS

The P40 Agile products have different conventions from the K-series products when it comes to numbering some hardware components. It is very important that you are aware of this. This is just a matter of convention and does not affect the terminal compatibility.

The equivalencies are as follows:

Component	P40 Agile products	K-series products
Output relay	RL1	RL0
Output relay	RL2	RL1
Output relay	RL3	RL2
Output relay	RL4	RL3
Output relay	RL5	RL4
Output relay	RL6	RL5
Output relay	RL7	RL6
Output relay	RL8	RL7
Opto-input	L1	L0
Opto-input	L2	L1
Opto-input	L3	L2
Opto-input	L4	L3
Opto-input	L5	L4
Opto-input	L6	L5
Opto-input	L7	L6
Opto-input	L8	L7

3.3 SOFTWARE ONLY

It is possible to upgrade an existing device by purchasing software only (providing the device is already fitted with the requisite hardware).

There are two options for software-only products:

- Your device is sent back to the General Electric factory for upgrade.
- The software is sent to you for upgrade. Please contact your local representative if you wish to procure the services of a commissioning engineer to help you with your device upgrade.

Note:
Software-only products are licensed for use with devices with specific serial numbers.

Caution:
Do not attempt to upgrade an existing device if the software has not been licensed for that speciific device.

4 CABLES AND CONNECTORS

This section describes the type of wiring and connections that should be used when installing the device. For pin-out details please refer to the Hardware Design chapter or the wiring diagrams.

Caution:
Before carrying out any work on the equipment you should be familiar with the Safety Section and the ratings on the equipment's rating label.

4.1 TERMINAL BLOCKS

The device uses MiDOS terminal blocks as shown below.

Figure 211: MiDOS terminal block

The MiDOS terminal block consists of up to 28 x M4 screw terminals. The wires should be terminated with rings using 90° ring terminals, with no more than two rings per terminal. The products are supplied with sufficient M4 screws.

M4 90° crimp ring terminals are available in three different sizes depending on the wire size. Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 - 1.65 mm^2 (22 – 16 AWG)	Red
ZB9124 900	1.04 - 2.63 mm^2 (16 – 14 AWG)	Blue

4.2 POWER SUPPLY CONNECTIONS

These should be wired with 1.5 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

Caution:
Protect the auxiliary power supply wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

4.3 EARTH CONNNECTION

Every device must be connected to the cubicle earthing bar using the M4 earth terminal.

Use a wire size of at least 2.5 mm^2 terminated with a ring terminal.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Note:
To prevent any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the product, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the product case, or using tinned ring terminals.

4.4 CURRENT TRANSFORMERS

Current transformers would generally be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Caution:
Current transformer circuits must never be fused.

Note:
If there are CTs present, spring-loaded shorting contacts ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken.

Note:
For 5A CT secondaries, we recommend using 2 x 2.5 mm^2 PVC insulated multi-stranded copper wire.

4.5 VOLTAGE TRANSFORMER CONNECTIONS

Voltage transformers should be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

4.6 WATCHDOG CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

4.7 EIA(RS)485 AND K-BUS CONNECTIONS

For connecting the EIA(RS485) / K-Bus ports, use 2-core screened cable with a maximum total length of 1000 m or 200 nF total cable capacitance.

A typical cable specification would be:

- Each core: 16/0.2 mm^2 copper conductors, PVC insulated
- Nominal conductor area: 0.5 mm^2 per core
- Screen: Overall braid, PVC sheathed

To guarantee the performance specifications, you must ensure continuity of the screen, when daisy chaining the connections. The device is supplied with an earth link pack (part number ZA0005092) consisting of an earth link and a self-tapping screw to facilitate this requirement.

The earth link is fastened to the Midos block just below terminal number 56 as shown:

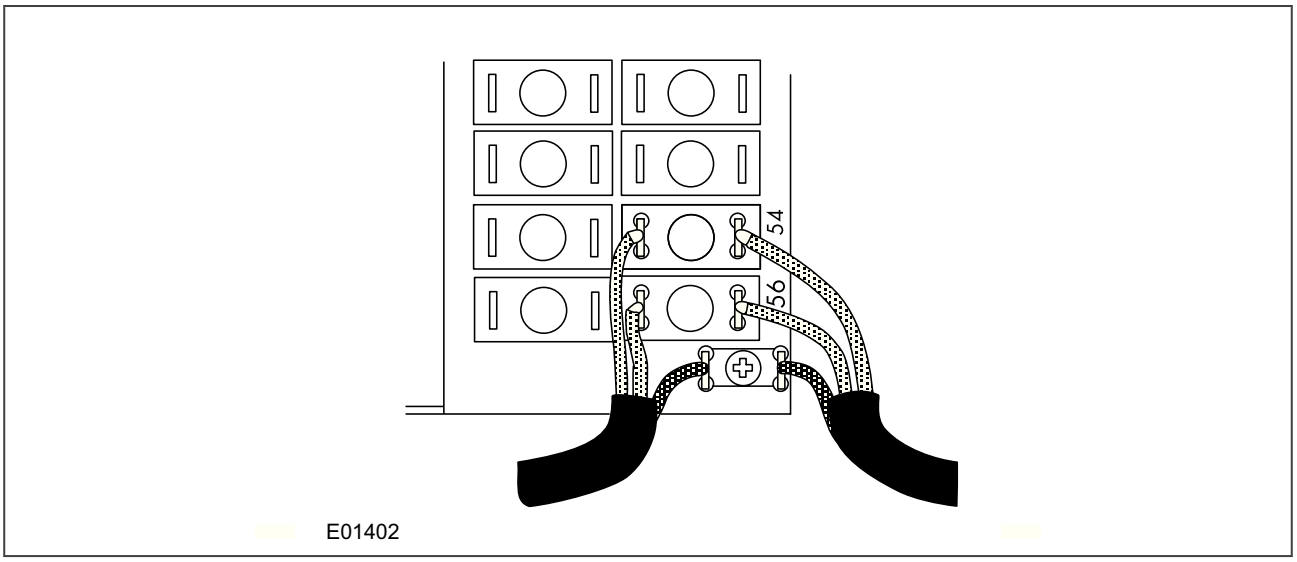


Figure 212: Earth link for cable screen

There is no electrical connection of the cable screen to the device. The link is provided purely to link together the two cable screens.

4.8 IRIG-B CONNECTION

The optional IRIG-B input uses the same terminals as the EIA(RS)485 port RP1. It is therefore apparent that RS485 communications and IRIG-B input are mutually exclusive.

A typical cable specification would be:

- Each core: 16/0.2 mm^2 copper conductors, PVC insulated
- Nominal conductor area: 0.5 mm^2 per core
- Screen: Overall braid, PVC sheathed

4.9 OPTO-INPUT CONNECTIONS

These should be wired with 1 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Each opto-input has a selectable preset ½ cycle filter. This makes the input immune to noise induced on the wiring. This can, however slow down the response. If you need to switch off the ½ cycle filter, either use double pole switching on the input, or screened twisted cable on the input circuit.

Caution:
Protect the opto-inputs and their wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

4.10 OUTPUT RELAY CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

4.11 ETHERNET METALLIC CONNECTIONS

If the device has a metallic Ethernet connection, it can be connected to either a 10Base-T or a 100Base-TX Ethernet hub. Due to noise sensitivity, we recommend this type of connection only for short distance connections, ideally where the products and hubs are in the same cubicle. For increased noise immunity, CAT 6 (category 6) STP (shielded twisted pair) cable and connectors can be used.

The connector for the Ethernet port is a shielded RJ-45. The pin-out is as follows:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

4.12 ETHERNET FIBRE CONNECTIONS

We recommend the use of fibre-optic connections for permanent connections in a substation environment. The 100 Mbps fibre optic port is based on the 100BaseFX standard and uses type LC connectors. They are compatible with 50/125 µm or 62.5/125 µm multimode fibres at 1300 nm wavelength.

4.13 USB CONNECTION

The IED has a type B USB socket on the front panel. A standard USB printer cable (type A one end, type B the other end) can be used to connect a local PC to the IED. This cable is the same as that used for connecting a printer to a PC.

5 CASE DIMENSIONS

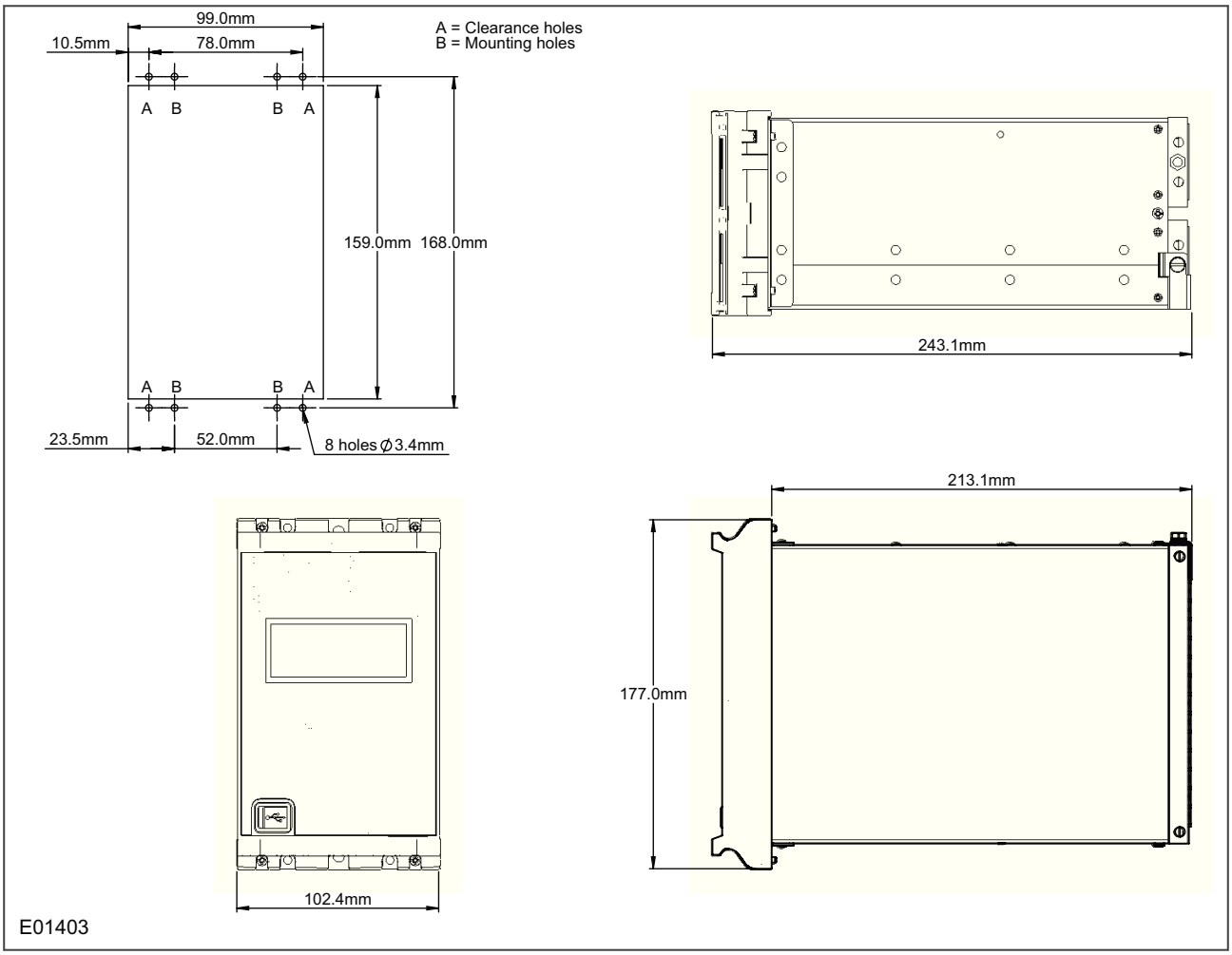


Figure 213: 20TE case dimensions

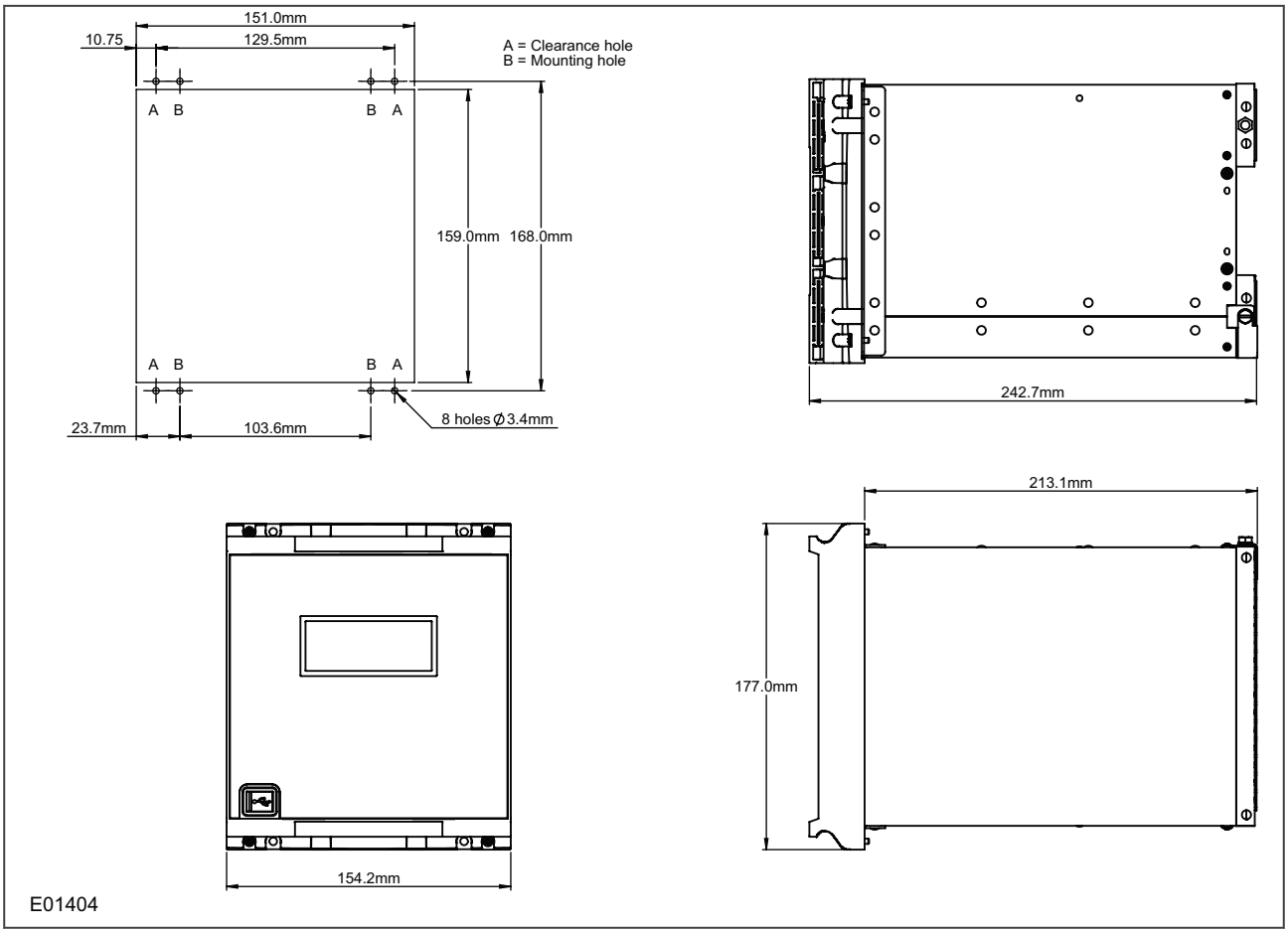


Figure 214: 30TE case dimensions

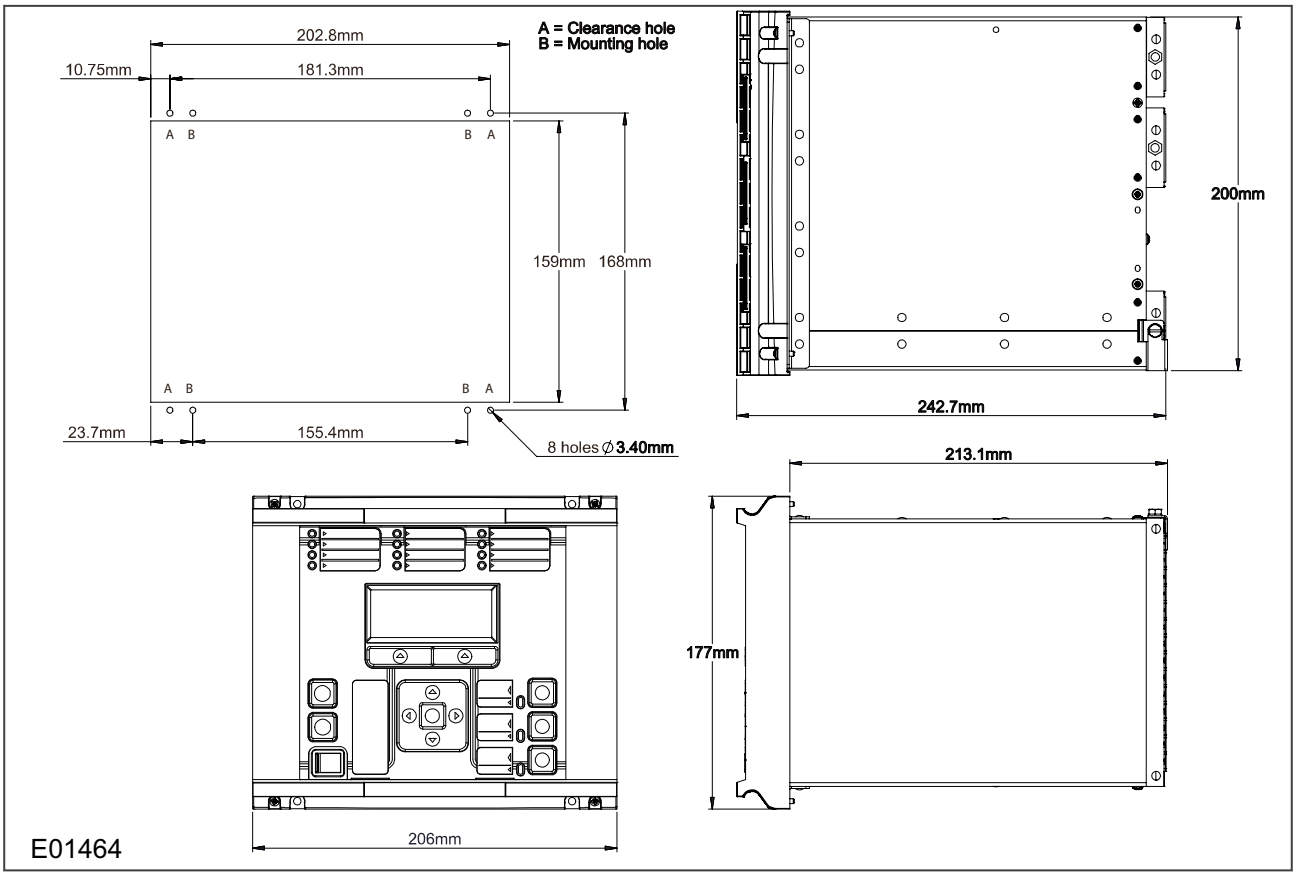


Figure 215: 40TE case dimensions

CHAPTER 20

COMMISSIONING INSTRUCTIONS

1 CHAPTER OVERVIEW

This chapter contains the following sections:

2 GENERAL GUIDELINES

General Electric IEDs are self-checking devices and will raise an alarm in the unlikely event of a failure. This is why the commissioning tests are less extensive than those for non-numeric electronic devices or electro-mechanical relays.

To commission the devices, you (the commissioning engineer) do not need to test every function. You need only verify that the hardware is functioning correctly and that the application-specific software settings have been applied. You can check the settings by extracting them using the settings application software, or by means of the front panel interface (HMI panel).

The menu language is user-selectable, so you can change it for commissioning purposes if required.

Note:
Remember to restore the language setting to the customer's preferred language on completion.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM as well as the ratings on the equipment's rating label.

Warning:
With the exception of the CT shorting contacts check, do not disassemble the device during commissioning.

3 COMMISSIONING TEST MENU

The IED provides several test facilities under the *COMMISSION TESTS* menu heading. There are menu cells that allow you to monitor the status of the opto-inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs. This section describes these commissioning test facilities.

3.1 OPTO I/P STATUS CELL (OPTO-INPUT STATUS)

This cell can be used to monitor the status of the opto-inputs while they are sequentially energised with a suitable DC voltage. The cell is a binary string that displays the status of the opto-inputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each logic input.

3.2 RELAY O/P STATUS CELL (RELAY OUTPUT STATUS)

This cell can be used to monitor the status of the relay outputs. The cell is a binary string that displays the status of the relay outputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each relay output.

The cell indicates the status of the output relays when the IED is in service. You can check for relay damage by comparing the status of the output contacts with their associated bits.

> *Note:*
> *When the **Test Mode** cell is set to `Contacts Blocked`, the relay output status indicates which contacts would operate if the IED was in-service. It does not show the actual status of the output relays, as they are blocked.*

3.3 TEST PORT STATUS CELL

This cell displays the status of the DDB signals that have been allocated in the ***Monitor Bit*** cells. If you move the cursor along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the IED. This allows you to test the Programmable Scheme Logic (PSL).

3.4 MONITOR BIT 1 TO 8 CELLS

The eight Monitor Bit cells allows you to select eight DDB signals that can be observed in the Test Port Status cell.

Each Monitor Bit cell can be assigned to a particular DDB signal. You set it by entering the required DDB signal number from the list of available DDB signals.

3.5 TEST MODE CELL

This cell allows you to perform secondary injection testing. It also lets you test the output contacts directly by applying menu-controlled test signals.

To go into test mode, select the `Test Mode` option in the ***Test Mode*** cell. This takes the IED out of service causing an alarm condition to be recorded and the ***Out of Service*** LED to illuminate. This also freezes any information stored in the *CB CONDITION* column. In IEC 60870-5-103 versions, it changes the Cause of Transmission (COT) to Test Mode.

In Test Mode, the output contacts are still active. To disable the output contacts you must select the `Contacts Blocked` option.

Once testing is complete, return the device back into service by setting the ***Test Mode*** Cell back to `Disabled`.

Caution:
When the cell is in Test Mode, the Scheme Logic still drives the output relays, which could result in tripping of circuit breakers. To avoid this, set the *Test Mode* cell to *Contacts Blocked*.

Note:
Test mode and Contacts Blocked mode can also be selected by energising an opto-input mapped to the Test Mode signal, and the Contact Block signal respectively.

3.6 TEST PATTERN CELL

The ***Test Pattern*** cell is used to select the output relay contacts to be tested when the ***Contact Test*** cell is set to *Apply Test*. The cell has a binary string with one bit for each user-configurable output contact, which can be set to '1' to operate the output and '0' to not operate it.

3.7 CONTACT TEST CELL

When the *Apply Test* command in this cell is issued, the contacts set for operation change state. Once the test has been applied, the command text on the LCD will change to ***No Operation*** and the contacts will remain in the Test state until reset by issuing the *Remove Test* command. The command text on the LCD will show ***No Operation*** after the *Remove Test* command has been issued.

Note:
*When the **Test Mode** cell is set to Contacts Blocked the **Relay O/P Status** cell does not show the current status of the output relays and therefore cannot be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.*

3.8 TEST LEDS CELL

When the *Apply Test* command in this cell is issued, the user-programmable LEDs illuminate for approximately 2 seconds before switching off, and the command text on the LCD reverts to ***No Operation***.

3.9 TEST AUTORECLOSE CELL

Where the IED provides an auto-reclose function, this cell will be available for testing the sequence of circuit breaker trip and auto-reclose cycles.

The *3 Pole Test* command causes the device to perform the first three phase trip/reclose cycle so that associated output contacts can be checked for operation at the correct times during the cycle. Once the trip output has operated the command text will revert to *No Operation* whilst the rest of the auto-reclose cycle is performed. To test subsequent three-phase autoreclose cycles, you repeat the *3 Pole Test* command.

Note:
The default settings for the programmable scheme logic has the AR Trip Test signals mapped to the Trip Input signals. If the programmable scheme logic has been changed, it is essential that these signals retain this mapping for the Test Autoreclose facility to work.

3.10 RED AND GREEN LED STATUS CELLS

These cells contain binary strings that indicate which of the user-programmable red and green LEDs are illuminated when accessing from a remote location. A '1' indicates that a particular LED is illuminated.

Note:
*When the status in both **Red LED Status** and **Green LED Status** cells is '1', this indicates the LEDs illumination is yellow.*

4 COMMISSIONING EQUIPMENT

Specialist test equipment is required to commission this product. We recognise three classes of equipment for commissioning :

- Recommended
- Essential
- Advisory

Recommended equipment constitutes equipment that is both necessary, and sufficient, to verify correct performance of the principal protection functions.

Essential equipment represents the minimum necessary to check that the product includes the basic expected protection functions and that they operate within limits.

Advisory equipment represents equipment that is needed to verify satisfactory operation of features that may be unused, or supplementary, or which may, for example, be integral to a distributed control/automation scheme. Operation of such features may, perhaps, be more appropriately verified as part of a customer defined commissioning requirement, or as part of a system-level commissioning regime.

4.1 RECOMMENDED COMMISSIONING EQUIPMENT

The minimum recommended equipment is a multifunctional three-phase AC current and voltage injection test set featuring :

- Controlled three-phase AC current and voltage sources,
- Transient (dynamic) switching between pre-fault and post-fault conditions (to generate delta conditions),
- Dynamic impedance state sequencer (capable of sequencing through 4 impedance states),
- Integrated or separate variable DC supply (0 - 250 V)
- Integrated or separate AC and DC measurement capabilities (0-440V AC, 0-250V DC)
- Integrated and/or separate timer,
- Integrated and/or separate test switches.

In addition, you will need :

- A portable computer, installed with appropriate software to liaise with the equipment under test (EUT). Typically this software will be proprietary to the product's manufacturer (for example MiCOM S1 Agile).
- Suitable electrical test leads.
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- Continuity tester
- Verified application-specific settings files

4.2 ESSENTIAL COMMISSIONING EQUIPMENT

As an absolute minimum, the following equipment is required:

- AC current source coupled with AC voltage source
- Variable DC supply (0 - 250V)
- Multimeter capable of measuring AC and DC current and voltage (0-440V AC, 0-250V DC)
- Timer
- Test switches
- Suitable electrical test leads
- Continuity tester

4.3 ADVISORY TEST EQUIPMENT

Advisory test equipment may be required for extended commissioning procedures:

- Current clamp meter
- Multi-finger test plug:
  - P992 for test block type P991
  - MMLB for test block type MMLG blocks
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- KITZ K-Bus - EIA(RS)232 protocol converter for testing EIA(RS)485 K-Bus port
- EIA(RS)485 to EIA(RS)232 converter for testing EIA(RS)485 Courier/MODBUS/IEC60870-5-103/DNP3 port
- A portable printer (for printing a setting record from the portable PC) and or writeable, detachable memory device.
- Phase angle meter
- Phase rotation meter
- Fibre-optic power meter.
- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm terminated with BFOC (ST) 2.5 connectors for testing the fibre-optic RP1 port.

5 PRODUCT CHECKS

These product checks are designed to ensure that the device has not been physically damaged prior to commissioning, is functioning correctly and that all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the IED prior to commissioning, you should make a copy of the settings. This will allow you to restore them at a later date if necessary. This can be done by:

- Obtaining a setting file from the customer.
- Extracting the settings from the IED itself, using a portable PC with appropriate setting software.

If the customer has changed the password that prevents unauthorised changes to some of the settings, either the revised password should be provided, or the original password restored before testing.

Note:
If the password has been lost, a recovery password can be obtained from General Electric.

5.1 PRODUCT CHECKS WITH THE IED DE-ENERGISED

Warning:
The following group of tests should be carried out without the auxiliary supply being applied to the IED and, if applicable, with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the IED for these checks. If a P991 test block is provided, the required isolation can be achieved by inserting test plug type P992. This open circuits all wiring routed through the test block.

Before inserting the test plug, you should check the scheme diagram to ensure that this will not cause damage or a safety hazard (the test block may, for example, be associated with protection current transformer circuits). The sockets in the test plug, which correspond to the current transformer secondary windings, must be linked before the test plug is inserted into the test block.

Warning:
Never open-circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.

If a test block is not provided, the voltage transformer supply to the IED should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the IED terminals. Where means of isolating the auxiliary supply and trip circuit (for example isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

5.1.1 VISUAL INSPECTION

Caution:
Check the rating information provided with the device. Check that the IED being tested is correct for the line or circuit.

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

Check that the current transformer shorting switches in the case are wired into the correct circuit. Ensure that, during withdrawal, they are closed by checking with a continuity tester. The shorting switches are between terminals 21 and 22, 23 and 24, 25 and 26, and 27 and 28.

5.1.2 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

5.1.3 EXTERNAL WIRING

Caution:
Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.

The auxiliary DC voltage supply uses terminals 13 (supply positive) and 14 (supply negative). Unlike the K-series products, the P40Agile series does not provide a field voltage supply. For K-series retrofit applications where pin-to-pin compatibility is required, the equivalent P40 Agile products emulate the field voltage supply by having internal links between pins 7 and 13, and pins 8 and 14, respectively.

5.1.4 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

Terminals	De-energised contact
3 - 5	Closed
4 - 6	Open

5.1.5 POWER SUPPLY

The IED can accept a nominal DC voltage from 24 V DC to 250 V DC, or a nominal AC voltage from 110 V AC to 240 V AC at 50 Hz or 60 Hz. Ensure that the power supply is within this operating range. The power supply must be rated at 12 Watts or more.

Warning:
Do not energise the IED or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.

Caution:
Energise the IED only if the auxiliary supply is within the specified operating ranges. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the IED.

5.2 PRODUCT CHECKS WITH THE IED ENERGISED

Warning:
The current and voltage transformer connections must remain isolated from the IED for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.

The following group of tests verifies that the IED hardware and software is functioning correctly and should be carried out with the supply applied to the IED.

5.2.1 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

Terminals	Energised contact
3 - 5	Open
4 - 6	Closed

5.2.2 TEST LCD

The Liquid Crystal Display (LCD) is designed to operate in a wide range of substation ambient temperatures. For this purpose, the IEDs have an ***LCD Contrast*** setting. The contrast is factory pre-set, but it may be necessary to adjust the contrast to give the best in-service display.

To change the contrast, you can increment or decrement the ***LCD Contrast*** cell in the *CONFIGURATION* column.

Caution:
Before applying a contrast setting, make sure that it will not make the display so light or dark such that menu text becomes unreadable. It is possible to restore the visibility of a display by downloading a setting file, with the LCD Contrast set within the typical range of 7 - 11.

5.2.3 DATE AND TIME

The date and time is stored in non-volatile memory. If the values are not already correct, set them to the correct values. The method of setting will depend on whether accuracy is being maintained by the IRIG-B port or by the IED's internal clock.

When using IRIG-B to maintain the clock, the IED must first be connected to the satellite clock equipment (usually a P594/RT430), which should be energised and functioning.

1. Set the IRIG-B Sync cell in the *DATE AND TIME* column to `Enabled`.
2. Ensure the IED is receiving the IRIG-B signal by checking that cell IRIG-B Status reads `Active`.
3. Once the IRIG-B signal is active, adjust the time offset of the universal co coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.
4. Check that the time, date and month are correct in the Date/Time cell. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.
5. Reconnect the IRIG-B signal.

If the time and date is not being maintained by an IRIG-B signal, ensure that the IRIG-B Sync cell in the *DATE AND TIME* column is set to `Disabled`.

1. Set the date and time to the correct local time and date using Date/Time cell or using the serial protocol.

5.2.4 TEST LEDS

On power-up, all LEDs should first flash yellow. Following this, the green "Healthy" LED should illuminate indicating that the device is healthy.

The IED's non-volatile memory stores the states of the alarm, the trip, and the user-programmable LED indicators (if configured to latch). These indicators may also illuminate when the auxiliary supply is applied.

If any of these LEDs are ON then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes off), no testing is needed for that LED because it is obviously operational.

5.2.5 TEST ALARM AND OUT-OF-SERVICE LEDS

The alarm and out of service LEDs can be tested using the *COMMISSION TESTS* menu column.

1. Set the ***Test Mode*** cell to `Contacts Blocked`.
2. Check that the out of service LED illuminates continuously and the alarm LED flashes.

It is not necessary to return the ***Test Mode*** cell to `Disabled` at this stage because the test mode will be required for later tests.

5.2.6 TEST TRIP LED

The trip LED can be tested by initiating a manual circuit breaker trip. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

5.2.7 TEST USER-PROGRAMMABLE LEDS

To test these LEDs, set the Test LEDs cell to `Apply Test`. Check that all user-programmable LEDs illuminate.

5.2.8 TEST OPTO-INPUTS

This test checks that all the opto-inputs on the IED are functioning correctly.

The opto-inputs should be energised one at a time. For terminal numbers, please see the external connection diagrams in the "Wiring Diagrams" chapter. Ensuring correct polarity, connect the supply voltage to the appropriate terminals for the input being tested.

The status of each opto-input can be viewed using either the ***Opto I/P Status*** cell in the *SYSTEM DATA* column, or the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column.

A '1' indicates an energised input and a '0' indicates a de-energised input. When each opto-input is energised, one of the characters on the bottom line of the display changes to indicate the new state of the input.

5.2.9 TEST OUTPUT RELAYS

This test checks that all the output relays are functioning correctly.

1. Ensure that the IED is still in test mode by viewing the ***Test Mode*** cell in the *COMMISSION TESTS* column. Ensure that it is set to `Contacts Blocked`.
2. The output relays should be energised one at a time. To select output relay 1 for testing, set the Test Pattern cell as appropriate.
3. Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagram.
4. To operate the output relay set the Contact Test cell to `Apply Test`.
5. Check the operation with the continuity tester.
6. Measure the resistance of the contacts in the closed state.

7. Reset the output relay by setting the Contact Test cell to `Remove Test`.
8. Repeat the test for the remaining output relays.
9. Return the IED to service by setting the Test Mode cell in the *COMMISSION TESTS* menu to `Disabled`.

5.2.10 TEST SERIAL COMMUNICATION PORT RP1

You need only perform this test if the IED is to be accessed from a remote location with a permanent serial connection to the communications port. The scope of this test does not extend to verifying operation with connected equipment beyond any supplied protocol converter. It verifies operation of the rear communication port (and if applicable the protocol converter) and varies according to the protocol fitted.

5.2.10.1 CHECK PHYSICAL CONNECTIVITY

The rear communication port RP1 is presented on terminals 54 and 56. Screened twisted pair cable is used to make a connection to the port. The cable screen should be connected to the earth link just below pin 56:

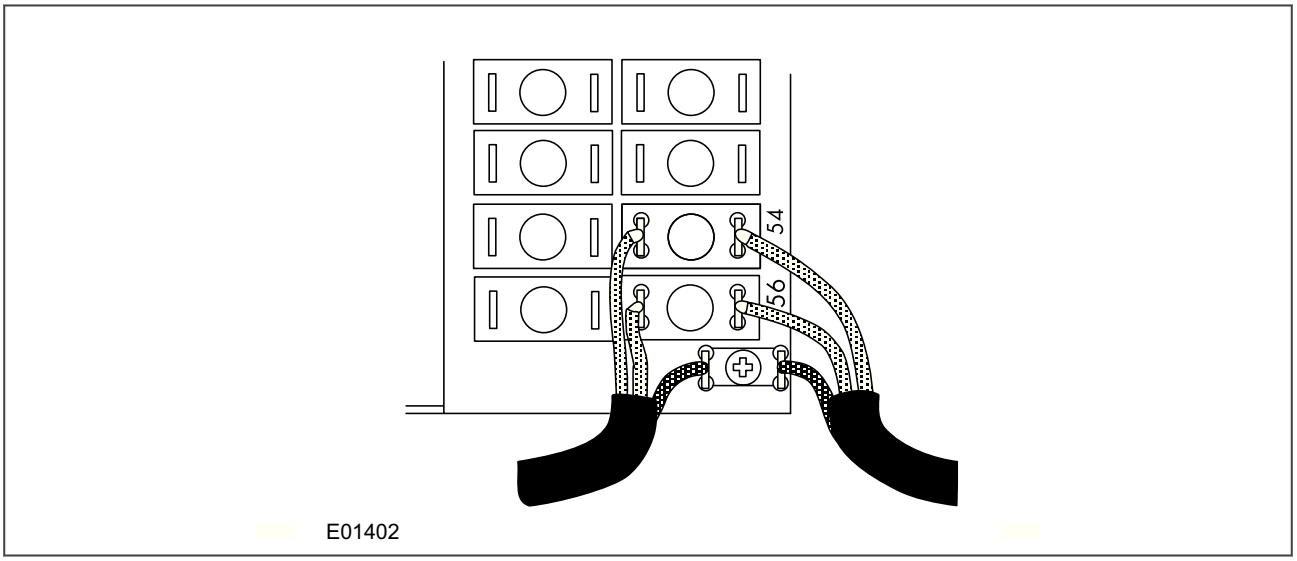


Figure 216: RP1 physical connection

For K-Bus applications, pins 54 and 56 are not polarity sensitive and it does not matter which way round the wires are connected. EIA(RS)485 is polarity sensitive, so you must ensure the wires are connected the correct way round (pin 54 is positive, pin 56 is negative).

If K-Bus is being used, a Kitz protocol converter (KITZ101, KITZ102 OR KITZ201) will have been installed to convert the K-Bus signals into RS232. Likewise, if RS485 is being used, an RS485-RS232 converter will have been installed. In the case where a protocol converter is being used, a laptop PC running appropriate software (such as MiCOM S1 Agile) can be connected to the incoming side of the protocol converter. An example for K-bus to RS232 conversion is shown below. RS485 to RS232 would follow the same principle, only using a RS485-RS232 converter. Most modern laptops have USB ports, so it is likely you will also require a RS232 to USB converter too.

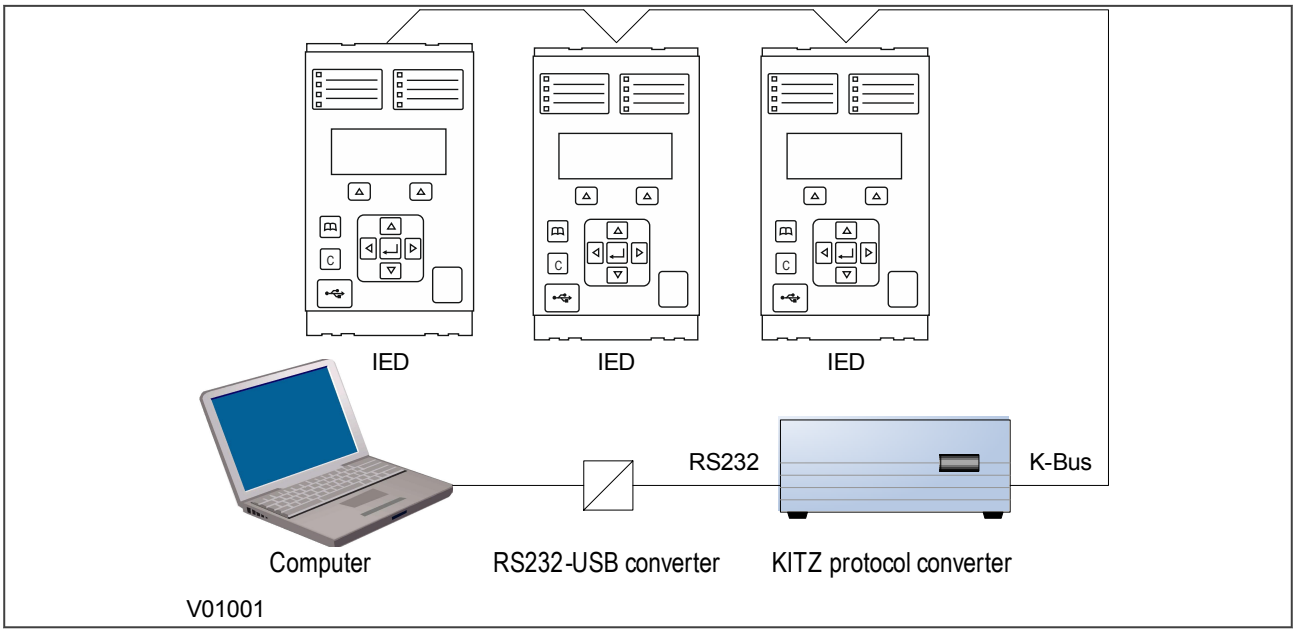


Figure 217: Remote communication using K-bus

5.2.10.2 CHECK LOGICAL CONNECTIVITY

The logical connectivity depends on the chosen data protocol, but the principles of testing remain the same for all protocol variants:

1. Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter.
2. For Courier models, ensure that you have set the correct RP1 address
3. Check that communications can be established with this IED using the portable PC/Master Station.

5.2.11 TEST SERIAL COMMUNICATION PORT RP2

RP2 is only available on selected models. If applicable, this test is the same as for RP1 only the relevant terminals are 82 and 84.

5.2.12 TEST ETHERNET COMMUNICATION

For products that employ Ethernet communications, we recommend that testing be limited to a visual check that the correct ports are fitted and that there is no sign of physical damage.

If there is no board fitted or the board is faulty, a NIC link alarm will be raised (providing this option has been set in the ***NIC Link Report*** cell in the *COMMUNICATIONS* column).

5.2.13 TEST CURRENT INPUTS

This test verifies that the current measurement inputs are configured correctly.

All devices leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required then this must be set in the Frequency cell in the *SYSTEM DATA* column.

1. Apply current equal to the line current transformer secondary winding rating to each current transformer input in turn.
2. Check its magnitude using a multi-meter or test set readout. The corresponding reading can then be checked in the *MEASUREMENTS 1* column.
3. Record the displayed value. The measured current values will either be in primary or secondary Amperes. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio (set in the *CT AND VT RATIOS* column), as shown below. If the Local Values cell is set to `Secondary`, the value displayed should be equal to the applied current.

Note:
If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.

The measurement accuracy of the IED is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Cell in MEASUREMENTS 1	Corresponding CT ratio (in CT AND VT RATIOS column)
IA magnitude IB magnitude IC magnitude	Phase CT Primary / Phase CT Sec'y
IN measured mag	E/F CT Primary / E/F CT Secondary
IN measured RMS	E/F CT Primary / E/F CT Secondary
ISEF magnitude	SEF CT Primary / SEF CT Secondary

5.2.14 TEST VOLTAGE INPUTS

This test verifies that the voltage measurement inputs are configured correctly.

1. Apply rated voltage to each voltage transformer input in turn
2. Check its magnitude using a multimeter or test set readout. The corresponding reading can then be checked in the *MEASUREMENTS 1* column.
3. Record the value displayed. The measured voltage values will either be in primary or secondary Volts. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio (set in the *CT AND VT RATIOS* column) as shown below. If the Local Values cell is set to `Secondary`, the value displayed should be equal to the applied voltage.

Note:
If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.

Cell in MEASUREMENTS 1	Corresponding VT ratio (in *CT AND VT RATIOS* column)
VAN magnitude VBN magnitude VCN magnitude	Main VT Primary / Main VT Sec'y

Cell in MEASUREMENTS 1	Corresponding VT ratio (in *CT AND VT RATIOS* column)
4th VT Voltage Mag	4th VT Primary / 4th VT Secondary

6 SETTING CHECKS

The setting checks ensure that all of the application-specific settings (both the IED's function and programmable scheme logic settings) have been correctly applied.

Note:
If applicable, the trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.

6.1 APPLY APPLICATION-SPECIFIC SETTINGS

There are two different methods of applying the settings to the IED

- Transferring settings to the IED from a pre-prepared setting file using MiCOM S1 Agile
- Enter the settings manually using the IED's front panel HMI

6.1.1 TRANSFERRING SETTINGS FROM A SETTINGS FILE

This is the preferred method for transferring function settings. It is much faster and there is a lower margin for error.

1. Connect a PC running the Settings Application Software to the IED's front port, or a rear Ethernet port. Alternatively connect to the rear Courier communications port, using a KITZ protocol converter if necessary.
2. Power on the IED
3. Enter the IP address of the device if it is Ethernet enabled
4. Right-click the appropriate device name in the System Explorer pane and select **Send**
5. In the **Send to** dialog select the setting files and click **Send**

Note:
*The device name may not already exist in the system shown in **System Explorer**. In this case, perform a **Quick Connect** to the IED, then manually add the settings file to the device name in the system. Refer to the Settings Application Software help for details of how to do this.*

6.1.2 ENTERING SETTINGS USING THE HMI

1. Starting at the default display, press the Down cursor key to show the first column heading.
2. Use the horizontal cursor keys to select the required column heading.
3. Use the vertical cursor keys to view the setting data in the column.
4. To return to the column header, either press the Up cursor key for a second or so, or press the **Cancel** key once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the Up cursor key or the Cancel key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
7. To change the setting value, press the vertical cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the left and right cursor keys.

8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the down cursor key. Before returning to the default display, the following prompt appears.

```
Update settings?
ENTER or CLEAR
```

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

Note:
If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.
Control and support settings are updated immediately after they are entered, without the Update settings prompt.
It is not possible to change the PSL using the IED's front panel HMI.

Caution:
Where the installation needs application-specific PSL, the relevant .psl files, must be transferred to the IED, for each and every setting group that will be used. If you do not do this, the factory default PSL will still be resident. This may have severe operational and safety consequences.

7 IEC 61850 EDITION 2 TESTING

7.1 USING IEC 61850 EDITION 2 TEST MODES

In a conventional substation, functionality typically resides in a single device. It is usually easy to physically isolate these functions, as the hardwired connects can simply be removed. Within a digital substation architecture however, functions may be distributed across many devices. This makes isolation of these functions difficult, because there are no physical wires that can be disconnected on a Ethernet network. Logical isolation of the various functions is therefore necessary.

With devices that support IEC 61850 Edition 2, it is possible to use a test mode to conduct online testing, which helps with the situation. The advantages of this are as follows:

- The device can be placed into a test mode, which can disable the relay outputs when testing the device with test input signals.
- Specific protection and control functions can be logically isolated.
- GOOSE messages can be tagged so that receiving devices can recognise they are test signals.
- An IED receiving simulated GOOSE or Sampled Value messages from test devices can differentiate these from normal process messages, and be configured to respond appropriately.

7.1.1 IED TEST MODE BEHAVIOUR

Test modes define how the device responds to test messages, and whether the relay outputs are activated or not. You can select the mode of operation by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column.
- Using an IEC 61850 control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the IED behaviour under the different modes:

IED Test Mode Setting	Result
`Disabled`	• Normal IED behaviour
`Test`	• Protection remains enabled • Output from the device is still active • IEC 61850 message output has the 'quality' parameter set to 'test' • The device only responds to IEC61850 MMS messages from the client with the 'test' flag set
`Contacts Blocked`	• Protection remains enabled • Output from the device is disabled • IEC 61850 message output has quality set to 'test' • The device only responds to IEC 61850 MMS messages from the client with the 'test' flag set

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

7.2 SIMULATED INPUT BEHAVIOUR

Simulated GOOSE messages can be used during testing.

The ***Subscriber Sim*** setting in the *COMMISSION TESTS* column controls whether a device listens to simulated signals or to real ones. An IEC 61850 control service to System/LPHD.Sim can also be used to change this value.

The device may be presented with both real signals and test signals. An internal state machine is used to control how the device switches between signals:

- The IED will continue subscribing to the 'real' GOOSE1 (in green) until it receives the first simulated GOOSE 1 (in red). This will initiate subscription changeover.
- After changeover to this new state, the IED will continue to subscribe to the simulated GOOSE 1 message (in red). Even if this simulated GOOSE 1 message disappears, the real GOOSE 1 message (in green) will still not be processed. This means all Virtual Inputs derived from the GOOSE 1 message will go to their default state.
- The only way to bring the IED out of this state is to set the ***Subscriber Sim*** setting back to False. The IED will then immediately stop processing the simulated messages and start processing real messages again.
- During above steps, IED1 will continuously process the real GOOSE 2 and GOOSE 3 messages as normal because it has not received any simulated messages for these that would initiate a changeover.

The process is represented in the following figure:

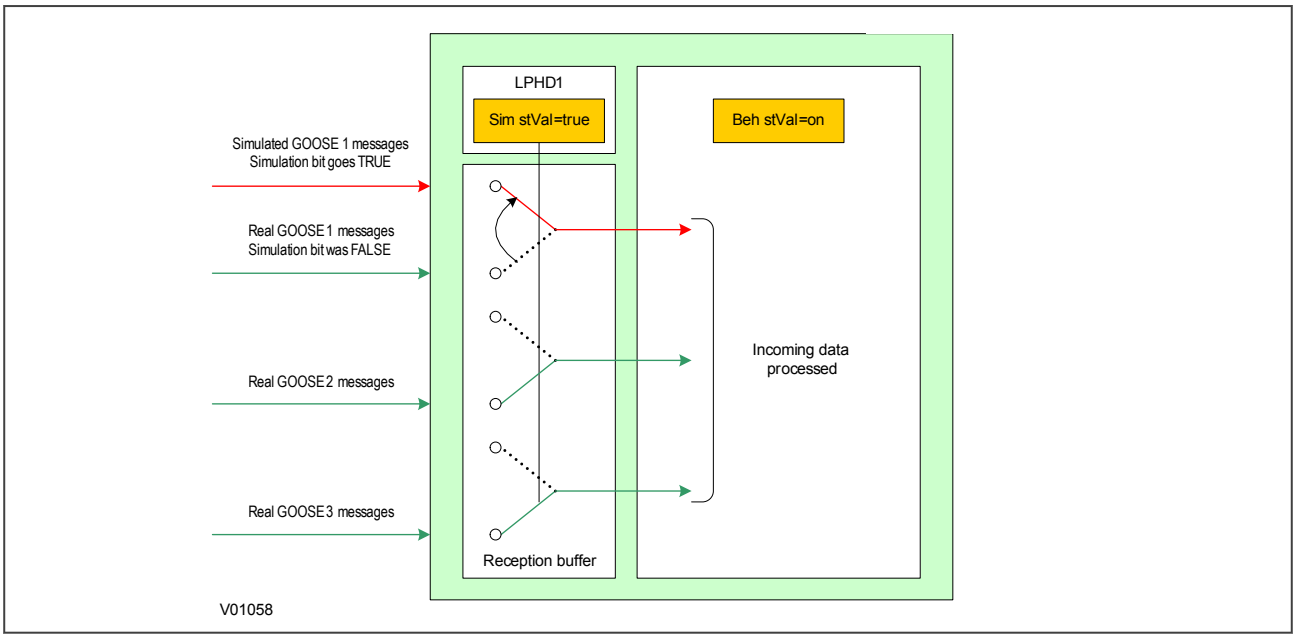


Figure 218: Simulated input behaviour

7.3 TESTING EXAMPLES

These examples show how you test the IED with and without simulated values. Depending on the IED Test Mode, it may respond by operating plant (for example by tripping the circuit breaker) or it may not operate plant.

7.3.1 TEST PROCEDURE FOR REAL VALUES

This procedure is for testing with real values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test-blocked`

3. Ensure the device Simulation Listening Mode is disabled
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Disabled`
4. Inject real GOOSE signals using a test device. The device will continue to listen to 'real' GOOSE messages and ignore simulated messages received.
5. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

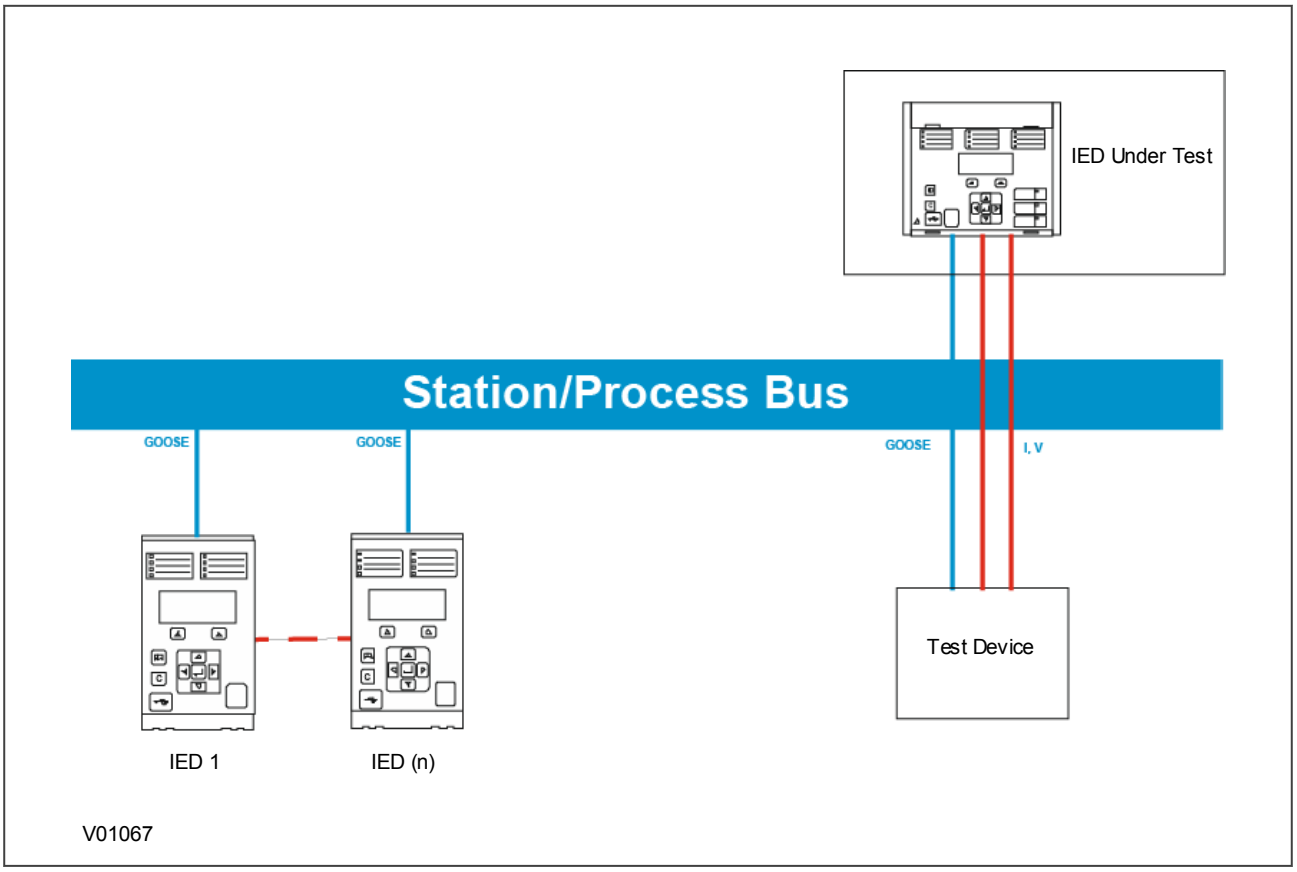


Figure 219: Test example 1

7.3.2 TEST PROCEDURE FOR SIMULATED VALUES - NO PLANT

This procedure is for testing with simulated values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `test-blocked`

3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = *Enabled*
4. Inject simulated GOOSE signals using a test device connected to the Ethernet network. The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of test mode. Each message is treated separately.
5. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

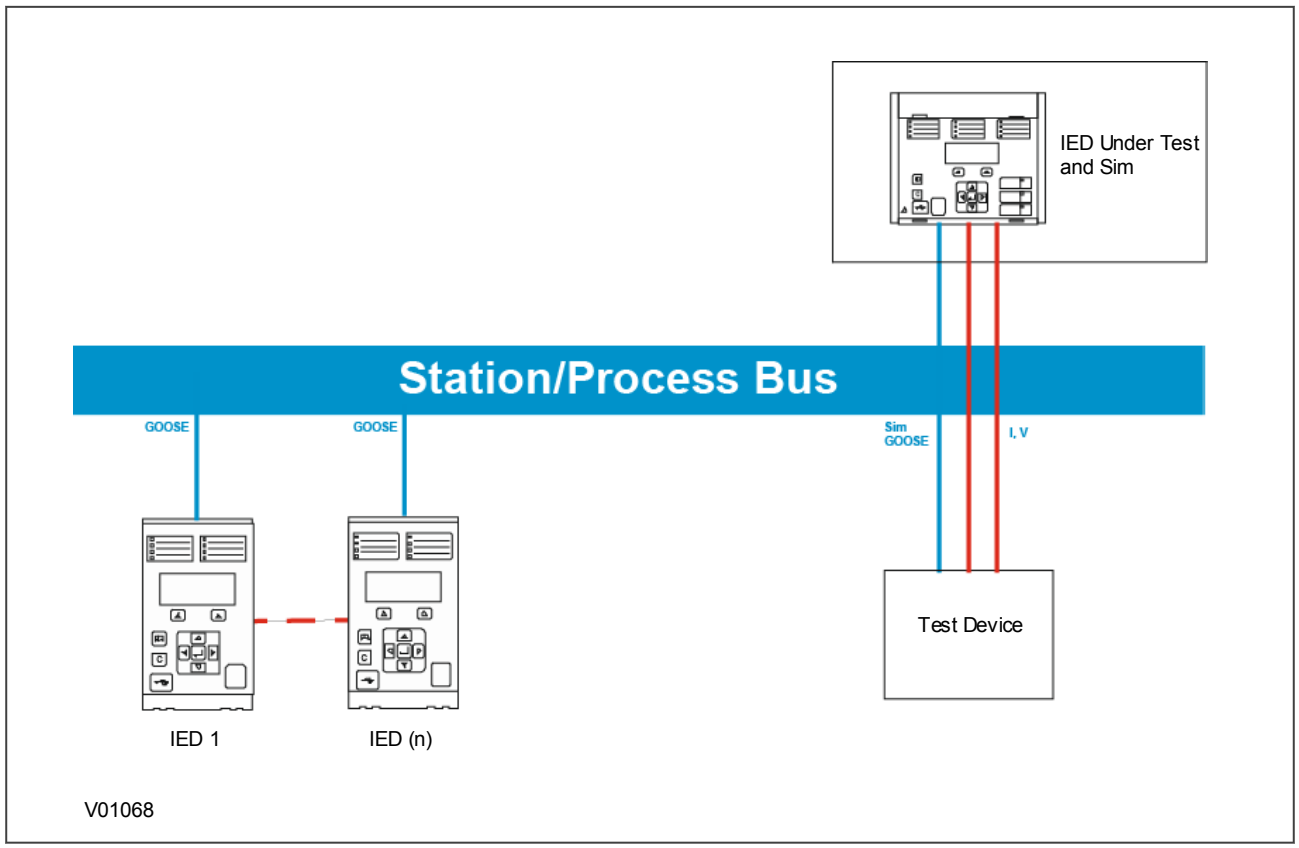


Figure 220: Test example 2

7.3.3 TEST PROCEDURE FOR SIMULATED VALUES - WITH PLANT

This procedure is for testing with simulated values with operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → *Test*
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows *Test*

3. Set device into Simulation Listening Mode

   Select *COMMISSION TESTS* → ***Subscriber Sim*** = *Enabled*

4. Inject simulated GOOSE signals using a test device connected to the Ethernet network.

   The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of IED test mode. Each message is treated separately, but sampled values are considered as a single message.

5. Verify function based on test signal outputs.

   Binary outputs (e.g. CB trips) will operate as normal. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram:

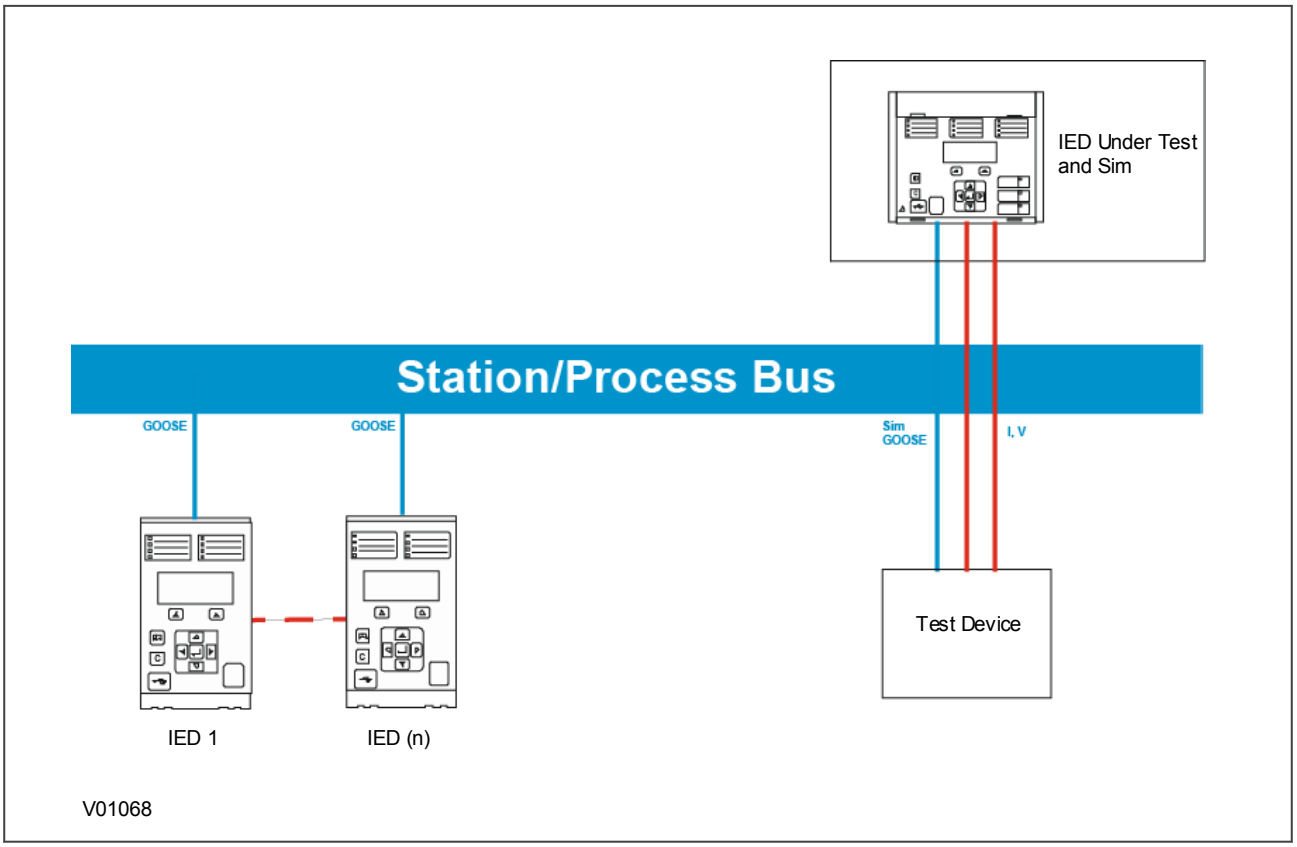


Figure 221: Test example 3

7.3.4 CONTACT TEST

The ***Apply Test*** command in this cell is used to change the state of the contacts set for operation.

If the device has been put into 'Contact Blocked' mode using an input signal (via the ***Block Contacts*** DDB signal) then the ***Apply Test*** command will not execute. This is to prevent a device that has been blocked by an external process having its contacts operated by a local operator using the HMI.

If the ***Block Contacts*** DDB is not set and the ***Apply Test*** command in this cell is issued, contacts change state and the command text on the LCD changes to *No Operation*. The contacts remain in the Test state until reset by issuing the ***Remove Test*** command. The command text on the LCD shows *No Operation* after the ***Remove Test*** command has been issued.

Note:
*When the **IED Test Mode** cell is set to Contacts Blocked, the **Relay O/P Status** cell does not show the current status of the output relays so cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.*

8 PROTECTION TIMING CHECKS

There is no need to check every protection function. Only one protection function needs to be checked as the purpose is to verify the timing on the processor is functioning correctly.

8.1 OVERCURRENT CHECK

If the overcurrent protection function is being used, test the overcurrent protection for stage 1.

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Make a note of which elements need to be re-enabled after testing.
4. Connect the test circuit.
5. Perform the test.
6. Check the operating time.

8.2 CONNECTING THE TEST CIRCUIT

1. Use the PSL to determine which output relay will operate when an overcurrent trip occurs.
2. Use the output relay assigned to ***Trip Output A***.
3. Use the PSL to map the protection stage under test directly to an output relay.

> *Note:*
> *If using the default PSL, use output relay 3 as this is already mapped to the DDB signal* ***Trip Command Out****.*

4. Connect the output relay so that its operation will trip the test set and stop the timer.
5. Connect the current output of the test set to the A-phase current transformer input.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column is set to `Directional Fwd`, the current should flow out of terminal 21. If set to `Directional Rev`, it should flow into terminal 21.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column has been set to `Directional Fwd` or 'Directional Rev', the rated voltage should be applied to terminals 18 and 19.
6. Ensure that the timer starts when the current is applied.

> *Note:*
> *If the timer does not stop when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the direction of operation set. Try again with the current connections reversed.*

8.3 PERFORMING THE TEST

1. Ensure that the timer is reset.
2. Apply a current of twice the setting shown in the ***I>1 Current Set*** cell in the *OVERCURRENT* column.
3. Note the time displayed when the timer stops.
4. Check that the red trip LED has illuminated.

8.4 CHECK THE OPERATING TIME

Check that the operating time recorded by the timer is within the range shown below.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating time at twice current setting and time multiplier/ time dial setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	I>1 Time Delay setting	Setting ±2%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	24.67 - 28.67
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 4.0
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.50	9.02 - 9.97
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Note:
With the exception of the definite time characteristic, the operating times given are for a Time Multiplier Setting (TMS) or Time Dial Setting (TDS) of 1. For other values of TMS or TDS, the values need to be modified accordingly.

Note:
For definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively. You may need to add this the IED's acceptable range of operating times.

Caution:
On completion of the tests, you must restore all settings to customer specifications.

9 ONLOAD CHECKS

Warning:
Onload checks are potentially very dangerous and may only be carried out by qualified and authorised personnel.

Onload checks can only be carried out if there are no restrictions preventing the energisation of the plant, and the other devices in the group have already been commissioned.

Remove all test leads and temporary shorting links, then replace any external wiring that has been removed to allow testing.

Warning:
If any external wiring has been disconnected for the commissioning process, replace it in accordance with the relevant external connection or scheme diagram.

9.1 CONFIRM CURRENT CONNECTIONS

1. Measure the current transformer secondary values for each input using a multimeter connected in series with the corresponding current input.
2. Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control centre.
3. Ensure the current flowing in the neutral circuit of the current transformers is negligible.
4. Compare the values of the secondary phase currents and phase angle with the measured values, which can be found in the *MEASUREMENTS 1* column.

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT AND VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

9.2 CONFIRM VOLTAGE CONNECTIONS

1. Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated.
2. Check that the system phase rotation is correct using a phase rotation meter.
3. Compare the values of the secondary phase voltages with the measured values, which can be found in the *MEASUREMENTS 1* menu column.

Cell in MEASUREMENTS 1 Column	Corresponding VT ratio in CT AND VT RATIOS column
VAB Magnitude ***VBC Magnitude*** ***VCA Magnitude*** ***VAN Magnitude*** ***VBN Magnitude*** ***VCN Magnitude***	Main VT Primary / Main VT Sec'y
C/S Voltage Mag.	4th VT Primary / 4th VT Secondary

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT AND VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

9.3 ON-LOAD DIRECTIONAL TEST

This test ensures that directional overcurrent and fault locator functions have the correct forward/reverse response to fault and load conditions. For this test you must first know the actual direction of power flow on the system. If you do not already know this you must determine it using adjacent instrumentation or protection already in-service.

- For load current flowing in the Forward direction (power export to the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show positive power signing.
- For load current flowing in the Reverse direction (power import from the remote line end), the ***A Phase Watts*** cell in the *MEASUREMENTS 2* column should show negative power signing.

Note:
*This check applies only for Measurement Modes 0 (default), and 2. This should be checked in the MEASURE'T SETUP column (**Measurement Mode** = 0 or 2). If measurement modes 1 or 3 are used, the expected power flow signing would be opposite to that shown above.*

In the event of any uncertainty, check the phase angle of the phase currents with respect to their phase voltage.

10 FINAL CHECKS

1. Remove all test leads and temporary shorting leads.
2. If you have had to disconnect any of the external wiring in order to perform the wiring verification tests, replace all wiring, fuses and links in accordance with the relevant external connection or scheme diagram.
3. The settings applied should be carefully checked against the required application-specific settings to ensure that they are correct, and have not been mistakenly altered during testing.
4. Ensure that all protection elements required have been set to `Enabled` in the *CONFIGURATION* column.
5. Ensure that the IED has been restored to service by checking that the ***Test Mode*** cell in the *COMMISSION TESTS* column is set to `Disabled`.
6. If the IED is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using the ***Reset All Values*** cell. If the required access level is not active, the device will prompt for a password to be entered so that the setting change can be made.
7. If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.
8. If a P991/MMLG test block is installed, remove the P992/MMLB test plug and replace the cover so that the protection is put into service.
9. Ensure that all event records, fault records, disturbance records, alarms and LEDs and communications statistics have been reset.

Note:
Remember to restore the language setting to the customer's preferred language on completion.

CHAPTER 21

MAINTENANCE AND TROUBLESHOOTING

1 CHAPTER OVERVIEW

The Maintenance and Troubleshooting chapter provides details of how to maintain and troubleshoot products based on the Px4x and P40Agile platforms. Always follow the warning signs in this chapter. Failure to do so may result injury or defective equipment.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

The troubleshooting part of the chapter allows an error condition on the IED to be identified so that appropriate corrective action can be taken.

If the device develops a fault, it is usually possible to identify which module needs replacing. It is not possible to perform an on-site repair to a faulty module.

If you return a faulty unit or module to the manufacturer or one of their approved service centres, you should include a completed copy of the Repair or Modification Return Authorization (RMA) form.

This chapter contains the following sections:

2 MAINTENANCE

2.1 MAINTENANCE CHECKS

In view of the critical nature of the application, General Electric products should be checked at regular intervals to confirm they are operating correctly. General Electric products are designed for a life in excess of 20 years.

The devices are self-supervising and so require less maintenance than earlier designs of protection devices. Most problems will result in an alarm, indicating that remedial action should be taken. However, some periodic tests should be carried out to ensure that they are functioning correctly and that the external wiring is intact. It is the responsibility of the customer to define the interval between maintenance periods. If your organisation has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

Although some functionality checks can be performed from a remote location, these are predominantly restricted to checking that the unit is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. For this reason, maintenance checks should also be performed locally at the substation.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

2.1.1 ALARMS

First check the alarm status LED to see if any alarm conditions exist. If so, press the Read key repeatedly to step through the alarms.

After dealing with any problems, clear the alarms. This will clear the relevant LEDs.

2.1.2 OPTO-ISOLATORS

Check the opto-inputs by repeating the commissioning test detailed in the Commissioning chapter.

2.1.3 OUTPUT RELAYS

Check the output relays by repeating the commissioning test detailed in the Commissioning chapter.

2.1.4 MEASUREMENT ACCURACY

If the power system is energised, the measured values can be compared with known system values to check that they are in the expected range. If they are within a set range, this indicates that the A/D conversion and the calculations are being performed correctly. Suitable test methods can be found in Commissioning chapter.

Alternatively, the measured values can be checked against known values injected into the device using the test block, (if fitted) or injected directly into the device's terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

2.2 REPLACING THE UNIT

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, you should normally replace the cradle which slides easily out of the case. This can be done without disturbing the scheme wiring.

In the unlikely event that the problem lies with the wiring and/or terminals, then you must replace the complete device, rewire and re-commission the device.

Caution:
If the repair is not performed by an approved service centre, the warranty will be invalidated.

Caution:
Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.

Warning:
Before working at the rear of the unit, isolate all voltage and current supplying it.

Note:
The General Electric products have integral current transformer shorting switches which will close, for safety reasons, when the terminal block is removed.

To replace the cradle without disturbing the case and wiring:

1. Remove the faceplate.
2. Carefully withdraw the cradle from the front.
3. To reinstall the unit, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and all connections are replaced. The terminal blocks are labelled alphabetically with 'A' on the left hand side when viewed from the rear.

Once the unit has been reinstalled, it should be re-commissioned as set out in the Commissioning chapter.

2.3 CLEANING

Warning:
Before cleaning the device, ensure that all AC and DC supplies and transformer connections are isolated, to prevent any chance of an electric shock while cleaning.

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the product's surfaces and leave a conductive residue.

3 TROUBLESHOOTING

3.1 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

3.2 POWER-UP ERRORS

If the IED does not appear to power up, use the following checks to determine whether the fault is in the external wiring, auxiliary fuse, IED power supply module or IED front panel.

Test	Check	Action
1	Measure the voltage on terminals 13 and 14. Verify the voltage level and polarity against the rating label	If the auxiliary voltage is correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply.
2	Check the LEDs and LCD backlight switch on at power-up. Also check the N/O (normally open) watchdog contact on terminals 4 and 6 to see if they close.	If the LEDs and LCD backlight switch on, or the Watchdog contacts close and no error code is displayed, the error is probably on the main processor board. If the LEDs and LCD backlight do not switch on and the N/O Watchdog contact does not close, the fault is probably in the IED power supply module.

3.3 ERROR MESSAGE OR CODE ON POWER-UP

The IED performs a self-test during power-up. If it detects an error, a message appears on the LCD and the power-up sequence stops. If the error occurs when the IED application software is running, a maintenance record is created and the device reboots.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If the IED locks up and displays an error code permanently, go to test 2. If the IED prompts for user input, go to test 3. If the IED reboots automatically, go to test 4.
2	Record displayed error and re-apply IED supply.	Record whether the same error code is displayed when the IED is rebooted, then contact the local service centre stating the error code and product details.
3	The IED displays a message for corrupt settings and prompts for the default values to be restored for the affected settings.	The power-up tests have detected corrupted IED settings. Restore the default settings to allow the power-up to complete, and then reapply the application-specific settings.

Test	Check	Action
4	The IED resets when the power-up is complete. A record error code is displayed.	Programmable scheme logic error due to excessive execution time. If the IED powers up successfully, check the programmable logic for feedback paths. Other error codes relate to software errors on the main processor board, contact the local service centre.

3.4 OUT OF SERVICE LED ON AT POWER-UP

Test	Check	Action	
1	Using the IED menu, confirm the Commission Test or Test Mode setting is Enabled. If it is not Enabled, go to test 2.	If the setting is Enabled, disable the test mode and make sure the Out of Service LED is OFF.	
2	Select the *VIEW RECORDS* column then view the last maintenance record from the menu.	Check for the H/W Verify Fail maintenance record. This indicates a discrepancy between the IED model number and the hardware. Examine the ***Maint Data***; cell. This indicates the causes of the failure using bit fields: Bit Meaning	
		0	The application 'type' field in the Cortec does not match the software ID
		1	The 'subset' field in the model number does not match the software ID
		2	The 'platform' field in the model number does not match the software ID
		3	The 'product type' field in the model number does not match the software ID
		4	The 'protocol' field in the Cortec does not match the software ID
		5	The 'model' field in the Cortec does not match the software ID
		6	The first 'software version' field in the does not match the software ID
		7	The second 'software version' field in the Cortec does not match the software ID
		8	No VTs are fitted
		9	No CTs are fitted
		10	No Earth CT is fitted
		11	No SEF CT is fitted

3.5 ERROR CODE DURING OPERATION

The IED performs continuous self-checking. If the IED detects an error it displays an error message, logs a maintenance record and after a short delay resets itself. A permanent problem (for example due to a hardware fault) is usually detected in the power-up sequence. In this case the IED displays an error code and halts. If the problem was transient, the IED reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

3.6 MAL-OPERATION DURING TESTING

3.6.1 FAILURE OF OUTPUT CONTACTS

An apparent failure of the relay output contacts can be caused by the configuration. Perform the following tests to identify the real cause of the failure. The self-tests verify that the coils of the output relay contacts have been energized. An error is displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED ON?	If this LED is ON, the relay may be in test mode or the protection has been disabled due to a hardware verify error.
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, go to test 4; if not, go to test 3.
3	Examine the fault record or use the test port to check the protection element is operating correctly.	If the protection element does not operate, check the test is correctly applied. If the protection element operates, check the programmable logic to make sure the protection element is correctly mapped to the contacts.
4	Using the Commissioning or Test mode function, apply a test pattern to the relevant relay output contacts. Consult the correct external connection diagram and use a continuity tester at the rear of the relay to check the relay output contacts operate.	If the output relay operates, the problem must be in the external wiring to the relay. If the output relay does not operate the output relay contacts may have failed (the self-tests verify that the relay coil is being energized). Ensure the closed resistance is not too high for the continuity tester to detect.

3.6.2 FAILURE OF OPTO-INPUTS

The opto-isolated inputs are mapped onto the IED's internal DDB signals using the programmable scheme logic. If an input is not recognized by the scheme logic, use the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column to check whether the problem is in the opto-input itself, or the mapping of its signal to the scheme logic functions.

If the device does not correctly read the opto-input state, test the applied signal. Verify the connections to the opto-input using the wiring diagram and the nominal voltage settings in the *OPTO CONFIG* column. To do this:

1. Select the nominal battery voltage for all opto-inputs by selecting one of the five standard ratings in the ***Global Nominal V*** cell.
2. Select `Custom` to set each opto-input individually to a nominal voltage.
3. Using a voltmeter, check that the voltage on its input terminals is greater than the minimum pick-up level (See the Technical Specifications chapter for opto pick-up levels).

If the signal is correctly applied, this indicates failure of an opto-input, in which case the complete cradle should be replaced.

3.6.3 INCORRECT ANALOGUE SIGNALS

If the measured analogue quantities do not seem correct, use the measurement function to determine the type of problem. The measurements can be configured in primary or secondary terms.

1. Compare the displayed measured values with the actual magnitudes at the terminals.
2. Check the correct terminals are used.
3. Check the CT and VT ratios set are correct.
4. Check the phase displacement to confirm the inputs are correctly connected.

3.7 PSL EDITOR TROUBLESHOOTING

A failure to open a connection could be due to one or more of the following:

- The IED address is not valid (this address is always 1 for the front port)
- Password in not valid

- Communication set-up (COM port, Baud rate, or Framing) is not correct
- Transaction values are not suitable for the IED or the type of connection
- The connection cable is not wired correctly or broken
- The option switches on any protocol converter used may be incorrectly set

3.7.1 DIAGRAM RECONSTRUCTION

Although a scheme can be extracted from an IED, a facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals are drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B. Any annotation added to the original diagram such as titles and notes are lost.

Sometimes a gate type does not appear as expected. For example, a single-input AND gate in the original scheme appears as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 also appear as OR gates

3.7.2 PSL VERSION CHECK

The PSL is saved with a version reference, time stamp and CRC check (Cyclic Redundancy Check). This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

3.8 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Return Authorization (RMA) form
   An electronic version of the RMA form is available from the following:
   contact.centre@ge.com
2. Fill in the RMA form
   Fill in only the white part of the form.
   Please ensure that all fields marked **(M)** are completed such as:
   - Equipment model
   - Model No. and Serial No.
   - Description of failure or modification required (please be specific)
   - Value for customs (in case the product requires export)
   - Delivery and invoice addresses
   - Contact details

3. Send the RMA form to your local contact
   For a list of local service contacts worldwide, email us at:
   contact.centre@ge.com
4. The local service contact provides the shipping information
   Your local service contact provides you with all the information needed to ship the product:
   - Pricing details
   - RMA number
   - Repair centre address

   If required, an acceptance of the quote must be delivered before going to the next stage.
5. Send the product to the repair centre
   - Address the shipment to the repair centre specified by your local contact
   - Make sure all items are packaged in an anti-static bag and foam protection
   - Make sure a copy of the import invoice is attached with the returned unit
   - Make sure a copy of the RMA form is attached with the returned unit
   - E-mail or fax a copy of the import invoice and airway bill document to your local contact.

CHAPTER 22

TECHNICAL SPECIFICATIONS

1 CHAPTER OVERVIEW

This chapter describes the technical specifications of the product.

This chapter contains the following sections:

2 INTERFACES

2.1 FRONT USB PORT

Front USB port	
Use	For local connection to laptop for configuration purposes and firmware downloads
Connector	USB type B
Isolation	Isolation to ELV level
Constraints	Maximum cable length 5 m

2.2 REAR SERIAL PORT 1

Rear serial port 1 (RP1)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus
Connector	General purpose block, M4 screws (2 wire)
Cable	Screened twisted pair (STP)
Supported Protocols *	Courier, IEC-60870-5-103, DNP3.0, MODBUS
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m

* Not all models support all protocols - see ordering options

2.3 REAR SERIAL PORT 2

Optional rear serial port (RP2)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus, EIA(RS)232
Connector	General purpose block, M4 screws (2 wire)
Cable	Screened twisted pair (STP)
Supported Protocols	Courier
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m

2.4 IRIG-B PORT

IRIG-B Interface (De-modulated)	
Use	External clock synchronization signal
Standard	IRIG 200-98 format B00X
Terminal type	MiDOS
Connector	General purpose block, M4 screws (2 wire)
Cable type	Screened twisted pair (STP)
Isolation	Isolation to SELV level
Accuracy	< +/- 1 s per day

2.5 REAR ETHERNET PORT COPPER

Rear Ethernet port using CAT 5/6/7 wiring	
Main Use	Substation Ethernet communications
Communication protocol	10BaseT/100BaseTX
Connector	RJ45
Cable type	Screened twisted pair (STP)
Isolation	1 kV
Supported Protocols	IEC 61850, DNP3.0 OE
Constraints	Maximum cable length 100 m

2.6 REAR ETHERNET PORT - FIBRE

Rear Ethernet port using fibre-optic cabling	
Main Use	IEC 61850 or DNP3 OE SCADA communications
Connector	UNI SONET OC-3 LC (1 each for Tx and Rx)
Communication protocol	100 BaseFX
Fibre type	Multimode 50/125 µm or 62.5/125 µm
Supported Protocols	IEC 61850, DNP3.0 OE
Wavelength	1300 nm

2.6.1 100 BASE FX RECEIVER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	–31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Conditions: TA = 0°C to 70°C

2.6.2 100 BASE FX TRANSMITTER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power BOL 62.5/125 µm NA = 0.275 Fibre EOL	PO	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm NA = 0.20 Fibre EOL	PO	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic "0" State	PO			-45	dBm avg.

Conditions: TA = 0°C to 70°C

3 PERFORMANCE OF CURRENT PROTECTION FUNCTIONS

3.1 THREE-PHASE OVERCURRENT PROTECTION

IDMT pick-up	1.05 x Setting +/-5%
DT Pick-up	Setting +/- 5%
Drop-off (IDMT and DT)	0.95 x setting +/- 5%
IDMT operation (for IEC and UK curves)	+/- 5% or 60 ms, whichever is greater (1.05 – <2) Is +/- 5% or 40 ms, whichever is greater (2 – 20) Is
IDMT operation (IEEE and US curves) For TD setting < 100s	+/- 5% or 60 ms, whichever is greater (1.05 – <2) Is +/- 5% or 40 ms, whichever is greater (2 – 20) Is
IDMT operation (IEEE and US curves) For TD setting > 100s	+/- 15% (1.05 - 20) Is
Disengagement	< 40 ms
DT operate	+/- 2% or 70 ms, whichever is greater (1.05 – <2) Is +/- 2% or 50 ms, whichever is greater (2 – 20) Is
DT reset	Setting +/- 5%
Repeatability	+/- 2.5%
Overshoot of overcurrent elements	<30 ms

3.1.1 THREE-PHASE OVERCURRENT DIRECTIONAL PARAMETERS

Directional boundary accuracy (RCA +/-90%)	+/-2° with hysteresis <3°
IDMT operate	+/- 5% or 70 ms, whichever is greater (1.05 – <2) Is +/- 2% or 50 ms, whichever is greater (2 – 20) Is
Disengagement	< 40 ms
DT operate	+/- 2% or 80 ms, whichever is greater (1.05 – <2) Is +/- 2% or 60 ms, whichever is greater (2 – 20) Is
DT reset	Setting +/-5%

3.2 EARTH FAULT PROTECTION

Measured and Derived	
IDMT pick-up	1.05 x Setting +/-5%
DT Pick-up	Setting +/- 5%
Drop-off (IDMT and DT) for IN1	0.95 x Setting +/-5%
Drop-off (IDMT and DT) for IN2	0.9 x Setting +/-5%
IDMT operate	+/- 5% or 60 ms, whichever is greater (1.05 – 2) Is +/- 5% or 40 ms, whichever is greater (2 – 20) Is
Disengagement	< 40 ms
DT operate	+/- 2% or 70 ms, whichever is greater (1.05 – 2) Is +/- 2% or 50 ms, whichever is greater (2 – 20) Is
DT reset	Setting +/- 5%
Repeatability	+/- 2.5% (measured), +/-5% (derived)

3.2.1 EARTH FAULT DIRECTIONAL PARAMETERS

Zero Sequence Polarising accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2°
Hysteresis	<3°
VN> pick-up	Setting+/-10%
VN> drop-off	0.9 x Setting +/-10%

Negative Sequence Polarising accuracy	
Directional boundary pick-up (RCA +/- 90°)	+/-2°
Hysteresis	<3°
VN2> pick-up	Setting+/-10%
VN2> drop-off	0.9 x Setting +/-10%
IN2> pick-up	Setting+/-10%
IN2> drop-off	0.9 x Setting +/-10%

3.3 SENSITIVE EARTH FAULT PROTECTION

IDMT pick-up	1.05 x Setting +/-5%
DT Pick-up	Setting +/- 5%
Drop-off (IDMT + DT)	0.95 x Setting +/-5%
IDMT operate	+/- 2% or 70 ms, whichever is greater (1.05 - <2) Is +/- 2% or 50 ms, whichever is greater (2 - 20) Is
Disengagement	< 40 ms
DT operate	+/- 2% or 70 ms, whichever is greater (1.05 - <2) Is +/- 2% or 50 ms, whichever is greater (2 - 20) Is
DT reset	Setting +/- 5%
Repeatability	+/- 5%

Note:
SEF claims apply to SEF input currents of no more than 2 x In. For input ranges above 2 x In, the claim is not supported.

3.3.1 SEF DIRECTIONAL PARAMETERS

Wattmetric SEF accuracy	
Pick-up for P = 0 W	ISEF > +/-5% or 5 mA
Pick-up for P > 0 W	P > +/-5%
Drop-off for P = 0 W	0.95 x ISEF> +/- 5% or 5 mA
Drop-off for P > 0 W	0.9 x P> +/- 5% or 5 mA
Boundary accuracy	+/-5% with hysteresis < 1°
Repeatability	+/- 5%

SEF CosΦ accuracy	
Pick-up	Setting +/-5% for angles RCA+/-60°

SEF CosΦ accuracy	
Drop-off	0.9 x setting
Repeatability	+/- 2%

SEF SinΦ accuracy	
Pick-up	Setting +/-5% for angles RCA+/-60° to RCA+/-90°
Drop-off	0.9 x setting
Repeatability	+/- 2%

3.4 RESTRICTED EARTH FAULT PROTECTION

High Impedance Retricted Earth Fault (REF) accuracy	
Pick-up	Setting formula +/- 5%
Drop-off	0.95 x Setting formula +/-5%
Operating time	< 30 ms
High pick-up	Setting +/- 10%
Repeatability	< 15%

Low Impedance Retricted Earth Fault (REF) accuracy	
Pick-up	Setting formula +/- 5%
Drop-off	0.9 x Setting formula +/-5%
Operating time	< 60 ms
High pick-up	Setting +/- 5%
Repeatability	< 15%

3.5 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

IDMT pick-up	1.05 x Setting +/-5%
DT pick-up	Setting +/- 5%
Drop-off (IDMT + DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 60 ms, whichever is greater (1.05 – <2) Is +/- 5% or 40 ms, whichever is greater (2 – 20) Is
Disengagement	< 40 ms
DT operate	+/- 2% or 70 ms, whichever is greater (1.05 – <2) Is +/- 2% or 50 ms, whichever is greater (2 – 20) Is
DT Reset	Setting +/- 5%

3.5.1 NPSOC DIRECTIONAL PARAMETERS

Directional boundary pick-up (RCA +/-90%)	+/- 2°
Directional boundary hysteresis	< 1°
IDMT operate	+/- 5% or 70 ms, whichever is greater (1.05 – <2) Is +/- 5% or 50 ms, whichever is greater (2 – 20) Is

IDMT reset	< 40 ms
DT operate	+/- 2% or 80 ms, whichever is greater (1.05 – <2) Is +/- 2% or 60 ms, whichever is greater (2 – 20) Is
DT reset	Setting +/- 5%

3.6 CIRCUIT BREAKER FAIL AND UNDERCURRENT PROTECTION

I< Pick-up	Setting +/- 5% or 20 mA, whichever is greater
I< Drop-off	100% of setting +/- 5% or 20 mA, whichever is greater
Timers	+/- 2% or 50 ms, whichever is greater
Reset time	< 35 ms

3.7 BROKEN CONDUCTOR PROTECTION

Pick-up	Setting +/- 2.5%
Drop-off	0.95 x Setting +/- 2.5%
DT operate	+/- 2% or 55 ms, whichever is greater

3.8 THERMAL OVERLOAD PROTECTION

Thermal alarm pick-up	Calculated trip time +/- 10%
Thermal overload pick-up	Calculated trip time +/- 10%
Cooling time accuracy	+/- 15% of theoretical
Repeatability	<5%

Note:
Operating time measured with applied current of 20% above thermal setting.

3.9 COLD LOAD PICKUP PROTECTION

I> Pick-up	Setting +/- 1.5%
IN> Pick-up	Setting +/- 1.5%
I> Drop-off	0.95 x Setting +/- 1.5%
IN> Drop-off	0.95 x Setting +/- 1.5%
DT operate	+/- 0.5% or 50 ms, whichever is greater
Repeatability	+/- 1%

3.10 SELECTIVE OVERCURRENT PROTECTION

Fast Block operation	< 25 ms
Fast Block reset	< 30 ms
Time delay	Setting +/- 2% or 20 ms, whichever is greater

3.11 VOLTAGE DEPENDENT OVERCURRENT PROTECTION

VCO/VRO threshold pick-up	Setting +/- 5%
Overcurrent pick-up	K-factor x setting +/- 5%
VCO/VRO threshold drop-off	1.05 x setting +/- 5%
Overcurrent drop-off	0.95(K-factor x setting) +/- 5%
Operating time	+/- 5% or 60 ms, whichever is greater
Repeatability	< 5%

3.12 NEUTRAL ADMITTANCE PROTECTION

YN, BN, GN measurements	+/-5%
YN, BN, GN pick-up	Setting +/-5%
YN, BN, GN drop-off	0.85 x setting +/-5%
DT operate	+/- 2% or 50 ms, whichever is greater
DT reset	Setting +/- 5%
Disengagement	< 40 ms
Directional boundary accuracy	+/- 2°
VN	Setting +/-5%

4 PERFORMANCE OF VOLTAGE PROTECTION FUNCTIONS

4.1 UNDERVOLTAGE PROTECTION

Pick-up (IDMT and DT)	Setting +/- 5%
Drop-off (IDMT and DT)	1.02 x Setting +/-5%
IDMT operate	+/- 3.5% or 40 ms, whichever is greater (<10 V) +/- 5% or 40 ms, whichever is greater (>10 V)
Disnegagement	<40 ms
DT operate	+/- 2% or 50 ms, whichever is greater
DT reset	Setting +/- 5%
Repeatability	+/- 1%

4.2 OVERVOLTAGE PROTECTION

IDMT pick-up	Setting +/- 2%
DT pick-up	Setting +/- 1%
Drop-off (IDMT and DT)	0.98 x Setting +/-5%
IDMT operate	+/-5% or 50 ms
Disengagement	< 40 ms
DT operate	+/- 2% or 50 ms, whichever is greater
DT reset	Setting +/- 5%
Repeatability	+/- 5%

4.3 RESIDUAL OVERVOLTAGE PROTECTION

IDMT pick-up	1.05 x Setting +/- 5%
DT pick-up	Setting +/- 5%
Drop-off (IDMT and DT)	0.95 x Setting +/-5%
IDMT operate	+/- 5% or 65 ms, whichever is greater
Disengagement	< 35 ms
DT operate	+/- 2% or 70 ms or whichever is greater
DT reset	Setting +/- 5%
Repeatability	<10%

4.4 NEGATIVE SEQUENCE VOLTAGE PROTECTION

Accuracy	
Pick-up	Setting +/- 5%
Drop-off	0.95 x Setting +/-5%

Accuracy	
DT operate (normal operation)	+/- 5% or 70 ms, whichever is greater (<45 Hz) +/- 2% or 65 ms, whichever is greater (45 Hz - 70 Hz)
DT operate (accelerated)	+/- 5% or 50 ms, whichever is greater (<45 Hz) +/- 2% or 45 ms, whichever is greater (45 Hz - 70 Hz)
Repeatability	+/- 1%

4.5 RATE OF CHANGE OF VOLTAGE PROTECTION

Accuracy for 110 V VT	
Tolerance	1% or 0.07, whichever is greater
Pick-up	Setting +/- tolerance
Drop-off for positive direction	(Setting – 0.07)+/- tolerance
Drop-off for negative direction	(Setting + 0.07)+/- tolerance
Operating time at 50 Hz	(Average cycle x 20) +60 ms
Reset time at 50 Hz	40 ms

5 PERFORMANCE OF FREQUENCY PROTECTION FUNCTIONS

5.1 OVERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/- 10 mHz
Drop-off	Setting -20 mHz +/- 10 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (Fs/Ff ratio less than 2)	<125 ms
Operating time (Fs/Ff ratio between 2 and 30)	<150 ms
Operating time (Fs/Ff ratio greater than 30)	<200 ms
Reset time	<200 ms

Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.

Fs = start frequency – frequency setting

Ff = frequency setting – end frequency

5.2 UNDERFREQUENCY PROTECTION

Accuracy	
Pick-up	Setting +/- 10 mHz
Drop-off	Setting + 20 mHz +/- 10 mHz
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (Fs/Ff ratio less than 2)	<100 ms
Operating time (Fs/Ff ratio between 2 and 6)	<160 ms
Operating time (Fs/Ff ratio greater than 6)	<230 ms
Reset time	<200 ms

Reference conditions: Tested using step changed in frequency with Freq. Av Cycles setting = 0 and no intentional time delay.

Fs = start frequency – frequency setting

Ff = frequency setting – end frequency

5.3 SUPERVISED RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (f)	Setting +/- 10 mHz
Pick-up (df/dt)	Setting +/- 3% or +/- 10 mHz/s, whichever is greater

Accuracy	
Drop-off (f, underfrequency)	(Setting + 20 mHz) +/- 10 mHz
Drop-off (f, overfrequency)	(Setting - 20 mHz) +/- 10 mHz
Drop-off (df/dt, falling, for settings between 10 mHz/s and 100 mHz/s)	(Setting + 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, falling, for settings greater than 100 mHz/s)	(Setting + 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater
Drop-off (df/dt, rising, for settings between 10 mHz/s and 100 mHz/s)	(Setting - 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, rising, for settings greater than 100 mHz/s)	(Setting - 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater

Operating and Reset time	
Instantaneous operating time (Freq AvCycles setting = 0)	<125 ms
Reset time time (df/dt AvCycles setting = 0)	<400 ms

5.4 INDEPENDENT RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (df/dt)	Setting +/- 3% or +/- 10 mHz/s, whichever is greater
Drop-off (df/dt, falling, for settings between 10 mHz/s and 100 mHz/s)	(Setting + 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, falling, for settings greater than 100 mHz/s)	(Setting + 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater
Drop-off (df/dt, rising, for settings between 10 mHz/s and 100 mHz/s)	(Setting - 5 mHz/s) +/- 10 mHz/s
Drop-off (df/dt, rising, for settings greater than 100 mHz/s)	(Setting - 50 mHz/s) +/- 5% or +/- 55 mHz/s, whichever is greater
Operating timer	+/- 2% or 50 ms, whichever is greater

Operating and Reset time	
Operating time (for ramps 2 x seting or greater)	<200 ms
Operating time (for ramps 1.3 x seting or greater)	<300 ms
Reset time time (df/dt AvCycles setting = 0 for df/dt settings greater than 0.1 Hz/s and no intentional time delay)	<250 ms

Referecne Conditions: Tested with df/dt Average Cycles = 0 for df/dt settings greater than 0.1 Hz/s, and no intentional time delay.

5.5 AVERAGE RATE OF CHANGE OF FREQUENCY PROTECTION

Accuracy	
Pick-up (f)	Setting +/- 10 mHz
Pick-up (Df/Dt)	Setting +/- 100 mHz/s
Drop-off (falling)	(Setting + 20 mHz) +/- 10 mHz
Drop-off (rising)	(Setting - 20 mHz) +/- 10 mHz
Operating timer	+/- 2% or 30 ms, whichever is greater

Operating time	
Operating time (Freq. Av Cycles setting = 0)	<125 ms

Reference conditions: To maintain accuracy, the minimum time delay setting should be:

Dt> 0.375 x Df + 0.23 (f0r Df setting <1 Hz)

Dt> 0.156 x Df + 0.47 (for Df setting >= 1 Hz)

5.6 LOAD RESTORATION

Pick-up	Setting +/- 2.5%
Drop-off	0.95% x Setting +/- 2.5%
Restoration timer	+/- 2% or 50 ms, whichever is greater
Holding timer	+/- 2% or 50 ms, whichever is greater

6 POWER PROTECTION FUNCTIONS

6.1 OVERPOWER / UNDERPOWER PROTECTION

Pick-up	Setting +/- 10%
Reverse/Overpower Drop-off	0.95 x Setting +/- 10%
Low forward power Drop-off	1.05 x Setting +/- 10%
Angle variation pick-up	+/- 2°
Angle variation drop-off	+/- 2.5°
Operating time	+/- 2% or 50 ms, whichever is greater
Repeatability	< 5%
Disengagement time	<50 ms
tRESET	+/- 5%
Instantaneous operating time	< 50 ms

6.2 SENSITIVE POWER PROTECTION

Pick-up	Setting +/- 10%
Reverse/Overpower Drop-off	0.9 x Setting +/- 10%
Low forward power Drop-off	1.1 x Setting +/- 10%
Angle variation pick-up	+/- 2°
Angle variation drop-off	+/- 2.5°
Operating time	+/- 2% or 50 ms, whichever is greater
Repeatability	< 5%
Disengagement time	<50 ms
tRESET	+/- 5%
Instantaneous operating time	< 50 ms

6.3 WATTMETRIC EARTH FAULT PROTECTION

Pickup	Setting +/- 10%
Dropoff	0.95 x setting +/- 10%
Operating time	+/- 5% or 50 ms, whichever is greater
Disengagement time	< 50 ms
Instantaneous operating time	< 50 ms

7 PERFORMANCE OF MONITORING AND CONTROL FUNCTIONS

7.1 VOLTAGE TRANSFORMER SUPERVISION

Fast block operation	< 25 ms
Fast block reset	< 40 ms
Time delay	+/- 2% or 40 ms, whichever is greater

7.2 CURRENT TRANSFORMER SUPERVISION

IN> Pick-up	Setting +/- 5%
VN< Pick-up	Setting +/- 5%
IN> Drop-off	0.9 x setting +/- 5%
VN< Drop-off	1.05 x setting +/-5% or 1 V, whichever is greater
Time delay operation	Setting +/-2% or 20 ms, whichever is greater
CTS block operation	< 1.1 cycles
CTS reset	< 40 ms

7.3 CB STATE AND CONDITION MONITORING

Timers	+/- 40 ms or 2%, whichever is greater
Broken current accuracy	< +/- 5%

7.4 PSL TIMERS

Output conditioner timer	Setting +/- 2% or 50 ms, whichever is greater
Dwell conditioner timer	Setting +/- 2% or 50 ms, whichever is greater
Pulse conditioner timer	Setting +/- 2% or 50 ms, whichever is greater

7.5 CHECK SYNCHRONISATION

Accuracy (CS1/CS2)	
Phase Angle	
Pick-up	(Setting-2°) ±1°
Drop-off	(Setting-1°) ±1°
Repeatability	<1%
Slip Frequency	
Pick-up	Setting ±0.01 Hz
Drop-off	0.95 x Setting) ±0.01 Hz

Accuracy (CS1/CS2)	
Repeatability	<1%
Slip Timer	
Timers	+/- 1% or 40 ms, whichever is greater
Reset Time	<30 ms
Repeatability	<10 ms

7.6 DC SUPPLY MONITOR

Measuring Range	19 V-310 V ±5%
Tolerance	±1.5 V for 19-100 V ±2% for 100-200 V ±2.5% for 200-300 V
Pickup	100% of Setting ± Tolerance *
Dropoff	Hysteresis 2% 102% of Setting ± Tolerance for the upper limit * 98% of Setting ± Tolerance for the lower limit *
Operate Time	Setting ± (2% or 500 ms whichever is greater)
Disengagement Time	< 250 ms

Note:
** Tested at 21°C*

8 MEASUREMENTS AND RECORDING

8.1 GENERAL

General Measurement Accuracy at 20° C	
General measurement accuracy	Typically +/- 1%, but +/- 0.5% between 0.2 - 2 In/Vn
Current magnitude	0.05 to 4 In +/- 0.5% of reading (1A input) 0.05 to 4 In +/- 1.0% of reading (5A input)
Voltage magnitude	0.05 to 2 Vn +/- 1.0% of reading
Current phase	0° to 360° +/- 0.5° (0.05 to 4 In for 1A input) 0° to 360° +/- 1° (0.05 to 4 In for 5A input)
Voltage phase	0° to 360° +/- 0.5° (0.2 to 2 Vn) 0° to 360° +/- 1° (0.05 to 2 Vn)
Frequency	40 to 70 Hz +/- 0.025 Hz
Power (W)	0.2 to 2 Vn and 0.05 to 3 In +/- 5.0% of reading at unity power factor
Reactive power (Vars)	0.2 to 2 Vn and 0.05 to 3 In +/- 5.0% of reading at zero power factor
Apparent power (VA)	0.2 to 2 Vn and 0.05 to 3 In +/- 5.0% of reading
Energy (Wh)	0.2 to 2 Vn and 0.2 to 3 In +/- 5.0% of reading at zero power factor
Energy (Varh)	0.2 to 2 Vn and 0.2 to 3 In +/- 5.0% of reading at zero power factor

8.2 DISTURBANCE RECORDS

Disturbance Records Measurement Accuracy	
Minimum record duration	0.1 s
Maximum record duration	10.5 s
Minimum number of records at 10.5 seconds	15
Magnitude and relative phases accuracy	±5% of applied quantities
Duration accuracy	±2%
Trigger position accuracy	±2% (minimum Trigger 100 ms)

8.3 EVENT, FAULT AND MAINTENANCE RECORDS

Event, Fault & Maintenance Records	
Record location	Flash memory
Viewing method	Front panel display or MiCOM S1 Agile
Extraction method	Extracted via the USB port
Number of Event records	Up to 2048 time tagged event records
Number of Fault Records	Up to 10
Number of Maintenance Records	Up to 10

8.4 FAULT LOCATOR

Accuracy	
Fault Location	+/- 3.5% of line length up to SIR 30 Reference conditions: solid fault applied on line

9 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

9.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

9.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

9.3 R&TTE COMPLIANCE: 2014/53/EU

Radio and Telecommunications Terminal Equipment (R&TTE) directive 2014/53/EU.

Conformity is demonstrated by compliance to both the EMC directive and the Low Voltage directive, to zero volts.

9.4 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

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10 MECHANICAL SPECIFICATIONS

10.1 PHYSICAL PARAMETERS

Physical Measurements	
Case Types	20TE 30TE 40TE
Weight (20TE case)	2 kg – 3 kg (depending on chosen options)
Weight (30TE case)	3 kg – 4 kg (depending on chosen options)
Weight (40TE case)	5.5 kg
Dimensions in mm (w x h x l) (20TE case)	W: 102.4mm H: 177.0mm D: 243.1mm
Dimensions in mm (w x h x l) (30TE case)	W: 154.2mm H: 177.0mm D: 243.1mm
Dimensions in mm (w x h x l) (40TE case)	W: 206.0mm H: 177.0mm D: 243.1mm
Mounting	Panel, rack, or retrofit

10.2 ENCLOSURE PROTECTION

Against dust and dripping water (front face)	IP52 as per IEC 60529:1989/A2:2013
Protection against dust (whole case)	IP50 as per IEC 60529:1989/A2:2013
Protection for sides of the case (safety)	IP30 as per IEC 60529:1989/A2:2013
Protection for rear of the case (safety)	IP10 as per IEC 60529:1989/A2:2013

10.3 MECHANICAL ROBUSTNESS

Vibration test per EN 60255-21-1:1998	Response: class 2, Endurance: class 2
Shock and bump immunity per EN 60255-21-2:1988	Shock response: class 2, Shock withstand: class 1, Bump withstand: class 1
Seismic test per EN 60255-21-3: 1993	Class 2

10.4 TRANSIT PACKAGING PERFORMANCE

Primary packaging carton protection	ISTA 1C
Vibration tests	3 orientations, 7 Hz, amplitude 5.3 mm, acceleration 1.05g
Drop tests	10 drops from 610 mm height on multiple carton faces, edges and corners

11 RATINGS

11.1 AC MEASURING INPUTS

AC Measuring Inputs	
Nominal frequency	50 Hz or 60 Hz (settable)
Operating range	40 Hz to 70 Hz
Phase rotation	ABC or CBA

11.2 CURRENT TRANSFORMER INPUTS

AC Current	
Nominal current (In)	1 A and 5 A dual rated*
Nominal burden per phase	< 0.05 VA at In
AC current thermal withstand	Continuous: 4 x In 10 s: 30 x In 1 s: 100 x In Linear to 40 x In (non-offset ac current)

Note:
A single input is used for both 1 A and 5 A applications. 1 A or 5 A operation is determined by means of software in the product's database.

Note:
These specifications are applicable to all CTs.

11.3 VOLTAGE TRANSFORMER INPUTS

AC Voltage	
Nominal voltage	100 V to 120 V
Nominal burden per phase	< 0.1 VA at Vn
Thermal withstand	Continuous: 2 x Vn, 10 s: 2.6 x Vn

12 POWER SUPPLY

12.1 AUXILIARY POWER SUPPLY VOLTAGE

Nominal operating range	24-250 V DC +/-20% 110-240 V AC -20% + 10%
Maximum operating range	19 to 300 V DC
Frequency range for AC supply	45 – 65 Hz
Ripple	<15% for a DC supply (compliant with IEC 60255-11:2008)

12.2 NOMINAL BURDEN

Quiescent burden	20TE	5 W max.
	30TE	6 W max.
	30TE with 2nd rear communications	6.2 W max.
	30TE with Ethernet or TCS	7 W max.
	40TE	8 W max.
Additions for energised relay outputs		0.26 W per output relay
Opto-input burden	24 V	0.065 W max.
	48 V	0.125 W max.
	110 V	0.36 W max.
	220 V	0.9 W max.

12.3 AUXILIARY POWER SUPPLY INTERRUPTION

Standard	IEC 60255-11:2008 (dc) IEC 61000-4-11:2004 (ac)			
	Quiescent / half load		Full load	
	19.2 V – 110 V dc	>110 V dc	19.2 V – 110 V dc	>110 V dc
20TE	50 ms	100 ms	50 ms	100 ms
30TE	50 ms	100 ms	30 ms	50 ms
30TE with 2nd rear communications	30 ms	100 ms	20 ms	50 ms
30TE with Ethernet or TCS	50 ms	100 ms	20 ms	100 ms
30TE with Redundant Ethernet Board	50 ms	100 ms	10 ms	100 ms
40TE with 2nd rear communications	20 ms	100 ms	10 ms*	50 ms

* for voltages > 48 V dc

Note:
Maximum loading = all inputs/outputs energised. Quiescent or 1/2 loading = 1/2 of all inputs/outputs energised.

13 INPUT / OUTPUT CONNECTIONS

13.1 ISOLATED DIGITAL INPUTS

Opto-isolated digital inputs (opto-inputs)	
Compliance	ESI 48-4
Rated nominal voltage	24 to 250 V dc
Operating range	19 to 265 V dc
Withstand	300 V dc
Recognition time with half-cycle ac immunity filter removed	< 2 ms
Recognition time with filter on	< 12 ms

13.1.1 NOMINAL PICKUP AND RESET THRESHOLDS

Nominal battery voltage	Logic levels: 60-80% DO/PU	Logic Levels: 50-70% DO/PU	Logic Levels: 58-75% DO/PU
24/27 V	Logic 0 < 16.2V, Logic 1 > 19.2V	Logic 0 <12V, Logic 1 > 16.8V	Logic 0 <15.7V, Logic 1 > 18V
30/34	Logic 0 < 20.4V, Logic 1 > 24V	Logic 0 < 15V, Logic 1 > 21V	Logic 0 < 19.7V, Logic 1 > 22.5V
48/54	Logic 0 < 32.4V, Logic 1 > 38.4V	Logic 0 < 24V, Logic 1 > 33.6V	Logic 0 < 31.3V, Logic 1 > 36V
110/125	Logic 0 < 75V, Logic 1 > 88V	Logic 0 < 55.V, Logic 1 > 77V	Logic 0 < 72.5V, Logic 1 > 82.5V
220/250	Logic 0 < 150V, Logic 1 > 176V	Logic 0 < 110V, Logic 1 > 154V	Logic 0 < 145V, Logic 1 > 165V

Note:
Filter is required to make the opto-inputs immune to induced AC voltages.

13.2 STANDARD OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	General purpose relay outputs for signalling, tripping and alarming
Rated voltage	300 V
Maximum continuous current	10 A
Short duration withstand carry	30 A for 3 s 250 A for 30 ms
Make and break, dc resistive	50 W
Make and break, dc inductive	62.5 W (L/R = 50 ms)
Make and break, ac resistive	2500 VA resistive (cos phi = unity)
Make and break, ac inductive	2500 VA inductive (cos phi = 0.7)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to a maximum load of 7500W))
Make, carry and break, dc resistive	4 A for 1.5 s, 10000 operations (subject to the above limit for make and break, dc resistive load)
Make, carry and break, dc inductive	0.5 A for 1 s, 10000 operations (subject to the above limit for make and break, dc inductive load)
Make, carry and break ac resistive	30 A for 200 ms, 2000 operations (subject to the above limits)

Make, carry and break ac inductive	10 A for 1.5 s, 10000 operations (subject to the above limits)
Loaded contact	10000 operations min.
Unloaded contact	100000 operations min.
Operate time	< 5 ms
Reset time	< 10 ms

13.3 WATCHDOG CONTACTS

Use	Non-programmable contacts for relay healthy/relay fail indication
Breaking capacity, dc resistive	30 W
Breaking capacity, dc inductive	15 W (L/R = 40 ms)
Breaking capacity, ac inductive	375 VA inductive (cos phi = 0.7)

13.4 SHORTING LINK

Maximum operating voltage	300Vrms, 300Vdc
Maximum operating current	20A

14 ENVIRONMENTAL CONDITIONS

14.1 AMBIENT TEMPERATURE RANGE

Compliance	IEC 60255-27: 2013
Test Method	IEC 60068-2-1:2007 and IEC 60068-2-2 2007
Operating temperature range	-25°C to +55°C (continuous)
Storage and transit temperature range	-25°C to +70°C (continuous)

14.2 TEMPERATURE ENDURANCE TEST

Temperature Endurance Test	
Test Method	IEC 60068-2-1: 2007 and 60068-2-2: 2007
Operating temperature range	-40°C (96 hours) +70°C (96 hours)
Storage and transit temperature range	-40°C (96 hours) +85°C (96 hours)

14.3 AMBIENT HUMIDITY RANGE

Compliance	IEC 60068-2-78: 2013 and IEC 60068-2-30: 2005
Durability	56 days at 93% relative humidity and +40°C
Damp heat cyclic	six (12 + 12) hour cycles, 93% RH, +25 to +55°C

14.4 CORROSIVE ENVIRONMENTS

Compliance	IEC 60068-2-42: 2003, IEC 60068-2-43: 2003
Industrial corrosive environment/poor environmental control, Sulphur Dioxide	21 days exposure to elevated concentrations (25ppm) of SO_2 at 75% relative humidity and +25°C
Industrial corrosive environment/poor environmental control, Hydrogen Sulphide	21 days exposure to elevated concentrations (10ppm) of H_2S at 75% relative humidity and +25°C
Salt mist	IEC 60068-2-52: 1996 KB severity 3

15 TYPE TESTS

15.1 INSULATION

Compliance	IEC 60255-27: 2013
Insulation resistance	> 100 M ohm at 500 V DC (Using only electronic/brushless insulation tester)

15.2 CREEPAGE DISTANCES AND CLEARANCES

Compliance	IEC 60255-27: 2013
Pollution degree	3
Overvoltage category	III
Impulse test voltage (not RJ45)	5 kV
Impulse test voltage (RJ45)	1 kV

15.3 HIGH VOLTAGE (DIELECTRIC) WITHSTAND

IEC Compliance	IEC 60255-27: 2005
Between independent opto-inputs or Vx and other circuits	2.82kV dc for 1 minute
Between all other independent circuits	2 kV ac rms for 1 minute
Between Vx or opto-inputs, and protective earth terminal	2.82kV dc for 1 minute
Between all other independent circuits and protective earth terminal	2 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute
Across open contacts of changeover output relays	1 kV ac rms for 1 minute
Between all RJ45 contacts and protective earth terminal	1 kV ac rms for 1 minute
Between all screw-type EIA(RS)485 contacts and protective earth terminal	1 kV ac rms for 1 minute
ANSI/IEEE Compliance	ANSI/IEEE C37.90-2005
Across open contacts of normally open output relays	1.5 kV ac rms for 1 minute
Across open contacts of normally open changeover output relays	1 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute

15.4 IMPULSE VOLTAGE WITHSTAND TEST

Compliance	IEC 60255-27: 2013
Between all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between terminals of all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between all independent circuits and protective earth conductor terminal	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J

Note:
Exceptions are communications ports and normally-open output contacts, where applicable.

16 ELECTROMAGNETIC COMPATIBILITY

16.1 1 MHZ BURST HIGH FREQUENCY DISTURBANCE TEST

Compliance	IEC 60255-22-1: 2008, Class III, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Differential test voltage (level 3)	1.0 kV

16.2 DAMPED OSCILLATORY TEST

Compliance	EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz. Level 4: 3 MHz, 10 MHz and 30 MHz, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Common-mode test voltage (level 4)	4.0 kV
Differential mode test voltage	1.0 kV

16.3 IMMUNITY TO ELECTROSTATIC DISCHARGE

Compliance	IEC 60255-26:2013
Class 4 Condition (20TE, 30TE)	15 kV discharge in air to user interface, display, and exposed metalwork 8 kV contact discharge to communication ports and exposed metalwork
Class 3 Condition (40TE)	6 kV contact discharge to communication ports and exposed metalwork

16.4 ELECTRICAL FAST TRANSIENT OR BURST REQUIREMENTS

Compliance	IEC 60255-26:2013, IEC 61000-4-4:2012
Applied to communication inputs	Amplitude: 2 kV, burst frequency 5 kHz and 100 KHz (level 4)
Applied to power supply and all other inputs except for communication inputs	Amplitude: 4 kV, burst frequency 5 kHz and 100 KHz (level 4)

16.5 SURGE WITHSTAND CAPABILITY

Compliance	IEEE/ANSI C37.90.1: 2002
Condition 1	4 kV fast transient and 2.5 kV oscillatory applied common mode and differential mode to opto inputs, output relays, CTs, VTs, power supply
Condition 2	4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B

16.6 SURGE IMMUNITY TEST

Compliance	IEC 60255-26:2013, IEC 61000-4-5:2014+AMD1:2017
Pulse duration	Time to half-value: 1.2/50 µs
Between all groups and protective earth conductor terminal	Amplitude 4 kV
Between terminals of each group (excluding communications ports, where applicable)	Amplitude 2 kV

16.7 IMMUNITY TO RADIATED ELECTROMAGNETIC ENERGY

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency band	80 MHz to 3.0 GHz
Spot tests at	80, 160, 380, 450, 900, 1850, 2150 MHz
Test field strength	10 V/m
Test using AM	1 kHz @ 80%
Compliance	IEEE/ANSI C37.90.2: 2004
Frequency band	80 MHz to 1 GHz
Spot tests at	80, 160, 380, 450 MHz
Waveform	1 kHz @ 80% am and pulse modulated
Field strength	35 V/m

16.8 RADIATED IMMUNITY FROM DIGITAL COMMUNICATIONS

Compliance	IEC 61000-4-3:2006 + A2:2010
Frequency bands	800 to 960 MHz, 1.4 to 2.0 GHz
Test field strength	30 V/m
Test using AM	1 kHz / 80%

16.9 RADIATED IMMUNITY FROM DIGITAL RADIO TELEPHONES

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency bands	900 MHz and 1.89 GHz
Test field strength	10 V/m

16.10 IMMUNITY TO CONDUCTED DISTURBANCES INDUCED BY RADIO FREQUENCY FIELDS

Compliance	IEC 60255-26:2013, IEC 61000-4-6:2013 Level 3
Frequency bands	150 kHz to 80 MHz

Test disturbance voltage	10 V rms
Test using AM	1 kHz @ 80%
Spot tests	27 MHz and 68 MHz

16.11 MAGNETIC FIELD IMMUNITY

Compliance	IEC 61000-4-8:2009 Level 5 IEC 61000-4-9:2016 Level 5 IEC 61000-4-10:2016 Level 5
IEC 61000-4-8 test	100 A/m applied continuously, 1000 A/m applied for 3 s
IEC 61000-4-9 test	1000 A/m applied in all planes
IEC 61000-4-10 test	100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 seconds

16.12 CONDUCTED EMISSIONS

Compliance	IEC 60255-26:2013, EN 55016-2-1:2014
Power supply test 1	0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
Power supply test 2	0.5 – 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)
RJ45 test 1 (where applicable)	0.15 - 0.5 MHz, 97 dBµV (quasi peak) 84 dBµV (average)
RJ45 test 2 (where applicable)	0.5 – 30 MHz, 87 dBµV (quasi peak) 74 dBµV (average)

16.13 RADIATED EMISSIONS

Compliance	IEC 60255-26:2013
Test 1	30 – 230 MHz, 40 dBµV/m at 10 m measurement distance
Test 2	230 – 1 GHz, 47 dBµV/m at 10 m measurement distance
Test 3	1 – 2 GHz, 76 dBµV/m at 10 m measurement distance

16.14 POWER FREQUENCY

Compliance	IEC 60255-26:2013, IEC 61000-4-16:2015
Opto-inputs (Compliance is achieved using the opto-input filter)	300 V common-mode (Class A) 150 V differential mode (Class A)

Note:
Compliance is achieved using the opto-input filter.

APPENDIX A

ORDERING OPTIONS

Variants	Order Number											
	1 - 4	5	6	7	8	9	10	11	12-13	14	15
Model Type												
Feeder Management Protection IED - Directional	P14D											
Application												
Adapted to 20TE case		A										
Base		B										
Small Generator		G										
Load / Line Management		L										
HIF (SEF CT only)		Z										
PWH (Wattmetric Directional Earthfault) (Standard Earth CT only)		H										
Current/Voltage Transformers												
Standard Earth CT			1									
SEF CT			2									
Hardware Options	**Case**											
EIA RS485/IRIG-B (demodulated)	20TE/30TE			1								
EIA RS485/IRIG-B (demodulated) and Ethernet - Single channel Fibre/Copper (setting configurable as Failover*)	30TE			6								
EIA RS485/IRIG-B (demodulated) and EIA RS485	30TE			8								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Copper Ethernet - 2x RJ45 Copper (setting configurable as Failover)	30TE/40TE			A								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (setting configurable as Failover)	30TE/40TE			B								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Copper Ethernet - 2x RJ45 Copper (setting configurable as RSTP)	30TE/40TE			C								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (setting configurable as RSTP)	30TE/40TE			D								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Copper Ethernet - 2x RJ45 Copper (setting configurable as PRP or HSR)	30TE/40TE			E								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (setting configurable as PRP or HSR)	30TE/40TE			F								
40TE only - EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Copper Ethernet - 2x RJ45 Copper (setting configurable as Failover)	40TE			G								
40TE only - EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (setting configurable as Failover)	40TE			H								
40TE only - EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Copper Ethernet - 2x RJ45 Copper (setting configurable as RSTP)	40TE			J								
40TE only - EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (setting configurable as RSTP)	40TE			K								
40TE only - EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Copper Ethernet - 2x RJ45 Copper (setting configurable as PRP or HSR)	40TE			L								
40TE only - EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (setting configurable as PRP or HSR)	40TE			M								
EIA RS485/IRIG-B (demodulated) and Dual Copper Ethernet - 2x RJ45 Copper (dual IP)	30TE/40TE			N								
EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (dual IP)	30TE/40TE			P								
EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Copper Ethernet - 2x RJ45 Copper (dual IP)	40TE			Q								
EIA RS485, EIA RS485/IRIG-B (demodulated) and Dual Redundant Fibre Ethernet - 2x multimode fibre (dual IP)	40TE			R								
I/O Options	**Case**											
Standard (8 logic inputs + 8 relay outputs)	20TE/30TE				A							
Total (11 logic inputs + 12 relay outputs)	30TE/40TE				B							
Total (11 logic inputs + 12 relay outputs) suitable for trip circuit supervision	30TE/40TE				C							
Total (13 logic inputs + 12 relay outputs)	30TE/40TE				D							
Total (3 logic inputs + 4 relay outputs)	20TE				E							
Total (6 logic inputs + 8 relay outputs) suitable for trip circuit supervision	30TE				F							
Total (7 logic inputs + 8 relay outputs) suitable for trip circuit supervision	30TE				G							
Total (10 logic inputs + 12 relay outputs) suitable for trip circuit supervision *	40TE				H							
Total (12 logic inputs + 12 relay outputs) suitable for trip circuit supervision *	40TE				J							
* Please contact Product Manager												
Communication protocol												
Courier						1						
Modbus						2						
IEC60870-5-103 (VDEW)						3						
DNP3.0						4						
IEC61850 over Ethernet and Courier via rear RS485						6						
IEC61850 over Ethernet and IEC60870-5-103 via rear RS485						7						
DNP3.0 over Ethernet and Courier via rear RS485						8						
IEC61850 over Ethernet and Modbus via rear RS485						9						
IEC61850 over Ethernet and DNP3.0 via rear RS485						A						
IEC61850 over Ethernet + DNP3.0 over Ethernet and Courier via RS485						B						
IEC61850 over Ethernet + DNP3.0 over Ethernet and Modbus via RS485						C						
IEC61850 over Ethernet + DNP3.0 over Ethernet and IEC60870-5-103 via RS485						D						
Case												
20TE Flush (no function keys, 4 programmable LEDs)							B					
30TE Flush (3 function keys with LEDs, 8 programmable LEDs)							C					
Software only							0					
30TE Flush (Adapted field voltage for KCEG retrofit)							3					
30TE Flush (without field voltage jumpering for KCEG retrofit)							5					
30TE Flush (Additional shorting link)							6					
40TE Flush (3 function keys with LEDs, 8 programmable LEDs)							D					
Language												
Multilingual (English, French, German, Spanish)								0				
Multilingual (English, Russian, Italian, Portuguese)								6				
Chinese, English or French via HMI, with English or French only via Communications port								C				
Software Reference												
Unless specified the latest version will be delivered									**			
Customisation / Regionalisation												
Default										0		
Customer specific										A		
With frequency function (Model P14DB in 20TE Case only)										F		
Hardware design suffix												
Initial release											A	

APPENDIX B

SETTINGS AND SIGNALS

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
SYSTEM DATA	00	00		
This column contains general system settings and records				
Language	00	01	English	English Francais Deutsch Espanol *[Indexed String]*
This setting defines the default language used by the device for ordering option language = 0				
Language	00	01	English	English Italiano Português PYCCKÕÖ *[Indexed String]*
This setting defines the default language used by the device for ordering option language = 6				
Password	00	02		4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair Each character is in the Courier range 33 - 122 *[ASCII Password (4 chars)* *ASCII Password (8 chars)]*
This setting defines the plain text password.				
Sys Fn Links	00	03	0	Trip LED S/Reset (1 = enable self reset) *[Binary Flag (1) Indexed String]*
This setting allows the fixed function trip LED to be self resetting (set to 1 to extinguish the LED after a period of healthy restoration of load current). Only bit 0 is used.				
Description	00	04	MiCOM P14N MiCOM P14D MiCOM P94V	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
In this cell, you can enter and edit a 16 character IED description.				
Plant Reference	00	05	MiCOM	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell, you can enter and edit a 16 character plant description.				
Model Number	00	06	Model Number	Model Number *[ASCII Text (16 chars)]*
This cell displays the IED model number. This cannot be edited.				
Serial Number	00	08	Serial Number	Serial Number *[ASCII Text (7 chars)]*
This cell displays the IED serial number. This cannot be edited				
Frequency	00	09	50	50 or 60 *[Unsigned Integer (16 bits)]*
This cell sets the mains frequency to either 50 Hz or 60 Hz				
Comms Level	00	0A	2	Comms Level *[Unsigned Integer (16 bits)]*
This cell displays the Courier communications conformance level				
Relay Address	00	0B	255	From 0 to 255 in steps of 1 *[Unsigned Integer (16 bits)]*
This cell sets the first rear port IED address. Available settings are dependent on the protocol. This setting can also be made in the COMMUNICATIONS column.				
Relay Address	00	0B	1	From 1 to 247 in steps of 1 *[Unsigned Integer (16 bits)]*
This cell sets the first rear port IED address. Available settings are dependent on the protocol. This setting can also be made in the COMMUNICATIONS column.				
Relay Address	00	0B	1	From 0 to 254 in steps of 1 *[Unsigned Integer (16 bits)]*
This cell sets the first rear port IED address. Available settings are dependent on the protocol. This setting can also be made in the COMMUNICATIONS column.				
Relay Address	00	0B	1	From 0 to 65519 in steps of 1 *[Unsigned Integer (16 bits)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell sets the first rear port IED address. Available settings are dependent on the protocol. This setting can also be made in the COMMUNICATIONS column.				
Plant Status	00	0C		CB1 Open CB1 Closed *[Binary Flag (16 bits)]*
This cell displays the circuit breaker plant status. The first two bits are used. One to indicate the 52A state and one to indicate the 52B state.				
Control Status	00	0D		Control Status *[Binary Flag (16 bits)]*
This cell is not used				
Active Group	00	0E	1	Active Group *[Unsigned Integer (16 bits)]*
This cell displays the active settings group				
CB Trip/Close	00	10	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the Circuit Breaker Control menu.				
CB Trip/Close	00	10	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the Circuit Breaker Control menu.				
Software Ref. 1	00	11		Software Ref. 1 *[ASCII Text (16 chars)]*
This cell displays the IED software version including the protocol and IED model.				
Software Ref. 2	00	12		Software Ref. 2 *[ASCII Text (16 chars)]*
This cell displays the software version of the Ethernet card for models equipped with IEC 61850.				
Opto I/P Status	00	20		Opto 1 Input State (0=Off, 1=Energised) Opto 2 Input State (0=Off, 1=Energised) Opto 3 Input State (0=Off, 1=Energised) Opto 4 Input State (0=Off, 1=Energised) Opto 5 Input State (0=Off, 1=Energised) Opto 6 Input State (0=Off, 1=Energised) Opto 7 Input State (0=Off, 1=Energised) Opto 8 Input State (0=Off, 1=Energised) Opto 9 Input State (0=Off, 1=Energised) Opto 10 Input State (0=Off, 1=Energised) Opto 11 Input State (0=Off, 1=Energised) Opto 12 Input State (0=Off, 1=Energised) Opto 13 Input State (0=Off, 1=Energised) Opto 14 Input State (0=Off, 1=Energised) Opto 15 Input State (0=Off, 1=Energised) Opto 16 Input State (0=Off, 1=Energised) Opto 17 Input State (0=Off, 1=Energised) Opto 18 Input State (0=Off, 1=Energised) Opto 19 Input State (0=Off, 1=Energised) Opto 20 Input State (0=Off, 1=Energised) Opto 21 Input State (0=Off, 1=Energised) Opto 22 Input State (0=Off, 1=Energised) Opto 23 Input State (0=Off, 1=Energised) Opto 24 Input State (0=Off, 1=Energised) Opto 25 Input State (0=Off, 1=Energised) Opto 26 Input State (0=Off, 1=Energised) Opto 27 Input State (0=Off, 1=Energised) Opto 28 Input State (0=Off, 1=Energised) Opto 29 Input State (0=Off, 1=Energised) Opto 30 Input State (0=Off, 1=Energised) Opto 31 Input State (0=Off, 1=Energised) Opto 32 Input State (0=Off, 1=Energised) *[Binary Flag (32 bits) Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell displays the status of the available opto-inputs. This information is also available in the COMMISSIONING TESTS column				
Relay O/P Status	00	21		Relay 1 (0=Not Operated, 1=Operated) Relay 2 (0=Not Operated, 1=Operated) Relay 3 (0=Not Operated, 1=Operated) Relay 4 (0=Not Operated, 1=Operated) Relay 5 (0=Not Operated, 1=Operated) Relay 6 (0=Not Operated, 1=Operated) Relay 7 (0=Not Operated, 1=Operated) Relay 8 (0=Not Operated, 1=Operated) Relay 9 (0=Not Operated, 1=Operated) Relay 10 (0=Not Operated, 1=Operated) Relay 11 (0=Not Operated, 1=Operated) Relay 12 (0=Not Operated, 1=Operated) Relay 13 (0=Not Operated, 1=Operated) Relay 14 (0=Not Operated, 1=Operated) Relay 15 (0=Not Operated, 1=Operated) Relay 16 (0=Not Operated, 1=Operated) Relay 17 (0=Not Operated, 1=Operated) Relay 18 (0=Not Operated, 1=Operated) Relay 19 (0=Not Operated, 1=Operated) Relay 20 (0=Not Operated, 1=Operated) Relay 21 (0=Not Operated, 1=Operated) Relay 22 (0=Not Operated, 1=Operated) Relay 23 (0=Not Operated, 1=Operated) Relay 24 (0=Not Operated, 1=Operated) Relay 25 (0=Not Operated, 1=Operated) Relay 26 (0=Not Operated, 1=Operated) Relay 27 (0=Not Operated, 1=Operated) Relay 28 (0=Not Operated, 1=Operated) Relay 29 (0=Not Operated, 1=Operated) Relay 30 (0=Not Operated, 1=Operated) Relay 31 (0=Not Operated, 1=Operated) Relay 32 (0=Not Operated, 1=Operated) *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the available output relays.				
Alarm Status 1	00	22		Thermal Lockout HIF Alarm SG-opto Invalid Prot'n Disabled F out of Range VT Fail Alarm CT Fail Alarm CB Fail Alarm I^ Maint Alarm I^ Lockout Alarm CB Ops Maint CB Ops Lockout CB Op Time Maint CB Op Time Lock Fault Freq Lock CB Status Alarm Man CB Trip Fail Man CB Cls Fail Man CB Unhealthy Man No Checksync A/R Lockout A/R CB Unhealthy A/R No Checksync System Split UV Block User Alarm 1 User Alarm 2 User Alarm 3

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				User Alarm 4 User Alarm 5 User Alarm 6 User Alarm 7 *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the first 32 alarms as a binary string, including fixed and user settable alarms. This information is repeated for system purposes. This cell uses data type G96-1.				
Opto I/P Status	00	30		Opto 1 Input State (0=Off, 1=Energised) Opto 2 Input State (0=Off, 1=Energised) Opto 3 Input State (0=Off, 1=Energised) Opto 4 Input State (0=Off, 1=Energised) Opto 5 Input State (0=Off, 1=Energised) Opto 6 Input State (0=Off, 1=Energised) Opto 7 Input State (0=Off, 1=Energised) Opto 8 Input State (0=Off, 1=Energised) Opto 9 Input State (0=Off, 1=Energised) Opto 10 Input State (0=Off, 1=Energised) Opto 11 Input State (0=Off, 1=Energised) Opto 12 Input State (0=Off, 1=Energised) Opto 13 Input State (0=Off, 1=Energised) Opto 14 Input State (0=Off, 1=Energised) Opto 15 Input State (0=Off, 1=Energised) Opto 16 Input State (0=Off, 1=Energised) Opto 17 Input State (0=Off, 1=Energised) Opto 18 Input State (0=Off, 1=Energised) Opto 19 Input State (0=Off, 1=Energised) Opto 20 Input State (0=Off, 1=Energised) Opto 21 Input State (0=Off, 1=Energised) Opto 22 Input State (0=Off, 1=Energised) Opto 23 Input State (0=Off, 1=Energised) Opto 24 Input State (0=Off, 1=Energised) Opto 25 Input State (0=Off, 1=Energised) Opto 26 Input State (0=Off, 1=Energised) Opto 27 Input State (0=Off, 1=Energised) Opto 28 Input State (0=Off, 1=Energised) Opto 29 Input State (0=Off, 1=Energised) Opto 30 Input State (0=Off, 1=Energised) Opto 31 Input State (0=Off, 1=Energised) Opto 32 Input State (0=Off, 1=Energised) *[Binary Flag (32 bits) Indexed String]*
This cell display the status of the available opto-inputs. This information is repeated for system purposes.				
Relay O/P Status	00	40		High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the available output relays. This information is repeated for system purposes.				
Alarm Status 1	00	50		Thermal Lockout HIF Alarm SG-opto Invalid Prot'n Disabled F out of Range VT Fail Alarm CT Fail Alarm CB Fail Alarm I^ Maint Alarm I^ Lockout Alarm CB Ops Maint CB Ops Lockout CB Op Time Maint CB Op Time Lock Fault Freq Lock CB Status Alarm

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Man CB Trip Fail Man CB Cls Fail Man CB Unhealthy Man No Checksync A/R Lockout A/R CB Unhealthy A/R No Checksync System Split UV Block User Alarm 1 User Alarm 2 User Alarm 3 User Alarm 4 User Alarm 5 User Alarm 6 User Alarm 7 *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the first 32 alarms as a binary string, including fixed and user settable alarms. This information is repeated for system purposes. This cell uses data type G96-1.				
Alarm Status 3	00	52		DC Supply Fail GOOSE IED Absent NIC Not Fitted NIC No Response NIC Fatal Error Bad TCP/IP Cfg. NIC Link Fail NIC SW Mis-Match IP Addr Conflict Port A Link Fail Port B Link Fail DREB Set.Invalid Bad DNP Settings *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the third set of alarms as a binary string, including fixed and user settable alarms. This cell uses data type G228.				
User Alarms	00	54		User Alarm 1 (0=Self-reset, 1=Manual reset) User Alarm 2 (0=Self-reset, 1=Manual reset) User Alarm 3 (0=Self-reset, 1=Manual reset) User Alarm 4 (0=Self-reset, 1=Manual reset) User Alarm 5 (0=Self-reset, 1=Manual reset) User Alarm 6 (0=Self-reset, 1=Manual reset) User Alarm 7 (0=Self-reset, 1=Manual reset) User Alarm 8 (0=Self-reset, 1=Manual reset) User Alarm 9 (0=Self-reset, 1=Manual reset) User Alarm 10 (0=Self-reset, 1=Manual reset) User Alarm 11 (0=Self-reset, 1=Manual reset) User Alarm 12 (0=Self-reset, 1=Manual reset) User Alarm 13 (0=Self-reset, 1=Manual reset) User Alarm 14 (0=Self-reset, 1=Manual reset) User Alarm 15 (0=Self-reset, 1=Manual reset) User Alarm 16 (0=Self-reset, 1=Manual reset) User Alarm 17 (0=Self-reset, 1=Manual reset) User Alarm 18 (0=Self-reset, 1=Manual reset) User Alarm 19 (0=Self-reset, 1=Manual reset) User Alarm 20 (0=Self-reset, 1=Manual reset) User Alarm 21 (0=Self-reset, 1=Manual reset) User Alarm 22 (0=Self-reset, 1=Manual reset) User Alarm 23 (0=Self-reset, 1=Manual reset) User Alarm 24 (0=Self-reset, 1=Manual reset) User Alarm 25 (0=Self-reset, 1=Manual reset) User Alarm 26 (0=Self-reset, 1=Manual reset) User Alarm 27 (0=Self-reset, 1=Manual reset) User Alarm 28 (0=Self-reset, 1=Manual reset)

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				User Alarm 29 (0=Self-reset, 1=Manual reset) User Alarm 30 (0=Self-reset, 1=Manual reset) User Alarm 31 (0=Self-reset, 1=Manual reset) User Alarm 32 (0=Self-reset, 1=Manual reset) *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the third set of alarms as a binary string, including fixed and user settable alarms. This cell uses data type G268.				
Build Date&Time	00	60	Build Date & Time	Build Date&Time *[ASCII Text (16 chars)]*
This cell displays the build date & time. This cannot be edited.				
Access Level	00	D0		Level 0 - Logged Out. Level 1 - Password required for level 2. Level 2 - Password required for level 3. Level 3 - No Password required. *[Unsigned Integer (16 bits)]*
This cell displays the current access level.				
Password Level 1	00	D2	blank	4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair Each character is in the Courier range 33 - 122 *[ASCII Password (8 chars)]*
This setting allows you to change password level 1.				
Password Level 1	00	D2	blank	4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair Each character is in the Courier range 33 - 122 *[ASCII Password (8 chars)]*
This setting allows you to change password level 1 for Modbus only.				
Password Level 2	00	D3	AAAA	4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair Each character is in the Courier range 33 - 122 *[ASCII Password (8 chars)]*
This setting allows you to change password level 2.				
Password Level 2	00	D3	AAAA	4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair Each character is in the Courier range 33 - 122 *[ASCII Password (8 chars)]*
This setting allows you to change password level 2 for Modbus only.				
Password Level 3	00	D4	AAAA	4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair Each character is in the Courier range 33 - 122 *[ASCII Password (8 chars)]*
This setting allows you to change password level 3.				
Password Level 3	00	D4	AAAA	4 registers for writing 8 character password Each register contains a pair of characters Each register is formatted as follows:- first character of a pair second character of a pair

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Each character is in the Courier range 33 - 122 *[ASCII Password (8 chars)]*
This setting allows you to change password level 3 for Modbus only.				
Security Feature	00	DF		Security Feature *[Unsigned Integer (16-bits)]*
This setting displays the level of cyber security implemented, 1 = phase 1.				
Password	00	E1		4 registers for writing encrypted password Registers can contain any bit pattern. *[Encrypted Password (8 chars)]*
This cell allows you to enter the encrypted password. It is not visible via the user interfaced.				
Password Level 1	00	E2	blank	4 registers for writing encrypted password Registers can contain any bit pattern. *[Encrypted Password (8 chars)]*
This setting allows you to change the encrypted password level 1. This is not visible via the user interface.				
Password Level 2	00	E3	AAAA	4 registers for writing encrypted password Registers can contain any bit pattern. *[Encrypted Password (8 chars)]*
This setting allows you to change the encrypted password level 2. This is not visible via the user interface.				
Password Level 3	00	E4	AAAA	4 registers for writing encrypted password Registers can contain any bit pattern. *[Encrypted Password (8 chars)]*
This setting allows you to change the encrypted password level 3. This is not visible via the user interface.				
VIEW RECORDS	01	00		
This column contains information about records. Most of these cells are not editable.				
Select Event [0...n]	01	01	0	From 0 to 2048 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting selects the required event record. A value of 0 corresponds to the latest event, 1 the second latest and so on.				
Menu Cell Ref	01	02	(From Record)	Menu Cell Ref *[Cell Reference]*
This cell indicates the type of event				
Time & Date	01	03	(From Record)	Time & Date *[IEC870 Date & Time]*
This cell shows the Time & Date of the event, given by the internal Real Time Clock.				
Event Text	01	04		Event Text *[ASCII Text (32 chars)]*
This cell shows the description of the event - up to 32 Characters over 2 lines.				
Event Value	01	05		Event Value *[Unsigned Integer (32 bits)]*
This cell displays a 32 bit binary flag representing the event.				
Select Fault [0...n]	01	06	0	From 0 to 9 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting selects the required fault record from those stored. A value of 0 corresponds to the latest fault and so on.				
Faulted Phase	01	07		Start A Start B Start C Start N Trip A Trip B Trip C Trip N *[Binary Flag (8 bits)]*
This cell displays the faulted phase.				
Start Elements 1	01	08		General Start Start I>1 Start I>2 Start I>3 Start I>4 Start BrokenLine Start IN1>1 Start IN1>2

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Start IN1>3 Start IN1>4 Start IN2>1 Start IN2>2 Start IN2>3 Start IN2>4 Start ISEF>1 Start ISEF>2 Start ISEF>3 Start ISEF>4 Start NVD VN>1 Start NVD VN>2 Thermal Alarm Start V2>1 Start V<1 Start V<2 Start V< A/AB Start V< B/BC Start V< C/CA Start V>1 Start V>2 Start V> A/AB Start V> B/BC Start V> C/CA *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the first set of 32 start signals.				
Start Elements 2	01	09		Start NVD VN>3 Start V<3 Start V>3 Start NVD VN>4 Start NVD VN<1 Start NVD VN<2 Start YN> Start GN> Start BN> Start df/dt>1 Start df/dt>2 Start df/dt>3 Start df/dt>4 Start I2>1 Start I2>2 Start I2>3 Start I2>4 Start I>5 Start I>6 Power>1 Start Power>2 Start Power> A Start Power> B Start Power> C Start Power<1 Start Power<2 Start Power< A Start Power< B Start Power< C Start SensP1 Start A SensP2 Start A Start V2>2 *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the second set of 32 start signals.				
Start Elements 3	01	0A		Start F 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Start F 2 Start F 3 Start F 4 Start F 5 Start F 6 Start F 7 Start F 8 Start F 9 Start df/dt+t 1 Start df/dt+t 2 Start df/dt+t 3 Start df/dt+t 4 Start df/dt+t 5 Start df/dt+t 6 Start df/dt+t 7 Start df/dt+t 8 Start df/dt+t 9 Sta DelF/DelT 1 Sta DelF/DelT 2 Sta DelF/DelT 3 Sta DelF/DelT 4 Sta DelF/DelT 5 Sta DelF/DelT 6 Sta DelF/DelT 7 Sta DelF/DelT 8 Sta DelF/DelT 9 dv/dt1 Start dv/dt2 Start dv/dt StartA/AB dv/dt StartB/BC dv/dt StartC/CA *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the third set of 32 start signals.				
Start Elements 4	01	0B		dv/dt3 Start dv/dt4 Start Vdc1 Start Vdc2 Start Vdc3 Start WDE>1 Fwd Start WDE>1 Rev Start WDE>2 Fwd Start WDE>2 Rev Start Start Vavg<1 Start Vavg<2 Start Vavg< PhA Start Vavg< PhB Start Vavg< PhC Start Vavg>1 Start Vavg>2 Start Vavg> PhA Start Vavg> PhB Start Vavg> PhC Start V0avg>1 Start V0avg>2 Start V1avg>1 Start V1avg>2 Start V2avg>1 Start V2avg>2 Start V1<1 Start V1<2 Start V1>1 Start V1>2

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Start Rev. Power *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the fourth set of 32 start signals.				
Trip Elements 1	01	0C		Any Trip Trip I>1 Trip I>2 Trip I>3 Trip I>4 Trip Broken Line Trip IN1>1 Trip IN1>2 Trip IN1>3 Trip IN1>4 Trip IN2>1 Trip IN2>2 Trip IN2>3 Trip IN2>4 Trip ISEF>1 Trip ISEF>2 Trip ISEF>3 Trip ISEF>4 Trip IREF> Trip NVD VN>1 Trip NVD VN>2 Trip Thermal Trip V2>1 Trip I>5 Trip I>6 Trip V2>2 *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the first set of 32 trip signals.				
Trip Elements 2	01	0D		Trip V<1 Trip V<2 Trip V< A/AB Trip V< B/BC Trip V< C/CA Trip V>1 Trip V>2 Trip V> A/AB Trip V> B/BC Trip V> C/CA Trip V<3 Trip V>3 Trip NVD VN>3 Trip NVD VN>4 Trip NVD VN<1 Trip NVD VN<2 Trip YN> Trip GN> Trip BN> Trip df/dt>1 Trip df/dt>2 Trip df/dt>3 Trip df/dt>4 Trip I2>1 Trip I2>2 Trip I2>3 Trip I2>4 *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the second set of 32 trip signals.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Trip Elements 3	01	0E		Trip F 1 Trip F 2 Trip F 3 Trip F 4 Trip F 5 Trip F 6 Trip F 7 Trip F 8 Trip F 9 Trip df/dt+t 1 Trip df/dt+t 2 Trip df/dt+t 3 Trip df/dt+t 4 Trip df/dt+t 5 Trip df/dt+t 6 Trip df/dt+t 7 Trip df/dt+t 8 Trip df/dt+t 9 Trip DelF/DelT 1 Trip DelF/DelT 2 Trip DelF/DelT 3 Trip DelF/DelT 4 Trip DelF/DelT 5 Trip DelF/DelT 6 Trip DelF/DelT 7 Trip DelF/DelT 8 Trip DelF/DelT 9 Vdc1 Trip Vdc2 Trip Vdc3 Trip *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the third set of 32 trip signals.				
Trip Elements 4	01	0F		Trip f+df/dt 1 Trip f+df/dt 2 Trip f+df/dt 3 Trip f+df/dt 4 Trip f+df/dt 5 Trip f+df/dt 6 Trip f+df/dt 7 Trip f+df/dt 8 Trip f+df/dt 9 dv/dt1 Trip dv/dt2 Trip dv/dt Trip A/AB dv/dt Trip B/BC dv/dt Trip C/CA Power>1 Trip Power>2 Trip Power> A Trip Power> B Trip Power> C Trip Power<1 Trip Power<2 Trip Power< A Trip Power< B Trip Power< C Trip SensP1 Trip A SensP2 Trip A dv/dt3 Trip dv/dt4 Trip FA HIF CHA HIF

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				WDE>1 Fwd Fault WDE>2 Fwd Fault *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the fourth set of 32 trip signals.				
Fault Alarms	01	10		CB Fail 1 CB Fail 2 VTS CTS VDep OC CLP AR Trip 1 AR Trip 2 AR Trip 3 AR Trip 4 AR Trip 5 DC Supply Fail *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the fault alarm signals.				
Fault Time	01	11		Fault Time *[IEC870 Date & Time]*
This cell displays the time and date of the fault				
Active Group	01	12		Active Group *[Unsigned Integer (16 bits)]*
This cell displays the active settings group				
System Frequency	01	13		System Frequency *[Courier Number (frequency)]*
This cell displays the system frequency				
Fault Duration	01	14		Fault Duration *[Courier Number (time-seconds)]*
This cell displays the duration of the fault time				
CB Operate Time	01	15		CB Operate Time *[Courier Number (time-seconds)]*
This cell displays the CB operate time				
Relay Trip Time	01	16		Relay Trip Time *[Courier Number (time-seconds)]*
This cell displays the time from protection start to protection trip				
Fault Location	01	17		Fault Location *[Courier Number (metres)]*
This cell displays the fault location in metres.				
Fault Location	01	18		Fault Location *[Courier Number (miles)]*
This cell displays the fault location in miles.				
Fault Location	01	19		Fault Location *[Courier Number (impedance)]*
This cell displays the fault location in ohms.				
Fault Location	01	1A		Fault Location *[Courier Number (percentage)]*
This cell displays the fault location in percentage.				
IA	01	1B		IA *[Courier Number (current)]*
This cell displays the phase A current				
IB	01	1C		IB *[Courier Number (current)]*
This cell displays the phase B current				
IC	01	1D		IC *[Courier Number (current)]*
This cell displays the phase C current				
VAB	01	1E		VAB

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (voltage)]
This cell displays VA with respect to VB				
VBC	01	1F		VBC *[Courier Number (voltage)]*
This cell displays VB with respect to VC				
VCA	01	20		VCA *[Courier Number (voltage)]*
This cell displays VC with respect to VA				
IN Measured	01	21		IN Measured *[Courier Number (current)]*
This cell displays the value of measured neutral current				
IN Derived	01	22		IN Derived *[Courier Number (current)]*
This cell displays the value of derived neutral current				
IN Sensitive	01	23		IN Sensitive *[Courier Number (current)]*
This cell displays the value of sensitive neutral current				
IREF Diff	01	24		IREF Diff *[Courier Number (current)]*
This cell displays the value of Restricted Earth Fault differential current				
IREF Bias	01	25		IREF Bias *[Courier Number (current)]*
This cell displays the value of Restricted Earth Fault bias current				
VAN	01	26		VAN *[Courier Number (voltage)]*
This cell displays VA with respect to Neutral				
VBN	01	27		VBN *[Courier Number (voltage)]*
This cell displays VB with respect to Neutral				
VCN	01	28		VCN *[Courier Number (voltage)]*
This cell displays VC with respect to Neutral				
VN Derived	01	29		VN Derived *[Courier Number (voltage)]*
This cell displays the derived Earth fault voltage				
VN Measured	01	29		VN Measured *[Courier Number (voltage)]*
This cell displays the measured Earth fault voltage				
SEF Admittance	01	2A		SEF Admittance *[Courier Number (inverse ohms)]*
This cell displays the Sensitive Earth Fault admittance				
SEF Conductance	01	2B		SEF Conductance *[Courier Number (inverse ohms)]*
This cell displays the Sensitive Earth Fault conductance				
SEF Susceptance	01	2C		SEF Susceptance *[Courier Number (inverse ohms)]*
This cell displays the Sensitive Earth Fault susceptance				
EF Admittance	01	2D		EF Admittance *[Courier Number (inverse ohms)]*
This cell displays the Sensitive Earth Fault admittance				
EF Conductance	01	2E		EF Conductance *[Courier Number (inverse ohms)]*
This cell displays the Earth Fault conductance				
EF Susceptance	01	2F		EF Susceptance *[Courier Number (inverse ohms)]*
This cell displays the Sensitive Earth Fault susceptance				
DC Supply Mag	01	30		DC Supply Mag *[Courier Number (voltage)]*
This cell displays the Auxiliary Supply Voltage level				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
V Shift Angle	01	31		V Shift Angle *[Courier Number (angle)]*
This cell displays the Voltage Vector Shift Angle				
Trip Elements 5	01	32		Trip Vavg<1 Trip Vavg<2 Trip Vavg< phA Trip Vavg< phB Trip Vavg< phC Trip Vavg>1 Trip Vavg>2 Trip Vavg> phA Trip Vavg> phB Trip Vavg> phC Trip V0avg>1 Trip V0avg>2 Trip V1avg>1 Trip V1avg>2 Trip V2avg>1 Trip V2avg>2 Trip V1<1 Trip V1<2 Trip V1>1 Trip V1>2 Trip Rev. Power Trip Tstart> Trip Tstall> Run Trip Tstall> St. Trip Vdip Trip V Shift *[Binary Flag (32 bits)* *Indexed String]*
This cell displays the status of the fifth set of 32 trip signals.				
Select Maint [0...n]	01	F0	Manual override to select a fault record.	From 0 to 9 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting selects the required maintenance report from those stored. A value of 0 corresponds to the latest report.				
Maint Text	01	F1		Maint Text *[ASCII Text (32 chars)]*
This cell displays the description of the maintenance record				
Maint Type	01	F2		Maint Type *[Unsigned Integer (32 bits)]*
This is the type of maintenance record				
Maint Data	01	F3		Maint Data *[Unsigned Integer (32 bits)]*
This is the maintenance record data (error code)				
Evt Iface Source	01	FA		Evt Iface Source *[Unsigned Integer (16 bits)]*
This cell displays the interface on which the event was logged				
Evt Access Level	01	FB		Evt Access Level *[Unsigned Integer (16 bits)]*
Any security event that indicates that it came from an interface action, such as disabling a port, will also record the access level of the interface that initiated the event. This access level is displayed in this cell.				
Evt Extra Info	01	FC		Evt Extra Info *[Unsigned Integer (16 bits)]*
This cell provides supporting information for the event and can vary between the different event types.				
Evt Unique Id	01	FE		Evt Unique Id *[Unsigned Integer (32 bits)]*
This cell displays the unique event ID associated with the event.				
Reset Indication	01	FF	No	No Yes *[Indexed String]*
This command resets the trip LED indications provided that the relevant protection element has reset.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
MEASUREMENTS 1	02	00		
This column contains measurement parameters				
IA Magnitude	02	01		IA Magnitude *[Courier Number (current)]*
This cell displays the A-phase current magnitude.				
IA Phase Angle	02	02		IA Phase Angle *[Courier Number (angle)]*
This cell displays the A-phase phase angle.				
IB Magnitude	02	03		IB Magnitude *[Courier Number (current)]*
This cell displays the B-phase current magnitude.				
IB Phase Angle	02	04		IB Phase Angle *[Courier Number (angle)]*
This cell displays the B-phase phase angle.				
IC Magnitude	02	05		IC Magnitude *[Courier Number (current)]*
This cell displays the C-phase current magnitude.				
IC Phase Angle	02	06		IC Phase Angle *[Courier Number (angle)]*
This cell displays the C-phase phase angle.				
IN Measured Mag	02	07		IN Measured Mag *[Courier Number (current)]*
This cell displays the measured neutral current magnitude.				
IN Measured Ang	02	08		IN Measured Ang *[Courier Number (angle)]*
This cell displays the measured neutral phase angle.				
IN Derived Mag	02	09		IN Derived Mag *[Courier Number (current)]*
This cell displays the derived neutral current magnitude.				
IN Derived Angle	02	0A		IN Derived Angle *[Courier Number (angle)]*
This cell displays the derived neutral phase angle.				
ISEF Magnitude	02	0B		ISEF Magnitude *[Courier Number (current)]*
This cell displays the sensitive earth fault current magnitude.				
ISEF Angle	02	0C		ISEF Angle *[Courier Number (angle)]*
This cell displays the sensitive earth fault phase angle.				
I1 Magnitude	02	0D		I1 Magnitude *[Courier Number (current)]*
This cell displays the positive sequence current magnitude.				
I2 Magnitude	02	0E		I2 Magnitude *[Courier Number (current)]*
This cell displays the negative sequence current magnitude.				
I0 Magnitude	02	0F		I0 Magnitude *[Courier Number (current)]*
This cell displays the zero sequence current magnitude.				
IA RMS	02	10		IA RMS *[Courier Number (current)]*
This cell displays the A-phase RMS current.				
IB RMS	02	11		IB RMS *[Courier Number (current)]*
This cell displays the B-phase RMS current.				
IC RMS	02	12		IC RMS *[Courier Number (current)]*
This cell displays the C-phase RMS current.				
IN RMS	02	13		IN RMS *[Courier Number (current)]*
This cell displays the C-phase RMS current.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
VAB Magnitude	02	14		VAB Magnitude *[Courier Number (voltage)]*
This cell displays the A-phase voltage magnitude with respect to B-phase (VAB)				
VAB Phase Angle	02	15		VAB Phase Angle *[Courier Number (angle)]*
This cell displays the VAB phase angle				
VBC Magnitude	02	16		VBC Magnitude *[Courier Number (voltage)]*
This cell displays the B-phase voltage magnitude with respect to C-phase (VBC)				
VBC Phase Angle	02	17		VBC Phase Angle *[Courier Number (angle)]*
This cell displays the VBC phase angle				
VCA Magnitude	02	18		VCA Magnitude *[Courier Number (voltage)]*
This cell displays the C-phase voltage magnitude with respect to A-phase (VCA)				
VCA Phase Angle	02	19		VCA Phase Angle *[Courier Number (angle)]*
This cell displays the VCA phase angle				
VAN Magnitude	02	1A		VAN Magnitude *[Courier Number (voltage)]*
This cell displays the A-phase voltage magnitude with respect to Neutral (VAN)				
VAN Phase Angle	02	1B		VAN Phase Angle *[Courier Number (angle)]*
This cell displays the VAN phase angle				
VBN Magnitude	02	1C		VBN Magnitude *[Courier Number (voltage)]*
This cell displays the B-phase voltage magnitude with respect to Neutral (VBN)				
VBN Phase Angle	02	1D		VBN Phase Angle *[Courier Number (angle)]*
This cell displays the VBN phase angle				
VCN Magnitude	02	1E		VCN Magnitude *[Courier Number (voltage)]*
This cell displays the C-phase voltage magnitude with respect to Neutral (VCN)				
VCN Phase Angle	02	1F		VCN Phase Angle *[Courier Number (angle)]*
This cell displays the VCN phase angle				
VN Mag	02	22		VN Mag *[Courier Number (voltage)]*
This cell displays the neutral voltage magnitude (can be measured or derived according to cell [0A 16])				
VN Ang	02	23		VN Ang *[Courier Number (angle)]*
This cell displays the neutral phase angle (can be measured or derived according to cell [0A 16])				
V1 Magnitude	02	24		V1 Magnitude *[Courier Number (voltage)]*
This cell displays the positive sequence voltage magnitude				
V2 Magnitude	02	25		V2 Magnitude *[Courier Number (voltage)]*
This cell displays the negative sequence voltage magnitude				
V0 Magnitude	02	26		V0 Magnitude *[Courier Number (voltage)]*
This cell displays the zero sequence voltage magnitude				
V0 Magnitude	02	26		V0 Magnitude *[Courier Number (voltage)]*
This cell displays the zero sequence voltage magnitude				
VAN RMS	02	27		VAN RMS *[Courier Number (voltage)]*
This cell displays the A-phase RMS voltage with respect to Neutral (VAN)				
VBN RMS	02	28		VBN RMS *[Courier Number (voltage)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell displays the B-phase RMS voltage with respect to Neutral (VAN)				
VCN RMS	02	29		VCN RMS *[Courier Number (voltage)]*
This cell displays the C-phase RMS voltage with respect to Neutral (VAN)				
Frequency	02	2D		Frequency *[Courier Number (frequency)]*
This cell displays the system frequency				
C/S Voltage Mag	02	2E		C/S Voltage Mag *[Courier Number (voltage)]*
This cell displays the Check Synchronisation voltage magnitude				
C/S Voltage Ang	02	2F		C/S Voltage Ang *[Courier Number (angle)]*
This cell displays the Check Synchronisation voltage phase angle				
C/S Bus-Line Ang	02	30		C/S Bus-Line Ang *[Courier Number (angle)]*
This cell displays the Check Synchronisation bus-to-line phase angle				
Slip Frequency	02	31		Slip Frequency *[Courier Number (frequency)]*
This cell displays the slip frequency				
C/S Bus-Line Mag	02	3A		C/S Bus-Line Mag *[Courier Number (voltage)]*
This cell displays the Check Synchronisation bus-to-line magnitude				
I1 Magnitude	02	40		I1 Magnitude *[Courier Number (current)]*
This cell displays the positive sequence current magnitude.				
I1 Phase Angle	02	41		I1 Phase Angle *[Courier Number (angle)]*
This cell displays the positive sequence phase angle.				
I2 Magnitude	02	42		I2 Magnitude *[Courier Number (current)]*
This cell displays the negative sequence current magnitude.				
I2 Phase Angle	02	43		I2 Phase Angle *[Courier Number (angle)]*
This cell displays the negative sequence phase angle.				
I0 Magnitude	02	44		I0 Magnitude *[Courier Number (current)]*
This cell displays the zero sequence current magnitude.				
I0 Phase Angle	02	45		I0 Phase Angle *[Courier Number (angle)]*
This cell displays the zero sequence phase angle.				
V1 Magnitude	02	46		V1 Magnitude *[Courier Number (voltage)]*
This cell displays the positive sequence voltage magnitude				
V1 Phase Angle	02	47		V1 Phase Angle *[Courier Number (angle)]*
This cell displays the positive sequence voltage phase angle				
V2 Magnitude	02	48		V2 Magnitude *[Courier Number (voltage)]*
This cell displays the negative sequence voltage magnitude				
V2 Phase Angle	02	49		V2 Phase Angle *[Courier Number (angle)]*
This cell displays the negative sequence voltage phase angle				
V0 Magnitude	02	4A		V0 Magnitude *[Courier Number (voltage)]*
This cell displays the zero sequence voltage magnitude				
V0 Magnitude	02	4A		V0 Magnitude *[Courier Number (voltage)]*
This cell displays the zero sequence voltage magnitude				
V0 Phase Angle	02	4B		V0 Phase Angle

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (angle)]
This cell displays the zero sequence voltage phase angle				
MEASUREMENTS 2	03	00		
This column contains measurement parameters				
A Phase Watts	03	01		A Phase Watts *[Courier Number (power Watts)]*
This cell displays the A-phase Watts measurement.				
B Phase Watts	03	02		B Phase Watts *[Courier Number (power Watts)]*
This cell displays the B-phase Watts measurement.				
C Phase Watts	03	03		C Phase Watts *[Courier Number (power Watts)]*
This cell displays the C-phase Watts measurement.				
A Phase VArs	03	04		A Phase VArs *[Courier Number (VAr)]*
This cell displays the A-phase VArs measurement.				
B Phase VArs	03	05		B Phase VArs *[Courier Number (VAr)]*
This cell displays the B-phase VArs measurement.				
C Phase VArs	03	06		C Phase VArs *[Courier Number (VAr)]*
This cell displays the C-phase VArs measurement.				
A Phase VA	03	07		A Phase VA *[Courier Number (VA)]*
This cell displays the A-phase VA measurement.				
B Phase VA	03	08		B Phase VA *[Courier Number (VA)]*
This cell displays the B-phase VA measurement.				
C Phase VA	03	09		C Phase VA *[Courier Number (VA)]*
This cell displays the C-phase VA measurement.				
3 Phase Watts	03	0A		3 Phase Watts *[Courier Number (power Watts)]*
This cell displays the 3-phase Watts measurement.				
3 Phase VArs	03	0B		3 Phase VArs *[Courier Number (VAr)]*
This cell displays the 3-phase VArs measurement.				
3 Phase VA	03	0C		3 Phase VA *[Courier Number (VA)]*
This cell displays the 3-phase VA measurement.				
3Ph Power Factor	03	0E		3Ph Power Factor *[Courier Number (decimal)]*
This cell displays the 3-phase Power Factor measurement.				
APh Power Factor	03	0F		APh Power Factor *[Courier Number (decimal)]*
This cell displays the A-phase Power Factor measurement.				
BPh Power Factor	03	10		BPh Power Factor *[Courier Number (decimal)]*
This cell displays the B-phase Power Factor measurement.				
CPh Power Factor	03	11		CPh Power Factor *[Courier Number (decimal)]*
This cell displays the C-phase Power Factor measurement.				
3Ph WHours Fwd	03	12		3Ph WHours Fwd *[Courier Number (Wh)]*
This cell displays the 3-phase Watt Hours forward measurement.				
3Ph WHours Rev	03	13		3Ph WHours Rev *[Courier Number (Wh)]*
This cell displays the 3-phase Watt Hours reverse measurement.				
3Ph VArHours Fwd	03	14		3Ph VArHours Fwd

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (VArh)]
This cell displays the 3-phase VAr Hours forward measurement.				
3Ph VArHours Rev	03	15		3Ph VArHours Rev *[Courier Number (VArh)]*
This cell displays the 3-phase VAr Hours reverse measurement.				
3Ph W Fix Demand	03	16		3Ph W Fix Demand *[Courier Number (power)]*
This cell displays the 3-phase W fixed demand measurement.				
3Ph VArs Fix Dem	03	17		3Ph VArs Fix Dem *[Courier Number (VAr)]*
This cell displays the 3-phase VArs fixed demand measurement.				
IA Fixed Demand	03	18		IA Fixed Demand *[Courier Number (current)]*
This cell displays the A-phase current fixed demand measurement				
IB Fixed Demand	03	19		IB Fixed Demand *[Courier Number (current)]*
This cell displays the B-phase current fixed demand measurement				
IC Fixed Demand	03	1A		IC Fixed Demand *[Courier Number (current)]*
This cell displays the C-phase current fixed demand measurement				
3 Ph W Roll Dem	03	1B		3 Ph W Roll Dem *[Courier Number (power)]*
This cell displays the 3-phase Watts rolling demand measurement.				
3Ph VArs RollDem	03	1C		3Ph VArs RollDem *[Courier Number (VAr)]*
This cell displays the 3-phase VArs rolling demand measurement.				
IA Roll Demand	03	1D		IA Roll Demand *[Courier Number (current)]*
This cell displays the A-phase current rolling demand measurement				
IB Roll Demand	03	1E		IB Roll Demand *[Courier Number (current)]*
This cell displays the B-phase current rolling demand measurement				
IC Roll Demand	03	1F		IC Roll Demand *[Courier Number (current)]*
This cell displays the C-phase current rolling demand measurement				
3Ph W Peak Dem	03	20		3Ph W Peak Dem *[Courier Number (power)]*
This cell displays the 3-phase Watts peak demand measurement.				
3Ph VAr Peak Dem	03	21		3Ph VAr Peak Dem *[Courier Number (VAr)]*
This cell displays the 3-phase VArs peak demand measurement.				
IA Peak Demand	03	22		IA Peak Demand *[Courier Number (current)]*
This cell displays the A-phase current peak demand measurement				
IB Peak Demand	03	23		IB Peak Demand *[Courier Number (current)]*
This cell displays the B-phase current peak demand measurement				
IC Peak Demand	03	24		IC Peak Demand *[Courier Number (current)]*
This cell displays the C-phase current peak demand measurement				
Reset Demand	03	25	No	No Yes *[Indexed String]*
This command resets all acquired demand values.				
VA Mov Average	03	28		VA Mov Average *[Courier Number (voltage)]*
A-phase RMS average voltage with respect to Neutral (VAN)				
VB Mov Average	03	29		VB Mov Average *[Courier Number (voltage)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
B-phase RMS average voltage with respect to Neutral (VBN)				
VC Mov Average	03	2A		VC Mov Average *[Courier Number (voltage)]*
C-phase RMS average voltage with respect to Neutral (VCN)				
V0 Mov Average	03	2B		V0 Mov Average *[Courier Number (voltage)]*
Zero sequence voltage magnitude average				
V1 Mov Average	03	2C		V1 Mov Average *[Courier Number (voltage)]*
Positive sequence voltage magnitude average				
V2 Mov Average	03	2D		V2 Mov Average *[Courier Number (voltage)]*
Negative sequence voltage magnitude average				
3Ph WHours	03	30		3Ph WHours *[Courier Number (Wh)]*
This cell displays the 3-phase Watt Hours measurement.				
3Ph VArHours	03	31		3Ph VArHours *[Courier Number (VArh)]*
This cell displays the 3-phase VAr Hours measurement.				
+3Ph W Fix Dem	03	40		+3Ph W Fix Dem *[Courier Number (power)]*
This cell displays the reverse 3-phase W fixed demand measurement.				
-3Ph W Fix Dem	03	41		-3Ph W Fix Dem *[Courier Number (power)]*
This cell displays the forward 3-phase W fixed demand measurement.				
+3Ph VAr Fix Dem	03	42		+3Ph VAr Fix Dem *[Courier Number (VAr)]*
This cell displays the reverse 3-phase VAr fixed demand measurement.				
-3Ph VAr Fix Dem	03	43		-3Ph VAr Fix Dem *[Courier Number (VAr)]*
This cell displays the forward 3-phase VAr fixed demand measurement.				
+3Ph W Peak Dem	03	44		+3Ph W Peak Dem *[Courier Number (power)]*
This cell displays the reverse 3-phase W peak demand measurement.				
-3Ph W Peak Dem	03	45		-3Ph W Peak Dem *[Courier Number (power)]*
This cell displays the forward 3-phase W peak demand measurement.				
+3Ph VAr Peak Dem	03	46		+3Ph VAr Peak Dem *[Courier Number (VAr)]*
This cell displays the reverse 3-phase VAr peak demand measurement.				
-3Ph VAr Peak Dem	03	47		-3Ph VAr Peak Dem *[Courier Number (VAr)]*
This cell displays the forward 3-phase VAr peak demand measurement.				
I Average	03	48		I Average *[Courier Number (current)]*
This cell displays the average of IA, IB, IC				
V Average	03	49		V Average *[Courier Number (voltage)]*
This cell displays the average of VA, VB, VC				
% I2 / I Average	03	4A		% I2 / I Average *[Courier Number (percentage)]*
This cell displays the percentage of I2 / I Average				
% V2 / V Average	03	4B		% V2 / V Average *[Courier Number (percentage)]*
This cell displays the percentage of V2 / V Average				
Cur Dem Period	03	F0		Cur Dem Period *[Courier Number (Time)]*
This cell displays the current demand period				
MEASUREMENTS 3	04	00		

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This column contains measurement parameters				
Highest Phase I	04	01		Highest Phase I *[Courier Number (current)]*
This cell displays the highest phase current				
Thermal State	04	02		Thermal State *[Courier Number (percentage)]*
This cell displays the thermal state				
Reset Thermal	04	03	No	No Yes *[Indexed String]*
This command resets the thermal state				
IREF Diff	04	04		IREF Diff *[Courier Number (current)]*
This cell displays the Restricted Earth Fault differential current				
IREF Bias	04	05		IREF Bias *[Courier Number (current)]*
This cell displays the Restricted Earth Fault bias current				
Admittance SEF	04	06		Admittance SEF *[Courier Number (inverse ohms)]*
This cell displays the SEF admittance				
Conductance SEF	04	07		Conductance SEF *[Courier Number (inverse ohms)]*
This cell displays the SEF conductance				
Susceptance SEF	04	08		Susceptance SEF *[Courier Number (inverse ohms)]*
This cell displays the SEF susceptance				
Admittance E/F	04	09		Admittance E/F *[Courier Number (inverse ohms)]*
This cell displays the earth fault admittance				
Conductance E/F	04	0A		Conductance E/F *[Courier Number (inverse ohms)]*
This cell displays the earth fault conductance				
Susceptance E/F	04	0B		Susceptance E/F *[Courier Number (inverse ohms)]*
This cell displays the earth fault susceptance				
I2/I1 Ratio	04	0C		I2/I1 Ratio *[Courier Number (decimal)]*
This cell displays the negative sequence current to positive sequence current ratio				
SEF Power	04	0D		SEF Power *[Courier Number (power)]*
This cell displays the Sensitive Earth Fault power				
SEF Power	04	0D		SEF Power *[Courier Number (power)]*
This cell displays the Sensitive Earth Fault power				
df/dt	04	0E		df/dt *[Courier Number (Hz/sec)]*
This cell displays the rate of change of frequency				
IA 2ndHarm	04	0F		IA 2ndHarm *[Courier Number (percentage)]*
This cell displays the A-phase 2nd harmonic current component				
IB 2ndHarm	04	10		IB 2ndHarm *[Courier Number (percentage)]*
This cell displays the B-phase 2nd harmonic current component				
IC 2ndHarm	04	11		IC 2ndHarm *[Courier Number (percentage)]*
This cell displays the C-phase 2nd harmonic current component				
APh Sen Watts	04	12		APh Sen Watts *[Courier Number (power Watts)]*
This cell displays the A-Phase Sensitive Watts				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
APh Sen Vars	04	13		APh Sen Vars *[Courier Number (Var)]*
This cell displays the A-Phase Sensitive VArs				
APh Power Angle	04	14		APh Power Angle *[Courier Number (angle)]*
This cell displays the A-Phase Power Angle				
Z1 Mag	04	15		Z1 Mag *[Courier Number (impedance)]*
This cell displays the Positive Sequence Impedance Magnitude				
Z1 Ang	04	16		Z1 Ang *[Courier Number (angle)]*
This cell displays the Positive Sequence Impedance Angle				
ZA Mag	04	17		ZA Mag *[Courier Number (impedance)]*
This cell displays the Phase A Impedance Magnitude				
ZA Ang	04	18		ZA Ang *[Courier Number (angle)]*
This cell displays the Phase A Impedance Angle				
ZB Mag	04	19		ZB Mag *[Courier Number (impedance)]*
This cell displays the Phase B Impedance Magnitude				
ZB Ang	04	1A		ZB Ang *[Courier Number (angle)]*
This cell displays the Phase B Impedance Angle				
ZC Mag	04	1B		ZC Mag *[Courier Number (impedance)]*
This cell displays the Phase C Impedance Magnitude				
ZC Ang	04	1C		ZC Ang *[Courier Number (angle)]*
This cell displays the Phase C Impedance Angle				
DC Supply Mag	04	20		DC Supply Mag *[Courier Number (voltage)]*
This cell displays the Auxiliary Supply Voltage level				
FREQUENCY STAT	05	00		
This column contains frequency protection statistical parameters				
Stg1 f+t Sta	05	01		Stg1 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 1				
Stg1 f+t Trp	05	02		Stg1 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 1				
Stg1 f+df/dt Trp	05	03		Stg1 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 1				
Stg1 df/dt+t Sta	05	04		Stg1 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 1				
Stg1 df/dt+t Trp	05	05		Stg1 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 1				
Stg1 f+Df/Dt Sta	05	06		Stg1 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 1				
Stg1 f+Df/Dt Trp	05	07		Stg1 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 1				
Stg1 Revn Date	05	08		Stg1 Revn Date *[IEC870 Date & Time]*
Stage 1 Revision Date				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Stg2 f+t Sta	05	0A		Stg2 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 2				
Stg2 f+t Trp	05	0B		Stg2 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 2				
Stg2 f+df/dt Trp	05	0C		Stg2 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 2				
Stg2 df/dt+t Sta	05	0D		Stg2 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 2				
Stg2 df/dt+t Trp	05	0E		Stg2 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 2				
Stg2 f+Df/Dt Sta	05	0F		Stg2 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 2				
Stg2 f+Df/Dt Trp	05	10		Stg2 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 2				
Stg2 Revn Date	05	11		Stg2 Revn Date *[IEC870 Date & Time]*
Stage 2 Revision Date				
Stg3 f+t Sta	05	13		Stg3 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 3				
Stg3 f+t Trp	05	14		Stg3 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 3				
Stg3 f+df/dt Trp	05	15		Stg3 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 3				
Stg3 df/dt+t Sta	05	16		Stg3 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 3				
Stg3 df/dt+t Trp	05	17		Stg3 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 3				
Stg3 f+Df/Dt Sta	05	18		Stg3 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 3				
Stg3 f+Df/Dt Trp	05	19		Stg3 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 3				
Stg3 Revn Date	05	1A		Stg3 Revn Date *[IEC870 Date & Time]*
Stage 3 Revision Date				
Stg4 f+t Sta	05	1C		Stg4 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 4				
Stg4 f+t Trp	05	1D		Stg4 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 4				
Stg4 f+df/dt Trp	05	1E		Stg4 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 4				
Stg4 df/dt+t Sta	05	1F		Stg4 df/dt+t Sta *[Unsigned Integer (16 bits)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Number of df/dt+t starts for Stage 4				
Stg4 df/dt+t Trp	05	20		Stg4 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 4				
Stg4 f+Df/Dt Sta	05	21		Stg4 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 4				
Stg4 f+Df/Dt Trp	05	22		Stg4 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 4				
Stg4 Revn Date	05	23		Stg4 Revn Date *[IEC870 Date & Time]*
Stage 4 Revision Date				
Stg5 f+t Sta	05	25		Stg5 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 5				
Stg5 f+t Trp	05	26		Stg5 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 5				
Stg5 f+df/dt Trp	05	27		Stg5 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 5				
Stg5 df/dt+t Sta	05	28		Stg5 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 5				
Stg5 df/dt+t Trp	05	29		Stg5 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 5				
Stg5 f+Df/Dt Sta	05	2A		Stg5 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 5				
Stg5 f+Df/Dt Trp	05	2B		Stg5 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 5				
Stg5 Revn Date	05	2C		Stg5 Revn Date *[IEC870 Date & Time]*
Stage 5 Revision Date				
Stg6 f+t Sta	05	2E		Stg6 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 6				
Stg6 f+t Trp	05	2F		Stg6 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 6				
Stg6 f+df/dt Trp	05	30		Stg6 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 6				
Stg6 df/dt+t Sta	05	31		Stg6 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 6				
Stg6 df/dt+t Trp	05	32		Stg6 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 6				
Stg6 f+Df/Dt Sta	05	33		Stg6 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 6				
Stg6 f+Df/Dt Trp	05	34		Stg6 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 6				
Stg6 Revn Date	05	35		Stg6 Revn Date

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[IEC870 Date & Time]
Stage 6 Revision Date				
Stg7 f+t Sta	05	37		Stg7 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 7				
Stg7 f+t Trp	05	38		Stg7 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 7				
Stg7 f+df/dt Trp	05	39		Stg7 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 7				
Stg7 df/dt+t Sta	05	3A		Stg7 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 7				
Stg7 df/dt+t Trp	05	3B		Stg7 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 7				
Stg7 f+Df/Dt Sta	05	3C		Stg7 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 7				
Stg7 f+Df/Dt Trp	05	3D		Stg7 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 7				
Stg7 Revn Date	05	3E		Stg7 Revn Date *[IEC870 Date & Time]*
Stage 7 Revision Date				
Stg8 f+t Sta	05	40		Stg8 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 8				
Stg8 f+t Trp	05	41		Stg8 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 8				
Stg8 f+df/dt Trp	05	42		Stg8 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 8				
Stg8 df/dt+t Sta	05	43		Stg8 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 8				
Stg8 df/dt+t Trp	05	44		Stg8 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 8				
Stg8 f+Df/Dt Sta	05	45		Stg8 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 8				
Stg8 f+Df/Dt Trp	05	46		Stg8 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 8				
Stg8 Revn Date	05	47		Stg8 Revn Date *[IEC870 Date & Time]*
Stage 8 Revision Date				
Stg9 f+t Sta	05	49		Stg9 f+t Sta *[Unsigned Integer (16 bits)]*
Number of f+t starts for Stage 9				
Stg9 f+t Trp	05	4A		Stg9 f+t Trp *[Unsigned Integer (16 bits)]*
Number of f+t trips for Stage 9				
Stg9 f+df/dt Trp	05	4B		Stg9 f+df/dt Trp *[Unsigned Integer (16 bits)]*
Number of f+df/dt trips for Stage 9				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Stg9 df/dt+t Sta	05	4C		Stg9 df/dt+t Sta *[Unsigned Integer (16 bits)]*
Number of df/dt+t starts for Stage 9				
Stg9 df/dt+t Trp	05	4D		Stg9 df/dt+t Trp *[Unsigned Integer (16 bits)]*
Number of df/dt trips for Stage 9				
Stg9 f+Df/Dt Sta	05	4E		Stg9 f+Df/Dt Sta *[Unsigned Integer (16 bits)]*
Number of f+DF/DT starts for Stage 9				
Stg9 f+Df/Dt Trp	05	4F		Stg9 f+Df/Dt Trp *[Unsigned Integer (16 bits)]*
Number of f+DF/DT trips for Stage 9				
Stg9 Revn Date	05	50		Stg9 Revn Date *[IEC870 Date & Time]*
Stage 9 Revision Date				
Reset Statistics	05	52	No Operation	No Operation All Stage 1 Stage 2 Stage 3 Stage 4 Stage 5 Stage 6 Stage 7 Stage 8 Stage 9 *[Indexed String]*
This command resets the statistics on a stage by stage basis or for all stages at once				
CB CONDITION	06	00		
This column contains CB condition monitoring measured parameters				
CB Operations	06	01		CB Operations *[Unsigned Integer (16 bits)]*
This cell displays the number of CB Operations				
Total IA Broken	06	02		Total IA Broken *[Courier Number (current)]*
This cell displays the total broken IA since the last maintenance procedure				
Total IB Broken	06	03		Total IB Broken *[Courier Number (current)]*
This cell displays the total broken IB since the last maintenance procedure				
Total IC Broken	06	04		Total IC Broken *[Courier Number (current)]*
This cell displays the total broken IC since the last maintenance procedure				
CB Operate Time	06	05		CB Operate Time *[Courier Number (time-seconds)]*
This cell displays the CB Operate Time				
Reset CB Data	06	06	No	No Yes *[Indexed String]*
This cell resets the CB condition monitoring data				
CB CONTROL	07	00		
This column controls the circuit Breaker Control configuration				
CB Control by	07	01	Disabled	Disabled Local Remote Local+Remote Opto Opto+local Opto+Remote Opto+Rem+local *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting selects the type of circuit breaker control to be used				
Close Pulse Time	07	02	0.5	From 0.1 to 50 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the CB should close when a close command is issued.				
Trip Pulse Time	07	03	0.5	From 0.1 to 5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the CB should trip when a manual or protection trip command is issued.				
Man Close Delay	07	05	10	From 0.01 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the delay time before the close pulse is executed.				
CB Healthy Time	07	06	5	From 0.01 to 9999 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the time period in which a CB needs to indicate a healthy condition before it closes. If the CB does not indicate a healthy condition in this time period following a close command then the IED will lockout and alarm.				
Sys Check Time	07	07	5	From 0.01 to 9999 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets a time delay for manual closure with System Check Synchronizing. If the System Check Synchronizing criteria are not satisfied in this time period following a close command, the IED will lockout and produce an alarm.				
Lockout Reset	07	08	No	No Yes *[Indexed String]*
This command resets the Autoreclose Lockout.				
Reset Lockout by	07	09	CB Close	User Interface CB Close *[Indexed String]*
This setting defines whether the Lockout signal is to be reset by the user interface or a CB Close signal.				
Man Close RstDly	07	0A	5	From 0.1 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time delay before the Lockout state can be reset following a manual closure.				
Autoreclose Mode	07	0B	No Operation	No Operation Auto Non Auto *[Indexed String]*
This command changes the Autoreclose mode				
AR Status	07	0E		Auto Mode Non-auto Mode Live Line *[Indexed String]*
This cell displays the Autoreclose - In Service or Out of Service				
Total Reclosures	07	0F		Total Reclosures *[Unsigned Integer (16 bits)]*
This cell displays the number of successful reclosures.				
Reset Total AR	07	10	No	No Yes *[Indexed String]*
This command allows you to reset the Autoreclose counters.				
CB Status Input	07	11	None	None 52A 52B Both 52A and 52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
1 Shot Clearance	07	12		1 Shot Clearance *[Unsigned Integer (16 bits)]*
This cell displays the total number of successful clearances after 1 shot				
2 Shot Clearance	07	13		2 Shot Clearance *[Unsigned Integer (16 bits)]*
This cell displays the total number of successful clearances after 2 shots				
3 Shot Clearance	07	14		3 Shot Clearance

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Unsigned Integer (16 bits)]
This cell displays the total number of successful clearances after 3 shots				
4 Shot Clearance	07	15		4 Shot Clearance *[Unsigned Integer (16 bits)]*
This cell displays the total number of successful clearances after 4 shots				
Persistent Fault	07	16		Persistent Fault *[Unsigned Integer (16 bits)]*
This cell displays the total number of unsuccessful clearances after which the Autoreclose went into lockout.				
Shot1 Recloses	07	20		Shot1 Recloses *[Unsigned Integer (16 bits)]*
This cell displays the total number of single-shot shot reclose attempts				
Shot234 Recloses	07	21		Shot234 Recloses *[Unsigned Integer (16 bits)]*
This cell displays the total number of multi-shot reclose attempts				
DATE AND TIME	08	00		
This column contains Date and Time stamp settings				
Date/Time	08	01		
This setting defines the IED's current date and time.				
IRIG-B Sync	08	04	None	None RP1 RP2 *[Indexed String]*
This setting enables or disables IRIG-B synchronisation and defines which rear port is to be used as an IRIG-B input.				
IRIG-B Status	08	05		Disabled Signal Healthy No Signal *[Indexed String]*
This cell displays the IRIG-B status				
SNTP Status	08	13		Disabled Trying Server 1 Trying Server 2 Server 1 OK Server 2 OK No Response No Valid Clock *[Indexed String]*
This cell displays the SNTP time synchronisation status for IEC61850 or DNP3 over Ethernet versions.				
LocalTime Enable	08	20	Fixed	Disabled Fixed Flexible *[Indexed String]*
Disabled: No local time zone will be maintained Fixed - Local time zone adjustment can be defined (all interfaces) Flexible - Local time zone adjustment can be defined (non-local interfaces)				
LocalTime Offset	08	21	0	From -720 to 720 in steps of 15 *[Courier Number (time-minutes)]*
This setting specifies the offset for the local time zone from -12 hours to +12 hrs in 15 minute intervals. This adjustment is applied to the time based on the UTC/GMT master clock.				
DST Enable	08	22	Enabled	Disabled Enabled *[Indexed String]*
This setting turns daylight saving time adjustment on or off.				
DST Offset	08	23	60	30 or 60 *[Courier Number (time-minutes)]*
This setting defines the daylight saving offset used for the local time adjustment.				
DST Start	08	24	Last	First Second Third Fourth Last

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting specifies the week of the month in which daylight saving time adjustment starts.				
DST Start Day	08	25	Sunday	Sunday Monday Tuesday Wednesday Thursday Friday Saturday *[Indexed String]*
This setting specifies the day of the week in which daylight saving time adjustment starts				
DST Start Month	08	26	March	January February March April May June July August September October November December *[Indexed String]*
This setting specifies the month in which daylight saving time adjustment starts				
DST Start Mins	08	27	60	From 0 to 1425 in steps of 15 *[Courier Number (time-minutes)]*
Setting to specify the time of day in which daylight saving time adjustment starts. This is set relative to 00:00 hrs on the selected day when time adjustment is to start				
DST End	08	28	Last	First Second Third Fourth Last *[Indexed String]*
This setting specifies the week of the month in which daylight saving time adjustment ends				
DST End Day	08	29	Sunday	Sunday Monday Tuesday Wednesday Thursday Friday Saturday *[Indexed String]*
This setting specifies the day of the week in which daylight saving time adjustment ends.				
DST End Month	08	2A	October	January February March April May June July August September October November December *[Indexed String]*
This setting specifies the month in which daylight saving time adjustment ends.				
DST End Mins	08	2B	60	From 0 to 1425 in steps of 15 *[Courier Number (time-minutes)]*
This setting specifies the time of day in which daylight saving time adjustment ends. This is set relative to 00:00 hrs on the selected day				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
when time adjustment is to end.				
RP1 Time Zone	08	30	Local	UTC Local *[Indexed String]*
Setting for the rear port 1 interface to specify if time synchronisation received will be local or universal time co-ordinated.				
RP2 Time Zone	08	31	Local	UTC Local *[Indexed String]*
Setting for the rear port 2 interface to specify if time synchronisation received will be local or universal time co-ordinated				
DNPOE Time Zone	08	32	Local	UTC Local *[Indexed String]*
This setting specifies whether DNP3.0 over Ethernet time synchronisation is coordinated by local time or universal time.				
Tunnel Time Zone	08	33	Local	UTC Local *[Indexed String]*
This setting specifies whether tunnelled Courier time synchronisation is coordinated by local time or universal time.				
CONFIGURATION	09	00		
This column contains the general configuration options				
Restore Defaults	09	01	No Operation	No Operation All Settings Setting Group 1 Setting Group 2 Setting Group 3 Setting Group 4 *[Indexed String]*
This setting restores the chosen setting groups to factory default values. Note: Restoring defaults to all settings may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.				
Setting Group	09	02	Select via Menu	Select via Menu Select via Opto *[Indexed String]*
This setting allows you to choose whether the setting group changes are to be initiated via an Opto-input or the HMI menu.				
Active Settings	09	03	Group 1	Group 1 Group 2 Group 3 Group 4 *[Indexed String]*
This setting selects the active settings group.				
Save Changes	09	04	No Operation	No Operation Save Abort *[Indexed String]*
This command saves all IED settings.				
Copy From	09	05	Group 1	Group 1 Group 2 Group 3 Group 4 *[Indexed String]*
This setting copies settings from a selected setting group.				
Copy To	09	06	No Operation	No Operation Group 1 Group 2 Group 3 Group 4 *[Indexed String]*
This command allows the displayed settings to be copied to a selected setting group.				
Setting Group 1	09	07	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables settings Group 1.				
Setting Group 2	09	08	Disabled	Disabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Enabled *[Indexed String]*
This setting enables or disables settings Group 2.				
Setting Group 3	09	09	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables settings Group 3.				
Setting Group 4	09	0A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables settings Group 4.				
System Config	09	0B	Visible	Invisible Visible *[Indexed String]*
This setting hides or unhides the System Config menu.				
WDE Protection	09	0F	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the PWH2 Protection function.				
Overcurrent	09	10	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Phase overcurrent Protection function.				
Neg Sequence O/C	09	11	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Negative Sequence overcurrent Protection function.				
Broken Conductor	09	12	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Broken Conductor function.				
Earth Fault 1	09	13	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the measured Earth Fault Protection function.				
Earth Fault 2	09	14	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the derived Earth Fault Protection function.				
Earth Fault 2	09	14	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the derived Earth Fault Protection function for model H.				
SEF Protection	09	15	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Sensitive Earth Fault Protection function.				
Residual O/V NVD	09	16	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Residual Overvoltage Protection function.				
Residual O/V NVD	09	16	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Residual Overvoltage Protection function for model H.				
Thermal Overload	09	17	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Thermal Overload Protection function.				
Thermal Overload	09	17	Disabled	Disabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Enabled *[Indexed String]*
This setting enables or disables the Thermal Overload Protection function for model H.				
Neg Sequence O/V	09	18	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Negative Sequence Overvoltage Protection function.				
Cold Load Pickup	09	19	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Cold Load Pickup protection.				
Selective Logic	09	1A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Selective Logic element.				
Admit Protection	09	1B	Disabled	Disabled Enabled *[Indexed String]*
This cell enables or disables the Admittance Protection.				
Power Protection	09	1C	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Power protection function.				
Power Protection	09	1C	Disabled	Disabled *[Indexed String]*
This setting disables the Power protection function for model B				
Volt Protection	09	1D	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Voltage protection.				
Volt Protection	09	1D	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Voltage protection for model H.				
REF Protection	09	1E	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Restricted Earth Fault Protection.				
DC SupplyMonitor	09	1F	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the DC Supply Monitoring supervision function.				
CB Fail	09	20	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Circuit Breaker Fail Protection function.				
Supervision	09	21	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Supervision (VTS & CTS) functions.				
Supervision	09	21	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Supervision (VTS & CTS) functions for model H.				
Fault Locator	09	22	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Fault Locator function.				
Fault Locator	09	22	Disabled	Disabled *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting disables the Fault Locator function for models B and G				
System Checks	09	23	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the System Checks function (Check Synchronisation and Voltage Monitor).				
Auto-Reclose	09	24	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Autoreclose function.				
Auto-Reclose	09	24	Disabled	Disabled *[Indexed String]*
This setting disables the Autoreclose function for some models				
Input Labels	09	25	Visible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Input Labels menu from the IED display.				
Output Labels	09	26	Visible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Output Labels menu from the IED display.				
Freq Protection	09	27	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Frequency Protection function.				
Freq Protection	09	27	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Frequency Protection function for model H.				
CT & VT Ratios	09	28	Visible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Transformer Ratios menu from the IED display.				
Record Control	09	29	Invisible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Record Control menu from the IED display.				
Disturb Recorder	09	2A	Invisible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Disturbance Recorder menu from the IED display.				
Measure't Setup	09	2B	Invisible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Measurement Setup menu from the IED display.				
Comms Settings	09	2C	Visible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Communication Settings menu from the IED display.				
Commission Tests	09	2D	Visible	Invisible Visible *[Indexed String]*
This setting hides or unhides the Commission Tests menu from the IED display.				
Setting Values	09	2E	Primary	Primary Secondary *[Indexed String]*
This setting determines the reference for all settings dependent on the transformer ratios; either referenced to the primary or the secondary.				
Control Inputs	09	2F	Visible	Invisible Visible *[Indexed String]*
Activates the Control Input status and operation menu further on in the IED setting menu.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Ctrl I/P Config	09	35	Visible	Invisible Visible *[Indexed String]*
Sets the Control Input Configuration menu visible further on in the IED setting menu.				
Ctrl I/P Labels	09	36	Visible	Invisible Visible *[Indexed String]*
Sets the Control Input Labels menu visible further on in the IED setting menu.				
HIF Detection	09	37	Disabled	Disabled *[Indexed String]*
This setting enables or disables the High Impedance (HIF) function.				
Direct Access	09	39	Enabled	Disabled Enabled Hotkey Only CB Ctrl Only *[Indexed String]*
This setting enables or disables direct control of the Circuit Breakers from the IED's hotkeys.				
Direct Access	09	39	Disabled	Disabled Enabled Hotkey Only CB Ctrl Only *[Indexed String]*
This setting enables or disables direct control of the Circuit Breakers from the IED's hotkeys for model H.				
Function Key	09	50	Visible	Invisible Visible *[Indexed String]*
This setting enables or disables the Function Key menu.				
PSL Timers	09	54	Invisible	Invisible Visible *[Indexed String]*
This setting enables or disables the PSL Timers menu.				
Switch Control	09	60	Disabled	Disabled Enabled *[Indexed String]*
Activates the user switch Input status and operation menu.				
RP1 Read Only	09	FB	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables Read Only Mode for Rear Port 1.				
RP2 Read Only	09	FC	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables Read Only Mode for Rear Port 2.				
NIC Read Only	09	FD	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables Read Only Mode of the Network Interface Card for Ethernet models.				
LCD Contrast	09	FF	13	From 0 to 31 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the LCD contrast.				
CT AND VT RATIOS	0A	00		
This column contains settings for Current and Voltage Transformer ratios				
Main VT Primary	0A	01	110	From 100 to 1000000 in steps of 1 *[Courier Number (voltage)]*
This setting sets the main voltage transformer input primary voltage.				
Main VT Sec'y	0A	02	110	From 40 to 140 in steps of 0.1 *[Courier Number (voltage)]*
This setting sets the main voltage transformer input secondary voltage.				
4th VT Primary	0A	03	110	From 100 to 1000000 in steps of 1 *[Courier Number (voltage)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the 4th VT voltage transformer input primary voltage. This 4th VT input can be used for System Check Synchronism or for Measured Residual Overvoltage Protections.				
4th VT Secondary	0A	04	110	From 40 to 140 in steps of 0.1 *[Courier Number (voltage)]*
This setting sets the 4th VT voltage transformer input secondary voltage. This 4th VT input can be used for System Check Synchronism or for Measured Residual Overvoltage Protections.				
4th VT Primary	0A	05	110	From 100 to 1000000 in steps of 1 *[Courier Number (voltage)]*
This setting sets the 4th VT voltage transformer input primary voltage. This 4th VT input can be used for Remanent Overvoltage or for Measured Residual Overvoltage Protections.				
4th VT Secondary	0A	06	110	From 40 to 200 in steps of 0.1 *[Courier Number (voltage)]*
This setting sets the 4th VT voltage transformer input secondary voltage. This 4th VT input can be used for Remanent Overvoltage or for Measured Residual Overvoltage Protections.				
Phase CT Primary	0A	07	1	From 1 to 30000 in steps of 1 *[Courier Number (current)]*
This setting sets the phase current transformer input primary current rating.				
Phase CT Sec'y	0A	08	1	1 or 5 *[Courier Number (current)]*
This setting sets the phase current transformer input secondary current rating.				
E/F CT Primary	0A	09	1	From 1 to 30000 in steps of 1 *[Courier Number (current)]*
This setting sets the earth fault current transformer input primary current rating.				
E/F CT Secondary	0A	0A	1	1 or 5 *[Courier Number (current)]*
This setting sets the earth fault current transformer input secondary current rating.				
SEF CT Primary	0A	0B	1	From 1 to 30000 in steps of 1 *[Courier Number (current)]*
This setting sets the sensitive earth fault current transformer input primary current rating.				
SEF CT Secondary	0A	0C	1	1 or 5 *[Courier Number (current)]*
Sets the sensitive earth fault current transformer input secondary current rating.				
C/S Input	0A	0F	A-N	A-N B-N C-N A-B B-C C-A *[Indexed String]*
This setting selects the System Check Synchronism Input voltage measurement.				
Main VT Location	0A	10	Line	Line Bus *[Indexed String]*
This setting defines the Main VT Location.				
C/S V kSM	0A	14	1	From 0.1 to 5 in steps of 0.001 *[Courier Number (decimal)]*
This setting sets the voltage magnitude correction factor for check synchronism in case of different VT ratios.				
C/S Phase kSA	0A	15	0	From -150 to 180 in steps of 30 *[Courier Number (angle)]*
This setting sets the phase angle correction factor for check synchronism.				
VN Input	0A	16	Derived	Measured Derived *[Indexed String]*
This cell indicates that VN Input is measured or derived.				
VN Input	0A	16	Measured	Measured Derived *[Indexed String]*
This cell indicates that VN Input is measured or derived.				
Phas CT Polarity	0A	20	Direct	Direct Inverse

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting defines the phase CT polarity				
Neut CT Polarity	0A	21	Direct	Direct Inverse *[Indexed String]*
This setting defines the neutral CT polarity				
RECORD CONTROL	0B	00		
This column contains settings for Record Controls.				
Alarm Event	0B	04	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of an event on alarm. Disabling this setting means that no event is generated for alarms.				
Relay O/P Event	0B	05	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of an event for a change of state of output relay contact. Disabling this setting means that no event will be generated for any change in logic output state.				
Opto Input Event	0B	06	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of an event for a change of state of opto-input. Disabling this setting means that no event will be generated for any change in logic input state.				
General Event	0B	07	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of general events. Disabling this setting means that no general events are generated.				
Fault Rec Event	0B	08	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of fault record events. Disabling this setting means that no event will be generated for any fault that produces a fault record.				
Maint Rec Event	0B	09	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of maintenance record events. Disabling this setting means that no event will be generated for any occurrence that produces a maintenance record.				
Protection Event	0B	0A	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the generation of protection events. Disabling this setting means that any operation of protection elements will not be logged as an event.				
DDB 31 - 0	0B	40	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 63 - 32	0B	41	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 95 - 64	0B	42	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 127 - 96	0B	43	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 159 - 128	0B	44	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 191 - 160	0B	45	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 223 - 192	0B	46	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 255 - 224	0B	47	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 287 - 256	0B	48	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 319 - 288	0B	49	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 351 - 320	0B	4A	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 383 - 352	0B	4B	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 415 - 384	0B	4C	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 447 - 416	0B	4D	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 479 - 448	0B	4E	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 511 - 480	0B	4F	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
DDB 543 - 512	0B	50	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 575 - 544	0B	51	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 607 - 576	0B	52	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 639 - 608	0B	53	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 671 - 640	0B	54	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 703 - 672	0B	55	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 735 - 704	0B	56	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 767 - 736	0B	57	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 799 - 768	0B	58	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 831 - 800	0B	59	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 863 - 832	0B	5A	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 895 - 864	0B	5B	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 927 - 896	0B	5C	0xFFFFFFFF	High order word of long stored in 1st register

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 959 - 928	0B	5D	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 991 - 960	0B	5E	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1023 - 992	0B	5F	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1055 - 1024	0B	60	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1087 - 1056	0B	61	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1119 - 1088	0B	62	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1151 - 1120	0B	63	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1183 - 1152	0B	64	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1215 - 1184	0B	65	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1247 - 1216	0B	66	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1279 - 1248	0B	67	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1311 - 1280	0B	68	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1343 - 1312	0B	69	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1375 - 1344	0B	6A	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1407 - 1376	0B	6B	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1439 - 1408	0B	6C	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1471 - 1440	0B	6D	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1503 - 1472	0B	6E	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1535 - 1504	0B	6F	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1567 - 1536	0B	70	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1599 - 1568	0B	71	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1631 - 1600	0B	72	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1663 - 1632	0B	73	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1695 - 1664	0B	74	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Binary Flag (32 bits)]
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1727 - 1696	0B	75	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1759- 1728	0B	76	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1791- 1760	0B	77	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1823 - 1792	0B	78	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1855 - 1824	0B	79	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1887 - 1856	0B	7A	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1919 - 1888	0B	7B	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1951 - 1920	0B	7C	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 1983 - 1952	0B	7D	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 2015 - 1984	0B	7E	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DDB 2047 - 2016	0B	7F	0xFFFFFFFF	High order word of long stored in 1st register Low order word of long stored in 2nd register Example 123456 stored as 123456 *[Binary Flag (32 bits)]*
These signals can be included or excluded from being stored as a Courier event record (assuming the DDB is capable of creating an event)				
DISTURB RECORDER	0C	00		
This column contains settings for the Disturbance Recorder				
Duration	0C	01	1.5	From 0.1 to 10.5 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the overall recording time.				
Trigger Position	0C	02	33.3	From 0 to 100 in steps of 0.1 *[Courier Number (percentage)]*
This setting sets the trigger point as a percentage of the duration. For example, the default setting, which is set to 33.3% (of 1.5s) gives 0.5s pre-fault and 1s post fault recording times.				
Trigger Mode	0C	03	Single	Single Extended *[Indexed String]*
When set to single mode, if a further trigger occurs whilst a recording is taking place, the recorder will ignore the trigger. However, if this has been set to Extended, the post trigger timer will be reset to zero, thereby extending the recording time.				
Analog Channel 1	0C	04	VA	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 2	0C	05	VB	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 3	0C	06	VC	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 4	0C	07	V Checksync	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 4	0C	07	V N	VA VB VC 4th V IA IB IC IN - ISEF

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 5	0C	08	IA	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 6	0C	09	IB	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 7	0C	0A	IC	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 8	0C	0B	IN-ISEF	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Analog Channel 9	0C	0C	Frequency	VA VB VC 4th V IA IB IC IN - ISEF Frequency *[Indexed String]*
This setting selects any available analogue input to be assigned to this channel.				
Digital Input 1	0C	0D	Output R1	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Input 1 Trigger	0C	0E	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 2	0C	0F	Output R2	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 2 Trigger	0C	10	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 3	0C	11	Output R3	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 3 Trigger	0C	12	Trigger L/H	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 4	0C	13	Output R4	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 4 Trigger	0C	14	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 5	0C	15	Output R5	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 5 Trigger	0C	16	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 6	0C	17	Output R6	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 6 Trigger	0C	18	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 7	0C	19	Output R7	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 7 Trigger	0C	1A	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 8	0C	1B	Output R8	From 0 to DDB Size in steps of 1 *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 8 Trigger	0C	1C	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 9	0C	1D	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 9 Trigger	0C	1E	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 10	0C	1F	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 10 Trigger	0C	20	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 11	0C	21	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 11 Trigger	0C	22	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 12	0C	23	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 12 Trigger	0C	24	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 13	0C	25	Input L1	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 13 Trigger	0C	26	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 14	0C	27	Input L2	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 14 Trigger	0C	28	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Digital Input 15	0C	29	Input L3	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 15 Trigger	0C	2A	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 16	0C	2B	Input L4	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 16 Trigger	0C	2C	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 17	0C	2D	Input L5	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 17 Trigger	0C	2E	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 18	0C	2F	Input L6	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 18 Trigger	0C	30	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 19	0C	31	Input L7	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 19 Trigger	0C	32	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 20	0C	33	Input L8	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 20 Trigger	0C	34	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 21	0C	35	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto isolated inputs or output contacts, in addition to a number of internal IED digital signals, such as protection starts, LEDs etc.				
Input 21 Trigger	0C	36	No Trigger	No Trigger Trigger L/H Trigger H/L

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 22	0C	37	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 22 Trigger	0C	38	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 23	0C	39	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 23 Trigger	0C	3A	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 24	0C	3B	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 24 Trigger	0C	3C	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 25	0C	3D	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto isolated inputs or output contacts, in addition to a number of internal IED digital signals, such as protection starts, LEDs etc.				
Input 25 Trigger	0C	3E	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 26	0C	3F	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 26 Trigger	0C	40	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 27	0C	41	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 27 Trigger	0C	42	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 28	0C	43	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Input 28 Trigger	0C	44	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 29	0C	45	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 29 Trigger	0C	46	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 30	0C	47	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 30 Trigger	0C	48	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 31	0C	49	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 31 Trigger	0C	4A	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 32	0C	4B	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Input 32 Trigger	0C	4C	No Trigger	No Trigger Trigger L/H Trigger H/L *[Indexed String]*
This setting defines whether the digital input is triggered and if so, the trigger polarity (low to high or high to low).				
Digital Input 33	0C	4D	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 34	0C	4E	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 35	0C	4F	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 36	0C	50	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 37	0C	51	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts,				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 38	0C	52	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 39	0C	53	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 40	0C	54	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 41	0C	55	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 42	0C	56	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 43	0C	57	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 44	0C	58	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 45	0C	59	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 46	0C	5A	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 47	0C	5B	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 48	0C	5C	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 49	0C	5D	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 50	0C	5E	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 51	0C	5F	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 52	0C	60	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts,				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 53	0C	61	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 54	0C	62	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 55	0C	63	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 56	0C	64	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 57	0C	65	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 58	0C	66	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 59	0C	67	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 60	0C	68	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 61	0C	69	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 62	0C	6A	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 63	0C	6B	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
Digital Input 64	0C	6C	Unused	From 0 to DDB Size in steps of 1 *[Indexed String]*
The digital channels may monitor any of the opto-inputs, output relay contacts and other internal digital signals, such as protection starts, LEDs etc. This setting assigns the digital channel to any one of these.				
MEASUREMENT SETUP	0D	00		
This column contains settings for the measurement setup				
Default Display	0D	01	Banner	User Banner 3Ph + N Current 3Ph Voltage Power Date and Time Description Plant Reference Frequency Access Level

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				DC Supply Mag *[Indexed String]*
This cell is used to show the default display option.				
Local Values	0D	02	Primary	Primary Secondary *[Indexed String]*
This setting controls whether local measured values (via HMI or front port) are displayed as primary or secondary quantities.				
Remote Values	0D	03	Primary	Primary Secondary *[Indexed String]*
This setting controls whether remote measured values (via rear comms ports) are displayed as primary or secondary quantities.				
Measurement Ref	0D	04	VA	VA VB VC IA IB IC *[Indexed String]*
This setting sets the phase reference for all angular measurements (for Measurements 1 only).				
Measurement Mode	0D	05	0	From 0 to 3 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is used to control the signing of the real and reactive power quantities.				
Fix Dem Period	0D	06	30	From 1 to 99 in steps of 1 *[Courier Number (time-minutes)]*
This setting defines the length of the fixed demand window in minutes				
Roll Sub Period	0D	07	30	From 1 to 99 in steps of 1 *[Courier Number (time-minutes)]*
This setting is used to set the length of the window used for the calculation of rolling demand quantities (in minutes).				
Num Sub Periods	0D	08	1	From 1 to 15 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is used to set the resolution of the rolling sub window.				
Distance Unit	0D	09	Miles	Kilometres Miles *[Indexed String]*
This setting is used to select the unit of distance for fault location purposes.				
Fault Location	0D	0A	Distance	Distance Ohms % of Line *[Indexed String]*
This setting sets the way the fault location is displayed - in terms of distance, impedance, or percentage of line length.				
Remote2 Values	0D	0B	Primary	Primary Secondary *[Indexed String]*
The setting defines whether the values measured via the Second Rear Communication port are displayed in primary or secondary terms.				
COMMUNICATIONS	0E	00		
This column contains general communications settings				
RP1 Protocol	0E	01		Courier IEC60870-5-103 Modbus DNP 3.0 *[Indexed String]*
This setting sets the address of RP1.				
RP1 Address	0E	02	255	From 0 to 255 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the address of RP1.				
RP1 Address	0E	02	1	From 1 to 247 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the address of RP1.				
RP1 Address	0E	02	1	From 0 to 254 in steps of 1 *[Unsigned Integer (16 bits)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the address of RP1.				
RP1 Address	0E	02	1	From 0 to 65519 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the address of RP1.				
RP1 InactivTimer	0E	03	15	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting defines the period of inactivity on RP1 before the IED reverts to its default state.				
RP1 Baud Rate	0E	04	19200	9600 bits/s 19200 bits/s 38400 bits/s *[Indexed String]*
This setting sets the communication speed between the IED RP1 port and the master station. It is important that both IED and master station are set at the same speed setting. This cell is applicable for the non-Courier protocols. Build = Modbus				
RP1 Baud Rate	0E	04	19200	9600 bits/s 19200 bits/s *[Indexed String]*
This setting sets the communication speed between the IED RP1 port and the master station. It is important that both IED and master station are set at the same speed setting. This cell is applicable for the non-Courier protocols. Build = CS103				
RP1 Baud Rate	0E	04	19200	1200 bits/s 2400 bits/s 4800 bits/s 9600 bits/s 19200 bits/s 38400 bits/s *[Indexed String]*
This setting sets the communication speed between the IED RP1 port and the master station. It is important that both IED and master station are set at the same speed setting. This cell is applicable for the non-Courier protocols. Build = DNP3.0				
RP1 Parity	0E	05	None	Odd Even None *[Indexed String]*
This setting controls the parity format used in the data frames of RP1. It is important that both IED and master station are set with the same parity setting.				
RP1 Meas Period	0E	06	15	From 1 to 60 in steps of 1 *[Courier Number (time-seconds)]*
This setting controls the time interval that the IED will use between sending measurement data to the master station for IEC60870-5-103 versions.				
RP1 Time Sync	0E	08	Disabled	Disabled Enabled *[Indexed String]*
This setting is for DNP3.0 versions only. If set to Enabled the master station can be used to synchronize the time on the IED via RP1. If set to Disabled either the internal free running clock or IRIG-B input are used.				
Modbus IEC Time	0E	09	Standard	Standard IEC (Existing format) Reverse IEC (Company agreed format) *[Indexed String]*
When 'Standard IEC' is selected the time format complies with IEC60870-5-4 requirements such that byte 1 of the information is transmitted first, followed by bytes 2 through to 7. If 'Reverse' is selected the transmission of information is reversed.				
RP1 CS103Blcking	0E	0A	Disabled	Disabled Monitor Blocking Command Blocking *[Indexed String]*
This cell sets the blocking type for IEC60870-5-103. With monitor blocking, reading of the status information and disturbance records is not permitted. When in this mode the IED returns a "termination of general interrogation" message to the master station				
RP1 Card Status	0E	0B		K-Bus OK EIA485 OK IRIG-B *[Indexed String]*
This setting displays the communication type and status of RP1				
RP1 Port Config	0E	0C	EIA485 (RS485)	K-Bus EIA485 (RS485) *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting selects the type of physical protocol for RP1 - either K-bus or RS485.				
RP1 Comms Mode	0E	0D	IEC60870 FT1.2	IEC60870 FT1.2 10-Bit No Parity *[Indexed String]*
This setting determines the serial communication mode.				
RP1 Baud Rate	0E	0E	19200	9600 bits/s 19200 bits/s 38400 bits/s *[Indexed String]*
This cell controls the communication speed between IED and master station. It is important that both IED and master station are set at the same speed setting. This cell is applicable for the Courier protocol.				
Meas Scaling	0E	0F	Primary	Normalised Primary Secondary *[Indexed String]*
This setting determines the scaling type of analogue quantities - in terms of primary, secondary or normalised, for DNP3 models				
Message Gap (ms)	0E	10	0	From 0 to 50 in steps of 1 *[Courier Number (time-ms)]*
This setting allows the master station to have an interframe gap. DNP 3.0 versions only				
DNP Need Time	0E	11	10	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the duration of time waited before requesting another time sync from the master. DNP 3.0 versions only.				
DNP App Fragment	0E	12	2048	From 100 to 2048 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the maximum message length (application fragment size) transmitted by the IED for DNP 3.0 versions.				
DNP App Timeout	0E	13	2	From 1 to 120 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time between sending a message fragment and receiving confirmation from the master. DNP 3.0 versions only.				
DNP SBO Timeout	0E	14	10	From 1 to 10 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time between receiving (sending?) a select command and awaiting an operate confirmation from the master. DNP 3.0 versions only.				
DNP Link Timeout	0E	15	0	From 0 to 120 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time for a Data Link Confirm from the master. A value of 0 means data link support disabled. DNP 3.0 versions only.				
Class 0 Poll	0E	16	0	Running Counters Frozen Counters *[Indexed String]*
This setting is for DNP3.0 versions only. In response to a Class 0 poll, an outstation device shall report either the count value or the frozen count value.				
NIC Protocol	0E	1F		UCA 2.0 UCA 2.0 GOOSE IEC61850 DNP3 IEC61850+DNP3 *[Indexed String]*
This cell indicates which Ethernet protocols are used on the rear Ethernet port.				
NIC MAC Address	0E	22	Ethernet MAC Address	NIC MAC Address *[ASCII Text (17 chars)]*
This setting displays the MAC address of the rear Ethernet port, if applicable.				
NIC Tunl Timeout	0E	64	5.00 min	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the maximum waiting time before an inactive tunnel to the application software is reset. DNP 3.0 over Ethernet versions only.				
NIC Link Report	0E	6A	Alarm	Alarm Event None *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting defines how a failed or unfitted network link is reported. DNP 3.0 over Ethernet versions only.				
REAR PORT2 (RP2)	0E	80		
The settings in this sub-menu are for models with a second communications port (RP2).				
RP2 Protocol	0E	81	Courier	Courier IEC60870-5-103 Modbus DNP 3.0 *[Indexed String]*
This cell displays the communications protocol relevant to main communication port (RP2) of the chosen IED model.				
RP2 Card Status	0E	84		K-Bus OK EIA485 OK IRIG-B *[Indexed String]*
This setting displays the communication type and status of RP2, if applicable				
RP2 Port Config	0E	88	EIA485 (RS485)	K-Bus EIA485 (RS485) *[Indexed String]*
This setting selects the type of physical protocol for RP2 - either K-bus or RS485.				
RP2 Comms Mode	0E	8A	IEC60870 FT1.2	IEC60870 FT1.2 10-Bit No Parity *[Indexed String]*
This setting determines the serial communication mode.				
RP2 Address	0E	90	255	From 0 to 255 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the address of RP2.				
RP2 InactivTimer	0E	92	15	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting defines the period of inactivity on RP2 before the IED reverts to its default state.				
RP2 Baud Rate	0E	94	19200	9600 bits/s 19200 bits/s 38400 bits/s *[Indexed String]*
This setting sets the communication speed between the IED RP2 port and the master station. It is important that both IED and master station are set at the same speed setting.				
NIC Protocol	0E	A0		UCA 2.0 UCA 2.0 GOOSE IEC61850 DNP3 IEC61850+DNP3 *[Indexed String]*
This cell indicates DNP 3.0 over Ethernet are used on the rear Ethernet port.				
IP Address	0E	A1	0.0.0.0	IP Address *[ASCII Text (16 chars)]*
This cell displays the IED's IP address. DNP over Ethernet versions only.				
Subnet Address	0E	A2	0.0.0.0	Subnet Address *[ASCII Text (16 chars)]*
This cell displays the LAN's subnet address on which the IED is located. DNP 3.0 over Ethernet versions only.				
NIC MAC Address	0E	A3	Ethernet MAC Address	NIC MAC Address *[ASCII Text (17 chars)]*
This setting displays the MAC address of the rear Ethernet port, if applicable.				
Gateway	0E	A4	0.0.0.0	Gateway *[ASCII Text (16 chars)]*
This cell displays the LAN's gateway address on which the IED is located. DNP 3.0 over Ethernet versions only.				
DNP Time Synch	0E	A5	Disabled	Disabled Enabled *[Indexed String]*
If set to 'Enabled' the DNP3.0 master station can be used to synchronise the IED's time clock. If set to 'Disabled' either the internal free running clock, or IRIG-B input are used. DNP 3.0 over Ethernet versions only.				
Meas Scaling	0E	A6	Primary	Normalised Primary

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Secondary *[Indexed String]*
This setting determines the scaling type of analogue quantities - in terms of primary, secondary or normalised, for DNP3 models.				
NIC Tunl Timeout	0E	A7	5	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the maximum waiting time before an inactive tunnel to the application software is reset. DNP 3.0 over Ethernet versions only.				
NIC Link Report	0E	A8	Alarm	Alarm Event None *[Indexed String]*
This setting defines how a failed or unfitted network link is reported. DNP 3.0 over Ethernet versions only.				
Media	0E	A9		Media Unknown RJ45 FO RJ45 Port A RJ45 Port B FO Port A FO Port B RJ45 Redundant FO Redundant *[Indexed String]*
Displays the communication media of the Ethernet port that is currently in use. DNP 3.0 over Ethernet versions only.				
SNTP PARAMETERS	0E	AA		
The settings in this sub-menu are for models using DNP3 over Ethernet.				
SNTP Server 1	0E	AB	0.0.0.0	SNTP Server 1 *[Courier Number (time-minutes)]*
This cell indicates the SNTP Server 1 address. DNP 3.0 over Ethernet versions only.				
SNTP Server 2	0E	AC	0.0.0.0	SNTP Server 2 *[Indexed String]*
This cell indicates the SNTP Server 2 address. DNP 3.0 over Ethernet versions only.				
SNTP Poll Rate	0E	AD	64s	SNTP Poll Rate *[Courier Number (time-seconds)]*
This cell displays the SNTP poll rate interval in seconds. DNP 3.0 over Ethernet versions only.				
DNP Need Time	0E	B1	10	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the duration of time waited before requesting another time sync from the master. DNP 3.0 versions only.				
DNP App Fragment	0E	B2	2048	From 100 to 2048 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the maximum message length (application fragment size) transmitted by the IED for DNP 3.0 versions.				
DNP App Timeout	0E	B3	2	From 1 to 120 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time between sending a message fragment and receiving confirmation from the master. DNP 3.0 versions only.				
DNP SBO Timeout	0E	B4	10	From 1 to 10 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time between receiving a select command and awaiting an operate confirmation from the master. DNP 3.0 versions only.				
Class 0 Poll	0E	B5	0	Running Counters Frozen Counters *[Indexed String]*
This setting is for DNP3.0 versions only. In response to a Class 0 poll, an outstation device shall report either the count value or the frozen count value.				
Redundancy	0E	CE		NONE FAILOVER RSTP PRP HSR *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
The settings is to indicate the type of Ethernet redundancy currently active				
RSTP	0E	D0		
The settings in this sub-menu are for models using RSTP				
Bridge MAC Address	0E	D1	0.0.0.0	Bridge MAC Address *[ASCII Text (17 chars)]*
This setting displays the Bridge MAC address of the device as per RSTP protocol				
Bridge Priority	0E	D2	32768	Bridge Priority *[Unsigned Integer (32 bits)]*
This setting displays the Bridge Priority configured in the device				
Root MAC Address	0E	D3	0.0.0.0	Root MAC Address *[ASCII Text (17 chars)]*
This setting displays the MAC address of the Root device as per RSTP protocol				
Root Priority	0E	D4	0	Root Priority *[Unsigned Integer (32 bits)]*
This setting displays the Root Priority of the Root device as per RSTP protocol				
Root Path Cost	0E	D5	0	Root Path Cost *[Unsigned Integer (32 bits)]*
This setting displays the Root Path Cost based on the RSTP network link speed				
Root Port	0E	D6	0	Unknown Port A Port B *[Indexed String]*
This setting displays the Root Port based on the root path cost in RSTP network.				
Root Max Age	0E	D7	0	Root Max Age *[Courier Number (time-seconds)]*
This setting displays the maximum age timer which specifies the maximum expected arrival time of hello BPDUs				
Root Hello Time	0E	D8	0	Root Hello Time *[Courier Number (time-seconds)]*
This setting displays the Hello time during which RSTP BPDUs are sent out				
RootForwardDelay	0E	D9	0	RootForwardDelay *[Courier Number (time-seconds)]*
This setting displays the Forward delay for the RSTP ports to be in FORWARDING State				
Port A State	0E	DA	Discarding	Unknown Disabled Discarding Learning Forwarding *[Indexed String]*
This setting displays the RSTP States DISCARDING, LEARNING or FORWARDING for Port A				
Port B State	0E	DB	Discarding	Unknown Disabled Discarding Learning Forwarding *[Indexed String]*
This setting displays the RSTP States DISCARDING, LEARNING or FORWARDING for Port B				
COMMISSION TESTS	0F	00		
This column contains commissioning test settings				
Opto I/P Status	0F	01		Opto 1 Input State (0=Off, 1=Energised) Opto 2 Input State (0=Off, 1=Energised) Opto 3 Input State (0=Off, 1=Energised) Opto 4 Input State (0=Off, 1=Energised) Opto 5 Input State (0=Off, 1=Energised) Opto 6 Input State (0=Off, 1=Energised) Opto 7 Input State (0=Off, 1=Energised) Opto 8 Input State (0=Off, 1=Energised) Opto 9 Input State (0=Off, 1=Energised) Opto 10 Input State (0=Off, 1=Energised) Opto 11 Input State (0=Off, 1=Energised) Opto 12 Input State (0=Off, 1=Energised)

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Opto 13 Input State (0=Off, 1=Energised) Opto 14 Input State (0=Off, 1=Energised) Opto 15 Input State (0=Off, 1=Energised) Opto 16 Input State (0=Off, 1=Energised) Opto 17 Input State (0=Off, 1=Energised) Opto 18 Input State (0=Off, 1=Energised) Opto 19 Input State (0=Off, 1=Energised) Opto 20 Input State (0=Off, 1=Energised) Opto 21 Input State (0=Off, 1=Energised) Opto 22 Input State (0=Off, 1=Energised) Opto 23 Input State (0=Off, 1=Energised) Opto 24 Input State (0=Off, 1=Energised) Opto 25 Input State (0=Off, 1=Energised) Opto 26 Input State (0=Off, 1=Energised) Opto 27 Input State (0=Off, 1=Energised) Opto 28 Input State (0=Off, 1=Energised) Opto 29 Input State (0=Off, 1=Energised) Opto 30 Input State (0=Off, 1=Energised) Opto 31 Input State (0=Off, 1=Energised) Opto 32 Input State (0=Off, 1=Energised) *[Binary Flag (16 bits) Indexed String]*
This cell displays the status of the available opto-inputs.				
Relay O/P Status	0F	02		Relay 1 (0=Not Operated, 1=Operated) Relay 2 (0=Not Operated, 1=Operated) Relay 3 (0=Not Operated, 1=Operated) Relay 4 (0=Not Operated, 1=Operated) Relay 5 (0=Not Operated, 1=Operated) Relay 6 (0=Not Operated, 1=Operated) Relay 7 (0=Not Operated, 1=Operated) Relay 8 (0=Not Operated, 1=Operated) Relay 9 (0=Not Operated, 1=Operated) Relay 10 (0=Not Operated, 1=Operated) Relay 11 (0=Not Operated, 1=Operated) Relay 12 (0=Not Operated, 1=Operated) Relay 13 (0=Not Operated, 1=Operated) Relay 14 (0=Not Operated, 1=Operated) Relay 15 (0=Not Operated, 1=Operated) Relay 16 (0=Not Operated, 1=Operated) Relay 17 (0=Not Operated, 1=Operated) Relay 18 (0=Not Operated, 1=Operated) Relay 19 (0=Not Operated, 1=Operated) Relay 20 (0=Not Operated, 1=Operated) Relay 21 (0=Not Operated, 1=Operated) Relay 22 (0=Not Operated, 1=Operated) Relay 23 (0=Not Operated, 1=Operated) Relay 24 (0=Not Operated, 1=Operated) Relay 25 (0=Not Operated, 1=Operated) Relay 26 (0=Not Operated, 1=Operated) Relay 27 (0=Not Operated, 1=Operated) Relay 28 (0=Not Operated, 1=Operated) Relay 29 (0=Not Operated, 1=Operated) Relay 30 (0=Not Operated, 1=Operated) Relay 31 (0=Not Operated, 1=Operated) Relay 32 (0=Not Operated, 1=Operated) *[Binary Flag (32 bits) Indexed String]*
This cell displays the status of the available output relays. Warning; When in Test Mode, this cell cannot be used to confirm operation of the output relays, therefore it will be necessary to monitor the state of each contact in turn.				
Test Port Status	0F	03		Test Port Status *[Binary Flag (8 bits) Indexed String]*
This cell displays the logic state of the DDB signals that have been allocated in the 'Monitor Bit' cells.				
Monitor Bit 1	0F	05	640	From 0 to 2047 in steps of 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Unsigned Integer (16 bits)]
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 2	0F	06	642	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 3	0F	07	644	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 4	0F	08	646	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 5	0F	09	648	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 6	0F	0A	650	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 7	0F	0B	652	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Monitor Bit 8	0F	0C	654	From 0 to 2047 in steps of 1 *[Unsigned Integer (16 bits)]*
The 'Monitor Bit' cells allow the user to select which DDB signals can be observed in the 'Test Port Status' cell.				
Test Mode	0F	0D	Disabled	Disabled Test Mode Contacts Blocked *[Indexed String]*
This cell is used to allow secondary injection testing to be performed on the IED without operation of the trip contacts. It also enables a facility to directly test the output contacts by applying menu controlled test signals				
Test Pattern	0F	0E	0x0	Relay 1 (0=Not Operated, 1=Operated) Relay 2 (0=Not Operated, 1=Operated) Relay 3 (0=Not Operated, 1=Operated) Relay 4 (0=Not Operated, 1=Operated) Relay 5 (0=Not Operated, 1=Operated) Relay 6 (0=Not Operated, 1=Operated) Relay 7 (0=Not Operated, 1=Operated) Relay 8 (0=Not Operated, 1=Operated) Relay 9 (0=Not Operated, 1=Operated) Relay 10 (0=Not Operated, 1=Operated) Relay 11 (0=Not Operated, 1=Operated) Relay 12 (0=Not Operated, 1=Operated) Relay 13 (0=Not Operated, 1=Operated) Relay 14 (0=Not Operated, 1=Operated) Relay 15 (0=Not Operated, 1=Operated) Relay 16 (0=Not Operated, 1=Operated) Relay 17 (0=Not Operated, 1=Operated) Relay 18 (0=Not Operated, 1=Operated) Relay 19 (0=Not Operated, 1=Operated) Relay 20 (0=Not Operated, 1=Operated) Relay 21 (0=Not Operated, 1=Operated) Relay 22 (0=Not Operated, 1=Operated) Relay 23 (0=Not Operated, 1=Operated) Relay 24 (0=Not Operated, 1=Operated) Relay 25 (0=Not Operated, 1=Operated) Relay 26 (0=Not Operated, 1=Operated) Relay 27 (0=Not Operated, 1=Operated) Relay 28 (0=Not Operated, 1=Operated) Relay 29 (0=Not Operated, 1=Operated) Relay 30 (0=Not Operated, 1=Operated) Relay 31 (0=Not Operated, 1=Operated) Relay 32 (0=Not Operated, 1=Operated)

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Binary Flag (32 bits)]
This cell is used to select the output relay contacts that will be tested when the 'Contact Test' cell is set to 'Apply Test'.				
Contact Test	0F	0F	No Operation	No Operation Apply Test Remove Test *[Indexed String]*
This command changes the state of the output relay contacts in the Test Pattern cell. After the test has been applied the command text on the LCD changes to 'No Operation' and the contacts will remain in the Test State until reset.				
Test LEDs	0F	10	No Operation	No Operation Apply Test *[Indexed String]*
This command illuminates the user-programmable LEDs for approximately 2 seconds, before they extinguish and the command text on the LCD reverts to 'No Operation'.				
Test Autoreclose	0F	11	No Operation	No Operation 3 Pole Test *[Indexed String]*
This command simulates tripping in order to test Autoreclose cycle.				
Red LED Status	0F	15		Red LED Status *[Binary Flag(18)]*
This cell indicates which of the user-programmable red LEDs are illuminated.				
Green LED Status	0F	16		Green LED Status *[Binary Flag(18)]*
This cell indicates which of the user-programmable green LEDs are illuminated.				
IED Mod/Beh	0F	1E	On	On On-blocked Test Test-blocked Off *[Indexed String]*
Indicates the current Mod/Beh status of whole IED				
Subscriber Sim	0F	1F	Disabled	Disabled Enabled *[Indexed String]*
Used to enable/disable the 'subscriber simulation' feature, for Sampled Values and GOOSE subscriptions				
DDB 31 - 0	0F	20		DDB 31 - 0 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 63 - 32	0F	21		DDB 63 - 32 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 95 - 64	0F	22		DDB 95 - 64 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 127 - 96	0F	23		DDB 127 - 96 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 159 - 128	0F	24		DDB 159 - 128 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 191 - 160	0F	25		DDB 191 - 160 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 223 - 192	0F	26		DDB 223 - 192 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 255 - 224	0F	27		DDB 255 - 224 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 287 - 256	0F	28		DDB 287 - 256 *[Binary Flag(32)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell displays the logic state of the DDB signals				
DDB 319 - 288	0F	29		DDB 319 - 288 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 351 - 320	0F	2A		DDB 351 - 320 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 383 - 352	0F	2B		DDB 383 - 352 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 415 - 384	0F	2C		DDB 415 - 384 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 447 - 416	0F	2D		DDB 447 - 416 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 479 - 448	0F	2E		DDB 479 - 448 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 511 - 480	0F	2F		DDB 511 - 480 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 543 - 512	0F	30		DDB 543 - 512 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 575 - 544	0F	31		DDB 575 - 544 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 607 - 576	0F	32		DDB 607 - 576 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 639 - 608	0F	33		DDB 639 - 608 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 671 - 640	0F	34		DDB 671 - 640 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 703 - 672	0F	35		DDB 703 - 672 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 735 - 704	0F	36		DDB 735 - 704 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 767 - 736	0F	37		DDB 767 - 736 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 799 - 768	0F	38		DDB 799 - 768 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 831 - 800	0F	39		DDB 831 - 800 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 863 - 832	0F	3A		DDB 863 - 832 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 895 - 864	0F	3B		DDB 895 - 864 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 927 - 896	0F	3C		DDB 927 - 896

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Binary Flag(32)]
This cell displays the logic state of the DDB signals				
DDB 959 - 928	0F	3D		DDB 959 - 928 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 991 - 960	0F	3E		DDB 991 - 960 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1023 - 992	0F	3F		DDB 1023 - 992 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1055 - 1024	0F	40		DDB 1055 - 1024 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1087 - 1056	0F	41		DDB 1087 - 1056 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1119 - 1088	0F	42		DDB 1119 - 1088 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1151 - 1120	0F	43		DDB 1151 - 1120 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1183 - 1152	0F	44		DDB 1183 - 1152 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1215 - 1184	0F	45		DDB 1215 - 1184 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1247 - 1216	0F	46		DDB 1247 - 1216 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1279 - 1248	0F	47		DDB 1279 - 1248 *[Binary Flag(32)]*
This cell displays the logic state of the DDB signals				
DDB 1311 - 1280	0F	48		DDB 1311 - 1280 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1343 - 1312	0F	49		DDB 1343 - 1312 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1375 - 1344	0F	4A		DDB 1375 - 1344 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1407 - 1376	0F	4B		DDB 1407 - 1376 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1439 - 1408	0F	4C		DDB 1439 - 1408 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1471 - 1440	0F	4D		DDB 1471 - 1440 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1503 - 1472	0F	4E		DDB 1503 - 1472 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1535 - 1504	0F	4F		DDB 1535 - 1504 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
DDB 1567 - 1536	0F	50		DDB 1567 - 1536 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1599 - 1568	0F	51		DDB 1599 - 1568 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1631 - 1600	0F	52		DDB 1631 - 1600 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1663 - 1632	0F	53		DDB 1663 - 1632 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1695 - 1664	0F	54		DDB 1695 - 1664 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1727 - 1696	0F	55		DDB 1727 - 1696 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1759- 1728	0F	56		DDB 1759- 1728 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1791- 1760	0F	57		DDB 1791- 1760 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1823 - 1792	0F	58		DDB 1823 - 1792 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1855 - 1824	0F	59		DDB 1855 - 1824 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1887 - 1856	0F	5A		DDB 1887 - 1856 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1919 - 1888	0F	5B		DDB 1919 - 1888 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1951 - 1920	0F	5C		DDB 1951 - 1920 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 1983 - 1952	0F	5D		DDB 1983 - 1952 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 2015 - 1984	0F	5E		DDB 2015 - 1984 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
DDB 2047 - 2016	0F	5F		DDB 2047 - 2016 *[Binary Flag (32 bits)]*
This cell displays the logic state of the DDB signals				
CB MONITOR SETUP	10	00		
This column contains Circuit Breaker monitoring parameters				
Broken I^	10	01	2	From 1 to 2 in steps of 0.1 *[Courier Number (decimal)]*
This setting sets the factor to be used for the cumulative broken current counter calculation. This factor is set according to the type of Circuit Breaker used.				
I^ Maintenance	10	02	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting determines whether an alarm is raised or not when the cumulative broken current maintenance counter threshold is exceeded.				
I^ Maintenance	10	03	1000	From 1 * NM1 to 25000 * NM1 in steps of 1 * NM1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (current)]
This setting determines the threshold for the cumulative broken current maintenance counter.				
I^ Lockout	10	04	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting determines whether an alarm will be raised or not when the cumulative broken current lockout counter threshold is exceeded.				
I^ Lockout	10	05	2000	From 1 * NM1 to 25000 * NM1 in steps of 1 * NM1 *[Courier Number (current)]*
This setting determines the threshold for the cumulative broken current lockout counter.				
No. CB Ops Maint	10	06	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting activates the 'number of CB operations' maintenance alarm.				
No. CB Ops Maint	10	07	10	From 1 to 10000 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the threshold for the 'Number of CB operations' alarm.				
No. CB Ops Lock	10	08	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting activates the 'number of CB operations' lockout alarm.				
No. CB Ops Lock	10	09	20	From 1 to 10000 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the threshold for the 'number of CB operations' lockout. Note: The IED can be set to lockout the Autoreclose function on reaching a second operations threshold.				
CB Time Maint	10	0A	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting activates the 'CB operate time' maintenance alarm.				
CB Time Maint	10	0B	0.1	From 0.005 to 0.5 in steps of 0.001 *[Courier Number (time-seconds)]*
This setting sets the threshold for the allowable accumulated CB interruption time before maintenance should be carried out				
CB Time Lockout	10	0C	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting activates the 'CB operate time' lockout alarm.				
CB Time Lockout	10	0D	0.2	From 0.005 to 0.5 in steps of 0.001 *[Courier Number (time-seconds)]*
This setting sets the threshold for the allowable accumulated CB interruption time before lockout.				
Fault Freq Lock	10	0E	Alarm Disabled	Alarm Disabled Alarm Enabled *[Indexed String]*
This setting enables or disables the 'excessive fault frequency' alarm.				
Fault Freq Count	10	0F	10	From 1 to 9999 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets a 'CB frequent operations' counter that monitors the number of operations over a set time period.				
Fault Freq Time	10	10	3600	From 0 to 9999 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the time period over which the CB operations are to be monitored. Should the set number of trip operations be accumulated within this time period, an alarm can be raised.				
OPTO CONFIG	11	00		
This column contains opto-input configuration settings				
Global Nominal V	11	01	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V Custom *[Indexed String]*
This setting sets the nominal DC voltage for all opto-inputs. The Custom setting allows you to set each opto-input to any voltage value individually.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Opto Input 1	11	02	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 1				
Opto Input 2	11	03	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 2				
Opto Input 3	11	04	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 3				
Opto Input 4	11	05	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 4				
Opto Input 5	11	06	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 5				
Opto Input 6	11	07	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 6				
Opto Input 7	11	08	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 7				
Opto Input 8	11	09	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 8				
Opto Input 9	11	0A	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This cell sets the nominal voltage for opto-input 9				
Opto Input 10	11	0B	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 10				
Opto Input 11	11	0C	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 11				
Opto Input 12	11	0D	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 12				
Opto Input 13	11	0E	48/54V	24/27V 30/34V 48/54V 110/125V 220/250V *[Indexed String]*
This cell sets the nominal voltage for opto-input 13				
Opto Filter Cntl	11	50	0xFFFFFFFF	Opto 1 Input State (0=Off, 1=Energised) Opto 2 Input State (0=Off, 1=Energised) Opto 3 Input State (0=Off, 1=Energised) Opto 4 Input State (0=Off, 1=Energised) Opto 5 Input State (0=Off, 1=Energised) Opto 6 Input State (0=Off, 1=Energised) Opto 7 Input State (0=Off, 1=Energised) Opto 8 Input State (0=Off, 1=Energised) Opto 9 Input State (0=Off, 1=Energised) Opto 10 Input State (0=Off, 1=Energised) Opto 11 Input State (0=Off, 1=Energised) Opto 12 Input State (0=Off, 1=Energised) Opto 13 Input State (0=Off, 1=Energised) Opto 14 Input State (0=Off, 1=Energised) Opto 15 Input State (0=Off, 1=Energised) Opto 16 Input State (0=Off, 1=Energised) Opto 17 Input State (0=Off, 1=Energised) Opto 18 Input State (0=Off, 1=Energised) Opto 19 Input State (0=Off, 1=Energised) Opto 20 Input State (0=Off, 1=Energised) Opto 21 Input State (0=Off, 1=Energised) Opto 22 Input State (0=Off, 1=Energised) Opto 23 Input State (0=Off, 1=Energised) Opto 24 Input State (0=Off, 1=Energised) Opto 25 Input State (0=Off, 1=Energised) Opto 26 Input State (0=Off, 1=Energised) Opto 27 Input State (0=Off, 1=Energised) Opto 28 Input State (0=Off, 1=Energised) Opto 29 Input State (0=Off, 1=Energised) Opto 30 Input State (0=Off, 1=Energised) Opto 31 Input State (0=Off, 1=Energised) Opto 32 Input State (0=Off, 1=Energised)

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Binary Flag (32 bits) Indexed String]
This setting determines whether the in-built noise filter is off or on for each opto-input.				
Characteristic	11	80	Standard 60%-80%	Standard 60%-80% 50% - 70% 58% - 75% *[Indexed String]*
This setting selects the opto-inputs' pick-up and drop-off characteristics.				
Opto 1 Mode	11	88	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option G and J only.				
Opto 2 Mode	11	89	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option G and J only.				
Opto 4 Mode	11	8B	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option F only.				
Opto 5 Mode	11	8C	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option F only.				
Opto 6 Mode	11	8D	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option F only.				
Opto 9 Mode	11	90	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option C and H only.				
Opto 10 Mode	11	91	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option C and H only.				
Opto 11 Mode	11	92	Normal	Normal TCS *[Indexed String]*
This setting selects the opto-input's mode of operation; either normal opto or Trip Circuit Supervision (TCS). Valid for I/O option C only.				
CONTROL INPUTS	12	00		
This column contains settings for the type of control input				
Ctrl I/P Status 1	12	01	0x00000000	Control Input 1 (0 = Reset, 1 = Set) Control Input 2 (0 = Reset, 1 = Set) Control Input 3 (0 = Reset, 1 = Set) Control Input 4 (0 = Reset, 1 = Set) Control Input 5 (0 = Reset, 1 = Set) Control Input 6 (0 = Reset, 1 = Set) Control Input 7 (0 = Reset, 1 = Set) Control Input 8 (0 = Reset, 1 = Set) Control Input 9 (0 = Reset, 1 = Set) Control Input 10 (0 = Reset, 1 = Set) Control Input 11 (0 = Reset, 1 = Set) Control Input 12 (0 = Reset, 1 = Set) Control Input 13 (0 = Reset, 1 = Set) Control Input 14 (0 = Reset, 1 = Set) Control Input 15 (0 = Reset, 1 = Set) Control Input 16 (0 = Reset, 1 = Set) Control Input 17 (0 = Reset, 1 = Set) Control Input 18 (0 = Reset, 1 = Set) Control Input 19 (0 = Reset, 1 = Set) Control Input 20 (0 = Reset, 1 = Set)

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Control Input 21 (0 = Reset, 1 = Set) Control Input 22 (0 = Reset, 1 = Set) Control Input 23 (0 = Reset, 1 = Set) Control Input 24 (0 = Reset, 1 = Set) Control Input 25 (0 = Reset, 1 = Set) Control Input 26 (0 = Reset, 1 = Set) Control Input 27 (0 = Reset, 1 = Set) Control Input 28 (0 = Reset, 1 = Set) Control Input 29 (0 = Reset, 1 = Set) Control Input 30 (0 = Reset, 1 = Set) Control Input 31 (0 = Reset, 1 = Set) Control Input 32 (0 = Reset, 1 = Set) *[Binary Flag (32 bits) Indexed String]*
This cell sets or resets the first batch of 32 Control Inputs by scrolling and changing the status of selected bits. Alternatively, each of the 32 Control inputs can be set and reset using the individual Control Input cells.				
Ctrl I/P Status 2	12	02	0x00000000	Control Input 33 (0 = Reset, 1 = Set) Control Input 34 (0 = Reset, 1 = Set) Control Input 35 (0 = Reset, 1 = Set) Control Input 36 (0 = Reset, 1 = Set) Control Input 37 (0 = Reset, 1 = Set) Control Input 38 (0 = Reset, 1 = Set) Control Input 39 (0 = Reset, 1 = Set) Control Input 40 (0 = Reset, 1 = Set) Control Input 41 (0 = Reset, 1 = Set) Control Input 42 (0 = Reset, 1 = Set) Control Input 43 (0 = Reset, 1 = Set) Control Input 44 (0 = Reset, 1 = Set) Control Input 45 (0 = Reset, 1 = Set) Control Input 46 (0 = Reset, 1 = Set) Control Input 47 (0 = Reset, 1 = Set) Control Input 48 (0 = Reset, 1 = Set) Control Input 49 (0 = Reset, 1 = Set) Control Input 50 (0 = Reset, 1 = Set) Control Input 51 (0 = Reset, 1 = Set) Control Input 52 (0 = Reset, 1 = Set) Control Input 53 (0 = Reset, 1 = Set) Control Input 54 (0 = Reset, 1 = Set) Control Input 55 (0 = Reset, 1 = Set) Control Input 56 (0 = Reset, 1 = Set) Control Input 57 (0 = Reset, 1 = Set) Control Input 58 (0 = Reset, 1 = Set) Control Input 59 (0 = Reset, 1 = Set) Control Input 60 (0 = Reset, 1 = Set) Control Input 61 (0 = Reset, 1 = Set) Control Input 62 (0 = Reset, 1 = Set) Control Input 63 (0 = Reset, 1 = Set) Control Input 64 (0 = Reset, 1 = Set) *[Binary Flag (32 bits) Indexed String]*
This cell sets or resets the second batch of 32 Control Inputs by scrolling and changing the status of selected bits. Alternatively, each of the 32 Control inputs can be set and reset using the individual Control Input cells.				
Control Input 1	12	10	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 1				
Control Input 2	12	11	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 2				
Control Input 3	12	12	No Operation	No Operation Set

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Reset *[Indexed String]*
This command sets or resets Control Input 3				
Control Input 4	12	13	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 4				
Control Input 5	12	14	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 5				
Control Input 6	12	15	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 6				
Control Input 7	12	16	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 7				
Control Input 8	12	17	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 8				
Control Input 9	12	18	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 9				
Control Input 10	12	19	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 10				
Control Input 11	12	1A	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 11				
Control Input 12	12	1B	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 12				
Control Input 13	12	1C	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 13				
Control Input 14	12	1D	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 14				
Control Input 15	12	1E	No Operation	No Operation Set Reset

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This command sets or resets Control Input 15				
Control Input 16	12	1F	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 16				
Control Input 17	12	20	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 17				
Control Input 18	12	21	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 18				
Control Input 19	12	22	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 19				
Control Input 20	12	23	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 20				
Control Input 21	12	24	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 21				
Control Input 22	12	25	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 22				
Control Input 23	12	26	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 23				
Control Input 24	12	27	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 24				
Control Input 25	12	28	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 25				
Control Input 26	12	29	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 26				
Control Input 27	12	2A	No Operation	No Operation Set Reset *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This command sets or resets Control Input 27				
Control Input 28	12	2B	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 28				
Control Input 29	12	2C	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 29				
Control Input 30	12	2D	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 30				
Control Input 31	12	2E	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 31				
Control Input 32	12	2F	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 32				
Control Input 33	12	30	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 33				
Control Input 34	12	31	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 34				
Control Input 35	12	32	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 35				
Control Input 36	12	33	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 36				
Control Input 37	12	34	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 37				
Control Input 38	12	35	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 38				
Control Input 39	12	36	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 39				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 40	12	37	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 40				
Control Input 41	12	38	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 41				
Control Input 42	12	39	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 42				
Control Input 43	12	3A	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 43				
Control Input 44	12	3B	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 44				
Control Input 45	12	3C	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 45				
Control Input 46	12	3D	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 46				
Control Input 47	12	3E	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 47				
Control Input 48	12	3F	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 48				
Control Input 49	12	40	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 49				
Control Input 50	12	41	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 50				
Control Input 51	12	42	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 51				
Control Input 52	12	43	No Operation	No Operation

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Set Reset *[Indexed String]*
This command sets or resets Control Input 52				
Control Input 53	12	44	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 53				
Control Input 54	12	45	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 54				
Control Input 55	12	46	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 55				
Control Input 56	12	47	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 56				
Control Input 57	12	48	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 57				
Control Input 58	12	49	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 58				
Control Input 59	12	4A	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 59				
Control Input 60	12	4B	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 60				
Control Input 61	12	4C	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 61				
Control Input 62	12	4D	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 62				
Control Input 63	12	4E	No Operation	No Operation Set Reset *[Indexed String]*
This command sets or resets Control Input 63				
Control Input 64	12	4F	No Operation	No Operation Set

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Reset *[Indexed String]*
This command sets or resets Control Input 64				
CTRL I/P CONFIG	13	00		
This column contains configuration settings for the control inputs.				
Hotkey Enabled 1	13	01	0xFFFFFFFF	Control Input 1 Control Input 2 Control Input 3 Control Input 4 Control Input 5 Control Input 6 Control Input 7 Control Input 8 Control Input 9 Control Input 10 Control Input 11 Control Input 12 Control Input 13 Control Input 14 Control Input 15 Control Input 16 Control Input 17 Control Input 18 Control Input 19 Control Input 20 Control Input 21 Control Input 22 Control Input 23 Control Input 24 Control Input 25 Control Input 26 Control Input 27 Control Input 28 Control Input 29 Control Input 30 Control Input 31 Control Input 32 *[Binary Flag (32 bits) Indexed String]*
This setting allows the control inputs to be individually assigned to the Hotkey menu. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the CONTROL INPUTS column.				
Hotkey Enabled 2	13	02	0xFFFFFFFF	Control Input 33 Control Input 34 Control Input 35 Control Input 36 Control Input 37 Control Input 38 Control Input 39 Control Input 40 Control Input 41 Control Input 42 Control Input 43 Control Input 44 Control Input 45 Control Input 46 Control Input 47 Control Input 48 Control Input 49 Control Input 50 Control Input 51 Control Input 52 Control Input 53 Control Input 54

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Control Input 55 Control Input 56 Control Input 57 Control Input 58 Control Input 59 Control Input 60 Control Input 61 Control Input 62 Control Input 63 Control Input 64 *[Binary Flag (32 bits) Indexed String]*
This setting allows the control inputs to be individually assigned to the Hotkey menu. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the CONTROL INPUTS column.				
Control Input 1	13	10	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 1	13	11	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 2	13	14	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 2	13	15	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 3	13	18	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 3	13	19	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 4	13	1C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 4	13	1D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 5	13	20	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 5	13	21	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 6	13	24	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 6	13	25	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 7	13	28	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 7	13	29	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 8	13	2C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 8	13	2D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 9	13	30	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 9	13	31	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 10	13	34	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 10	13	35	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 11	13	38	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 11	13	39	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 12	13	3C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 12	13	3D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 13	13	40	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 13	13	41	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 14	13	44	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 14	13	45	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 15	13	48	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 15	13	49	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 16	13	4C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 16	13	4D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 17	13	50	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 17	13	51	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 18	13	54	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 18	13	55	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 19	13	58	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 19	13	59	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 20	13	5C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 20	13	5D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 21	13	60	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 21	13	61	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 22	13	64	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 22	13	65	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 23	13	68	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 23	13	69	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 24	13	6C	Latched	Latched

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 24	13	6D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 25	13	70	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 25	13	71	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 26	13	74	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 26	13	75	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 27	13	78	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 27	13	79	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 28	13	7C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 28	13	7D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 29	13	80	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 29	13	81	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 30	13	84	Latched	Latched Pulsed

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 30	13	85	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 31	13	88	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 31	13	89	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 32	13	8C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 32	13	8D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 33	13	90	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 33	13	91	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 34	13	93	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 34	13	94	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 35	13	96	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 35	13	97	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 36	13	99	Latched	Latched Pulsed *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 36	13	9A	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 37	13	9C	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 37	13	9D	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 38	13	9F	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 38	13	A0	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 39	13	A2	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 39	13	A3	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 40	13	A5	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 40	13	A6	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 41	13	A8	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 41	13	A9	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 42	13	AB	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Ctrl Command 42	13	AC	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 43	13	AE	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 43	13	AF	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 44	13	B1	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 44	13	B2	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 45	13	B4	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 45	13	B5	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 46	13	B7	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 46	13	B8	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 47	13	BA	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 47	13	BB	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 48	13	BD	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 48	13	BE	SET/RESET	ON/OFF

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 49	13	C0	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 49	13	C1	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 50	13	C3	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 50	13	C4	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 51	13	C6	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 51	13	C7	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 52	13	C9	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 52	13	CA	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 53	13	CC	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 53	13	CD	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 54	13	CF	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 54	13	D0	SET/RESET	ON/OFF SET/RESET

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 55	13	D2	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 55	13	D3	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 56	13	D5	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 56	13	D6	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 57	13	D8	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 57	13	D9	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 58	13	DB	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 58	13	DC	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 59	13	DE	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 59	13	DF	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 60	13	E1	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 60	13	E2	SET/RESET	ON/OFF SET/RESET IN/OUT

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 61	13	E4	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 61	13	E5	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 62	13	E7	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 62	13	E8	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 63	13	EA	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 63	13	EB	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
Control Input 64	13	ED	Latched	Latched Pulsed *[Indexed String]*
This setting configures the control input as either 'latched' or 'pulsed'.				
Ctrl Command 64	13	EE	SET/RESET	ON/OFF SET/RESET IN/OUT ENABLED/DISABLED *[Indexed String]*
This setting allows you to select the text to be displayed on the hotkey menu.				
FUNCTION KEYS	17	00		
This column contains the function key definitions (only available for 30TE case).				
Fn Key Status	17	01	0	Fn Key Status *[Binary Flag (10 bits) Indexed String]*
This cell displays the status of each function key				
Fn Key 1	17	02	Unlocked	Disabled Unlocked Locked *[Indexed String]*
This setting activates function key 1. The 'Lock' setting allows a function key, which is in toggle mode, to be locked in its current active state.				
Fn Key 1 Mode	17	03	Toggled	Normal Toggled *[Indexed String]*
This setting sets the function key mode. In 'Toggle' mode, a single key press set sand latches the function key output to 'high' or 'low' in the PSL. In 'Normal' mode the function key output remains high as long as key is pressed.				
Fn Key 1 Label	17	04	Function Key 1	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting lets you change the function key text to something more suitable for the application.				
Fn Key 2	17	05	Unlocked	Disabled Unlocked Locked *[Indexed String]*
This setting activates function key 2. The 'Lock' setting allows a function key, which is in toggle mode, to be locked in its current active state.				
Fn Key 2 Mode	17	06	Normal	Normal Toggled *[Indexed String]*
This setting sets the function key mode. In 'Toggle' mode, a single key press set sand latches the function key output to 'high' or 'low' in the PSL. In 'Normal' mode the function key output remains high as long as key is pressed.				
Fn Key 2 Label	17	07	Function Key 2	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
This setting lets you change the function key text to something more suitable for the application.				
Fn Key 3	17	08	Unlocked	Disabled Unlocked Locked *[Indexed String]*
This setting activates function key 3. The 'Lock' setting allows a function key, which is in toggle mode, to be locked in its current active state.				
Fn Key 3 Mode	17	09	Normal	Normal Toggled *[Indexed String]*
This setting sets the function key mode. In 'Toggle' mode, a single key press set sand latches the function key output to 'high' or 'low' in the PSL. In 'Normal' mode the function key output remains high as long as key is pressed.				
Fn Key 3 Label	17	0A	Function Key 3	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
This setting lets you change the function key text to something more suitable for the application.				
IEC61850 CONFIG.	19	00		
This column contains settings for the IEC61850 IED Configurator				
Switch Conf.Bank	19	05	No Action	No Action Switch Banks *[Indexed String]*
This command allows you to switch between the current configuration, held in the Active Memory Bank to the configuration held in the Inactive Memory Bank.				
Restore MCL	19	0A	No Action	No Action Restore MCL *[Indexed String]*
This command lets you restore the MCL (MiCOM Control Language).				
Active Conf.Name	19	10	Not Available	Active Conf.Name *[ASCII Text]*
This cell displays the name of the configuration in the Active Memory Bank (usually taken from the SCL file).				
Active Conf.Rev	19	11	Not Available	Active Conf.Rev *[ASCII Text]*
This cell displays the configuration revision number of the configuration in the Active Memory Bank (usually taken from the SCL file).				
Inact.Conf.Name	19	20	Not Available	Inact.Conf.Name *[ASCII Text]*
This cell displays the name of the configuration in the Inactive Memory Bank (usually taken from the SCL file).				
Inact.Conf.Rev	19	21	Not Available	Inact.Conf.Rev *[ASCII Text]*
This cell displays the configuration revision number of the configuration in the Inactive Memory Bank (usually taken from the SCL file).				
IP PARAMETERS	19	30		
The data in this sub-heading relates to the IEC61850 IP parameters				
IP Address	19	31	0.0.0.0	IP Address *[ASCII Text]*
This cell displays the IED's IP address.				
Subnet mask	19	32	0.0.0.0	Subnet mask *[ASCII Text]*
This cell displays the subnet mask, which defines the subnet on which the IED is located.				
Gateway	19	33	0.0.0.0	Gateway *[ASCII Text]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell displays the gateway address of the LAN on which the IED is located.				
Media	19	34		Media Unknown RJ45 FO RJ45 Port A RJ45 Port B FO Port A FO Port B RJ45 Redundant FO Redundant *[Indexed String]*
IEC 61850 versions only. Displays the communication media of the Ethernet port that is currently in use.				
SNTP PARAMETERS	19	40		
The data and settings under this sub-heading relate to the IEC61850 SNTP parameters				
SNTP Server 1	19	41	0.0.0.0	SNTP Server 1 *[ASCII Text]*
This cell displays the IP address of the primary SNTP server.				
SNTP Server 2	19	42	0.0.0.0	SNTP Server 2 *[ASCII Text]*
This cell displays the IP address of the secondary SNTP server.				
IEC 61850 SCL	19	50		
IEC61850 versions only.				
IED Name	19	51	Not Available	IED Name *[ASCII Text]*
This setting displays the unique IED name used on the IEC 61850 network (usually taken from the SCL file).				
IEC 61850 GOOSE	19	60		
IEC61850 versions only.				
GoEna	19	70	0x00	From 0x00 to 0xFF in steps of 1 *[Binary Flag (8 bits)]*
This setting enables the GOOSE publisher settings.				
Publisher Sim	19	71	0x00000000	From 0x00 to 0xFF in steps of 1 *[Binary Flag (8 bits)]*
IEC 61850 versions only. The Publisher Sim cell allows the simulation bit to be sent in the GOOSE message, for example for testing or commissioning. When '0' is set, the simulation bit for the goose control block is not set. When '1' is set, the simulation bit for the goose control block is set. Once testing is complete the cell must be set back to '0' to restore the GOOSE scheme back to normal service. Note: The cell 'Test Mode' under IED Configurator used in software prior to IEC 61850 Edition 2 has been renamed as 'Publisher Sim'				
Ignore Test Flag	19	73	No	No Yes *[Indexed String]*
This cell allows you to ignore the test flag, if set.				
NIC MAC Address	19	82	Ethernet MAC Address	NIC MAC Address *[ASCII Text (17 chars)]*
This setting displays the MAC address of the rear Ethernet port A in case IEC61850+DNP3 comms and dual IP used				
NIC Tunl Timeout	19	83	5	No Yes *[Indexed String]*
This setting sets the maximum waiting time before an inactive tunnel to the application software is reset.				
DNP SETTINGS	1B	00		
This column contains settings for the DNP Configurator				
Dest Address	1B	01	1	From 0 to 255 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 versions only.Address of Master Device to send the unsolicited response to				
Unso Mode	1B	02	0	ON OFF *[Indexed String]*
This setting is for DNP3.0 versions only.When unsolicited response is configure off, the device shall never send an unsolicited response, but otherwise responds to master requests				
Unso Retry	1B	03	3	From 0 to 5 in steps of 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Unsigned Integer (16 bits)]
This setting is for DNP3.0 versions only. The setting is the number of retries that an outstation transmits in each unsolicited response series if it does not receive confirmation back from the master.				
Unso Response	1B	04	2	From 1 to 30 in steps of 1 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. The setting is the amount of time that the outstation shall wait for an Application Layer confirmation back from the master.				
Unso Offline Time	1B	05	30	From 1 to 60 in steps of 1 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. If an unsolicited response has been retried (Number of Unsolicited retries) without a confirmation then this parameter defines the time interval between unsolicited retries from that point forward				
Unso Class1 Event	1B	06	5	From 1 to 100 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 versions only. The unsolicited message will send if the class 1 event number is larger than this parameter.				
Unso Class1 Delay	1B	07	3	From 0.1 to 5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. The unsolicited message of class 1 events will send after the delay time.				
Unso Class2 Event	1B	08	5	From 1 to 100 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 versions only. The unsolicited message will send if the class 2 event number is larger than this parameter.				
Unso Class2 Delay	1B	09	3	From 0.1 to 5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. The unsolicited message of class 2 events will send after the delay time.				
Unso Class3 Event	1B	0A	5	From 1 to 100 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 versions only. The unsolicited message will send if the class 3 event number is larger than this parameter.				
Unso Class3 Delay	1B	0B	3	From 0.1 to 5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. The unsolicited message of class 3 events will send after the delay time.				
Backoff Max Time	1B	0C	0.5	From 0 to 0.5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. The setting sets the maximum back off time				
Backoff Min Time	1B	0D	0	From 0 to 0.5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 versions only. The setting sets the minimum back off time				
Dest Address	1B	21	1	From 0 to 255 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 over Ethernet versions only.Address of Master Device to send the unsolicited response to				
Unso Mode	1B	22	0	ON OFF *[Indexed String]*
This setting is for DNP3.0 over Ethernet versions only.When unsolicited response is configure off, the device shall never send an unsolicited response, but otherwise responds to master requests				
Unso Retry	1B	23	3	From 0 to 5 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 over Ethernet versions only. The setting is the number of retries that an outstation transmits in each unsolicited response series if it does not receive confirmation back from the master.				
Unso Response	1B	24	2	From 1 to 30 in steps of 1 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 over Ethernet versions only. The setting is the amount of time that the outstation shall wait for an Application Layer confirmation back from the master.				
Unso Offline Time	1B	25	30	From 1 to 60 in steps of 1 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 over Ethernet versions only. If an unsolicited response has been retried (Number of Unsolicited retries) without a confirmation then this parameter defines the time interval between unsolicited retries from that point forward				
Unso Class1 Event	1B	26	5	From 1 to 100 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 over Ethernet versions only. The unsolicited message will send if the class 1 event number is larger than this parameter.				
Unso Class1 Delay	1B	27	3	From 0.1 to 5 in steps of 0.01

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (time-seconds)]
This setting is for DNP3.0 over Ethernet versions only. The unsolicited message of class 1 events will send after the delay time.				
Unso Class2 Event	1B	28	5	From 1 to 100 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 over Ethernet versions only. The unsolicited message will send if the class 2 event number is larger than this parameter.				
Unso Class2 Delay	1B	29	3	From 0.1 to 5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 over Ethernet versions only. The unsolicited message of class 2 events will send after the delay time.				
Unso Class3 Event	1B	2A	5	From 1 to 100 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting is for DNP3.0 over Ethernet versions only. The unsolicited message will send if the class 3 event number is larger than this parameter.				
Unso Class3 Delay	1B	2B	3	From 0.1 to 5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 over Ethernet versions only. The unsolicited message of class 3 events will send after the delay time.				
Backoff Max Time	1B	2C	0.5	From 0 to 0.5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 over Ethernet versions only. The setting sets the maximum back off time				
Backoff Min Time	1B	2D	0	From 0 to 0.5 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting is for DNP3.0 over Ethernet versions only. The setting sets the minimum back off time				
IP Address	1B	A1	0.0.0.0	IP Address *[ASCII Text]*
This cell displays the IED's IP address for port B (in case IEC61850+DNP3OE comms)				
Subnet mask	1B	A2	0.0.0.0	Subnet mask *[ASCII Text]*
This cell displays the subnet mask, which defines the subnet on which the IED is located.				
DNP MAC Address	1B	A3	Ethernet MAC Address	DNP MAC Address *[ASCII Text (17 chars)]*
This setting displays the MAC address of the rear Ethernet port A in case IEC61850+DNP3 comms and dual IP used				
Gateway	1B	A4	0.0.0.0	Gateway *[ASCII Text]*
This cell displays the gateway address of the LAN on which the IED is located.				
DNP Time Synch	1B	A5	Disabled	Disabled Enabled *[Indexed String]*
If set to 'Enabled' the DNP3.0 master station can be used to synchronise the IED's time clock. If set to 'Disabled' either the internal free running clock, or IRIG-B input are used. DNP 3.0 over Ethernet versions only.				
Meas Scaling	1B	A6	Primary	Normalised Primary Secondary *[Indexed String]*
This setting determines the scaling type of analogue quantities - in terms of primary, secondary or normalised, for DNP3 models.				
Media	1B	A9		Media Unknown RJ45 FO RJ45 Port A RJ45 Port B FO Port A FO Port B RJ45 Redundant FO Redundant *[Indexed String]*
IEC 61850 versions only. Displays the communication media of the Ethernet port that is currently in use.				
DNP Need Time	1B	B1	10	From 1 to 30 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the duration of time waited before requesting another time sync from the master. DNP 3.0 versions only.				
DNP App Fragment	1B	B2	2048	From 100 to 2048 in steps of 1 *[Unsigned Integer (16 bits)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the maximum message length (application fragment size) transmitted by the IED for DNP 3.0 versions.				
DNP App Timeout	1B	B3	2	From 1 to 120 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time between sending a message fragment and receiving confirmation from the master. DNP 3.0 versions only.				
DNP SBO Timeout	1B	B4	10	From 1 to 10 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the maximum waiting time between receiving a select command and awaiting an operate confirmation from the master. DNP 3.0 versions only.				
Class 0 Poll	1B	B5	0	Running Counters Frozen Counters *[Indexed String]*
This setting is for DNP3.0 versions only. In response to a Class 0 poll, an outstation device shall report either the count value or the frozen count value.				
SWITCH CONTROL	22	00		
This column controls the user switch operation configuration				
SWITCH 1	22	01		SWITCH 1 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH1 Type	22	02	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI1 Status Inpt	22	03	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI1 Control by	22	04	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI1 Trip/Close	22	05	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI1 Trp Puls T	22	06	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI1 Cls Puls T	22	07	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI1 Trp Alrm T	22	08	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI1 Cls Alrm T	22	09	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI1 Sta Alrm T	22	0A	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI1 Operations	22	0B		SWI1 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI1 Data	22	0C	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SWITCH 2	22	0D		SWITCH 2 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH2 Type	22	0E	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI2 Status Inpt	22	0F	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI2 Control by	22	10	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI2 Trip/Close	22	11	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI2 Trp Puls T	22	12	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI2 Cls Puls T	22	13	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI2 Trp Alrm T	22	14	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI2 Cls Alrm T	22	15	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI2 Sta Alrm T	22	16	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI2 Operations	22	17		SWI2 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI2 Data	22	18	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
SWITCH 3	22	19		SWITCH 3 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH3 Type	22	1A	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI3 Status Inpt	22	1B	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI3 Control by	22	1C	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI3 Trip/Close	22	1D	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI3 Trp Puls T	22	1E	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI3 Cls Puls T	22	1F	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI3 Trp Alrm T	22	20	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI3 Cls Alrm T	22	21	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI3 Sta Alrm T	22	22	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI3 Operations	22	23		SWI3 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI3 Data	22	24	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SWITCH 4	22	25		SWITCH 4 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH4 Type	22	26	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Switch type				
SWI4 Status Inpt	22	27	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI4 Control by	22	28	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI4 Trip/Close	22	29	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI4 Trp Puls T	22	2A	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI4 Cls Puls T	22	2B	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI4 Trp Alrm T	22	2C	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI4 Cls Alrm T	22	2D	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI4 Sta Alrm T	22	2E	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI4 Operations	22	2F		SWI4 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI4 Data	22	30	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SWITCH 5	22	31		SWITCH 5 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH5 Type	22	32	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI5 Status Inpt	22	33	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
SWI5 Control by	22	34	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI5 Trip/Close	22	35	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI5 Trp Puls T	22	36	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI5 Cls Puls T	22	37	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI5 Trp Alrm T	22	38	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI5 Cls Alrm T	22	39	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI5 Sta Alrm T	22	3A	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI5 Operations	22	3B		SWI5 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI5 Data	22	3C	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SWITCH 6	22	3D		SWITCH 6 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH6 Type	22	3E	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI6 Status Inpt	22	3F	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI6 Control by	22	40	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI6 Trip/Close	22	41	No Operation	No Operation Trip Close

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
Supports trip and close commands if enabled in the user switch Control menu.				
SWI6 Trp Puls T	22	42	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI6 Cls Puls T	22	43	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI6 Trp Alrm T	22	44	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI6 Cls Alrm T	22	45	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI6 Sta Alrm T	22	46	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI6 Operations	22	47		SWI6 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI6 Data	22	48	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SWITCH 7	22	49		SWITCH 7 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH7 Type	22	4A	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI7 Status Inpt	22	4B	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI7 Control by	22	4C	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI7 Trip/Close	22	4D	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI7 Trp Puls T	22	4E	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI7 Cls Puls T	22	4F	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
issued.				
SWI7 Trp Alrm T	22	50	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI7 Cls Alrm T	22	51	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a protection trip command is issued.				
SWI7 Sta Alrm T	22	52	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI7 Operations	22	53		SWI7 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI7 Data	22	54	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SWITCH 8	22	55		SWITCH 8 *[Indexed String]*
This cell indicates that setting below are for Switch 1				
SWITCH8 Type	22	56	Load Break	Load Break Disconnector Earthing SWI HiSpeed Ear SWI *[Indexed String]*
Switch type				
SWI8 Status Inpt	22	57	None	None 52A 52B Both 52A+52B *[Indexed String]*
Setting to define the type of circuit breaker contacts that will be used for the circuit breaker control logic. Form A contacts match the status of the circuit breaker primary contacts, form B are opposite to the breaker status.				
SWI8 Control by	22	58	Disabled	Disabled Local Remote Local+Remote *[Indexed String]*
This setting selects the type of switch control to be used				
SWI8 Trip/Close	22	59	No Operation	No Operation Trip Close *[Indexed String]*
Supports trip and close commands if enabled in the user switch Control menu.				
SWI8 Trp Puls T	22	5A	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the close pulse within which the userswitch should close when a close command is issued.				
SWI8 Cls Puls T	22	5B	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of the trip pulse within which the user switch should trip when a manual or protection trip command is issued.				
SWI8 Trp Alrm T	22	5C	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when a close command is issued.				
SWI8 Cls Alrm T	22	5D	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise alarm when				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
a protection trip command is issued.				
SWI8 Sta Alrm T	22	5E	0.5	From 0.1 to 60 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the duration of wait timer before the relay raise a status alarm.				
SWI8 Operations	22	5F		SWI8 Operations *[Indexed String]*
This cell displays the number of switch Operations				
Reset SWI8 Data	22	60	No	No Yes *[Indexed String]*
This cell resets the switch condition monitoring data				
SECURITY CONFIG	25	00		
This column contains settings for the Cyber Security configuration				
User Banner	25	01	ACCESS ONLY FOR AUTHORISED USERS	From 32 to 234 in steps of 1 *[ASCII Text (32 chars)]*
With this setting, you can enter text for the NERC compliant banner.				
Attempts Limit	25	02	3	From 0 to 3 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting defines the maximum number of failed password attempts before action is taken.				
Attempts Timer	25	03	2	From 1 to 3 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting defines the time window used in which the number of failed password attempts is counted.				
Blocking Timer	25	04	5	From 1 to 30 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting defines the time duration for which the user is blocked, after exceeding the maximum attempts limit.				
Front Port	25	05	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the physical Front Port.				
Rear Port 1	25	06	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the primary physical rear port (RP1).				
Rear Port 2	25	07	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the secondary physical rear port (RP2).				
Ethernet Port	25	08	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the physical Ethernet Port				
Courier Tunnel	25	09	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the logical tunnelled Courier port				
IEC61850	25	0A	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the logical IEC61850 port.				
DNP3 OE	25	0B	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the logical DNP3 over Ethernet port.				
Attempts Remain	25	11		Attempts Remain *[Unsigned Integer (16 bits)]*
This cell displays the number of password attempts remaining				
Blk Time Remain	25	12		Blk Time Remain *[Unsigned Integer (16 bits)]*
This cell displays the remaining blocking time.				
Fallbck PW level	25	20		Level 0 - Logged Out.

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Level 1 - Password required for level 2. Level 2 - Password required for level 3. Level 3 - No Password required. *[Unsigned Integer (16 bits)]*
This cell displays the password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest level password that is blank, or level 0 if no passwords are blank.				
Security Code	25	FF		Security Code *[ASCII Text]*
This cell displays the 16-character security code required when requesting a recovery password. UI only cell.				
USER ALARMS	28	00		
This column contains settings for the User Alarms				
Manual Reset	28	01	0x00000000	From 0x00000000 to 0xFFFFFFFF in steps of 1 *[Binary Flag (32 bits)]*
Set the user alarm is manual reset or self reset				
Labels	28	10	Sub-Heading	
This sub-heading contains the user alarm labels				
User Alarm 1	28	11	User Alarm 1	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 2	28	12	User Alarm 2	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 3	28	13	User Alarm 3	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 4	28	14	User Alarm 4	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 5	28	15	User Alarm 5	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 6	28	16	User Alarm 6	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 7	28	17	User Alarm 7	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 8	28	18	User Alarm 8	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 9	28	19	User Alarm 9	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 10	28	1A	User Alarm 10	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 11	28	1B	User Alarm 11	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 12	28	1C	User Alarm 12	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 13	28	1D	User Alarm 13	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 14	28	1E	User Alarm 14	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 15	28	1F	User Alarm 15	From 32 to 163 in steps of 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[ASCII Text (16 chars)]
Here you can set a text label to describe each user alarm				
User Alarm 16	28	20	User Alarm 16	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 17	28	21	User Alarm 17	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 18	28	22	User Alarm 18	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 19	28	23	User Alarm 19	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 20	28	24	User Alarm 20	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 21	28	25	User Alarm 21	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 22	28	26	User Alarm 22	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 23	28	27	User Alarm 23	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 24	28	28	User Alarm 24	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 25	28	29	User Alarm 25	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 26	28	2A	User Alarm 26	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 27	28	2B	User Alarm 27	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 28	28	2C	User Alarm 28	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 29	28	2D	User Alarm 29	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 30	28	2E	User Alarm 30	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 31	28	2F	User Alarm 31	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
User Alarm 32	28	30	User Alarm 32	From 32 to 163 in steps of 1 *[ASCII Text (16 chars)]*
Here you can set a text label to describe each user alarm				
CTRL I/P LABELS	29	00		
This column contains settings for the Control Input Labels				
Control Input 1	29	01	Control Input 1	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 2	29	02	Control Input 2	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 3	29	03	Control Input 3	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 4	29	04	Control Input 4	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 5	29	05	Control Input 5	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 6	29	06	Control Input 6	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 7	29	07	Control Input 7	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 8	29	08	Control Input 8	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 9	29	09	Control Input 9	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 10	29	0A	Control Input 10	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 11	29	0B	Control Input 11	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 12	29	0C	Control Input 12	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 13	29	0D	Control Input 13	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 14	29	0E	Control Input 14	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 15	29	0F	Control Input 15	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 16	29	10	Control Input 16	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 17	29	11	Control Input 17	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 18	29	12	Control Input 18	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 19	29	13	Control Input 19	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 20	29	14	Control Input 20	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 21	29	15	Control Input 21	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 22	29	16	Control Input 22	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 23	29	17	Control Input 23	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 24	29	18	Control Input 24	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 25	29	19	Control Input 25	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 26	29	1A	Control Input 26	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 27	29	1B	Control Input 27	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 28	29	1C	Control Input 28	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 29	29	1D	Control Input 29	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 30	29	1E	Control Input 30	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 31	29	1F	Control Input 31	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 32	29	20	Control Input 32	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 33	29	21	Control Input 1	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 34	29	22	Control Input 2	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 35	29	23	Control Input 3	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 36	29	24	Control Input 4	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 37	29	25	Control Input 5	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 38	29	26	Control Input 6	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 39	29	27	Control Input 7	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 40	29	28	Control Input 8	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 41	29	29	Control Input 9	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 42	29	2A	Control Input 10	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 43	29	2B	Control Input 11	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 44	29	2C	Control Input 12	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 45	29	2D	Control Input 13	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 46	29	2E	Control Input 14	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 47	29	2F	Control Input 15	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 48	29	30	Control Input 16	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 49	29	31	Control Input 17	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 50	29	32	Control Input 18	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 51	29	33	Control Input 19	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 52	29	34	Control Input 20	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 53	29	35	Control Input 21	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 54	29	36	Control Input 22	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 55	29	37	Control Input 23	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 56	29	38	Control Input 24	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 57	29	39	Control Input 25	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 58	29	3A	Control Input 26	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 59	29	3B	Control Input 27	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 60	29	3C	Control Input 28	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 61	29	3D	Control Input 29	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Control Input 62	29	3E	Control Input 30	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 63	29	3F	Control Input 31	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
Control Input 64	29	40	Control Input 32	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
In this cell you can enter a text label to describe the control input. This text is displayed when a control input is accessed by the hotkey menu and in the programmable scheme logic description of the control input.				
DC SUP. MONITOR	2A	00		
This column contains settings for DC Voltage Supply Supervision				
DC ZONE ONE	2A	01		
The settings under this sub-heading apply to zone 1				
Vdc1 Status	2A	02	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the DC Supply Monitoring supervision function for zone 1				
Vdc1 Lower Limit	2A	03	88	From 19 to 300 in steps of 1 *[Courier Number (voltage)]*
This setting set the lower threshold for the ZONE setting.				
Vdc1 Upper Limit	2A	04	99	From 19 to 300 in steps of 1 *[Courier Number (voltage)]*
This setting sets the upper threshold for the ZONE setting.				
Vdc1 Time Delay	2A	05	0.4	From 0 to 7200 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting sets the pickup/drop-off for the trip signal of the ZONE Supply Monitoring.				
DC ZONE TWO	2A	11		
The settings under this sub-heading apply to zone 2				
Vdc2 Status	2A	12	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the DC Supply Monitoring supervision function for zone 2				
Vdc2 Lower Limit	2A	13	77	From 19 to 300 in steps of 1 *[Courier Number (voltage)]*
This setting set the lower threshold for the ZONE setting.				
Vdc2 Upper Limit	2A	14	88	From 19 to 300 in steps of 1 *[Courier Number (voltage)]*
This setting sets the upper threshold for the ZONE setting.				
Vdc2 Time Delay	2A	15	0.4	From 0 to 7200 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting sets the pickup/drop-off for the trip signal of the ZONE Supply Monitoring.				
DC ZONE THREE	2A	21		
The settings under this sub-heading apply to zone 3				
Vdc3 Status	2A	22	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the DC Supply Monitoring supervision function for zone 3				
Vdc3 Lower Limit	2A	23	121	From 19 to 300 in steps of 1 *[Courier Number (voltage)]*
This setting set the lower threshold for the ZONE setting.				
Vdc3 Upper Limit	2A	24	238	From 19 to 300 in steps of 1 *[Courier Number (voltage)]*
This setting sets the upper threshold for the ZONE setting.				
Vdc3 Time Delay	2A	25	0.4	From 0 to 7200 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting sets the pickup/drop-off for the trip signal of the ZONE Supply Monitoring.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
GROUP 1: SYSTEM CONFIG	30	00		
This column contains settings for setting the phase rotation and 2nd harmonic blocking				
Phase Sequence	30	02	Standard ABC	Standard ABC Reverse ACB *[Indexed String]*
This setting sets the phase rotation to standard (ABC) or reverse (ACB). Warning: This will affect the positive and negative sequence quantities calculated by the IED as well as other functions that are dependant on phase quantities.				
2NDHARM BLOCKING	30	03		
The settings under this sub-heading relate to 2nd harmonic blocking				
2nd Harmonic	30	04	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the 2nd Harmonic blocking of the overcurrent protection.				
2ndHarm Thresh	30	05	20	From 5 to 70 in steps of 1 *[Courier Number (percentage)]*
This setting sets the lower threshold for 2nd harmonic blocking in percent. If the 2nd harmonic component exceeds this threshold, the overcurrent protection will be blocked.				
I>lift 2H	30	06	10	From 4 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the upper threshold for 2nd harmonic blocking in amps If the 2nd harmonic exceeds this threshold, there will be no blocking applied.				
Dir Char Setting	30	11	Simple	Simple Advance *[Indexed String]*
This setting make the char angle global or specific to each stage for overcurrent protections (OVERCURRENT, EARTH FAULT 1, EARTH FAULT 2, SEF PROTECTION)				
GROUP 1: WDE PROTECTION	34	00		
This column contains settings for Wattmetric Directional Earthfault				
VN Input	34	01	Measured	Measured Derived *[Indexed String]*
This cell indicates that VN Input is always measured				
WDE>1 Function	34	10	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the WDE>1 function.				
WDE>1 Act Pow	34	11	0.4	From 0.01 to 45 in steps of 0.01 *[Courier Number (power Watts)]*
This setting sets the active power pick-up threshold for WDE>1				
WDE>1 Fwd Time	34	12	400ms	From 0.1 to 3 in steps of 0.05 *[Courier Number (time-seconds)]*
This setting sets the forward fault time delay (Temporisation AVal) for WDE>1				
WDE>1 Hold Time	34	13	200ms	From 0 to 0.2 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting sets the detection maintain time delay (Temporisation Maintien Détection) for WDE>1				
WDE>1 Inhib Time	34	14	550ms	From 0 to 2 in steps of 0.025 *[Courier Number (time-seconds)]*
This setting sets the inhibition time delay (Temporisation Module d'Inhibition) for WDE>1				
WDE>2 Function	34	20	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the WDE>2 function.				
WDE>2 Res Cur	34	21	IN	IN IA IB IC *[Indexed String]*
This setting selects the channel to use for WDE>2 Ires				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
WDE>2 Act Pow	34	22	0.4W	From 0.01 to 45 in steps of 0.01 *[Courier Number (power Watts)]*
This setting sets the active power pick-up threshold for WDE>2				
WDE>2 Fwd Time	34	23	400ms	From 0.1 to 3 in steps of 0.05 *[Courier Number (time-seconds)]*
This setting sets the forward fault time delay (Temporisation AVal) for WDE>2				
WDE>2 Hold Time	34	24	200ms	From 0 to 0.2 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting sets the detection maintain time delay (Temporisation Maintien Détection) for WDE>2				
WDE>2 Inhib Time	34	25	550ms	From 0 to 2 in steps of 0.025 *[Courier Number (time-seconds)]*
This setting sets the inhibition time delay (Temporisation Module d'Inhibition) for WDE>2				
P-Q+ detect angle	34	30	87	From 0 to 90 in steps of 0.1 *[Courier Number (angle)]*
This settings sets the P-Q+ detection angle				
P-Q- detect angle	34	31	87	From 0 to 90 in steps of 0.1 *[Courier Number (angle)]*
This settings sets the P-Q- detection angle				
P-Q+ non-det angle	34	32	87	From 0 to 90 in steps of 0.1 *[Courier Number (angle)]*
This settings sets the P-Q+ non-detection angle				
P-Q- non-det angle	34	33	87	From 0 to 90 in steps of 0.1 *[Courier Number (angle)]*
This settings sets the P-Q- non-detection angle				
WDE>2 Res Cur	34	F0	IN	IN IA IB IC *[Indexed String]*
This setting is a backup of WDE>2 Ires used for RDF file. This is not visible via the user interface.				
GROUP 1: OVERCURRENT	35	00		
This column contains settings for Overcurrent				
I>1 Function	35	23	IEC S Inverse	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse UK Rectifier RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage overcurrent element.				
I>1 Direction	35	24	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the first stage overcurrent element.				
I>1 Char Angle	35	25	45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current overcurrent stage.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
I>1 Trip Angle	35	26	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current overcurrent stage.				
I>1 Current Set	35	27	1	From 0.01 to 4.00*I1 in steps of 0.01*I1 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage overcurrent element.				
I>1 Time Delay	35	29	1	From 0 to 10 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage overcurrent element.				
I>1 Time Delay	35	29	1	From 0 to 28800 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage overcurrent element for model H.				
I>1 TMS	35	2A	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I>1 Time Dial	35	2B	1	From 0.01 to 10 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I>1 Time Dial	35	2B	1	From 0.01 to 28800 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves for model H.				
I>1 k (RI)	35	2C	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
I>1 DT Adder	35	2D	0	From 0 to 10 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
I>1 DT Adder	35	2D	0	From 0 to 28800 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic for model H				
I>1 Reset Char	35	2E	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
I>1 tRESET	35	2F	0	From 0 to 10 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
I>1 tRESET	35	2F	0	From 0 to 28800 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic for model H.				
I>1 Usr Rst Char	35	30	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
I>2 Function	35	32	Disabled	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse UK Rectifier RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the second stage overcurrent element.				
I>2 Direction	35	33	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the second stage overcurrent element.				
I>2 Char Angle	35	34	45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current overcurrent stage.				
I>2 Trip Angle	35	35	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current overcurrent stage.				
I>2 Current Set	35	36	1	From 0.01*I1 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the second stage overcurrent element.				
I>2 Time Delay	35	38	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage element.				
I>2 TMS	35	39	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I>2 Time Dial	35	3A	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I>2 k (RI)	35	3B	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
I>2 DT Adder	35	3C	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
I>2 Reset Char	35	3D	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
I>2 tRESET	35	3E	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
I>2 Usr Rst Char	35	3F	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
I>3 Status	35	40	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage overcurrent element. There is no choice of curves because this stage is DT only.				
I>3 Direction	35	41	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the third stage overcurrent element.				
I>3 Char Angle	35	42	45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting defines the characteristic angle for the directional element. This setting is applicable to current overcurrent stage.				
I>3 Trip Angle	35	43	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current overcurrent stage.				
I>3 Current Set	35	44	20	From 0.01*I1 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the third stage overcurrent element.				
I>3 Time Delay	35	45	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage overcurrent element.				
I>4 Status	35	47	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage overcurrent element. There is no choice of curves because this stage is DT only.				
I>4 Direction	35	48	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the third stage overcurrent element.				
I>4 Char Angle	35	49	45	From -180 to 180 in steps of 1 *[Available Options Description Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current overcurrent stage.				
I>4 Trip Angle	35	4A	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current overcurrent stage.				
I>4 Current Set	35	4B	20	From 0.01*I1 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the fourth stage overcurrent element.				
I>4 Time Delay	35	4C	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fourth stage overcurrent element.				
I> Blocking	35	4E	0x003F	VTS Blocks I>1 VTS Blocks I>2 VTS Blocks I>3 VTS Blocks I>4 VTS Blocks I>5 VTS Blocks I>6 AR Blocks I>3 AR Blocks I>4 AR Blocks I>6 2H Blocks I>1 2H Blocks I>2 2H Blocks I>3 2H Blocks I>4 2H Blocks I>5 2H Blocks I>6 2H 1PH Block *[Binary Flag (16 bits)]*
This setting cell contains a binary string where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with Autoreclose, VTS and second harmonic blocking				
I> Blocking	35	4E	0x003F	VTS Blocks I>1 VTS Blocks I>2 VTS Blocks I>3 VTS Blocks I>4 VTS Blocks I>5 VTS Blocks I>6 2H Blocks I>1 2H Blocks I>2 2H Blocks I>3 2H Blocks I>4

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				2H Blocks I>5 2H Blocks I>6 2H 1PH Block *[Binary Flag (16 bits)]*
This setting cell contains a binary string where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with VTS and second harmonic blocking.				
I> Char Angle	35	4F	45	From -95 to 95 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to all overcurrent stages.				
I> Blocking 2	35	50	0x0	Blinder Blk I>1 Blinder Blk I>2 Blinder Blk I>5 *[Binary Flag (4 bits)]*
This setting cell contains a binary string (data type G406), where you can define which Load Blinder blocking signals block which stage.				
I>5 Function	35	63	Disabled	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse UK Rectifier RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the fifth stage overcurrent element.				
I>5 Direction	35	64	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the fifth stage overcurrent element.				
I>5 Char Angle	35	65	45	From -180 to -180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current overcurrent stage.				
I>5 Trip Angle	35	66	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current overcurrent stage.				
I>5 Current Set	35	67	1	From 0.01*I1 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the fifth stage overcurrent element.				
I>5 Time Delay	35	69	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fifth stage overcurrent element.				
I>5 TMS	35	6A	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I>5 Time Dial	35	6B	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I>5 k (RI)	35	6C	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
I>5 DT Adder	35	6D	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
I>5 Reset Char	35	6E	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
I>5 tRESET	35	6F	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
I>5 Usr Rst Char	35	70	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
I>6 Status	35	71	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the sixth stage overcurrent element. There is no choice of curves because this stage is DT only.				
I>6 Direction	35	72	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the sixth stage overcurrent element.				
I>6 Char Angle	35	73	45	From -180 to -180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current overcurrent stage.				
I>6 Trip Angle	35	74	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current overcurrent stage.				
I>6 Current Set	35	75	20	From 0.01*I1 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the sixth stage overcurrent element.				
I>6 Time Delay	35	76	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the sixth stage overcurrent element.				
V DEPENDANT O/C	35	81		
The settings under this sub-heading relate to				
V Dep OC Status	35	82	Disabled	Disabled VCO I>1 VCO I>2 VCO I>1 & I>2 VCO I>5 VCO I>1&I>2&I>5 VCO I>1 & I>5 VCO I>2 & I>5 VRO I>1 VRO I>2 VRO I>5 VRO I>1 & I>2 VRO I>1 & I>5 VRO I>2 & I>5 VRO I>1&I>2&I>5 *[Indexed String]*
This setting cell contains a binary string (data type G100), where you can define which stages are influenced by the Voltage Controlled Overcurrent (VCO) and Voltage Restrained Overcurrent (VRO) functions. Note: Some models do not provide VRO.				
V Dep OC Status	35	82	Disabled	Disabled VCO I>1 VCO I>2 VCO I>1 & I>2 VCO I>5

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				VCO I>1&I>2&I>5 VCO I>1 & I>5 VCO I>2 & I>5 *[Indexed String]*
Allows selection of whether voltage control should be applied to each of the first or second stage overcurrent elements.				
V Dep OC V<1 Set	35	83	80	From 10 to 120 in steps of 1 *[Courier Number (voltage)]*
This setting sets the voltage V1 threshold at which the current setting of the overcurrent stages becomes reduced. This is on a per phase basis.				
V Dep OC k Set	35	84	0.25	From 0.1 to 1 in steps of 0.05 *[Courier Number (decimal)]*
This setting determines the Overcurrent multiplier factor used to reduce the pick-up overcurrent setting.				
V Dep OC V<2 Set	35	85	60	From 10 to 120 in steps of 1 *[Courier Number (voltage)]*
This setting sets the voltage V2 threshold at which the current setting of the overcurrent stages becomes reduced. This is on a per phase basis.				
LOAD BLINDER	35	90		
The settings under this sub-heading relate to the Load Blinder function				
Blinder Status	35	91	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Load Blinder blocking function.				
Blinder Status	35	91	Disabled	Disabled *[Indexed String]*
This setting disables the Load Blinder blocking function for models B and G				
Blinder Function	35	92	3Ph(based on Z1)	3Ph(based on Z1) 1Ph(based on Z) *[Indexed String]*
This setting sets the Load Blinder to three-phase or single-phase blocking.				
Blinder Mode	35	93	Both	Reverse Forward Both *[Indexed String]*
This setting sets the Load Blinder direction measurement.				
FWD Z Impedance	35	94	15	From 0.1 to 500 in steps of 0.01 *[Courier Number (impedance)]*
This setting sets the Forward Impedance (in ohms) for the Load Blinder function.				
FWD Z Angle	35	95	30	From 5 to 85 in steps of 1 *[Courier Number (angle)]*
This setting sets the Forward Angle (in degrees) for the Load Blinder function.				
REV Z Impedance	35	97	15	From 0.1 to 500 in steps of 0.01 *[Courier Number (impedance)]*
This setting sets the Reverse Impedance (in ohms) for the Load Blinder function.				
REV Z Angle	35	98	30	From 5 to 85 in steps of 1 *[Courier Number (angle)]*
This setting sets the Reverse Angle (in degrees) for the Load Blinder function.				
Blinder V< Block	35	9A	15	From 10 to 120 in steps of 1 *[Courier Number (voltage)]*
This setting sets the undervoltage threshold for the Load Blinder function.				
Blinder I2>Block	35	9B	0.2	From 0.08 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the Negative Phase Sequence current threshold for the Load Blinder function.				
PU Cycles	35	9C	1	From 0 to 50 in steps of 0.5 *[Courier Number]*
This setting sets the pick-up count threshold for the Load Blinder function.				
DO Cycles	35	9D	1	From 0 to 50 in steps of 0.5 *[Courier Number]*
This setting sets the drop-off count threshold for the Load Blinder function.				
GROUP 1: NEG SEQ O/C	36	00		
This column contains settings for Negative Sequence overcurrent				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
I2>1 Status	36	10	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage NPSOC element.				
I2>1 Direction	36	12	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the first stage NPSOC element.				
I2>1 Current Set	36	15	0.2	From 0.08 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage NPSOC element.				
I2>1 Time Delay	36	17	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage NPSOC element.				
I2>1 TMS	36	18	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I2>1 Time Dial	36	19	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I2>1 DT Adder	36	1B	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
I2>1 Reset Char	36	1C	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
I2>1 tRESET	36	1D	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
I2>1 Usr RstChar	36	1E	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
I2>2 Status	36	20	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage NPSOC element.				
I2>2 Direction	36	22	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the second stage NPSOC element.				
I2>2 Current Set	36	25	0.2	From 0.08 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the second stage NPSOC element.				
I2>2 Time Delay	36	27	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage NPSOC element.				
I2>2 TMS	36	28	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I2>2 Time Dial	36	29	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I2>2 DT Adder	36	2B	0	From 0 to 100 in steps of 0.01

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (time-seconds)]
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
I2>2 Reset Char	36	2C	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
I2>2 tRESET	36	2D	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
I2>2 Usr RstChar	36	2E	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
I2>3 Status	36	30	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage NPSOC element. There is no choice of curves because this stage is DT only.				
I2>3 Direction	36	32	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the third stage NPSOC element.				
I2>3 Current Set	36	35	0.2	From 0.08 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the third stage NPSOC element.				
I2>3 Time Delay	36	37	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage NPSOC element.				
I2>4 Status	36	40	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage NPSOC element. There is no choice of curves because this stage is DT only.				
I2>4 Direction	36	42	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the fourth stage NPSOC element.				
I2>4 Current Set	36	45	0.2	From 0.08 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the fourth stage NPSOC element.				
I2>4 Time Delay	36	47	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fourth stage NPSOC element.				
I2> Blocking	36	50	0x0F	VTS Blocks I2>1 VTS Blocks I2>2 VTS Blocks I2>3 VTS Blocks I2>4 2H Blocks I2>1 2H Blocks I2>2 2H Blocks I2>3 2H Blocks I2>4 *[Binary Flag (8 bits)]*
This setting cell contains a binary string (data type G158), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with VTS blocking and second harmonic blocking.				
I2> Char Angle	36	51	-60	From -95 to 95 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to all NPSOC stages.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
I2> V2pol Set	36	52	5	From 0.5 to 25 in steps of 0.5 *[Courier Number (voltage)]*
This setting determines the minimum negative sequence voltage threshold that must be present to determine directionality.				
GROUP 1: BROKEN CONDUCTOR	37	00		
This column contains settings for Broken Conductor				
Broken Conductor	37	01	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Broken Conductor function.				
I2/I1 Setting	37	02	0.1	From 0.1 to 1 in steps of 0.01 *[Courier Number (decimal)]*
This setting determines the pick-up threshold of the negative to positive sequence current ratio.				
I2/I1 Time Delay	37	03	60	From 0 to 100 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting sets the time delay for the broken conductor element				
GROUP 1: EARTH FAULT 1	38	00		
This column contains settings for Measured Earth Fault protection (EF1)				
IN1> Input	38	01	Measured	Measured Derived *[Indexed String]*
This cell displays the input type. For EF1 it is always 'Measured'				
IN1>1 Function	38	25	IEC S Inverse	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse IDG Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 EPATR B *[Indexed String]*
This setting determines the tripping characteristic for the first stage EF1 element.				
IN1>1 Direction	38	26	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the first stage EF1 element.				
IN1>1 Current	38	29	0.2	From 0.01 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage EF1 element.				
IN1>1 Current	38	29	0.2	From 0.005 to 4 in steps of 0.001 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage EF1 element.				
IN1>1 IDG Is	38	2A	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting is set as a multiple of the Earth Fault overcurrent setting IN> for the IDG curve. It determines the actual current threshold at which the element starts.				
IN1>1 Time Delay	38	2C	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage EF1 element.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
IN1>1 TMS	38	2D	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN1>1 Time Dial	38	2E	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
IN1>1 k (RI)	38	2F	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
IN1>1 IDG Time	38	30	1.2	From 1 to 2 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time at high levels of fault current for IDG curves.				
IN1>1 DT Adder	38	31	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
IN1>1 Reset Char	38	32	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
IN1>1 tRESET	38	33	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
IN1>1 Usr RstChr	38	34	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
IN1>2 Function	38	36	Disabled	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse IDG Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 EPATR B *[Indexed String]*
This setting determines the tripping characteristic for the second stage EF1 element.				
IN1>2 Direction	38	37	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the second stage EF1 element.				
IN1>2 Current	38	3A	0.2	From 0.01 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the second stage EF1 element.				
IN1>2 Current	38	3A	0.2	From 0.005 to 4 in steps of 0.001 *[Courier Number (current)]*
This setting sets the pick-up threshold for the second stage EF1 element.				
IN1>2 IDG Is	38	3B	1.5	From 1 to 4 in steps of 0.1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (decimal)]
This setting is set as a multiple of the Earth Fault overcurrent setting IN> for the IDG curve. It determines the actual current threshold at which the element starts.				
IN1>2 Time Delay	38	3D	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage EF1 element.				
IN1>2 TMS	38	3E	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN1>2 Time Dial	38	3F	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
IN1>2 k (RI)	38	40	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
IN1>2 IDG Time	38	41	1.2	From 1 to 2 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time at high levels of fault current for IDG curves.				
IN1>2 DT Adder	38	42	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
IN1>2 Reset Char	38	43	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
IN1>2 tRESET	38	44	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
IN1>2 Usr RstChr	38	45	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
IN1>3 Status	38	46	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage EF1 element. There is no choice of curves because this stage is DT only.				
IN1>3 Direction	38	47	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the third stage EF1 element.				
IN1>3 Current	38	4A	0.2	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the third stage EF1 element.				
IN1>3 Time Delay	38	4B	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage EF1 element.				
IN1>4 Status	38	4D	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage EF1 element. There is no choice of curves because this stage is DT only.				
IN1>4 Direction	38	4E	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the fourth stage EF1 element.				
IN1>4 Trip Angle	38	50	180	From 0 to 180 in steps of 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (angle)]
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
IN1>4 Current	38	51	0.2	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the fourth stage EF1 element.				
IN1>4 Time Delay	38	52	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fourth stage EF1 element.				
IN1> Blocking	38	54	0x00F	VTS Blocks IN>1 VTS Blocks IN>2 VTS Blocks IN>3 VTS Blocks IN>4 AR Blocks IN>3 AR Blocks IN>4 2H Blocks IN>1 2H Blocks IN>2 2H Blocks IN>3 2H Blocks IN>4 *[Binary Flag (12 bits)]*
This setting cell contains a binary string (data type G63), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with Autoreclose.				
IN1> Blocking	38	54	0x00F	VTS Blocks IN>1 VTS Blocks IN>2 VTS Blocks IN>3 VTS Blocks IN>4 2H Blocks IN>1 2H Blocks IN>2 2H Blocks IN>3 2H Blocks IN>4 *[Binary Flag (12 bits)]*
This setting cell contains a binary string (data type G63A), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models without Autoreclose.				
IN1> POL	38	55		
The settings under this sub-heading relate to the polarisation for directional control for EF1 (measured)				
IN1> Char Angle	38	56	-45	From -95 to 95 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle used for the directional decision.				
IN1> Pol	38	57	Zero Sequence	Zero Sequence Neg Sequence *[Indexed String]*
This setting determines whether the directional function uses zero sequence or negative sequence voltage polarisation.				
IN1> VNpol Set	38	59	5	From 0.5 to 80 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision.				
IN1> VNpol Set	38	59	5	From 0.50 *V3 to 80.00 *V3 in steps of 0.50 *V3 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision.				
IN1> V2pol Set	38	5A	5	From 0.5 to 25 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision. Derived				
IN1> I2pol Set	38	5B	0.08	From 0.08 to 1 in steps of 0.01 *[Courier Number (current)]*
This setting sets the minimum negative sequence current polarising quantity for directional decision.				
GROUP 1: EARTH FAULT 2	39	00		
This column contains settings for Derived Earth Fault				
IN2> Input	39	01	Derived	Measured Derived *[Indexed String]*
This cell displays the input type. For EF2 it is always 'Derived'				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
IN2>1 Function	39	25	IEC S Inverse	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse IDG Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 EPATR B *[Indexed String]*
This setting determines the tripping characteristic for the first stage EF2 element.				
IN2>1 Direction	39	26	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the first stage EF2 element.				
IN2>1 Char Angle	39	27	-45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
IN2>1 Trip Angle	39	28	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
IN2>1 Current	39	29	0.2	From 0.05 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage EF2 element.				
IN2>1 IDG Is	39	2A	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting is set as a multiple of the Earth Fault overcurrent setting IN> for the IDG curve. It determines the actual current threshold at which the element starts.				
IN2>1 Time Delay	39	2C	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage EF2 element.				
IN2>1 TMS	39	2D	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN2>1 Time Dial	39	2E	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
IN2>1 k (RI)	39	2F	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
IN2>1 IDG Time	39	30	1.2	From 1 to 2 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time at high levels of fault current for IDG curves.				
IN2>1 DT Adder	39	31	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
IN2>1 Reset Char	39	32	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
IN2>1 tRESET	39	33	0	From 0 to 100 in steps of 0.01

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (time-seconds)]
This setting determines the Reset time for the Definite Time Reset characteristic				
IN2>1 Usr RstChr	39	34	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
IN2>2 Function	39	36	Disabled	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse RI IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse IDG Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 EPATR B *[Indexed String]*
This setting determines the tripping characteristic for the second stage EF2 element.				
IN2>2 Direction	39	37	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the second stage EF2 element.				
IN2>2 Char Angle	39	38	-45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
IN2>2 Trip Angle	39	39	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
IN2>2 Current	39	3A	0.2	From 0.05 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the second stage EF2 element.				
IN2>2 IDG Is	39	3B	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting is set as a multiple of the Earth Fault overcurrent setting IN> for the IDG curve. It determines the actual current threshold at which the element starts.				
IN2>2 Time Delay	39	3D	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage EF2 element.				
IN2>2 TMS	39	3E	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN2>2 Time Dial	39	3F	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
IN2>2 k (RI)	39	40	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
IN2>2 IDG Time	39	41	1.2	From 1 to 2 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the minimum operate time at high levels of fault current for IDG curves.				
IN2>2 DT Adder	39	42	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
IN2>2 Reset Char	39	43	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
IN2>2 tRESET	39	44	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
IN2>2 Usr RstChr	39	45	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
IN2>3 Status	39	46	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage EF2 element. There is no choice of curves because this stage is DT only.				
IN2>3 Direction	39	47	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the third stage EF2 element.				
IN2>3 Char Angle	39	48	-45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
IN2>3 Trip Angle	39	49	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
IN2>3 Current	39	4A	0.2	From 0.05 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the third stage EF2 element.				
IN2>3 Time Delay	39	4B	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage EF2 element.				
IN2>4 Status	39	4D	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage EF2 element. There is no choice of curves because this stage is DT only.				
IN2>4 Direction	39	4E	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the fourth stage EF2 element.				
IN2>4 Char Angle	39	4F	-45	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
IN2>4 Trip Angle	39	50	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
IN2>4 Current	39	51	0.2	From 0.05 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the pick-up threshold for the fourth stage EF2 element.				
IN2>4 Time Delay	39	52	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fourth stage EF2 element.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
IN2> Blocking	39	54	0x00F	VTS Blocks IN>1 VTS Blocks IN>2 VTS Blocks IN>3 VTS Blocks IN>4 AR Blocks IN>3 AR Blocks IN>4 2H Blocks IN>1 2H Blocks IN>2 2H Blocks IN>3 2H Blocks IN>4 *[Binary Flag (12 bits)]*
This setting cell contains a binary string (data type G63), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with Autoreclose.				
IN2> Blocking	39	54	0x00F	VTS Blocks IN>1 VTS Blocks IN>2 VTS Blocks IN>3 VTS Blocks IN>4 2H Blocks IN>1 2H Blocks IN>2 2H Blocks IN>3 2H Blocks IN>4 *[Binary Flag (12 bits)]*
This setting cell contains a binary string (data type G63A), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models without Autoreclose.				
IN2> POL	39	55		
The settings under this sub-heading relate to the polarisation for directional control for EF2 derived				
IN2> Char Angle	39	56	-45	From -95 to 95 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle used for the directional decision.				
IN2> Pol	39	57	Zero Sequence	Zero Sequence Neg Sequence *[Indexed String]*
This setting determines whether the directional function uses zero sequence or negative sequence voltage polarisation.				
IN2> VNpol Set	39	59	5	From 0.5 to 80 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision. Derived				
IN2> VNpol Set	39	59	5	From 0.50 *V3 to 80.00 *V3 in steps of 0.50 *V3 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision. Measured				
IN2> V2pol Set	39	5A	5	From 0.5 to 25 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision. Derived				
IN2> I2pol Set	39	5B	0.08	From 0.08 to 1 in steps of 0.01 *[Courier Number (current)]*
This setting sets the minimum negative sequence current polarising quantity for directional decision.				
GROUP 1: SEF PROTECTION	3A	00		
This column contains settings for Sensitive Earth Fault protection				
SEF Options	3A	01	SEF	SEF SEF cos(PHI) SEF sin(PHI) Wattmetric *[Indexed String]*
This setting selects the type of sensitive earth fault protection function.				
ISEF>1 Function	3A	2A	DT	Disabled DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse IEEE M Inverse

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse IDG EPATR B Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage SEF element.				
ISEF>1 Direction	3A	2B	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the first stage SEF element.				
ISEF>1 CharAngle	3A	2C	90	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
ISEF>1 TripAngle	3A	2D	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
ISEF>1 Current	3A	2E	0.05	From 0.001 to 0.1 in steps of 0.00025 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage SEF element.				
ISEF>1 IDG Is	3A	2F	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting is set as a multiple of ISEF> setting for the IDG curve (Scandinavian) and determines the actual IED current threshold at which the element starts.				
ISEF>1 Delay	3A	31	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage SEF element.				
ISEF>1 TMS	3A	32	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
ISEF>1 Time Dial	3A	33	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
ISEF>1 IDG Time	3A	34	1.2	From 1 to 2 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time at high levels of fault current for IDG curves.				
ISEF>1 DT Adder	3A	35	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
ISEF>1 Reset Chr	3A	36	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
ISEF>1 tRESET	3A	37	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
ISEF>1 UsrRstChr	3A	38	DT	DT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
ISEF>2 Function	3A	3A	Disabled	Disabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				DT IEC S Inverse IEC V Inverse IEC E Inverse UK LT Inverse IEEE M Inverse IEEE V Inverse IEEE E Inverse US Inverse US ST Inverse IDG EPATR B Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage SEF element.				
ISEF>2 Direction	3A	3B	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the first stage SEF element.				
ISEF>2 CharAngle	3A	3C	90	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
ISEF>2 TripAngle	3A	3D	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
ISEF>2 Current	3A	3E	0.05	From 0.001 to 0.1 in steps of 0.00025 *[Courier Number (current)]*
This setting sets the pick-up threshold for the first stage SEF element.				
ISEF>2 IDG Is	3A	3F	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting is set as a multiple of ISEF> setting for the IDG curve (Scandinavian) and determines the actual IED current threshold at which the element starts.				
ISEF>2 Delay	3A	41	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage SEF element.				
ISEF>2 TMS	3A	42	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
ISEF>2 Time Dial	3A	43	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
ISEF>2 IDG Time	3A	44	1.2	From 1 to 2 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time at high levels of fault current for IDG curves.				
ISEF>2 DT Adder	3A	45	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting adds an additional fixed time delay to the IDMT Operate characteristic.				
ISEF>2 Reset Chr	3A	46	DT	DT Inverse *[Indexed String]*
This setting determines the type of Reset characteristic used for the IEEE/US curves.				
ISEF>2 tRESET	3A	47	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
ISEF>2 UsrRstChr	3A	48	DT	DT Def User Curve 1 Def User Curve 2

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the type of Reset characteristic used for the user defined curves.				
ISEF>3 Status	3A	49	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage SEF element. There is no choice of curves because this stage is DT only.				
ISEF>3 Direction	3A	4A	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the third stage SEF element.				
ISEF>3 CharAngle	3A	4B	90	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
ISEF>3 TripAngle	3A	4C	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
ISEF>3 Current	3A	4D	0.4	From 0.001 to 2 in steps of 0.001 *[Courier Number (current)]*
This setting sets the pick-up threshold for the third stage SEF element.				
ISEF>3 Delay	3A	4E	0.5	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage SEF element.				
ISEF>4 Status	3A	50	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage SEF element. There is no choice of curves because this stage is DT only.				
ISEF>4 Direction	3A	51	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for the fourth stage SEF element.				
ISEF>4 CharAngle	3A	52	90	From -180 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle for the directional element. This setting is applicable to current stage.				
ISEF>4 TripAngle	3A	53	180	From 0 to 180 in steps of 1 *[Courier Number (angle)]*
This setting defines the opening angle of the forward or reverse trip zone for current stage.				
ISEF>4 Current	3A	54	0.6	From 0.001 to 2 in steps of 0.001 *[Courier Number (current)]*
This setting sets the pick-up threshold for the fourth stage SEF element.				
ISEF>4 Delay	3A	55	0.25	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fourth stage SEF element.				
ISEF> Blocking	3A	57	0x00F	VTS Blks ISEF>1 VTS Blks ISEF>2 VTS Blks ISEF>3 VTS Blks ISEF>4 AR Blks ISEF>3 AR Blks ISEF>4 2H Blocks ISEF>1 2H Blocks ISEF>2 2H Blocks ISEF>3 2H Blocks ISEF>4 *[Binary Flag (12 bits)]*
This setting cell contains a binary string (data type G64), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with Autoreclose.				
ISEF> Blocking	3A	57	0x00F	VTS Blks ISEF>1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				VTS Blks ISEF>2 VTS Blks ISEF>3 VTS Blks ISEF>4 2H Blocks ISEF>1 2H Blocks ISEF>2 2H Blocks ISEF>3 2H Blocks ISEF>4 *[Binary Flag (12 bits)]*
This setting cell contains a binary string (data type G64A), where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models without Autoreclose.				
ISEF POL	3A	58		
ISEF> Char Angle	3A	59	90	From -95 to 95 in steps of 1 *[Courier Number (angle)]*
This setting defines the characteristic angle used for the directional decision.				
ISEF> VNpol Set	3A	5B	5	From 0.5 to 80 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision.				
ISEF> VNpol Set	3A	5B	5	From 0.50 *V3/0.50 *V1 to 80.00 *V3/80.00 *V1 in steps of 0.50 *V3/0.50 *V1 *[Courier Number (voltage)]*
This setting sets the minimum zero sequence voltage polarising quantity required for a directional decision.				
WATTMETRIC SEF	3A	5D		
The settings under this sub-heading relate to Watt metric directional control for SEF				
PN> Setting	3A	5E	9	From 0 to 20 in steps of 0.05 *[Courier Number (power Watts)]*
This setting sets the threshold for the wattmetric component of zero sequence power.				
PN> Setting	3A	5E	9	From 0.00 *V3*I3/0.00 *V1*I3 to 20.00 *V3*I3/20.00 *V1*I3 in steps of 0.05 *V3*I3/0.05 *V1*I3 *[Courier Number (power Watts)]*
This setting sets the threshold for the wattmetric component of zero sequence power.				
GROUP 1: RESIDUAL O/V NVD	3B	00		
This column contains settings for Residual Overvoltage (Neutral Voltage Displacement)				
VN Input	3B	01	Derived	Measured Derived *[Indexed String]*
This cell indicates that VN Input is always derived from 3 phase				
VN Input	3B	01	Measured	Measured Derived *[Indexed String]*
This cell indicates that VN Input is always measured				
VN>1 Function	3B	02	DT	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage residual overvoltage element.				
VN>1 Voltage Set	3B	03	5	From 1*V1 to 80*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage.				
VN>1 Voltage Set	3B	03	5	From 1*V3/1*V1 to 80*V3/80*V1 in steps of 0.1*V3/0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage.				
VN>1 Time Delay	3B	04	5	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the operate time delay for the first stage.				
VN>1 TMS	3B	05	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This setting sets the time multiplier setting for the IDMT characteristic.				
VN>1 tReset	3B	06	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT reset time.				
VN>2 Status	3B	07	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage SEF element. There is no choice of curves because this stage is DT only.				
VN>2 Voltage Set	3B	08	10	From 1*V1 to 80*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage.				
VN>2 Voltage Set	3B	08	10	From 1*V3/1*V1 to 80*V3/80*V1 in steps of 0.1*V3/0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage.				
VN>2 Time Delay	3B	09	10	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay for the second stage.				
VN>3 Function	3B	0A	Disabled	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the third stage residual overvoltage element.				
VN>3 Voltage Set	3B	0B	5	From 1*V1 to 80*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the third stage.				
VN>3 Voltage Set	3B	0B	5	From 1*V3/1*V1 to 80*V3/80*V1 in steps of 0.1*V3/0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the third stage.				
VN>3 Time Delay	3B	0C	5	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay for the third stage.				
VN>3 TMS	3B	0D	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This setting sets the time multiplier setting for the IDMT characteristic.				
VN>3 tReset	3B	0E	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT reset time.				
VN>4 Status	3B	10	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage SEF element. There is no choice of curves because this stage is DT only.				
VN>4 Voltage Set	3B	11	10	From 1*V1 to 80*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage.				
VN>4 Voltage Set	3B	11	10	From 1*V3/1*V1 to 80*V3/80*V1 in steps of 0.1*V3/0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage.				
VN>4 Time Delay	3B	12	10	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay for the second stage.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
VN<1 Function	3B	30	DT	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage residual undervoltage element.				
VN<1 Voltage Set	3B	31	5	From 1*V1 to 150*V1 in steps of 0.5*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage.				
VN<1 Voltage Set	3B	31	5	From 1*V3/1*V1 to 150*V3/80*V1 in steps of 0.5*V3/0.5*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage.				
VN<1 Time Delay	3B	32	5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay for the first stage.				
VN<1 TMS	3B	33	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This setting sets the time multiplier setting for the IDMT characteristic.				
VN<1 tReset	3B	34	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT reset time.				
VN<2 Status	3B	40	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage SEF element. There is no choice of curves because this stage is DT only.				
VN<2 Voltage Set	3B	41	10	From 1*V1 to 150*V1 in steps of 0.5*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage.				
VN<2 Voltage Set	3B	41	10	From 1*V3/1*V1 to 150*V3/150*V1 in steps of 0.5*V3/0.5*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage.				
VN<2 Time Delay	3B	42	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay for the second stage.				
GROUP 1: THERMAL OVERLOAD	3C	00		
This column contains settings for Thermal Overload				
Characteristic	3C	01	Single	Disabled Single Dual *[Indexed String]*
This setting determines the operate characteristic for the thermal overload element.				
Thermal Trip	3C	02	1	From 0.08*I1 to 4.0*I1 in steps of 0.01*I1 *[Courier Number (current)]*
This setting sets the pick-up threshold of the thermal characteristic. This would normally be the maximum full load current.				
Thermal Alarm	3C	03	70	From 50 to 100 in steps of 1 *[Courier Number (percentage)]*
This setting sets the thermal state threshold at which an alarm will be generated. This corresponds to a percentage of the trip threshold				
Time Constant 1	3C	04	10	From 1 to 200 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the thermal time constant for a single time constant characteristic.				
Time Constant 2	3C	05	5	From 1 to 200 in steps of 1 *[Courier Number (time-minutes)]*
This setting sets the thermal time constant for a dual time constant characteristic.				
k factor	3C	06	1.05	From 1 to 1.5 in steps of 0.01

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number]
This setting sets the k factor				
GROUP 1: NEG SEQUENCE O/V	3D	00		
This column contains settings for Negative Sequence overvoltage protection (NPSOV)				
V2>1 Status	3D	01	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage for NPSOV.				
V2>1 Voltage Set	3D	02	15	From 1*V1 to 110*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage for the NPSOV protection element.				
V2>1 Time Delay	3D	03	5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time-delay for the first stage for the NPSOV protection element.				
V2>2 Status	3D	11	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage for NPSOV.				
V2>2 Voltage Set	3D	12	15	From 1*V1 to 110*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage for the NPSOV protection element.				
V2>2 Time Delay	3D	15	5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time-delay for the second stage for the NPSOV protection element.				
GROUP 1: COLD LOAD PICKUP	3E	00		
This column contains settings for Cold Load Pickup				
tcold Time Delay	3E	01	7200	From 0 to 14400 in steps of 1 *[Courier Number (time-seconds)]*
This setting determines the time the load needs to be de-energised (dead time) before the new settings are applied.				
tclp Time Delay	3E	02	7200	From 0 to 14400 in steps of 1 *[Courier Number (time-seconds)]*
This setting controls the period of time for which the relevant overcurrent and earth fault settings are altered or inhibited following circuit breaker closure.				
OVERCURRENT	3E	20		
The settings under this sub-heading relate to the Phase Overcurrent elements				
I>1 Status	3E	21	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
I>1 Current Set	3E	22	1.5	From 0.01 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting determines the new pick-up setting for the first stage Overcurrent element during the tclp time delay.				
I>1 Time Delay	3E	24	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the first stage Overcurrent element during the tclp time.				
I>1 Time Delay	3E	24	1	From 0 to 28800 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the first stage Overcurrent element during the tclp time.				
I>1 TMS	3E	25	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I>1 Time Dial	3E	26	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I>1 Time Dial	3E	26	1	From 0.01 to 28800 in steps of 0.01 *[Courier Number (decimal)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				
I>1 k (RI)	3E	27	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting sets the new time multiplier setting to adjust the operate time of the RI curve during the tclp time.				
I>2 Status	3E	29	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
I>2 Current Set	3E	2A	1.5	From 0.01 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting determines the new pick-up setting for the second stage Overcurrent element during the tclp time delay.				
I>2 Time Delay	3E	2C	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the second stage Overcurrent element during the tclp time.				
I>2 TMS	3E	2D	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This setting sets the new time multiplier setting for the second stage Overcurrent element to adjust the operate time of the IEC IDMT characteristic during the tclp time.				
I>2 Time Dial	3E	2E	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This setting sets the new time multiplier setting to adjust the operate time of the IEEE/US IDMT curves during the tclp time.				
I>2 k (RI)	3E	2F	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
I>3 Status	3E	31	Block	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
I>3 Current Set	3E	32	25	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the third stage Overcurrent element during the tclp time delay.				
I>3 Time Delay	3E	33	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the first stage Overcurrent element during the tclp time.				
I>4 Status	3E	35	Block	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
I>4 Current Set	3E	36	25	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the fourth stage Overcurrent element during the tclp time delay.				
I>4 Time Delay	3E	37	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
Setting for the new operate time delay for the fourth stage definite time element during the tclp time.				
STAGE 1 E/F 1	3E	39		
The settings under this sub-heading relate to measured Earth Fault protection (EF1)				
IN1>1 Status	3E	3A	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN1>1 Current	3E	3B	0.2	From 0.01 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the measured Earth Fault element during the tclp time delay.				
IN1>1 Current	3E	3B	0.2	From 0.005 to 4 in steps of 0.001 *[Courier Number (current)]*
This setting sets the new pick-up setting for the measured Earth Fault element during the tclp time delay.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
IN1>1 IDG Is	3E	3C	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting defines the new TMS of the IDG curve during the tclp time.				
IN1>1 Time Delay	3E	3E	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the measured Earth Fault element during the tclp time.				
IN1>1 TMS	3E	3F	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN1>1 Time Dial	3E	40	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/IDMT curves.				
IN1>1 k (RI)	3E	41	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
STAGE 1 E/F 2	3E	43		
The settings under this sub-heading relate to derived Earth Fault protection (EF2)				
IN2>1 Status	3E	44	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN2>1 Current	3E	45	0.2	From 0.05 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the derived Earth Fault element during the tclp time delay.				
IN2>1 IDG Is	3E	46	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting defines the new TMS of the IDG curve during the tclp time.				
IN2>1 Time Delay	3E	48	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the derived Earth Fault element during the tclp time.				
IN2>1 TMS	3E	49	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN2>1 Time Dial	3E	4A	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/IDMT curves.				
IN2>1 k (RI)	3E	4B	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
OVERCURRENT	3E	4F		
The settings under this sub-heading relate to the Phase Overcurrent elements				
I>5 Status	3E	50	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
I>5 Current Set	3E	51	1.5	From 0.01 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the fifth stage Overcurrent element during the tclp time delay.				
I>5 Time Delay	3E	53	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the fifth stage Overcurrent element during the tclp time.				
I>5 TMS	3E	54	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
I>5 Time Dial	3E	55	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/US IDMT curves.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
I>5 k (RI)	3E	56	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting sets the new time multiplier setting to adjust the operate time of the RI curve during the tclp time.				
I>6 Status	3E	58	Block	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
I>6 Current Set	3E	59	25	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the sixth stage Overcurrent element during the tclp time delay.				
I>6 Time Delay	3E	5A	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the sixth stage Overcurrent element during the tclp time.				
STAGE 2 E/F 1	3E	5C		
The settings under this sub-heading relate to measured Earth Fault protection (EF1)				
IN1>2 Status	3E	5D	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN1>2 Current	3E	5E	0.2	From 0.01 to 4 in steps of 0.001 *[Courier Number (current)]*
This setting sets the new pick-up setting for the measured Earth Fault element during the tclp time delay.				
IN1>2 Current	3E	5E	0.2	From 0.005 to 4 in steps of 0.001 *[Courier Number (current)]*
This setting sets the new pick-up setting for the measured Earth Fault element during the tclp time delay.				
IN1>2 IDG Is	3E	5F	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting defines the new TMS of the IDG curve during the tclp time.				
IN1>2 Time Delay	3E	60	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the measured Earth Fault element during the tclp time.				
IN1>2 TMS	3E	61	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN1>2 Time Dial	3E	62	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/IDMT curves.				
IN1>2 k (RI)	3E	63	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
STAGE 3 E/F 1	3E	65		
The settings under this sub-heading relate to measured Earth Fault protection (EF1)				
IN1>3 Status	3E	66	Block	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN1>3 Current	3E	67	0.2	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the measured Earth Fault element during the tclp time delay.				
IN1>3 Time Delay	3E	68	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the measured Earth Fault element during the tclp time.				
STAGE 4 E/F 1	3E	6A		
The settings under this sub-heading relate to measured Earth Fault protection (EF1)				
IN1>4 Status	3E	6B	Block	Block Enable *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN1>4 Current	3E	6C	0.2	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the measured Earth Fault element during the tclp time delay.				
IN1>4 Time Delay	3E	6D	1	From 0 to 1200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the measured Earth Fault element during the tclp time.				
STAGE 2 E/F 2	3E	6F		
The settings under this sub-heading relate to derived Earth Fault protection (EF2)				
IN2>2 Status	3E	70	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN2>2 Current	3E	71	0.2	From 0.05 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the derived Earth Fault element during the tclp time delay.				
IN2>2 IDG Is	3E	72	1.5	From 1 to 4 in steps of 0.1 *[Courier Number (decimal)]*
This setting defines the new TMS of the IDG curve during the tclp time.				
IN2>2 Time Delay	3E	73	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the derived Earth Fault element during the tclp time.				
IN2>2 TMS	3E	74	1	From 0.025 to 1.2 in steps of 0.005 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
IN2>2 Time Dial	3E	75	1	From 0.01 to 100 in steps of 0.01 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEEE/IDMT curves.				
IN2>2 k (RI)	3E	76	1	From 0.1 to 10 in steps of 0.05 *[Courier Number (decimal)]*
This setting defines the TMS constant to adjust the operate time of the RI curve.				
STAGE 3 E/F 2	3E	78		
The settings under this sub-heading relate to derived Earth Fault protection (EF2)				
IN2>3 Status	3E	79	Block	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN2>3 Current	3E	7A	0.2	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the derived Earth Fault element during the tclp time delay.				
IN2>3 Time Delay	3E	7B	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the derived Earth Fault element during the tclp time.				
STAGE 4 E/F 2	3E	7D		
The settings under this sub-heading relate to derived Earth Fault protection (EF2)				
IN2>4 Status	3E	7E	Block	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
IN2>4 Current	3E	7F	0.2	From 0.01 to 32 in steps of 0.01 *[Courier Number (current)]*
This setting sets the new pick-up setting for the derived Earth Fault element during the tclp time delay.				
IN2>4 Time Delay	3E	80	1	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the derived Earth Fault element during the tclp time.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
STAGE 1 WDE	3E	82		
The settings under this sub-heading relate to Wattmetric Directional Earth Fault stage 1				
WDE>1 Status	3E	83	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
WDE>1 Act Pow	3E	84	0.4W	From 0.01 to 45 in steps of 0.01 *[Courier Number (power Watts)]*
This setting sets the active power pick-up threshold for WDE>1				
WDE>1 Fwd Time	3E	85	400ms	From 0.1 to 3 in steps of 0.05 *[Courier Number (time-seconds)]*
This setting sets the forward fault time delay (Temporisation AVal) for WDE>1				
STAGE 2 WDE	3E	87		
The settings under this sub-heading relate to Wattmetric Directional Earth Fault stage 1				
WDE>2 Status	3E	88	Enable	Block Enable *[Indexed String]*
Selecting 'Enable' means that the current and time settings in these cells will be used during the "tclp" time. Selecting 'Block' simply blocks the protection stage during the "tclp" time.				
WDE>2 Act Pow	3E	89	0.4W	From 0.01 to 45 in steps of 0.01 *[Courier Number (power Watts)]*
This setting sets the active power pick-up threshold for WDE>2				
WDE>2 Fwd Time	3E	8A	400ms	From 0.1 to 3 in steps of 0.05 *[Courier Number (time-seconds)]*
This setting sets the forward fault time delay (Temporisation AVal) for WDE>2				
GROUP 1: SELECTIVE LOGIC	3F	00		
This column contains settings for selective logic				
OVERCURRENT	3F	01		
The settings under this sub-heading relate to Phase Overcurrent Protection (POC). Selective Logic is only available for stages 3 and 4 and 6.				
I>3 Time Delay	3F	02	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the third stage Overcurrent element when the Selective Logic function is active.				
I>4 Time Delay	3F	03	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the fourth stage Overcurrent element when the Selective Logic function is active.				
I>6 Time Delay	3F	0D	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the new operate DT time delay for the sixth stage Overcurrent element when the Selective Logic function is active.				
EARTH FAULT 1	3F	14		
The settings under this sub-heading relate to measured Earth Fault Protection (EF1). Selective Logic is only available for stages 3 and 4.				
IN1>3 Time Delay	3F	15	2	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
Setting for the third stage definite time earth fault (measured) element operate time when the selective logic is active.				
IN1>4 Time Delay	3F	16	2	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
Setting for the fourth stage definite time earth fault (measured) element operate time when the selective logic is active.				
EARTH FAULT 2	3F	17		
The settings under this sub-heading relate to derived Earth Fault Protection (EF1). Selective Logic is only available for stages 3 and 4.				
IN2>3 Time Delay	3F	18	2	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
Setting for the third stage definite time earth fault (derived) element operate time when the selective logic is active.				
IN2>4 Time Delay	3F	19	2	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
Setting for the fourth stage definite time earth fault (derived) element operate time when the selective logic is active.				
SENSITIVE E/F	3F	1A		
The settings under this sub-heading relate to Sensitive Earth Fault Protection (EF1). Selective Logic is only available for stages 3 and 4.				
ISEF>3 Delay	3F	1B	1	From 0 to 200 in steps of 0.01

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (time-seconds)]
Setting for the third stage definite time sensitive earth fault element operate time when the selective logic is active.				
ISEF>4 Delay	3F	1C	0.5	From 0 to 200 in steps of 0.01 *[Courier Number (time-seconds)]*
Setting for the fourth stage definite time sensitive earth fault element operate time when the selective logic is active.				
GROUP 1: ADMIT PROTECTION	40	00		
This column contains settings for Admittance protection				
VN Threshold	40	01	10	From 1 to 40 in steps of 1 *[Courier Number (voltage)]*
The over admittance elements YN>. GN> and BN> will operate providing the neutral voltage remains above the set level for the set operating time of the element. They are blocked by operation of the fast VTS supervision output.				
Averaging Cycles	40	02	2	From 2 to 8 in steps of 1 *[Courier Number]*
This setting determine the number of averaging cycles used.				
Correction Angle	40	03	0	From -30 to 30 in steps of 1 *[Courier Number (angle)]*
This setting causes rotation of the directional boundary for conductance through the set correction angle.				
OVER ADMITTANCE	40	04		
The settings under this sub-heading relate to over admittance				
YN> Status	40	05	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the overadmittance stage. If the function is disabled, then all associated settings with exception of this setting, are hidden.				
YN> Set	40	06	0.005	From 0.0001*I3/V1 to 0.01*I3/V1 in steps of 0.0001*I3/V1 *[Courier Number (inverse ohms)]*
This sets the magnitude of the admittance threshold. If the measurement exceeds the set value and the magnitude of neutral voltage exceeds the set value threshold, the device will operate.				
YN> Set	40	07	0.05	From 0.001*I2/V1 to 0.1*I2/V1 in steps of 0.001*I2/V1 *[Courier Number (inverse ohms)]*
This cell sets the magnitude of the admittance threshold. If the measurement exceeds the set value and the magnitude of neutral voltage exceeds the set value threshold, the device will operate.				
YN> Time Delay	40	08	1	From 0.05 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This cell sets the operating time delay setting for the over admittance element.				
YN> tRESET	40	09	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This cell sets the reset/release time for the definite time reset characteristic.				
OVER CONDUCTANCE	40	0A		
The settings under this sub-heading relate to over conductance				
GN> Status	40	0B	Disabled	Disabled Enabled *[Indexed String]*
This setting to enables or disables the over conductance stage. If the function is disabled, then all associated settings with exception of this setting, are hidden.				
GN> Direction	40	0C	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for this element.				
GN> Set	40	0D	0.0008 0.0002	From 0.0001*I3/V1 to 0.005*I3/V1 in steps of 0.0001*I3/V1 *[Courier Number (inverse ohms)]*
This cell sets the magnitude of the over conductance threshold. Provided the magnitude and direction criteria are met for conductance and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate.				
GN> Set	40	0E	0.002	From 0.001*I2/V1 to 0.05*I2/V1 in steps of 0.001*I2/V1 *[Courier Number (inverse ohms)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell sets the magnitude of the over conductance threshold. Provided the magnitude and direction criteria are met for conductance and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate.				
GN> Time Delay	40	0F	1	From 0.05 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This cell sets the operating time delay setting for the over conductance element.				
GN> tRESET	40	10	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This cell sets the reset/release time for the definite time reset characteristic.				
OVER SUSCEPTANCE	40	11		
The settings under this sub-heading relate to over susceptance				
BN> Status	40	12	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the over susceptance stage. If the function is disabled, then all associated settings with exception of this setting, are hidden.				
BN> Direction	40	13	Non-Directional	Non-Directional Directional Fwd Directional Rev *[Indexed String]*
This setting determines the direction of measurement for this element.				
BN> Set	40	14	0.0008	From 0.0001*I3/V1 to 0.005*I3/V1 in steps of 0.0001*I3/V1 *[Courier Number (inverse ohms)]*
This cell sets the magnitude of the over susceptance threshold. Provided the magnitude and direction criteria are met for suseptance and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate.				
BN> Set	40	15	0.002	From 0.001*I2/V1 to 0.05*I2/V1 in steps of 0.001*I2/V1 *[Courier Number (inverse ohms)]*
This cell sets the magnitude of the over susceptance threshold. Provided the magnitude and direction criteria are met for suseptance and the magnitude of neutral voltage exceeds the set value VN Threshold, the device will operate.				
BN> Time Delay	40	16	1	From 0.05 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This cell sets the operating time delay setting for the over susceptance element.				
BN> tRESET	40	17	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This cell sets the reset/release time for the definite time reset characteristic.				
GROUP 1: POWER PROTECTION	41	00		
This column contains settings for Power protection				
OVER POWER	41	01		
The settings under this sub-heading relate to Overpower				
Power>1 Status	41	02	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage Overpower protection.				
Power>1Direction	41	03	Forward	Reverse Forward *[Indexed String]*
This setting determines the direction of the first stage Overpower element.				
Power>1 Mode	41	04	Active	Active Reactive *[Indexed String]*
There are two operation modes; Active or Reactive. This setting determines which mode is to be used for the first stage Overpower element.				
Power>1TimeDelay	41	05	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay setting for the first stage Overpower element.				
Power>1 tRESET	41	06	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time delay for the first stage Overpower element.				
Power>1 1Ph Watt	41	07	40	From 1 to 325 in steps of 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (power Watts)]
This setting sets the pick-up threshold for the single-phase Overpower element for the 'Active' mode.				
Power>1 1Ph VAr	41	08	24	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the single-phase Overpower element for the 'Reactive' mode.				
Power>1 3Ph Watt	41	09	120	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the three-phase Overpower element for the 'Active' mode.				
Power>1 3Ph VAr	41	0A	72	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the three-phase Overpower element for the 'Reactive' mode.				
Power>2 Status	41	0B	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage Overpower protection.				
Power>2Direction	41	0C	Forward	Reverse Forward *[Indexed String]*
This setting determines the direction of the second stage Overpower element.				
Power>2 Mode	41	0D	Active	Active Reactive *[Indexed String]*
There are two operation modes; Active or Reactive. This setting determines which mode is to be used for the second stage Overpower element.				
Power>2TimeDelay	41	0E	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay setting for the second stage Overpower element.				
Power>2 tRESET	41	0F	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time delay for the second stage Overpower element.				
Power>2 1Ph Watt	41	10	40	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the single-phase Overpower element for the 'Active' mode.				
Power>2 1Ph VAr	41	11	24	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the single-phase Overpower element for the 'Reactive' mode.				
Power>2 3Ph Watt	41	12	120	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the three-phase Overpower element for the 'Active' mode.				
Power>2 3Ph VAr	41	13	72	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the three-phase Overpower element for the 'Reactive' mode.				
UNDER POWER	41	14		
The settings under this sub-heading relate to Underpower				
Power<1 Status	41	15	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage Underpower protection.				
Power<1Direction	41	16	Forward	Reverse Forward *[Indexed String]*
This setting determines the direction of the first stage Underpower element.				
Power<1 Mode	41	17	Active	Active Reactive *[Indexed String]*
There are two operation modes; Active or Reactive. This setting determines which mode is to be used for the first stage Underpower element.				
Power<1TimeDelay	41	18	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay setting for the first stage Underpower element.				
Power<1 tRESET	41	19	0	From 0 to 100 in steps of 0.01

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Courier Number (time-seconds)]
This setting sets the time delay for the first stage Underpower element.				
Power<1 1Ph Watt	41	1A	10	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the single-phase Underpower element for the 'Active' mode.				
Power<1 1Ph VAr	41	1B	6	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the single-phase Underpower element for the 'Reactive' mode.				
Power<1 3Ph Watt	41	1C	30	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the three-phase Underpower element for the 'Active' mode.				
Power<1 3Ph VAr	41	1D	18	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the three-phase Underpower element for the 'Reactive' mode.				
Power<2 Status	41	1E	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage Underpower protection.				
Power<2Direction	41	1F	Forward	Reverse Forward *[Indexed String]*
This setting determines the direction of the second stage Underpower element.				
Power<2 Mode	41	20	Active	Active Reactive *[Indexed String]*
There are two operation modes; Active or Reactive. This setting determines which mode is to be used for the second stage Underpower element.				
Power<2TimeDelay	41	21	1	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay setting for the second stage Underpower element.				
Power<2 tRESET	41	22	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time delay for the second stage Underpower element.				
Power<2 1Ph Watt	41	23	10	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the single-phase Underpower element for the 'Active' mode.				
Power<2 1Ph VAr	41	24	6	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the single-phase Underpower element for the 'Reactive' mode.				
Power<2 3Ph Watt	41	25	30	From 1 to 325 in steps of 1 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the three-phase Underpower element for the 'Active' mode.				
Power<2 3Ph VAr	41	26	18	From 1 to 325 in steps of 1 *[Courier Number (power VARs)]*
This setting sets the pick-up threshold of the three-phase Underpower element for the 'Reactive' mode.				
Power< Blocking	41	27	0x3	Poledead Blocks Power<1 Poledead Blocks Power<2 *[Binary Flag (2 bits)]*
This setting is a 2 bit binary (Data type G402), whereby you can activate the Poledead Blocking for the Underpower and Overpower elements.				
SENSITIVE POWER	41	28		
The settings under this sub-heading relate to Sensitive Power protection				
Aph Sens Power	41	29	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables Sensitive Power protection (A-phase only)				
Comp Angle	41	2A	0	From -5 to 5 in steps of 0.1 *[Courier Number (angle)]*
This setting sets the CT compensating angle.				
Sens P1 Function	41	2B	Reverse	Disabled Reverse

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Low Forward Over *[Indexed String]*
This setting determines the type of Sensitive Power protection is used for this stage.				
Sens -P>1Setting	41	2C	0.5*V1*I3	From 0.3*V1*I3 to 100*V1*I3 in steps of 0.1*V1*I3 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the first stage Sensitive Reverse Power element.				
Sens P<1 Setting	41	2D	0.5*V1*I3	From 0.3*V1*I3 to 100*V1*I3 in steps of 0.1*V1*I3 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the first stage Low Forward Power element.				
Sens P>1 Setting	41	2E	50*V1*I3	From 0.3*V1*I3 to 100*V1*I3 in steps of 0.1*V1*I3 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the first stage Overpower element.				
Sens P1 Delay	41	2F	5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay setting for the first stage Sensitive Power element.				
Sens P1 tRESET	41	30	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the reset time delay for the first stage Sensitive Power element.				
P1 Poledead Inh	41	31	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage Pole Dead inhibit signal.				
Sens P2 Function	41	32	Low Forward	Disabled Reverse Low Forward Over *[Indexed String]*
This setting determines the type of Sensitive Power protection is used for this stage.				
Sens -P>2Setting	41	33	0.5*V1*I3	From 0.3*V1*I3 to 100*V1*I3 in steps of 0.1*V1*I3 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the second stage Sensitive Reverse Power element.				
Sens P<2 Setting	41	34	0.5*V1*I3	From 0.3*V1*I3 to 100*V1*I3 in steps of 0.1*V1*I3 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the second stage Low Forward Power element.				
Sens P>2 Setting	41	35	50*V1*I3	From 0.3*V1*I3 to 100*V1*I3 in steps of 0.1*V1*I3 *[Courier Number (power Watts)]*
This setting sets the pick-up threshold for the second stage Overpower element.				
Sens P2 Delay	41	36	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operate time delay setting for the second stage Sensitive Power element.				
Sens P2 tRESET	41	37	0	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the reset time delay for the second stage Sensitive Power element.				
P2 Poledead Inh	41	38	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage Pole Dead inhibit signal.				
GROUP 1: VOLT PROTECTION	42	00		
This column contains settings for Voltage protection				
UNDERVOLTAGE	42	01		
The settings under this sub-heading relate to undervoltage				
V< Measur't Mode	42	02	Phase-Phase	Phase-Phase Phase-Neutral *[Indexed String]*
This set determines the voltage input mode - phase-to-phase or phase-to-neutral.				
V< Operate Mode	42	03	Any Phase	Any Phase Three Phase *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting determines whether any one of the phases or all three of the phases has to satisfy the undervoltage criteria before a decision is made.				
V<1 Function	42	04	DT	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage undervoltage element.				
V<1 Voltage Set	42	05	80	From 5*V1 to 120*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage undervoltage element.				
V<1 Time Delay	42	06	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage undervoltage element.				
V<1 TMS	42	07	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
V<1 Poledead Inh	42	08	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Pole Dead inhibit logic.				
V<2 Status	42	09	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage undervoltage element. There is no choice of curves because this stage is DT only.				
V<2 Voltage Set	42	0A	60	From 5*V1 to 120*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage undervoltage element.				
V<2 Time Delay	42	0B	5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage undervoltage element.				
V<2 Poledead Inh	42	0C	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Pole Dead inhibit logic.				
V<3 Function	42	0D	Disabled	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the third stage undervoltage element.				
V<3 Voltage Set	42	0E	80	From 5*V1 to 120*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the third stage undervoltage element.				
V<3 Time Delay	42	0F	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage undervoltage element.				
V<3 TMS	42	10	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
V<3 Poledead Inh	42	11	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Pole Dead inhibit logic.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
OVERVOLTAGE	42	12		
The settings under this sub-heading relate to Overvoltage				
V> Measur't Mode	42	13	Phase-Phase	Phase-Phase Phase-Neutral *[Indexed String]*
This set determines the voltage input mode - phase-to-phase or phase-to-neutral.				
V> Operate Mode	42	14	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the overvoltage criteria before a decision is made.				
V>1 Function	42	15	DT	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the first stage overvoltage element.				
V>1 Voltage Set	42	16	130	From 10*V1 to 200*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage overvoltage element.				
V>1 Time Delay	42	17	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage overvoltage element.				
V>1 TMS	42	18	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
V>2 Status	42	19	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage overvoltage element. There is no choice of curves because this stage is DT only.				
V>2 Voltage Set	42	1A	150	From 10*V1 to 200*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage overvoltage element.				
V>2 Time Delay	42	1B	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage overvoltage element.				
V>3 Function	42	1C	Disabled	Disabled DT IDMT Def User Curve 1 Def User Curve 2 Def User Curve 3 Def User Curve 4 *[Indexed String]*
This setting determines the tripping characteristic for the third stage overvoltage element.				
V>3 Voltage Set	42	1D	130	From 10*V1 to 200*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the third stage overvoltage element.				
V>3 Time Delay	42	1E	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage overvoltage element.				
V>3 TMS	42	1F	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
DV/DT PROTECTION	42	20		
The settings under this sub-heading relate to rate of change of voltage				
dv/dt Meas Mode	42	21	Phase-Phase	Phase-Phase

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Phase-Neutral *[Indexed String]*
This set determines the voltage input mode - phase-to-phase or phase-to-neutral.				
dv/dt1 Function	42	22	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting determines the tripping direction for the first stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt1 Function	42	22	Disabled	Disabled *[Indexed String]*
This setting determines the tripping direction for the first stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt1 Oper Mode	42	23	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the dv/dt criteria before a decision is made.				
dv/dt1 AvgCycles	42	24	10	From 5 to 50 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of averaging cycles for the first stage dv/dt element.				
dv/dt1 Threshold	42	25	10	From 0.5*V1 to 200*V1 in steps of 0.5*V1 *[Courier Number (voltage/second)]*
This setting sets the voltage threshold for the first stage dv/dt element.				
dv/dt1 TimeDelay	42	26	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage dv/dt element.				
dv/dt1 tRESET	42	27	0.03	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
dv/dt2 Function	42	28	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting determines the tripping direction for the second stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt2 Function	42	28	Disabled	Disabled *[Indexed String]*
This setting determines the tripping direction for the second stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt2 Oper Mode	42	29	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the dv/dt criteria before a decision is made.				
dv/dt2 AvgCycles	42	2A	5	From 5 to 50 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of averaging cycles for the second stage dv/dt element.				
dv/dt2 Threshold	42	2B	50	From 0.5*V1 to 200*V1 in steps of 0.5*V1 *[Courier Number (voltage/second)]*
This setting sets the voltage threshold for the second stage dv/dt element.				
dv/dt2 TimeDelay	42	2C	0.3	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage dv/dt element.				
dv/dt2 tRESET	42	2D	0.03	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
dv/dt3 Function	42	2E	Disabled	Disabled Negative Positive

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Both *[Indexed String]*
This setting determines the tripping direction for the third stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt3 Function	42	2E	Disabled	Disabled *[Indexed String]*
This setting determines the tripping direction for the third stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt3 Oper Mode	42	2F	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the dv/dt criteria before a decision is made.				
dv/dt3 AvgCycles	42	30	10	From 5 to 50 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of averaging cycles for the third stage dv/dt element.				
dv/dt3 Threshold	42	31	10	From 0.5*V1 to 200*V1 in steps of 0.5*V1 *[Courier Number (voltage/second)]*
This setting sets the voltage threshold for the third stage dv/dt element.				
dv/dt3 TimeDelay	42	32	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the third stage dv/dt element.				
dv/dt3 tRESET	42	33	0.03	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
dv/dt4 Function	42	34	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting determines the tripping direction for the fourth stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt4 Function	42	34	Disabled	Disabled *[Indexed String]*
This setting determines the tripping direction for the fourth stage of dv/dt element - either disabled, for a rising voltage (positive), or a falling voltage (negative).				
dv/dt4 Oper Mode	42	35	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the dv/dt criteria before a decision is made.				
dv/dt4 AvgCycles	42	36	5	From 5 to 50 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of averaging cycles for the fourth stage dv/dt element.				
dv/dt4 Threshold	42	37	50	From 0.5*V1 to 200*V1 in steps of 0.5*V1 *[Courier Number (voltage/second)]*
This setting sets the voltage threshold for the fourth stage dv/dt element.				
dv/dt4 TimeDelay	42	38	0.3	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the fourth stage dv/dt element.				
dv/dt4 tRESET	42	39	0.03	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting determines the Reset time for the Definite Time Reset characteristic				
AVG UNDERVOLTAGE	42	40		
Sub-heading: Settings below are related to average undervoltage				
Vavg< Oper Mode	42	41	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the average undervoltage criteria before decision				
Vavg<1 Status	42	42	Disabled	Disabled Enabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting enables or disables the first stage average undervoltage element. There is no choice of curves because this stage is DT only.				
Vavg<1 Volt Set	42	43	80	From 10*V1 to 120*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage average undervoltage element.				
Vavg<1 Stt Time	42	44	0	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT start time delay for the first stage average undervoltage element.				
Vavg<1 Trip Time	42	45	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT trip time delay for the first stageaverage undervoltage element.				
Vavg<2 Status	42	4A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage average undervoltage element. There is no choice of curves because this stage is DT only.				
Vavg<2 Volt Set	42	4B	60	From 10*V1 to 120*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage average undervoltage element.				
Vavg<2 Stt Time	42	4C	0	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT start time delay for the second stage average undervoltage element.				
Vavg<2 Trip Time	42	4D	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT trip time delay for the second stage average undervoltage element.				
AVG OVERVOLTAGE	42	50		
Sub-heading: Settings below are related to average overvoltage				
Vavg> Oper Mode	42	51	Any Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the average overvoltage criteria before decision.				
Vavg>1 Status	42	52	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage average overvoltage element. There is no choice of curves because this stage is DT only.				
Vavg>1 Volt Set	42	53	130	From 40*V1 to 185*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage average overvoltage element.				
Vavg>1 Stt Time	42	54	0	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT start time delay for the first stage average overvoltage element.				
Vavg>1 Trip Time	42	55	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT trip time delay for the first stage average overvoltage element.				
Vavg>2 Status	42	5A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage average overvoltage element. There is no choice of curves because this stage is DT only.				
Vavg>2 Volt Set	42	5B	150	From 40*V1 to 185*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage average overvoltage element.				
Vavg>2 Stt Time	42	5C	0	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT start time delay for the second stage average overvoltage element.				
Vavg>2 Trip Time	42	5D	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the DT trip time delay for the second stage average overvoltage element.				
AVG ZERO SEQ O/V	42	60		
Sub-heading: Settings below are related to average zero sequence overvoltage				
V0avg>1 Status	42	61	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage "avg zero seq O/V" element. There is no choice of curves because this stage is DT only.				
V0avg>1 Volt Set	42	62	15	From 1*V1 to 110*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage average zero sequence overvoltage element.				
V0avg>1 Delay	42	63	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage "avg zero seq O/V" element.				
V0avg>2 Status	42	6A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage "avg zero seq O/V" element. There is no choice of curves because this stage is DT only.				
V0avg>2 Volt Set	42	6B	15	From 1*V1 to 110*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage "avg zero seq O/V" element.				
V0avg>2 Delay	42	6C	10	
This setting sets the DT time delay for the second stage "avg zero seq O/V" element.				
AVG POS SEQ O/V	42	70		
Sub-heading: Settings below are related to average positive sequence over voltage				
V1avg>1 Status	42	71	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage "avg pos seq O/V" element. There is no choice of curves because this stage is DT only.				
V1avg>1 Volt Set	42	72	130	From 40*V1 to 185*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage "avg pos seq O/V" element.				
V1avg>1 Delay	42	73	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage "avg pos seq O/V" element.				
V1avg>2 Status	42	7A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage "avg pos seq O/V" element. There is no choice of curves because this stage is DT only.				
V1avg>2 Volt Set	42	7B	130	From 40*V1 to 185*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage "avg pos seq O/V" element.				
V1avg>2 Delay	42	7C	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage of "avg pos seq O/V" element.				
AVG NEG SEQ O/V	42	80		
Sub-heading: Settings below are related to average negative sequence over voltage				
V2avg>1 Status	42	81	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage "avg neg seq O/V" element. There is no choice of curves because this stage is DT only.				
V2avg>1 Volt Set	42	82	15	From 1*V1 to 110*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage "avg neg seq O/V" element.				
V2avg>1 Stt Time	42	83	0	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the DT start time delay for the first stage "avg neg seq O/V" element.				
V2avg>1 Trp Time	42	84	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT trip time delay for the first stage "avg neg seq O/V" element.				
V2avg>2 Status	42	8A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage "avg neg seq O/V" element. There is no choice of curves because this stage is DT only.				
V2avg>2 Volt Set	42	8B	15	From 1*V1 to 110*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage "avg neg seq O/V" element.				
V2avg>2 Stt Time	42	8C	0	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT start time delay for the second stage "avg neg seq O/V" element.				
V2avg>2 Trp Time	42	8D	10	From 0 to 600 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the DT trip time delay for the second stage "avg neg seq O/V" element.				
POS SEQ U/V	42	A0		
The settings under this sub-heading relate to positive sequence undervoltage				
V1<1 Function	42	A1	Disabled	Disabled DT IDMT *[Indexed String]*
This setting determines the tripping characteristic for the first stage positive sequence undervoltage element.				
V1<1 Voltage Set	42	A2	80	From 5*V1 to 120*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage positive sequence undervoltage element.				
V1<1 Time Delay	42	A3	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage positive sequence undervoltage element.				
V1<1 TMS	42	A4	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
V1<1 Poledead Inh	42	A5	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Pole Dead inhibit logic.				
V1<2 Status	42	A9	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage positive sequence undervoltage element. There is no choice of curves because this stage is DT only.				
V1<2 Voltage Set	42	AA	60	From 5*V1 to 120*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage positive sequence undervoltage element.				
V1<2 Time Delay	42	AB	5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage positive sequence undervoltage element.				
V1<2 Poledead Inh	42	AC	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Pole Dead inhibit logic.				
POS SEQ O/V	42	B0		
The settings under this sub-heading relate to Overvoltage				
V1>1 Function	42	B1	Disabled	Disabled DT IDMT *[Indexed String]*
This setting determines the tripping characteristic for the first stage positive sequence overvoltage element.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
V1>1 Voltage Set	42	B2	130	From 5*V1 to 200*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the first stage positive sequence overvoltage element.				
V1>1 Time Delay	42	B3	10	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the first stage positive sequence overvoltage element.				
V1>1 TMS	42	B4	1	From 0.5 to 100 in steps of 0.5 *[Courier Number (decimal)]*
This is the Time Multiplier Setting to adjust the operate time of IEC IDMT curves.				
V1>2 Status	42	B9	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage positive sequence overvoltage element. There is no choice of curves because this stage is DT only.				
V1>2 Voltage Set	42	BA	150	From 5*V1 to 200*V1 in steps of 0.1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the second stage positive sequence overvoltage element.				
V1>2 Time Delay	42	BB	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the DT time delay for the second stage positive sequence overvoltage element.				
V VECTOR SHIFT	42	C0		
The settings under this sub-heading relate to Overvoltage				
V Shift Status	42	C1	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the voltage vector shift protection.				
V Shift Angle	42	C2	10	From 2 to 30 in steps of 1 *[Courier Number (angle)]*
This setting sets the voltage vector shift angle threshold				
VTS Block 1	42	FD	0x00000C00	VTS Blk Vavg<1 VTS Blk Vavg<2 VTS Blk Vavg>1 VTS Blk Vavg>2 VTS Blk V0avg>1 VTS Blk V0avg>2 VTS Blk V1avg>1 VTS Blk V1avg>2 VTS Blk V2avg>1 VTS Blk V2avg>2 VTS Blk V1<1 VTS Blk V1<2 VTS Blk V1>1 VTS Blk V1>2 *[Binary Flag (32 bits)]*
This setting cell contains a binary string where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with VTS				
VTS Block 2	42	FE	0x00000007	VTS Blk Vavg<1 VTS Blk Vavg<2 VTS Blk Vavg>1 VTS Blk Vavg>2 VTS Blk V0avg>1 VTS Blk V0avg>2 VTS Blk V1avg>1 VTS Blk V1avg>2 VTS Blk V2avg>1 VTS Blk V2avg>2 VTS Blk V1<1 VTS Blk V1<2 VTS Blk V1>1 VTS Blk V1>2 *[Binary Flag (32 bits)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting cell contains a binary string where you can define which blocking signals block which stage. The available settings depend on the model chosen. This description is for models with VTS				
GROUP 1: RESTRICTED E/F	43	00		
This column contains settings for Restricted Earth Fault Protection				
REF Options	43	01	Lo Z REF	Hi Z REF Lo Z REF *[Indexed String]*
This setting determines the Restricted Earth Fault mode of operation - high impedance or low impedance.				
IREF> k1	43	02	20	From 0 to 20 in steps of 1 *[Courier Number (percentage)]*
This setting sets the first slope constant of the low impedance biased characteristic.				
IREF> k2	43	03	150	From 0 to 150 in steps of 1 *[Courier Number (percentage)]*
This setting sets the second slope constant of the low impedance biased characteristic.				
IREF> Is1	43	04	0.2	From 0.08 to 1 in steps of 0.01 *[Courier Number (current)]*
This setting sets the bias current threshold for the first slope of the low impedance characteristic.				
IREF> Is2	43	05	1	From 0.1 to 1.5 in steps of 0.01 *[Courier Number (current)]*
This setting sets the bias current threshold for the second slope of the low impedance characteristic.				
IREF> Is	43	06	0.2	From 0.05 to 1 in steps of 0.01 *[Courier Number (current)]*
Setting that determines the minimum differential operate current for the hi-impedance element.				
GROUP 1: CB FAIL & I<	45	00		
This column contains settings for circuit breaker fail and undercurrent protection.				
BREAKER FAIL	45	01		
The settings under this sub-heading relate to Circuit Breaker Fail (CB Fail) settings.				
CB Fail 1 Status	45	02	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage of the CB Fail protection.				
CB Fail 1 Timer	45	03	0.2	From 0 to 50 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the first stage CB Fail timer in which the CB opening must be detected.				
CB Fail 2 Status	45	04	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage of the CB Fail protection.				
CB Fail 2 Timer	45	05	0.4	From 0 to 50 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the second stage CB Fail timer in which the CB opening must be detected.				
Volt Prot Reset	45	06	CB Open & I<	I< Only CB Open & I Prot Reset & I *[Indexed String]*
This setting determines the elements that will reset the CB fail timer for CB Failures, which were initiated by the voltage protection function.				
Ext Prot Reset	45	07	CB Open & I<	I< Only CB Open & I Prot Reset & I *[Indexed String]*
This setting determines the elements that will reset the CB fail timer for CB Failures initiated by external protection functions.				
UNDER CURRENT	45	08		
The settings under this sub-heading relate to Undercurrent settings				
I< Current Set	45	09	0.1	From 0.02*I1 to 3.2*I1 in steps of 0.01*I1 *[Courier Number (current)]*
This setting determines the current threshold, which will reset the CB Fail timer for Overcurrent-based protection.				
IN< Current Set	45	0A	0.1	From 0.02*I2 to 3.2*I2 in steps of 0.01*I2 *[Courier Number (current)]*
This setting determines the current threshold, which will reset the CB Fail timer for Earth Fault-based protection				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
ISEF< Current	45	0B	0.02	From 0.001*I3 to 0.8*I3 in steps of 0.0005*I3 *[Courier Number (current)]*
This setting determines the current threshold, which will reset the CB Fail timer for SEF-based protection.				
BLOCKED O/C	45	0C		
The settings under this sub-heading relate to Blocked Overcurrent settings.				
Remove I> Start	45	0D	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Remove I>Start signal.				
Remove IN> Start	45	0E	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the Remove IN>Start signal.				
GROUP 1: SUPERVISION	46	00		
This column contains settings for Supervision.				
VT SUPERVISION	46	01		
The settings under this sub-heading relate to Voltage Transformer Supervision (VTS).				
VTS Status	46	02	Blocking	Blocking Indication *[Indexed String]*
This setting determines which operations will occur upon VTS detection. • VTS provides alarm indication only. • VTS provides blocking of voltage dependent protection elements.				
VTS Reset Mode	46	03	Manual	Manual Auto *[Indexed String]*
There are two reset methods; Manual reset (via the front panel or remote communications), or Automatic reset (providing the VTS condition has been removed and the 3 phase voltages have been restored for more than 240ms.				
VTS Time Delay	46	04	5	From 1 to 10 in steps of 0.1 *[Courier Number (time-seconds)]*
This setting that determines the operate time-delay upon detection of a VTS condition.				
VTS I> Inhibit	46	05	10	From 0.08*I1 to 32*I1 in steps of 0.01*I1 *[Courier Number (current)]*
The setting is used to override a VTS blocking signal in the event of a phase fault occurring on the system that could trigger VTS logic.				
VTS I2> Inhibit	46	06	0.05	From 0.05*I1 to 0.5*I1 in steps of 0.01*I1 *[Courier Number (current)]*
The setting is used to override a voltage supervision block in the event of a fault occurring on the system with negative sequence current above this setting which could trigger the voltage supervision logic.				
CT SUPERVISION	46	07		
The settings under this sub-heading relate to Current Transformer Supervision (CTS).				
CTS Status	46	08	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables CT Supervision.				
CTS VN< Inhibit	46	09	5	From 0.5 to 22 in steps of 0.5 *[Courier Number (voltage)]*
This setting is used to inhibit the CTS element should the zero sequence voltage exceed this threshold The setting is only visible if CTS Mode is not disabled.				
CTS VN< Inhibit	46	09	5	From 0.50*V3/0.50*V1 to 22.00*V3/22.00*V1 in steps of 0.50*V3/0.50*V1 *[Courier Number (voltage)]*
This setting is used to inhibit the CTS element should the zero sequence voltage exceed this threshold The setting is only visible if CTS Mode is not disabled.				
CTS IN> Set	46	0A	0.1	From 0.08 to 4 in steps of 0.01 *[Courier Number (current)]*
This setting determines the level of zero sequence current that must be present for a valid current transformer supervision condition. The setting is visible if CTS Mode is not disabled				
CTS Time Delay	46	0B	5	From 0 to 10 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the operate time delay for the CTS element.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
VTS PickupThresh	46	0C	30	From 20 to 120 in steps of 1 *[Courier Number (voltage)]*
This setting sets the threshold for the VTS element.				
GROUP 1: FAULT LOCATOR	47	00		
This column contains settings for Fault locator				
Line Length	47	01	16000	From 10 to 1000000 in steps of 1 *[Courier Number (metres)]*
This setting sets the line length in metres.				
Line Length	47	02	9.936	From 0.006 to 621 in steps of 0.006 *[Courier Number (miles)]*
This setting sets the line length in miles.				
Line Impedance	47	03	6	From 0.1*V1/I1 to 250*V1/I1 in steps of 0.01*V1/I1 *[Courier Number (impedance)]*
This setting sets the positive sequence line impedance in ohms				
Line Angle	47	04	70	From 5 to 85 in steps of 1 *[Courier Number (angle)]*
This setting sets the positive sequence line impedance angle in degrees				
KZN Residual	47	05	1	From 0 to 7 in steps of 0.01 *[Courier Number (decimal)]*
This setting sets the residual compensating factor.				
KZN Res Angle	47	06	0	From -90 to 90 in steps of 1 *[Courier Number (angle)]*
This setting sets the residual compensating factor angle.				
GROUP 1: SYSTEM CHECKS	48	00		
This column contains settings for the Voltage Monitors and the Check Synchronism function.				
VOLTAGE MONITORS	48	14		
The settings under this sub-heading relate to Voltage Monitors				
Live Voltage	48	15	32	From 1*V1 to 132*V1 in steps of 0.5*V1 *[Courier Number (voltage)]*
This setting sets the minimum voltage threshold above which a line or bus is considered 'Live'.				
Dead Voltage	48	16	13	From 1*V1 to 132*V1 in steps of 0.5*V1 *[Courier Number (voltage)]*
This setting sets the maximum voltage threshold below which a line or bus is considered 'Dead'.				
CHECK SYNC.	48	17		
The settings under this sub-heading relate to Check Synchronism.				
CS1 Status	48	18	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage Check Synchronism element.				
CS1 Phase Angle	48	19	20	From 5 to 90 in steps of 1 *[Courier Number (angle)]*
This setting sets the maximum phase angle difference between the line and bus voltage for the first stage Phase Angle check to be satisfactory.				
CS1 Slip Control	48	1A	Frequency	None Timer Frequency Both *[Indexed String]*
This setting determines whether the first stage Slip Control is by slip frequency, by timer, or a combination of both.				
CS1 Slip Freq	48	1B	0.05	From 0.001 to 2 in steps of 0.001 *[Courier Number (frequency)]*
This setting sets the maximum frequency difference between the line and bus voltage for the first stage Slip Frequency check to be satisfactory.				
CS1 Slip Timer	48	1C	1	From 0 to 99 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time delay for the first stage Check Synchronism element.				
CS2 Status	48	1D	Disabled	Disabled Enabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting enables or disables the second stage Check Synchronism element.				
CS2 Phase Angle	48	1E	20	From 5 to 90 in steps of 1 *[Courier Number (angle)]*
This setting sets the maximum phase angle difference between the line and bus voltage for the second stage Phase Angle check to be satisfactory.				
CS2 Slip Control	48	1F	Frequency	None Timer Frequency Timer + Freq Freq + CB Comp *[Indexed String]*
This setting determines whether the second stage Slip Control is by slip frequency, by timer, or a combination of both.				
CS2 Slip Freq	48	20	0.05	From 0.001 to 2 in steps of 0.001 *[Courier Number (frequency)]*
This setting sets the maximum frequency difference between the line and bus voltage for the second stage Slip Frequency check to be satisfactory.				
CS2 Slip Timer	48	21	1	From 0 to 99 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the minimum operate time delay for the second stage Check Synchronism element.				
CS Undervoltage	48	22	54	From 10 to 132 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the check sync undervoltage threshold				
CS Overvoltage	48	23	130	From 40 to 185 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the check sync overvoltage threshold				
CS Diff Voltage	48	24	6.5	From 1 to 132 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets the maximum voltage magnitude difference between the line and bus, which is allowed for the check to be satisfactory.				
CS Voltage Block	48	25	V<	None V< V> Vdiff> V< and V> V< and Vdiff> V> and Vdiff> V< V> and Vdiff> *[Indexed String]*
This setting determines which condition or conditions must be satisfied in order for the Check Synchronism condition to be satisfactory. The setting is an 8-bit binary string (data type G41).				
SYSTEM SPLIT	48	26		
The settings under this sub-heading relate to System Split condition (System Split is where a line and bus are detected, which are not possible to synchronise).				
SS Status	48	27	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the System Split function.				
SS Phase Angle	48	28	120	From 90 to 175 in steps of 1 *[Courier Number (angle)]*
This setting sets the maximum phase angle difference between the line and bus voltage, which must be exceeded for the System Split condition to be satisfied.				
SS Under V Block	48	29	Enabled	Disabled Enabled *[Indexed String]*
This setting activates the undervoltage blocking.				
SS Undervoltage	48	2A	54	From 10 to 132 in steps of 0.5 *[Courier Number (voltage)]*
This setting sets an undervoltage threshold above which the line and bus voltage must be, to satisfy the System Split condition.				
SS Timer	48	2B	1	From 0 to 99 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
The System Split output remains set for as long as the System Split criteria are true, or for a minimum period equal to the System Split Timer setting, whichever is longer.				
CB Close Time	48	2F	0.05	From 0 to 0.5 in steps of 0.001 *[Courier Number (time-seconds)]*
This setting sets the CB closing time, from receipt of a CB close command until the main contacts touch.				
GROUP 1: AUTORECLOSE	49	00		
This column contains settings for Autoreclose (AR)				
AR Mode Select	49	01	Command Mode	Command Mode Opto Set Mode User Set Mode Pulse Set Mode *[Indexed String]*
This setting determines the Autoreclose mode.				
Number of Shots	49	02	1	From 1 to 4 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the required number of Autoreclose cycles for Overcurrent trips.				
Number SEF Shots	49	03	0	From 0 to 4 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of required Autoreclose cycles for SEF trips.				
Sequence Co-ord	49	04	Disabled	Disabled Enabled *[Indexed String]*
This setting enables the sequence co-ordination function to ensure the correct protection grading between an upstream and downstream re-closing device.				
CS AR Immediate	49	05	Disabled	Disabled Enabled *[Indexed String]*
This setting allows immediate re-closure of the circuit breaker provided both sides of the circuit breaker are live and in synchronism at any time after the dead time has started.				
Dead Time 1	49	06	10	From 0.01 to 300 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the dead time for the first Autoreclose cycle.				
Dead Time 2	49	07	60	From 0.01 to 300 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the dead time for the second Autoreclose cycle.				
Dead Time 3	49	08	180	From 0.01 to 9999 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the dead time for the third Autoreclose cycle.				
Dead Time 4	49	09	180	From 0.01 to 9999 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the dead time for the fourth Autoreclose cycle.				
CB Healthy Time	49	0A	5	From 0.01 to 9999 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the CB lockout time				
Start Dead t On	49	0B	Protection Reset	Protection Reset CB Trips *[Indexed String]*
This setting determines whether the dead time has started when the circuit breaker trips or when the protection trip resets.				
tReclaim Extend	49	0C	No Operation	On Prot Start No Operation *[Indexed String]*
This setting allows the user to control whether the reclaim timer is suspended by the protection start contacts or not (i.e. whether the IED is permitted to reclaim if a fault condition is present and will be cleared in a long time-scale).				
Reclaim Time 1	49	0D	180	From 1 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
Sets the Autoreclose reclaim time for the first Autoreclose cycle.				
Reclaim Time 2	49	0E	180	From 1 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
Sets the Autoreclose reclaim time for the second Autoreclose cycle.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Reclaim Time 3	49	0F	180	From 1 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
Sets the Autoreclose reclaim time for the third Autoreclose cycle.				
Reclaim Time 4	49	10	180	From 1 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
Sets the Autoreclose reclaim time for the fourth Autoreclose cycle.				
AR Inhibit Time	49	11	5	From 0.01 to 600 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting defines the inhibit time before Autoreclose is initiated following a manual CB closure.				
AR Lockout	49	12	No Block	No Block Block Inst Prot *[Indexed String]*
This setting is used to block instantaneous protection if the IED has undergone Autoreclose Lockout.				
EFF Maint Lock	49	13	No Block	No Block Block Inst Prot *[Indexed String]*
This setting is used to block instantaneous protection for the last circuit breaker trip before lockout occurs.				
AR Deselected	49	14	No Block	No Block Block Inst Prot *[Indexed String]*
This setting allows the instantaneous protection to be blocked when Autoreclose is in non-auto mode of operation.				
Manual Close	49	15	No Block	No Block Block Inst Prot *[Indexed String]*
This setting is used to block instantaneous protection when the circuit breaker is closed manually whilst there is no auto-reclose sequence in progress or Autoreclose is inhibited.				
Trip 1 Main	49	16	No Block	No Block Block Inst Prot *[Indexed String]*
The Trip (n) Main settings are used to selectively block the instantaneous elements of phase and earth fault protection elements for a circuit breaker trip sequence.				
Trip 2 Main	49	17	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) Main settings are used to selectively block the instantaneous elements of phase and earth fault protection elements for a circuit breaker trip sequence.				
Trip 3 Main	49	18	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) Main settings are used to selectively block the instantaneous elements of phase and earth fault protection elements for a circuit breaker trip sequence.				
Trip 4 Main	49	19	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) Main settings are used to selectively block the instantaneous elements of phase and earth fault protection elements for a circuit breaker trip sequence.				
Trip 5 Main	49	1A	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) Main settings are used to selectively block the instantaneous elements of phase and earth fault protection elements for a circuit breaker trip sequence.				
Trip 1 SEF	49	1B	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) SEF settings are used to selectively block the instantaneous elements of sensitive earth fault protection elements for a circuit breaker trip sequence.				
Trip 2 SEF	49	1C	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) SEF settings are used to selectively block the instantaneous elements of sensitive earth fault protection elements for a circuit				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
breaker trip sequence.				
Trip 3 SEF	49	1D	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) SEF settings are used to selectively block the instantaneous elements of sensitive earth fault protection elements for a circuit breaker trip sequence.				
Trip 4 SEF	49	1E	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) SEF settings are used to selectively block the instantaneous elements of sensitive earth fault protection elements for a circuit breaker trip sequence.				
Trip 5 SEF	49	1F	Block Inst Prot	No Block Block Inst Prot *[Indexed String]*
The Trip (n) SEF settings are used to selectively block the instantaneous elements of sensitive earth fault protection elements for a circuit breaker trip sequence.				
Man Close on Flt	49	20	Lockout	No Lockout Lockout *[Indexed String]*
This setting decides whether the AR should lockout or not after a Manual Close on Fault operation.				
Trip AR Inactive	49	21	No Lockout	No Lockout Lockout *[Indexed String]*
When AR is inactive (Non-auto, or Live Line mode), this setting determines whether The AR should be locked out or not.				
Reset Lockout by	49	22	User Interface	User Interface Select NonAuto *[Indexed String]*
This setting is used to determine the method by which the Lockout is reset.				
AR on Man Close	49	24	Inhibited	Enabled Inhibited *[Indexed String]*
If this is set to 'Enabled', autoreclosing can be initiated immediately on circuit breaker closure, overriding the settings AR Inhibit Time, Man Close on Flt and Manual Close.				
Sys Check Time	49	25	5	From 0.01 to 9999 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the amount of time set for System Checks for Autoreclose operation.				
AR Skip Shot 1	49	26	Disabled	Disabled Enabled *[Indexed String]*
When enabled this setting allows the Autoreclose sequence counter to be incremented by one via a DDB input signal. This will therefore decrease the number of available re-close shots.				
AR INITIATION	49	28		
The settings under this sub-heading relate to Autoreclose initiation				
I>1 AR	49	29	Initiate Main AR	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the first stage overcurrent protection on AR operation.				
I>2 AR	49	2A	Initiate Main AR	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the second stage overcurrent protection on AR operation.				
I>3 AR	49	2B	Initiate Main AR	No Action Initiate Main AR Block AR *[Indexed String]*
This setting determines impact of the third stage overcurrent protection on AR operation.				
I>4 AR	49	2C	Initiate Main AR	No Action Initiate Main AR Block AR *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting determines impact of the fourth stage overcurrent protection on AR operation.				
IN1>1 AR	49	2D	Initiate Main AR	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the first stage measured earth fault overcurrent protection on AR operation.				
IN1>2 AR	49	2E	Initiate Main AR	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the second stage measured earth fault overcurrent protection on AR operation.				
IN1>3 AR	49	2F	Initiate Main AR	No Action Initiate Main AR Block AR *[Indexed String]*
This setting determines impact of the third stage measured earth fault overcurrent protection on AR operation.				
IN1>4 AR	49	30	Initiate Main AR	No Action Initiate Main AR Block AR *[Indexed String]*
This setting determines impact of the fourth stage measured earth fault overcurrent protection on AR operation.				
IN2>1 AR	49	31	No Action	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the first stage derived earth fault overcurrent protection on AR operation.				
IN2>2 AR	49	32	No Action	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the second stage derived earth fault overcurrent protection on AR operation.				
IN2>3 AR	49	33	No Action	No Action Initiate Main AR Block AR *[Indexed String]*
This setting determines impact of the third stage derived earth fault overcurrent protection on AR operation.				
IN2>4 AR	49	34	No Action	No Action Initiate Main AR Block AR *[Indexed String]*
This setting determines impact of the fourth stage derived earth fault overcurrent protection on AR operation.				
ISEF>1 AR	49	35	No Action	No Action Initiate Main AR Initiate SEF AR Block AR *[Indexed String]*
This setting determines impact of the first stage sensitive earth fault overcurrent protection on AR operation.				
ISEF>2 AR	49	36	No Action	No Action Initiate Main AR Initiate SEF AR Block AR *[Indexed String]*
This setting determines impact of the second stage sensitive earth fault overcurrent protection on AR operation.				
ISEF>3 AR	49	37	No Action	No Action Initiate Main AR Initiate SEF AR Block AR *[Indexed String]*
This setting determines impact of the third stage sensitive earth fault overcurrent protection on AR operation.				
ISEF>4 AR	49	38	No Action	No Action Initiate Main AR Initiate SEF AR Block AR *[Indexed String]*
This setting determines impact of the fourth stage sensitive earth fault overcurrent protection on AR operation.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Ext Prot	49	3C	No Action	No Action Initiate Main AR *[Indexed String]*
This setting determines if external protection inputs initiates auto-reclose. This must be mapped in programmable scheme logic.				
I>5 AR	49	3D	Initiate Main AR	No Action Initiate Main AR *[Indexed String]*
This setting determines impact of the fifth stage overcurrent protection on AR operation.				
I>6 AR	49	3E	Initiate Main AR	No Action Initiate Main AR Block AR *[Indexed String]*
This setting determines impact of the sixth stage overcurrent protection on AR operation.				
SYSTEM CHECKS	49	40		
The settings under this sub-heading relate to Autoreclose system checks				
AR with ChkSyn	49	41	Disabled	Disabled Enabled *[Indexed String]*
This setting enables/disables Autoreclose with check synchronisation for Check Sync stage 1 (CS1)				
AR with SysSyn	49	42	Disabled	Disabled Enabled *[Indexed String]*
This setting enables/disables Autoreclose with check synchronisation for Check Sync stage 2 (CS2)				
Live/Dead Ccts	49	43	Disabled	Disabled Enabled *[Indexed String]*
When enabled, this setting will produce an "AR Check Ok" DDB signal when the Live/Dead Ccts DDB signal is high.				
No System Checks	49	44	Enabled	Disabled Enabled *[Indexed String]*
When enabled this setting completely disables system checks thus allowing Autoreclose initiation without system checks.				
SysChk on Shot 1	49	45	Enabled	Disabled Enabled *[Indexed String]*
This setting is used to enable/disable system checks for the first auto-reclose shot.				
GROUP 1: INPUT LABELS	4A	00		
This column contains settings for the opto-input Labels				
Opto Input 1	4A	01	Input L1	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 1				
Opto Input 2	4A	02	Input L2	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 2				
Opto Input 3	4A	03	Input L3	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 3				
Opto Input 4	4A	04	Input L4	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 4				
Opto Input 5	4A	05	Input L5	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 5				
Opto Input 6	4A	06	Input L6	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 6				
Opto Input 7	4A	07	Input L7	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 7				
Opto Input 8	4A	08	Input L8	From 32 to 234 in steps of 1

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[ASCII Text (16 chars)]
This setting defines the label for opto-input 8				
Opto Input 9	4A	09	Input L9	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 9				
Opto Input 10	4A	0A	Input L10	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 10				
Opto Input 11	4A	0B	Input L11	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 11				
Opto Input 12	4A	0C	Input L12	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 12				
Opto Input 13	4A	0D	Input L13	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for opto-input 13				
GROUP 1: OUTPUT LABELS	4B	00		
This column contains settings for the output relay labels				
Relay 1	4B	01	Output R1	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 1				
Relay 2	4B	02	Output R2	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 2				
Relay 3	4B	03	Output R3	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 3				
Relay 4	4B	04	Output R4	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 4				
Relay 5	4B	05	Output R5	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 5				
Relay 6	4B	06	Output R6	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 6				
Relay 7	4B	07	Output R7	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 7				
Relay 8	4B	08	Output R8	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 8				
Relay 9	4B	09	Output R9	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 9				
Relay 10	4B	0A	Output R10	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 10				
Relay 11	4B	0B	Output R11	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 11				
Relay 12	4B	0C	Output R12	From 32 to 234 in steps of 1 *[ASCII Text (16 chars)]*
This setting defines the label for output relay 12				
GROUP 1: FREQ PROTECTION	4D	00		
This column contains settings for frequency protection.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Freq Avg.Cycles	4D	01	5	From 0 to 48 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of power system cycles that are used to average the frequency measurement.				
df/dt Avg.Cycles	4D	02	5	From 0 to 48 in steps of 1 *[Unsigned Integer (16 bits)]*
This setting sets the number of power system cycles that are used to average the rate of change of frequency measurement.				
V<B Status	4D	03	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the frequency protection elements.				
V<B Voltage Set	4D	04	25*V1	From 10*V1 to 120*V1 in steps of 1*V1 *[Courier Number (voltage)]*
This setting sets the pick-up threshold for the undervoltage blocking element.				
V<B Measur Mode	4D	05	Phase-Phase	Phase-Phase Phase-Neutral *[Indexed String]*
This set determines the mode for the measured input voltage that will be used for the undervoltage blocking: phase-to-phase or phase-to-neutral.				
V<B Operate Mode	4D	06	Three Phase	Any Phase Three Phase *[Indexed String]*
This setting determines whether any one of the phases or all three of the phases has to satisfy the undervoltage criteria before a decision is made.				
Stage 1	4D	07	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage of frequency protection.				
Stg 1 f+t Status	4D	08	Under	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 1 f+t Freq	4D	09	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the first stage frequency protection element.				
Stg 1 f+t Time	4D	0A	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the first stage frequency protection element.				
df/dt+t 1 Status	4D	0B	Negative	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the first stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 1 Set	4D	0C	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the first stage.				
df/dt+t 1 Time	4D	0D	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the first stage rate of change of frequency protection element.				
f+df/dt 1 Status	4D	0E	Negative	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the first stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 1 Status	4D	0E	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the first stage frequency-supervised rate of change of frequency protection				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
(f+df/dt).				
f+df/dt 1 freq	4D	0F	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the first stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 1 df/dt	4D	10	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the first stage frequency-supervised rate of change of frequency.				
f+Df/Dt 1 Status	4D	11	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 1 Status	4D	11	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 1 freq	4D	12	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the first stage average rate of change of frequency protection element.				
f+Df/Dt 1 Dfreq	4D	13	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the first stage average rate of change of frequency protection element.				
f+Df/Dt 1 Dtime	4D	14	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the first stage average rate of change of frequency protection element.				
Restore1 Status	4D	15	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the first stage of load restoration.				
Restore1 Status	4D	15	Disabled	Disabled *[Indexed String]*
This setting enables or disables the first stage of load restoration.				
Restore1 Freq	4D	16	49.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the first stage of load restoration, above which the associated load restoration time can start.				
Restore1 Time	4D	17	240	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the first stage restoration frequency setting to permit load restoration.				
Holding Timer 1	4D	18	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the first stage load restoration.				
Stg 1 UV Block	4D	19	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the first stage load restoration element.				
Stage 2	4D	1A	Enabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage of frequency protection.				
Stg 2 f+t Status	4D	1B	Under	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 2 f+t Freq	4D	1C	48.6	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the pick-up threshold for the second stage frequency protection element.				
Stg 2 f+t Time	4D	1D	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the second stage frequency protection element.				
df/dt+t 2 Status	4D	1E	Negative	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the second stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 2 Set	4D	1F	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the second stage.				
df/dt+t 2 Time	4D	20	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the second stage rate of change of frequency protection element.				
f+df/dt 2 Status	4D	21	Negative	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the second stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 2 Status	4D	21	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the second stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 2 freq	4D	22	48.6	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the second stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 2 df/dt	4D	23	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the second stage frequency-supervised rate of change of frequency.				
f+Df/Dt 2 Status	4D	24	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 2 Status	4D	24	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 2 freq	4D	25	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the second stage average rate of change of frequency protection element.				
f+Df/Dt 2 Dfreq	4D	26	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the second stage average rate of change of frequency protection element.				
f+Df/Dt 2 Dtime	4D	27	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the second stage average rate of change of frequency protection element.				
Restore2 Status	4D	28	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the second stage of load restoration.				
Restore2 Status	4D	28	Disabled	Disabled *[Indexed String]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting enables or disables the second stage of load restoration.				
Restore2 Freq	4D	29	49.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the second stage of load restoration, above which the associated load restoration time can start.				
Restore2 Time	4D	2A	180	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the second stage restoration frequency setting to permit load restoration.				
Holding Timer 2	4D	2B	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the second stage load restoration.				
Stg 2 UV Block	4D	2C	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the second stage load restoration element.				
Stage 3	4D	2D	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage of frequency protection.				
Stg 3 f+t Status	4D	2E	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 3 f+t Freq	4D	2F	48.2	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the third stage frequency protection element.				
Stg 3 f+t Time	4D	30	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the third stage frequency protection element.				
df/dt+t 3 Status	4D	31	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the third stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 3 Set	4D	32	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the third stage.				
df/dt+t 3 Time	4D	33	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the third stage rate of change of frequency protection element.				
f+df/dt 3 Status	4D	34	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the third stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 3 Status	4D	34	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the third stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 3 freq	4D	35	48.2	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the third stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 3 df/dt	4D	36	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the third stage frequency-supervised rate of change of frequency.				
f+Df/Dt 3 Status	4D	37	Disabled	Disabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 3 Status	4D	37	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 3 freq	4D	38	48.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the third stage average rate of change of frequency protection element.				
f+Df/Dt 3 Dfreq	4D	39	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the third stage average rate of change of frequency protection element.				
f+Df/Dt 3 Dtime	4D	3A	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the third stage average rate of change of frequency protection element.				
Restore3 Status	4D	3B	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the third stage of load restoration.				
Restore3 Status	4D	3B	Disabled	Disabled *[Indexed String]*
This setting enables or disables the third stage of load restoration.				
Restore3 Freq	4D	3C	49.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the third stage of load restoration, above which the associated load restoration time can start.				
Restore3 Time	4D	3D	120	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the third stage restoration frequency setting to permit load restoration.				
Holding Timer 3	4D	3E	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the third stage load restoration.				
Stg 3 UV Block	4D	3F	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the third stage load restoration element.				
Stage 4	4D	40	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage of frequency protection.				
Stg 4 f+t Status	4D	41	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 4 f+t Freq	4D	42	47.8	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fourth stage frequency protection element.				
Stg 4 f+t Time	4D	43	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the fourth stage frequency protection element.				
df/dt+t 4 Status	4D	44	Disabled	Disabled Negative Positive Both

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting disables or determines the tripping direction for the fourth stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 4 Set	4D	45	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the fourth stage.				
df/dt+t 4 Time	4D	46	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the fourth stage rate of change of frequency protection element.				
f+df/dt 4 Status	4D	47	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the fourth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 4 Status	4D	47	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the fourth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 4 freq	4D	48	47.8	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fourth stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 4 df/dt	4D	49	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the fourth stage frequency-supervised rate of change of frequency.				
f+Df/Dt 4 Status	4D	4A	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 4 Status	4D	4A	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 4 freq	4D	4B	48.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fourth stage average rate of change of frequency protection element.				
f+Df/Dt 4 Dfreq	4D	4C	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the fourth stage average rate of change of frequency protection element.				
f+Df/Dt 4 Dtime	4D	4D	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the fourth stage average rate of change of frequency protection element.				
Restore4 Status	4D	4E	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fourth stage of load restoration.				
Restore4 Status	4D	4E	Disabled	Disabled *[Indexed String]*
This setting enables or disables the fourth stage of load restoration.				
Restore4 Freq	4D	4F	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fourth stage of load restoration, above which the associated load restoration time can start.				
Restore4 Time	4D	50	240	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the fourth stage restoration frequency setting to permit load restoration.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Holding Timer 4	4D	51	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the fourth stage load restoration.				
Stg 4 UV Block	4D	52	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the fourth stage load restoration element.				
Stage 5	4D	53	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fifth stage of frequency protection.				
Stg 5 f+t Status	4D	54	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 5 f+t Freq	4D	55	47.4	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fifth stage frequency protection element.				
Stg 5 f+t Time	4D	56	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the fifth stage frequency protection element.				
df/dt+t 5 Status	4D	57	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the fifth stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 5 Set	4D	58	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the fifth stage.				
df/dt+t 5 Time	4D	59	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the fifth stage rate of change of frequency protection element.				
f+df/dt 5 Status	4D	5A	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the fifth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 5 Status	4D	5A	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the fifth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 5 freq	4D	5B	47.4	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fifth stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 5 df/dt	4D	5C	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the fifth stage frequency-supervised rate of change of frequency.				
f+Df/Dt 5 Status	4D	5D	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 5 Status	4D	5D	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
this stage.				
f+Df/Dt 5 freq	4D	5E	48	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fifth stage average rate of change of frequency protection element.				
f+Df/Dt 5 Dfreq	4D	5F	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the fifth stage average rate of change of frequency protection element.				
f+Df/Dt 5 Dtime	4D	60	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the fifth stage average rate of change of frequency protection element.				
Restore5 Status	4D	61	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the fifth stage of load restoration.				
Restore5 Status	4D	61	Disabled	Disabled *[Indexed String]*
This setting enables or disables the fifth stage of load restoration.				
Restore5 Freq	4D	62	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the fifth stage of load restoration, above which the associated load restoration time can start.				
Restore5 Time	4D	63	180	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the fifth stage restoration frequency setting to permit load restoration.				
Holding Timer 5	4D	64	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the fifth stage load restoration.				
Stg 5 UV Block	4D	65	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the fifth stage load restoration element.				
Stage 6	4D	66	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the sixth stage of frequency protection.				
Stg 6 f+t Status	4D	67	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 6 f+t Freq	4D	68	47	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the sixth stage frequency protection element.				
Stg 6 f+t Time	4D	69	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the sixth stage frequency protection element.				
df/dt+t 6 Status	4D	6A	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting determines the tripping direction for the sixth stage of dv/dt element - either disabled, for a rising frequency (positive), or a falling frequency (negative) for the sixth stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 6 Set	4D	6B	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the sixth stage.				
df/dt+t 6 Time	4D	6C	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This setting sets the operating time delay for the sixth stage rate of change of frequency protection element.				
f+df/dt 6 Status	4D	6D	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the sixth stage independent rate of change of frequency protection (df/dt+t).				
f+df/dt 6 Status	4D	6D	Disabled	Disabled *[Indexed String]*
This setting sets the rate of change of frequency threshold for the sixth stage.				
f+df/dt 6 freq	4D	6E	47	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the operating time delay for the sixth stage rate of change of frequency protection element.				
f+df/dt 6 df/dt	4D	6F	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting disables or determines the tripping direction for the sixth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+Df/Dt 6 Status	4D	70	Disabled	Disabled Under Over *[Indexed String]*
This setting disables or determines the tripping direction for the sixth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+Df/Dt 6 Status	4D	70	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 6 freq	4D	71	48	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the sixth stage average rate of change of frequency protection element.				
f+Df/Dt 6 Dfreq	4D	72	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the sixth stage average rate of change of frequency protection element.				
f+Df/Dt 6 Dtime	4D	73	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the sixth stage average rate of change of frequency protection element.				
Restore6 Status	4D	74	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the sixth stage of load restoration.				
Restore6 Status	4D	74	Disabled	Disabled *[Indexed String]*
This setting enables or disables the sixth stage of load restoration.				
Restore6 Freq	4D	75	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the sixth stage of load restoration, above which the associated load restoration time can start.				
Restore6 Time	4D	76	120	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the sixth stage restoration frequency setting to permit load restoration.				
Holding Timer 6	4D	77	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the sixth stage load restoration.				
Stg 6 UV Block	4D	78	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the sixth stage load restoration element.				
Stage 7	4D	79	Disabled	Disabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				Enabled *[Indexed String]*
This setting enables or disables the seventh stage of frequency protection.				
Stg 7 f+t Status	4D	7A	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 7 f+t Freq	4D	7B	46.6	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the seventh stage frequency protection element.				
Stg 7 f+t Time	4D	7C	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the seventh stage frequency protection element.				
df/dt+t 7 Status	4D	7D	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the seventh stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 7 Set	4D	7E	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the seventh stage.				
df/dt+t 7 Time	4D	7F	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the seventh stage rate of change of frequency protection element.				
f+df/dt 7 Status	4D	80	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the seventh stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 7 Status	4D	80	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the seventh stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 7 freq	4D	81	46.6	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the seventh stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 7 df/dt	4D	82	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the seventh stage frequency-supervised rate of change of frequency.				
f+Df/Dt 7 Status	4D	83	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 7 Status	4D	83	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 7 freq	4D	84	47.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the seventh stage average rate of change of frequency protection element.				
f+Df/Dt 7 Dfreq	4D	85	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the seventh stage average rate of change of frequency protection element.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
f+Df/Dt 7 Dtime	4D	86	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the seventh stage average rate of change of frequency protection element.				
Restore7 Status	4D	87	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the seventh stage of load restoration.				
Restore7 Status	4D	87	Disabled	Disabled *[Indexed String]*
This setting enables or disables the seventh stage of load restoration.				
Restore7 Freq	4D	88	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the seventh stage of load restoration, above which the associated load restoration time can start.				
Restore7 Time	4D	89	100	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the seventh stage restoration frequency setting to permit load restoration.				
Holding Timer 7	4D	8A	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the seventh stage load restoration.				
Stg 7 UV Block	4D	8B	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the seventh stage load restoration element.				
Stage 8	4D	8C	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the eighth stage of frequency protection.				
Stg 8 f+t Status	4D	8D	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				
Stg 8 f+t Freq	4D	8E	50.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the eighth stage frequency protection element.				
Stg 8 f+t Time	4D	8F	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the eighth stage frequency protection element.				
df/dt+t 8 Status	4D	90	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the eighth stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 8 Set	4D	91	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the eighth stage.				
df/dt+t 8 Time	4D	92	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the eighth stage rate of change of frequency protection element.				
f+df/dt 8 Status	4D	93	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the eighth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 8 Status	4D	93	Disabled	Disabled

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
This setting disables or determines the tripping direction for the eighth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 8 freq	4D	94	50.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the eighth stage frequency-supervised rate of change of frequency protection element.				
f+df/dt 8 df/dt	4D	95	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the eighth stage frequency-supervised rate of change of frequency.				
f+Df/Dt 8 Status	4D	96	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 8 Status	4D	96	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 8 freq	4D	97	50.5	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the eighth stage average rate of change of frequency protection element.				
f+Df/Dt 8 Dfreq	4D	98	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the eighth stage average rate of change of frequency protection element.				
f+Df/Dt 8 Dtime	4D	99	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the eighth stage average rate of change of frequency protection element.				
Restore8 Status	4D	9A	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the eighth stage of load restoration.				
Restore8 Status	4D	9A	Disabled	Disabled *[Indexed String]*
This setting enables or disables the eighth stage of load restoration.				
Restore8 Freq	4D	9B	49	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the eighth stage of load restoration, above which the associated load restoration time can start.				
Restore8 Time	4D	9C	80	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the eighth stage restoration frequency setting to permit load restoration.				
Holding Timer 8	4D	9D	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the eighth stage load restoration.				
Stg 8 UV Block	4D	9E	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the undervoltage blocking of the eighth stage load restoration element.				
Stage 9	4D	9F	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the ninth stage of frequency protection.				
Stg 9 f+t Status	4D	A0	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection, or disables it for this stage.				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Stg 9 f+t Freq	4D	A1	51	From 40.1 to 69.9 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the pick-up threshold for the ninth stage frequency protection element.				
Stg 9 f+t Time	4D	A2	2	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the ninth stage frequency protection element.				
df/dt+t 9 Status	4D	A3	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the ninth stage independent rate of change of frequency protection (df/dt+t).				
df/dt+t 9 Set	4D	A4	2	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the rate of change of frequency threshold for the ninth stage.				
df/dt+t 9 Time	4D	A5	0.5	From 0 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the operating time delay for the ninth stage rate of change of frequency protection element.				
f+df/dt 9 Status	4D	A6	Disabled	Disabled Negative Positive Both *[Indexed String]*
This setting disables or determines the tripping direction for the ninth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 9 Status	4D	A6	Disabled	Disabled *[Indexed String]*
This setting disables or determines the tripping direction for the ninth stage frequency-supervised rate of change of frequency protection (f+df/dt).				
f+df/dt 9 df/dt	4D	A8	1	From 0.01 to 15 in steps of 0.01 *[Courier Number (Hz/sec)]*
This setting sets the df/dt threshold for the ninth stage frequency-supervised rate of change of frequency.				
f+Df/Dt 9 Status	4D	A9	Disabled	Disabled Under Over *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 9 Status	4D	A9	Disabled	Disabled *[Indexed String]*
This setting selects either underfrequency or overfrequency protection for the average rate of change of frequency (Df/Dt), or disables it for this stage.				
f+Df/Dt 9 Dfreq	4D	AB	1	From 0.1 to 15 in steps of 0.01 *[Courier Number (frequency)]*
This setting sets the change in frequency that must be measured in the set time for the ninth stage average rate of change of frequency protection element.				
f+Df/Dt 9 Dtime	4D	AC	0.5	From 0.02 to 100 in steps of 0.01 *[Courier Number (time-seconds)]*
This setting sets the time period in which an excessive change in frequency must be measured for the ninth stage average rate of change of frequency protection element.				
Restore9 Status	4D	AD	Disabled	Disabled Enabled *[Indexed String]*
This setting enables or disables the ninth stage of load restoration.				
Restore9 Status	4D	AD	Disabled	Disabled *[Indexed String]*
This setting enables or disables the ninth stage of load restoration.				
Restore9 Time	4D	AF	60	From 0 to 7200 in steps of 0.25 *[Courier Number (time-seconds)]*
This setting sets the time period for which the measured frequency must be higher than the ninth stage restoration frequency setting to				

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
permit load restoration.				
Holding Timer 9	4D	B0	5	From 1 to 7200 in steps of 1 *[Courier Number (time-seconds)]*
This setting sets the holding time of the ninth stage load restoration.				
Stg 9 UV Block	4D	B1	Disabled	0 or 1 *[Indexed String]*
This setting enables or disables the undervoltage blocking of the ninth stage load restoration element.				
GROUP 1: PSL TIMERS	4E	00		
This column contains settings for frequency protection.				
Timer 1	4E	01	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #1				
Timer 2	4E	02	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #2				
Timer 3	4E	03	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #3				
Timer 4	4E	04	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #4				
Timer 5	4E	05	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #5				
Timer 6	4E	06	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #6				
Timer 7	4E	07	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #7				
Timer 8	4E	08	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #8				
Timer 9	4E	09	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #9				
Timer 10	4E	0A	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #10				
Timer 11	4E	0B	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #11				
Timer 12	4E	0C	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #12				
Timer 13	4E	0D	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #13				
Timer 14	4E	0E	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #14				
Timer 15	4E	0F	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #15				
Timer 16	4E	10	0	See 50300.3110.004 *[Courier Number (time-ms)]*
This setting sets PSL timer #16				
Domain	B2	04	PSL Settings	PSL Settings PSL Configuration

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Indexed String]
Sub-Domain	B2	08	Group 1	Group 1 Group 2 Group 3 Group 4 *[Indexed String]*
Version	B2	0C	256	From 0 to 65535 in steps of 1 *[Unsigned Integer (16 bits)]*
Transfer Mode	B2	1C	6	Prepare Rx Complete Rx Prepare Tx Complete Tx Rx Prepared Tx Prepared OK Error *[Indexed String]*
Data Transfer	B2	20		
Select Record Number - n	B4	01	0	From -199 to 199 in steps of 1 *[Unsigned Integer]*
Trigger Time	B4	02		Trigger Time *[IEC870 Date & Time]*
Active Channels	B4	03		Active Channels *[Binary Flag]*
Channel Types	B4	04		Channel Types *[Binary Flag]*
Channel Offsets	B4	05		Channel Offsets *[Courier Number (decimal)]*
Channel Scaling	B4	06		Channel Scaling *[Courier Number (decimal)]*
Channel SkewVal	B4	07		Channel SkewVal *[Integer]*
Channel MinVal	B4	08		Channel MinVal *[Integer]*
Channel MaxVal	B4	09		Channel MaxVal *[Integer]*
Compression Format	B4	0A	1	Compression Format *[Unsigned Integer (16 bits)]*
Upload Compression Record	B4	0B		Upload Compression Record *[Unsigned Integer (16 bits)]*
No. Of Samples	B4	10		No. Of Samples *[Unsigned Integer]*
Trig Position	B4	11		Trig Position

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
				[Unsigned Integer]
Time Base	B4	12		Time Base *[Courier Number (time-seconds)]*
Sample Timer	B4	14		Sample Timer *[Unsigned Integer]*
Dist. Channel 1	B4	20		Dist. Channel 1 *[Integer]*
Dist. Channel 2	B4	21		Dist. Channel 2 *[Integer]*
Dist. Channel 3	B4	22		Dist. Channel 3 *[Integer]*
Dist. Channel 4	B4	23		Dist. Channel 4 *[Integer]*
Dist. Channel 5	B4	24		Dist. Channel 5 *[Integer]*
Dist. Channel 6	B4	25		Dist. Channel 6 *[Integer]*
Dist. Channel 7	B4	26		Dist. Channel 7 *[Integer]*
Dist. Channel 8	B4	27		Dist. Channel 8 *[Integer]*
Dist. Channel 9	B4	28		Dist. Channel 9 *[Integer]*
Dist. Channel 10	B4	29		Dist. Channel 10 *[Integer]*
Dist. Channel 11	B4	2A		Dist. Channel 11 *[Integer]*
Dist. Channel 12	B4	2B		Dist. Channel 12 *[Integer]*
Dist. Channel 13	B4	2C		Dist. Channel 13 *[Integer]*
Dist. Channel 29	B4	3C		Dist. Channel 29 *[Binary Flag]*
Dist. Channel 30	B4	3D		Dist. Channel 30 *[Binary Flag]*
Dist. Channel 31	B4	3E		Dist. Channel 31 *[Binary Flag]*
Dist. Channel 32	B4	3F		Dist. Channel 32 *[Binary Flag]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
PSL DATA	B7	00		
This column contains information about the Programmable Scheme Logic				
Grp1 PSL Ref	B7	01		Grp1 PSL Ref *[ASCII Text (32 chars)]*
This setting displays the Group 1 PSL reference				
Date/Time	B7	02		Date/Time *[IEC870 Date & Time]*
This setting displays the date and time the PSL was created				
Grp1 PSL ID	B7	03		Grp1 PSL ID *[Unsigned Integer (32 bits)]*
This setting displays the Group 1 PSL ID				
Grp2 PSL Ref	B7	11		Grp2 PSL Ref *[ASCII Text (32 chars)]*
This setting displays the Group 2 PSL reference				
Date/Time	B7	12		Date/Time *[IEC870 Date & Time]*
This setting displays the date and time the PSL was created				
Grp2 PSL ID	B7	13		Grp2 PSL ID *[Unsigned Integer (32 bits)]*
This setting displays the Group 2 PSL ID				
Grp3 PSL Ref	B7	21		Grp3 PSL Ref *[ASCII Text (32 chars)]*
This setting displays the Group 3 PSL reference				
Date/Time	B7	22		Date/Time *[IEC870 Date & Time]*
This setting displays the date and time the PSL was created				
Grp3 PSL ID	B7	23		Grp3 PSL ID *[Unsigned Integer (32 bits)]*
This setting displays the Group 3 PSL ID				
Grp4 PSL Ref	B7	31		Grp4 PSL Ref *[ASCII Text (32 chars)]*
This setting displays the Group 4 PSL reference				
Date/Time	B7	32		Date/Time *[IEC870 Date & Time]*
This setting displays the date and time the PSL was created				
Grp4 PSL ID	B7	33		Grp4 PSL ID *[Unsigned Integer (32 bits)]*
This setting displays the Group 4 PSL ID				
USER CURVES DATA	B8	00		
This column contains settings and data for the user curves				
Curve 1 Name	B8	01	Def User Curve 1	Curve 1 Name *[ASCII Text (32 Chars)]*
This cell displays the name of user curve 1				
Date & Time	B8	02		Date & Time *[IEC 870 Date & Time]*
This cell displays the date and time the user curve was downloaded to the IED				
Curve 1 ID	B8	03		Curve 1 ID *[Unsigned Integer (16 bits)]*
This cell displays the ID of user curve 1				
UsrCrv1 Vrsn	B8	04	Operate Curve	Operate Curve Reset Curve UV Operate Curve *[Indexed String]*
This setting sets the curve type; either operate or reset.				
Curve 2 Name	B8	11	Def User Curve 2	Curve 2 Name *[ASCII Text (32 Chars)]*
This cell displays the name of user curve 2				
Date & Time	B8	12		Date & Time *[IEC 870 Date & Time]*

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
This cell displays the date and time the user curve was downloaded to the IED				
Curve 2 ID	B8	13		Curve 2 ID *[Unsigned Integer (16 bits)]*
This cell displays the ID of user curve 2				
UsrCrv2 Vrsn	B8	14	Operate Curve	Operate Curve Reset Curve UV Operate Curve *[Indexed String]*
This setting sets the curve type; either operate or reset.				
Curve 3 Name	B8	21	Def User Curve 3	Curve 3 Name *[ASCII Text (32 Chars)]*
This cell displays the name of user curve 3				
Date & Time	B8	22		Date & Time *[IEC 870 Date & Time]*
This cell displays the date and time the user curve was downloaded to the IED				
Curve 3 ID	B8	23		Curve 3 ID *[Unsigned Integer (16 bits)]*
This cell displays the ID of user curve 3				
UsrCrv3 Vrsn	B8	24	Reset Curve	Operate Curve Reset Curve UV Operate Curve *[Indexed String]*
This setting sets the curve type; either operate or reset.				
UsrCrv3 Vrsn	B8	24	Reset Curve	Operate Curve Reset Curve UV Operate Curve Th Operate Curve Th Reset Curve *[Indexed String]*
This setting sets the curve type; either operate or reset.				
Curve 4 Name	B8	31	Def User Curve 4	Curve 4 Name *[ASCII Text (32 Chars)]*
This cell displays the name of user curve 4				
Date & Time	B8	32		Date & Time *[IEC 870 Date & Time]*
This cell displays the date and time the user curve was downloaded to the IED				
Curve 4 ID	B8	33		Curve 4 ID *[Unsigned Integer (16 bits)]*
This cell displays the ID of user curve 4				
UsrCrv4 Vrsn	B8	34	Reset Curve	Operate Curve Reset Curve UV Operate Curve *[Indexed String]*
This setting sets the curve type; either operate or reset.				
UsrCrv4 Vrsn	B8	34	Reset Curve	Operate Curve Reset Curve UV Operate Curve Th Operate Curve Th Reset Curve *[Indexed String]*
This setting sets the curve type; either operate or reset.				
COMMS SYS DATA	BF	00		
Dist Record Cntrl Ref	BF	01	B300	Dist Record Cntrl Ref *[Menu Cell(2)]*
Dist Record Extract Ref	BF	02	B400	Dist Record Extract Ref *[Menu Cell(2)]*
Setting Transfer	BF	03		

MENU TEXT	COL	ROW	DEFAULT SETTING	AVAILABLE OPTIONS
DESCRIPTION				
Reset Demand Timers	BF	04		
Block Transfer Ref	BF	06	B200	Block Transfer Ref *[Menu Cell(2)]*
Read Only Mode	BF	07		Read Only Mode *[Menu Cell]*
Encryption Key	BF	10		Encryption Key *[Foreign Data]*
Connected i/face	BF	11		Connected i/face *[Unsigned Integer (16 bit)]*
Security Column	BF	12		Security Column *[Menu Cell]*
Port Disable	BF	13		Port Disable *[Menu Cell]*
Port Disable end	BF	14		Port Disable end *[Menu Cell]*
PW Entry Needed	BF	15		PW Entry Needed *[Unsigned Integer (32 bits)]*
ETHERNET STATUS	F0	00		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
0	Relay 1	DDB_OUTPUT_RELAY_1
DDB signal connected to output relay contact 1		
1	Relay 2	DDB_OUTPUT_RELAY_2
DDB signal connected to output relay contact 2		
2	Relay 3	DDB_OUTPUT_RELAY_3
DDB signal connected to output relay contact 3		
3	Relay 4	DDB_OUTPUT_RELAY_4
DDB signal connected to output relay contact 4		
4	Relay 5	DDB_OUTPUT_RELAY_5
DDB signal connected to output relay contact 5		
5	Relay 6	DDB_OUTPUT_RELAY_6
DDB signal connected to output relay contact 6		
6	Relay 7	DDB_OUTPUT_RELAY_7
DDB signal connected to output relay contact 7		
7	Relay 8	DDB_OUTPUT_RELAY_8
DDB signal connected to output relay contact 8		
8	Relay 9	DDB_OUTPUT_RELAY_9
DDB signal connected to output relay contact 9		
9	Relay 10	DDB_OUTPUT_RELAY_10
DDB signal connected to output relay contact 10		
10	Relay 11	DDB_OUTPUT_RELAY_11
DDB signal connected to output relay contact 11		
11	Relay 12	DDB_OUTPUT_RELAY_12
DDB signal connected to output relay contact 12		
32	Opto Input 1	DDB_OPTO_ISOLATOR_1
DDB signal connected to opto-input 1		
33	Opto Input 2	DDB_OPTO_ISOLATOR_2
DDB signal connected to opto-input 2		
34	Opto Input 3	DDB_OPTO_ISOLATOR_3
DDB signal connected to opto-input 3		
35	Opto Input 4	DDB_OPTO_ISOLATOR_4
DDB signal connected to opto-input 4		
36	Opto Input 5	DDB_OPTO_ISOLATOR_5
DDB signal connected to opto-input 5		
37	Opto Input 6	DDB_OPTO_ISOLATOR_6
DDB signal connected to opto-input 6		
38	Opto Input 7	DDB_OPTO_ISOLATOR_7
DDB signal connected to opto-input 7		
39	Opto Input 8	DDB_OPTO_ISOLATOR_8
DDB signal connected to opto-input 8		
40	Opto Input 9	DDB_OPTO_ISOLATOR_9
DDB signal connected to opto-input 9		
41	Opto Input 10	DDB_OPTO_ISOLATOR_10
DDB signal connected to opto-input 10		
42	Opto Input 11	DDB_OPTO_ISOLATOR_11
DDB signal connected to opto-input 11		
43	Opto Input 12	DDB_OPTO_ISOLATOR_12
DDB signal connected to opto-input 12		
44	Opto Input 13	DDB_OPTO_ISOLATOR_13
DDB signal connected to opto-input 13		
72	Relay Cond 1	DDB_OUTPUT_CON_1
DDB signal connected to output relay conditioner 1		
73	Relay Cond 2	DDB_OUTPUT_CON_2
DDB signal connected to output relay conditioner 2		
74	Relay Cond 3	DDB_OUTPUT_CON_3
DDB signal connected to output relay conditioner 3		
75	Relay Cond 4	DDB_OUTPUT_CON_4
DDB signal connected to output relay conditioner 4		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
76	Relay Cond 5	DDB_OUTPUT_CON_5
DDB signal connected to output relay conditioner 5		
77	Relay Cond 6	DDB_OUTPUT_CON_6
DDB signal connected to output relay conditioner 6		
78	Relay Cond 7	DDB_OUTPUT_CON_7
DDB signal connected to output relay conditioner 7		
79	Relay Cond 8	DDB_OUTPUT_CON_8
DDB signal connected to output relay conditioner 8		
80	Relay Cond 9	DDB_OUTPUT_CON_9
DDB signal connected to output relay conditioner 9		
81	Relay Cond 10	DDB_OUTPUT_CON_10
DDB signal connected to output relay conditioner 10		
82	Relay Cond 11	DDB_OUTPUT_CON_11
DDB signal connected to output relay conditioner 11		
83	Relay Cond 12	DDB_OUTPUT_CON_12
DDB signal connected to output relay conditioner 12		
112	Timer in 1	DDB_TIMERIN_1
DDB signal connected to timer 1 input		
113	Timer in 2	DDB_TIMERIN_2
DDB signal connected to timer 2 input		
114	Timer in 3	DDB_TIMERIN_3
DDB signal connected to timer 3 input		
115	Timer in 4	DDB_TIMERIN_4
DDB signal connected to timer 4 input		
116	Timer in 5	DDB_TIMERIN_5
DDB signal connected to timer 5 input		
117	Timer in 6	DDB_TIMERIN_6
DDB signal connected to timer 6 input		
118	Timer in 7	DDB_TIMERIN_7
DDB signal connected to timer 7 input		
119	Timer in 8	DDB_TIMERIN_8
DDB signal connected to timer 8 input		
120	Timer in 9	DDB_TIMERIN_9
DDB signal connected to timer 9 input		
121	Timer in 10	DDB_TIMERIN_10
DDB signal connected to timer 10 input		
122	Timer in 11	DDB_TIMERIN_11
DDB signal connected to timer 11 input		
123	Timer in 12	DDB_TIMERIN_12
DDB signal connected to timer 12 input		
124	Timer in 13	DDB_TIMERIN_13
DDB signal connected to timer 13 input		
125	Timer in 14	DDB_TIMERIN_14
DDB signal connected to timer 14 input		
126	Timer in 15	DDB_TIMERIN_15
DDB signal connected to timer 15 input		
127	Timer in 16	DDB_TIMERIN_16
DDB signal connected to timer 16 input		
128	Timer out 1	DDB_TIMEROUT_1
DDB signal connected to timer 1 output		
129	Timer out 2	DDB_TIMEROUT_2
DDB signal connected to timer 2 output		
130	Timer out 3	DDB_TIMEROUT_3
DDB signal connected to timer 3 output		
131	Timer out 4	DDB_TIMEROUT_4
DDB signal connected to timer 4 output		
132	Timer out 5	DDB_TIMEROUT_5
DDB signal connected to timer 5 output		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
133	Timer out 6	DDB_TIMEROUT_6
DDB signal connected to timer 6 output		
134	Timer out 7	DDB_TIMEROUT_7
DDB signal connected to timer 7 output		
135	Timer out 8	DDB_TIMEROUT_8
DDB signal connected to timer 8 output		
136	Timer out 9	DDB_TIMEROUT_9
DDB signal connected to timer 9 output		
137	Timer out 10	DDB_TIMEROUT_10
DDB signal connected to timer 10 output		
138	Timer out 11	DDB_TIMEROUT_11
DDB signal connected to timer 11output		
139	Timer out 12	DDB_TIMEROUT_12
DDB signal connected to timer 12 output		
140	Timer out 13	DDB_TIMEROUT_13
DDB signal connected to timer 13 output		
141	Timer out 14	DDB_TIMEROUT_14
DDB signal connected to timer 1 4 output		
142	Timer out 15	DDB_TIMEROUT_15
DDB signal connected to timer 15 output		
143	Timer out 16	DDB_TIMEROUT_16
DDB signal connected to timer 16 output		
144	Fault REC TRIG	DDB_FAULT_RECORDER_START
This DDB triggers the fault recorder		
145	SG-opto Invalid	DDB_ILLEGAL_OPTO_SETTINGS_GROUP
This DDB signal indicates that the Setting Group selection via opto-input is invalid		
146	Prot'n Disabled	DDB_OOS_ALARM
This DDB signal indicates an Out-of-Service condition		
147	F out of Range	DDB_FREQ_ALARM
This DDB signal indicates a 'Frequency out of range' condition		
148	VT Fail Alarm	DDB_VTS_INDICATION
This DDB signal indicates a Voltage Transformer Fail condition		
149	CT Fail Alarm	DDB_CTS_INDICATION
This DDB signal indicates a Current Transformer Fail condition		
150	CB Fail Alarm	DDB_BREAKER_FAIL_ALARM
This DDB signal is an alarm indicating CB Failure		
151	I^ Maint Alarm	DDB_BROKEN_CURRENT_ALARM
This DDB signal indicates that the total Broken Current has exceeded the set maintenance threshold		
152	I^ Lockout Alarm	DDB_BROKEN_CURRENT_LOCKOUT
This DDB signal initiates a CB lockout when the set Broken Current threshold has been exceeded		
153	CB Ops Maint	DDB_MAINTENANCE_ALARM
This DDB signal indicates that the number of CB operations has exceeded the set maintenance threshold		
154	CB Ops Lockout	DDB_MAINTENANCE_LOCKOUT
This DDB signal initiates a CB lockout when the set maintenance threshold has been exceeded		
155	CB Op Time Maint	DDB_EXCESSIVE_OP_TIME_ALARM
This DDB signal indicates that the total amount of CB operating time has exceeded the set maintenance threshold		
156	CB Op Time Lock	DDB_EXCESSIVE_OP_TIME_LOCKOUT
This DDB signal initiates a CB lockout when the set CB operating time threshold has been exceeded		
157	Fault Freq Lock	DDB_EFF_LOCKOUT
This DDB signal initiates a CB lockout when the set Excessive Fault Frequency threshold has been exceeded		
158	CB Status Alarm	DDB_CB_STATUS_ALARM
This DDB signal indicates that the CB is in an invalid state		
159	Man CB Trip Fail	DDB_CB_FAILED_TO_TRIP
This DDB signal indicates that the CB has failed to trip following manual trip		
160	CB Cls Fail	DDB_CB_FAILED_TO_CLOSE
This DDB signal indicates that the CB has failed to close		
161	Man CB Unhealthy	DDB_CONTROL_CB_UNHEALTHY
This DDB signal indicates that the CB is unhealthy		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
162	Man No Checksync	DDB_CONTROL_NO_CHECK_SYNC
This DDB signal indicates that there is no check synchronization while closing		
163	AR Lockout	DDB_AR_LOCKOUT
This DDB signal indicates that the AR did not result in successful reclosure and locks out further reclose attempts		
164	AR CB Unhealthy	DDB_AR_CB_UNHEALTHY
The scheme has waited for the "CB HEALTHY" signal for the HEALTHY WINDOW time.		
165	AR No Sys Check	DDB_AR_NO_SYS_CHECK
The scheme has waited for the "SYSTEM OK TO CLOSE" input for the SYSTEM CHECK WINDOW time		
166	System Split	DDB_SYSTEM_SPLIT_ALARM
This DDB signal is the System Split alarm		
167	UV Block	DDB_UNDERVOLTAGE_BLOCK
This DDB blocks the undervoltage element		
168	User Alarm 1	DDB_USER_ALARM_1
This DDB signal can be configured as a user-defined Alarm		
169	User Alarm 2	DDB_USER_ALARM_2
This DDB signal can be configured as a user-defined Alarm		
170	User Alarm 3	DDB_USER_ALARM_3
This DDB signal can be configured as a user-defined Alarm		
171	User Alarm 4	DDB_USER_ALARM_4
This DDB signal can be configured as a user-defined Alarm		
172	User Alarm 5	DDB_USER_ALARM_5
This DDB signal can be configured as a user-defined Alarm		
173	User Alarm 6	DDB_USER_ALARM_6
This DDB signal can be configured as a user-defined Alarm		
174	User Alarm 7	DDB_USER_ALARM_7
This DDB signal can be configured as a user-defined Alarm		
175	User Alarm 8	DDB_USER_ALARM_8
This DDB signal can be configured as a user-defined Alarm		
176	User Alarm 9	DDB_USER_ALARM_9
This DDB signal can be configured as a user-defined Alarm		
177	User Alarm 10	DDB_USER_ALARM_10
This DDB signal can be configured as a user-defined Alarm		
178	User Alarm 11	DDB_USER_ALARM_11
This DDB signal can be configured as a user-defined Alarm		
179	User Alarm 12	DDB_USER_ALARM_12
This DDB signal can be configured as a user-defined Alarm		
180	User Alarm 13	DDB_USER_ALARM_13
This DDB signal can be configured as a user-defined Alarm		
181	User Alarm 14	DDB_USER_ALARM_14
This DDB signal can be configured as a user-defined Alarm		
182	User Alarm 15	DDB_USER_ALARM_15
This DDB signal can be configured as a user-defined Alarm		
183	User Alarm 16	DDB_USER_ALARM_16
This DDB signal can be configured as a user-defined Alarm		
184	User Alarm 17	DDB_USER_ALARM_17
This DDB signal can be configured as a user-defined Alarm		
185	User Alarm 18	DDB_USER_ALARM_18
This DDB signal can be configured as a user-defined Alarm		
186	User Alarm 19	DDB_USER_ALARM_19
This DDB signal can be configured as a user-defined Alarm		
187	User Alarm 20	DDB_USER_ALARM_20
This DDB signal can be configured as a user-defined Alarm		
188	User Alarm 21	DDB_USER_ALARM_21
This DDB signal can be configured as a user-defined Alarm		
189	User Alarm 22	DDB_USER_ALARM_22
This DDB signal can be configured as a user-defined Alarm		
190	User Alarm 23	DDB_USER_ALARM_23
This DDB signal can be configured as a user-defined Alarm		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
191	User Alarm 24	DDB_USER_ALARM_24
This DDB signal can be configured as a user-defined Alarm		
192	User Alarm 25	DDB_USER_ALARM_25
This DDB signal can be configured as a user-defined Alarm		
193	User Alarm 26	DDB_USER_ALARM_26
This DDB signal can be configured as a user-defined Alarm		
194	User Alarm 27	DDB_USER_ALARM_27
This DDB signal can be configured as a user-defined Alarm		
195	User Alarm 28	DDB_USER_ALARM_28
This DDB signal can be configured as a user-defined Alarm		
196	User Alarm 29	DDB_USER_ALARM_29
This DDB signal can be configured as a user-defined Alarm		
197	User Alarm 30	DDB_USER_ALARM_30
This DDB signal can be configured as a user-defined Alarm		
198	User Alarm 31	DDB_USER_ALARM_31
This DDB signal can be configured as a user-defined Alarm		
199	User Alarm 32	DDB_USER_ALARM_32
This DDB signal can be configured as a user-defined Alarm		
200	MR User Alarm 33	DDB_USER_ALARM_33
This DDB signal can be configured as manual reset alarm		
201	MR User Alarm 34	DDB_USER_ALARM_34
This DDB signal can be configured as manual reset alarm		
202	MR User Alarm 35	DDB_USER_ALARM_35
This DDB signal can be configured as manual reset alarm		
203	I>1 Timer Block	DDB_POC_1_TIMER_BLOCK
This DDB signal blocks the first stage overcurrent time delay		
204	I>2 Timer Block	DDB_POC_2_TIMER_BLOCK
This DDB signal blocks the second stage overcurrent time delay		
205	I>3 Timer Block	DDB_POC_3_TIMER_BLOCK
This DDB signal blocks the third stage overcurrent time delay		
206	I>4 Timer Block	DDB_POC_4_TIMER_BLOCK
This DDB signal blocks the fourth stage overcurrent time delay		
207	Inhibit CBF	DDB_INHIBIT_CBF
This DDB signal is used to inhibit the CB Fail function and reset all associated DDBs.		
208	IN1>1 Timer Blk	DDB_EF1_1_TIMER_BLOCK
This DDB signal blocks the first stage measured Earth Fault time delay		
209	IN1>2 Timer Blk	DDB_EF1_2_TIMER_BLOCK
This DDB signal blocks the second stage measured Earth Fault time delay		
210	IN1>3 Timer Blk	DDB_EF1_3_TIMER_BLOCK
This DDB signal blocks the third stage measured Earth Fault time delay		
211	IN1>4 Timer Blk	DDB_EF1_4_TIMER_BLOCK
This DDB signal blocks the fourth stage measured Earth Fault time delay		
212	IN2>1 Timer Blk	DDB_EF2_1_TIMER_BLOCK
This DDB signal blocks the first stage derived Earth Fault time delay		
213	IN2>2 Timer Blk	DDB_EF2_2_TIMER_BLOCK
This DDB signal blocks the second stage derived Earth Fault time delay		
214	IN2>3 Timer Blk	DDB_EF2_3_TIMER_BLOCK
This DDB signal blocks the third stage derived Earth Fault time delay		
215	IN2>4 Timer Blk	DDB_EF2_4_TIMER_BLOCK
This DDB signal blocks the fourth stage derived Earth Fault time delay		
216	ISEF>1 Timer Blk	DDB_SEF_1_TIMER_BLOCK
This DDB signal blocks the first stage Sensitive Earth Fault time delay		
217	ISEF>2 Timer Blk	DDB_SEF_2_TIMER_BLOCK
This DDB signal blocks the second stage Sensitive Earth Fault time delay		
218	ISEF>3 Timer Blk	DDB_SEF_3_TIMER_BLOCK
This DDB signal blocks the third stage Sensitive Earth Fault time delay		
219	ISEF>4 Timer Blk	DDB_SEF_4_TIMER_BLOCK
This DDB signal blocks the fourth stage Sensitive Earth Fault time delay		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
220	VN>1 Timer Blk	DDB_RESOV_1_TIMER_BLOCK
This DDB signal blocks the first stage Residual Overvoltage time delay		
221	VN>2 Timer Blk	DDB_RESOV_2_TIMER_BLOCK
This DDB signal blocks the second stage Residual Overvoltage time delay		
222	V<1 Timer Block	DDB_PUV_1_TIMER_BLOCK
This DDB signal blocks the first stage Phase Undervoltage time delay		
223	V<2 Timer Block	DDB_PUV_2_TIMER_BLOCK
This DDB signal blocks the second stage Phase Undervoltage time delay		
224	V>1 Timer Block	DDB_POV_1_TIMER_BLOCK
This DDB signal blocks the first stage Phase Overvoltage time delay		
225	V>2 Timer Block	DDB_POV_2_TIMER_BLOCK
This DDB signal blocks the second stage Phase Overvoltage time delay		
226	CLP Initiate	DDB_CLP_INITIATE
This DDB signal initiates the CLP operation		
227	Ext. Trip 3ph	DDB_EXTERNAL_TRIP_3PH
This DDB signal receives an external three-phase trip signal		
228	CB Aux 3ph(52-A)	DDB_CB_THREE_PHASE_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of CB)		
229	CB Aux 3ph(52-B)	DDB_CB_THREE_PHASE_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of CB)		
230	CB Healthy	DDB_CB_HEALTHY
This DDB signal indicates that the CB is healthy.		
231	MCB/VTS	DDB_VTS_MCB_OPTO
This DDB signal initiates a VTS condition from a 3phase miniature circuit breaker		
232	Init Trip CB	DDB_LOGIC_INPUT_TRIP
This DDB signals the circuit breaker to open		
233	Init Close CB	DDB_LOGIC_INPUT_CLOSE
This DDB signals the circuit breaker to open		
234	Reset Close Dly	DDB_RESET_CB_CLOSE_DELAY
This DDB signal resets the Manual CB Close Time Delay		
235	Reset Relays/LED	DDB_RESET_RELAYS_LEDS
This DDB resets all latched output relays and LEDs		
236	Reset Thermal	DDB_RESET_THERMAL
This DDB signal resets the Thermal State		
237	Reset Lockout	DDB_RESET_LOCKOUT
This DDB Resets a lockout condition		
238	Reset CB Data	DDB_RESET_ALL_VALUES
This DDB resets the CB Maintenance Values		
239	Block AR	DDB_BLOCK_AR
This DDB signal blocks the Autoreclose function		
240	AR LiveLine Mode	DDB_LIVE_LINE_MODE
This DB indicates that the autoreclose function is in Live Line mode		
241	AR Auto Mode	DDB_AUTO_MODE
This DB indicates that the autoreclose function is in Auto mode		
242	Telecontrol Mode	DDB_TELECONTROL_MODE
This DB indicates that the autoreclose function is in Telecontrol mode		
243	I>1 Trip	DDB_POC_1_3PH_TRIP
This DDB signal is the first stage any-phase Phase Overcurrent trip signal		
244	I>1 Trip A	DDB_POC_1_PH_A_TRIP
This DDB signal is the first stage A-phase Phase Overcurrent trip signal		
245	I>1 Trip B	DDB_POC_1_PH_B_TRIP
This DDB signal is the first stage B-phase Phase Overcurrent trip signal		
246	I>1 Trip C	DDB_POC_1_PH_C_TRIP
This DDB signal is the first stage C-phase Phase Overcurrent trip signal		
247	I>2 Trip	DDB_POC_2_3PH_TRIP
This DDB signal is the second stage any-phase Phase Overcurrent trip signal		
248	I>2 Trip A	DDB_POC_2_PH_A_TRIP
This DDB signal is the second stage A-phase Phase Overcurrent trip signal		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
249	I>2 Trip B	DDB_POC_2_PH_B_TRIP
This DDB signal is the second stage B-phase Phase Overcurrent trip signal		
250	I>2 Trip C	DDB_POC_2_PH_C_TRIP
This DDB signal is the second stage C-phase Phase Overcurrent trip signal		
251	I>3 Trip	DDB_POC_3_3PH_TRIP
This DDB signal is the third stage any-phase Phase Overcurrent trip signal		
252	I>3 Trip A	DDB_POC_3_PH_A_TRIP
This DDB signal is the third stage A-phase Phase Overcurrent trip signal		
253	I>3 Trip B	DDB_POC_3_PH_B_TRIP
This DDB signal is the third stage B-phase Phase Overcurrent trip signal		
254	I>3 Trip C	DDB_POC_3_PH_C_TRIP
This DDB signal is the third stage C-phase Phase Overcurrent trip signal		
255	I>4 Trip	DDB_POC_4_3PH_TRIP
This DDB signal is the fourth stage any-phase Phase Overcurrent trip signal		
256	I>4 Trip A	DDB_POC_4_PH_A_TRIP
This DDB signal is the fourth stage A-phase Phase Overcurrent trip signal		
257	I>4 Trip B	DDB_POC_4_PH_B_TRIP
This DDB signal is the fourth stage B-phase Phase Overcurrent trip signal		
258	I>4 Trip C	DDB_POC_4_PH_C_TRIP
This DDB signal is the fourth stage C-phase Phase Overcurrent trip signal		
259	V Shift Trip	DDB_VSHIFT_TRIP
This DDB signal is the Voltage Vector Shift trip signal		
260	Broken Line Trip	DDB_BROKEN_CONDUCTOR_TRIP
This DDB signal is the Broken Conductor trip signal		
261	IN1>1 Trip	DDB_EF1_1_TRIP
This DDB signal is the first stage measured Earth Fault trip signal		
262	IN1>2 Trip	DDB_EF1_2_TRIP
This DDB signal is the second stage measured Earth Fault trip signal		
263	IN1>3 Trip	DDB_EF1_3_TRIP
This DDB signal is the third stage measured Earth Fault trip signal		
264	IN1>4 Trip	DDB_EF1_4_TRIP
This DDB signal is the fourth stage measured Earth Fault trip signal		
265	IN2>1 Trip	DDB_EF2_1_TRIP
This DDB signal is the first stage derived Earth Fault trip signal		
266	IN2>2 Trip	DDB_EF2_2_TRIP
This DDB signal is the second stage derived Earth Fault trip signal		
267	IN2>3 Trip	DDB_EF2_3_TRIP
This DDB signal is the third stage derived Earth Fault trip signal		
268	IN2>4 Trip	DDB_EF2_4_TRIP
This DDB signal is the fourth stage derived Earth Fault trip signal		
269	ISEF>1 Trip	DDB_SEF_1_TRIP
This DDB signal is the first stage Sensitive Earth Fault trip signal		
270	ISEF>2 Trip	DDB_SEF_2_TRIP
This DDB signal is the second stage Sensitive Earth Fault trip signal		
271	ISEF>3 Trip	DDB_SEF_3_TRIP
This DDB signal is the third stage Sensitive Earth Fault trip signal		
272	ISEF>4 Trip	DDB_SEF_4_TRIP
This DDB signal is the fourth stage Sensitive Earth Fault trip signal		
273	IREF> Trip	DDB_REF_TRIP
This DDB signal is the Restricted Earth Fault trip signal		
274	VN>1 Trip	DDB_RESOV_1_TRIP
This DDB signal is the first stage Residual Overvoltage trip signal		
275	VN>2 Trip	DDB_RESOV_2_TRIP
This DDB signal is the second stage Residual Overvoltage trip signal		
276	Thermal Trip	DDB_THERMAL_TRIP
This DDB signal is the Thermal Overload trip signal		
277	V2> Trip	DDB_NEGSEQOV_TRIP
This DDB signal is the negative Sequence Overvoltage trip signal		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
278	V<1 Trip	DDB_PUV_1_3PH_TRIP
This DDB signal is the first stage three-phase or any-phase Undervoltage trip signal		
279	V<1 Trip A/AB	DDB_PUV_1_PH_A_TRIP
This DDB signal is the first stage A-phase Undervoltage trip signal		
280	V<1 Trip B/BC	DDB_PUV_1_PH_B_TRIP
This DDB signal is the first stage B-phase Undervoltage trip signal		
281	V<1 Trip C/CA	DDB_PUV_1_PH_C_TRIP
This DDB signal is the first stage C-phase Undervoltage trip signal		
282	V<2 Trip	DDB_PUV_2_3PH_TRIP
This DDB signal is the second stage three-phase or any-phase Undervoltage trip signal		
283	V<2 Trip A/AB	DDB_PUV_2_PH_A_TRIP
This DDB signal is the second stage A-phase Undervoltage trip signal		
284	V<2 Trip B/BC	DDB_PUV_2_PH_B_TRIP
This DDB signal is the second stage B-phase Undervoltage trip signal		
285	V<2 Trip C/CA	DDB_PUV_2_PH_C_TRIP
This DDB signal is the second stage C-phase Undervoltage trip signal		
286	V>1 Trip	DDB_POV_1_3PH_TRIP
This DDB signal is the first stage three-phase or any-phase Overvoltage trip signal		
287	V>1 Trip A/AB	DDB_POV_1_PH_A_TRIP
This DDB signal is the first stage A-phase Overvoltage trip signal		
288	V>1 Trip B/BC	DDB_POV_1_PH_B_TRIP
This DDB signal is the first stage B-phase Overvoltage trip signal		
289	V>1 Trip C/CA	DDB_POV_1_PH_C_TRIP
This DDB signal is the first stage C-phase Overvoltage trip signal		
290	V>2 Trip	DDB_POV_2_3PH_TRIP
This DDB signal is the second stage three-phase or any-phase Overvoltage trip signal		
291	V>2 Trip A/AB	DDB_POV_2_PH_A_TRIP
This DDB signal is the second stage A-phase Overvoltage trip signal		
292	V>2 Trip B/BC	DDB_POV_2_PH_B_TRIP
This DDB signal is the second stage B-phase Overvoltage trip signal		
293	V>2 Trip C/CA	DDB_POV_2_PH_C_TRIP
This DDB signal is the second stage C-phase Overvoltage trip signal		
294	Any Start	DDB_ANY_START
This DDB signal is the Any Start signal originating from the fixed scheme logic		
295	I>1 Start	DDB_POC_1_3PH_START
This DDB signal is the first stage any-phase Overcurrent start signal		
296	I>1 Start A	DDB_POC_1_PH_A_START
This DDB signal is the first stage A-phase Overcurrent start signal		
297	I>1 Start B	DDB_POC_1_PH_B_START
This DDB signal is the first stage B-phase Overcurrent start signal		
298	I>1 Start C	DDB_POC_1_PH_C_START
This DDB signal is the first stage C-phase Overcurrent start signal		
299	I>2 Start	DDB_POC_2_3PH_START
This DDB signal is the second stage any-phase Overcurrent start signal		
300	I>2 Start A	DDB_POC_2_PH_A_START
This DDB signal is the second stage A-phase Overcurrent start signal		
301	I>2 Start B	DDB_POC_2_PH_B_START
This DDB signal is the second stage B-phase Overcurrent start signal		
302	I>2 Start C	DDB_POC_2_PH_C_START
This DDB signal is the second stage C-phase Overcurrent start signal		
303	I>3 Start	DDB_POC_3_3PH_START
This DDB signal is the third stage any-phase Overcurrent start signal		
304	I>3 Start A	DDB_POC_3_PH_A_START
This DDB signal is the third stage A-phase Overcurrent start signal		
305	I>3 Start B	DDB_POC_3_PH_B_START
This DDB signal is the third stage B-phase Overcurrent start signal		
306	I>3 Start C	DDB_POC_3_PH_C_START
This DDB signal is the third stage C-phase Overcurrent start signal		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
307	I>4 Start	DDB_POC_4_3PH_START
This DDB signal is the fourth stage any-phase Overcurrent start signal		
308	I>4 Start A	DDB_POC_4_PH_A_START
This DDB signal is the fourth stage A-phase Overcurrent start signal		
309	I>4 Start B	DDB_POC_4_PH_B_START
This DDB signal is the fourth stage B-phase Overcurrent start signal		
310	I>4 Start C	DDB_POC_4_PH_C_START
This DDB signal is the fourth stage C-phase Overcurrent start signal		
311	VDep OC Start AB	DDB_VCO_PH_AB_START
This DDB signal is the Voltage Dependent Overcurrent start signal for phase A-B		
312	VDep OC Start BC	DDB_VCO_PH_BC_START
This DDB signal is the Voltage Dependent Overcurrent start signal for phase B-C		
313	VDep OC Start CA	DDB_VCO_PH_CA_START
This DDB signal is the Voltage Dependent Overcurrent start signal for phase C-A		
315	IN1>1 Start	DDB_EF1_1_START
This DDB signal is the first stage measured Earth Fault start signal		
316	IN1>2 Start	DDB_EF1_2_START
This DDB signal is the second stage measured Earth Fault start signal		
317	IN1>3 Start	DDB_EF1_3_START
This DDB signal is the third stage measured Earth Fault start signal		
318	IN1>4 Start	DDB_EF1_4_START
This DDB signal is the fourth stage measured Earth Fault start signal		
319	IN2>1 Start	DDB_EF2_1_START
This DDB signal is the first stage derived Earth Fault start signal		
320	IN2>2 Start	DDB_EF2_2_START
This DDB signal is the second stage derived Earth Fault start signal		
321	IN2>3 Start	DDB_EF2_3_START
This DDB signal is the third stage derived Earth Fault start signal		
322	IN2>4 Start	DDB_EF2_4_START
This DDB signal is the fourth stage derived Earth Fault start signal		
323	ISEF>1 Start	DDB_SEF_1_START
This DDB signal is the first stage Sensitive Earth Fault start signal		
324	ISEF>2 Start	DDB_SEF_2_START
This DDB signal is the second stage Sensitive Earth Fault start signal		
325	ISEF>3 Start	DDB_SEF_3_START
This DDB signal is the third stage Sensitive Earth Fault start signal		
326	ISEF>4 Start	DDB_SEF_4_START
This DDB signal is the fourth stage Sensitive Earth Fault start signal		
327	VN>1 Start	DDB_RESOV_1_START
This DDB signal is the first stage Residual Overvoltage start signal		
328	VN>2 Start	DDB_RESOV_2_START
This DDB signal is the second stage Residual Overvoltage start signal		
329	Thermal Alarm	DDB_THERMAL_ALARM
This DDB signal is the Thermal Overload start signal		
330	V2> Start	DDB_NEGSEQOV_START
This DDB signal is the Negative Sequence Overvoltage start signal		
331	V<1 Start	DDB_PUV_1_3PH_START
This DDB signal is the first stage three-phase or any-phase Undervoltage start signal		
332	V<1 Start A/AB	DDB_PUV_1_PH_A_START
This DDB signal is the first stage A-phase Phase Undervoltage start signal		
333	V<1 Start B/BC	DDB_PUV_1_PH_B_START
This DDB signal is the first stage B-phase Phase Undervoltage start signal		
334	V<1 Start C/CA	DDB_PUV_1_PH_C_START
This DDB signal is the first stage C-phase Phase Undervoltage start signal		
335	V<2 Start	DDB_PUV_2_3PH_START
This DDB signal is the second stage three-phase or any-phase Undervoltage start signal		
336	V<2 Start A/AB	DDB_PUV_2_PH_A_START
This DDB signal is the second stage A-phase Phase Undervoltage start signal		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
337	V<2 Start B/BC	DDB_PUV_2_PH_B_START
This DDB signal is the second stage B-phase Phase Undervoltage start signal		
338	V<2 Start C/CA	DDB_PUV_2_PH_C_START
This DDB signal is the second stage C-phase Phase Undervoltage start signal		
339	V>1 Start	DDB_POV_1_3PH_START
This DDB signal is the first stage three-phase or any-phase Overvoltage start signal		
340	V>1 Start A/AB	DDB_POV_1_PH_A_START
This DDB signal is the first stage A-phase Phase Overvoltage start signal		
341	V>1 Start B/BC	DDB_POV_1_PH_B_START
This DDB signal is the first stage B-phase Phase Overvoltage start signal		
342	V>1 Start C/CA	DDB_POV_1_PH_C_START
This DDB signal is the first stage C-phase Phase Overvoltage start signal		
343	V>2 Start	DDB_POV_2_3PH_START
This DDB signal is the second stage three-phase or any-phase Overvoltage start signal		
344	V>2 Start A/AB	DDB_POV_2_PH_A_START
This DDB signal is the second stage A-phase Phase Overvoltage start signal		
345	V>2 Start B/BC	DDB_POV_2_PH_B_START
This DDB signal is the second stage B-phase Phase Overvoltage start signal		
346	V>2 Start C/CA	DDB_POV_2_PH_C_START
This DDB signal is the second stage C-phase Phase Overvoltage start signal		
347	CLP Operation	DDB_CLP_OPERATION
This DDB signal indicates that the CLP is operating and informs the Overcurrent protection to use the CLP settings		
348	I> BlockStart	DDB_PH_BLOCKED_OC_START
This DDB signal is the start signal for Blocked Overcurrent functionality		
349	IN/SEF>Blk Start	DDB_N_BLOCKED_OC_START
This DDB signal is the start signal for Blocked Earth Fault functionality		
350	VTS Fast Block	DDB_VTS_FAST_BLOCK
This DDB signal is an instantaneously blocking output from the VTS which can block other functions		
351	VTS Slow Block	DDB_VTS_SLOW_BLOCK
This DDB signal is a purposely delayed output from the VTS which can block other functions		
352	CTS Block	DDB_CTS_BLOCK
This DDB signal is an instantaneously blocking output from the CTS which can block other functions		
353	Bfail1 Trip 3ph	DDB_CBF1_TRIP_3PH
This DDB signal is the three-phase trip signal for the stage 1 CB Fail function		
354	Bfail2 Trip 3ph	DDB_CBF2_TRIP_3PH
This DDB signal is the three-phase trip signal for the stage 2 CB Fail function		
355	Control Trip	DDB_CONTROL_TRIP
This DDB signal tells the CB to trip		
356	Control Close	DDB_CONTROL_CLOSE
This DDB signal tells the CB to close		
357	Close in Prog	DDB_CONTROL_CLOSE_IN_PROGRESS
This DDB signal indicates that CB closure is in progress		
358	AR Blk Main Prot	DDB_AR_BLOCK_MAIN_PROTECTION
This DDB signal, generated by the Autoreclose function, blocks the Main Protection elements (POC, EF1, EF2, NPSOC)		
359	AR Blk SEF Prot	DDB_AR_BLOCK_SEF_PROTECTION
This DDB signal, generated by the Autoreclose function, blocks the SEF Protection element (POC, EF1, EF2, NPSOC)		
360	AR In Progress	DDB_AR_3_POLE_IN_PROGRESS
This DDB signal indicates that three-pole Autoreclose is in progress		
361	AR In Service	DDB_AR_IN_SERVICE
This DDB signal indicates that Autoreclose is in or out of service (auto, or non-auto mode)		
362	AR SeqCounter 0	DDB_SEQ_COUNT_0
This DDB signal indicates that the AR has not been initiated		
363	AR SeqCounter 1	DDB_SEQ_COUNT_1
This DDB signal indicates that the AR function is in its first shot		
364	AR SeqCounter 2	DDB_SEQ_COUNT_2
This DDB signal indicates that the AR function is in its second shot		
365	AR SeqCounter 3	DDB_SEQ_COUNT_3
This DDB signal indicates that the AR function is in its third shot		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
366	AR SeqCounter 4	DDB_SEQ_COUNT_4
This DDB signal indicates that the AR function is in its fourth shot		
367	Successful Close	DDB_AR_SUCCESSFUL_RECLOSE
This DDB signal indicates a successful reclosure		
368	DeadTime in Prog	DDB_DEAD_TIME_IN_PROGRESS
This DDB signal indicates that the Autoreclose dead time is in progress		
369	Protection Lockt	DDB_AR_PROTECTION_LOCKOUT
This DB signal locks out the Autoreclose function		
370	Reset Lckout Alm	DDB_AR_RESET_LOCKOUT_ALARM
This DDB signal indicates that a lockout has been reset.		
371	Auto Close	DDB_AUTO_CLOSE
This DDB signal tells the CB to close, originating from Autoreclose only. This DDB signal has a fixed reset time.		
372	AR Trip Test	DDB_AR_TRIP_TEST
This DDB signal is used to test the Autoreclose function Autoreclose trip test		
373	IA< Start	DDB_PHASE_A_UNDERCURRENT
This DDB signal is the A-phase Phase Undercurrent start signal		
374	IB< Start	DDB_PHASE_B_UNDERCURRENT
This DDB signal is the B-phase Phase Undercurrent start signal		
375	IC< Start	DDB_PHASE_C_UNDERCURRENT
This DDB signal is the C-phase Phase Undercurrent start signal		
376	IN< Start	DDB_EF_UNDERCURRENT
This DDB signal is the Earth Fault undercurrent start signal		
377	ISEF< Start	DDB_SEF_UNDERCURRENT
This DDB signal is the Sensitive Earth Fault undercurrent start signal		
378	CB Open 3 ph	DDB_CB_OPEN
This DDB signal indicates that the CB is open on all 3 phases		
379	CB Closed 3 ph	DDB_CB_CLOSED
This DDB signal indicates that the CB is closed on all 3 phases		
380	All Poles Dead	DDB_ALL_POLEDEAD
This DDB signal indicates that all poles are dead		
381	Any Pole Dead	DDB_ANY_POLEDEAD
This DDB signal indicates that one or more of the poles is dead.		
382	Pole Dead A	DDB_PHASE_A_POLEDEAD
This DDB signal indicates that the A-phase pole is dead.		
383	Pole Dead B	DDB_PHASE_B_POLEDEAD
This DDB signal indicates that the B-phase pole is dead.		
384	Pole Dead C	DDB_PHASE_C_POLEDEAD
This DDB signal indicates that the C-phase pole is dead.		
385	VTS Acc Ind	DDB_VTS_ACCELERATE_INPUT
This DDB signal indicates that the VTS accelerate function is active		
386	VTS Volt Dep	DDB_VTS_ANY_VOLTAGE_DEP_FN
This DDB signal indicates that the Voltage Dependent Overcurrent Protection has started		
387	VTS IA>	DDB_VTS_IA_OPERATED
This DDB signal indicates that phase A current is over threshold (VTS I>Inhibit)		
388	VTS IB>	DDB_VTS_IB_OPERATED
This DDB signal indicates that phase B current is over threshold (VTS I>Inhibit)		
389	VTS IC>	DDB_VTS_IC_OPERATED
This DDB signal indicates that phase C current is over threshold (VTS I>Inhibit)		
390	VTS VA>	DDB_VTS_VA_OPERATED
This DDB signal indicates that phase A voltage is over threshold (VTS Pickup Thresh)		
391	VTS VB>	DDB_VTS_VB_OPERATED
This DDB signal indicates that phase B voltage is over threshold (VTS Pickup Thresh)		
392	VTS VC>	DDB_VTS_VC_OPERATED
This DDB signal indicates that phase C voltage is over threshold (VTS Pickup Thresh)		
393	VTS I2>	DDB_VTS_I2_OPERATED
This DDB signal indicates that negative sequence current is over threshold (VTS I2>Inhibit)		
394	VTS V2>	DDB_VTS_V2_OPERATED
This DDB signal indicates that negative sequence current is over threshold		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
395	VTS IA delta>	DDB_VTS_DELTA_IA_OPERATED
This DDB signal indicates that phase A superimposed current is over threshold (0.1In)		
396	VTS IB delta>	DDB_VTS_DELTA_IB_OPERATED
This DDB signal indicates that phase B superimposed current is over threshold (0.1In)		
397	VTS IC delta>	DDB_VTS_DELTA_IC_OPERATED
This DDB signal indicates that phase C superimposed current is over threshold (0.1In)		
398	CBF SEF Trip	DDB_CURRENT_PROT_SEF_TRIP
This DDB signal is the CBF current protection SEF Trip		
399	CBF Non I Trip	DDB_CBF_NON_CURRENT_PROT_TRIP
This DDB signal is the non-current CBF Protection Trip		
400	CBF SEF Trip-1	DDB_CBF_SEF_STAGE_TRIP
This DDB signal is the Fixed Scheme Logic CBF SEF Stage Trip		
401	CBF Non I Trip-1	DDB_CBF_NON_CURRENT_STAGE_TRIP
This DDB signal is the Fixed Scheme Logic CBF Non Current Protection Stage Trip		
402	Man Check Synch	DDB_SYNC_CTRL_SYS_CHECK_OK
This DDB signal initiates a manual Checks Synch		
403	AR Sys Checks	DDB_SYNC_AR_SYS_CHECK_OK
This DDB signal tells the Autoreclose that the system checks are satisfied.		
404	Lockout Alarm	DDB_CB_LOCKOUT_ALARM
This DDB signal is the Composite circuit breaker Lockout Alarm		
405	Pre-Lockout	DDB_CB_PRE_LOCKOUT
This DDB signal is for CB conditioning and monitoring pre-Lockout. It is related to the number of trips and EFF		
406	Freq High	DDB_FREQ_ABOVE_RANGE_LIMIT
This DDB signal indicates that the frequency is above 70Hz		
407	Freq Low	DDB_FREQ_BELOW_RANGE_LIMIT
This DDB signal indicates that the frequency is below 40Hz		
408	Stop Freq Track	DDB_FREQ_STOP_TRACK
This DDB signal stops frequency Tracking		
409	Start N	DDB_EF_START
This DDB signal is the composite EF Start signal used in the FSL		
411	Freq Not Found	DDB_FREQ_NOT_FOUND
This DDB signal indicates that no frequency has been found		
430	YN> Timer Block	DDB_YN_TIMER_BLOCK
Block Overadmittance Timer		
431	GN> Timer Block	DDB_GN_TIMER_BLOCK
Block Overconductance Timer		
432	BN> Timer Block	DDB_BN_TIMER_BLOCK
Block Oversusceptance Timer		
433	YN> Start	DDB_YN_START
Overadmittance Start		
434	GN> Start	DDB_GN_START
Overconductance Start		
435	BN> Start	DDB_BN_START
Oversusceptance Start		
436	YN> Trip	DDB_YN_TRIP
Overadmittance Trip		
437	GN> Trip	DDB_GN_TRIP
Overconductance Trip		
438	BN> Trip	DDB_BN_TRIP
Oversusceptance Trip		
439	Ext AR Prot Trip	DDB_EXT_AR_PROT_TRIP
This DDB can initiate an Autoreclose sequence from an external trip		
440	Ext AR Prot Strt	DDB_EXT_AR_PROT_START
This DDB informs the Autoreclose function of an external start		
441	Test Mode	DDB_TEST_MODE
This DDB signal initiates the test mode		
442	Inhibit SEF	DDB_SEF_INHIBIT
This DDB signal inhibits Sensitive Earth Fault protection		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
443	Live Line	DDB_SYSCHECKS_LINE_LIVE
This DDB signal indicates a Live Line		
444	Dead Line	DDB_SYSCHECKS_LINE_DEAD
This DDB signal indicates a Dead Line		
445	Live Bus	DDB_SYSCHECKS_BUS_LIVE
This DDB signal indicates a Live Bus		
446	Dead Bus	DDB_SYSCHECKS_BUS_DEAD
This DDB signal indicates a Dead Bus		
447	Check Sync 1 OK	DDB_CHECKSYNC_1_OK
This DDB signal indicates that Check Synchronism stage 1 (CS1) is OK		
448	Check Sync 2 OK	DDB_CHECKSYNC_2_OK
This DDB signal indicates that Check Synchronism stage 2 (CS2) is OK		
449	SysChks Inactive	DDB_SYSCHECKS_INACTIVE
This DDB signal indicates that all System Checks are inactive		
450	CS1 Enabled	DDB_CHECKSYNC_1_ENABLED
This DDB signal enables CS1		
451	CS2 Enabled	DDB_CHECKSYNC_2_ENABLED
This DDB signal enables CS2		
452	SysSplit Enabled	DDB_SYSTEM_SPLIT_ENABLED
This DDB signal enables System Split		
453	DAR Complete	DDB_DAR_COMPLETE
This DDB signal resets the AR in Progress 1 signal		
454	CB in Service	DDB_CB_IN_SERVICE
This DDB signal indicates that the Circuit Breaker is in service		
455	AR Restart	DDB_AR_RESTART
This DDB signal triggers a Restart of the Autoreclose initiation process		
456	DAR In Progress	DDB_AR_IP_1
This DDB signal indicates that delayed Auto-Reclose is in progress		
457	DeadTime Enabled	DDB_DEADTIME_ENABLE
This DDB signal enables the Dead Time timers		
458	DT OK To Start	DDB_DEADTIME_OK_TO_START
This DDB signal tells the AR that it is OK to start the Autoreclose Dead Timer.		
459	DT Complete	DDB_DEADTIME_COMPLETE
This DDB signal indicates that the Autoreclose Dead Time is complete		
460	Reclose Checks	DDB_ARCHECKS_IN_PROGRESS
This DDB signal indicates that Autoreclose system checks are in progress		
461	LiveDead Ccts OK	DDB_AR_LIVEDEAD_CCTS_OK
This DDB informs the AR function that there is a Live/Dead circuit condition		
462	AR Sync Check	DDB_AR_SYNC_CHECK
This DDB signal indicates that the Autoreclose Synchronisation Check is OK		
463	AR SysChecks OK	DDB_AR_SYSTEMCHECKS_OK
This DDB signal indicates that the Autoreclose System Checks are is OK		
464	AR Init TripTest	DDB_INIT_AR_TRIP_TEST
This DDB signal initiates an Autoreclose trip test.		
465	103 MonitorBlock	DDB_MONITOR_BLOCKING
This DDB signal enables the Monitor Blocking for the IEC60870-103 protocol		
466	103 CommandBlock	DDB_COMMAND_BLOCKING
This DDB signal enables the Command Blocking for the IEC60870-103 protocol		
467	ISEF1 Start Watt	DDB_SEF_1_START_2
This signal indicates that the SEF has picked up but not fully satisfied the decision of the Wattmetric SEF		
468	ISEF2 Start Watt	DDB_SEF_2_START_2
This signal indicates that the SEF has picked up but not fully satisfied the decision of the Wattmetric SEF		
469	ISEF3 Start Watt	DDB_SEF_3_START_2
This signal indicates that the SEF has picked up but not fully satisfied the decision of the Wattmetric SEF		
470	ISEF4 Start Watt	DDB_SEF_4_START_2
This signal indicates that the SEF has picked up but not fully satisfied the decision of the Wattmetric SEF		
471	CS1 Slipfreq>	DDB_CS1_SLIP_ABOVE_SETTING
This DDB signal indicates that the CS1 Slip frequency is above the set threshold		

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
472	CS1 Slipfreq<	DDB_CS1_SLIP_BELOW_SETTING
This DDB signal indicates that the CS1 Slip frequency is below the set threshold		
473	CS2 Slipfreq>	DDB_CS2_SLIP_ABOVE_SETTING
This DDB signal indicates that the CS2 Slip frequency is above the set threshold		
474	CS2 Slipfreq<	DDB_CS2_SLIP_BELOW_SETTING
This DDB signal indicates that the CS2 Slip frequency is below the set threshold		
478	I> Inhibit	DDB_POC_INHIBIT
I> Inhibit		
479	VN> Inhibit	DDB_RESOV_INHIBIT
VN> Inhibit		
480	VN> Inhibit	DDB_RESUV_INHIBIT
VN< Inhibit		
480	Block Contacts	DDB_CONTACTS_BLOCKED_IP
Input DDB signal used to drive IED to be contacts blocked If the device has been put into 'Contact Blocked' mode using this input signal then the Apply Test command will not execute. This is to prevent a device that has been blocked by an external process having its contacts operated by a local operator using the HMI. If the Block Contacts DDB is not set and the Apply Test command in is issued, the contacts will change state.		
489	CS Vline<	DDB_SYSCHECKS_VLINE_UV
This DDB signal indicates that the line voltage is less than the Check Synchronism Undervoltage threshold		
490	CS Vbus<	DDB_SYSCHECKS_VBUS_UV
This DDB signal indicates that the bus voltage is less than the Check Synchronism Undervoltage threshold		
491	CS Vline>	DDB_SYSCHECKS_VLINE_OV
This DDB signal indicates that the line voltage is more than the Check Synchronism Overvoltage threshold		
492	CS Vbus>	DDB_SYSCHECKS_VBUS_OV
This DDB signal indicates that the bus voltage is more than the Check Synchronism Overvoltage threshold		
493	CS Vline>Vbus	DDB_SYSCHECKS_VLINE_DIFF_HIGH
This DDB signal indicates that the line voltage is greater than the bus voltage + the CS diff voltage setting		
494	CS Vline<Vbus	DDB_SYSCHECKS_VBUS_DIFF_HIGH
This DDB signal indicates that the bus voltage is greater than the line voltage + the CS diff voltage setting		
495	CS1 Fline>Fbus	DDB_CS1_LINE_FREQ_GT_BUS_FREQ
This DDB signal indicates that the line frequency is greater than the bus frequency + the CS1 slip frequency setting		
496	CS1 Fline<Fbus	DDB_CS1_LINE_FREQ_LT_BUS_FREQ
This DDB signal indicates that the bus frequency is greater than the line frequency + the CS1 slip frequency setting		
497	CS1 Ang Not OK +	DDB_CS1_ANG_NOT_OK_POS
This DDB signal indicates that the line angle has crossed 0 degrees into the 0 to 180 quadrant.		
498	CS1 Ang Not OK -	DDB_CS1_ANG_NOT_OK_NEG
This DDB signal indicates that the line angle has crossed 0 degrees into the 0 to -180 quadrant.		
499	External Trip A	DDB_EXTERNAL_TRIP_A
This DDB signal is connected to an external A-Phase trip, which initiates a CB Fail condition		
500	External Trip B	DDB_EXTERNAL_TRIP_B
This DDB signal is connected to an external B-Phase trip, which initiates a CB Fail condition		
501	External Trip C	DDB_EXTERNAL_TRIP_C
This DDB signal is connected to an external C-Phase Trip, which initiates a CB Fail condition		
502	External Trip EF	DDB_EXTERNAL_TRIP_EF
This DDB signal is connected to an external Earth Fault trip, which initiates a CB Fail condition		
503	External TripSEF	DDB_EXTERNAL_TRIP_SEF
This DDB signal is connected to an external Sensitive Earth Fault trip, which initiates a CB Fail condition		
504	I2> Inhibit	DDB_NPSOC_INHIBIT
This DDB signal inhibits the Negative Phase Overcurrent protection		
505	I2>1 Tmr Blk	DDB_NPSOC_1_TIMER_BLOCK
This DDB signal blocks the first stage Negative Phase Overcurrent timer		
506	I2>2 Tmr Blk	DDB_NPSOC_2_TIMER_BLOCK
This DDB signal blocks the second stage Negative Phase Overcurrent timer		
507	I2>3 Tmr Blk	DDB_NPSOC_3_TIMER_BLOCK
This DDB signal blocks the third stage Negative Phase Overcurrent timer		
508	I2>4 Tmr Blk	DDB_NPSOC_4_TIMER_BLOCK

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal blocks the fourth stage Negative Phase Overcurrent timer		
509	I2>1 Start	DDB_NPSOC_1_START
This DDB signal is the first stage NPSOC start signal		
510	I2>2 Start	DDB_NPSOC_2_START
This DDB signal is the second stage NPSOC start signal		
511	I2>3 Start	DDB_NPSOC_3_START
This DDB signal is the third stage NPSOC start signal		
512	I2>4 Start	DDB_NPSOC_4_START
This DDB signal is the fourth stage NPSOC start signal		
513	I2>1 Trip	DDB_NPSOC_1_TRIP
This DDB signal is the first stage NPSOC trip signal		
514	I2>2 Trip	DDB_NPSOC_2_TRIP
This DDB signal is the second stage NPSOC trip signal		
515	I2>3 Trip	DDB_NPSOC_3_TRIP
This DDB signal is the third stage NPSOC trip signal		
516	I2>4 Trip	DDB_NPSOC_4_TRIP
This DDB signal is the fourth stage NPSOC trip signal		
517	V2> Accelerate	DDB_ACCELERATE_NPSOV
This DDB reduces the pickup delay of the negative sequence overvoltage function.		
518	Trip LED Trigger	DDB_TRIP_LED_TRIGGER
This DDB triggers the fixed trip LED		
519	CS2 Fline>Fbus	DDB_CS2_LINE_FREQ_GT_BUS_FREQ
This DDB signal indicates that the line frequency is greater than the bus frequency + the CS2 slip frequency setting		
520	CS2 Fline<Fbus	DDB_CS2_LINE_FREQ_LT_BUS_FREQ
This DDB signal indicates that the bus frequency is greater than the line frequency + the CS2 slip frequency setting		
521	CS2 Ang Not OK +	DDB_CS2_ANG_NOT_OK_POS
This DDB signal indicates that the line angle has crossed 0 degrees into the 0 to 180 quadrant.		
522	CS2 Ang Not OK -	DDB_CS2_ANG_NOT_OK_NEG
This DDB signal indicates that the line angle has crossed 0 degrees into the 0 to -180 quadrant.		
523	CS Ang Rot ACW	DDB_SYSCHECKS_ANG_ACW
This DDB signal indicates that the Line/Bus phase angle is rotating anti-clockwise		
524	CS Ang Rot CW	DDB_SYSCHECKS_ANG_CW
This DDB signal indicates that the Line/Bus phase angle is rotating clockwise		
525	Blk Rmt. CB Ops	DDB_BLOCK_REMOTE_CB_OPS
This DDB signal blocks remote CB Trip and Close commands.		
526	SG Select x1	DDB_SG_SELECTOR_X1
This DDB signal sets the setting group		
527	SG Select 1x	DDB_SG_SELECTOR_1X
This DDB signal sets the setting group		
528	IN1> Inhibit	DDB_EF1_INHIBIT
This DDB signal inhibits the measured Earth Fault protection		
529	IN2> Inhibit	DDB_EF2_INHIBIT
This DDB signal inhibits the derived Earth Fault protection		
530	AR Skip Shot 1	DDB_AR_SKIP_SHOT_1
This DDB signal forces the Autoreclose function to skip shot 1 of a reclose sequence.		
531	Logic 0 Ref.	DDB_LOGIC_0
This DDB signal is a logic 0 for use in the programmable scheme logic. It never changes state.		
532	Inh Reclaim Time	DDB_AR_INHIBIT_RECLAIM_TIME
This DDB signal inhibits the Autoreclose Reclaim Timer		
533	Reclaim In Prog	DDB_AR_RECLAIM_IN_PROGRESS
This DDB signal indicates that the Autoreclose Reclaim Time is in progress		
534	Reclaim Complete	DDB_AR_RECLAIM_TIME_COMPLETE
This DDB signal indicates that the Autoreclose Reclaim Time is complete		
535	BrokenLine Start	DDB_BROKEN_CONDUCTOR_START
This DDB signal is the Broken Conductor start signal		
536	Trip Command In	DDB_ANY_TRIP
This DDB signal is the Trip Command In signal, which triggers the fixed trip LED and is mapped to the Trip Command Out signal in the FSL.		
537	Trip Command Out	DDB_TRIP_INITIATE

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This is the Trip Command Out signal, which is mapped to the trip relay in the default PSL		
538	IA2H Start	DDB_2ND_HARMONIC_IA
This DDB signal is the A-phase 2nd Harmonic start signal		
539	IB2H Start	DDB_2ND_HARMONIC_IB
This DDB signal is the B-phase 2nd Harmonic start signal		
540	IC2H Start	DDB_2ND_HARMONIC_IC
This DDB signal is the C-phase 2nd Harmonic start signal		
541	I2H Any Start	DDB_2ND_HARMONIC
This DDB signal is the 2nd Harmonic start signal for any phase		
542	RP1 Read Only	DDB_RP1_READ_ONLY
This DDB signal enables Read-only mode for rear port 1 (RP1)		
543	RP2 Read Only	DDB_RP2_READ_ONLY
This DDB signal enables Read-only mode for the optional rear port 2 (RP2)		
544	NIC Read Only	DDB_NIC_READ_ONLY
This DDB signal enables Read-only mode for the optional network interface Card (NIC)		
545	dv/dt1 StartA/AB	DDB_DVDT_1_PH_A_START
This DDB signal is the first stage dv/dt start signal for phase A-N or A-B		
546	dv/dt1 StartB/BC	DDB_DVDT_1_PH_B_START
This DDB signal is the first stage dv/dt start signal for phase B-N or B-C		
547	dv/dt1 StartC/CA	DDB_DVDT_1_PH_C_START
This DDB signal is the first stage dv/dt start signal for phase C-N or C-A		
548	dv/dt1 Start	DDB_DVDT_1_START
This DDB signal is the first stage dv/dt start signal for any phase or three-phase (select with setting).		
549	dv/dt2 StartA/AB	DDB_DVDT_2_PH_A_START
This DDB signal is the second stage dv/dt start signal for phase A-N or A-B		
550	dv/dt2 StartB/BC	DDB_DVDT_2_PH_B_START
This DDB signal is the second stage dv/dt start signal for phase B-N or B-C		
551	dv/dt2 StartC/CA	DDB_DVDT_2_PH_C_START
This DDB signal is the second stage dv/dt start signal for phase C-N or C-A		
552	dv/dt2 Start	DDB_DVDT_2_START
This DDB signal is the second stage dv/dt start signal for any phase or three-phase (select with setting).		
553	dv/dt1 Trip A/AB	DDB_DVDT_1_PH_A_TRIP
This DDB signal is the first stage dv/dt trip signal for phase A-N or A-B		
554	dv/dt1 Trip B/BC	DDB_DVDT_1_PH_B_TRIP
This DDB signal is the first stage dv/dt trip signal for phase B-N or B-C		
555	dv/dt1 Trip C/CA	DDB_DVDT_1_PH_C_TRIP
This DDB signal is the first stage dv/dt trip signal for phase C-N or C-A		
556	dv/dt1 Trip	DDB_DVDT_1_TRIP
This DDB signal is the first stage dv/dt trip signal for any phase or three-phase (select with setting).		
557	dv/dt2 Trip A/AB	DDB_DVDT_2_PH_A_TRIP
This DDB signal is the second stage dv/dt trip signal for phase A-N or A-B		
558	dv/dt2 Trip B/BC	DDB_DVDT_2_PH_B_TRIP
This DDB signal is the second stage dv/dt trip signal for phase B-N or B-C		
559	dv/dt2 Trip C/CA	DDB_DVDT_2_PH_C_TRIP
This DDB signal is the second stage dv/dt trip signal for phase C-N or C-A		
560	dv/dt2 Trip	DDB_DVDT_2_TRIP
This DDB signal is the second stage dv/dt trip signal for any phase or three-phase (select with setting).		
561	dv/dt1 Blocking	DDB_DVDT_1_BLOCK
This DDB signal blocks the first stage dv/dt protection.		
562	dv/dt2 Blocking	DDB_DVDT_2_BLOCK
This DDB signal blocks the second stage dv/dt protection.		
563	ZCD IA<	DDB_PHASE_A_ZCD
This DDB signal indicates an A-phase Undercurrent condition using a zero-crossing method. It is used only to reset CB Fail.		
564	ZCD IB<	DDB_PHASE_B_ZCD
This DDB signal indicates a B-phase Undercurrent condition using a zero-crossing method. It is used only to reset CB Fail.		
565	ZCD IC<	DDB_PHASE_C_ZCD
This DDB signal indicates a C-phase Undercurrent condition using a zero-crossing method. It is used only to reset CB Fail.		
566	ZCD IN<	DDB_EF_ZCD

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal indicates an Earth Fault Undercurrent condition using a zero-crossing method. It is used only to reset CB Fail.		
567	I>5 Timer Block	DDB_POC_5_TIMER_BLOCK
This DDB signal blocks the fifth stage overcurrent time delay		
568	I>6 Timer Block	DDB_POC_6_TIMER_BLOCK
This DDB signal blocks the sixth stage overcurrent time delay		
569	ZCD ISEF<	DDB_SEF_ZCD
This DDB signal indicates a Sensitive Earth Fault Undercurrent condition using a zero-crossing method. It is used only to reset CB Fail.		
570	I>5 Trip	DDB_POC_5_3PH_TRIP
This DDB signal is the fifth stage three-phase Phase Overcurrent trip signal		
571	I>5 Trip A	DDB_POC_5_PH_A_TRIP
This DDB signal is the fifth stage A-phase Phase Overcurrent trip signal		
572	I>5 Trip B	DDB_POC_5_PH_B_TRIP
This DDB signal is the fifth stage B-phase Phase Overcurrent trip signal		
573	I>5 Trip C	DDB_POC_5_PH_C_TRIP
This DDB signal is the fifth stage C-phase Phase Overcurrent trip signal		
574	I>6 Trip	DDB_POC_6_3PH_TRIP
This DDB signal is the sixth stage three-phase Phase Overcurrent trip signal		
575	I>6 Trip A	DDB_POC_6_PH_A_TRIP
This DDB signal is the sixth stage A-phase Phase Overcurrent trip signal		
576	I>6 Trip B	DDB_POC_6_PH_B_TRIP
This DDB signal is the sixth stage B-phase Phase Overcurrent trip signal		
577	I>6 Trip C	DDB_POC_6_PH_C_TRIP
This DDB signal is the sixth stage C-phase Phase Overcurrent trip signal		
579	I>5 Start	DDB_POC_5_3PH_START
This DDB signal is the fifth stage three-phase Phase Overcurrent start signal		
580	I>5 Start A	DDB_POC_5_PH_A_START
This DDB signal is the fifth stage A-phase Phase Overcurrent start signal		
581	I>5 Start B	DDB_POC_5_PH_B_START
This DDB signal is the fifth stage B-phase Phase Overcurrent start signal		
582	I>5 Start C	DDB_POC_5_PH_C_START
This DDB signal is the fifth stage C-phase Phase Overcurrent start signal		
583	I>6 Start	DDB_POC_6_3PH_START
This DDB signal is the sixth stage three-phase Phase Overcurrent start signal		
584	I>6 Start A	DDB_POC_6_PH_A_START
This DDB signal is the sixth stage A-phase Phase Overcurrent start signal		
585	I>6 Start B	DDB_POC_6_PH_B_START
This DDB signal is the sixth stage B-phase Phase Overcurrent start signal		
586	I>6 Start C	DDB_POC_6_PH_C_START
This DDB signal is the sixth stage C-phase Phase Overcurrent start signal		
587	dv/dt3 StartA/AB	DDB_DVDT_3_PH_A_START
This DDB signal is the third stage dv/dt start signal for phase A-N or A-B		
588	dv/dt3 StartB/BC	DDB_DVDT_3_PH_B_START
This DDB signal is the third stage dv/dt start signal for phase B-N or B-C		
589	dv/dt3 StartC/CA	DDB_DVDT_3_PH_C_START
This DDB signal is the third stage dv/dt start signal for phase C-N or C-A		
590	dv/dt3 Start	DDB_DVDT_3_START
This DDB signal is the third stage dv/dt start signal for any phase or three-phase (select with setting).		
591	dv/dt4 StartA/AB	DDB_DVDT_4_PH_A_START
This DDB signal is the fourth stage dv/dt start signal for phase A-N or A-B		
592	dv/dt4 StartB/BC	DDB_DVDT_4_PH_B_START
This DDB signal is the fourth stage dv/dt start signal for phase B-N or B-C		
593	dv/dt4 StartC/CA	DDB_DVDT_4_PH_C_START
This DDB signal is the fourth stage dv/dt start signal for phase C-N or C-A		
594	dv/dt4 Start	DDB_DVDT_4_START
This DDB signal is the fourth stage dv/dt start signal for any phase or three-phase (select with setting).		
595	dv/dt3 Trip A/AB	DDB_DVDT_3_PH_A_TRIP
This DDB signal is the third stage dv/dt trip signal for phase A-N or A-B		
596	dv/dt3 Trip B/BC	DDB_DVDT_3_PH_B_TRIP

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is the third stage dv/dt trip signal for phase B-N or B-C		
597	dv/dt3 Trip C/CA	DDB_DVDT_3_PH_C_TRIP
This DDB signal is the third stage dv/dt trip signal for phase C-N or C-A		
598	dv/dt3 Trip	DDB_DVDT_3_TRIP
This DDB signal is the third stage dv/dt trip signal for any phase or three-phase (select with setting).		
599	dv/dt4 Trip A/AB	DDB_DVDT_4_PH_A_TRIP
This DDB signal is the fourth stage dv/dt trip signal for phase A-N or A-B		
600	dv/dt4 Trip B/BC	DDB_DVDT_4_PH_B_TRIP
This DDB signal is the fourth stage dv/dt trip signal for phase B-N or B-C		
601	dv/dt4 Trip C/CA	DDB_DVDT_4_PH_C_TRIP
This DDB signal is the fourth stage dv/dt trip signal for phase C-N or C-A		
602	dv/dt4 Trip	DDB_DVDT_4_TRIP
This DDB signal is the fourth stage dv/dt trip signal for any phase or three-phase (select with setting).		
603	dv/dt3 Blocking	DDB_DVDT_3_BLOCK
This DDB signal blocks the third stage dv/dt protection.		
604	dv/dt4 Blocking	DDB_DVDT_4_BLOCK
This DDB signal blocks the fourth stage dv/dt protection.		
605	VN>3 Start	DDB_RESOV_3_START
This DDB signal is the third stage Residual Overvoltage start signal		
606	VN>3 Trip	DDB_RESOV_3_TRIP
This DDB signal is the third stage Residual Overvoltage trip signal		
607	VN>3 Timer Blk	DDB_RESOV_3_TIMER_BLOCK
This DDB signal blocks the third stage Residual Overvoltage time delay		
608	V<3 Start	DDB_PUV_3_3PH_START
This DDB signal is the third stage three-phase or any-phase Phase Undervoltage start signal		
609	V<3 Start A/AB	DDB_PUV_3_PH_A_START
This DDB signal is the third stage A-phase Phase Undervoltage start signal		
610	V<3 Start B/BC	DDB_PUV_3_PH_B_START
This DDB signal is the third stage B-phase Phase Undervoltage start signal		
611	V<3 Start C/CA	DDB_PUV_3_PH_C_START
This DDB signal is the third stage C-phase Phase Undervoltage start signal		
612	V<3 Trip	DDB_PUV_3_3PH_TRIP
This DDB signal is the first stage three-phase or any-phase Phase Undervoltage trip signal		
613	V<3 Trip A/AB	DDB_PUV_3_PH_A_TRIP
This DDB signal is the first stage A-phase Phase Undervoltage trip signal		
614	V<3 Trip B/BC	DDB_PUV_3_PH_B_TRIP
This DDB signal is the first stage B-phase Phase Undervoltage trip signal		
615	V<3 Trip C/CA	DDB_PUV_3_PH_C_TRIP
This DDB signal is the first stage C-phase Phase Undervoltage trip signal		
616	V>3 Start	DDB_POV_3_3PH_START
This DDB signal is the third stage three-phase or any-phase Phase Overvoltage start signal		
617	V>3 Start A/AB	DDB_POV_3_PH_A_START
This DDB signal is the third stage A-phase Phase Overvoltage start signal		
618	V>3 Start B/BC	DDB_POV_3_PH_B_START
This DDB signal is the third stage B-phase Phase Overvoltage start signal		
619	V>3 Start C/CA	DDB_POV_3_PH_C_START
This DDB signal is the third stage C-phase Phase Overvoltage start signal		
620	V>3 Trip	DDB_POV_3_3PH_TRIP
This DDB signal is the first stage three-phase or any-phase Phase Overvoltage trip signal		
621	V>3 Trip A/AB	DDB_POV_3_PH_A_TRIP
This DDB signal is the first stage A-phase Phase Overvoltage trip signal		
622	V>3 Trip B/BC	DDB_POV_3_PH_B_TRIP
This DDB signal is the first stage B-phase Phase Overvoltage trip signal		
623	V>3 Trip C/CA	DDB_POV_3_PH_C_TRIP
This DDB signal is the first stage C-phase Phase Overvoltage trip signal		
624	V<3 Timer Block	DDB_PUV_3_TIMER_BLOCK
This DDB signal blocks the third stage Phase Undervoltage time delay		
625	V>3 Timer Block	DDB_POV_3_TIMER_BLOCK

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal blocks the third stage Phase Overvoltage time delay		
626	ISEF> Any Start	DDB_SEF_ANY_START
This DDB signal is the any-phase start signal for SEF		
627	Blinder Inhibit	DDB_POC_LOAD_BLINDER_INHIBIT
This DDB signal inhibits the Load Blinder function		
628	A FWD Blinder	DDB_POC_LOAD_BLINDER_Z_FWD_PH_A
This DDB signal is the Phase A Load Blinder signal for the forward direction		
629	A REV Blinder	DDB_POC_LOAD_BLINDER_Z_REV_PH_A
This DDB signal is the Phase A Load Blinder signal for the reverse direction		
630	A LoadBlinder	DDB_POC_LOAD_BLINDER_Z_PH_A
This DDB signal is the Phase A Load Blinder signal, either direction		
631	B FWD Blinder	DDB_POC_LOAD_BLINDER_Z_FWD_PH_B
This DDB signal is the Phase B Load Blinder signal for the forward direction		
632	B REV Blinder	DDB_POC_LOAD_BLINDER_Z_REV_PH_B
This DDB signal is the Phase B Load Blinder signal for the reverse direction		
633	B LoadBlinder	DDB_POC_LOAD_BLINDER_Z_PH_B
This DDB signal is the Phase B Load Blinder signal, either direction		
634	C FWD Blinder	DDB_POC_LOAD_BLINDER_Z_FWD_PH_C
This DDB signal is the Phase C Load Blinder signal for the forward direction		
635	C REV Blinder	DDB_POC_LOAD_BLINDER_Z_REV_PH_C
This DDB signal is the Phase C Load Blinder signal for the reverse direction		
636	C LoadBlinder	DDB_POC_LOAD_BLINDER_Z_PH_C
This DDB signal is the Phase C Load Blinder signal, either direction		
637	Z1 FWD Blinder	DDB_POC_LOAD_BLINDER_Z1_FWD
This DDB signal is the 3-phase Load Blinder signal for the forward direction		
638	Z1 REV Blinder	DDB_POC_LOAD_BLINDER_Z1_REV
This DDB signal is the 3-phase Load Blinder signal for the reverse direction		
639	Z1 LoadBlinder	DDB_POC_LOAD_BLINDER_Z1
This DDB signal is the 3-phase Load Blinder signal, either direction		
640	LED1 Red	DDB_OUTPUT_TRI_LED_1_RED
DDB signal indicates that the red LED is active		
641	LED1 Grn	DDB_OUTPUT_TRI_LED_1_GRN
DDB signal indicates that the green LED is active		
642	LED2 Red	DDB_OUTPUT_TRI_LED_2_RED
DDB signal indicates that the red LED is active		
643	LED2 Grn	DDB_OUTPUT_TRI_LED_2_GRN
DDB signal indicates that the green LED is active		
644	LED3 Red	DDB_OUTPUT_TRI_LED_3_RED
DDB signal indicates that the red LED is active		
645	LED3 Grn	DDB_OUTPUT_TRI_LED_3_GRN
DDB signal indicates that the green LED is active		
646	LED4 Red	DDB_OUTPUT_TRI_LED_4_RED
DDB signal indicates that the red LED is active		
647	LED4 Grn	DDB_OUTPUT_TRI_LED_4_GRN
DDB signal indicates that the green LED is active		
648	LED5 Red(30TE)	DDB_OUTPUT_TRI_LED_5_RED
DDB signal indicates that the red LED is active		
649	LED5 Grn(30TE)	DDB_OUTPUT_TRI_LED_5_GRN
DDB signal indicates that the green LED is active		
650	LED6 Red(30TE)	DDB_OUTPUT_TRI_LED_6_RED
DDB signal indicates that the red LED is active		
651	LED6 Grn(30TE)	DDB_OUTPUT_TRI_LED_6_GRN
DDB signal indicates that the green LED is active		
652	LED7 Red(30TE)	DDB_OUTPUT_TRI_LED_7_RED
DDB signal indicates that the red LED is active		
653	LED7 Grn(30TE)	DDB_OUTPUT_TRI_LED_7_GRN
DDB signal indicates that the green LED is active		
654	LED8 Red(30TE)	DDB_OUTPUT_TRI_LED_8_RED

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
DDB signal indicates that the red LED is active		
655	LED8 Grn(30TE)	DDB_OUTPUT_TRI_LED_8_GRN
DDB signal indicates that the green LED is active		
656	FnKey LED1 Red	DDB_OUTPUT_TRI_LED_9_RED
DDB signal indicates that the red Function Key LED is active		
657	FnKey LED1 Grn	DDB_OUTPUT_TRI_LED_9_GRN
DDB signal indicates that the green Function Key LED is active		
658	FnKey LED2 Red	DDB_OUTPUT_TRI_LED_10_RED
DDB signal indicates that the red Function Key LED is active		
659	FnKey LED2 Grn	DDB_OUTPUT_TRI_LED_10_GRN
DDB signal indicates that the green Function Key LED is active		
660	FnKey LED3 Red	DDB_OUTPUT_TRI_LED_11_RED
DDB signal indicates that the red Function Key LED is active		
661	FnKey LED3 Grn	DDB_OUTPUT_TRI_LED_11_GRN
DDB signal indicates that the green Function Key LED is active		
676	LED1 Con R	DDB_TRI_LED_RED_CON_1
This DDB signal drives the red LED Conditioner 1		
677	LED1 Con G	DDB_TRI_LED_GRN_CON_1
This DDB signal drives the green LED Conditioner 1		
678	LED2 Con R	DDB_TRI_LED_RED_CON_2
This DDB signal drives the red LED Conditioner 2		
679	LED2 Con G	DDB_TRI_LED_GRN_CON_2
This DDB signal drives the green LED Conditioner 2		
680	LED3 Con R	DDB_TRI_LED_RED_CON_3
This DDB signal drives the red LED Conditioner 3		
681	LED3 Con G	DDB_TRI_LED_GRN_CON_3
This DDB signal drives the green LED Conditioner 3		
682	LED4 Con R	DDB_TRI_LED_RED_CON_4
This DDB signal drives the red LED Conditioner 4		
683	LED4 Con G	DDB_TRI_LED_GRN_CON_4
This DDB signal drives the green LED Conditioner 4		
684	LED5 Con R(30TE)	DDB_TRI_LED_RED_CON_5
This DDB signal drives the red LED Conditioner 5		
685	LED5 Con G(30TE)	DDB_TRI_LED_GRN_CON_5
This DDB signal drives the green LED Conditioner 5		
686	LED6 Con R(30TE)	DDB_TRI_LED_RED_CON_6
This DDB signal drives the red LED Conditioner 6		
687	LED6 Con G(30TE)	DDB_TRI_LED_GRN_CON_6
This DDB signal drives the green LED Conditioner 6		
688	LED7 Con R(30TE)	DDB_TRI_LED_RED_CON_7
This DDB signal drives the red LED Conditioner 7		
689	LED7 Con G(30TE)	DDB_TRI_LED_GRN_CON_7
This DDB signal drives the green LED Conditioner 7		
690	LED8 Con R(30TE)	DDB_TRI_LED_RED_CON_8
This DDB signal drives the red LED Conditioner 8		
691	LED8 Con G(30TE)	DDB_TRI_LED_GRN_CON_8
This DDB signal drives the green LED Conditioner 8		
692	FnKey LED1 ConR	DDB_TRI_LED_RED_CON_9
This DDB signal drives the red Function Key LED Conditioner 1		
693	FnKey LED1 ConG	DDB_TRI_LED_GRN_CON_9
This DDB signal drives the green Function Key LED Conditioner 1		
694	FnKey LED2 ConR	DDB_TRI_LED_RED_CON_10
This DDB signal drives the red Function Key LED Conditioner 2		
695	FnKey LED2 ConG	DDB_TRI_LED_GRN_CON_10
This DDB signal drives the green Function Key LED Conditioner 2		
696	FnKey LED3 ConR	DDB_TRI_LED_RED_CON_11
This DDB signal drives the red Function Key LED Conditioner 3		
697	FnKey LED3 ConG	DDB_TRI_LED_GRN_CON_11

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal drives the red Function Key LED Conditioner 3		
712	Function Key 1	DDB_FN_KEY_1
DDB signal indicates that Function key 1 is active		
713	Function Key 2	DDB_FN_KEY_2
DDB signal indicates that Function key 2 is active		
714	Function Key 3	DDB_FN_KEY_3
DDB signal indicates that Function key 3 is active		
722	Power>1 3PhStart	DDB_OVER_POWER_1_3PH_START
This DDB signal is the first stage three-phase Phase Overpower start signal		
723	Power>1 A Start	DDB_OVER_POWER_1_A_PH_START
This DDB signal is the first stage A-phase Phase Overpower start signal		
724	Power>1 B Start	DDB_OVER_POWER_1_B_PH_START
This DDB signal is the first stage B-phase Phase Overpower start signal		
725	Power>1 C Start	DDB_OVER_POWER_1_C_PH_START
This DDB signal is the first stage C-phase Phase Overpower start signal		
726	Power>2 3PhStart	DDB_OVER_POWER_2_3PH_START
This DDB signal is the second stage three-phase Phase Overpower start signal		
727	Power>2 A Start	DDB_OVER_POWER_2_A_PH_START
This DDB signal is the second stage A-phase Phase Overpower start signal		
728	Power>2 B Start	DDB_OVER_POWER_2_B_PH_START
This DDB signal is the second stage B-phase Phase Overpower start signal		
729	Power>2 C Start	DDB_OVER_POWER_2_C_PH_START
This DDB signal is the second stage C-phase Phase Overpower start signal		
730	Power<1 3PhStart	DDB_UNDER_POWER_1_3PH_START
This DDB signal is the first stage three-phase Phase Underpower start signal		
731	Power<1 A Start	DDB_UNDER_POWER_1_A_PH_START
This DDB signal is the first stage A-phase Phase Underpower start signal		
732	Power<1 B Start	DDB_UNDER_POWER_1_B_PH_START
This DDB signal is the first stage B-phase Phase Underpower start signal		
733	Power<1 C Start	DDB_UNDER_POWER_1_C_PH_START
This DDB signal is the first stage C-phase Phase Underpower start signal		
734	Power<2 3PhStart	DDB_UNDER_POWER_2_3PH_START
This DDB signal is the second stage three-phase Phase Underpower start signal		
735	Power<2 A Start	DDB_UNDER_POWER_2_A_PH_START
This DDB signal is the second stage A-phase Phase Underpower start signal		
736	Power<2 B Start	DDB_UNDER_POWER_2_B_PH_START
This DDB signal is the second stage B-phase Phase Underpower start signal		
737	Power<2 C Start	DDB_UNDER_POWER_2_C_PH_START
This DDB signal is the second stage C-phase Phase Underpower start signal		
738	Power>1 3Ph Trip	DDB_OVER_POWER_1_3PH_TRIP
This DDB signal is the first stage three-phase Phase Overpower trip signal		
739	Power>1 A Trip	DDB_OVER_POWER_1_A_PH_TRIP
This DDB signal is the first stage A-phase Phase Overpower trip signal		
740	Power>1 B Trip	DDB_OVER_POWER_1_B_PH_TRIP
This DDB signal is the first stage B-phase Phase Overpower trip signal		
741	Power>1 C Trip	DDB_OVER_POWER_1_C_PH_TRIP
This DDB signal is the first stage C-phase Phase Overpower trip signal		
742	Power>2 3Ph Trip	DDB_OVER_POWER_2_3PH_TRIP
This DDB signal is the second stage three-phase Phase Overpower trip signal		
743	Power>2 A Trip	DDB_OVER_POWER_2_A_PH_TRIP
This DDB signal is the second stage A-phase Phase Overpower trip signal		
744	Power>2 B Trip	DDB_OVER_POWER_2_B_PH_TRIP
This DDB signal is the second stage B-phase Phase Overpower trip signal		
745	Power>2 C Trip	DDB_OVER_POWER_2_C_PH_TRIP
This DDB signal is the second stage C-phase Phase Overpower trip signal		
746	Power<1 3Ph Trip	DDB_UNDER_POWER_1_3PH_TRIP
This DDB signal is the first stage three-phase Phase Underpower trip signal		
747	Power<1 A Trip	DDB_UNDER_POWER_1_A_PH_TRIP

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is the first stage A-phase Phase Underpower trip signal		
748	Power<1 B Trip	DDB_UNDER_POWER_1_B_PH_TRIP
This DDB signal is the first stage B-phase Phase Underpower trip signal		
749	Power<1 C Trip	DDB_UNDER_POWER_1_C_PH_TRIP
This DDB signal is the first stage C-phase Phase Underpower trip signal		
750	Power<2 3Ph Trip	DDB_UNDER_POWER_2_3PH_TRIP
This DDB signal is the second stage three-phase Phase Underpower trip signal		
751	Power<2 A Trip	DDB_UNDER_POWER_2_A_PH_TRIP
This DDB signal is the second stage A-phase Phase Underpower trip signal		
752	Power<2 B Trip	DDB_UNDER_POWER_2_B_PH_TRIP
This DDB signal is the second stage B-phase Phase Underpower trip signal		
753	Power<2 C Trip	DDB_UNDER_POWER_2_C_PH_TRIP
This DDB signal is the second stage C-phase Phase Underpower trip signal		
754	Power>1 Block	DDB_OVER_POWER_1_BLOCK
This DDB signal blocks the first stage Overpower protection		
755	Power>2 Block	DDB_OVER_POWER_2_BLOCK
This DDB signal blocks the second stage Overpower protection		
756	Power<1 Block	DDB_UNDER_POWER_1_BLOCK
This DDB signal blocks the first stage Underpower protection		
757	Power<2 Block	DDB_UNDER_POWER_2_BLOCK
This DDB signal blocks the second stage Underpower protection		
758	SensP1 Start A	DDB_SPOWER_1_START
This DDB signal is the first stage Sensitive Power protection start signal		
759	SensP2 Start A	DDB_SPOWER_2_START
This DDB signal is the second stage Sensitive Power protection start signal		
760	SensP1 Trip A	DDB_SPOWER_1_TRIP
This DDB signal is the first stage Sensitive Power protection trip signal		
761	SensP2 Trip A	DDB_SPOWER_2_TRIP
This DDB signal is the second stage Sensitive Power protection trip signal		
762	Vdc1 Start	DDB_ZONE_1_VDC_START
This DDB signal is the DC Supply Monitoring Zone 1 Start signal		
763	Vdc2 Start	DDB_ZONE_2_VDC_START
This DDB signal is the DC Supply Monitoring Zone 2 Start signal		
764	Vdc3 Start	DDB_ZONE_3_VDC_START
This DDB signal is the DC Supply Monitoring Zone 3 Start signal		
765	Vdc1 Trip	DDB_ZONE_1_VDC_TRIP
This DDB signal is the DC Supply Monitoring Zone 1 Trip signal		
766	Vdc2 Trip	DDB_ZONE_2_VDC_TRIP
This DDB signal is the DC Supply Monitoring Zone 2 Trip signal		
767	Vdc3 Trip	DDB_ZONE_3_VDC_TRIP
This DDB signal is the DC Supply Monitoring Zone 3 Trip signal		
768	InhibitDC SupMon	DDB_DC_SUPPLY_MON_INHIBIT
This DDB signal is the DC Supply Monitoring Inhibit Signal		
769	DC Supply Fail	DDB_DC_SUPPLY_MON_ALARM
This DDB signal is the DC Supply Monitoring Alarm Signal		
771	GOOSE IED Absent	DDB_GOOSE_MISSING_IED_ALARM
This is a GOOSE alarm indicating that the IED is absent.		
772	NIC Not Fitted	DDB_ECARD_NOT_FITTED_ALARM
This DDB signal indicates that an Ethernet card is not fitted		
773	NIC No Response	DDB_NIC_NOT_RESPONDING_ALARM
This DDB signal indicates that the Ethernet card is not responding		
774	NIC Fatal Error	DDB_NIC_FATAL_ERROR_ALARM
This DDB signal indicates that the Ethernet card has a fatal error		
776	Bad TCP/IP Cfg.	DDB_INVALID_TCP_IP_CONFIG_ALARM
This DDB signal indicates that the TCP/IP configuration is invalid		
778	NIC Link Fail	DDB_NIC_LINK_FAIL_ALARM
This DDB signal indicates that there is a communication failure on the Ethernet card		
779	NIC SW Mis-Match	DDB_SW_MISMATCH_ALARM

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is the main card/Ethernet card software mismatch Alarm		
780	IP Addr Conflict	DDB_IP_ADDRESS_CONFLICT_ALARM
This DDB signal indicates that there is an IP Address conflict		
781	Port A Link Fail	DDB_NIC_LINK_PORT_A_FAIL_ALARM
This DDB signal indicates that Port A has no link		
782	Port B Link Fail	DDB_NIC_LINK_PORT_B_FAIL_ALARM
This DDB signal indicates that Port B has no link		
783	DREB Set.Invalid	DDB_NIC_SETTING_INVALID_ALARM
This DDB signal indicates that the redundancy settings are not valid for this IED model no		
784	VN>4 Start	DDB_RESOV_4_START
This DDB signal is the fourth stage Residual Overvoltage start signal		
785	VN>4 Trip	DDB_RESOV_4_TRIP
This DDB signal is the fourth stage Residual Overvoltage trip signal		
786	VN>4 Timer Blk	DDB_RESOV_4_TIMER_BLOCK
This DDB signal blocks the fourth stage Residual Overvoltage time delay		
787	VN<1 Start	DDB_RESUV_1_START
This DDB signal is the first stage Residual Undervoltage start signal		
788	VN<1 Trip	DDB_RESUV_1_TRIP
This DDB signal is the first stage Residual Undervoltage trip signal		
789	VN<1 Timer Blk	DDB_RESUV_1_TIMER_BLOCK
This DDB signal blocks the first stage Residual Undervoltage time delay		
790	VN<2 Start	DDB_RESUV_2_START
This DDB signal is the second stage Residual Undervoltage start signal		
791	VN<2 Trip	DDB_RESUV_2_TRIP
This DDB signal is the second stage Residual Undervoltage trip signal		
792	VN<2 Timer Blk	DDB_RESUV_2_TIMER_BLOCK
This DDB signal blocks the second stage Residual Undervoltage time delay		
800	Control Input 1	DDB_CONTROL_1
This DDB signal is a control input signal		
801	Control Input 2	DDB_CONTROL_2
This DDB signal is a control input signal		
802	Control Input 3	DDB_CONTROL_3
This DDB signal is a control input signal		
803	Control Input 4	DDB_CONTROL_4
This DDB signal is a control input signal		
804	Control Input 5	DDB_CONTROL_5
This DDB signal is a control input signal		
805	Control Input 6	DDB_CONTROL_6
This DDB signal is a control input signal		
806	Control Input 7	DDB_CONTROL_7
This DDB signal is a control input signal		
807	Control Input 8	DDB_CONTROL_8
This DDB signal is a control input signal		
808	Control Input 9	DDB_CONTROL_9
This DDB signal is a control input signal		
809	Control Input 10	DDB_CONTROL_10
This DDB signal is a control input signal		
810	Control Input 11	DDB_CONTROL_11
This DDB signal is a control input signal		
811	Control Input 12	DDB_CONTROL_12
This DDB signal is a control input signal		
812	Control Input 13	DDB_CONTROL_13
This DDB signal is a control input signal		
813	Control Input 14	DDB_CONTROL_14
This DDB signal is a control input signal		
814	Control Input 15	DDB_CONTROL_15
This DDB signal is a control input signal		
815	Control Input 16	DDB_CONTROL_16

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a control input signal		
816	Control Input 17	DDB_CONTROL_17
This DDB signal is a control input signal		
817	Control Input 18	DDB_CONTROL_18
This DDB signal is a control input signal		
818	Control Input 19	DDB_CONTROL_19
This DDB signal is a control input signal		
819	Control Input 20	DDB_CONTROL_20
This DDB signal is a control input signal		
820	Control Input 21	DDB_CONTROL_21
This DDB signal is a control input signal		
821	Control Input 22	DDB_CONTROL_22
This DDB signal is a control input signal		
822	Control Input 23	DDB_CONTROL_23
This DDB signal is a control input signal		
823	Control Input 24	DDB_CONTROL_24
This DDB signal is a control input signal		
824	Control Input 25	DDB_CONTROL_25
This DDB signal is a control input signal		
825	Control Input 26	DDB_CONTROL_26
This DDB signal is a control input signal		
826	Control Input 27	DDB_CONTROL_27
This DDB signal is a control input signal		
827	Control Input 28	DDB_CONTROL_28
This DDB signal is a control input signal		
828	Control Input 29	DDB_CONTROL_29
This DDB signal is a control input signal		
829	Control Input 30	DDB_CONTROL_30
This DDB signal is a control input signal		
830	Control Input 31	DDB_CONTROL_31
This DDB signal is a control input signal		
831	Control Input 32	DDB_CONTROL_32
This DDB signal is a control input signal		
832	Virtual Input 1	DDB_GOOSEIN_1
This DDB signal is a GOOSE virtual input		
833	Virtual Input 2	DDB_GOOSEIN_2
This DDB signal is a GOOSE virtual input		
834	Virtual Input 3	DDB_GOOSEIN_3
This DDB signal is a GOOSE virtual input		
835	Virtual Input 4	DDB_GOOSEIN_4
This DDB signal is a GOOSE virtual input		
836	Virtual Input 5	DDB_GOOSEIN_5
This DDB signal is a GOOSE virtual input		
837	Virtual Input 6	DDB_GOOSEIN_6
This DDB signal is a GOOSE virtual input		
838	Virtual Input 7	DDB_GOOSEIN_7
This DDB signal is a GOOSE virtual input		
839	Virtual Input 8	DDB_GOOSEIN_8
This DDB signal is a GOOSE virtual input		
840	Virtual Input 9	DDB_GOOSEIN_9
This DDB signal is a GOOSE virtual input		
841	Virtual Input 10	DDB_GOOSEIN_10
This DDB signal is a GOOSE virtual input		
842	Virtual Input 11	DDB_GOOSEIN_11
This DDB signal is a GOOSE virtual input		
843	Virtual Input 12	DDB_GOOSEIN_12
This DDB signal is a GOOSE virtual input		
844	Virtual Input 13	DDB_GOOSEIN_13

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a GOOSE virtual input		
845	Virtual Input 14	DDB_GOOSEIN_14
This DDB signal is a GOOSE virtual input		
846	Virtual Input 15	DDB_GOOSEIN_15
This DDB signal is a GOOSE virtual input		
847	Virtual Input 16	DDB_GOOSEIN_16
This DDB signal is a GOOSE virtual input		
848	Virtual Input 17	DDB_GOOSEIN_17
This DDB signal is a GOOSE virtual input		
849	Virtual Input 18	DDB_GOOSEIN_18
This DDB signal is a GOOSE virtual input		
850	Virtual Input 19	DDB_GOOSEIN_19
This DDB signal is a GOOSE virtual input		
851	Virtual Input 20	DDB_GOOSEIN_20
This DDB signal is a GOOSE virtual input		
852	Virtual Input 21	DDB_GOOSEIN_21
This DDB signal is a GOOSE virtual input		
853	Virtual Input 22	DDB_GOOSEIN_22
This DDB signal is a GOOSE virtual input		
854	Virtual Input 23	DDB_GOOSEIN_23
This DDB signal is a GOOSE virtual input		
855	Virtual Input 24	DDB_GOOSEIN_24
This DDB signal is a GOOSE virtual input		
856	Virtual Input 25	DDB_GOOSEIN_25
This DDB signal is a GOOSE virtual input		
857	Virtual Input 26	DDB_GOOSEIN_26
This DDB signal is a GOOSE virtual input		
858	Virtual Input 27	DDB_GOOSEIN_27
This DDB signal is a GOOSE virtual input		
859	Virtual Input 28	DDB_GOOSEIN_28
This DDB signal is a GOOSE virtual input		
860	Virtual Input 29	DDB_GOOSEIN_29
This DDB signal is a GOOSE virtual input		
861	Virtual Input 30	DDB_GOOSEIN_30
This DDB signal is a GOOSE virtual input		
862	Virtual Input 31	DDB_GOOSEIN_31
This DDB signal is a GOOSE virtual input		
863	Virtual Input 32	DDB_GOOSEIN_32
This DDB signal is a GOOSE virtual input		
864	Virtual Input 33	DDB_GOOSEIN_33
This DDB signal is a GOOSE virtual input		
865	Virtual Input 34	DDB_GOOSEIN_34
This DDB signal is a GOOSE virtual input		
866	Virtual Input 35	DDB_GOOSEIN_35
This DDB signal is a GOOSE virtual input		
867	Virtual Input 36	DDB_GOOSEIN_36
This DDB signal is a GOOSE virtual input		
868	Virtual Input 37	DDB_GOOSEIN_37
This DDB signal is a GOOSE virtual input		
869	Virtual Input 38	DDB_GOOSEIN_38
This DDB signal is a GOOSE virtual input		
870	Virtual Input 39	DDB_GOOSEIN_39
This DDB signal is a GOOSE virtual input		
871	Virtual Input 40	DDB_GOOSEIN_40
This DDB signal is a GOOSE virtual input		
872	Virtual Input 41	DDB_GOOSEIN_41
This DDB signal is a GOOSE virtual input		
873	Virtual Input 42	DDB_GOOSEIN_42

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a GOOSE virtual input		
874	Virtual Input 43	DDB_GOOSEIN_43
This DDB signal is a GOOSE virtual input		
875	Virtual Input 44	DDB_GOOSEIN_44
This DDB signal is a GOOSE virtual input		
876	Virtual Input 45	DDB_GOOSEIN_45
This DDB signal is a GOOSE virtual input		
877	Virtual Input 46	DDB_GOOSEIN_46
This DDB signal is a GOOSE virtual input		
878	Virtual Input 47	DDB_GOOSEIN_47
This DDB signal is a GOOSE virtual input		
879	Virtual Input 48	DDB_GOOSEIN_48
This DDB signal is a GOOSE virtual input		
880	Virtual Input 49	DDB_GOOSEIN_49
This DDB signal is a GOOSE virtual input		
881	Virtual Input 50	DDB_GOOSEIN_50
This DDB signal is a GOOSE virtual input		
882	Virtual Input 51	DDB_GOOSEIN_51
This DDB signal is a GOOSE virtual input		
883	Virtual Input 52	DDB_GOOSEIN_52
This DDB signal is a GOOSE virtual input		
884	Virtual Input 53	DDB_GOOSEIN_53
This DDB signal is a GOOSE virtual input		
885	Virtual Input 54	DDB_GOOSEIN_54
This DDB signal is a GOOSE virtual input		
886	Virtual Input 55	DDB_GOOSEIN_55
This DDB signal is a GOOSE virtual input		
887	Virtual Input 56	DDB_GOOSEIN_56
This DDB signal is a GOOSE virtual input		
888	Virtual Input 57	DDB_GOOSEIN_57
This DDB signal is a GOOSE virtual input		
889	Virtual Input 58	DDB_GOOSEIN_58
This DDB signal is a GOOSE virtual input		
890	Virtual Input 59	DDB_GOOSEIN_59
This DDB signal is a GOOSE virtual input		
891	Virtual Input 60	DDB_GOOSEIN_60
This DDB signal is a GOOSE virtual input		
892	Virtual Input 61	DDB_GOOSEIN_61
This DDB signal is a GOOSE virtual input		
893	Virtual Input 62	DDB_GOOSEIN_62
This DDB signal is a GOOSE virtual input		
894	Virtual Input 63	DDB_GOOSEIN_63
This DDB signal is a GOOSE virtual input		
895	Virtual Input 64	DDB_GOOSEIN_64
This DDB signal is a GOOSE virtual input		
923		DDB_PSLINT_1
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
924		DDB_PSLINT_2
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
925		DDB_PSLINT_3
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
926		DDB_PSLINT_4
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
927		DDB_PSLINT_5
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
928		DDB_PSLINT_6
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
929		DDB_PSLINT_7

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
930		DDB_PSLINT_8
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
931		DDB_PSLINT_9
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
932		DDB_PSLINT_10
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
933		DDB_PSLINT_11
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
934		DDB_PSLINT_12
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
935		DDB_PSLINT_13
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
936		DDB_PSLINT_14
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
937		DDB_PSLINT_15
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
938		DDB_PSLINT_16
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
939		DDB_PSLINT_17
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
940		DDB_PSLINT_18
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
941		DDB_PSLINT_19
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
942		DDB_PSLINT_20
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
943		DDB_PSLINT_21
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
944		DDB_PSLINT_22
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
945		DDB_PSLINT_23
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
946		DDB_PSLINT_24
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
947		DDB_PSLINT_25
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
948		DDB_PSLINT_26
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
949		DDB_PSLINT_27
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
950		DDB_PSLINT_28
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
951		DDB_PSLINT_29
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
952		DDB_PSLINT_30
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
953		DDB_PSLINT_31
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
954		DDB_PSLINT_32
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
955		DDB_PSLINT_33
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
956		DDB_PSLINT_34
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
957		DDB_PSLINT_35
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
958		DDB_PSLINT_36

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
959		DDB_PSLINT_37
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
960		DDB_PSLINT_38
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
961		DDB_PSLINT_39
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
962		DDB_PSLINT_40
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
963		DDB_PSLINT_41
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
964		DDB_PSLINT_42
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
965		DDB_PSLINT_43
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
966		DDB_PSLINT_44
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
967		DDB_PSLINT_45
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
968		DDB_PSLINT_46
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
969		DDB_PSLINT_47
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
970		DDB_PSLINT_48
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
971		DDB_PSLINT_49
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
972		DDB_PSLINT_50
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
973		DDB_PSLINT_51
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
974		DDB_PSLINT_52
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
975		DDB_PSLINT_53
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
976		DDB_PSLINT_54
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
977		DDB_PSLINT_55
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
978		DDB_PSLINT_56
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
979		DDB_PSLINT_57
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
980		DDB_PSLINT_58
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
981		DDB_PSLINT_59
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
982		DDB_PSLINT_60
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
983		DDB_PSLINT_61
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
984		DDB_PSLINT_62
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
985		DDB_PSLINT_63
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
986		DDB_PSLINT_64
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
987		DDB_PSLINT_65

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
988		DDB_PSLINT_66
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
989		DDB_PSLINT_67
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
990		DDB_PSLINT_68
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
991		DDB_PSLINT_69
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
992		DDB_PSLINT_70
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
993		DDB_PSLINT_71
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
994		DDB_PSLINT_72
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
995		DDB_PSLINT_73
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
996		DDB_PSLINT_74
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
997		DDB_PSLINT_75
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
998		DDB_PSLINT_76
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
999		DDB_PSLINT_77
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1000		DDB_PSLINT_78
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1001		DDB_PSLINT_79
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1002		DDB_PSLINT_80
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1003		DDB_PSLINT_81
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1004		DDB_PSLINT_82
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1005		DDB_PSLINT_83
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1006		DDB_PSLINT_84
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1007		DDB_PSLINT_85
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1008		DDB_PSLINT_86
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1009		DDB_PSLINT_87
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1010		DDB_PSLINT_88
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1011		DDB_PSLINT_89
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1012		DDB_PSLINT_90
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1013		DDB_PSLINT_91
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1014		DDB_PSLINT_92
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1015		DDB_PSLINT_93
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1016		DDB_PSLINT_94

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1017		DDB_PSLINT_95
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1018		DDB_PSLINT_96
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1019		DDB_PSLINT_97
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1020		DDB_PSLINT_98
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1021		DDB_PSLINT_99
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1022		DDB_PSLINT_100
This DDB signal is assigned to a PSL node used internally, and is defined by the Programmable Scheme Logic		
1024	Virtual Output 1	DDB_GOOSEOUT_1
This DDB signal is a GOOSE virtual output		
1025	Virtual Output 2	DDB_GOOSEOUT_2
This DDB signal is a GOOSE virtual output		
1026	Virtual Output 3	DDB_GOOSEOUT_3
This DDB signal is a GOOSE virtual output		
1027	Virtual Output 4	DDB_GOOSEOUT_4
This DDB signal is a GOOSE virtual output		
1028	Virtual Output 5	DDB_GOOSEOUT_5
This DDB signal is a GOOSE virtual output		
1029	Virtual Output 6	DDB_GOOSEOUT_6
This DDB signal is a GOOSE virtual output		
1030	Virtual Output 7	DDB_GOOSEOUT_7
This DDB signal is a GOOSE virtual output		
1031	Virtual Output 8	DDB_GOOSEOUT_8
This DDB signal is a GOOSE virtual output		
1032	Virtual Output 9	DDB_GOOSEOUT_9
This DDB signal is a GOOSE virtual output		
1033	Virtual Output10	DDB_GOOSEOUT_10
This DDB signal is a GOOSE virtual output		
1034	Virtual Output11	DDB_GOOSEOUT_11
This DDB signal is a GOOSE virtual output		
1035	Virtual Output12	DDB_GOOSEOUT_12
This DDB signal is a GOOSE virtual output		
1036	Virtual Output13	DDB_GOOSEOUT_13
This DDB signal is a GOOSE virtual output		
1037	Virtual Output14	DDB_GOOSEOUT_14
This DDB signal is a GOOSE virtual output		
1038	Virtual Output15	DDB_GOOSEOUT_15
This DDB signal is a GOOSE virtual output		
1039	Virtual Output16	DDB_GOOSEOUT_16
This DDB signal is a GOOSE virtual output		
1040	Virtual Output17	DDB_GOOSEOUT_17
This DDB signal is a GOOSE virtual output		
1041	Virtual Output18	DDB_GOOSEOUT_18
This DDB signal is a GOOSE virtual output		
1042	Virtual Output19	DDB_GOOSEOUT_19
This DDB signal is a GOOSE virtual output		
1043	Virtual Output20	DDB_GOOSEOUT_20
This DDB signal is a GOOSE virtual output		
1044	Virtual Output21	DDB_GOOSEOUT_21
This DDB signal is a GOOSE virtual output		
1045	Virtual Output22	DDB_GOOSEOUT_22
This DDB signal is a GOOSE virtual output		
1046	Virtual Output23	DDB_GOOSEOUT_23

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a GOOSE virtual output		
1047	Virtual Output24	DDB_GOOSEOUT_24
This DDB signal is a GOOSE virtual output		
1048	Virtual Output25	DDB_GOOSEOUT_25
This DDB signal is a GOOSE virtual output		
1049	Virtual Output26	DDB_GOOSEOUT_26
This DDB signal is a GOOSE virtual output		
1050	Virtual Output27	DDB_GOOSEOUT_27
This DDB signal is a GOOSE virtual output		
1051	Virtual Output28	DDB_GOOSEOUT_28
This DDB signal is a GOOSE virtual output		
1052	Virtual Output29	DDB_GOOSEOUT_29
This DDB signal is a GOOSE virtual output		
1053	Virtual Output30	DDB_GOOSEOUT_30
This DDB signal is a GOOSE virtual output		
1054	Virtual Output31	DDB_GOOSEOUT_31
This DDB signal is a GOOSE virtual output		
1055	Virtual Output32	DDB_GOOSEOUT_32
This DDB signal is a GOOSE virtual output		
1056	Quality VIP 1	DDB_VIP_QUALITY_1
This DDB signal is a GOOSE Virtual input Quality bit		
1057	Quality VIP 2	DDB_VIP_QUALITY_2
This DDB signal is a GOOSE Virtual input Quality bit		
1058	Quality VIP 3	DDB_VIP_QUALITY_3
This DDB signal is a GOOSE Virtual input Quality bit		
1059	Quality VIP 4	DDB_VIP_QUALITY_4
This DDB signal is a GOOSE Virtual input Quality bit		
1060	Quality VIP 5	DDB_VIP_QUALITY_5
This DDB signal is a GOOSE Virtual input Quality bit		
1061	Quality VIP 6	DDB_VIP_QUALITY_6
This DDB signal is a GOOSE Virtual input Quality bit		
1062	Quality VIP 7	DDB_VIP_QUALITY_7
This DDB signal is a GOOSE Virtual input Quality bit		
1063	Quality VIP 8	DDB_VIP_QUALITY_8
This DDB signal is a GOOSE Virtual input Quality bit		
1064	Quality VIP 9	DDB_VIP_QUALITY_9
This DDB signal is a GOOSE Virtual input Quality bit		
1065	Quality VIP 10	DDB_VIP_QUALITY_10
This DDB signal is a GOOSE Virtual input Quality bit		
1066	Quality VIP 11	DDB_VIP_QUALITY_11
This DDB signal is a GOOSE Virtual input Quality bit		
1067	Quality VIP 12	DDB_VIP_QUALITY_12
This DDB signal is a GOOSE Virtual input Quality bit		
1068	Quality VIP 13	DDB_VIP_QUALITY_13
This DDB signal is a GOOSE Virtual input Quality bit		
1069	Quality VIP 14	DDB_VIP_QUALITY_14
This DDB signal is a GOOSE Virtual input Quality bit		
1070	Quality VIP 15	DDB_VIP_QUALITY_15
This DDB signal is a GOOSE Virtual input Quality bit		
1071	Quality VIP 16	DDB_VIP_QUALITY_16
This DDB signal is a GOOSE Virtual input Quality bit		
1072	Quality VIP 17	DDB_VIP_QUALITY_17
This DDB signal is a GOOSE Virtual input Quality bit		
1073	Quality VIP 18	DDB_VIP_QUALITY_18
This DDB signal is a GOOSE Virtual input Quality bit		
1074	Quality VIP 19	DDB_VIP_QUALITY_19
This DDB signal is a GOOSE Virtual input Quality bit		
1075	Quality VIP 20	DDB_VIP_QUALITY_20

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a GOOSE Virtual input Quality bit		
1076	Quality VIP 21	DDB_VIP_QUALITY_21
This DDB signal is a GOOSE Virtual input Quality bit		
1077	Quality VIP 22	DDB_VIP_QUALITY_22
This DDB signal is a GOOSE Virtual input Quality bit		
1078	Quality VIP 23	DDB_VIP_QUALITY_23
This DDB signal is a GOOSE Virtual input Quality bit		
1079	Quality VIP 24	DDB_VIP_QUALITY_24
This DDB signal is a GOOSE Virtual input Quality bit		
1080	Quality VIP 25	DDB_VIP_QUALITY_25
This DDB signal is a GOOSE Virtual input Quality bit		
1081	Quality VIP 26	DDB_VIP_QUALITY_26
This DDB signal is a GOOSE Virtual input Quality bit		
1082	Quality VIP 27	DDB_VIP_QUALITY_27
This DDB signal is a GOOSE Virtual input Quality bit		
1083	Quality VIP 28	DDB_VIP_QUALITY_28
This DDB signal is a GOOSE Virtual input Quality bit		
1084	Quality VIP 29	DDB_VIP_QUALITY_29
This DDB signal is a GOOSE Virtual input Quality bit		
1085	Quality VIP 30	DDB_VIP_QUALITY_30
This DDB signal is a GOOSE Virtual input Quality bit		
1086	Quality VIP 31	DDB_VIP_QUALITY_31
This DDB signal is a GOOSE Virtual input Quality bit		
1087	Quality VIP 32	DDB_VIP_QUALITY_32
This DDB signal is a GOOSE Virtual input Quality bit		
1088	Quality VIP 33	DDB_VIP_QUALITY_33
This DDB signal is a GOOSE Virtual input Quality bit		
1089	Quality VIP 34	DDB_VIP_QUALITY_34
This DDB signal is a GOOSE Virtual input Quality bit		
1090	Quality VIP 35	DDB_VIP_QUALITY_35
This DDB signal is a GOOSE Virtual input Quality bit		
1091	Quality VIP 36	DDB_VIP_QUALITY_36
This DDB signal is a GOOSE Virtual input Quality bit		
1092	Quality VIP 37	DDB_VIP_QUALITY_37
This DDB signal is a GOOSE Virtual input Quality bit		
1093	Quality VIP 38	DDB_VIP_QUALITY_38
This DDB signal is a GOOSE Virtual input Quality bit		
1094	Quality VIP 39	DDB_VIP_QUALITY_39
This DDB signal is a GOOSE Virtual input Quality bit		
1095	Quality VIP 40	DDB_VIP_QUALITY_40
This DDB signal is a GOOSE Virtual input Quality bit		
1096	Quality VIP 41	DDB_VIP_QUALITY_41
This DDB signal is a GOOSE Virtual input Quality bit		
1097	Quality VIP 42	DDB_VIP_QUALITY_42
This DDB signal is a GOOSE Virtual input Quality bit		
1098	Quality VIP 43	DDB_VIP_QUALITY_43
This DDB signal is a GOOSE Virtual input Quality bit		
1099	Quality VIP 44	DDB_VIP_QUALITY_44
This DDB signal is a GOOSE Virtual input Quality bit		
1100	Quality VIP 45	DDB_VIP_QUALITY_45
This DDB signal is a GOOSE Virtual input Quality bit		
1101	Quality VIP 46	DDB_VIP_QUALITY_46
This DDB signal is a GOOSE Virtual input Quality bit		
1102	Quality VIP 47	DDB_VIP_QUALITY_47
This DDB signal is a GOOSE Virtual input Quality bit		
1103	Quality VIP 48	DDB_VIP_QUALITY_48
This DDB signal is a GOOSE Virtual input Quality bit		
1104	Quality VIP 49	DDB_VIP_QUALITY_49

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a GOOSE Virtual input Quality bit		
1105	Quality VIP 50	DDB_VIP_QUALITY_50
This DDB signal is a GOOSE Virtual input Quality bit		
1106	Quality VIP 51	DDB_VIP_QUALITY_51
This DDB signal is a GOOSE Virtual input Quality bit		
1107	Quality VIP 52	DDB_VIP_QUALITY_52
This DDB signal is a GOOSE Virtual input Quality bit		
1108	Quality VIP 53	DDB_VIP_QUALITY_53
This DDB signal is a GOOSE Virtual input Quality bit		
1109	Quality VIP 54	DDB_VIP_QUALITY_54
This DDB signal is a GOOSE Virtual input Quality bit		
1110	Quality VIP 55	DDB_VIP_QUALITY_55
This DDB signal is a GOOSE Virtual input Quality bit		
1111	Quality VIP 56	DDB_VIP_QUALITY_56
This DDB signal is a GOOSE Virtual input Quality bit		
1112	Quality VIP 57	DDB_VIP_QUALITY_57
This DDB signal is a GOOSE Virtual input Quality bit		
1113	Quality VIP 58	DDB_VIP_QUALITY_58
This DDB signal is a GOOSE Virtual input Quality bit		
1114	Quality VIP 59	DDB_VIP_QUALITY_59
This DDB signal is a GOOSE Virtual input Quality bit		
1115	Quality VIP 60	DDB_VIP_QUALITY_60
This DDB signal is a GOOSE Virtual input Quality bit		
1116	Quality VIP 61	DDB_VIP_QUALITY_61
This DDB signal is a GOOSE Virtual input Quality bit		
1117	Quality VIP 62	DDB_VIP_QUALITY_62
This DDB signal is a GOOSE Virtual input Quality bit		
1118	Quality VIP 63	DDB_VIP_QUALITY_63
This DDB signal is a GOOSE Virtual input Quality bit		
1119	Quality VIP 64	DDB_VIP_QUALITY_64
This DDB signal is a GOOSE Virtual input Quality bit		
1120	PubPres VIP 1	DDB_VIP_PUB_PRES_1
GOOSE Virtual input 1 publisher bit		
1121	PubPres VIP 2	DDB_VIP_PUB_PRES_2
GOOSE Virtual input 2 publisher bit		
1122	PubPres VIP 3	DDB_VIP_PUB_PRES_3
GOOSE Virtual input 3 publisher bit		
1123	PubPres VIP 4	DDB_VIP_PUB_PRES_4
GOOSE Virtual input 4 publisher bit		
1124	PubPres VIP 5	DDB_VIP_PUB_PRES_5
GOOSE Virtual input 5 publisher bit		
1125	PubPres VIP 6	DDB_VIP_PUB_PRES_6
GOOSE Virtual input 6 publisher bit		
1126	PubPres VIP 7	DDB_VIP_PUB_PRES_7
GOOSE Virtual input 7 publisher bit		
1127	PubPres VIP 8	DDB_VIP_PUB_PRES_8
GOOSE Virtual input 8 publisher bit		
1128	PubPres VIP 9	DDB_VIP_PUB_PRES_9
GOOSE Virtual input 9 publisher bit		
1129	PubPres VIP 10	DDB_VIP_PUB_PRES_10
GOOSE Virtual input 10 publisher bit		
1130	PubPres VIP 11	DDB_VIP_PUB_PRES_11
GOOSE Virtual input 11 publisher bit		
1131	PubPres VIP 12	DDB_VIP_PUB_PRES_12
GOOSE Virtual input 12 publisher bit		
1132	PubPres VIP 13	DDB_VIP_PUB_PRES_13
GOOSE Virtual input 13 publisher bit		
1133	PubPres VIP 14	DDB_VIP_PUB_PRES_14

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
GOOSE Virtual input 14 publisher bit		
1134	PubPres VIP 15	DDB_VIP_PUB_PRES_15
GOOSE Virtual input 15 publisher bit		
1135	PubPres VIP 16	DDB_VIP_PUB_PRES_16
GOOSE Virtual input 16 publisher bit		
1136	PubPres VIP 17	DDB_VIP_PUB_PRES_17
GOOSE Virtual input 17 publisher bit		
1137	PubPres VIP 18	DDB_VIP_PUB_PRES_18
GOOSE Virtual input 18 publisher bit		
1138	PubPres VIP 19	DDB_VIP_PUB_PRES_19
GOOSE Virtual input 19 publisher bit		
1139	PubPres VIP 20	DDB_VIP_PUB_PRES_20
GOOSE Virtual input 20 publisher bit		
1140	PubPres VIP 21	DDB_VIP_PUB_PRES_21
GOOSE Virtual input 21 publisher bit		
1141	PubPres VIP 22	DDB_VIP_PUB_PRES_22
GOOSE Virtual input 22 publisher bit		
1142	PubPres VIP 23	DDB_VIP_PUB_PRES_23
GOOSE Virtual input 23 publisher bit		
1143	PubPres VIP 24	DDB_VIP_PUB_PRES_24
GOOSE Virtual input 24 publisher bit		
1144	PubPres VIP 25	DDB_VIP_PUB_PRES_25
GOOSE Virtual input 25 publisher bit		
1145	PubPres VIP 26	DDB_VIP_PUB_PRES_26
GOOSE Virtual input 26 publisher bit		
1146	PubPres VIP 27	DDB_VIP_PUB_PRES_27
GOOSE Virtual input 27 publisher bit		
1147	PubPres VIP 28	DDB_VIP_PUB_PRES_28
GOOSE Virtual input 28 publisher bit		
1148	PubPres VIP 29	DDB_VIP_PUB_PRES_29
GOOSE Virtual input 29 publisher bit		
1149	PubPres VIP 30	DDB_VIP_PUB_PRES_30
GOOSE Virtual input 30 publisher bit		
1150	PubPres VIP 31	DDB_VIP_PUB_PRES_31
GOOSE Virtual input 31 publisher bit		
1151	PubPres VIP 32	DDB_VIP_PUB_PRES_32
GOOSE Virtual input 32 publisher bit		
1152	PubPres VIP 33	DDB_VIP_PUB_PRES_33
GOOSE Virtual input 33 publisher bit		
1153	PubPres VIP 34	DDB_VIP_PUB_PRES_34
GOOSE Virtual input 34 publisher bit		
1154	PubPres VIP 35	DDB_VIP_PUB_PRES_35
GOOSE Virtual input 35 publisher bit		
1155	PubPres VIP 36	DDB_VIP_PUB_PRES_36
GOOSE Virtual input 36 publisher bit		
1156	PubPres VIP 37	DDB_VIP_PUB_PRES_37
GOOSE Virtual input 37 publisher bit		
1157	PubPres VIP 38	DDB_VIP_PUB_PRES_38
GOOSE Virtual input 38 publisher bit		
1158	PubPres VIP 39	DDB_VIP_PUB_PRES_39
GOOSE Virtual input 39 publisher bit		
1159	PubPres VIP 40	DDB_VIP_PUB_PRES_40
GOOSE Virtual input 40 publisher bit		
1160	PubPres VIP 41	DDB_VIP_PUB_PRES_41
GOOSE Virtual input 41 publisher bit		
1161	PubPres VIP 42	DDB_VIP_PUB_PRES_42
GOOSE Virtual input 42 publisher bit		
1162	PubPres VIP 43	DDB_VIP_PUB_PRES_43

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
GOOSE Virtual input 43 publisher bit		
1163	PubPres VIP 44	DDB_VIP_PUB_PRES_44
GOOSE Virtual input 44 publisher bit		
1164	PubPres VIP 45	DDB_VIP_PUB_PRES_45
GOOSE Virtual input 45 publisher bit		
1165	PubPres VIP 46	DDB_VIP_PUB_PRES_46
GOOSE Virtual input 46publisher bit		
1166	PubPres VIP 47	DDB_VIP_PUB_PRES_47
GOOSE Virtual input 47 publisher bit		
1167	PubPres VIP 48	DDB_VIP_PUB_PRES_48
GOOSE Virtual input 48 publisher bit		
1168	PubPres VIP 49	DDB_VIP_PUB_PRES_49
GOOSE Virtual input 49 publisher bit		
1169	PubPres VIP 50	DDB_VIP_PUB_PRES_50
GOOSE Virtual input 50 publisher bit		
1170	PubPres VIP 51	DDB_VIP_PUB_PRES_51
GOOSE Virtual input 51 publisher bit		
1171	PubPres VIP 52	DDB_VIP_PUB_PRES_52
GOOSE Virtual input 52 publisher bit		
1172	PubPres VIP 53	DDB_VIP_PUB_PRES_53
GOOSE Virtual input 53 publisher bit		
1173	PubPres VIP 54	DDB_VIP_PUB_PRES_54
GOOSE Virtual input 54 publisher bit		
1174	PubPres VIP 55	DDB_VIP_PUB_PRES_55
GOOSE Virtual input 55 publisher bit		
1175	PubPres VIP 56	DDB_VIP_PUB_PRES_56
GOOSE Virtual input 56 publisher bit		
1176	PubPres VIP 57	DDB_VIP_PUB_PRES_57
GOOSE Virtual input 57 publisher bit		
1177	PubPres VIP 58	DDB_VIP_PUB_PRES_58
GOOSE Virtual input 58 publisher bit		
1178	PubPres VIP 59	DDB_VIP_PUB_PRES_59
GOOSE Virtual input 59 publisher bit		
1179	PubPres VIP 60	DDB_VIP_PUB_PRES_60
GOOSE Virtual input 60 publisher bit		
1180	PubPres VIP 61	DDB_VIP_PUB_PRES_61
GOOSE Virtual input 61 publisher bit		
1181	PubPres VIP 62	DDB_VIP_PUB_PRES_62
GOOSE Virtual input 62 publisher bit		
1182	PubPres VIP 63	DDB_VIP_PUB_PRES_63
GOOSE Virtual input 63 publisher bit		
1183	PubPres VIP 64	DDB_VIP_PUB_PRES_64
GOOSE Virtual input 64 publisher bit		
1184	HMI Access Lvl 1	DDB_UIPASSWORD_ONE
level 1 access for HMI interface		
1185	HMI Access Lvl 2	DDB_UIPASSWORD_TWO
level 2 access for HMI interface		
1186	FPort AccessLvl1	DDB_FCURPASSWORD_ONE
level 1 access for the front port interface		
1187	FPort AccessLvl2	DDB_FCURPASSWORD_TWO
level 2 access for the front port interface		
1188	RPrt1 AccessLvl1	DDB_REMOTEPASSWORD_ONE
level 1 access for the rear port 1 interface		
1189	RPrt1 AccessLvl2	DDB_REMOTEPASSWORD_TWO
level 2 access for the rear port 1 interface		
1190	RPrt2 AccessLvl1	DDB_REMOTE2PASSWORD_ONE
level 1 access for the rear port 2 interface		
1191	RPrt2 AccessLvl2	DDB_REMOTE2PASSWORD_TWO

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
level 2 access for the rear port 2 interface		
1192	HMI Access Lvl 3	DDB_UIPASSWORD_THREE
level 3 access for HMI interface		
1193	FPort AccessLvl3	DDB_FCURPASSWORD_THREE
Level 3 access for the front port interface		
1194	RPrt1 AccessLvl3	DDB_REMOTEPASSWORD_THREE
level 3 access for the rear port 1 interface		
1195	RPrt2 AccessLvl3	DDB_REMOTE2PASSWORD_THREE
level 3 access for the rear port 2 interface		
1200	Monitor bit 1	DDB_MONITOR1
This DDB signal can be assigned to any other DDB for commissioning purposes		
1201	Monitor bit 2	DDB_MONITOR2
This DDB signal can be assigned to any other DDB for commissioning purposes		
1202	Monitor bit 3	DDB_MONITOR3
This DDB signal can be assigned to any other DDB for commissioning purposes		
1203	Monitor bit 4	DDB_MONITOR4
This DDB signal can be assigned to any other DDB for commissioning purposes		
1204	Monitor bit 5	DDB_MONITOR5
This DDB signal can be assigned to any other DDB for commissioning purposes		
1205	Monitor bit 6	DDB_MONITOR6
This DDB signal can be assigned to any other DDB for commissioning purposes		
1206	Monitor bit 7	DDB_MONITOR7
This DDB signal can be assigned to any other DDB for commissioning purposes		
1207	Monitor bit 8	DDB_MONITOR8
This DDB signal can be assigned to any other DDB for commissioning purposes		
1208	HIF Any Start	DDB_HIZ_START
HIF Any Start		
1209	HIF Alarm	DDB_HIZ_ALARM
HIF Alarm = FA HIF || CHA HIF		
1210	FA HIF	DDB_HIZ_FA_HIF
HIF FA detected HIF		
1211	FA Transient	DDB_HIZ_FA_TRANSIENT
HIF FA detected Transient Event		
1212	FA Steady Fault	DDB_HIZ_FA_STEADY
HIF FA detected Steady Event		
1213	CHA HIF	DDB_HIZ_CHA_HIF
HIF CHA detected HIF		
1214	CHA Transient	DDB_HIZ_CHA_TRANSIENT
HIF CHA detected Transient Event		
1215	FA Burst Valid	DDB_HIZ_FA_BURST_VALID
HIF FA Burst Valid Signal		
1216	HIF Forced Reset	DDB_HIZ_RESET
HIF Forced Resetting of all calculation		
1217	CHA SS Valid	DDB_HIZ_CHA_SATISFIED_STATE
HIF CHA Satisfied State		
1218	FA DIR Forward	DDB_HIZ_FORWARD
HIF FA DIR Forward decision		
1219	FA DIR Reverse	DDB_HIZ_REVERSE
HIF FA DIR Reverse decision		
1220	FA IntermitTimer	DDB_FA_INTERMITTENT_COUNTING
FA tINTERMITTENT timer counting		
1221	CHA tDuration	DDB_HIZ_CHA_DURATION_TIMER
1222	CHA tTransient	DDB_HIZ_CHA_TRANSIENT_TIMER
1223	FA Prepare	DDB_FA_PREPARE
1224	FA Ready	DDB_FA_READY

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
1225	FA Start	DDB_FA_START
1226	FA Alarm	DDB_FA_ALARM
1227	CHA Prepare	DDB_CHA_PREPARE
1228	CHA Ready	DDB_CHA_READY
1229	CHA Start	DDB_CHA_START
1230	CHA Alarm	DDB_CHA_ALARM
1231	WDE>1 Trip	DDB_PWH_AVT_1
This DDB signal indicates WDE>1 Trip (AVT=AVal Temporisé)		
1232	WDE>1 Fwd Start	DDB_PWH_AVI_1
This DDB signal indicates WDE>1 forward start (AVI=AVal Instantané)		
1233	WDE>1 Rev Start	DDB_PWH_AMI_1
This DDB signal indicates WDE>1 reverse start (AMI=AMont Instantané)		
1234	WDE>2 Trip	DDB_PWH_AVT_2
This DDB signal indicates WDE>2 Trip (AVT=AVal Temporisé)		
1235	WDE>2 Fwd Start	DDB_PWH_AVI_2
This DDB signal indicates WDE>2 forward start (AVI=AVal Instantané)		
1236	WDE>2 Rev Start	DDB_PWH_AMI_2
This DDB signal indicates WDE>2 reverse start (AMI=AMont Instantané)		
1237	WDE Inhibit	DDB_PWH_INHIBIT
This DDB signal inhibits WDE protection		
1239	WDE Inhib Delay	DDB_PWH_INHIBIT_TEMPO
This DDB signal forces delayed signals (AVT) to act as instantaneous (AVI) (ie as if TAV=0ms)		
1240	Reset Demand	DDB_RESET_DEMAND
This DDB signal resets Demand Period		
1241	WDE>1 Reset	DDB_PWH_1_RESET
WDE>1 Reset		
1242	WDE>2 Reset	DDB_PWH_2_RESET
WDE>2 Reset		
1248	Control Input 33	DDB_CONTROL_33
This DDB signal is a control input signal		
1249	Control Input 34	DDB_CONTROL_34
This DDB signal is a control input signal		
1250	Control Input 35	DDB_CONTROL_35
This DDB signal is a control input signal		
1251	Control Input 36	DDB_CONTROL_36
This DDB signal is a control input signal		
1252	Control Input 37	DDB_CONTROL_37
This DDB signal is a control input signal		
1253	Control Input 38	DDB_CONTROL_38
This DDB signal is a control input signal		
1254	Control Input 39	DDB_CONTROL_39
This DDB signal is a control input signal		
1255	Control Input 40	DDB_CONTROL_40
This DDB signal is a control input signal		
1256	Control Input 41	DDB_CONTROL_41
This DDB signal is a control input signal		
1257	Control Input 42	DDB_CONTROL_42
This DDB signal is a control input signal		
1258	Control Input 43	DDB_CONTROL_43
This DDB signal is a control input signal		
1259	Control Input 44	DDB_CONTROL_44

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is a control input signal		
1260	Control Input 45	DDB_CONTROL_45
This DDB signal is a control input signal		
1261	Control Input 46	DDB_CONTROL_46
This DDB signal is a control input signal		
1262	Control Input 47	DDB_CONTROL_47
This DDB signal is a control input signal		
1263	Control Input 48	DDB_CONTROL_48
This DDB signal is a control input signal		
1264	Control Input 49	DDB_CONTROL_49
This DDB signal is a control input signal		
1265	Control Input 50	DDB_CONTROL_50
This DDB signal is a control input signal		
1266	Control Input 51	DDB_CONTROL_51
This DDB signal is a control input signal		
1267	Control Input 52	DDB_CONTROL_52
This DDB signal is a control input signal		
1268	Control Input 53	DDB_CONTROL_53
This DDB signal is a control input signal		
1269	Control Input 54	DDB_CONTROL_54
This DDB signal is a control input signal		
1270	Control Input 55	DDB_CONTROL_55
This DDB signal is a control input signal		
1271	Control Input 56	DDB_CONTROL_56
This DDB signal is a control input signal		
1272	Control Input 57	DDB_CONTROL_57
This DDB signal is a control input signal		
1273	Control Input 58	DDB_CONTROL_58
This DDB signal is a control input signal		
1274	Control Input 59	DDB_CONTROL_59
This DDB signal is a control input signal		
1275	Control Input 60	DDB_CONTROL_60
This DDB signal is a control input signal		
1276	Control Input 61	DDB_CONTROL_61
This DDB signal is a control input signal		
1277	Control Input 62	DDB_CONTROL_62
This DDB signal is a control input signal		
1278	Control Input 63	DDB_CONTROL_63
This DDB signal is a control input signal		
1279	Control Input 64	DDB_CONTROL_64
This DDB signal is a control input signal		
1280	FreqProt Inhibit	DDB_ADV_FREQ_INHIBIT
This DDB inhibits frequency protection		
1281	Stg1 f+t Sta	DDB_STG1_F_T_START
This DDB signal is the start signal for the first stage Frequency protection element.		
1282	Stg1 f+t Trp	DDB_STG1_F_T_TRIP
This DDB signal is the trip signal for the first stage Frequency protection element.		
1283	Stg1 f+df/dt Trp	DDB_STG1_F_DFDT_TRIP
This DDB signal is the trip signal for the first stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1284	Stg1 df/dt+t Sta	DDB_STG1_DFDT_T_START
This DDB signal is the start signal for the first stage Independent Rate-of-Change-of-Frequency protection element.		
1285	Stg1 df/dt+t Trp	DDB_STG1_DFDT_T_TRIP
This DDB signal is the trip signal for the first stage Independent Rate-of-Change-of-Frequency protection element.		
1286	Stg1 f+Df/Dt Sta	DDB_STG1_F_DELF_DELT_START
This DDB signal is the start signal for the first stage Average Rate-of-Change-of-Frequency protection element.		
1287	Stg1 f+Df/Dt Trp	DDB_STG1_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the first stage Average Rate-of-Change-of-Frequency protection element.		
1288	Stg1 Block	DDB_STG1_ADV_FREQ_BLOCK

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal blocks all first stage Frequency protection elements		
1291	Stg1 Restore Cls	DDB_STG1_RESTORE_CLOSE
This DDB signal closes the first stage Load Restoration		
1292	Stg1 Restore Sta	DDB_STG1_RESTORE_START
This DDB signal starts the first stage Load Restoration		
1295	Stg2 f+t Sta	DDB_STG2_F_T_START
This DDB signal is the start signal for the second stage Frequency protection element.		
1296	Stg2 f+t Trp	DDB_STG2_F_T_TRIP
This DDB signal is the trip signal for the second stage Frequency protection element.		
1297	Stg2 f+df/dt Trp	DDB_STG2_F_DFDT_TRIP
This DDB signal is the trip signal for the second stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1298	Stg2 df/dt+t Sta	DDB_STG2_DFDT_T_START
This DDB signal is the start signal for the second stage Independent Rate-of-Change-of-Frequency protection element.		
1299	Stg2 df/dt+t Trp	DDB_STG2_DFDT_T_TRIP
This DDB signal is the trip signal for the second stage Independent Rate-of-Change-of-Frequency protection element.		
1300	Stg2 f+Df/Dt Sta	DDB_STG2_F_DELF_DELT_START
This DDB signal is the start signal for the second stage Average Rate-of-Change-of-Frequency protection element.		
1301	Stg2 f+Df/Dt Trp	DDB_STG2_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the second stage Average Rate-of-Change-of-Frequency protection element.		
1302	Stg2 Block	DDB_STG2_ADV_FREQ_BLOCK
This DDB signal blocks all second stage Frequency protection elements		
1305	Stg2 Restore Cls	DDB_STG2_RESTORE_CLOSE
This DDB signal closes the second stage Load Restoration		
1306	Stg2 Restore Sta	DDB_STG2_RESTORE_START
This DDB signal starts the second stage Load Restoration		
1309	Stg3 f+t Sta	DDB_STG3_F_T_START
This DDB signal is the start signal for the third stage Frequency protection element.		
1310	Stg3 f+t Trp	DDB_STG3_F_T_TRIP
This DDB signal is the trip signal for the third stage Frequency protection element.		
1311	Stg3 f+df/dt Trp	DDB_STG3_F_DFDT_TRIP
This DDB signal is the trip signal for the third stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1312	Stg3 df/dt+t Sta	DDB_STG3_DFDT_T_START
This DDB signal is the start signal for the third stage Independent Rate-of-Change-of-Frequency protection element.		
1313	Stg3 df/dt+t Trp	DDB_STG3_DFDT_T_TRIP
This DDB signal is the trip signal for the third stage Independent Rate-of-Change-of-Frequency protection element.		
1314	Stg3 f+Df/Dt Sta	DDB_STG3_F_DELF_DELT_START
This DDB signal is the start signal for the third stage Average Rate-of-Change-of-Frequency protection element.		
1315	Stg3 f+Df/Dt Trp	DDB_STG3_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the third stage Average Rate-of-Change-of-Frequency protection element.		
1316	Stg3 Block	DDB_STG3_ADV_FREQ_BLOCK
This DDB signal blocks all third stage Frequency protection elements		
1319	Stg3 Restore Cls	DDB_STG3_RESTORE_CLOSE
This DDB signal closes the third stage Load Restoration		
1320	Stg3 Restore Sta	DDB_STG3_RESTORE_START
This DDB signal starts the third stage Load Restoration		
1323	Stg4 f+t Sta	DDB_STG4_F_T_START
This DDB signal is the start signal for the fourth stage Frequency protection element.		
1324	Stg4 f+t Trp	DDB_STG4_F_T_TRIP
This DDB signal is the trip signal for the fourth stage Frequency protection element.		
1325	Stg4 f+df/dt Trp	DDB_STG4_F_DFDT_TRIP
This DDB signal is the trip signal for the fourth stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1326	Stg4 df/dt+t Sta	DDB_STG4_DFDT_T_START
This DDB signal is the start signal for the fourth stage Independent Rate-of-Change-of-Frequency protection element.		
1327	Stg4 df/dt+t Trp	DDB_STG4_DFDT_T_TRIP
This DDB signal is the trip signal for the fourth stage Independent Rate-of-Change-of-Frequency protection element.		
1328	Stg4 f+Df/Dt Sta	DDB_STG4_F_DELF_DELT_START
This DDB signal is the start signal for the fourth stage Average Rate-of-Change-of-Frequency protection element.		
1329	Stg4 f+Df/Dt Trp	DDB_STG4_F_DELF_DELT_TRIP

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is the trip signal for the fourth stage Average Rate-of-Change-of-Frequency protection element.		
1330	Stg4 Block	DDB_STG4_ADV_FREQ_BLOCK
This DDB signal blocks all fourth stage Frequency protection elements		
1333	Stg4 Restore Cls	DDB_STG4_RESTORE_CLOSE
This DDB signal closes the fourth stage Load Restoration		
1334	Stg4 Restore Sta	DDB_STG4_RESTORE_START
This DDB signal starts the fourth stage Load Restoration		
1337	Stg5 f+t Sta	DDB_STG5_F_T_START
This DDB signal is the start signal for the fifth stage Frequency protection element.		
1338	Stg5 f+t Trp	DDB_STG5_F_T_TRIP
This DDB signal is the trip signal for the fifth stage Frequency protection element.		
1339	Stg5 f+df/dt Trp	DDB_STG5_F_DFDT_TRIP
This DDB signal is the trip signal for the fifth stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1340	Stg5 df/dt+t Sta	DDB_STG5_DFDT_T_START
This DDB signal is the start signal for the fifth stage Independent Rate-of-Change-of-Frequency protection element.		
1341	Stg5 df/dt+t Trp	DDB_STG5_DFDT_T_TRIP
This DDB signal is the trip signal for the fifth stage Independent Rate-of-Change-of-Frequency protection element.		
1342	Stg5 f+Df/Dt Sta	DDB_STG5_F_DELF_DELT_START
This DDB signal is the start signal for the fifth stage Average Rate-of-Change-of-Frequency protection element.		
1343	Stg5 f+Df/Dt Trp	DDB_STG5_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the fifth stage Average Rate-of-Change-of-Frequency protection element.		
1344	Stg5 Block	DDB_STG5_ADV_FREQ_BLOCK
This DDB signal blocks all fifth stage Frequency protection elements		
1347	Stg5 Restore Cls	DDB_STG5_RESTORE_CLOSE
This DDB signal closes the fifth stage Load Restoration		
1348	Stg5 Restore Sta	DDB_STG5_RESTORE_START
This DDB signal starts the fifth stage Load Restoration		
1351	Stg6 f+t Sta	DDB_STG6_F_T_START
This DDB signal is the start signal for the sixth stage Frequency protection element.		
1352	Stg6 f+t Trp	DDB_STG6_F_T_TRIP
This DDB signal is the trip signal for the sixth stage Frequency protection element.		
1353	Stg6 f+df/dt Trp	DDB_STG6_F_DFDT_TRIP
This DDB signal is the trip signal for the sixth stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1354	Stg6 df/dt+t Sta	DDB_STG6_DFDT_T_START
This DDB signal is the start signal for the sixth stage Independent Rate-of-Change-of-Frequency protection element.		
1355	Stg6 df/dt+t Trp	DDB_STG6_DFDT_T_TRIP
This DDB signal is the trip signal for the sixth stage Independent Rate-of-Change-of-Frequency protection element.		
1356	Stg6 f+Df/Dt Sta	DDB_STG6_F_DELF_DELT_START
This DDB signal is the start signal for the sixth stage Average Rate-of-Change-of-Frequency protection element.		
1357	Stg6 f+Df/Dt Trp	DDB_STG6_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the sixth stage Average Rate-of-Change-of-Frequency protection element.		
1358	Stg6 Block	DDB_STG6_ADV_FREQ_BLOCK
This DDB signal blocks all sixth stage Frequency protection elements		
1361	Stg6 Restore Cls	DDB_STG6_RESTORE_CLOSE
This DDB signal closes the sixth stage Load Restoration		
1362	Stg6 Restore Sta	DDB_STG6_RESTORE_START
This DDB signal starts the sixth stage Load Restoration		
1365	Stg7 f+t Sta	DDB_STG7_F_T_START
This DDB signal is the start signal for the seventh stage Frequency protection element.		
1366	Stg7 f+t Trp	DDB_STG7_F_T_TRIP
This DDB signal is the trip signal for the seventh stage Frequency protection element.		
1367	Stg7 f+df/dt Trp	DDB_STG7_F_DFDT_TRIP
This DDB signal is the trip signal for the seventh stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1368	Stg7 df/dt+t Sta	DDB_STG7_DFDT_T_START
This DDB signal is the start signal for the seventh stage Independent Rate-of-Change-of-Frequency protection element.		
1369	Stg7 df/dt+t Trp	DDB_STG7_DFDT_T_TRIP
This DDB signal is the trip signal for the seventh stage Independent Rate-of-Change-of-Frequency protection element.		
1370	Stg7 f+Df/Dt Sta	DDB_STG7_F_DELF_DELT_START

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal is the start signal for the seventh stage Average Rate-of-Change-of-Frequency protection element.		
1371	Stg7 f+Df/Dt Trp	DDB_STG7_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the seventh stage Average Rate-of-Change-of-Frequency protection element.		
1372	Stg7 Block	DDB_STG7_ADV_FREQ_BLOCK
This DDB signal blocks all seventh stage Frequency protection elements		
1375	Stg7 Restore Cls	DDB_STG7_RESTORE_CLOSE
This DDB signal closes the seventh stage Load Restoration		
1376	Stg7 Restore Sta	DDB_STG7_RESTORE_START
This DDB signal starts the seventh stage Load Restoration		
1379	Stg8 f+t Sta	DDB_STG8_F_T_START
This DDB signal is the start signal for the eighth stage Frequency protection element.		
1380	Stg8 f+t Trp	DDB_STG8_F_T_TRIP
This DDB signal is the trip signal for the eighth stage Frequency protection element.		
1381	Stg8 f+df/dt Trp	DDB_STG8_F_DFDT_TRIP
This DDB signal is the trip signal for the eighth stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1382	Stg8 df/dt+t Sta	DDB_STG8_DFDT_T_START
This DDB signal is the start signal for the eighth stage Independent Rate-of-Change-of-Frequency protection element.		
1383	Stg8 df/dt+t Trp	DDB_STG8_DFDT_T_TRIP
This DDB signal is the trip signal for the eighth stage Independent Rate-of-Change-of-Frequency protection element.		
1384	Stg8 f+Df/Dt Sta	DDB_STG8_F_DELF_DELT_START
This DDB signal is the start signal for the eighth stage Average Rate-of-Change-of-Frequency protection element.		
1385	Stg8 f+Df/Dt Trp	DDB_STG8_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the eighth stage Average Rate-of-Change-of-Frequency protection element.		
1386	Stg8 Block	DDB_STG8_ADV_FREQ_BLOCK
This DDB signal blocks all eighth stage Frequency protection elements		
1389	Stg8 Restore Cls	DDB_STG8_RESTORE_CLOSE
This DDB signal closes the eighth stage Load Restoration		
1390	Stg8 Restore Sta	DDB_STG8_RESTORE_START
This DDB signal starts the eighth stage Load Restoration		
1393	Stg9 f+t Sta	DDB_STG9_F_T_START
This DDB signal is the start signal for the ninth stage Frequency protection element.		
1394	Stg9 f+t Trp	DDB_STG9_F_T_TRIP
This DDB signal is the trip signal for the ninth stage Frequency protection element.		
1395	Stg9 f+df/dt Trp	DDB_STG9_F_DFDT_TRIP
This DDB signal is the trip signal for the ninth stage Frequency-Supervised Rate-of-Change-of-Frequency protection element.		
1396	Stg9 df/dt+t Sta	DDB_STG9_DFDT_T_START
This DDB signal is the start signal for the ninth stage Independent Rate-of-Change-of-Frequency protection element.		
1397	Stg9 df/dt+t Trp	DDB_STG9_DFDT_T_TRIP
This DDB signal is the trip signal for the ninth stage Independent Rate-of-Change-of-Frequency protection element.		
1398	Stg9 f+Df/Dt Sta	DDB_STG9_F_DELF_DELT_START
This DDB signal is the start signal for the ninth stage Average Rate-of-Change-of-Frequency protection element.		
1399	Stg9 f+Df/Dt Trp	DDB_STG9_F_DELF_DELT_TRIP
This DDB signal is the trip signal for the ninth stage Average Rate-of-Change-of-Frequency protection element.		
1400	Stg9 Block	DDB_STG9_ADV_FREQ_BLOCK
This DDB signal blocks all ninth stage Frequency protection elements		
1403	Stg9 Restore Cls	DDB_STG9_RESTORE_CLOSE
This DDB signal closes the ninth stage Load Restoration		
1404	Stg9 Restore Sta	DDB_STG9_RESTORE_START
This DDB signal starts the ninth stage Load Restoration		
1405	Restore Reset	DDB_RESTORE_RESET
This DDB signal resets all Load Restoration stages		
1406	Reset Stats	DDB_RESET_STATISTICS
This DDB signal resets all statistics counters		
1409	REF IN< Op	DDB_REF_NEUT_UC
Ref In Under 80% of Is1 Operate		
1410	REF Block	DDB_REF_BLOCK
Blocks Ref		
1450	User Alarm in 1	DDB_USER_ALARM_INPUT_1

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
User Alarm		
1451	User Alarm in 2	DDB_USER_ALARM_INPUT_2
User Alarm		
1452	User Alarm in 3	DDB_USER_ALARM_INPUT_3
User Alarm		
1453	User Alarm in 4	DDB_USER_ALARM_INPUT_4
User Alarm		
1454	User Alarm in 5	DDB_USER_ALARM_INPUT_5
User Alarm		
1455	User Alarm in 6	DDB_USER_ALARM_INPUT_6
User Alarm		
1456	User Alarm in 7	DDB_USER_ALARM_INPUT_7
User Alarm		
1457	User Alarm in 8	DDB_USER_ALARM_INPUT_8
User Alarm		
1458	User Alarm in 9	DDB_USER_ALARM_INPUT_9
User Alarm		
1459	User Alarm in 10	DDB_USER_ALARM_INPUT_10
User Alarm		
1460	User Alarm in 11	DDB_USER_ALARM_INPUT_11
User Alarm		
1461	User Alarm in 12	DDB_USER_ALARM_INPUT_12
User Alarm		
1462	User Alarm in 13	DDB_USER_ALARM_INPUT_13
User Alarm		
1463	User Alarm in 14	DDB_USER_ALARM_INPUT_14
User Alarm		
1464	User Alarm in 15	DDB_USER_ALARM_INPUT_15
User Alarm		
1465	User Alarm in 16	DDB_USER_ALARM_INPUT_16
User Alarm		
1466	User Alarm in 17	DDB_USER_ALARM_INPUT_17
User Alarm		
1467	User Alarm in 18	DDB_USER_ALARM_INPUT_18
User Alarm		
1468	User Alarm in 19	DDB_USER_ALARM_INPUT_19
User Alarm		
1469	User Alarm in 20	DDB_USER_ALARM_INPUT_20
User Alarm		
1470	User Alarm in 21	DDB_USER_ALARM_INPUT_21
User Alarm		
1471	User Alarm in 22	DDB_USER_ALARM_INPUT_22
User Alarm		
1472	User Alarm in 23	DDB_USER_ALARM_INPUT_23
User Alarm		
1473	User Alarm in 24	DDB_USER_ALARM_INPUT_24
User Alarm		
1474	User Alarm in 25	DDB_USER_ALARM_INPUT_25
User Alarm		
1475	User Alarm in 26	DDB_USER_ALARM_INPUT_26
User Alarm		
1476	User Alarm in 27	DDB_USER_ALARM_INPUT_27
User Alarm		
1477	User Alarm in 28	DDB_USER_ALARM_INPUT_28
User Alarm		
1478	User Alarm in 29	DDB_USER_ALARM_INPUT_29
User Alarm		
1479	User Alarm in 30	DDB_USER_ALARM_INPUT_30

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
User Alarm		
1480	User Alarm in 31	DDB_USER_ALARM_INPUT_31
User Alarm		
1481	User Alarm in 32	DDB_USER_ALARM_INPUT_32
User Alarm		
1599		DDB_PSLINT_101
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1600		DDB_PSLINT_102
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1601		DDB_PSLINT_103
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1602		DDB_PSLINT_104
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1603		DDB_PSLINT_105
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1604		DDB_PSLINT_106
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1605		DDB_PSLINT_107
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1606		DDB_PSLINT_108
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1607		DDB_PSLINT_109
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1608		DDB_PSLINT_110
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1609		DDB_PSLINT_111
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1610		DDB_PSLINT_112
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1611		DDB_PSLINT_113
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1612		DDB_PSLINT_114
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1613		DDB_PSLINT_115
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1614		DDB_PSLINT_116
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1615		DDB_PSLINT_117
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1616		DDB_PSLINT_118
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1617		DDB_PSLINT_119
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1618		DDB_PSLINT_120
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1619		DDB_PSLINT_121
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1620		DDB_PSLINT_122
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1621		DDB_PSLINT_123
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1622		DDB_PSLINT_124
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1623		DDB_PSLINT_125
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1624		DDB_PSLINT_126
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1625		DDB_PSLINT_127

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1626		DDB_PSLINT_128
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1627		DDB_PSLINT_129
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1628		DDB_PSLINT_130
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1629		DDB_PSLINT_131
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1630		DDB_PSLINT_132
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1631		DDB_PSLINT_133
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1632		DDB_PSLINT_134
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1633		DDB_PSLINT_135
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1634		DDB_PSLINT_136
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1635		DDB_PSLINT_137
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1636		DDB_PSLINT_138
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1637		DDB_PSLINT_139
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1638		DDB_PSLINT_140
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1639		DDB_PSLINT_141
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1640		DDB_PSLINT_142
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1641		DDB_PSLINT_143
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1642		DDB_PSLINT_144
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1643		DDB_PSLINT_145
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1644		DDB_PSLINT_146
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1645		DDB_PSLINT_147
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1646		DDB_PSLINT_148
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1647		DDB_PSLINT_149
This DDB signal can be defined by the user in the Programmmable Scheme Logic		
1648		DDB_PSLINT_150
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1649		DDB_PSLINT_151
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1650		DDB_PSLINT_152
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1651		DDB_PSLINT_153
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1652		DDB_PSLINT_154
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1653		DDB_PSLINT_155
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1654		DDB_PSLINT_156

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1655		DDB_PSLINT_157
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1656		DDB_PSLINT_158
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1657		DDB_PSLINT_159
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1658		DDB_PSLINT_160
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1659		DDB_PSLINT_161
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1660		DDB_PSLINT_162
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1661		DDB_PSLINT_163
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1662		DDB_PSLINT_164
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1663		DDB_PSLINT_165
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1664		DDB_PSLINT_166
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1665		DDB_PSLINT_167
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1666		DDB_PSLINT_168
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1667		DDB_PSLINT_169
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1668		DDB_PSLINT_170
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1669		DDB_PSLINT_171
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1670		DDB_PSLINT_172
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1671		DDB_PSLINT_173
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1672		DDB_PSLINT_174
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1673		DDB_PSLINT_175
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1674		DDB_PSLINT_176
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1675		DDB_PSLINT_177
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1676		DDB_PSLINT_178
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1677		DDB_PSLINT_179
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1678		DDB_PSLINT_180
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1679		DDB_PSLINT_181
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1680		DDB_PSLINT_182
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1681		DDB_PSLINT_183
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1682		DDB_PSLINT_184
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1683		DDB_PSLINT_185

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1684		DDB_PSLINT_186
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1685		DDB_PSLINT_187
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1686		DDB_PSLINT_188
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1687		DDB_PSLINT_189
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1688		DDB_PSLINT_190
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1689		DDB_PSLINT_191
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1690		DDB_PSLINT_192
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1691		DDB_PSLINT_193
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1692		DDB_PSLINT_194
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1693		DDB_PSLINT_195
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1694		DDB_PSLINT_196
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1695		DDB_PSLINT_197
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1696		DDB_PSLINT_198
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1697		DDB_PSLINT_199
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1698		DDB_PSLINT_200
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1699		DDB_PSLINT_201
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1700		DDB_PSLINT_202
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1701		DDB_PSLINT_203
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1702		DDB_PSLINT_204
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1703		DDB_PSLINT_205
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1704		DDB_PSLINT_206
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1705		DDB_PSLINT_207
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1706		DDB_PSLINT_208
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1707		DDB_PSLINT_209
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1708		DDB_PSLINT_210
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1709		DDB_PSLINT_211
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1710		DDB_PSLINT_212
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1711		DDB_PSLINT_213
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1712		DDB_PSLINT_214

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1713		DDB_PSLINT_215
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1714		DDB_PSLINT_216
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1715		DDB_PSLINT_217
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1716		DDB_PSLINT_218
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1717		DDB_PSLINT_219
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1718		DDB_PSLINT_220
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1719		DDB_PSLINT_221
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1720		DDB_PSLINT_222
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1721		DDB_PSLINT_223
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1722		DDB_PSLINT_224
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1723		DDB_PSLINT_225
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1724		DDB_PSLINT_226
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1725		DDB_PSLINT_227
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1726		DDB_PSLINT_228
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1727		DDB_PSLINT_229
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1728		DDB_PSLINT_230
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1729		DDB_PSLINT_231
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1730		DDB_PSLINT_232
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1731		DDB_PSLINT_233
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1732		DDB_PSLINT_234
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1733		DDB_PSLINT_235
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1734		DDB_PSLINT_236
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1735		DDB_PSLINT_237
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1736		DDB_PSLINT_238
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1737		DDB_PSLINT_239
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1738		DDB_PSLINT_240
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1739		DDB_PSLINT_241
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1740		DDB_PSLINT_242
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1741		DDB_PSLINT_243

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1742		DDB_PSLINT_244
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1743		DDB_PSLINT_245
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1744		DDB_PSLINT_246
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1745		DDB_PSLINT_247
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1746		DDB_PSLINT_248
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1747		DDB_PSLINT_249
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1748		DDB_PSLINT_250
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1749		DDB_PSLINT_251
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1750		DDB_PSLINT_252
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1751		DDB_PSLINT_253
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1752		DDB_PSLINT_254
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1753		DDB_PSLINT_255
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1754		DDB_PSLINT_256
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1755		DDB_PSLINT_257
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1756		DDB_PSLINT_258
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1757		DDB_PSLINT_259
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1758		DDB_PSLINT_260
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1759		DDB_PSLINT_261
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1760		DDB_PSLINT_262
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1761		DDB_PSLINT_263
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1762		DDB_PSLINT_264
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1763		DDB_PSLINT_265
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1764		DDB_PSLINT_266
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1765		DDB_PSLINT_267
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1766		DDB_PSLINT_268
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1767		DDB_PSLINT_269
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1768		DDB_PSLINT_270
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1769		DDB_PSLINT_271
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1770		DDB_PSLINT_272

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1771		DDB_PSLINT_273
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1772		DDB_PSLINT_274
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1773		DDB_PSLINT_275
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1774		DDB_PSLINT_276
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1775		DDB_PSLINT_277
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1776		DDB_PSLINT_278
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1777		DDB_PSLINT_279
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1778		DDB_PSLINT_280
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1779		DDB_PSLINT_281
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1780		DDB_PSLINT_282
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1781		DDB_PSLINT_283
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1782		DDB_PSLINT_284
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1783		DDB_PSLINT_285
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1784		DDB_PSLINT_286
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1785		DDB_PSLINT_287
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1786		DDB_PSLINT_288
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1787		DDB_PSLINT_289
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1788		DDB_PSLINT_290
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1789		DDB_PSLINT_291
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1790		DDB_PSLINT_292
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1791		DDB_PSLINT_293
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1792		DDB_PSLINT_294
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1793		DDB_PSLINT_295
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1794		DDB_PSLINT_296
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1795		DDB_PSLINT_297
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1796		DDB_PSLINT_298
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1797		DDB_PSLINT_299
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1798		DDB_PSLINT_300
This DDB signal can be defined by the user in the Programmable Scheme Logic		
1799	Vavg<1 Start	DDB_AVG_UV_1_3PH_START

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
1st Stage Avg Phase U/V Start 3ph		
1800	Vavg<1 Start A	DDB_AVG_UV_1_PH_A_START
1st Stage Avg Phase U/V Start A		
1801	Vavg<1 Start B	DDB_AVG_UV_1_PH_B_START
1st Stage Avg Phase U/V Start B		
1802	Vavg<1 Start C	DDB_AVG_UV_1_PH_C_START
1st Stage Avg Phase U/V Start C		
1803	Vavg<2 Start	DDB_AVG_UV_2_3PH_START
2nd Stage Avg Phase U/V Start 3ph		
1804	Vavg<2 Start A	DDB_AVG_UV_2_PH_A_START
2nd Stage Avg Phase U/V Start A		
1805	Vavg<2 Start B	DDB_AVG_UV_2_PH_B_START
2nd Stage Avg Phase U/V Start B		
1806	Vavg<2 Start C	DDB_AVG_UV_2_PH_C_START
2nd Stage Avg Phase U/V Start C		
1807	Vavg>1 Start	DDB_AVG_OV_1_3PH_START
1st Stage Avg Phase O/V Start 3ph		
1808	Vavg>1 Start A	DDB_AVG_OV_1_PH_A_START
1st Stage Avg Phase O/V Start A		
1809	Vavg>1 Start B	DDB_AVG_OV_1_PH_B_START
1st Stage Avg Phase O/V Start B		
1810	Vavg>1 Start C	DDB_AVG_OV_1_PH_C_START
1st Stage Avg Phase O/V Start C		
1811	Vavg>2 Start	DDB_AVG_OV_2_3PH_START
2nd Stage Avg Phase O/V Start 3ph		
1812	Vavg>2 Start A	DDB_AVG_OV_2_PH_A_START
2nd Stage Avg Phase O/V Start A		
1813	Vavg>2 Start B	DDB_AVG_OV_2_PH_B_START
2nd Stage Avg Phase O/V Start B		
1814	Vavg>2 Start C	DDB_AVG_OV_2_PH_C_START
2nd Stage Avg Phase O/V Start C		
1815	V0avg>1 Start	DDB_AVG_V0_1_START
1st Stage Avg Zero Seq O/V Start		
1816	V0avg>2 Start	DDB_AVG_V0_2_START
2nd Stage Avg Zero Seq O/V Start		
1817	V1avg>1 Start	DDB_AVG_V1_1_START
1st Stage Avg Pos Seq O/V Start		
1818	V1avg>2 Start	DDB_AVG_V1_2_START
2nd Stage Avg Pos Seq O/V Start		
1819	V2avg>1 Start	DDB_AVG_V2_1_START
1st Stage Avg Neg Seq O/V Start		
1820	V2avg>2 Start	DDB_AVG_V2_2_START
2nd Stage Avg Neg Seq O/V Start		
1821	Vavg<1 Trip	DDB_AVG_UV_1_3PH_TRIP
1st Stage Avg Phase U/V Trip 3ph		
1822	Vavg<1 Trip A	DDB_AVG_UV_1_PH_A_TRIP
1st Stage Avg Phase U/V Trip A		
1823	Vavg<1 Trip B	DDB_AVG_UV_1_PH_B_TRIP
1st Stage Avg Phase U/V Trip B		
1824	Vavg<1 Trip C	DDB_AVG_UV_1_PH_C_TRIP
1st Stage Avg Phase U/V Trip C		
1825	Vavg<2 Trip	DDB_AVG_UV_2_3PH_TRIP
2nd Stage Avg Phase U/V Trip 3ph		
1826	Vavg<2 Trip A	DDB_AVG_UV_2_PH_A_TRIP
2nd Stage Avg Phase U/V Trip A		
1827	Vavg<2 Trip B	DDB_AVG_UV_2_PH_B_TRIP
2nd Stage Avg Phase U/V Trip B		
1828	Vavg<2 Trip C	DDB_AVG_UV_2_PH_C_TRIP

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
2nd Stage Avg Phase U/V Trip C		
1829	Vavg>1 Trip	DDB_AVG_OV_1_3PH_TRIP
1st Stage Avg Phase O/V Trip 3ph		
1830	Vavg>1 Trip A	DDB_AVG_OV_1_PH_A_TRIP
1st Stage Avg Phase O/V Trip A		
1831	Vavg>1 Trip B	DDB_AVG_OV_1_PH_B_TRIP
1st Stage Avg Phase O/V Trip B		
1832	Vavg>1 Trip C	DDB_AVG_OV_1_PH_C_TRIP
1st Stage Avg Phase O/V Trip C		
1833	Vavg>2 Trip	DDB_AVG_OV_2_3PH_TRIP
2nd Stage Avg Phase O/V Trip 3ph		
1834	Vavg>2 Trip A	DDB_AVG_OV_2_PH_A_TRIP
2nd Stage Avg Phase O/V Trip A		
1835	Vavg>2 Trip B	DDB_AVG_OV_2_PH_B_TRIP
2nd Stage Avg Phase O/V Trip B		
1836	Vavg>2 Trip C	DDB_AVG_OV_2_PH_C_TRIP
2nd Stage Avg Phase O/V Trip C		
1837	V0avg>1 Trip	DDB_AVG_V0_1_TRIP
1st Stage Avg Zero Seq O/V Trip		
1838	V0avg>2 Trip	DDB_AVG_V0_2_TRIP
2nd Stage Avg Zero Seq O/V Trip		
1839	V1avg>1 Trip	DDB_AVG_V1_1_TRIP
1st Stage Avg Pos Seq O/V Trip		
1840	V1avg>2 Trip	DDB_AVG_V1_2_TRIP
2nd Stage Avg Pos Seq O/V Trip		
1841	V2avg>1 Trip	DDB_AVG_V2_1_TRIP
1st Stage Avg Neg Seq O/V Trip		
1842	V2avg>2 Trip	DDB_AVG_V2_2_TRIP
2nd Stage Avg Neg Seq O/V Trip		
1843	Inter PSL 1 IN	DDB_INTER_PSL_1_IN
Inter PSL 1 Input		
1844	Inter PSL 2 IN	DDB_INTER_PSL_2_IN
Inter PSL 2 Input		
1845	Inter PSL 3 IN	DDB_INTER_PSL_3_IN
Inter PSL 3 Input		
1846	Inter PSL 4 IN	DDB_INTER_PSL_4_IN
Inter PSL 4 Input		
1847	Inter PSL 5 IN	DDB_INTER_PSL_5_IN
Inter PSL 5 Input		
1848	Inter PSL 6 IN	DDB_INTER_PSL_6_IN
Inter PSL 6 Input		
1849	Inter PSL 7 IN	DDB_INTER_PSL_7_IN
Inter PSL 7 Input		
1850	Inter PSL 8 IN	DDB_INTER_PSL_8_IN
Inter PSL 8 Input		
1851	Inter PSL 9 IN	DDB_INTER_PSL_9_IN
Inter PSL 9 Input		
1852	Inter PSL 10 IN	DDB_INTER_PSL_10_IN
Inter PSL 10 Input		
1853	Inter PSL 11 IN	DDB_INTER_PSL_11_IN
Inter PSL 11 Input		
1854	Inter PSL 12 IN	DDB_INTER_PSL_12_IN
Inter PSL 12 Input		
1855	Inter PSL 13 IN	DDB_INTER_PSL_13_IN
Inter PSL 13 Input		
1856	Inter PSL 14 IN	DDB_INTER_PSL_14_IN
Inter PSL 14 Input		
1857	Inter PSL 15 IN	DDB_INTER_PSL_15_IN

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
Inter PSL 15 Input		
1858	Inter PSL 16 IN	DDB_INTER_PSL_16_IN
Inter PSL 16 Input		
1859	Inter PSL 17 IN	DDB_INTER_PSL_17_IN
Inter PSL 17 Input		
1860	Inter PSL 18 IN	DDB_INTER_PSL_18_IN
Inter PSL 18 Input		
1861	Inter PSL 19 IN	DDB_INTER_PSL_19_IN
Inter PSL 19 Input		
1862	Inter PSL 20 IN	DDB_INTER_PSL_20_IN
Inter PSL 20 Input		
1863	Inter PSL 21 IN	DDB_INTER_PSL_21_IN
Inter PSL 21 Input		
1864	Inter PSL 22 IN	DDB_INTER_PSL_22_IN
Inter PSL 22 Input		
1865	Inter PSL 23 IN	DDB_INTER_PSL_23_IN
Inter PSL 23 Input		
1866	Inter PSL 24 IN	DDB_INTER_PSL_24_IN
Inter PSL 24 Input		
1867	Inter PSL 25 IN	DDB_INTER_PSL_25_IN
Inter PSL 25 Input		
1868	Inter PSL 26 IN	DDB_INTER_PSL_26_IN
Inter PSL 26 Input		
1869	Inter PSL 27 IN	DDB_INTER_PSL_27_IN
Inter PSL 27 Input		
1870	Inter PSL 28 IN	DDB_INTER_PSL_28_IN
Inter PSL 28 Input		
1871	Inter PSL 29 IN	DDB_INTER_PSL_29_IN
Inter PSL 29 Input		
1872	Inter PSL 30 IN	DDB_INTER_PSL_30_IN
Inter PSL 30 Input		
1873	Inter PSL 31 IN	DDB_INTER_PSL_31_IN
Inter PSL 31 Input		
1874	Inter PSL 32 IN	DDB_INTER_PSL_32_IN
Inter PSL 32 Input		
1875	Inter PSL 1 OUT	DDB_INTER_PSL_1_OUT
Inter PSL 1 Output		
1876	Inter PSL 2 OUT	DDB_INTER_PSL_2_OUT
Inter PSL 2 Output		
1877	Inter PSL 3 OUT	DDB_INTER_PSL_3_OUT
Inter PSL 3 Output		
1878	Inter PSL 4 OUT	DDB_INTER_PSL_4_OUT
Inter PSL 4 Output		
1879	Inter PSL 5 OUT	DDB_INTER_PSL_5_OUT
Inter PSL 5 Output		
1880	Inter PSL 6 OUT	DDB_INTER_PSL_6_OUT
Inter PSL 6 Output		
1881	Inter PSL 7 OUT	DDB_INTER_PSL_7_OUT
Inter PSL 7 Output		
1882	Inter PSL 8 OUT	DDB_INTER_PSL_8_OUT
Inter PSL 8 Output		
1883	Inter PSL 9 OUT	DDB_INTER_PSL_9_OUT
Inter PSL 9 Output		
1884	Inter PSL 10 OUT	DDB_INTER_PSL_10_OUT
Inter PSL 10 Output		
1885	Inter PSL 11 OUT	DDB_INTER_PSL_11_OUT
Inter PSL 11 Output		
1886	Inter PSL 12 OUT	DDB_INTER_PSL_12_OUT

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
Inter PSL 12 Output		
1887	Inter PSL 13 OUT	DDB_INTER_PSL_13_OUT
Inter PSL 13 Output		
1888	Inter PSL 14 OUT	DDB_INTER_PSL_14_OUT
Inter PSL 14 Output		
1889	Inter PSL 15 OUT	DDB_INTER_PSL_15_OUT
Inter PSL 15 Output		
1890	Inter PSL 16 OUT	DDB_INTER_PSL_16_OUT
Inter PSL 16 Output		
1891	Inter PSL 17 OUT	DDB_INTER_PSL_17_OUT
Inter PSL 17 Output		
1892	Inter PSL 18 OUT	DDB_INTER_PSL_18_OUT
Inter PSL 18 Output		
1893	Inter PSL 19 OUT	DDB_INTER_PSL_19_OUT
Inter PSL 19 Output		
1894	Inter PSL 20 OUT	DDB_INTER_PSL_20_OUT
Inter PSL 20 Output		
1895	Inter PSL 21 OUT	DDB_INTER_PSL_21_OUT
Inter PSL 21 Output		
1896	Inter PSL 22 OUT	DDB_INTER_PSL_22_OUT
Inter PSL 22 Output		
1897	Inter PSL 23 OUT	DDB_INTER_PSL_23_OUT
Inter PSL 23 Output		
1898	Inter PSL 24 OUT	DDB_INTER_PSL_24_OUT
Inter PSL 24 Output		
1899	Inter PSL 25 OUT	DDB_INTER_PSL_25_OUT
Inter PSL 25 Output		
1900	Inter PSL 26 OUT	DDB_INTER_PSL_26_OUT
Inter PSL 26 Output		
1901	Inter PSL 27 OUT	DDB_INTER_PSL_27_OUT
Inter PSL 27 Output		
1902	Inter PSL 28 OUT	DDB_INTER_PSL_28_OUT
Inter PSL 28 Output		
1903	Inter PSL 29 OUT	DDB_INTER_PSL_29_OUT
Inter PSL 29 Output		
1904	Inter PSL 30 OUT	DDB_INTER_PSL_30_OUT
Inter PSL 30 Output		
1905	Inter PSL 31 OUT	DDB_INTER_PSL_31_OUT
Inter PSL 31 Output		
1906	Inter PSL 32 OUT	DDB_INTER_PSL_32_OUT
Inter PSL 32 Output		
1907	V1< Inhibit	DDB_PSUV_INHIBIT
Pos Seq U/V Inhibit		
1908	V1<1 Timer Block	DDB_PSUV_1_TIMER_BLOCK
1st Stage Pos Seq U/V Timer Block		
1909	V1<1 Start	DDB_PSUV_1_START
1st Stage Pos Seq U/V Start		
1910	V1<1 Trip	DDB_PSUV_1_TRIP
1st Stage Pos Seq U/V Trip		
1911	V1<2 Timer Block	DDB_PSUV_2_TIMER_BLOCK
2nd Stage Pos Seq U/V Timer Block		
1912	V1<2 Start	DDB_PSUV_2_START
2nd Stage Pos Seq U/V Start		
1913	V1<2 Trip	DDB_PSUV_2_TRIP
2nd Stage Pos Seq U/V Trip		
1914	V1> Inhibit	DDB_PSOV_INHIBIT
Pos Seq O/V Inhibit		
1915	V1>1 Timer Block	DDB_PSOV_1_TIMER_BLOCK

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
1st Stage Pos Seq O/V Timer Block		
1916	V1>1 Start	DDB_PSOV_1_START
1st Stage Pos Seq O/V Start		
1917	V1>1 Trip	DDB_PSOV_1_TRIP
1st Stage Pos Seq O/V Trip		
1918	V1>2 Timer Block	DDB_PSOV_2_TIMER_BLOCK
2nd Stage Pos Seq O/V Timer Block		
1919	V1>2 Start	DDB_PSOV_2_START
2nd Stage Pos Seq O/V Start		
1920	V1>2 Trip	DDB_PSOV_2_TRIP
2nd Stage Pos Seq O/V Trip		
1921	V2>2 Start	DDB_NEGSEQOV_2_START
2nd Stage Negative Sequence O/V Start		
1922	V2>2 Trip	DDB_NEGSEQOV_2_TRIP
2nd Stage Negative Sequence O/V Trip		
1923	Vavg< Inhibit	DDB_AVG_UV_INHIBIT
Avg Phase U/V Inhibit		
1924	Speed Input	DDB_SPEED_INPUT
Speed Input		
1925	Emergency Rest.	DDB_EMERGENCY_RESTART
Emergency Rest.		
1926	Thermal Lockout	DDB_ALARM_THERMAL_LOCKOUT
Thermal Lockout		
1927	Time Betwe Start	DDB_ALARM_TIME_BETWEEN_START
Time Betwe Start		
1928	Hot Start Nb.	DDB_ALARM_HOT_START_NB
Hot Start Nb.		
1929	Cold Start Nb.	DDB_ALARM_COLD_START_NB
Cold Start Nb.		
1930	Antibkspin Alarm	DDB_ALARM_ANTIBACKSPIN
Antibkspin Alarm		
1931	Reacc Low Volt.	DDB_UNDERV_REAC
Reacc Low Volt.		
1932	Strt in Progress	DDB_START_IN_PROGRESS
Strt in Progress		
1933	Strt Sucessfull	DDB_START_SUCCESSFUL
Strt Sucessfull		
1934	Prolonged Start	DDB_PROLONGED_START
Prolonged Start		
1935	Reac in Progress	DDB_REAC_IN_PROGRESS
Reac in Progress		
1936	Stall Rotor-run	DDB_STALL_ROTOR_RUN
Stall Rotor-run		
1937	Stall Rotor-strt	DDB_STALL_ROTOR_START
Stall Rotor-strt		
1938	Vdip<1 AB Phase	DDB_VDIP_START_PH_AB
Vdip<1 AB Phase		
1939	Vdip<1 BC Phase	DDB_VDIP_START_PH_BC
Vdip<1 BC Phase		
1940	Vdip<1 CA Phase	DDB_VDIP_START_PH_CA
Vdip<1 CA Phase		
1941	Trip Vdip<1	DDB_VDIP_TRIP
Trip Vdip<1		
1942	Auto Re-Start OK	DDB_AUTO_RESTART_SUCCEED
Auto Re-Start OK		
1943	Auto Re-Start	DDB_AUTO_RESTART_IN_PROGRESS
Auto Re-Start		
1944	Auto Re-Start KO	DDB_AUTO_RESTART_FAIL

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
Auto Re-Start KO		
1945	Start Rev. Power	DDB_REV_POW_START
Start Rev. Power		
1946	Trip Rev. Power	DDB_REV_POW_TRIP
Trip Rev. Power		
1947	Hour Run Alarm1	DDB_ALARM_HOUR_RUN_METER_1
Hour Run Alarm 1		
1948	Hour Run Alarm2	DDB_ALARM_HOUR_RUN_METER_2
Hour Run Alarm 2		
1949	Hour Run Alarm3	DDB_ALARM_HOUR_RUN_METER_3
Hour Run Alarm 3		
1950	Test Mode Info	DDB_TEST_MODE_INFO
Test Mode In progress		
1951	TEFD Inhibit	DDB_TEFD_INHIBIT
TEFD Inhibit		
1952	TEFD Reset	DDB_TEFD_RESET
TEFD Reset		
1953	TEFD Start	DDB_TEFD_START
TEFD Start		
1954	TEFD Forward	DDB_TEFD_FORWARD
TEFD Forward		
1955	TEFD Reverse	DDB_TEFD_REVERSE
TEFD Reverse		
1959	SWI1 Aux (52-A)	DDB_SWI1_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 1)		
1960	SWI1 Aux (52-B)	DDB_SWI1_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 1)		
1961	SWI1 Input Alm	DDB_SWI1_STATUS_ALARM
This DDB signal indicates that the switch 1 is in an invalid state		
1962	SWI2 Aux (52-A)	DDB_SWI2_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 2)		
1963	SWI2 Aux (52-B)	DDB_SWI2_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 2)		
1964	SWI2 Input Alm	DDB_SWI2_STATUS_ALARM
This DDB signal indicates that the switch 2 is in an invalid state		
1965	SWI3 Aux (52-A)	DDB_SWI3_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 3)		
1966	SWI3 Aux (52-B)	DDB_SWI3_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 3)		
1967	SWI3 Input Alm	DDB_SWI3_STATUS_ALARM
This DDB signal indicates that the switch 3 is in an invalid state		
1968	SWI4 Aux (52-A)	DDB_SWI4_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 4)		
1969	SWI4 Aux (52-B)	DDB_SWI4_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 4)		
1970	SWI4 Input Alm	DDB_SWI4_STATUS_ALARM
This DDB signal indicates that the switch 4 is in an invalid state		
1971	SWI5 Aux (52-A)	DDB_SWI5_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 5)		
1972	SWI5 Aux (52-B)	DDB_SWI5_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 5)		
1973	SWI5 Input Alm	DDB_SWI5_STATUS_ALARM
This DDB signal indicates that the switch 5 is in an invalid state		
1974	SWI6 Aux (52-A)	DDB_SWI6_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 6)		
1975	SWI6 Aux (52-B)	DDB_SWI6_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 6)		
1976	SWI6 Input Alm	DDB_SWI6_STATUS_ALARM

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal indicates that the switch 6 is in an invalid state		
1977	SWI7 Aux (52-A)	DDB_SWI7_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 7)		
1978	SWI7 Aux (52-B)	DDB_SWI7_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 7)		
1979	SWI7 Input Alm	DDB_SWI7_STATUS_ALARM
This DDB signal indicates that the switch 7 is in an invalid state		
1980	SWI8 Aux (52-A)	DDB_SWI8_STATUS_INPUT_52A
This DDB signal is the 3-phase 52A signal (signal indicating state of switch 8)		
1981	SWI8 Aux (52-B)	DDB_SWI8_STATUS_INPUT_52B
This DDB signal is the 3-phase 52B signal (signal indicating inverse state of switch 8)		
1982	SWI8 Input Alm	DDB_SWI8_STATUS_ALARM
This DDB signal indicates that the switch 8 is in an invalid state		
1983	SWI1 Control Trp	DDB_SWI1_CONTROL_TRIP
This DDB signal tells the switch 1 to trip		
1984	SWI1 Control Cls	DDB_SWI1_CONTROL_CLOSE
This DDB signal tells the switch 1 to close		
1985	SWI2 Control Trp	DDB_SWI2_CONTROL_TRIP
This DDB signal tells the switch 2 to trip		
1986	SWI2 Control Cls	DDB_SWI2_CONTROL_CLOSE
This DDB signal tells the switch 2 to close		
1987	SWI3 Control Trp	DDB_SWI3_CONTROL_TRIP
This DDB signal tells the switch 3 to trip		
1988	SWI3 Control Cls	DDB_SWI3_CONTROL_CLOSE
This DDB signal tells the switch 3 to close		
1989	SWI4 Control Trp	DDB_SWI4_CONTROL_TRIP
This DDB signal tells the switch 4 to trip		
1990	SWI4 Control Cls	DDB_SWI4_CONTROL_CLOSE
This DDB signal tells the switch 4 to close		
1991	SWI5 Control Trp	DDB_SWI5_CONTROL_TRIP
This DDB signal tells the switch 5 to trip		
1992	SWI5 Control Cls	DDB_SWI5_CONTROL_CLOSE
This DDB signal tells the switch 5 to close		
1993	SWI6 Control Trp	DDB_SWI6_CONTROL_TRIP
This DDB signal tells the switch 6 to trip		
1994	SWI6 Control Cls	DDB_SWI6_CONTROL_CLOSE
This DDB signal tells the switch 6 to close		
1995	SWI7 Control Trp	DDB_SWI7_CONTROL_TRIP
This DDB signal tells the switch 7 to trip		
1996	SWI7 Control Cls	DDB_SWI7_CONTROL_CLOSE
This DDB signal tells the switch 7 to close		
1997	SWI8 Control Trp	DDB_SWI8_CONTROL_TRIP
This DDB signal tells the switch 8 to trip		
1998	SWI8 Control Cls	DDB_SWI8_CONTROL_CLOSE
This DDB signal tells the switch 8 to close		
1999	Blk Rmt SWI1 Ops	DDB_BLK_REMOTE_SWI1_OPS
This DDB signal blocks remote switch 1 Trip and Close		
2000	Blk Rmt SWI2 Ops	DDB_BLK_REMOTE_SWI2_OPS
This DDB signal blocks remote switch 2 Trip and Close		
2001	Blk Rmt SWI3 Ops	DDB_BLK_REMOTE_SWI3_OPS
This DDB signal blocks remote switch 3 Trip and Close		
2002	Blk Rmt SWI4 Ops	DDB_BLK_REMOTE_SWI4_OPS
This DDB signal blocks remote switch 4 Trip and Close		
2003	Blk Rmt SWI5 Ops	DDB_BLK_REMOTE_SWI5_OPS
This DDB signal blocks remote switch 5 Trip and Close		
2004	Blk Rmt SWI6 Ops	DDB_BLK_REMOTE_SWI6_OPS
This DDB signal blocks remote switch 6 Trip and Close		
2005	Blk Rmt SWI7 Ops	DDB_BLK_REMOTE_SWI7_OPS

ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal blocks remote switch 7 Trip and Close		
2006	Blk Rmt SWI8 Ops	DDB_BLK_REMOTE_SWI8_OPS
This DDB signal blocks remote switch 8 Trip and Close		
2007	SWI1 Status Opn	DDB_SWI1_STATUS_OPEN
This DDB signal is assigned to output the switch1 status-Open		
2008	SWI1 Status Cls	DDB_SWI1_STATUS_CLOSE
This DDB signal is assigned to output the switch1 status-Close		
2009	SWI2 Status Opn	DDB_SWI2_STATUS_OPEN
This DDB signal is assigned to output the switch2 status-Open		
2010	SWI2 Status Cls	DDB_SWI2_STATUS_CLOSE
This DDB signal is assigned to output the switch2 status-Close		
2011	SWI3 Status Opn	DDB_SWI3_STATUS_OPEN
This DDB signal is assigned to output the switch3 status-Open		
2012	SWI3 Status Cls	DDB_SWI3_STATUS_CLOSE
This DDB signal is assigned to output the switch3 status-Close		
2013	SWI4 Status Opn	DDB_SWI4_STATUS_OPEN
This DDB signal is assigned to output the switch4 status-Open		
2014	SWI4 Status Cls	DDB_SWI4_STATUS_CLOSE
This DDB signal is assigned to output the switch4 status-Close		
2015	SWI5 Status Opn	DDB_SWI5_STATUS_OPEN
This DDB signal is assigned to output the switch5 status-Open		
2016	SWI5 Status Cls	DDB_SWI5_STATUS_CLOSE
This DDB signal is assigned to output the switch5 status-Close		
2017	SWI6 Status Opn	DDB_SWI6_STATUS_OPEN
This DDB signal is assigned to output the switch6 status-Open		
2018	SWI6 Status Cls	DDB_SWI6_STATUS_CLOSE
This DDB signal is assigned to output the switch6 status-Close		
2019	SWI7 Status Opn	DDB_SWI7_STATUS_OPEN
This DDB signal is assigned to output the switch7 status-Open		
2020	SWI7 Status Cls	DDB_SWI7_STATUS_CLOSE
This DDB signal is assigned to output the switch7 status-Close		
2021	SWI8 Status Opn	DDB_SWI8_STATUS_OPEN
This DDB signal is assigned to output the switch8 status-Open		
2022	SWI8 Status Cls	DDB_SWI8_STATUS_CLOSE
This DDB signal is assigned to output the switch8 status-Close		
2023	SWI1 Trip Fail	DDB_SWI1_FAILED_TO_TRIP
This DDB signal indicates that the switch 1 has failed to trip		
2024	SWI1 Cls Fail	DDB_SWI1_FAILED_TO_CLOSE
This DDB signal indicates that the switch 1 has failed to close		
2025	SWI2 Trip Fail	DDB_SWI2_FAILED_TO_TRIP
This DDB signal indicates that the switch 2 has failed to trip		
2026	SWI2 Cls Fail	DDB_SWI2_FAILED_TO_CLOSE
This DDB signal indicates that the switch 2 has failed to close		
2027	SWI3 Trip Fail	DDB_SWI3_FAILED_TO_TRIP
This DDB signal indicates that the switch 3 has failed to trip		
2028	SWI3 Cls Fail	DDB_SWI3_FAILED_TO_CLOSE
This DDB signal indicates that the switch 3 has failed to close		
2029	SWI4 Trip Fail	DDB_SWI4_FAILED_TO_TRIP
This DDB signal indicates that the switch 4 has failed to trip		
2030	SWI4 Cls Fail	DDB_SWI4_FAILED_TO_CLOSE
This DDB signal indicates that the switch 4 has failed to close		
2031	SWI5 Trip Fail	DDB_SWI5_FAILED_TO_TRIP
This DDB signal indicates that the switch 5 has failed to trip		
2032	SWI5 Cls Fail	DDB_SWI5_FAILED_TO_CLOSE
This DDB signal indicates that the switch 5 has failed to close		
2033	SWI6 Trip Fail	DDB_SWI6_FAILED_TO_TRIP
This DDB signal indicates that the switch 6 has failed to trip		
2034	SWI6 Cls Fail	DDB_SWI6_FAILED_TO_CLOSE

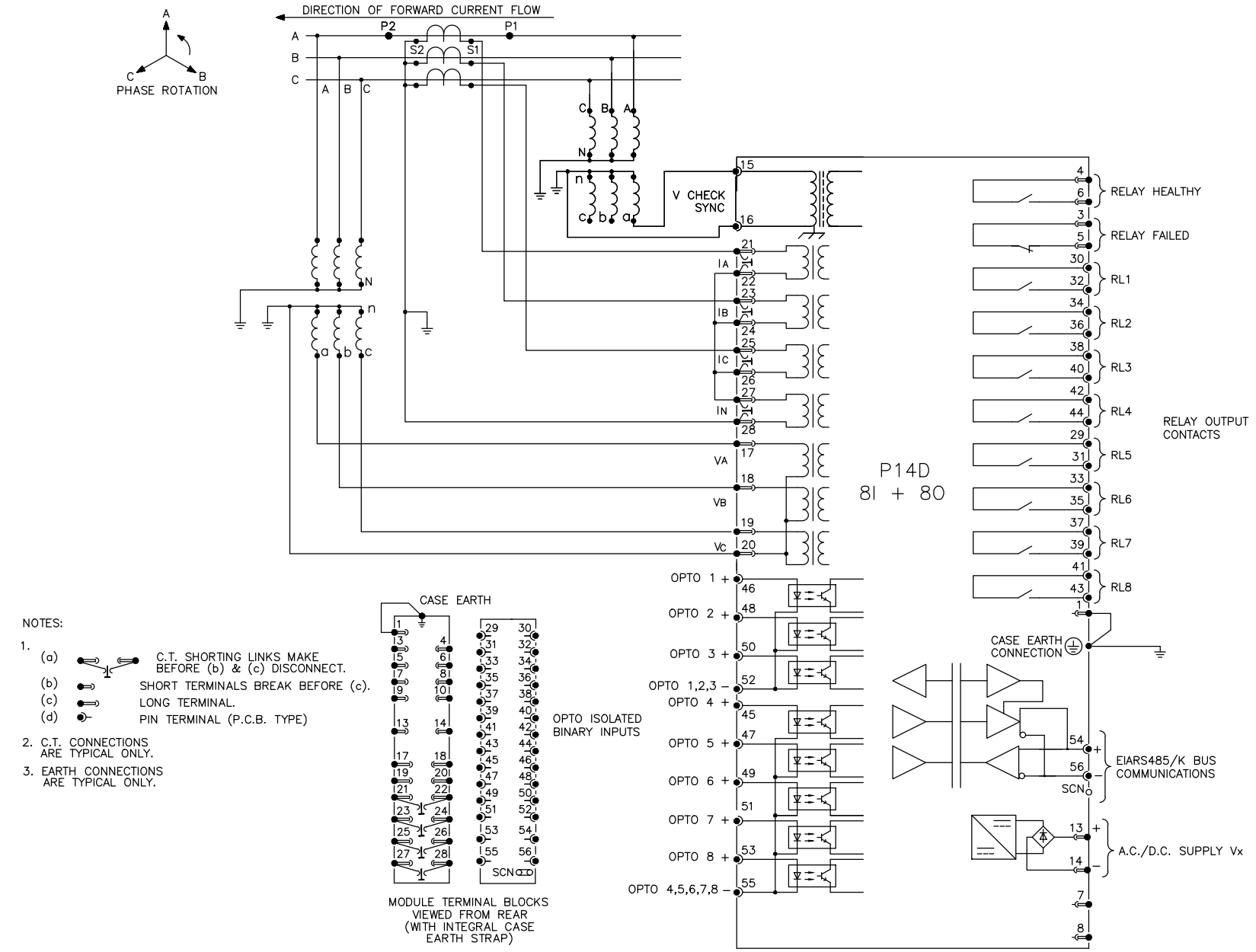
ORDINAL	SIGNAL NAME	ELEMENT NAME
DESCRIPTION		
This DDB signal indicates that the switch 6 has failed to close		
2035	SWI7 Trip Fail	DDB_SWI7_FAILED_TO_TRIP
This DDB signal indicates that the switch 7 has failed to trip		
2036	SWI7 Cls Fail	DDB_SWI7_FAILED_TO_CLOSE
This DDB signal indicates that the switch 7 has failed to close		
2037	SWI8 Trip Fail	DDB_SWI8_FAILED_TO_TRIP
This DDB signal indicates that the switch 8 has failed to trip		
2038	SWI8 Cls Fail	DDB_SWI8_FAILED_TO_CLOSE
This DDB signal indicates that the switch 8 has failed to close		

APPENDIX C

WIRING DIAGRAMS

MODEL	CORTEC OPTION*	EXTERNAL CONNECTION DIAGRAM TITLE	DRAWING-SHEET	ISSUE
P14D	IO option A	DIRECTIONAL PHASE OVERCURRENT AND E/F (8 I/P & 8 O/P)	10P14D01-1	D
	IO option A	DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P)	10P14D02-1	D
	IO option A	DIRECTIONAL PHASE OVERCURRENT AND E/F (8 I/P & 8 O/P) WITH ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (8 I/P & 8 O/P) WITH DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (8 I/P & 8 O/P) WITH DUAL FIBRE ETHERNET	10P14D03-1 10P14D03-2 10P14D03-3	D C C
	IO option A	DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P) WITH ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P) WITH DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P) WITH DUAL FIBRE ETHERNET	10P14D04-1 10P14D04-2 10P14D04-3	D C C
	IO option B	DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH 2 RS485 DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH 2 RS485 & ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET	10P14D05-1 10P14D05-2 10P14D05-3 10P14D05-4	C C C C
	IO option B	DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH 2 RS485 DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH 2 RS485 & ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET	10P14D06-1 10P14D06-2 10P14D06-3 10P14D06-4	D C C C
	IO option C	DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH TCS DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH TCS & ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH TCS & DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (11 I/P & 12 O/P) WITH TCS & DUAL FIBRE ETHERNET	10P14D07-1 10P14D07-2 10P14D07-3 10P14D07-4	C C C C
	IO option C	DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH TCS DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH TCS & ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH TCS & DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH TCS & DUAL FIBRE ETHERNET	10P14D08-1 10P14D08-2 10P14D08-3 10P14D08-4	D C C C
	IO option D	DIRECTIONAL PHASE OVERCURRENT AND E/F (13 I/P & 12 O/P) DIRECTIONAL PHASE OVERCURRENT AND E/F (13 I/P & 12 O/P) WITH ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (13 I/P & 12 O/P) WITH DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND E/F (13 I/P & 12 O/P) WITH DUAL FIBRE ETHERNET	10P14D09-1 10P14D09-2 10P14D09-3 10P14D09-4	C C C C
	IO option D	DIRECTIONAL PHASE OVERCURRENT AND SEF (13 I/P & 12 O/P) DIRECTIONAL PHASE OVERCURRENT AND SEF (13 I/P & 12 O/P) WITH ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (13 I/P & 12 O/P) WITH DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT AND SEF (13 I/P & 12 O/P) WITH DUAL FIBRE ETHERNET	10P14D10-1 10P14D10-2 10P14D10-3 10P14D10-4	D C C C
	IO option A	DIRECTIONAL PHASE OVERCURRENT AND E/F (8 I/P & 8 O/P) FOR KCEG 140/142 RETROFIT	10P14D11-1	C
		DIRECTIONAL PHASE OVERCURRENT AND E/F WITH SEPERATE RESIDUAL VOLTAGE INPUT 8I/P + 8O/P	10P14D12-1	C
	IO option E	DIRECTIONAL PHASE OVER CURRENT AND E/F (3 I/P & 4 O/P)	10P14D13-1	D
	IO option F	DIRECTIONAL PHASE OVER CURRENT AND E/F (6 I/P & 8 O/P) WITH TCS	10P14D14-1	D
	IO option A	DIRECTIONAL PHASE OVERCURRENT AND E/F (8 I/P & 8 O/P) - WITH OPTIONAL SHORTING LINK	10P14D15-1	D
	IO option H	DIRECTIONAL PHASE OVERCURRENT & E/F (10 I/P & 12 O/P) WITH 2 RS485 DIRECTIONAL PHASE OVERCURRENT & E/F (10 I/P & 12 O/P) WITH 2 RS485 & ETHERNET DIRECTIONAL PHASE OVERCURRENT & E/F (10 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT & E/F (10 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET	10P14D16-1 10P14D16-2 10P14D16-3 10P14D16-4	C C C C
	IO option H	DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 & ETHERNET DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET	10P14D17-1 10P14D17-2 10P14D17-3 10P14D17-4	C C C C
	IO option J	DIRECTIONAL PHASE OVERCURRENT & E/F (12 I/P & 12 O/P) DIRECTIONAL PHASE OVERCURRENT & E/F (12 I/P & 12 O/P) WITH ETHERNET DIRECTIONAL PHASE OVERCURRENT & E/F (12 I/P & 12 O/P) WITH DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT & E/F (12 I/P & 12 O/P) WITH DUAL FIBRE ETHERNET	10P14D18-1 10P14D18-2 10P14D18-3 10P14D18-4	C C C C
	IO option J	DIRECTIONAL PHASE OVERCURRENT & SEF (12 I/P & 12 O/P) DIRECTIONAL PHASE OVERCURRENT & SEF (12 I/P & 12 O/P) WITH ETHERNET DIRECTIONAL PHASE OVERCURRENT & SEF (12 I/P & 12 O/P) WITH DUAL COPPER ETHERNET DIRECTIONAL PHASE OVERCURRENT & SEF (12 I/P & 12 O/P) WITH DUAL FIBRE ETHERNET	10P14D19-1 10P14D19-2 10P14D19-3 10P14D19-4	C C C C

* When selecting applicable connection diagram(s), it may be helpful to reference the appropriate model's CORTEC.



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. EARTH CONNECTIONS ARE TYPICAL ONLY.

Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P)	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D01	Sht: 1
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -

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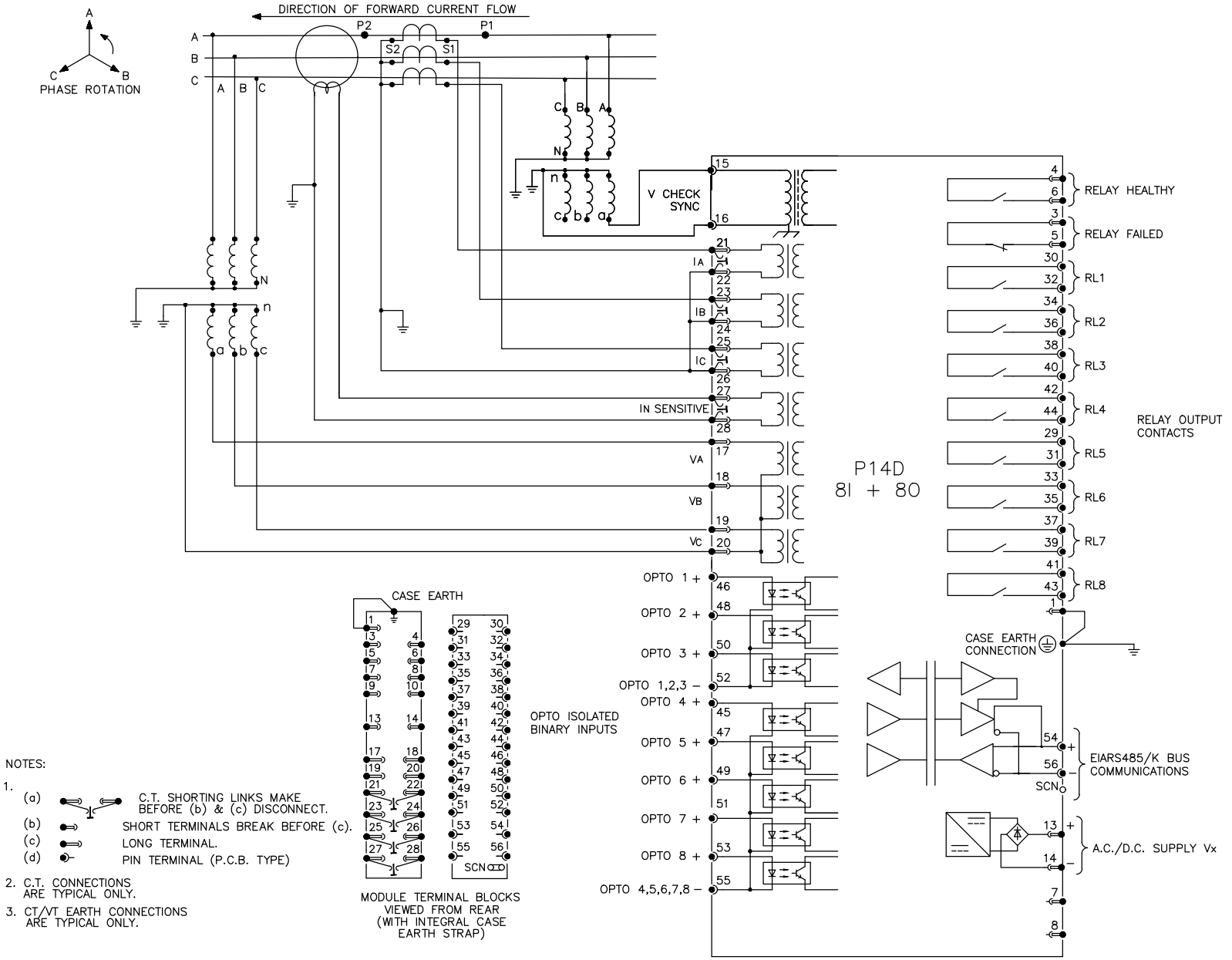

Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P)	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D02	Sht: 1
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -

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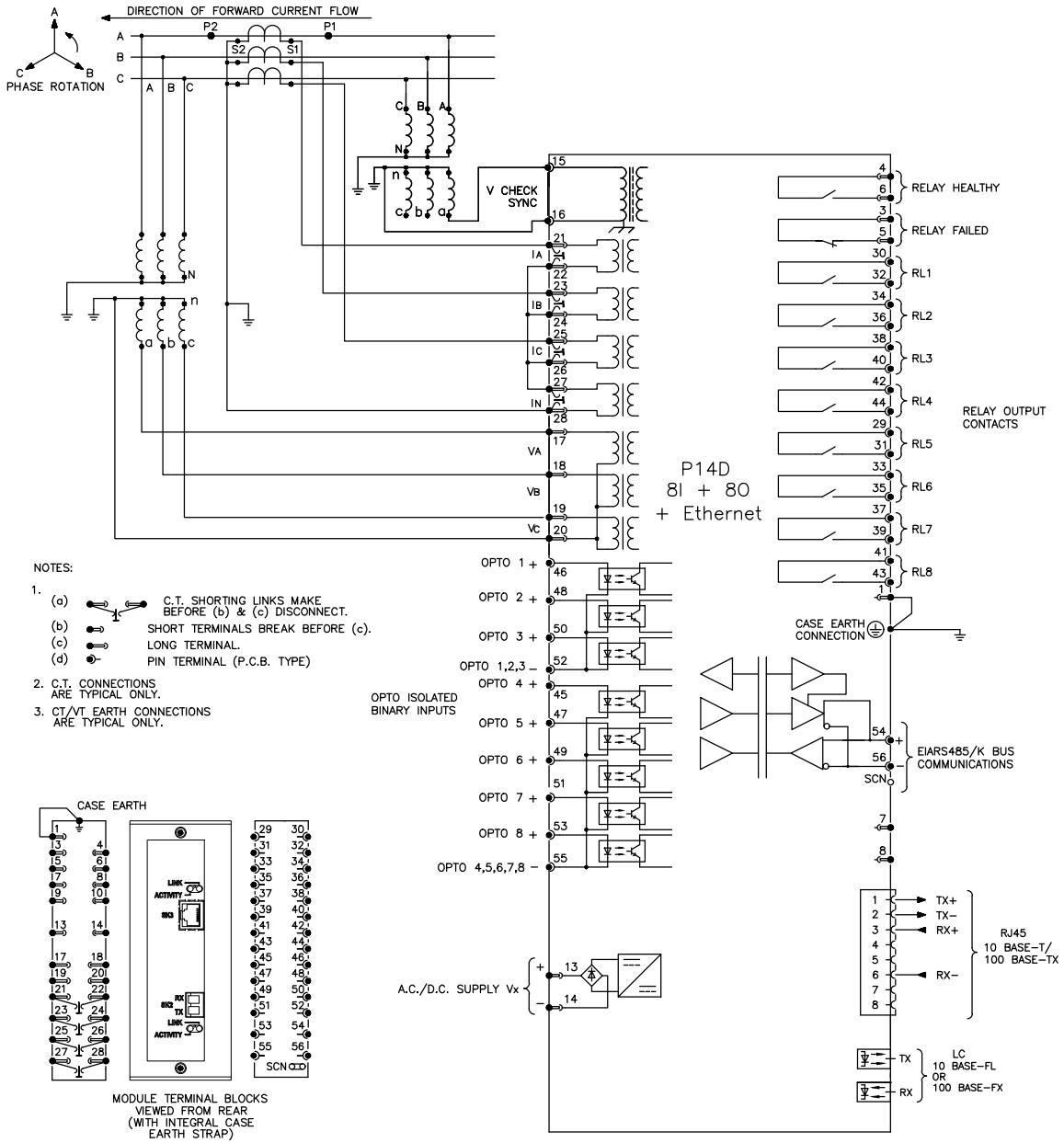
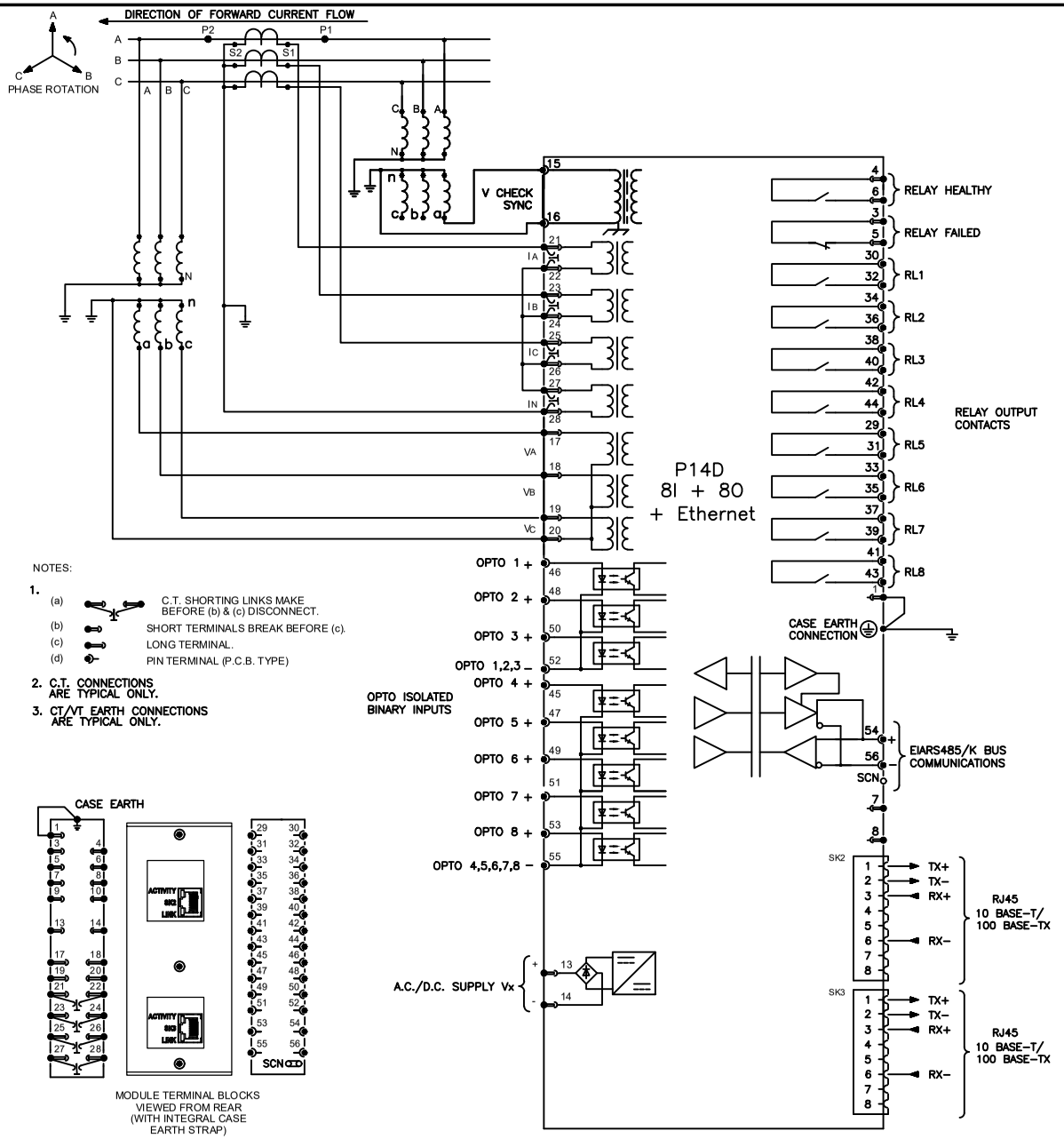
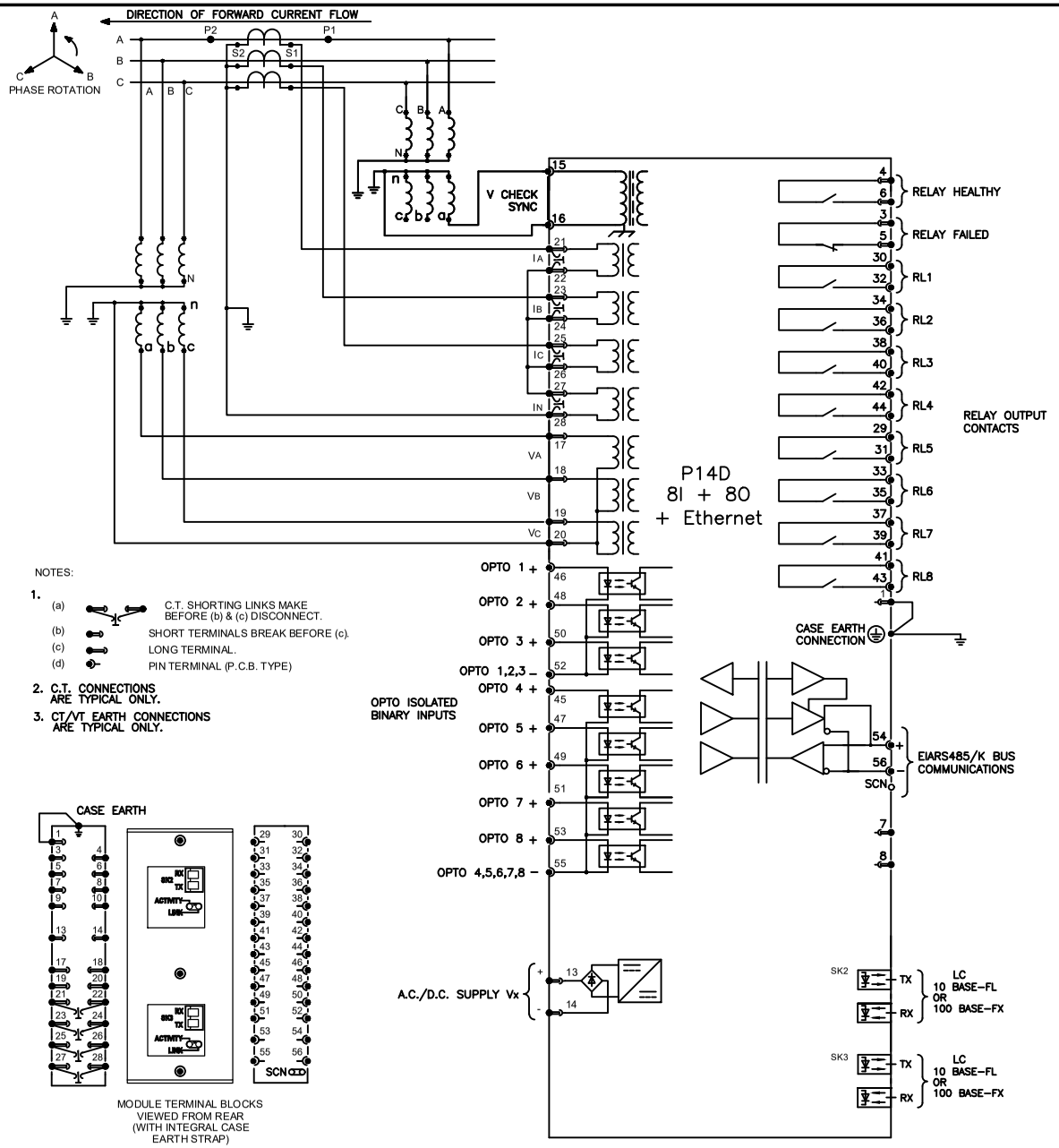


Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P) WITH ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D03	Sht: 1	
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: 2	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P) WITH DUAL COPPER ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P14D03	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date:	Chkd: CP.TEOH			Next Sht: 3	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P) WITH DUAL FIBRE ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D03	Sht: 3
Date:	Chkd: CP.TEOH			Next Sht: -

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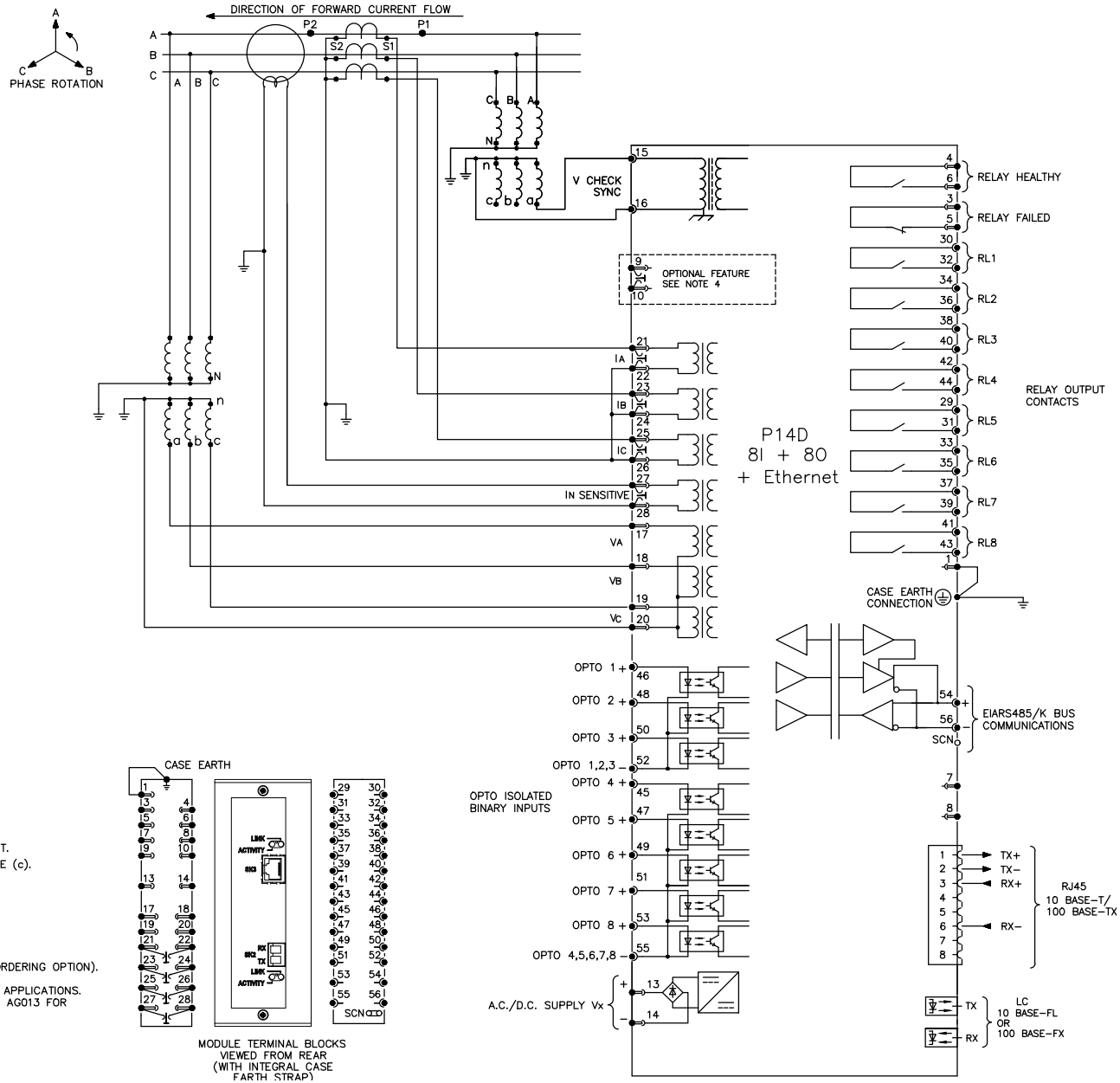
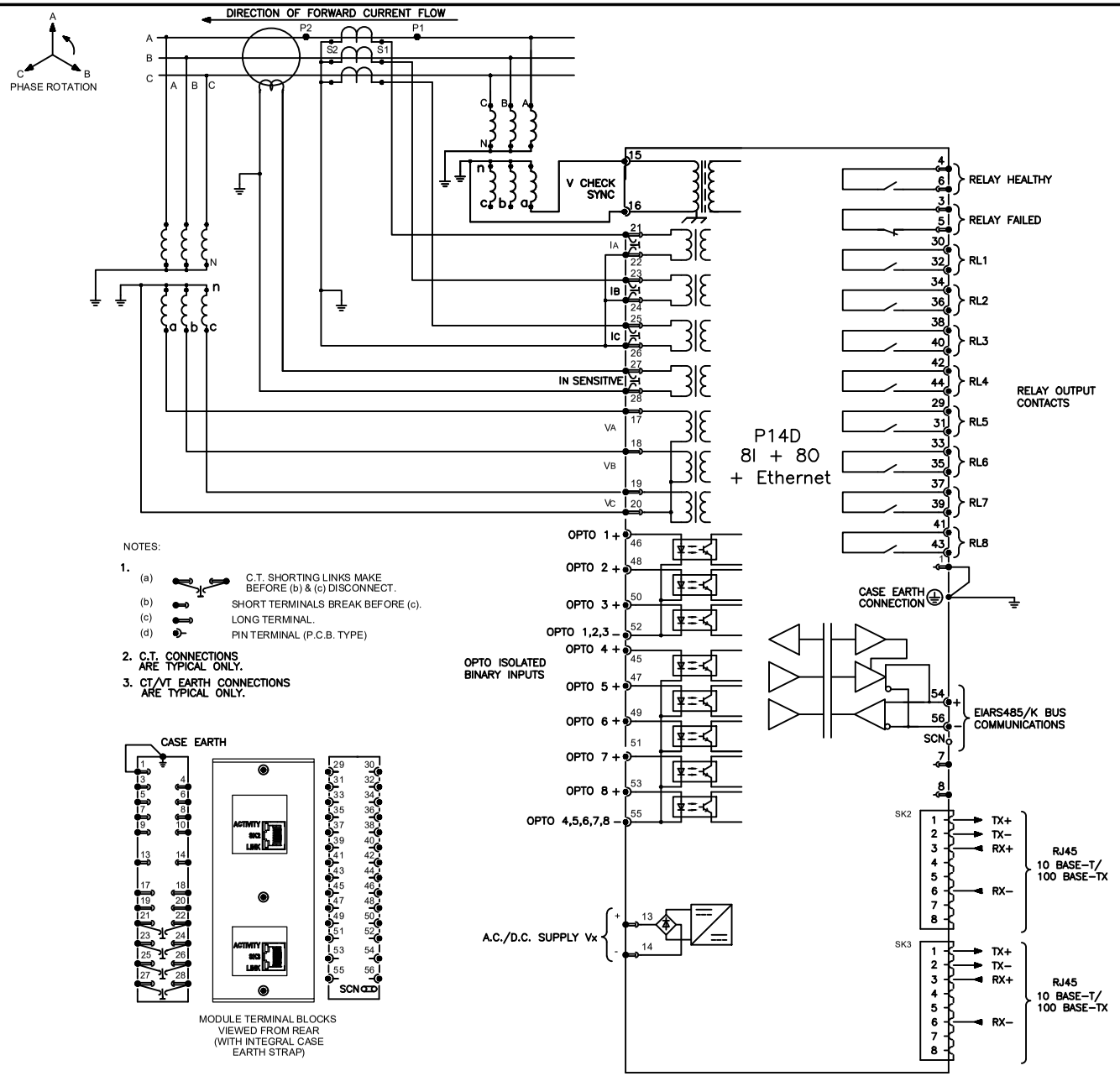


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. CT/VT EARTH CONNECTIONS ARE TYPICAL ONLY.
4. TERMINALS 9 & 10: OPTIONAL SHORTING LINK (ORDERING OPTION). ONLY AVAILABLE FOR THE 30TE MODEL VARIANTS. THESE TERMINALS ARE USED FOR CAPACITOR CONE APPLICATIONS. PLEASE REFER TO ALSTOM GRID APPLICATION GUIDE AG013 FOR GUIDANCE.

Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P) WITH ETHERNET & OPTIONAL SHORTING LINK		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D04	Sht: 1	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: 2	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (8 I/P & 8 O/P) WITH DUAL COPPER ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P14D04	Sht: 2
Date:	Chkd: CP.TEOH			Next Sht: 3

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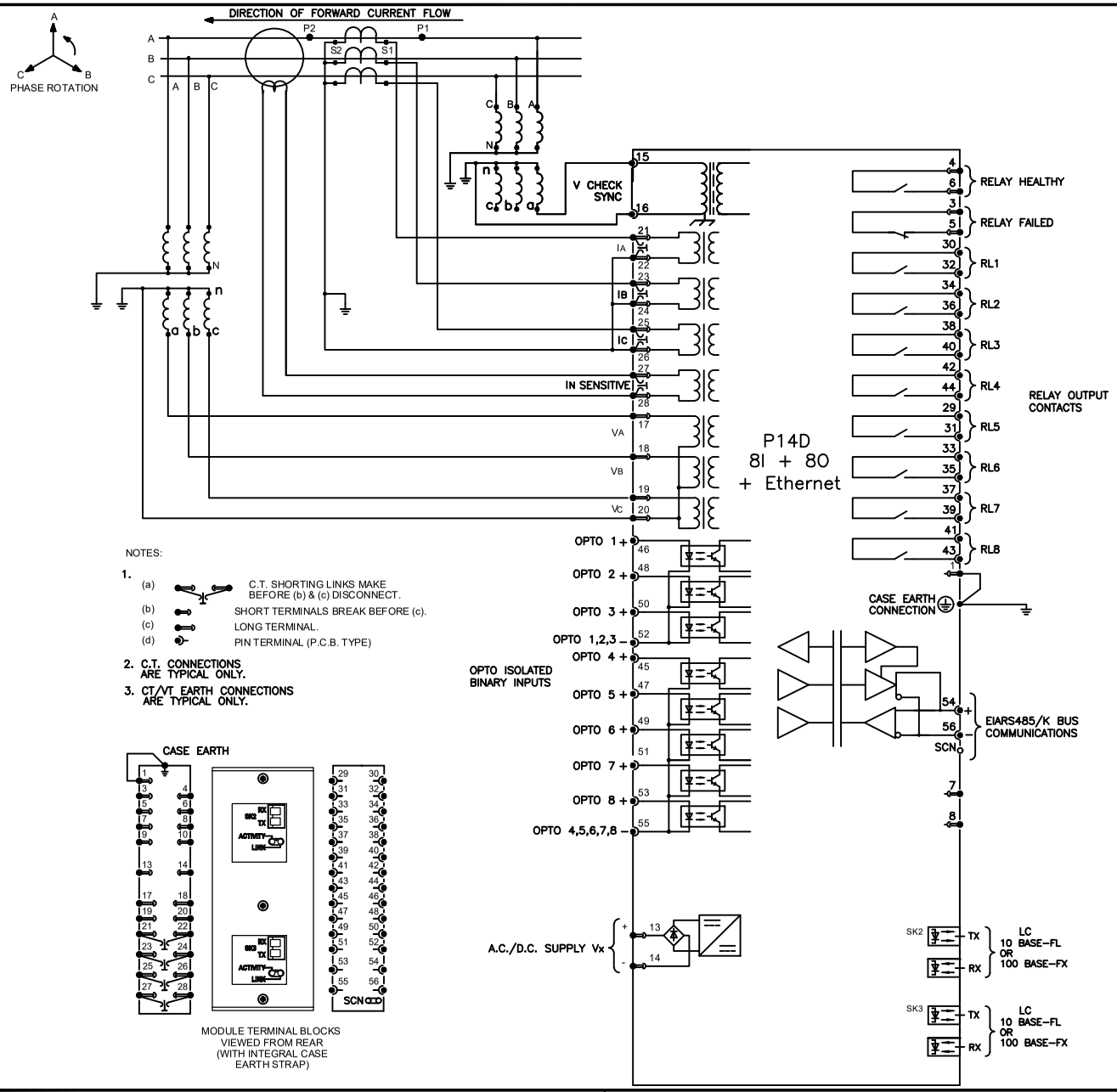

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. CT/VT EARTH CONNECTIONS ARE TYPICAL ONLY.

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P) WITH DUAL FIBRE ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D04	Sht: 3
Date:	Chkd: CP.TEOH			Next Sht: -

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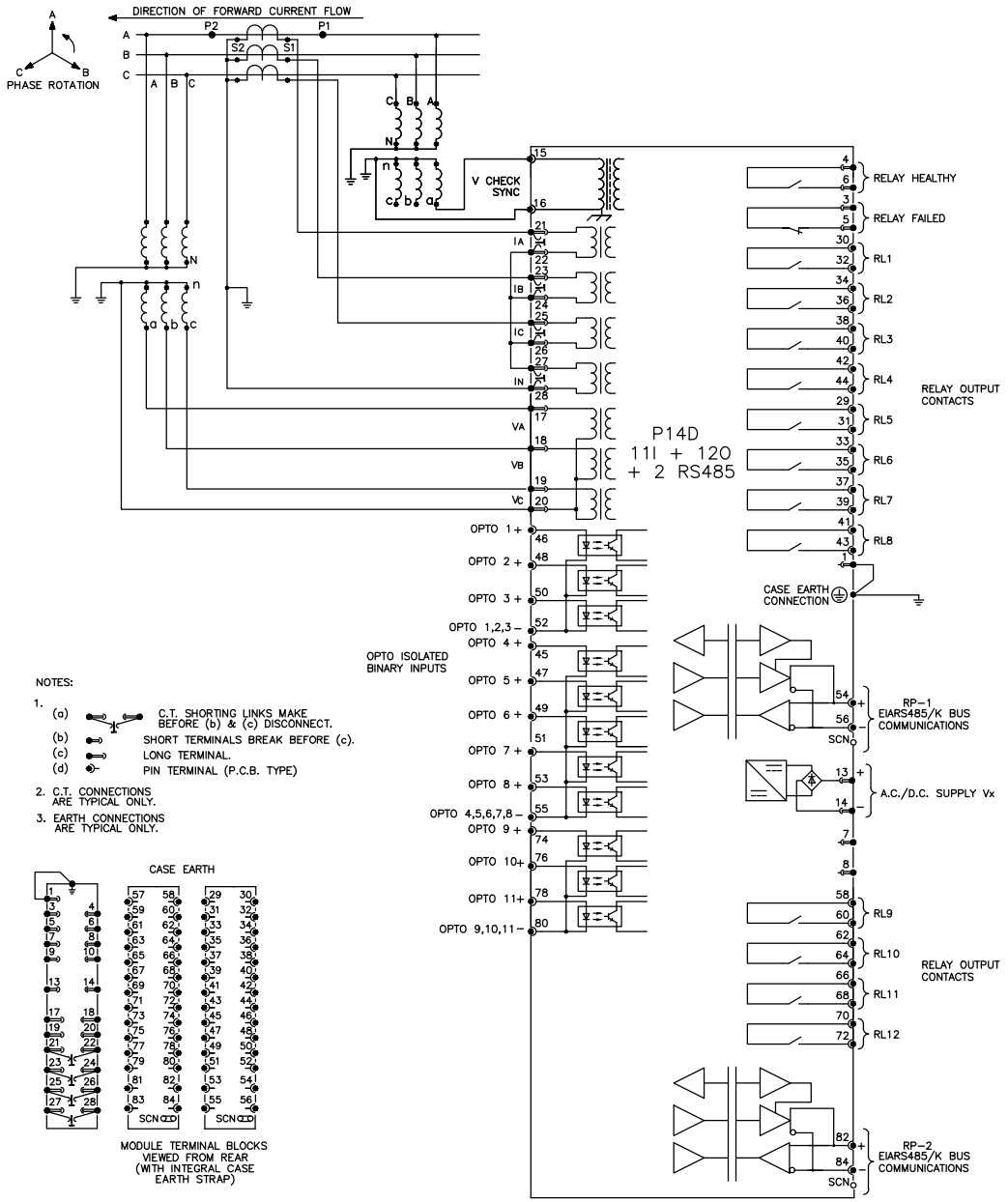
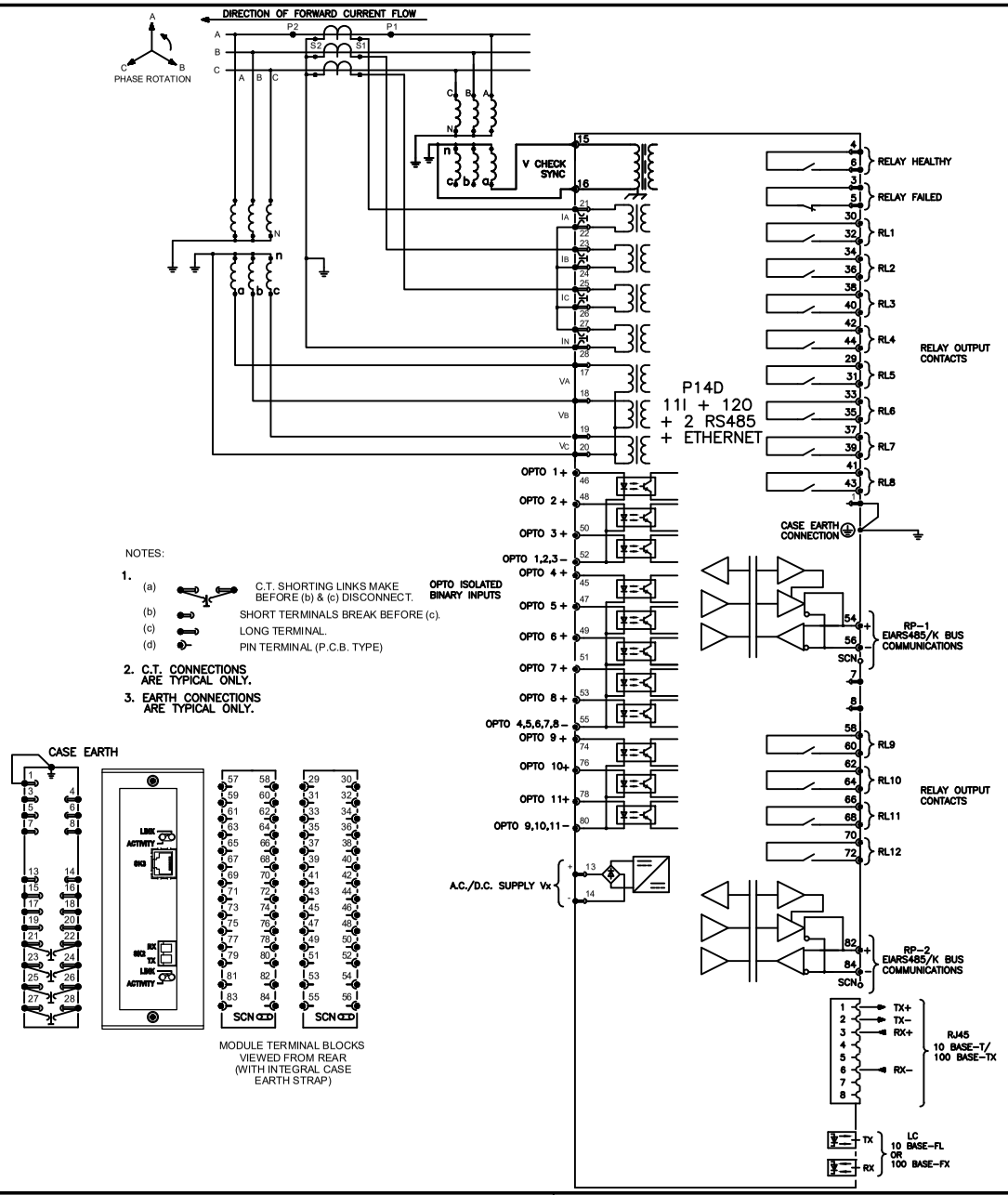


Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (11 I/P & 12 O/P) WITH 2 RS485		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D05	Sht: 1	
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (11 I/P & 12 O/P) WITH 2 RS485 ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D05	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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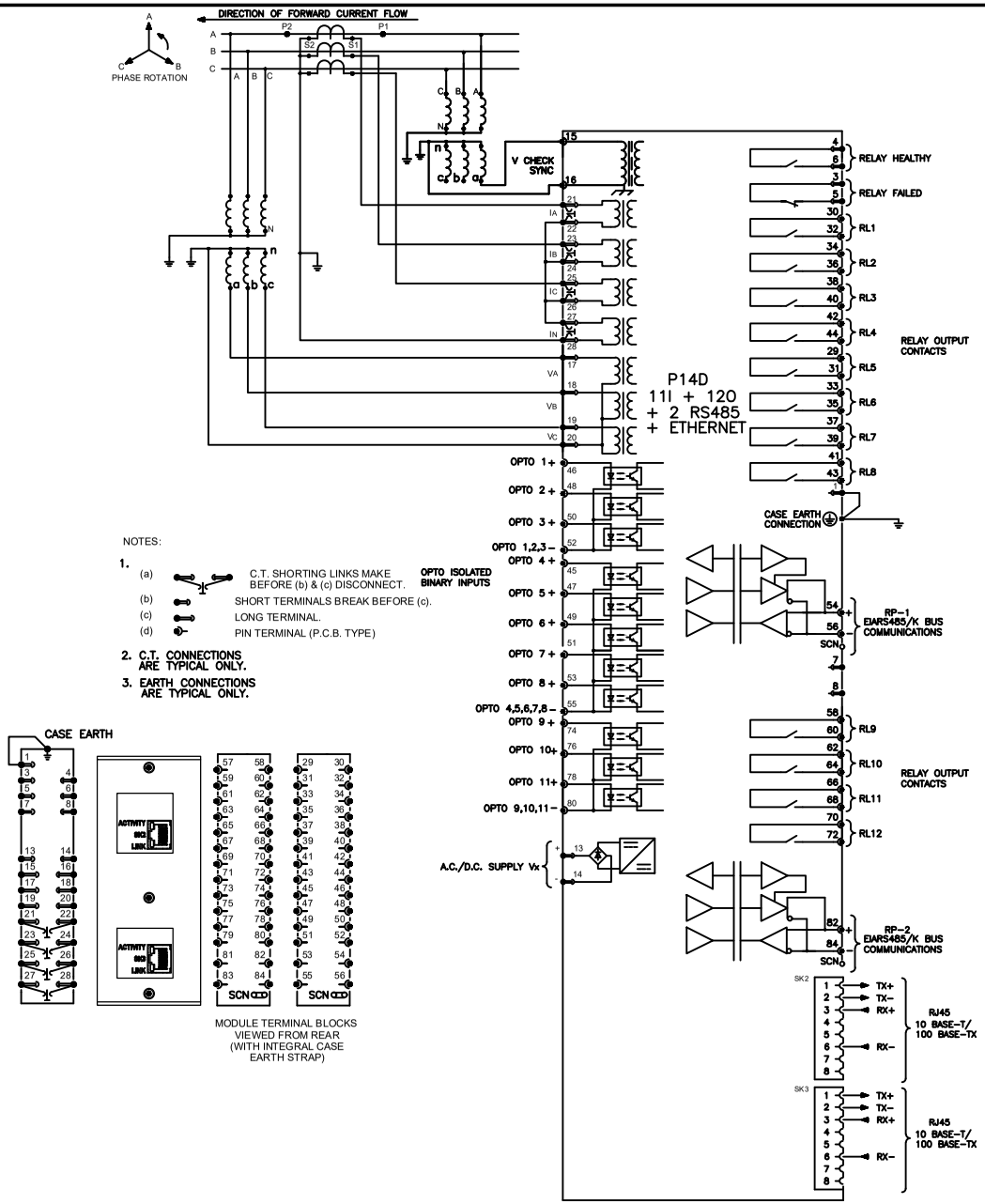

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & E/F (11 I/P & 12 O/P) WITH 2 RS485 DUAL COPPER ETHERNET		
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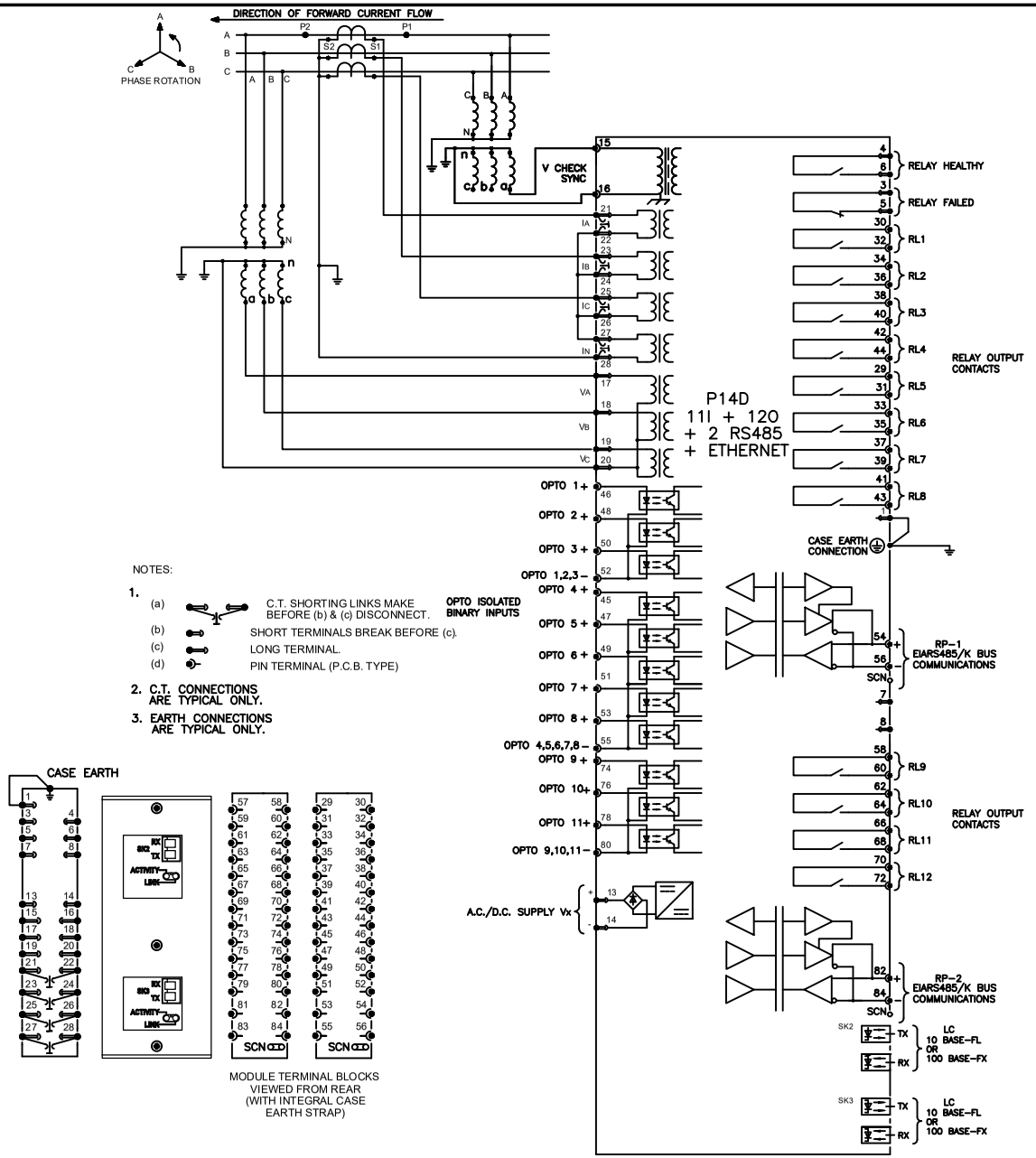

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & E/F (11 I/P & 12 O/P) WITH 2 RS485 DUAL FIBRE ETHERNET	
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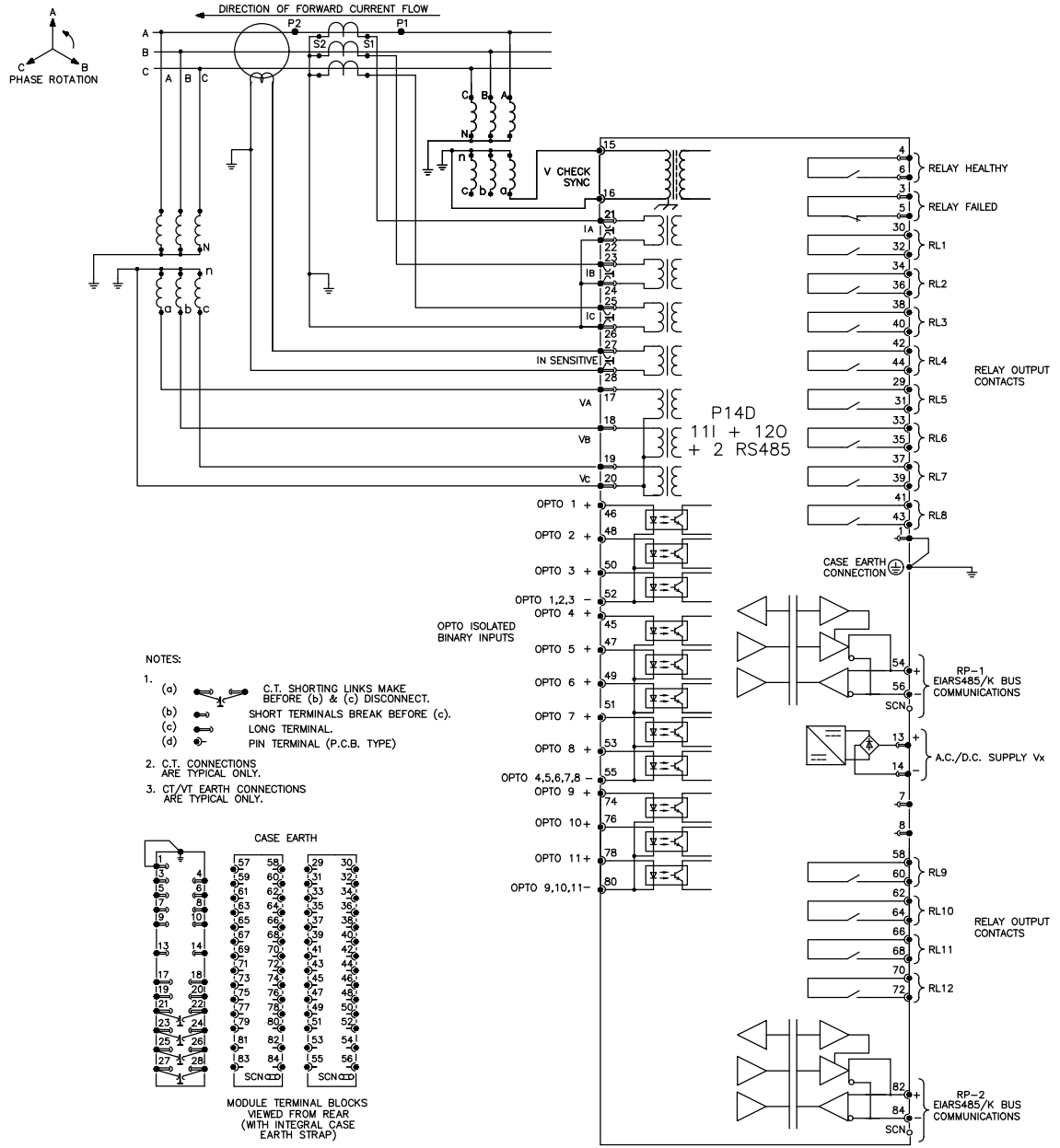
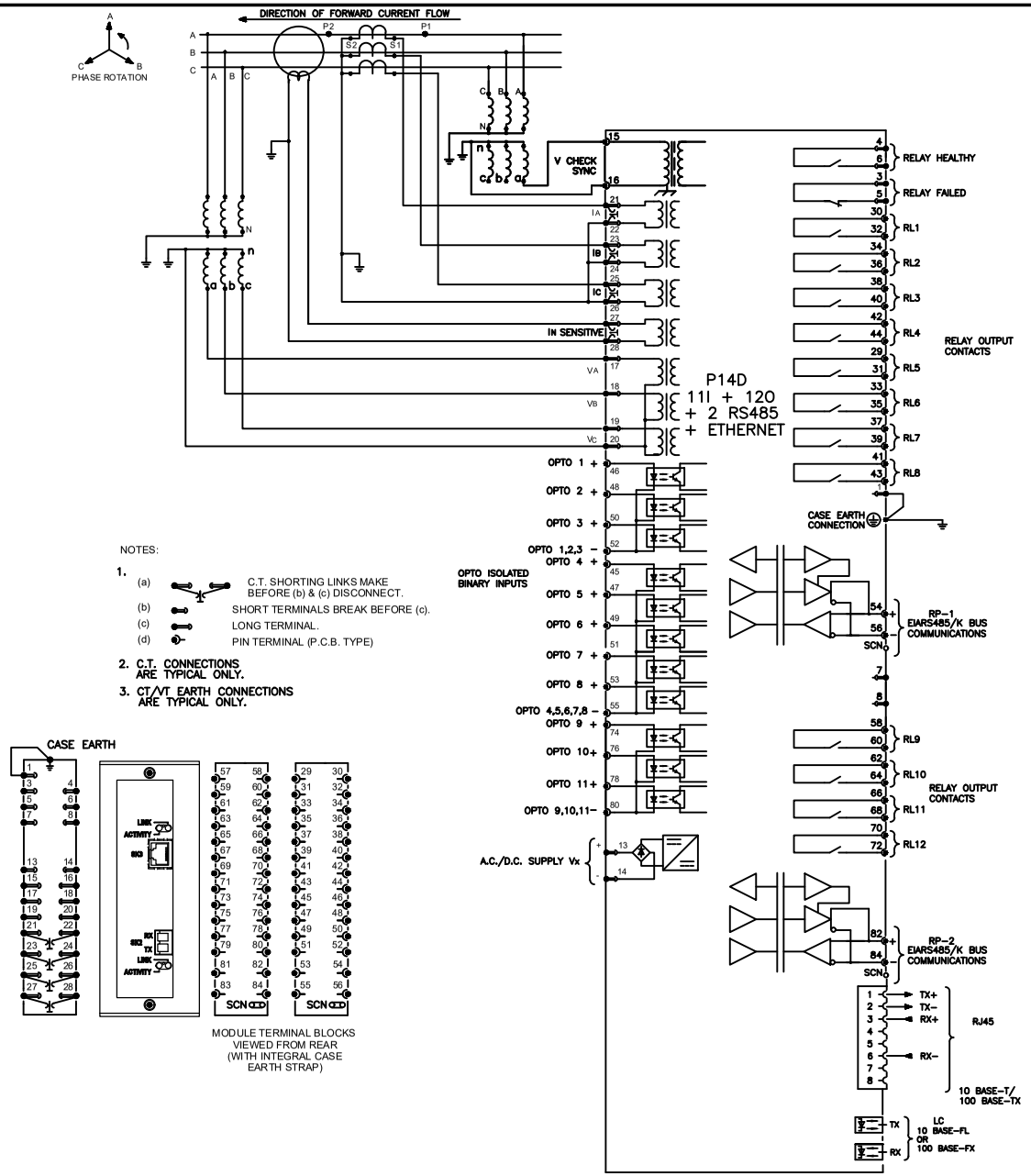


Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH 2 RS485		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P14D06	Sht: 1	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH 2 RS485 & ETHERNET	
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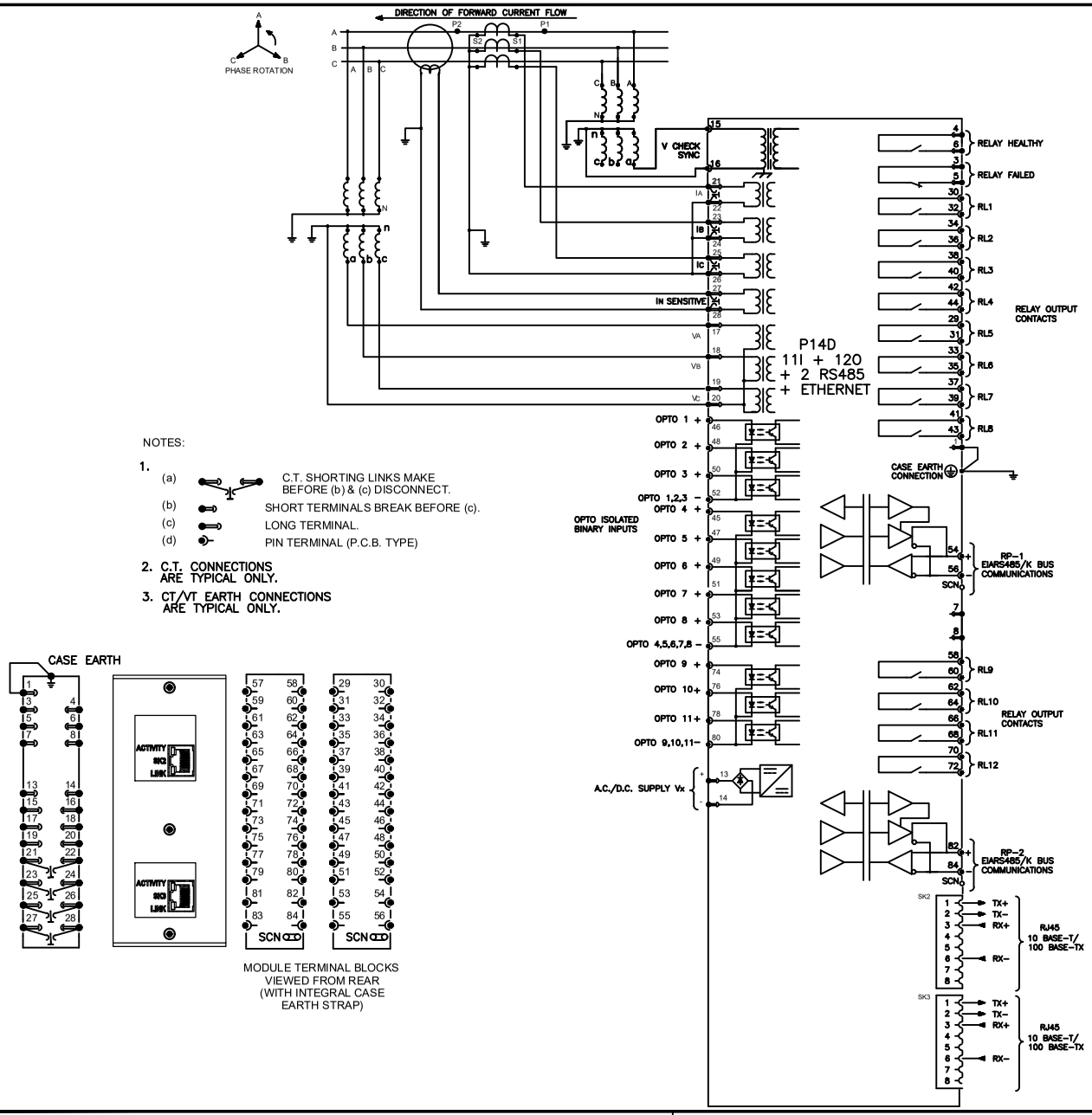
Date:	Chkd: TEOH C.P.			© UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK

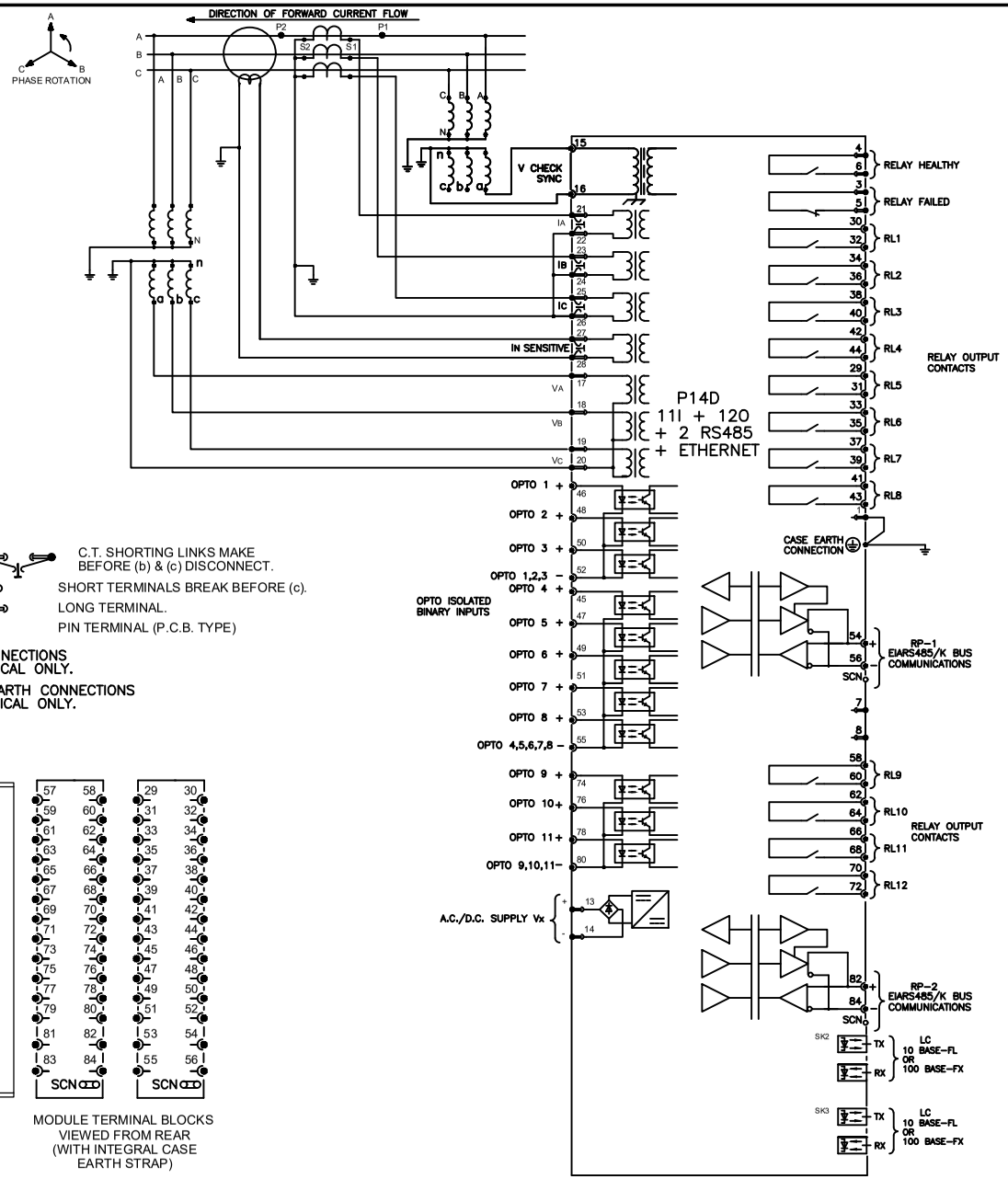


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. CT/VT EARTH CONNECTIONS ARE TYPICAL ONLY.

MODULE TERMINAL BLOCKS VIEWED FROM REAR (WITH INTEGRAL CASE EARTH STRAP)

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (11 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D06	Sht: 3	© UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date:	Chkd: TEOH C.P.			Next Sht: 4	



NOTES:

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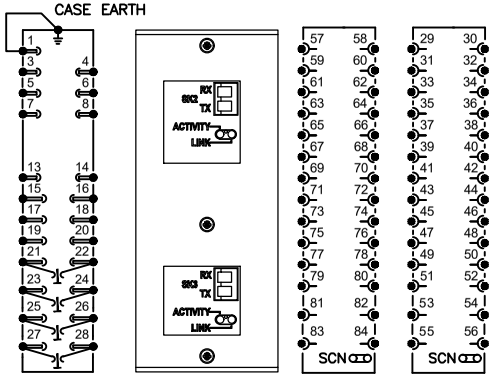
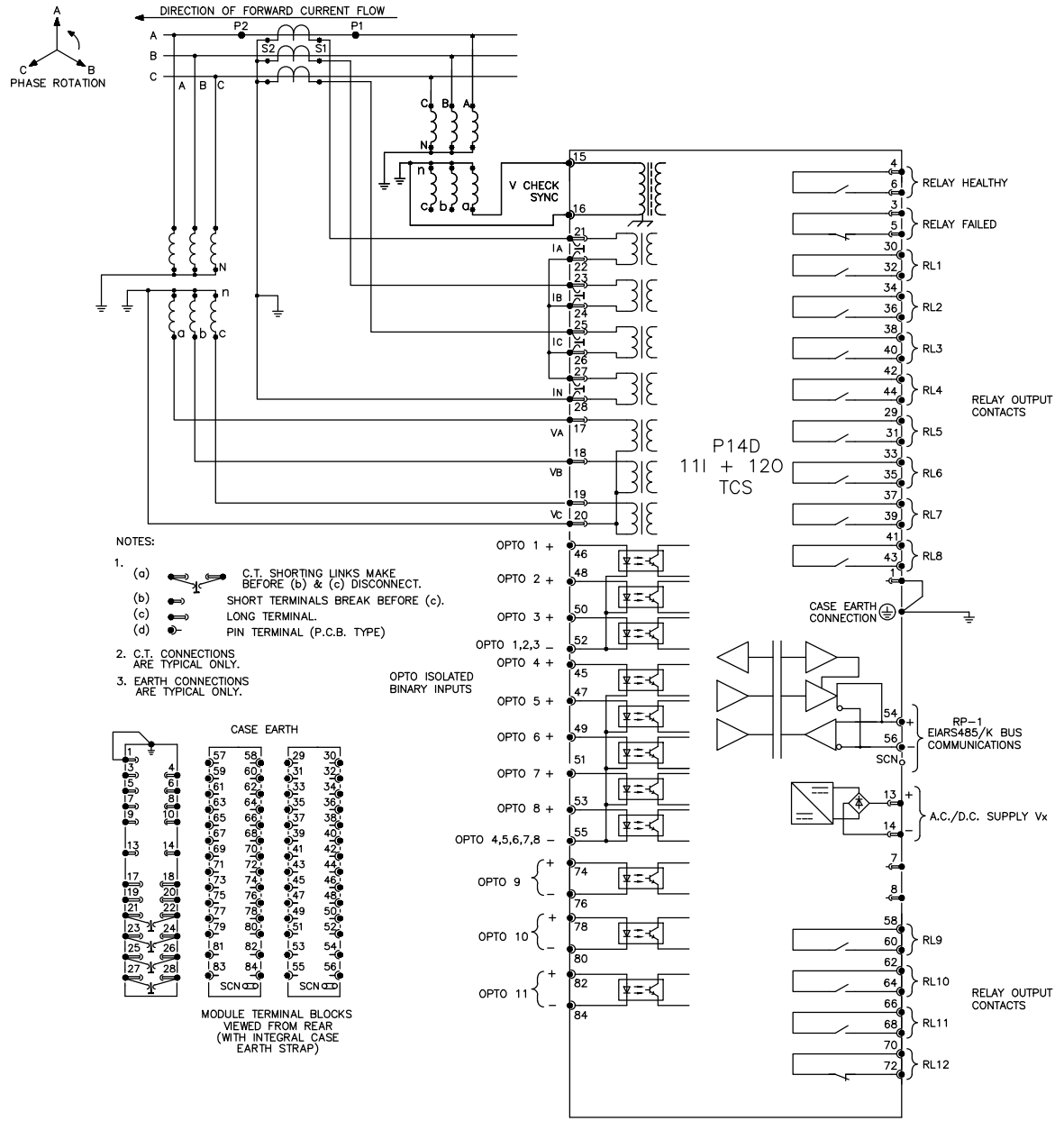
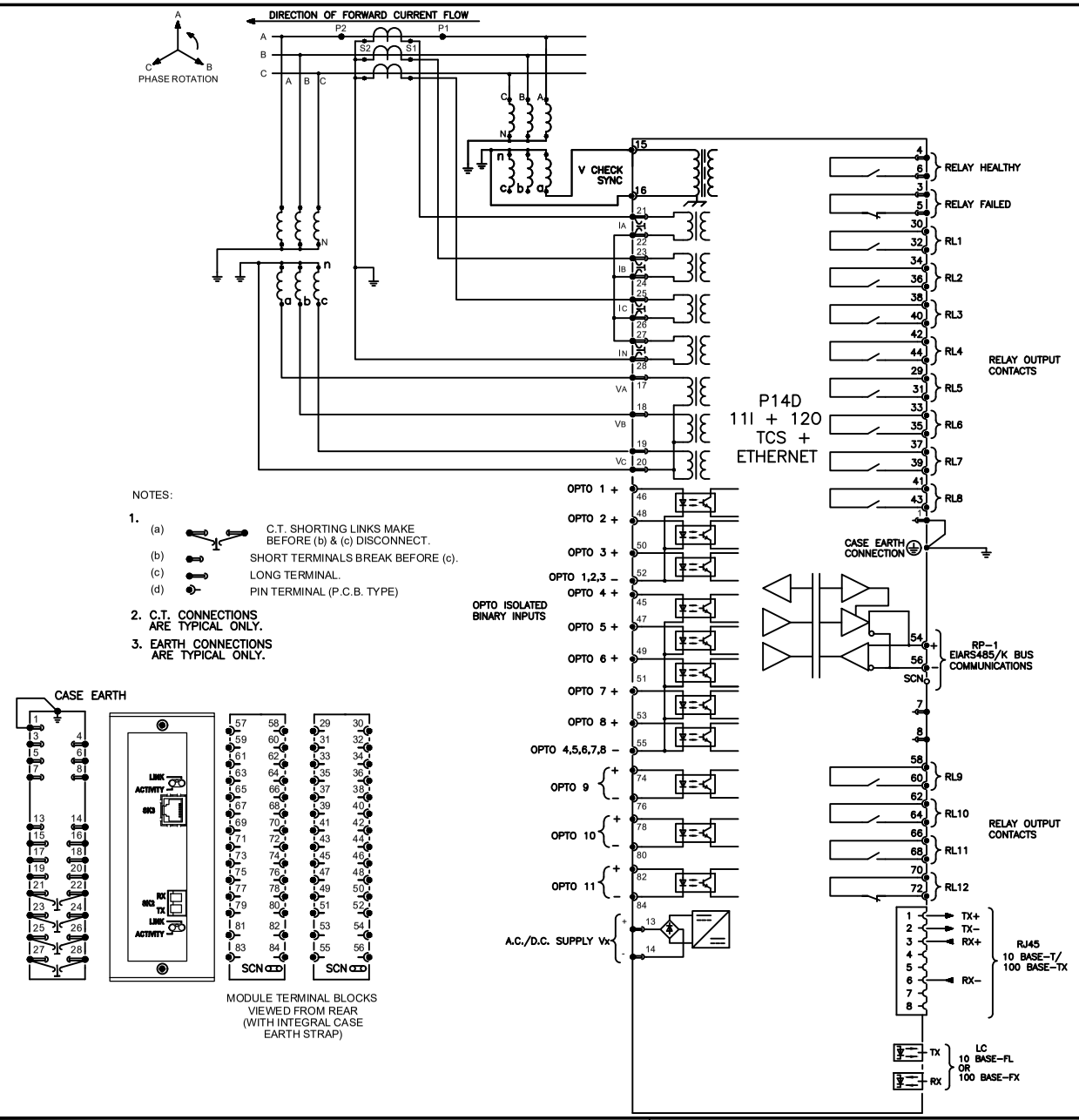


MODULE TERMINAL BLOCKS VIEWED FROM REAR (WITH INTEGRAL CASE EARTH STRAP)

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (11 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D06	Sht: 4	© UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date:	Chkd: TEOH C.P.			Next Sht: -	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (11 I/P & 12 O/P) WITH TCS		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D07	Sht: 1	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. EARTH CONNECTIONS ARE TYPICAL ONLY.

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (11 I/P & 12 O/P) WITH TCS & ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D07	Sht: 2
Date:	Chkd: TEOH C.P.			Next Sht: 3

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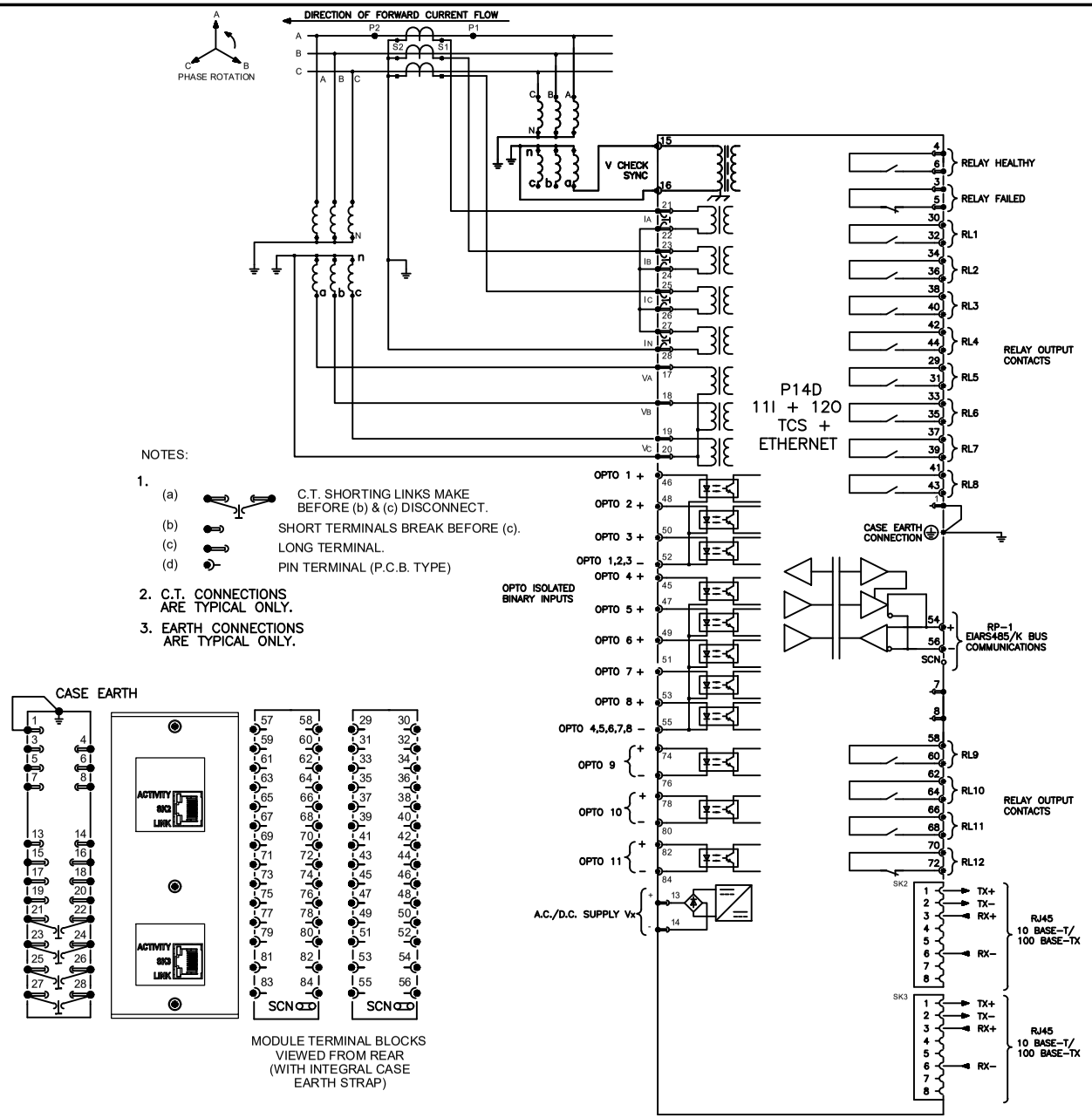

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
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Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & E/F (11 I/P & 12 O/P) WITH TCS & DUAL COPPER ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D07	Sht: 3
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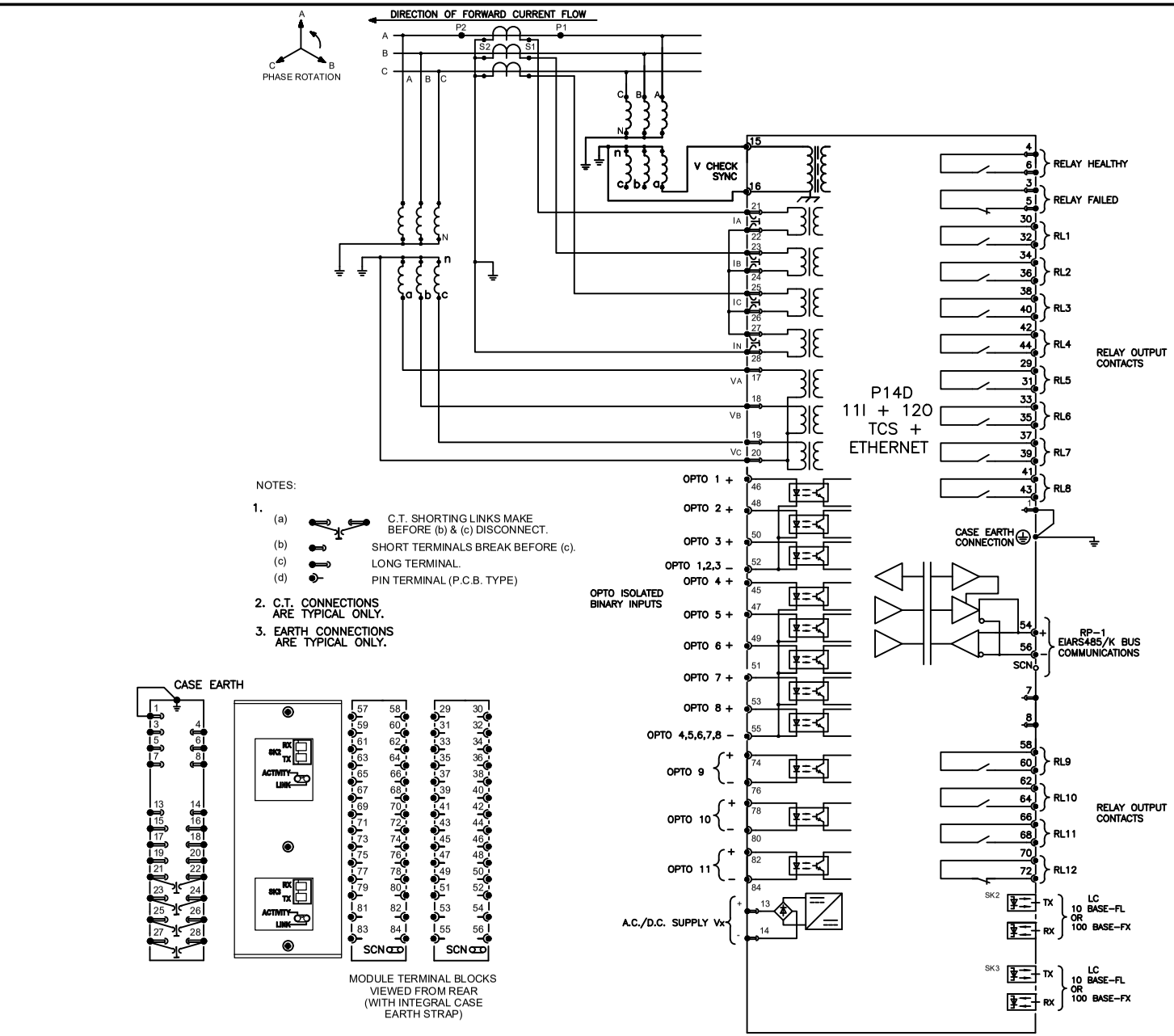

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & E/F (11 I/P & 12 O/P) WITH TCS & DUAL FIBRE ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D07	Sht: 4
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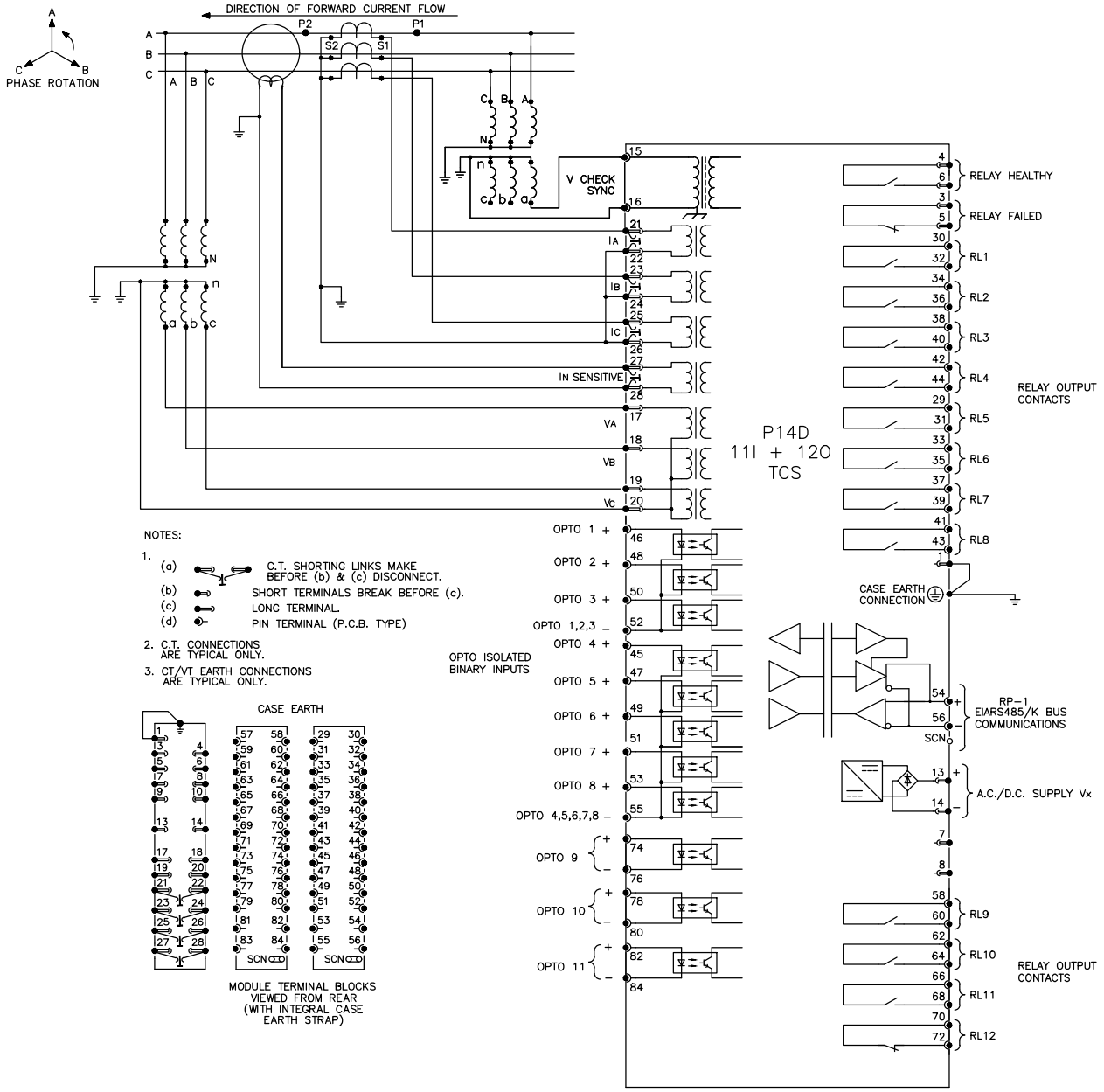
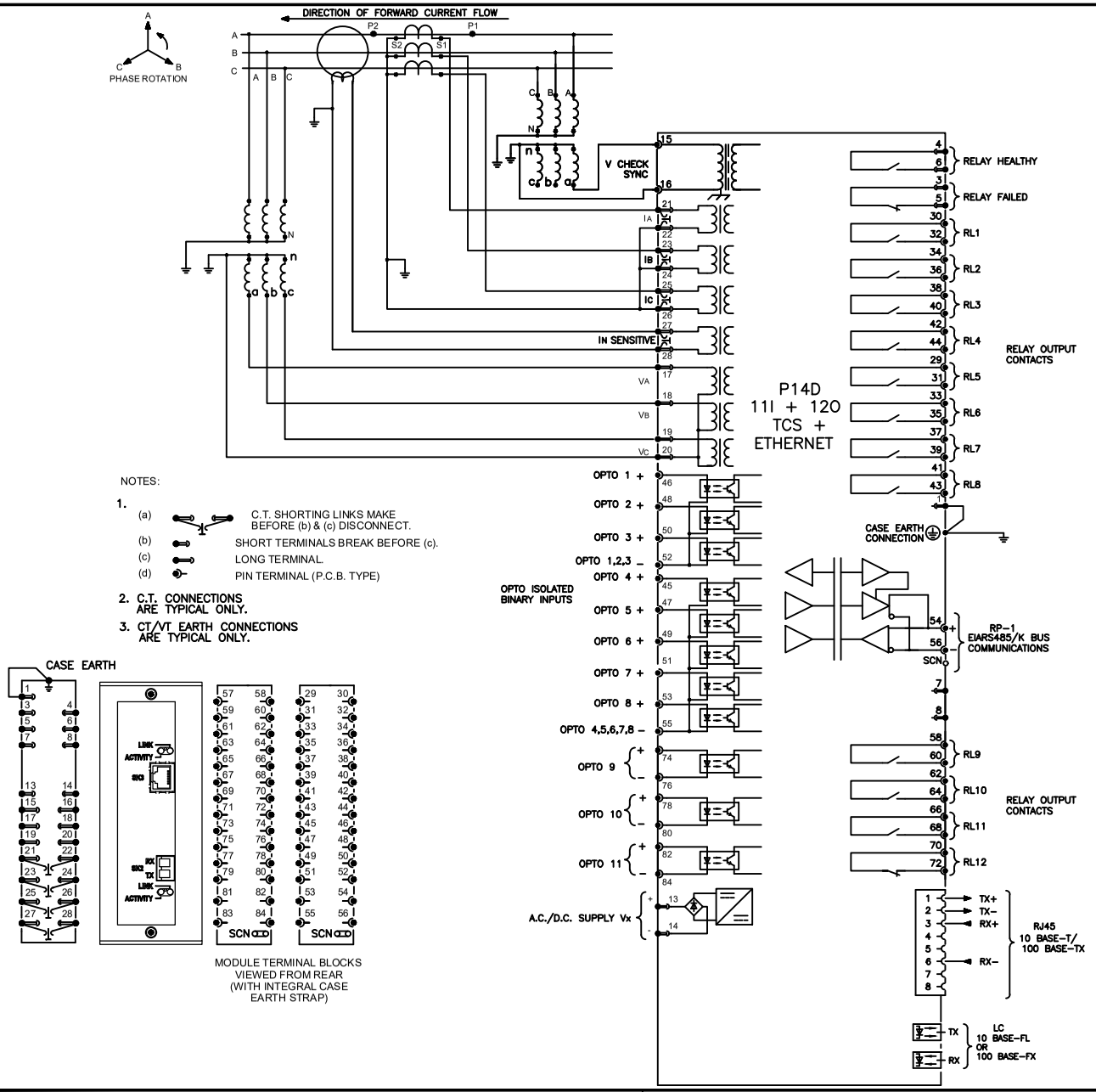


Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH TCS		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D08	Sht: 1	
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -	St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (11 I/P & 12 O/P) WITH TCS & ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D08	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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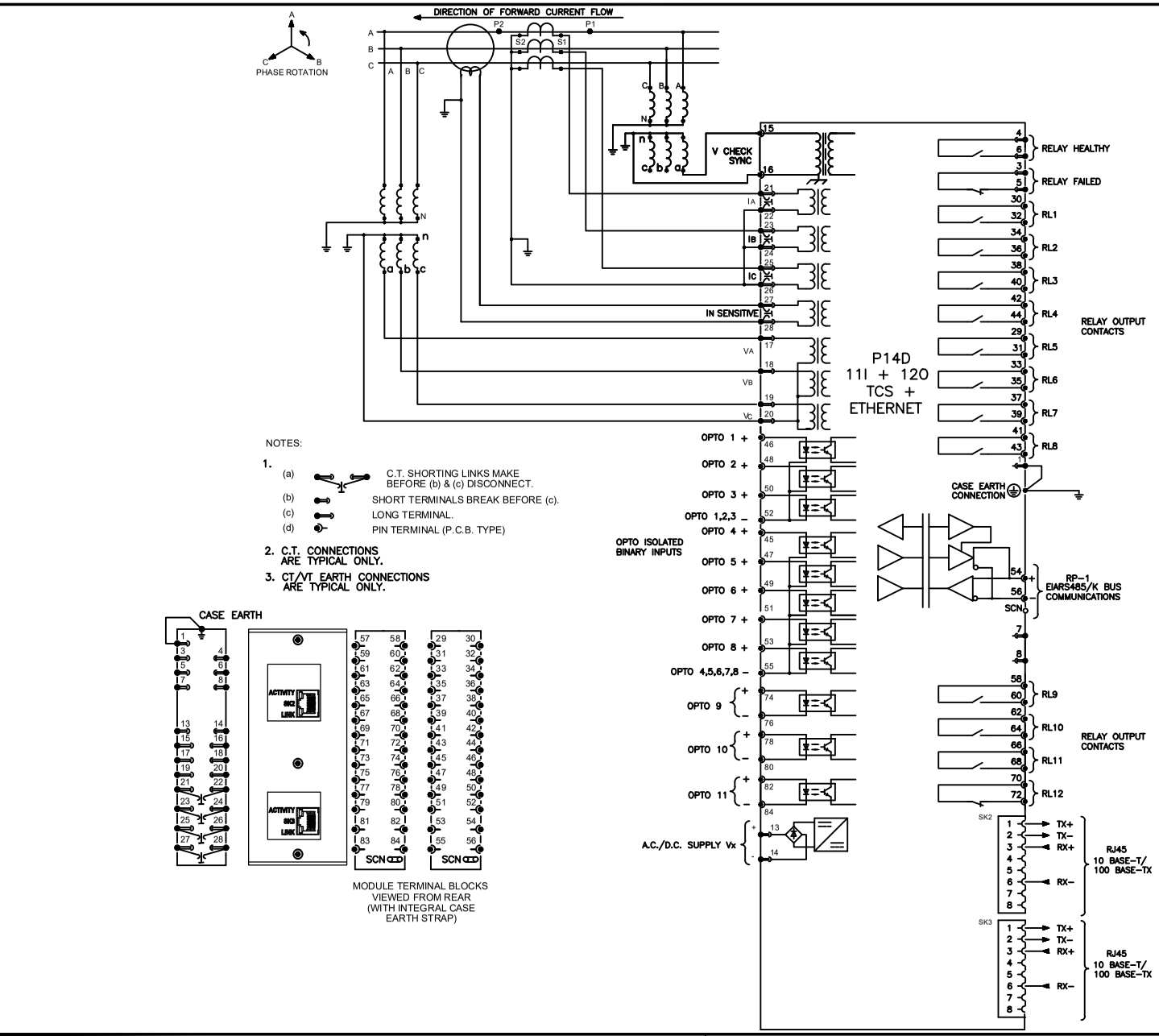

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (11 I/P & 12 O/P) WITH TCS & DUAL COPPER ETHERNET		
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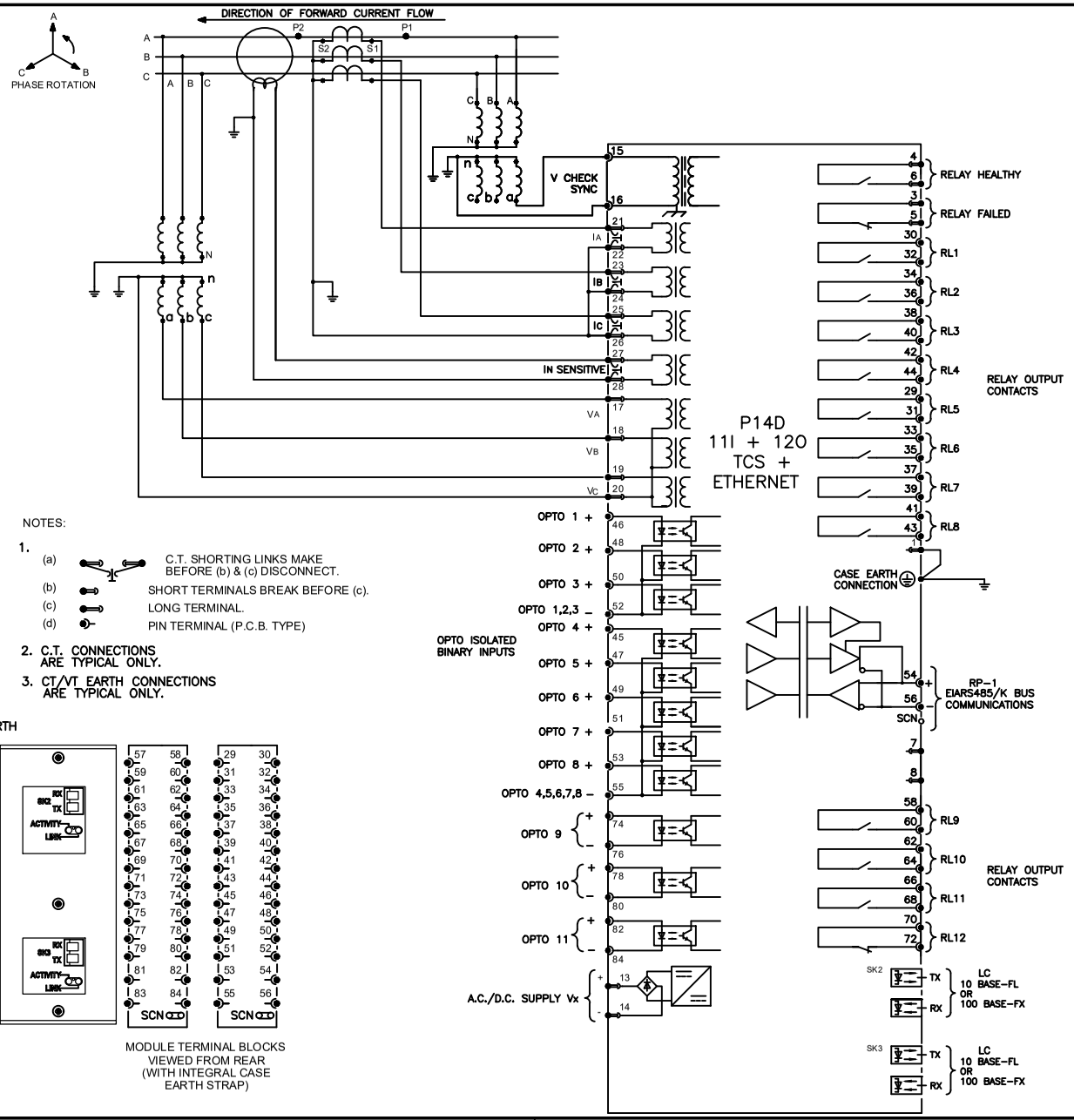

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (11 I/P & 12 O/P) WITH TCS & DUAL FIBRE ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D08	Sht: 4	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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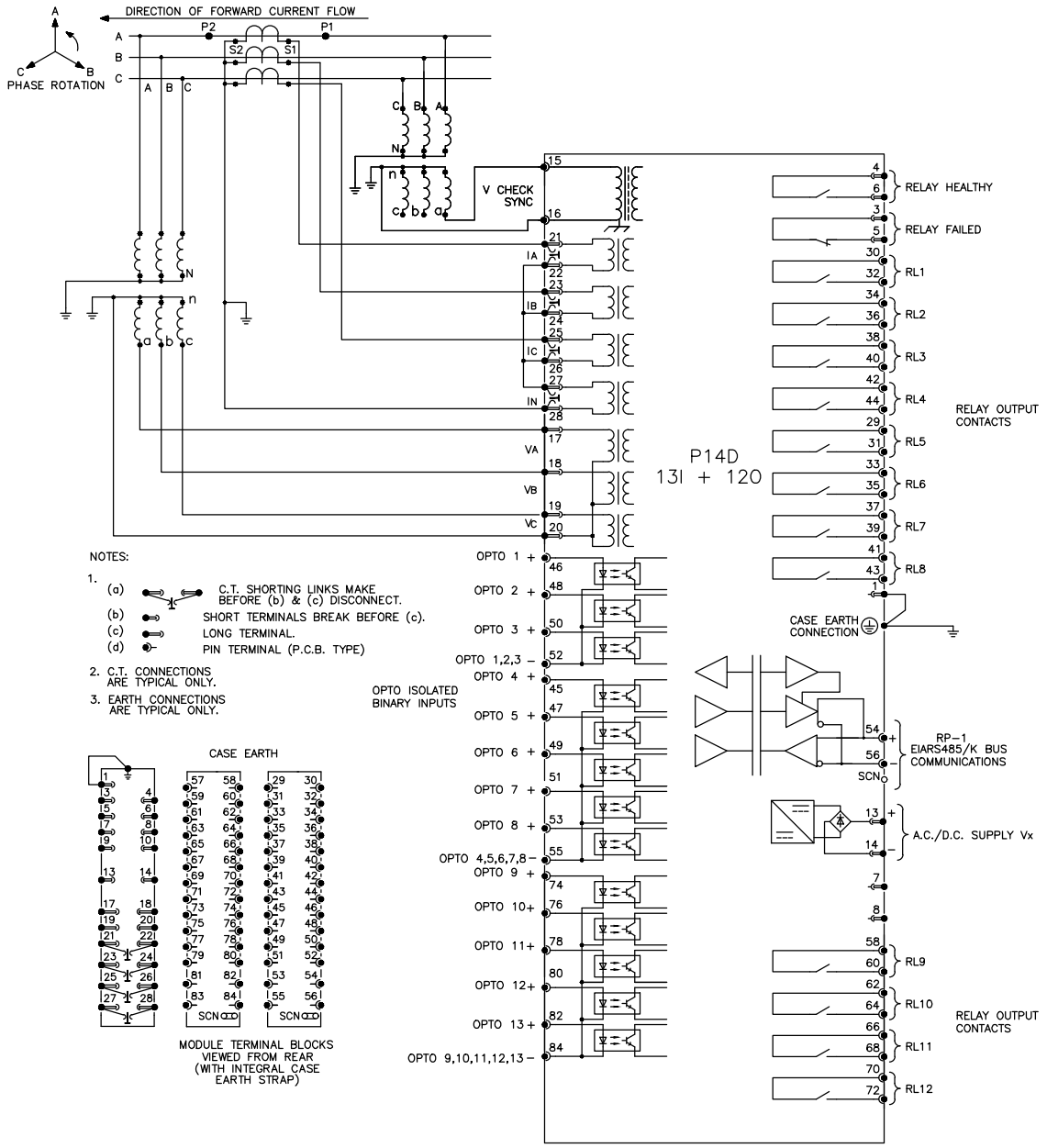

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (13 I/P & 12 O/P)		
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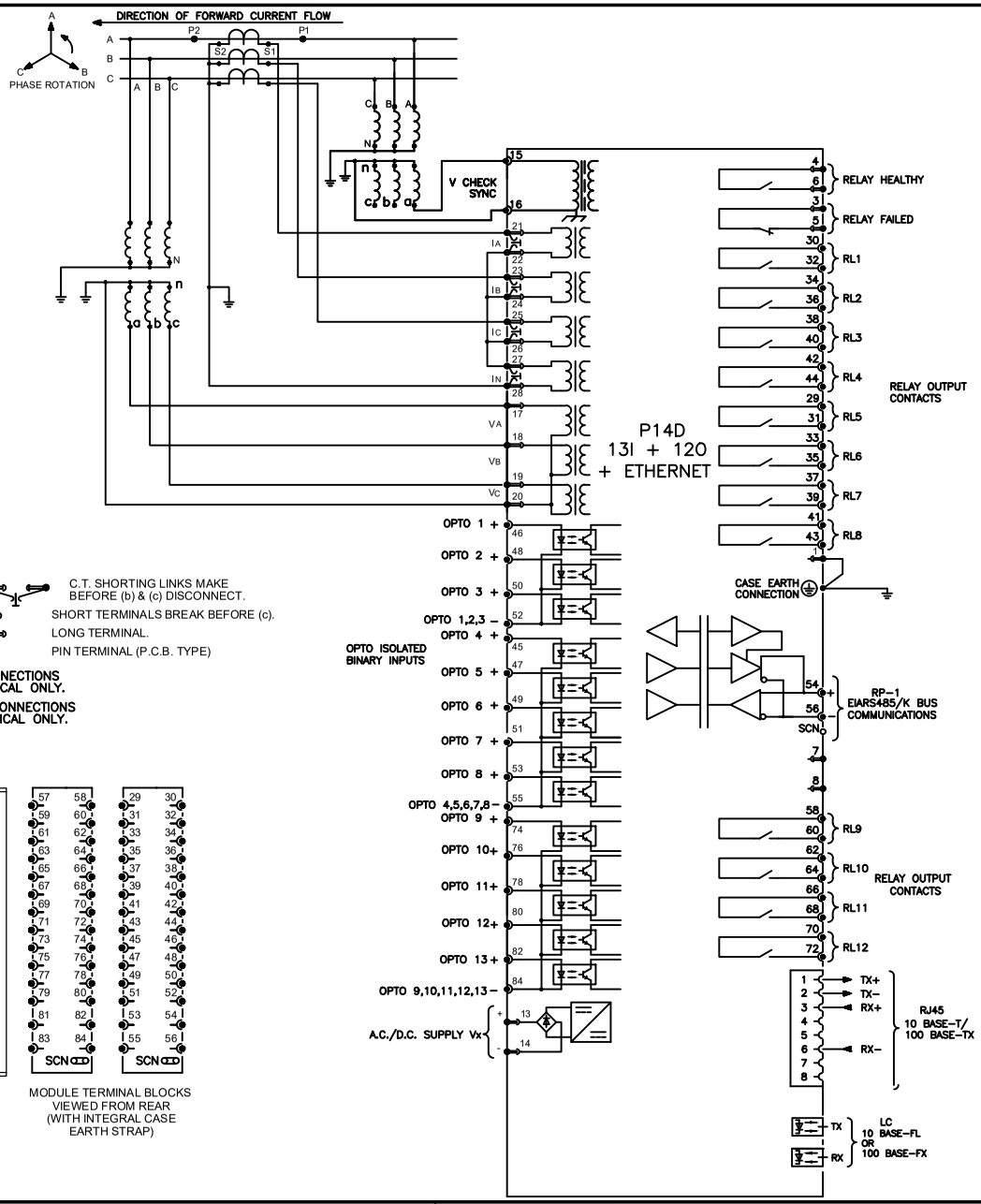
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & E/F (13 I/P & 12 O/P) WITH ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D09	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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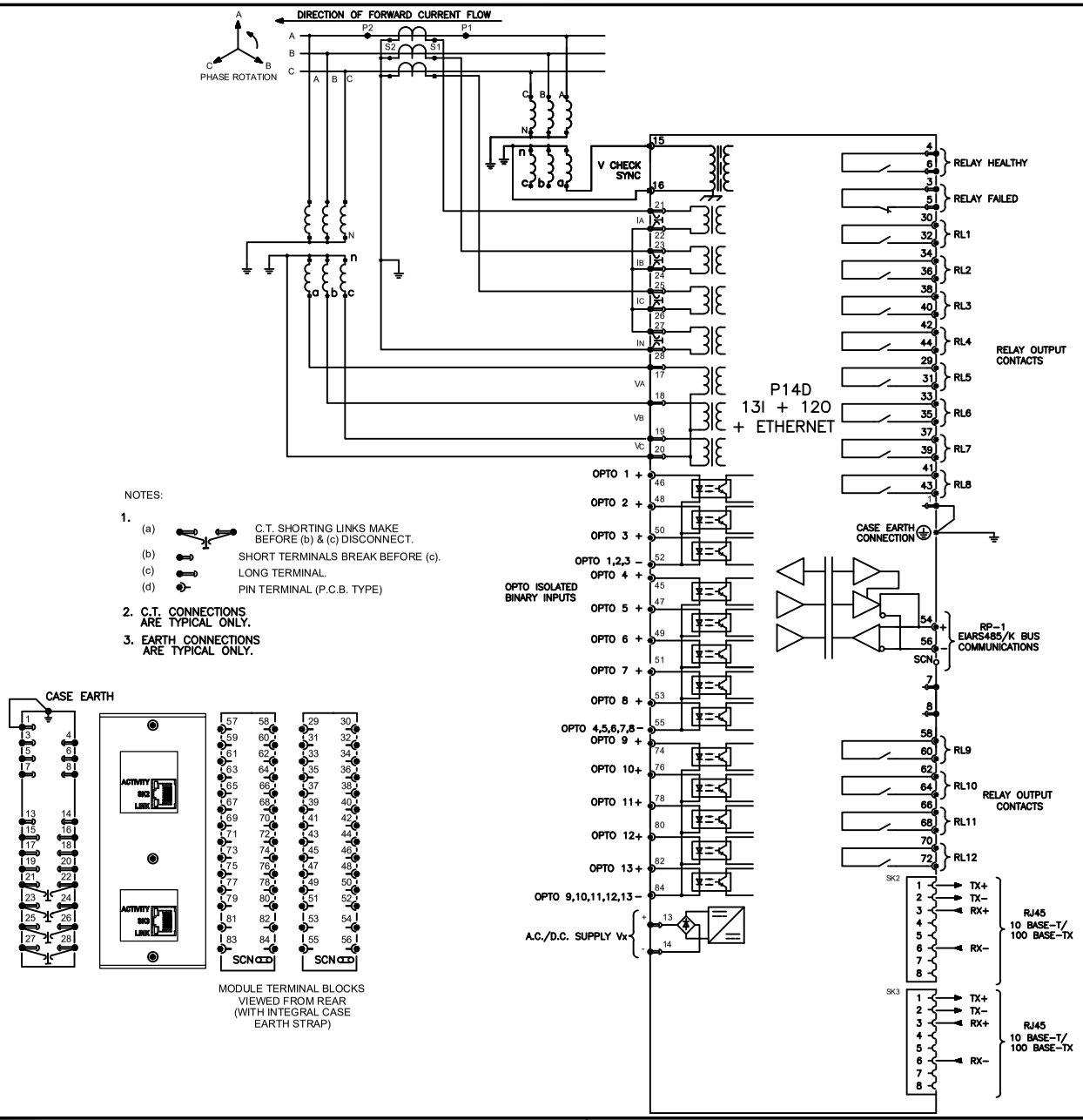

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. EARTH CONNECTIONS ARE TYPICAL ONLY.

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (13 I/P & 12 O/P) & DUAL COPPER ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D09	Sht: 3
Date:	Chkd: TEOH C.P.			Next Sht: 4

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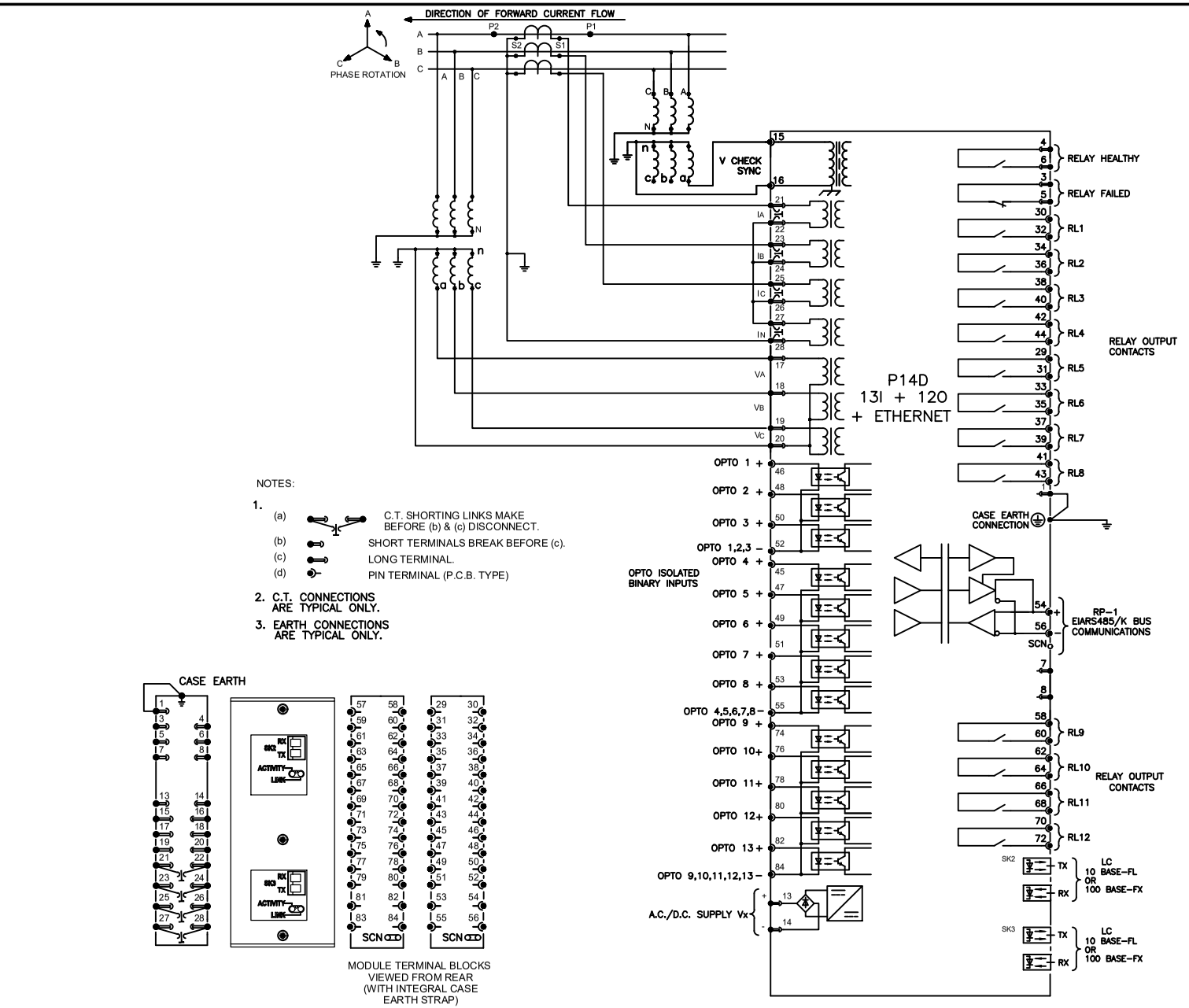

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (13 I/P & 12 O/P) & DUAL FIBRE ETHERNET		
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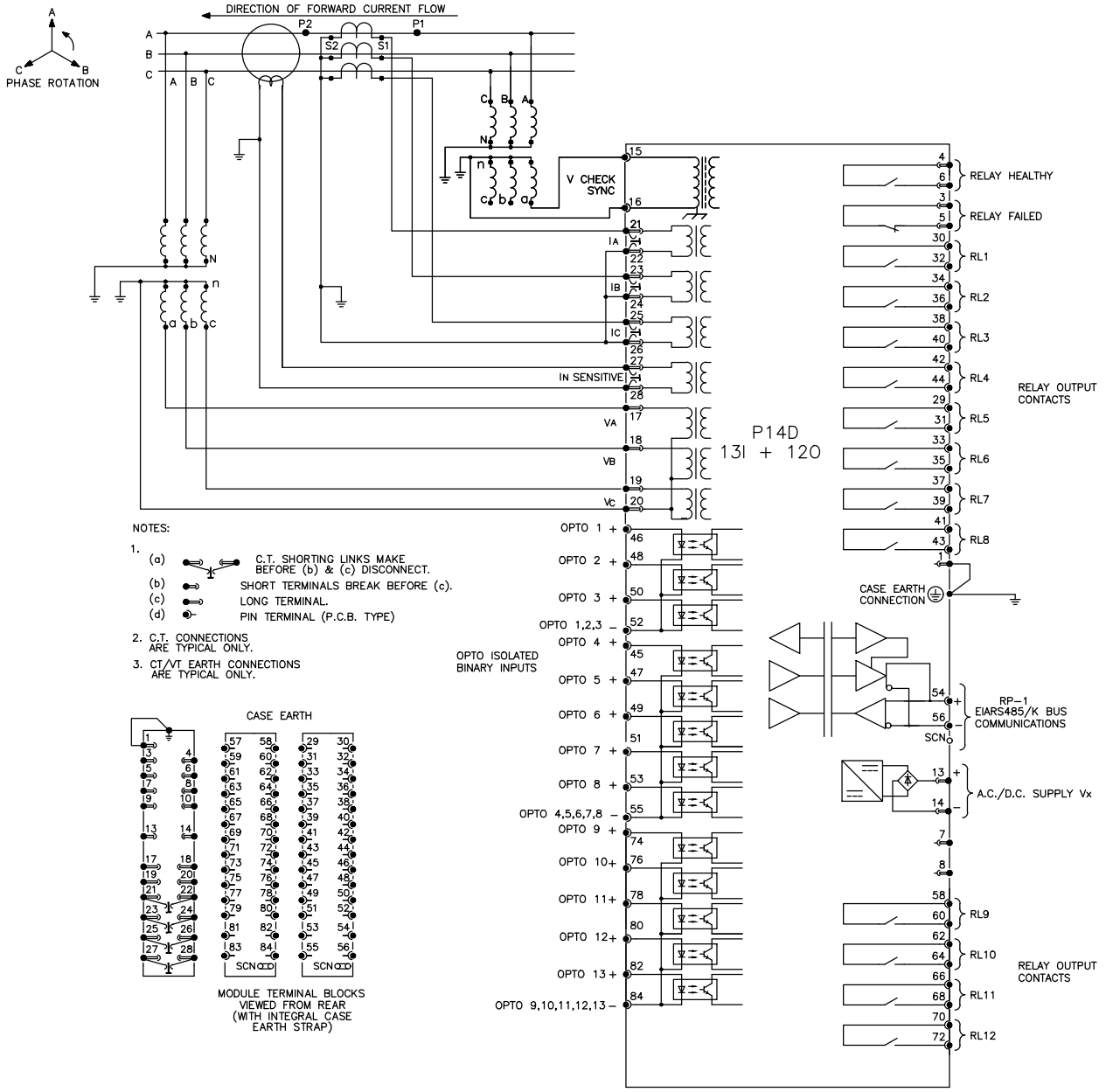
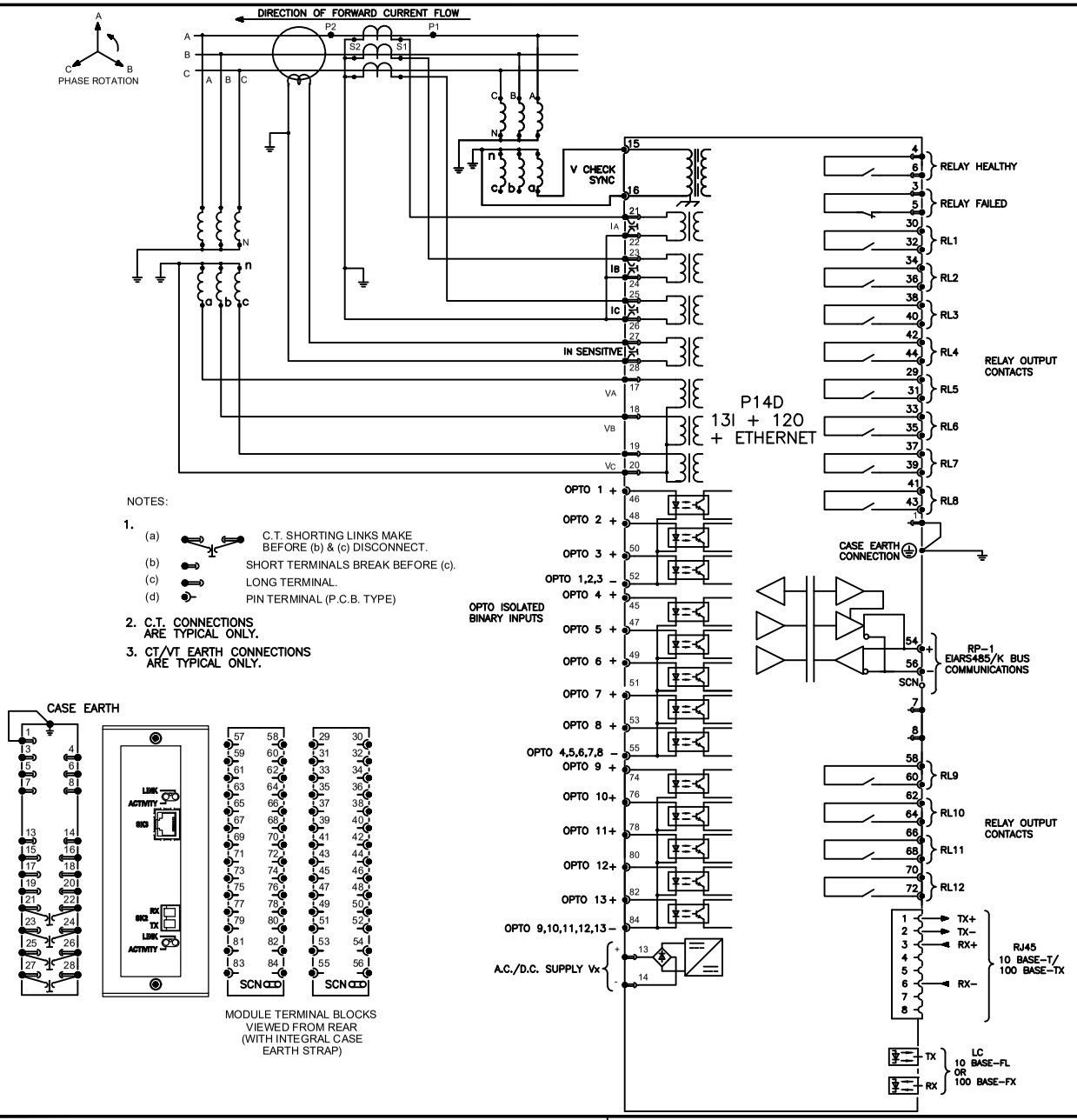


Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (13 I/P & 12 O/P)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D10	Sht: 1	
Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -	St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (13 I/P & 12 O/P) & ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D10	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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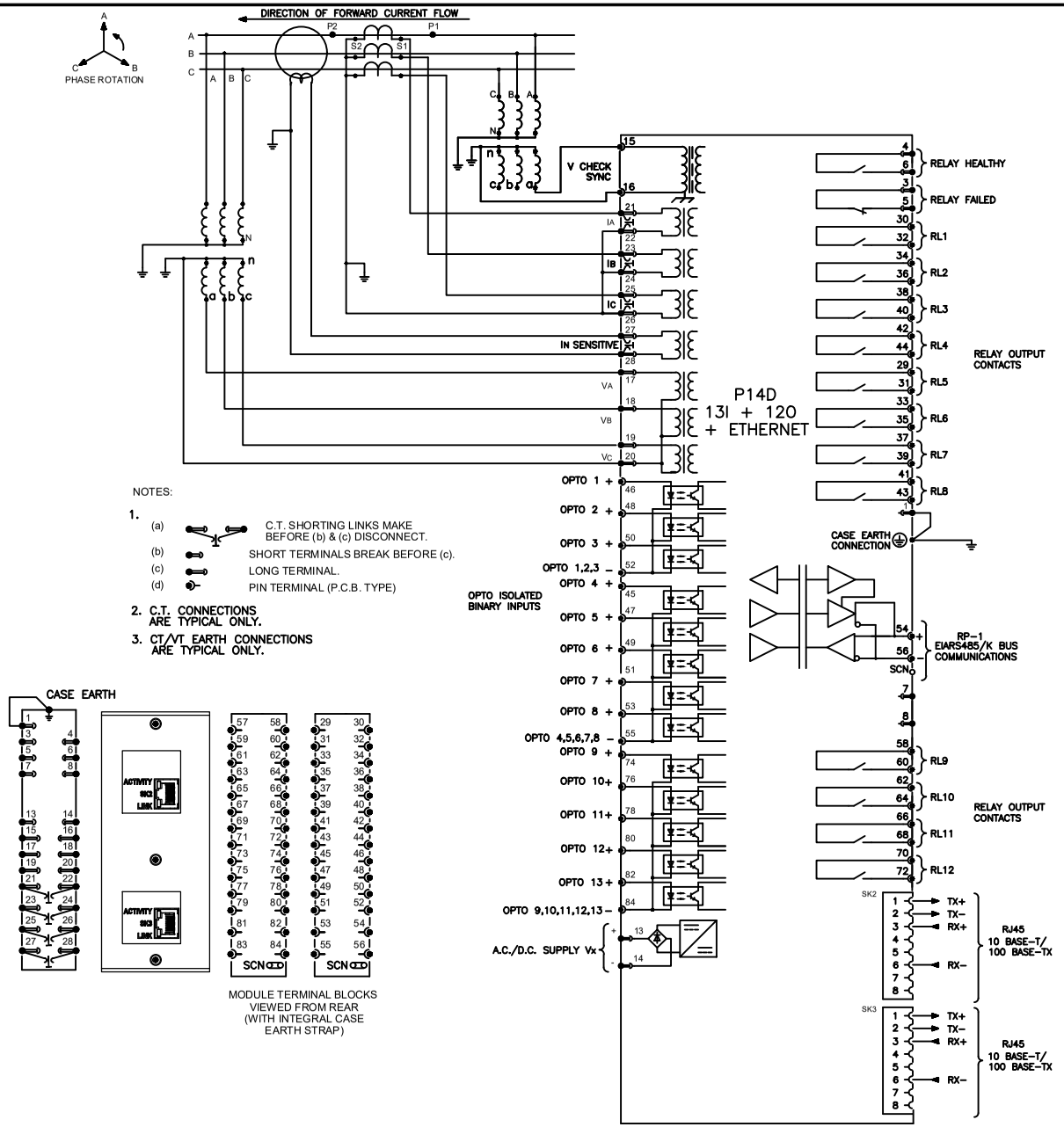

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (13 I/P & 12 O/P) & DUAL COPPER ETHERNET		
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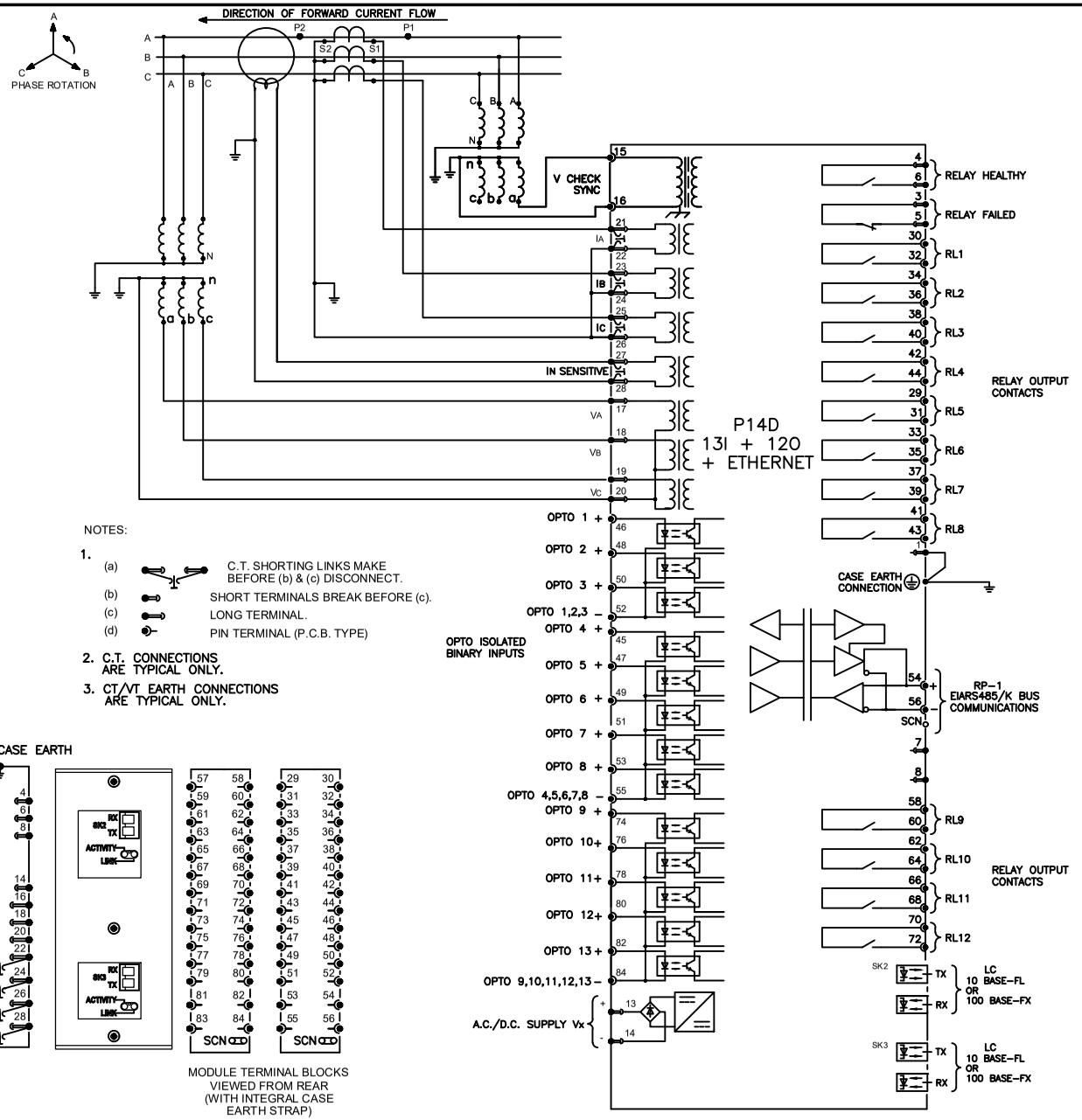

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (13 I/P & 12 O/P) & DUAL FIBRE ETHERNET		
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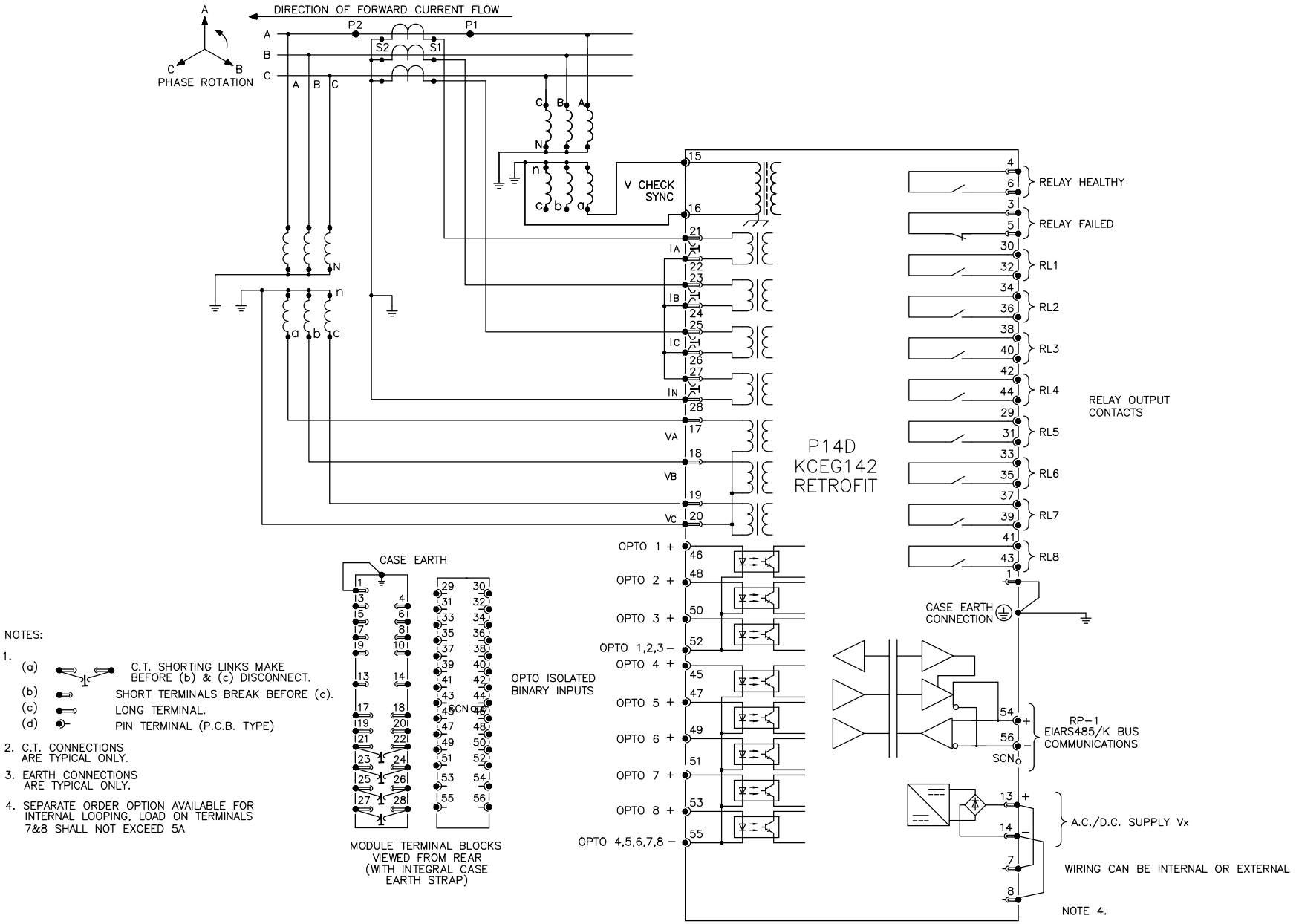

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. C.T. CONNECTIONS ARE TYPICAL ONLY.
3. EARTH CONNECTIONS ARE TYPICAL ONLY.
4. SEPARATE ORDER OPTION AVAILABLE FOR INTERNAL LOOPING, LOAD ON TERMINALS 7&8 SHALL NOT EXCEED 5A

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P) FOR KCEG 140/142 RETROFIT	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D11	Sht: 1
Date: 13/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -

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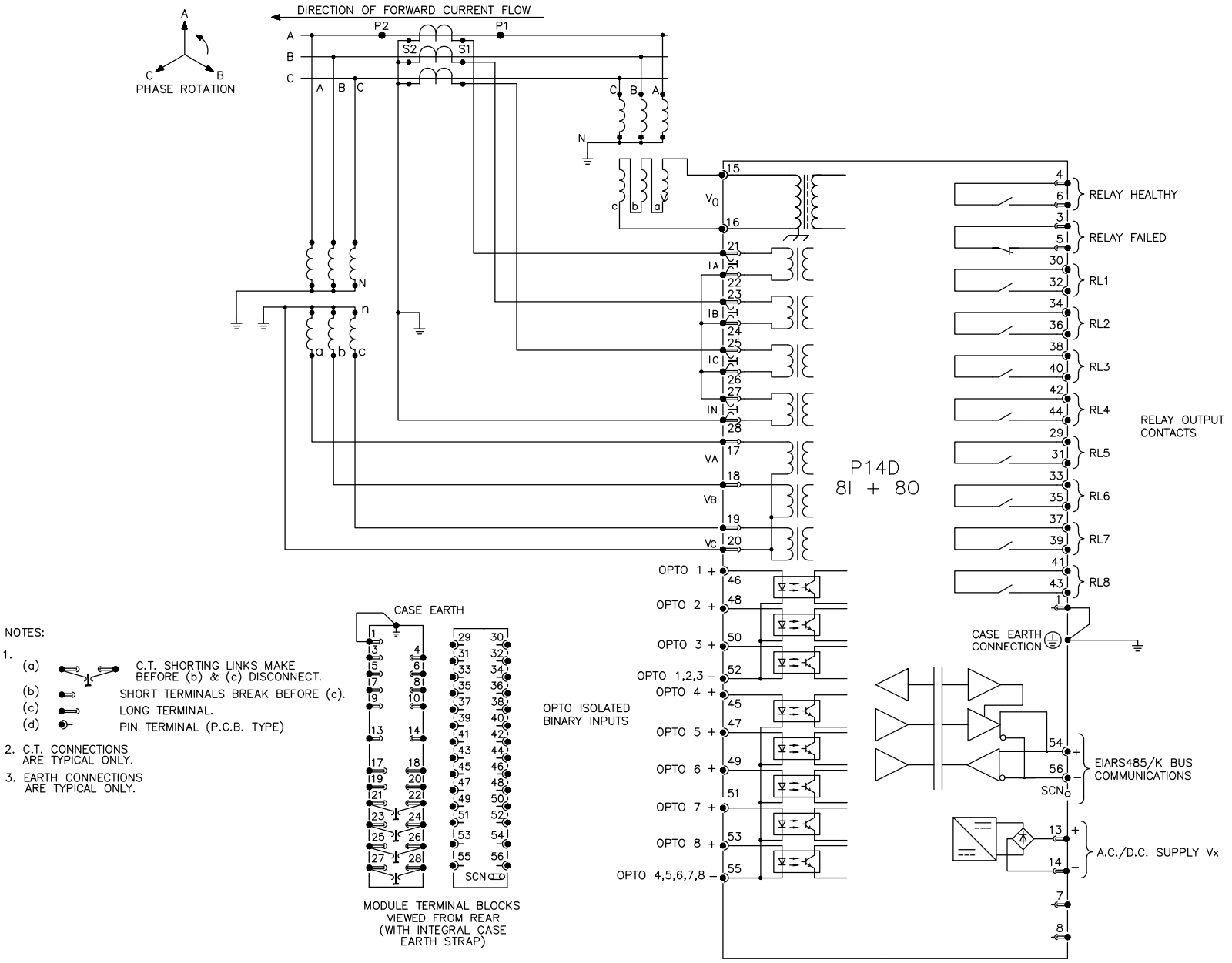

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT WITH SEPERATE RESIDUAL VOLTAGE INPUT 8I/P + 8O/P	
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Date: 03/12/2011	Chkd: K.VENKATARAMAN			Next Sht: -

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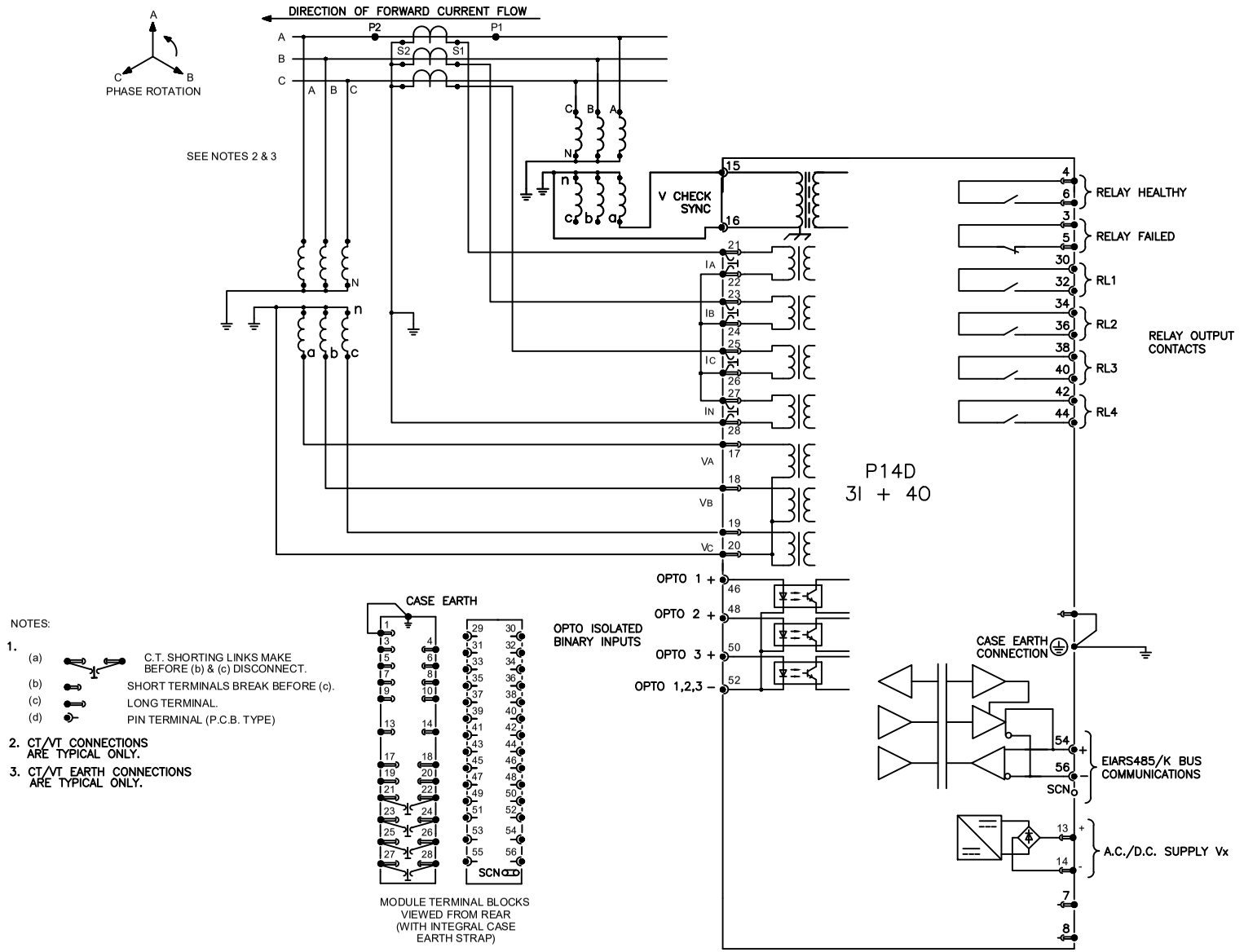

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
   (b) SHORT TERMINALS BREAK BEFORE (c).
   (c) LONG TERMINAL.
   (d) PIN TERMINAL (P.C.B. TYPE)
2. CT/VT CONNECTIONS ARE TYPICAL ONLY.
3. CT/VT EARTH CONNECTIONS ARE TYPICAL ONLY.

Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVER CURRENT AND EARTH FAULT (3 I/P & 4 O/P)		
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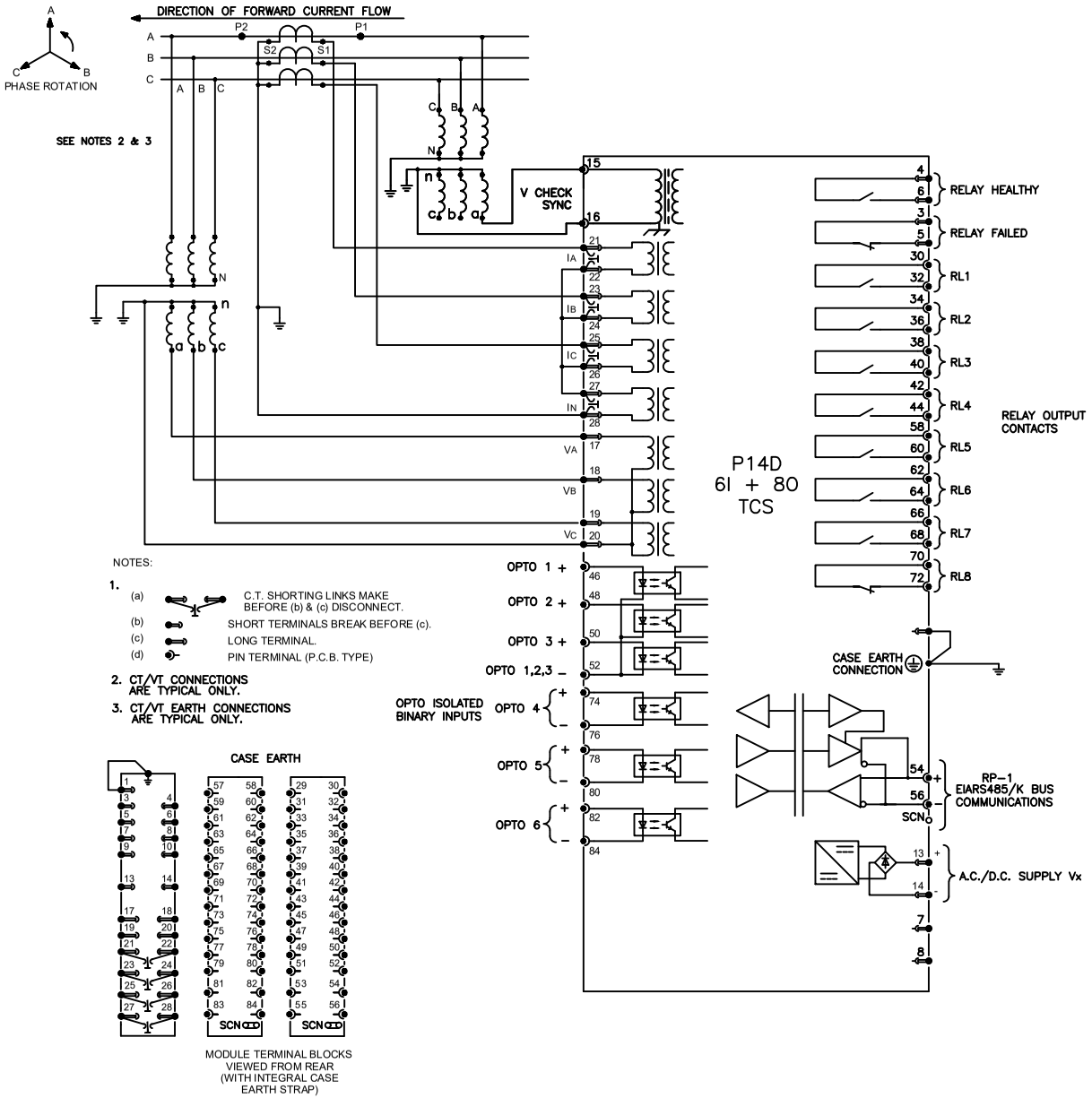

Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVER CURRENT AND EARTH FAULT (6 I/P & 8 O/P) WITH TCS		
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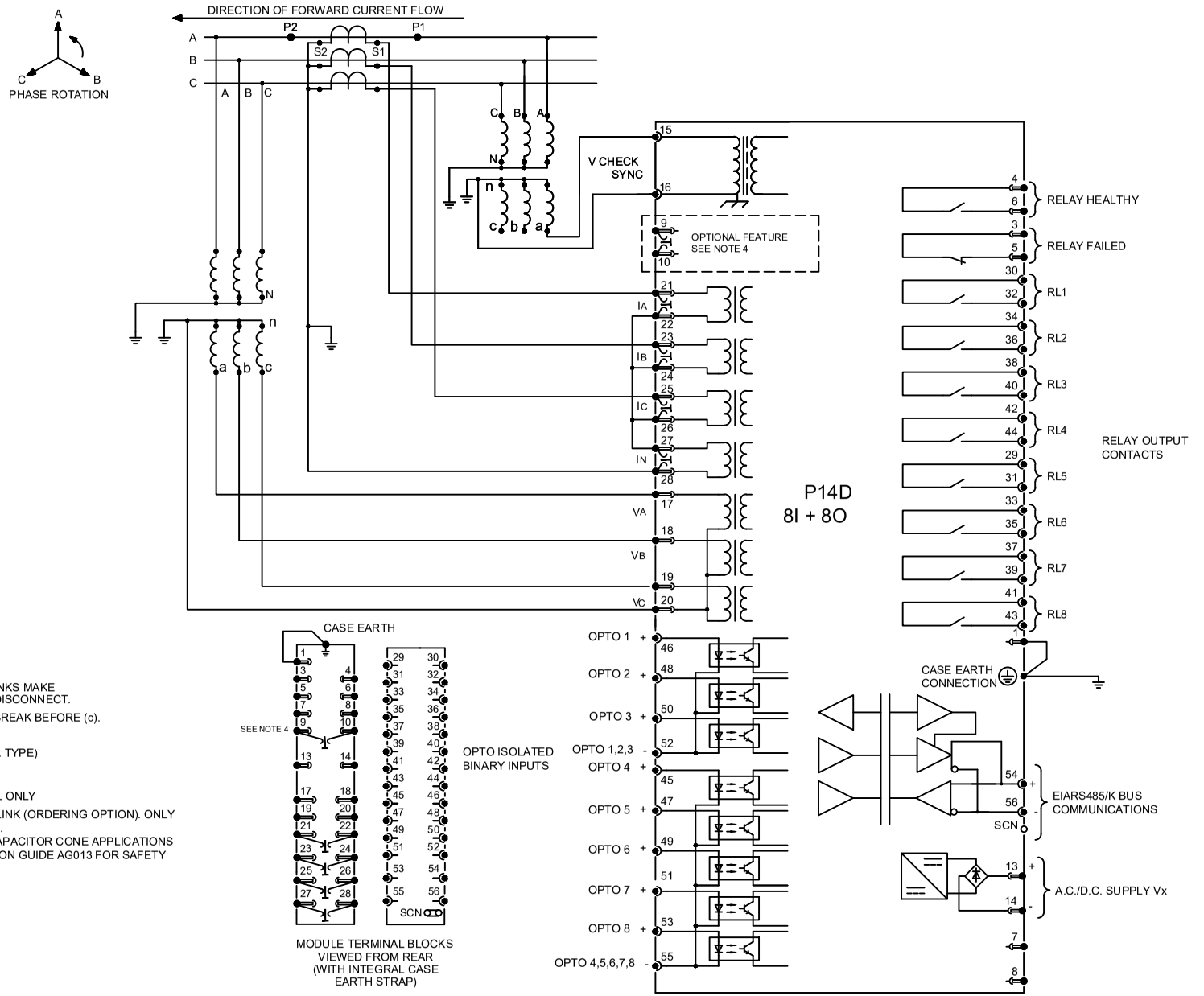

NOTES:

1.
(a) C.T. SHORTING LINKS MAKE BEFORE (b) & (c) DISCONNECT.
(b) SHORT TERMINALS BREAK BEFORE (c).
(c) LONG TERMINAL.
(d) PIN TERMINAL (P.C.B. TYPE)

2. C.T. CONNECTIONS ARE TYPICAL ONLY

3. CT/VT EARTH CONNECTIONS ARE TYPICAL ONLY

4. TERMINALS 9 & 10: OPTIONAL SHORTING LINK (ORDERING OPTION). ONLY AVAILABLE FOR THE 30TE MODEL VARIANTS.
WHEN THESE TERMINALS ARE USED FOR CAPACITOR CONE APPLICATIONS PLEASE REFER TO ALSTOM GRID APPLICATION GUIDE AG013 FOR SAFETY PROCEDURE.

Issue: D	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND EARTH FAULT (8 I/P & 8 O/P) - WITH OPTIONAL SHORTING LINK	
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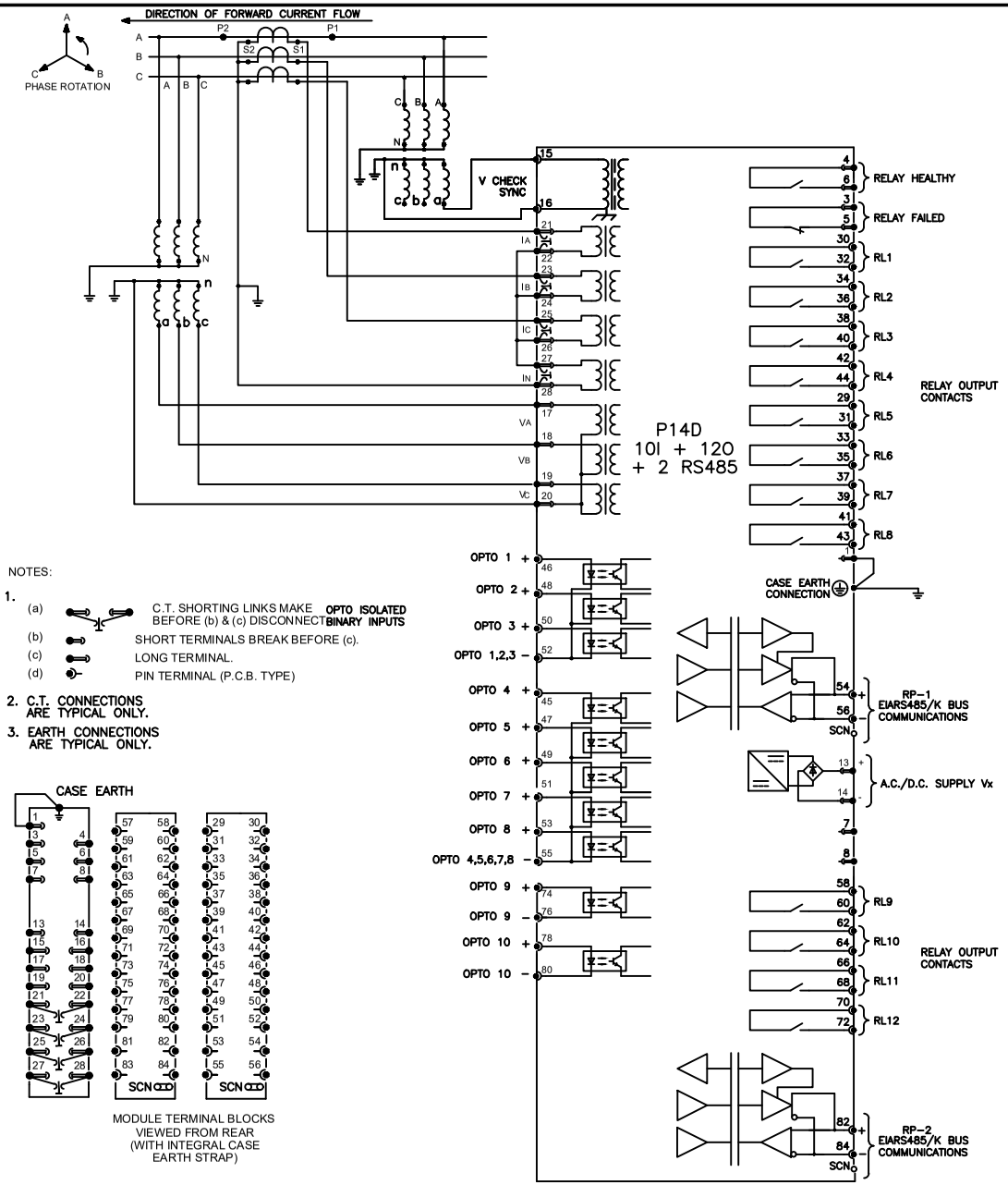

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (10 I/P & 12 O/P) WITH 2 RS485	
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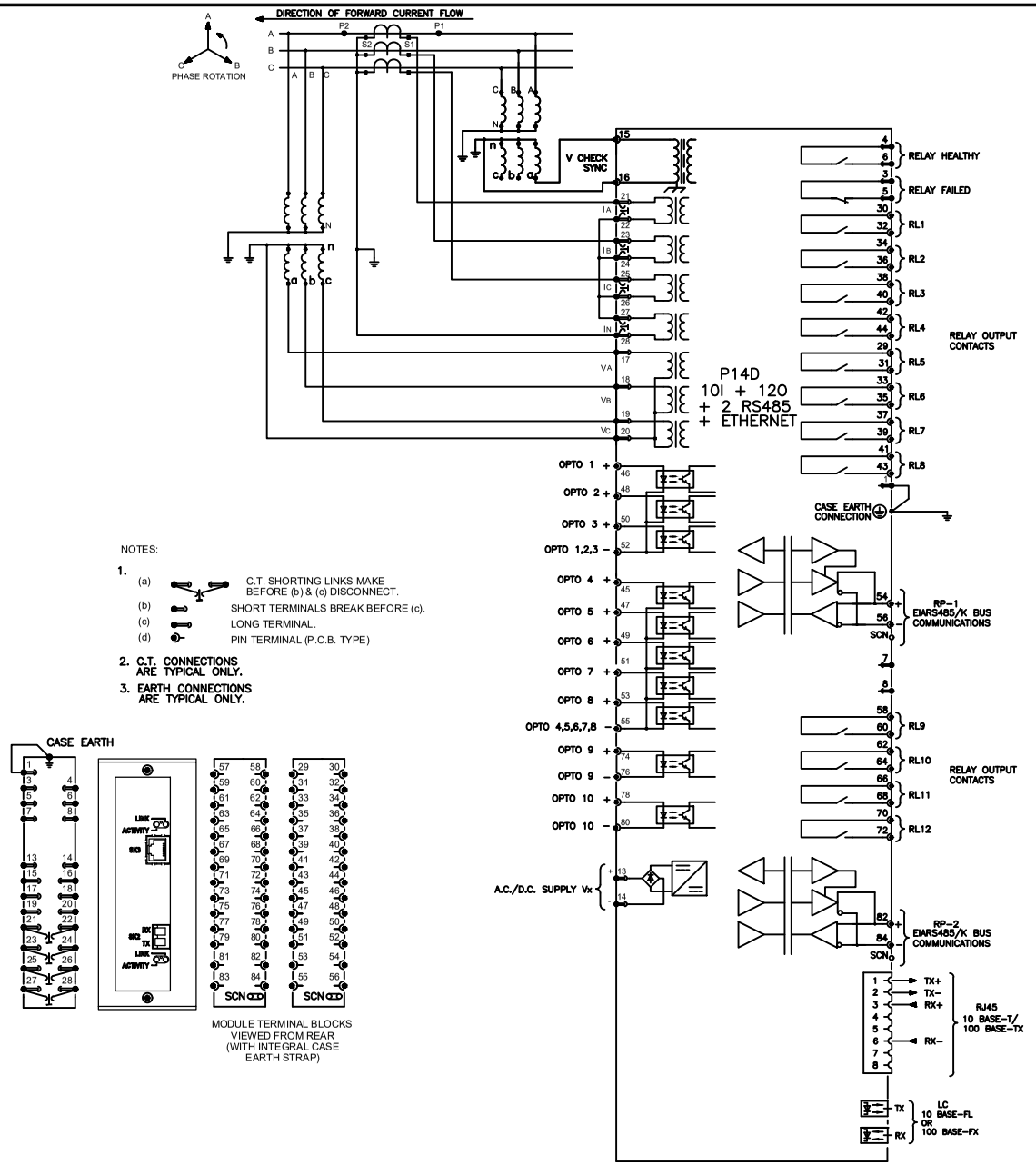
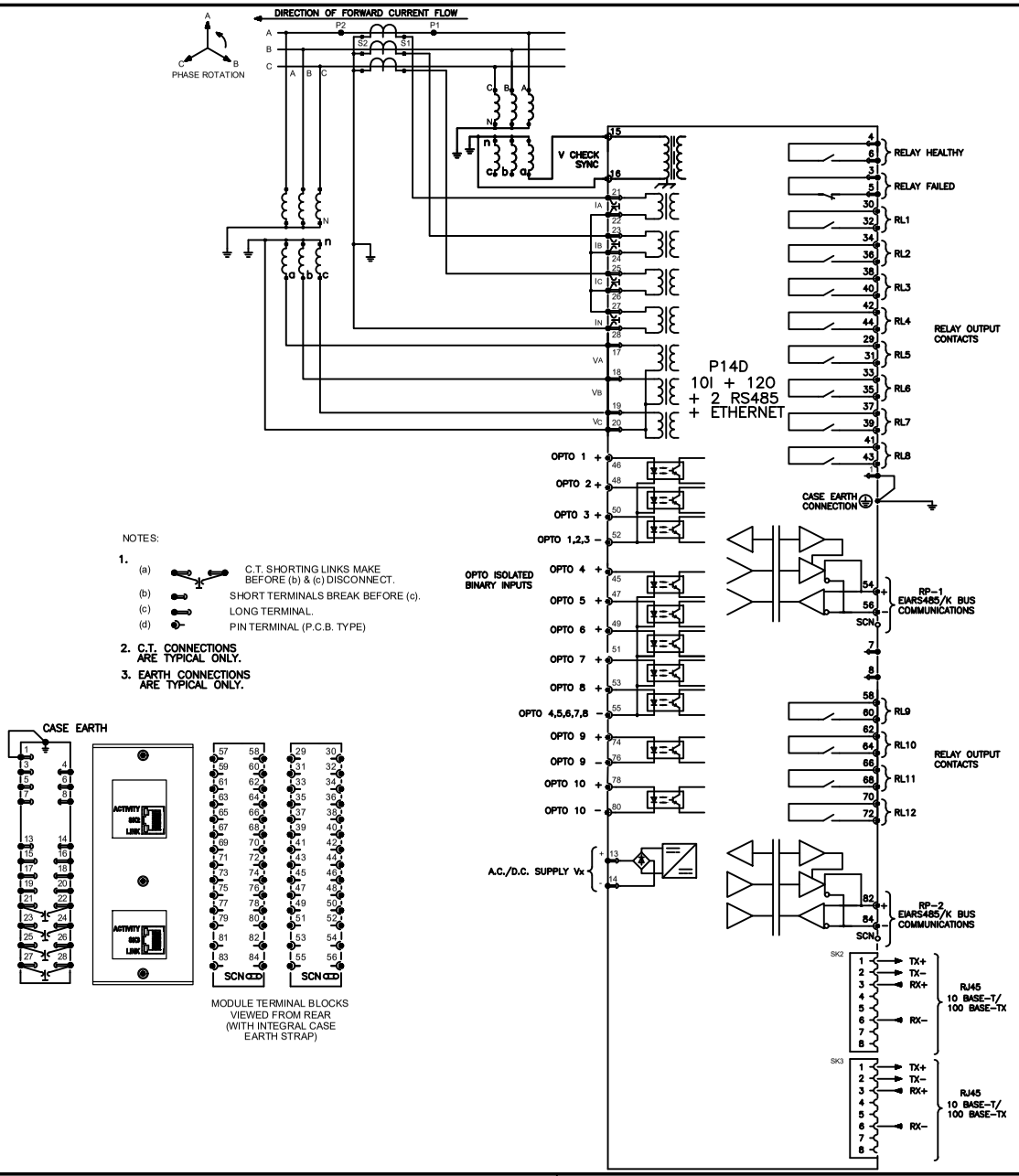


Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (10 I/P & 12 O/P) WITH 2 RS485 & ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D16	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date:	Chkd: TEOH C.P.			Next Sht: 3	



Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (10 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET		
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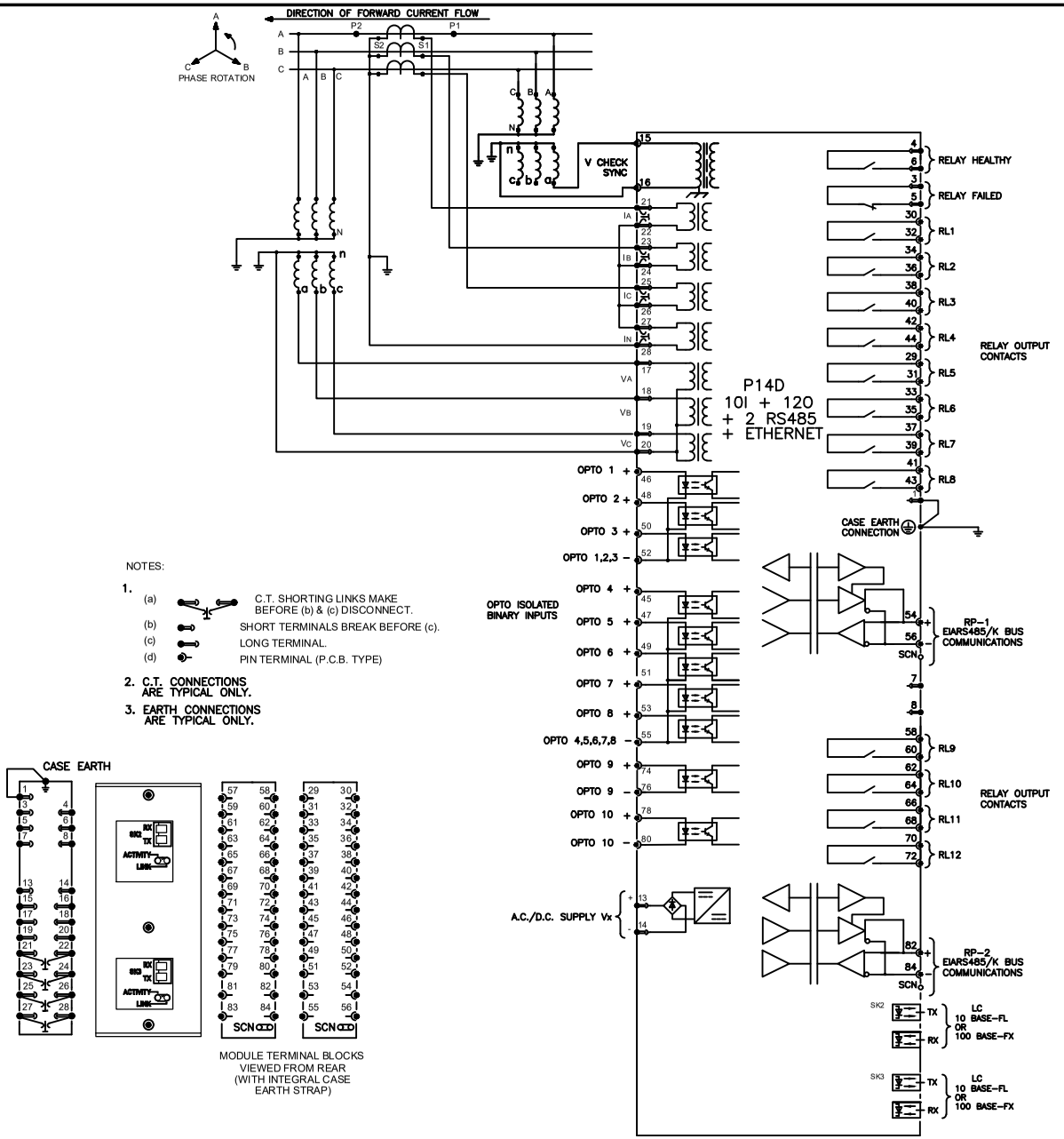

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (10 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D16	Sht: 4
Date:	Chkd: TEOH C.P.			Next Sht: -

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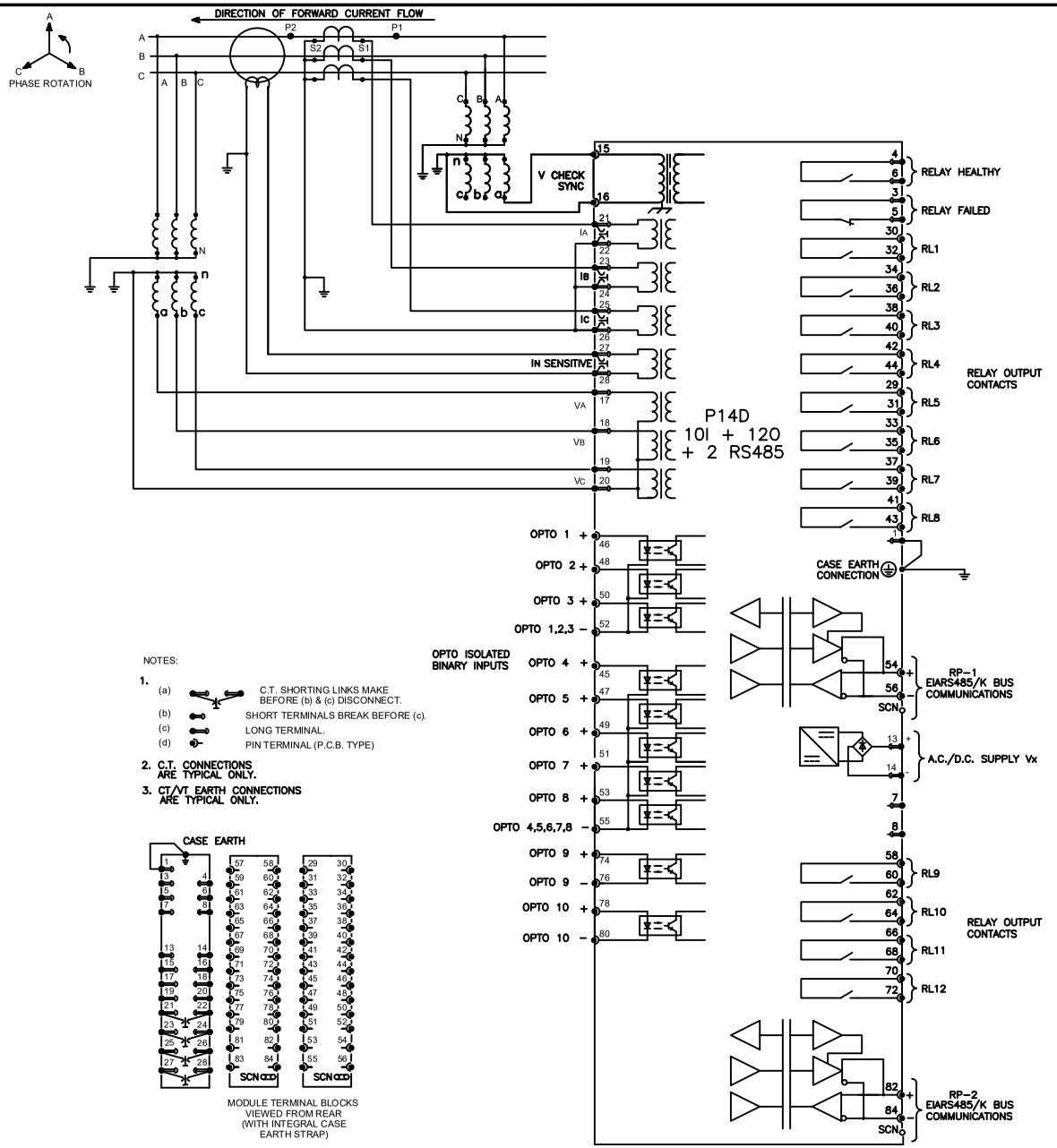

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D17	Sht: 1	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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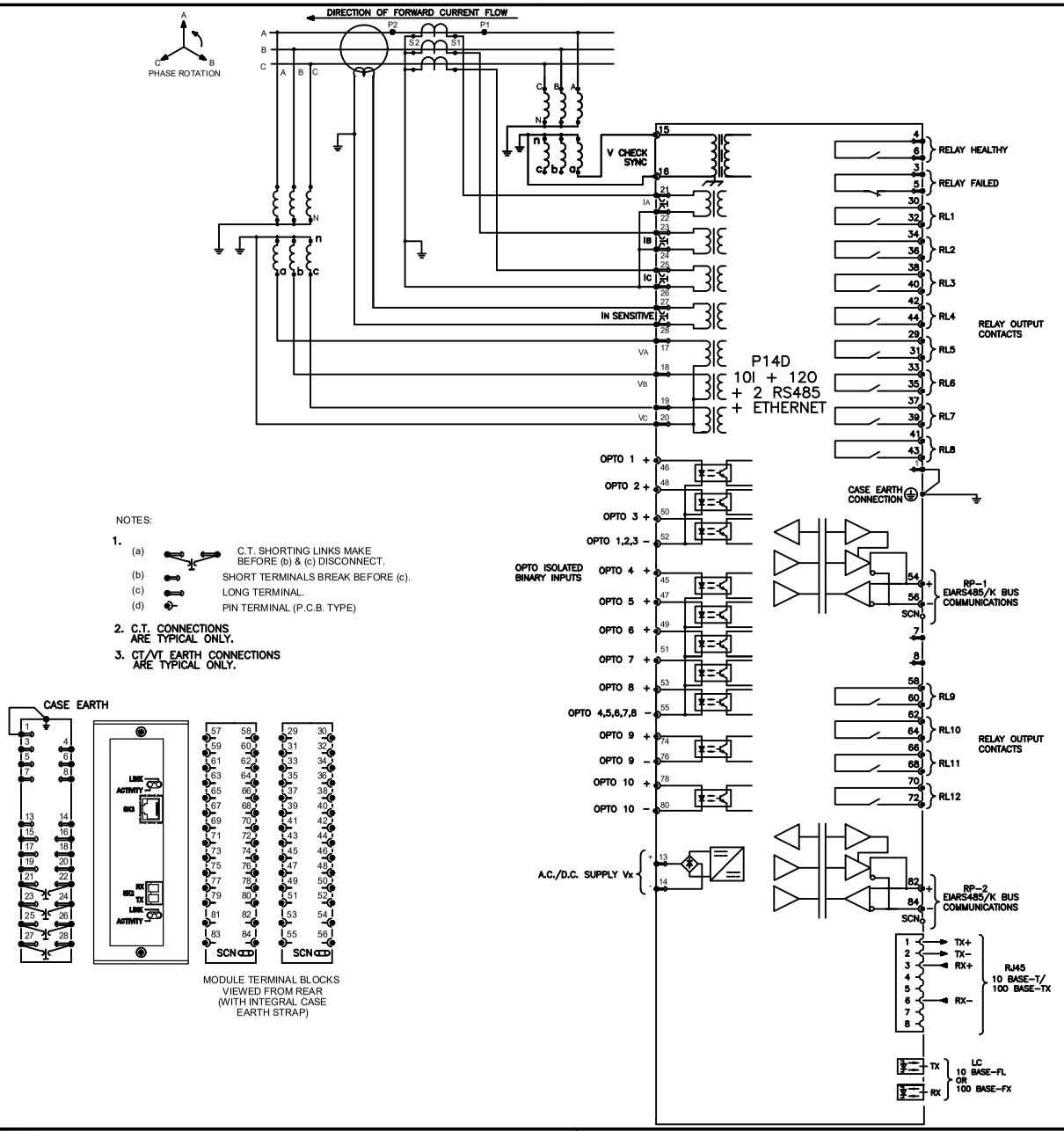

NOTES:

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MODULE TERMINAL BLOCKS VIEWED FROM REAR (WITH INTEGRAL CASE EARTH STRAP)

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 & ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D17	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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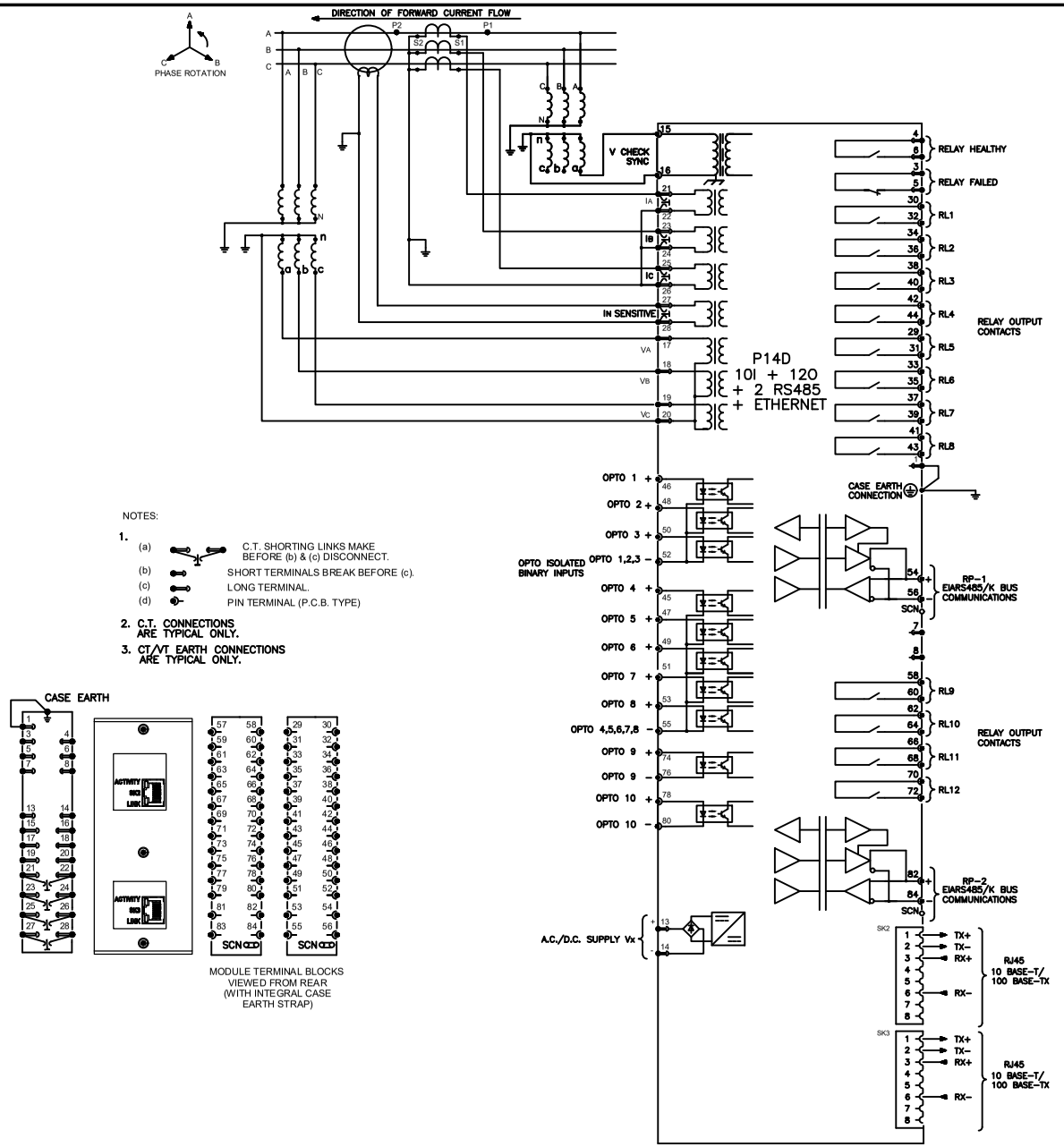

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 & DUAL COPPER ETHERNET	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D17	Sht: 3
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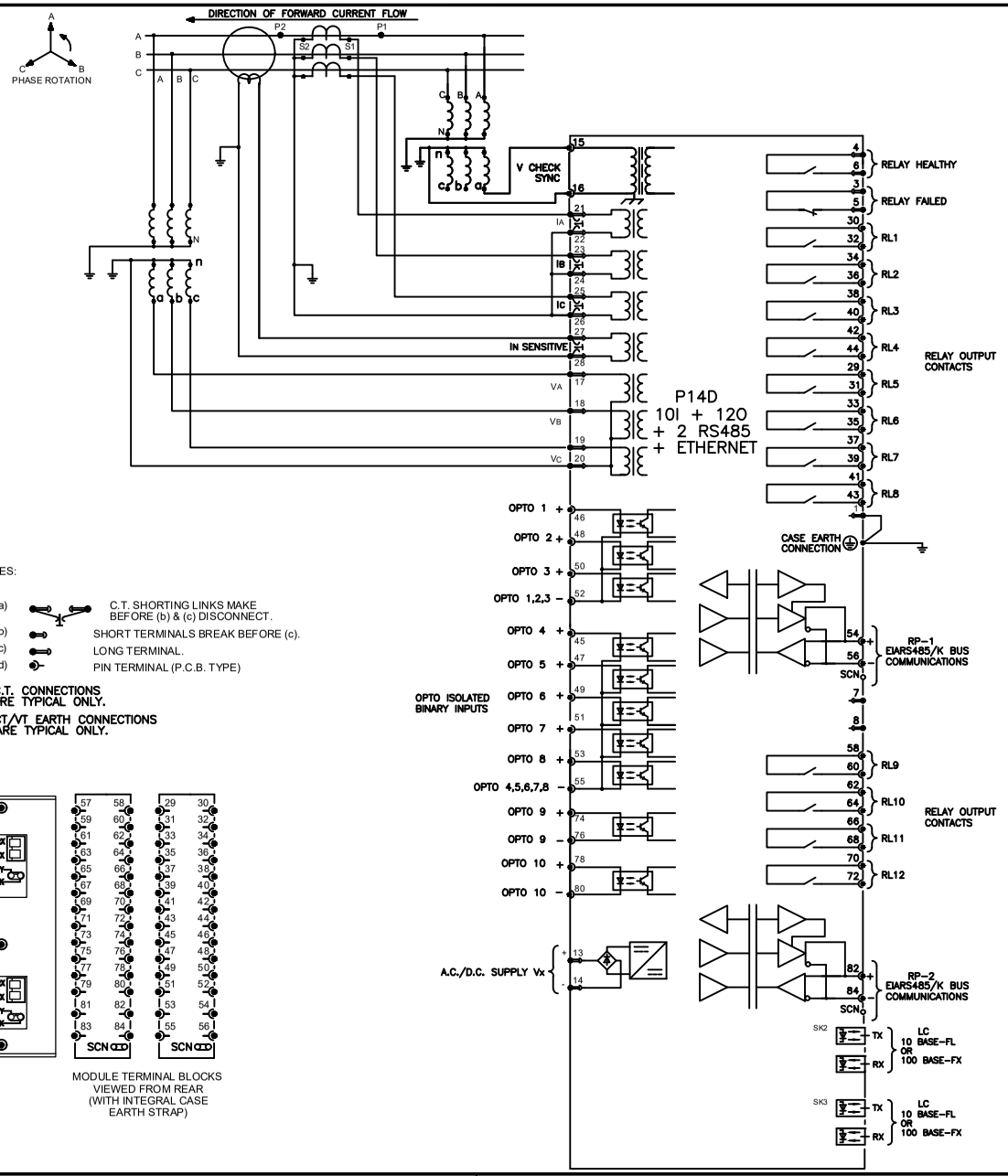

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & SEF (10 I/P & 12 O/P) WITH 2 RS485 & DUAL FIBRE ETHERNET	
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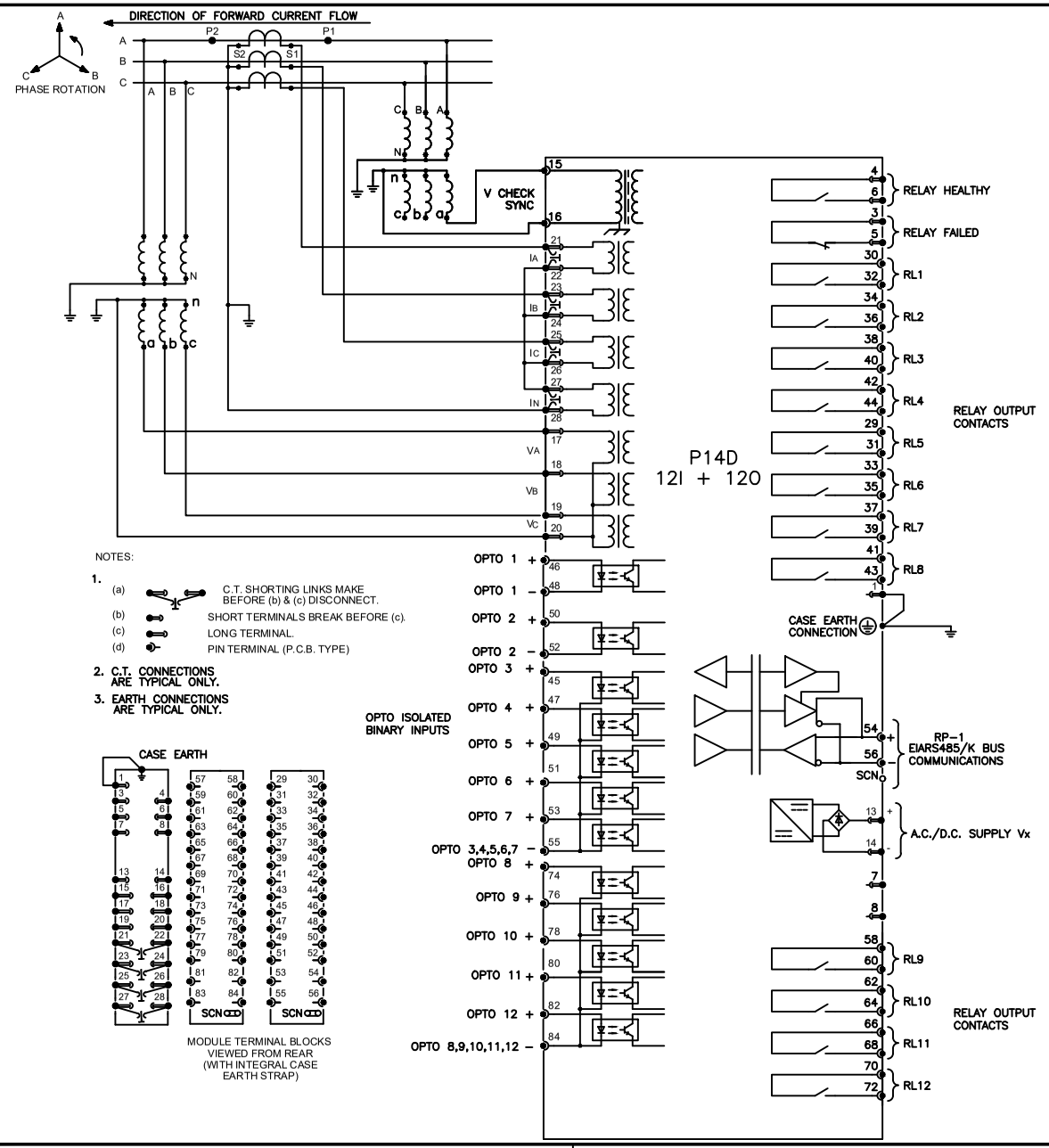

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (12 I/P & 12 O/P)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D18	Sht: 1	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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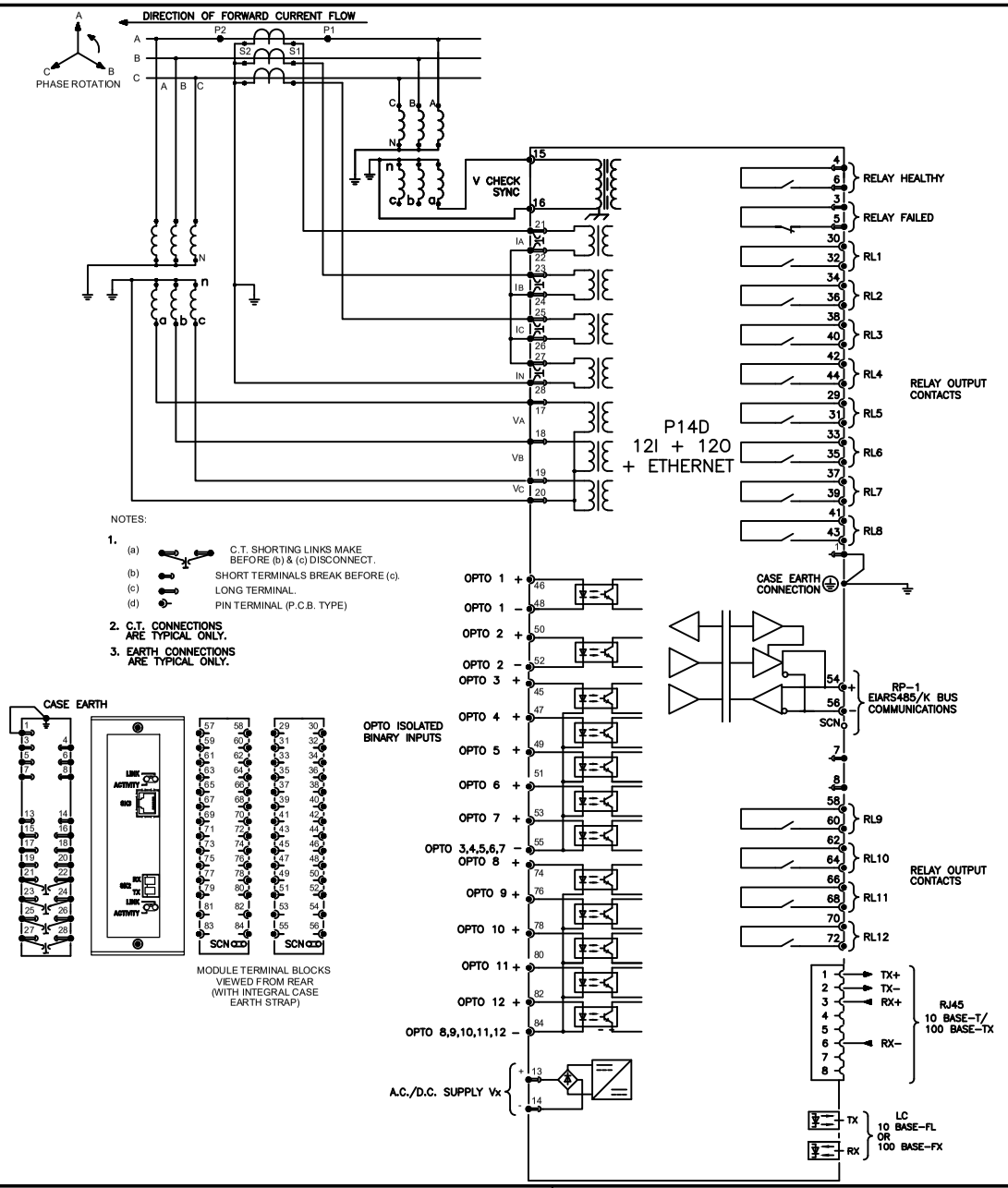

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (12 I/P & 12 O/P) & ETHERNET		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P14D18	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
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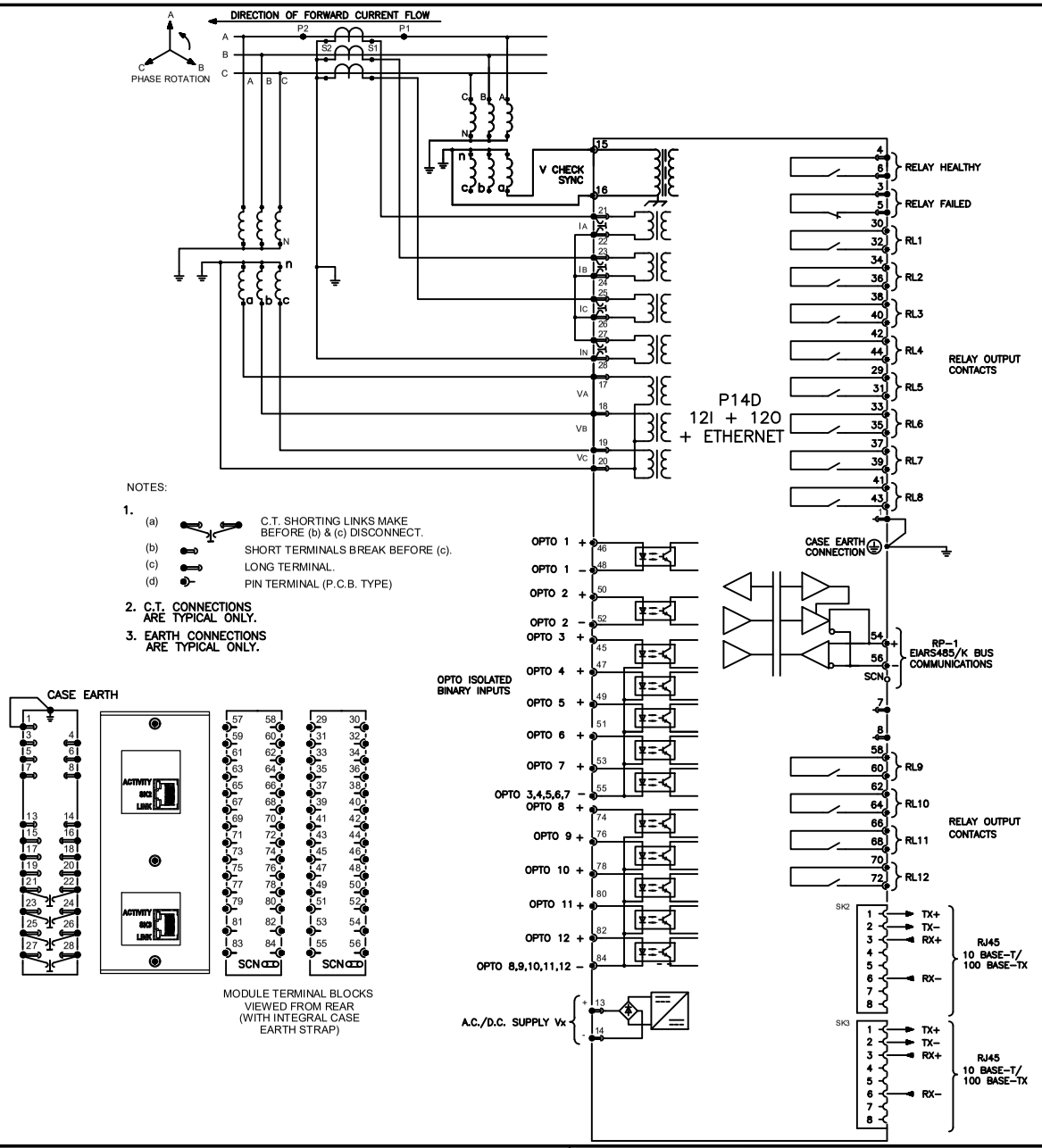

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (12 I/P & 12 O/P) & DUAL COPPER ETHERNET	
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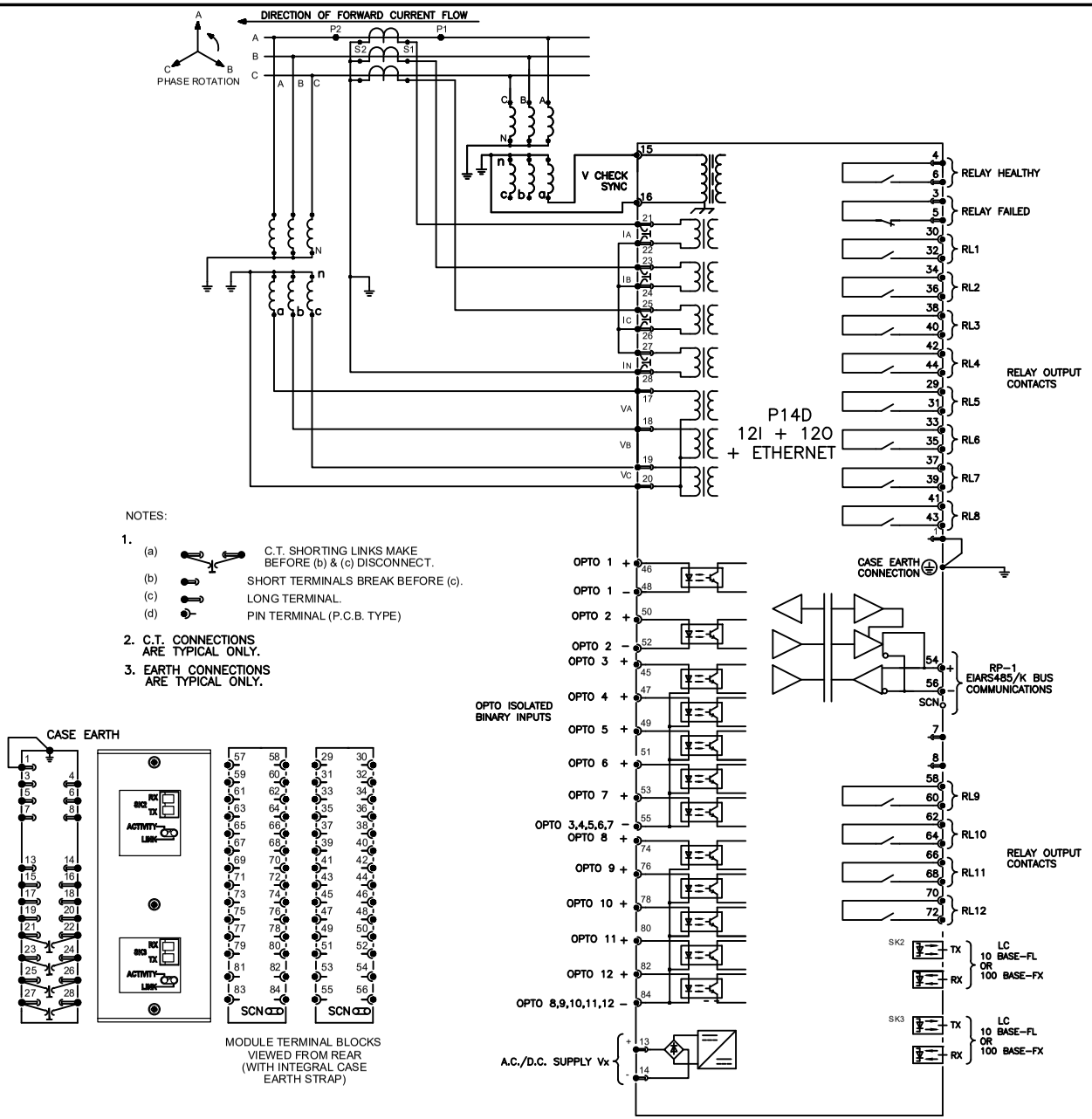

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT & EARTH FAULT (12 I/P & 12 O/P) & DUAL FIBRE ETHERNET	
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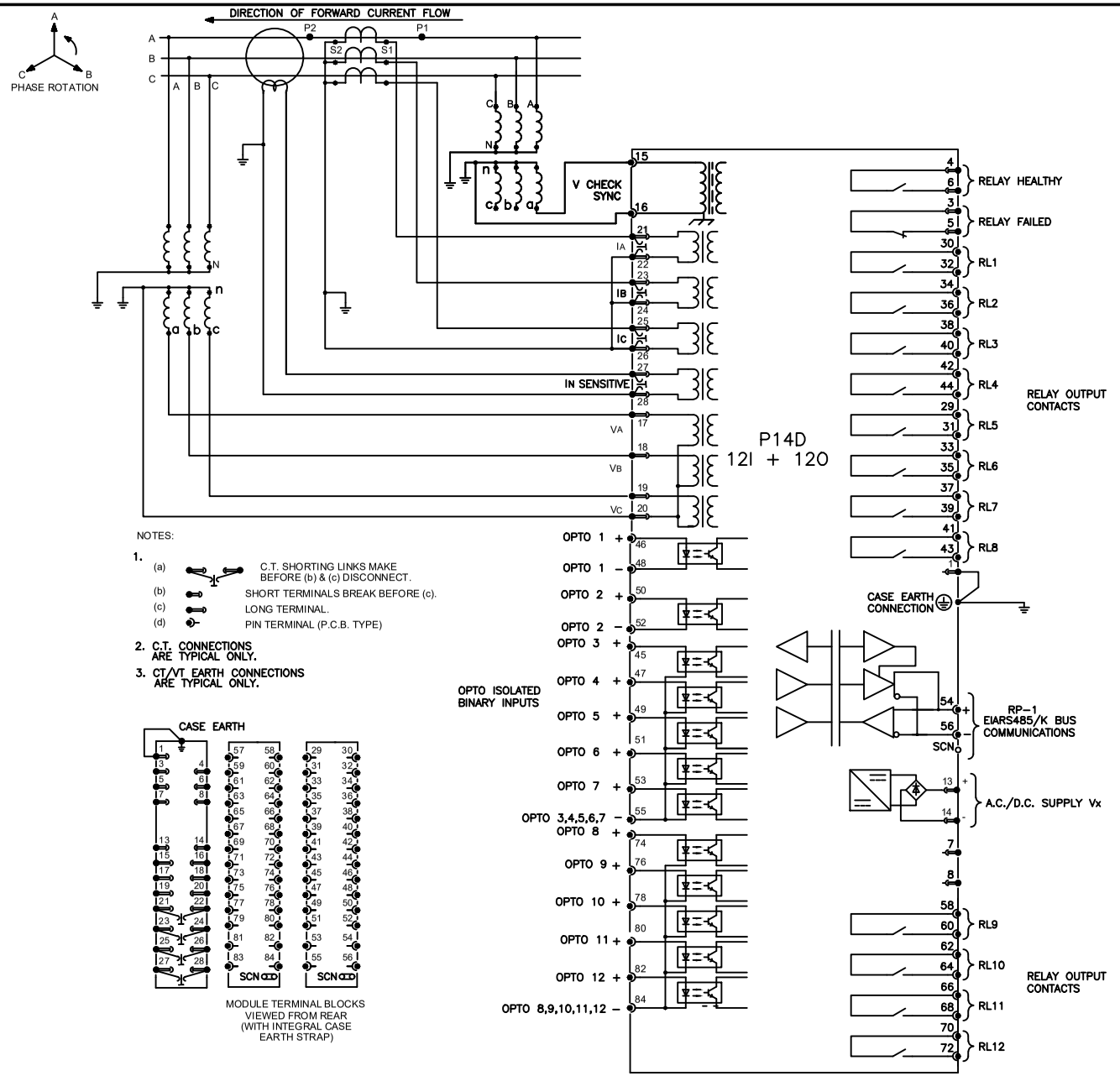

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MODULE TERMINAL BLOCKS VIEWED FROM REAR (WITH INTEGRAL CASE EARTH STRAP)

Issue: C	Revision: CID006234 Outlines updated to GE Format	Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (12 I/P & 12 O/P)	
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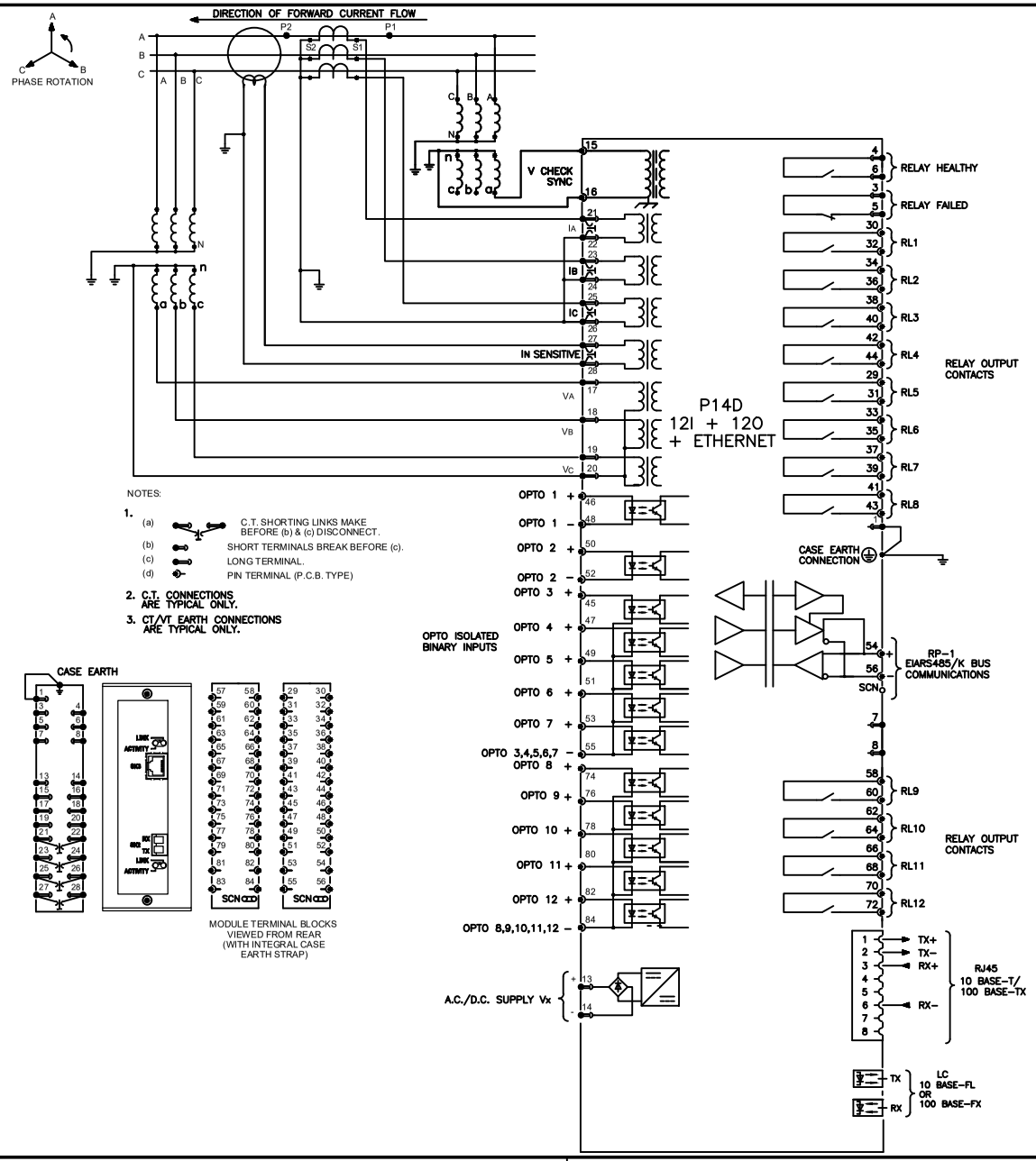

Issue: C	Revision: CID006234 Outlines updated to GE Format		Title: P14D DIRECTIONAL PHASE OVERCURRENT AND SEF (12 I/P & 12 O/P) & ETHERNET		
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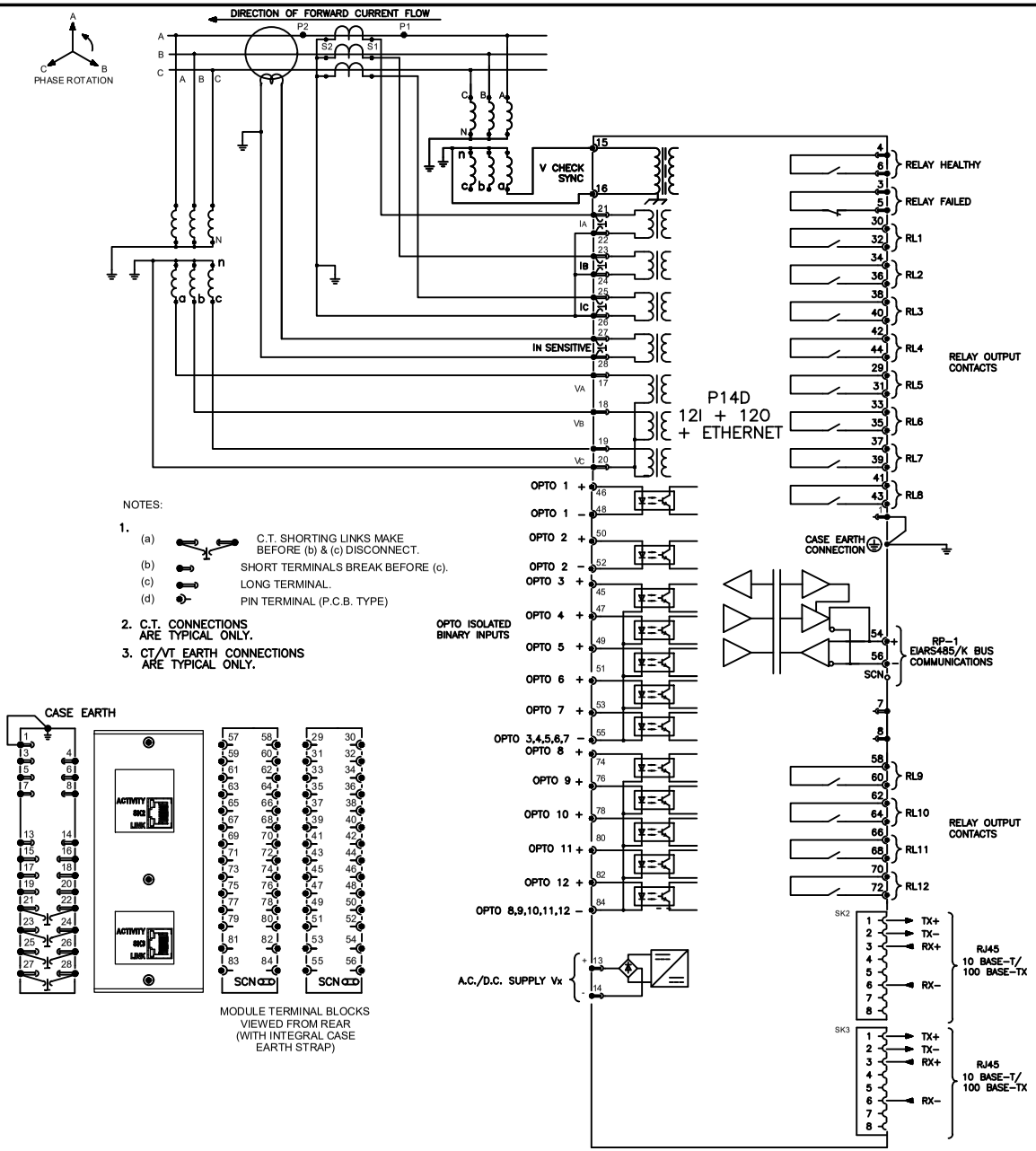

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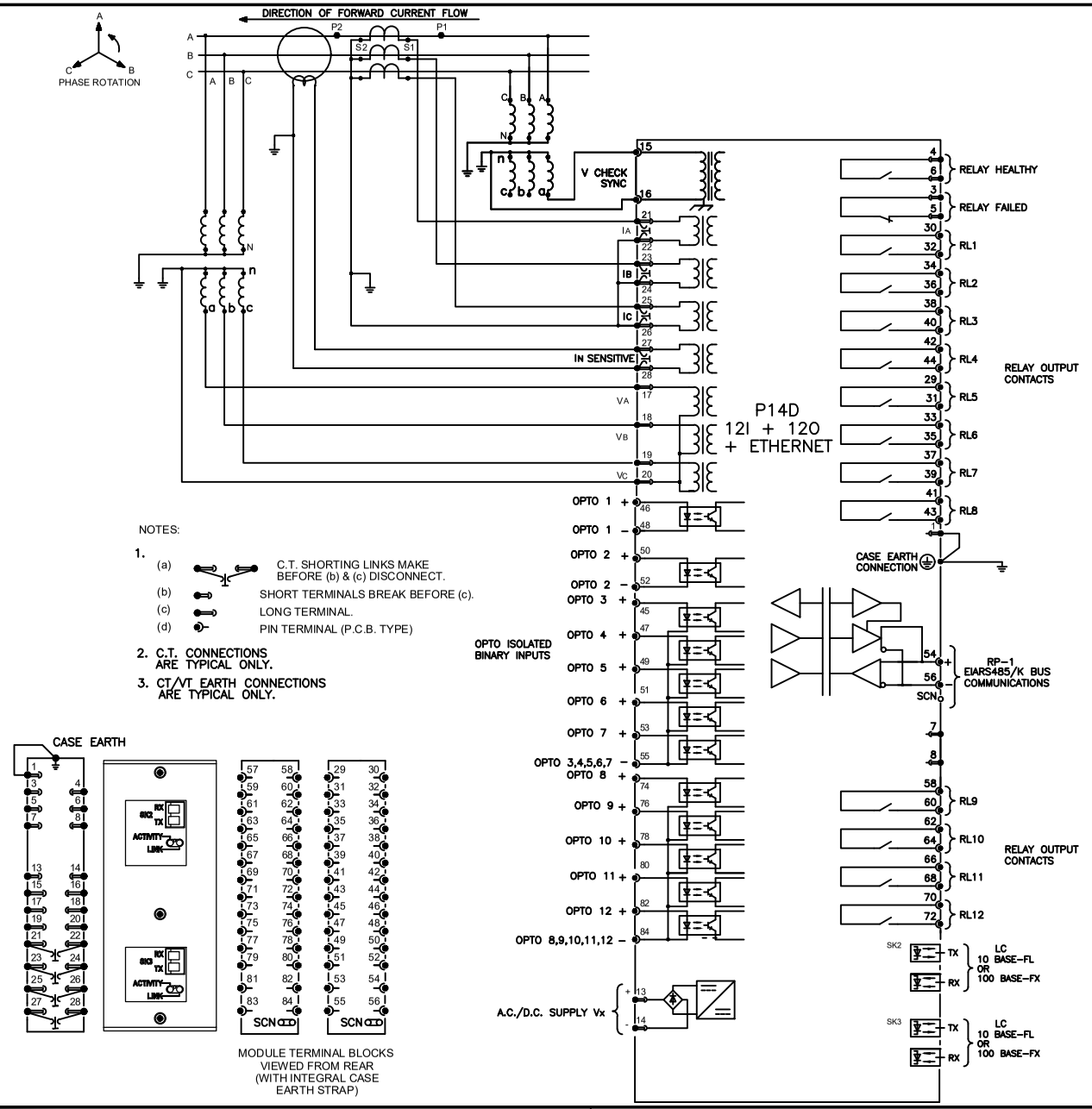

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